Modeling and Control of a Zeta Converter

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***Abstract*--A Zeta converter is a fourth-order DC-DC converter made up of two inductors and two capacitors and capable of operating in either step-up or step-down mode. Compared with other converters in the same class, such as Cuk and SEPIC converters, the Zeta converter has received the least attention, and more importantly, its dynamic modeling and control have never been reported before in the literature. This paper presents dynamic modeling and control of a Zeta converter operating in Continuous Conduction Mode (CCM). The State-Space Averaging (SSA) technique is applied to find small-signal linear dynamic model of the converter and its various transfer functions. Based on the derived control-to-output transfer function, the PWM feedback controller is designed to regulate the output voltage. Results show that the converter exhibits good performance in steady state and during a step-load change.**

***Index Terms*--Modeling, Zeta converter, SSA technique, Averaged switch model, PWM-switch model, PWM feedback control.**

I. Introduction

Nowadays, the use of a converter is widespread in modern portable electronic equipment and systems. In the battery-operated portable devices, when not connected to the AC mains, the battery provides an input voltage to the converter, which then converts it into the output voltage suitable for use by the electronic load. The battery voltage can vary over a wide range, depending on a charge level. At the low charge level, it may drop below the load voltage. Hence, to continue supplying the constant load voltage over the entire battery voltage range, the converter must be able to work in both buck and boost modes. The DC-DC converters that meet this operational requirement are Buck-boost, Cuk, SEPIC, and Zeta converters. However, the Buck-boost and Cuk converters, in their basic form, produce the output voltage, whose polarity is reversed from the input voltage [1, 2]. The problem can be corrected by incorporating an isolation transformer into the circuits, but this will inevitably lead to the increased size and cost of the converters. On the other hand, the SEPIC and Zeta converters are the fourth-order DC-DC converters capable of operating in both step-up and step-down modes and do not suffer from the polarity reversal problem. They are therefore attractive for the aforementioned application.

Recently, modeling of the SEPIC converter has been carried out by some researchers [3-6]. The linear converter models were derived by the substitution of the power switch and diode of the converter by the so-called small-signal PWM-switch model [7] or the so-called small-signal averaged switch model [2]. After the substitution, the resulting equivalent circuit was manipulated and reduced until the desired transfer function can be derived. Both the PWM-switch model and averaged switch model are a circuit-oriented approach of modeling the DC-DC converters.

Unlike SEPIC converter, modeling of a Zeta converter has never been performed and reported before in the literature. The Zeta converter is made up of an active power switch, a diode, two inductors, and two capacitors and is thus a fourth-order nonlinear system. A PWM feedback control loop is usually incorporated to regulate the converter's output voltage. To facilitate feedback control design or stability analysis, a linear model of the converter is needed. This paper presents modeling and control of a Zeta converter operating in Continuous Conduction Mode (CCM). The State-Space Averaging (SSA) technique [8] is applied to find small-signal linear dynamic model of the converter and its various transfer functions. As opposed to the PWM-switch model and averaged switch model, the SSA is a matrix-based approach in that all modeling steps in the SSA are performed systematically via matrices. Hence, mathematical software such as MATLAB can readily be used to aid the modeling process. Based on the control-to-output transfer function, the PWM feedback controller is designed to regulate an output voltage of the Zeta converter. This transfer function is found to have two pairs of the complex poles on the left half plane and a pair of the complex zeros which can locate either on the left or right half plane, depending on the circuit parameters. The Right-Half-Plane (RHP) zeros are undesirable because they cause extra 180 degrees phase-lag to the control-to-output transfer function. In this paper, conditions for selecting the converter parameters to ensure CCM operation and avoid RHP zeros are given.

II. Overview of SSA Technique

For DC-DC converters operating in Continuous Conduction Mode (CCM), there exist two circuit states within one switching period, T. One is when the MOSFET is turned on for an interval dT, and another is when the MOSFET is turned off for an interval $(1\text{-}d)T$, where d is a duty cycle. The state-space equations for these two circuit states are represented by:

$$\begin{cases} \dfrac{d\mathbf{x}(t)}{dt} = \mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}_1\mathbf{x}(t) + \mathbf{E}_1\mathbf{u}(t) \end{cases} \quad (1\text{-a})$$

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$$\begin{cases} \dfrac{d\mathbf{x}(t)}{dt} = \mathbf{A}_2\mathbf{x}(t) + \mathbf{B}_2\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}_2\mathbf{x}(t) + \mathbf{E}_2\mathbf{u}(t) \end{cases} \quad (1\text{-b})$$

To find the averaged behaviour of the converter over one switching period, equations (1-a) and (1-b) are weighed average by the duty cycle:

$$\begin{cases} \dfrac{d\mathbf{x}(t)}{dt} = \mathbf{A}_S < \mathbf{x}(t) > + \mathbf{B}_S < \mathbf{u}(t) > \\ \mathbf{y}(t) = \mathbf{C}_S < \mathbf{x}(t) > + \mathbf{E}_S < \mathbf{u}(t) > \end{cases} \quad (2)$$

where $\mathbf{A_S} = \mathbf{A_1}d + \mathbf{A_2}(1-d)$, $\mathbf{B_S} = \mathbf{B_1}d + \mathbf{B_2}(1-d)$, $\mathbf{C_S} = \mathbf{C_1}d + \mathbf{C_2}(1-d)$, and $\mathbf{E_S} = \mathbf{E_1}d + \mathbf{E_2}(1-d)$.

Note that variables in the bracket are the average value. Equation (2) is a nonlinear continuous-time equation. It can be linearized by small-signal perturbation with $<\mathbf{x}> = \mathbf{X} + \tilde{\mathbf{x}}$, $<\mathbf{y}> = \mathbf{Y} + \tilde{\mathbf{y}}$, $<\mathbf{u}> = \mathbf{U} + \tilde{\mathbf{u}}$, and $d = D + \tilde{d}$, where the letter with tilde symbol, ~, represents a small-signal value and the capital letter a DC value. It should be noted that $\mathbf{X} >> \tilde{\mathbf{x}}$, $\mathbf{Y} >> \tilde{\mathbf{y}}$, $\mathbf{U} >> \tilde{\mathbf{u}}$, and $D >> \tilde{d}$. The perturbation yields the steady-state and linear small-signal state-space equations in (3-a) and (3-b) respectively.

$$\begin{cases} \dfrac{d\mathbf{X}}{dt} = \mathbf{AX} + \mathbf{BU} = 0 \\ \mathbf{Y} = \mathbf{CX} + \mathbf{EU} \end{cases} \quad (3\text{-a})$$

$$\begin{cases} \dfrac{d\tilde{\mathbf{x}}(t)}{dt} = \mathbf{A}\tilde{\mathbf{x}}(t) + \mathbf{B}\tilde{\mathbf{u}}(t) + \mathbf{B_d}\tilde{d}(t) \\ \tilde{\mathbf{y}}(t) = \mathbf{C}\tilde{\mathbf{x}}(t) + \mathbf{E}\tilde{\mathbf{u}}(t) + \mathbf{E_d}\tilde{d}(t) \end{cases} \quad (3\text{-b})$$

where $\mathbf{A} = \mathbf{A_1}D + \mathbf{A_2}(1-D)$, $\mathbf{B} = \mathbf{B_1}D + \mathbf{B_2}(1-D)$, $\mathbf{C} = \mathbf{C_1}D + \mathbf{C_2}(1-D)$, $\mathbf{E} = \mathbf{E_1}D + \mathbf{E_2}(1-D)$, $\mathbf{B_d} = (\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})\mathbf{U}$, and $\mathbf{E_d} = (\mathbf{C_1} - \mathbf{C_2})\mathbf{X} + (\mathbf{E_1} - \mathbf{E_2})\mathbf{U}$.

The steady-state solution of the converter can be found by solving (3-a), which gives:

$$\begin{cases} \mathbf{X} = -\mathbf{A}^{-1}\mathbf{BU} \\ \mathbf{Y} = (-\mathbf{CA}^{-1}\mathbf{B} + \mathbf{E})\mathbf{U} \end{cases} \quad (4)$$

The small-signal transfer functions of the converter can be found by applying Laplace transform to (3-b). In a matrix form, we get:

$$\begin{cases} \tilde{\mathbf{x}}(s) = \begin{bmatrix} (s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B} & (s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d} \end{bmatrix} \begin{bmatrix} \tilde{\mathbf{u}}(s) \\ \tilde{d}(s) \end{bmatrix} \\ \tilde{\mathbf{y}}(s) = \begin{bmatrix} \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B} + \mathbf{E} & \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d} + \mathbf{E_d} \end{bmatrix} \begin{bmatrix} \tilde{\mathbf{u}}(s) \\ \tilde{d}(s) \end{bmatrix} \end{cases} \quad (5)$$

The input variable $\tilde{\mathbf{u}}$ usually contains the input voltage and load current. Hence, $\tilde{\mathbf{u}}$ can be expressed as $\tilde{\mathbf{u}}=[u_1\ u_2]^T$, the matrix $\mathbf{B}$ as $\mathbf{B}=[\mathbf{B_{u1}}\ \mathbf{B_{u2}}]$, and the matrix $\mathbf{E}$ as $\mathbf{E}=[\mathbf{E_{u1}}\ \mathbf{E_{u2}}]$. Therefore, equation (5) becomes:

$$\begin{cases} \tilde{\mathbf{x}}(s) = \begin{bmatrix} (s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u1}} \\ (s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u2}} \\ (s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d} \end{bmatrix}^T \begin{bmatrix} \tilde{u}_1(s) \\ \tilde{u}_2(s) \\ \tilde{d}(s) \end{bmatrix} \\ \tilde{\mathbf{y}}(s) = \begin{bmatrix} \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u1}} + \mathbf{E_{u1}} \\ \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u2}} + \mathbf{E_{u2}} \\ \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d} + \mathbf{E_d} \end{bmatrix}^T \begin{bmatrix} \tilde{u}_1(s) \\ \tilde{u}_2(s) \\ \tilde{d}(s) \end{bmatrix} \end{cases} \quad (6)$$

For the fourth-order converters, $(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u1}}$, $(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u2}}$, and $(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d}$ are the matrices that have four rows and one column. So, equation (6) can be expanded into:

$$\begin{cases} \tilde{\mathbf{x}}(s) = \begin{bmatrix} G_{vi_1}(s) & G_{zi_1}(s) & G_{di_1}(s) \\ G_{vi_2}(s) & G_{zi_2}(s) & G_{di_2}(s) \\ G_{vv_1}(s) & G_{zv_1}(s) & G_{dv_1}(s) \\ G_{vv_2}(s) & G_{zv_2}(s) & G_{dv_2}(s) \end{bmatrix} \begin{bmatrix} \tilde{u}_1(s) \\ \tilde{u}_2(s) \\ \tilde{d}(s) \end{bmatrix} \\ \tilde{\mathbf{y}}(s) = \begin{bmatrix} G_{vv}(s) & G_{zv}(s) & G_{dv}(s) \end{bmatrix} \begin{bmatrix} \tilde{u}_1(s) \\ \tilde{u}_2(s) \\ \tilde{d}(s) \end{bmatrix} \end{cases} \quad (7)$$

where $G_{vi_1}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u1}}]_{11}$, $G_{zi_1}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u2}}]_{11}$,

$G_{di_1}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d}]_{11}$, $G_{vi_2}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u1}}]_{21}$,

$G_{zi_2}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u2}}]_{21}$, $G_{di_2}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d}]_{21}$,

$G_{vv_1}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u1}}]_{31}$, $G_{zv_1}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u2}}]_{31}$,

$G_{dv_1}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d}]_{31}$, $G_{vv_2}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u1}}]_{41}$,

$G_{zv_2}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u2}}]_{41}$, $G_{dv_2}(s) = [(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d}]_{41}$,

$G_{vv}(s) = \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u1}} + \mathbf{E_{u1}}$, $G_{zv}(s) = \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_{u2}} + \mathbf{E_{u2}}$, and

$G_{dv}(s) = \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B_d} + \mathbf{E_d}$.

III. Modeling of ZETA Converter by SSA Technique

A Zeta converter is shown in Fig. 1(a). It is comprised of the MOSFET switch (*Q*), diode (*D*), two capacitors (C_1 and C_2), and two inductors (L_1 and L_2). The resistor, *R*, represents a standing load, and the current source, I_Z, the load current. The resistors, r_{C1}, r_{C2}, r_{L1}, and r_{L2}, are Equivalent Series Resistances (ESRs) of the capacitors and inductors respectively. Their values are usually very small, compared to *R*. In the ideal converter, these ESRs are zero. In CCM, the converter exhibits two circuit states. The first state is when the MOSFET switch is turned on (Fig. 1(b)). During this interval (*dT*), the inductors L_1 and L_2 are in a charging phase; hence, i_{L1} and i_{L2} increase linearly as shown in Fig. 2. The second state is when the MOSFET switch is turned off (Fig. 1(c)). During this interval ((1-*d*)*T*), L_1 and L_2 are in a discharging phase; that is, L_1 discharges the stored energy to C_1, and L_2 releases the stored energy to output section. Thus, i_{L1} and i_{L2} decrease linearly as depicted in Fig. 2.

The output voltage, V_O, is a DC voltage with small ripple due to the switching action. For the ideal Zeta

converter, the relationship between V_O and V_g is given by

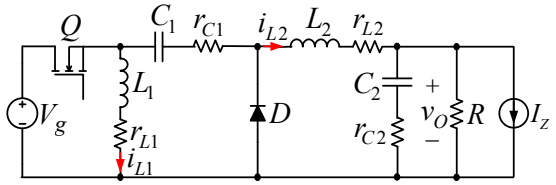
$$M=\frac{V_O}{V_g}=\frac{d}{1-d} \tag{8}$$

where M is a voltage conversion ratio. It can be seen that V_O could be larger or smaller than V_g, depending on the duty cycle. From Fig. 2, the averaged inductor currents, I_{L1} and I_{L2}, must be greater than one-half of their ripple components, Δi_{L1} and Δi_{L2}, for the circuit to operate in CCM. It can be shown that for CCM operation the values of L_1 and L_2 must satisfy the following conditions:

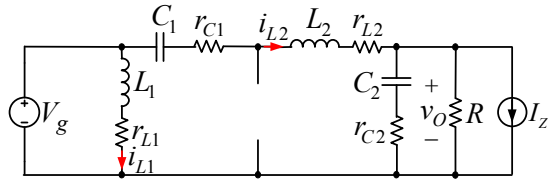
$$\begin{cases} L_1>\dfrac{(1-D)^2R}{2Df}\left(1+\dfrac{r_{L2}}{R}+\dfrac{r_{C1}}{R}\dfrac{D}{1-D}\right) \\ L_2>\dfrac{(1-D)R}{2f}\left(1+\dfrac{r_{L2}}{R}\right) \end{cases} \tag{9}$$

A. State-Space Description of Zeta Converter

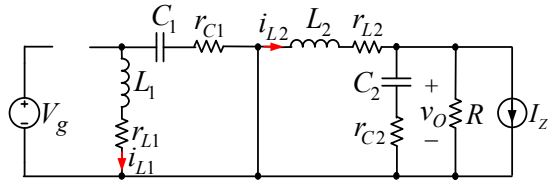
The state-space equations of the Zeta converter for the on and off states of the switch can be written from Fig. 1(b) and Fig. 1(c) respectively.



(a) Zeta converter.

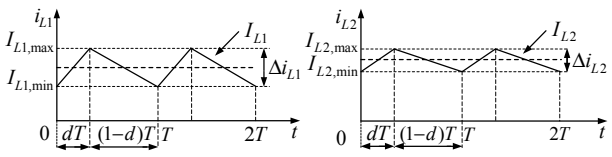


(b) Zeta converter when Q is turned on.



(c) Zeta converter when Q is turned off.

Fig. 1. Operation of Zeta converter in CCM.



(a) i_{L1} waveform. (b) i_{L2} waveform.

Fig. 2. Inductor current waveforms.

$$\begin{cases} \dfrac{di_{L1}}{dt}=\dfrac{r_{C1}}{L_1}(\delta-1)i_{L1}-\dfrac{r_{L1}}{L_1}+\dfrac{v_{C1}}{L_1}(\delta-1)+\dfrac{V_g}{L_1}\delta \\ \dfrac{di_{L2}}{dt}=\dfrac{-1}{L_2}\left(r_{L2}+r_{C1}\delta+\dfrac{r_{C2}R}{r_{C2}+R}\right)i_{L2}+\dfrac{v_{C1}}{L_2}\delta \\ \qquad -\dfrac{R}{L_2(r_{C2}+R)}v_{C2}+\dfrac{V_g}{L_2}\delta+\dfrac{r_{C2}R}{L_2(r_{C2}+R)}I_Z \\ \dfrac{dv_{C1}}{dt}=\dfrac{i_{L1}}{C_1}(1-\delta)-\dfrac{i_{L2}}{C_1}\delta \\ \dfrac{dv_{C2}}{dt}=\dfrac{R}{C_2(r_{C2}+R)}i_{L2}-\dfrac{1}{C_2(r_{C2}+R)}v_{C2}-\dfrac{R}{C_2(r_{C2}+R)}I_Z \\ v_O=\dfrac{r_{C2}R}{r_{C2}+R}i_{L2}+\dfrac{R}{r_{C2}+R}v_{C2}-\dfrac{r_{C2}R}{r_{C2}+R}I_Z \end{cases} \tag{10}$$

Note that equation (10) is expressed in a compact form using the switching function, δ. When the switch is on (δ=1), equation (10) will become the on-state equation. When the switch is off (δ=0), equation (10) will become the off-state equation.

The averaged matrices for the steady-state and linear small-signal state-space equations can be written according to (3-a) and (3-b).

$$\mathbf{A}=\begin{bmatrix} -\dfrac{r_{C1}(1-D)+r_{L1}}{L_1} & 0 & -\dfrac{1-D}{L_1} & 0 \\ 0 & -\dfrac{(r_{C2}+R)(Dr_{C1}+r_{L2})+r_{C2}R}{L_2(r_{C2}+R)} & \dfrac{D}{L_2} & \dfrac{-R}{L_2(r_{C2}+R)} \\ \dfrac{1-D}{C_1} & \dfrac{-D}{C_1} & 0 & 0 \\ 0 & \dfrac{R}{C_2(r_{C2}+R)} & 0 & \dfrac{-1}{C_2(r_{C2}+R)} \end{bmatrix} \tag{11-a}$$

$$\mathbf{B}=\begin{bmatrix} \dfrac{D}{L_1} & 0 \\ \dfrac{D}{L_2} & \dfrac{r_{C2}R}{L_2(r_{C2}+R)} \\ 0 & 0 \\ 0 & \dfrac{-R}{C_2(r_{C2}+R)} \end{bmatrix} \tag{11-b}$$

$$\mathbf{C}=\begin{bmatrix} 0 & \dfrac{r_{C2}R}{r_{C2}+R} & 0 & \dfrac{r_{C2}R}{r_{C2}+R} \end{bmatrix} \tag{11-c}$$

$$\mathbf{E}=\begin{bmatrix} 0 & \dfrac{-r_{C2}R}{r_{C2}+R} \end{bmatrix} \tag{11-d}$$

$$\mathbf{B}_d=\frac{\eta}{R(1-D)^2}\begin{bmatrix} \dfrac{1}{L_1}[V_g[(1-D)(R+r_{L2})+Dr_{C1}]-I_ZDr_{L1}R] \\ \dfrac{1}{L_2}[V_g(r_{L2}+R)(1-D)-[r_{C1}(1-D)+Dr_{L1}]RI_Z] \\ \dfrac{-1}{C_1}[DV_g+RI_Z(1-D)] \\ 0 \end{bmatrix} \tag{11-e}$$

$$\mathbf{E}_d=[0] \tag{11-f}$$

B. Steady-Stage Equations

Given the averaged matrices in (11-a) to (11-d), steady-state solutions of the converter is obtained from (4).

$$\begin{cases}\begin{bmatrix}I_{L1}\\ I_{L2}\\ V_{C1}\\ V_{C2}\end{bmatrix}=M\eta\begin{bmatrix}\frac{D}{R(1-D)} & 1\\ \frac{1}{R} & \frac{1}{M}\\ 1+\frac{r_{L2}}{R}-\frac{r_{L1}}{R}M & -(r_{C1}+r_{L1}\frac{1}{1-D})\\ 1 & -(r_{C1}+r_{L1}M+r_{L2}\frac{1}{M})\end{bmatrix}\begin{bmatrix}V_g\\ I_Z\end{bmatrix}\\ V_O=[V_g-I_Z(r_{C1}+r_{L1}M+r_{L2}\frac{1}{M})]M\eta\end{cases} \quad (12)$$

where $\eta=\dfrac{1}{1+\frac{r_{L2}}{R}+\frac{r_{L1}}{R}M^2+\frac{r_{C1}}{R}M}$, and $M=\dfrac{D}{1-D}$.

Note that if r_{C1}, r_{C2}, r_{L1}, and r_{L2} are assumed to be zero, equation (12) will be reduced to $M=V_O/V_g=D/(1-D)$, the same as the expression for the ideal Zeta converter in (8).

C. Linear Small-Signal State-Space Equations

Given the averaged matrices (11-a) to (11-f), the linear small-signal state-space equations of the Zeta converter can be formulated in accordance with (3-b):

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_{L1}(t)\\ \tilde{i}_{L2}(t)\\ \tilde{v}_{C1}(t)\\ \tilde{v}_{C2}(t)\end{bmatrix}=\begin{bmatrix}-\frac{r_{C1}(1-D)+r_{L1}}{L_1} & 0 & -\frac{1-D}{L_1} & 0\\ 0 & -\frac{(r_{C2}+R)(Dr_{C1}+r_{L2})+r_{C2}R}{L_2(r_{C2}+R)} & \frac{D}{L_2} & \frac{-R}{L_2(r_{C2}+R)}\\ \frac{1-D}{C_1} & -\frac{D}{C_1} & 0 & 0\\ 0 & \frac{R}{C_2(r_{C2}+R)} & 0 & \frac{-1}{C_2(r_{C2}+R)}\end{bmatrix}\begin{bmatrix}\tilde{i}_{L1}(t)\\ \tilde{i}_{L2}(t)\\ \tilde{v}_{C1}(t)\\ \tilde{v}_{C2}(t)\end{bmatrix}$$
$$+\begin{bmatrix}\frac{D}{L_1} & 0 & \frac{\eta[V_g[(1-D)(R+r_{L2})+Dr_{C1}]-I_ZDr_{L1}R]}{L_1R(1-D)^2}\\ \frac{D}{L_2} & \frac{r_{C2}R}{L_2(r_{C2}+R)} & \frac{\eta[V_g(r_{L2}+R)(1-D)-I_ZR[r_{C1}(1-D)+Dr_{L1}]]}{L_2R(1-D)^2}\\ 0 & 0 & \frac{-\eta[DV_g+RI_Z(1-D)]}{C_1R(1-D)^2}\\ 0 & -\frac{R}{C_2(r_{C2}+R)} & 0\end{bmatrix}\begin{bmatrix}\tilde{v}_g(t)\\ \tilde{i}_Z(t)\\ \tilde{d}(t)\end{bmatrix} \quad (13)$$

$$\tilde{v}_O(t)=\begin{bmatrix}0 & \frac{r_{C2}R}{r_{C2}+R} & 0 & \frac{r_{C2}R}{r_{C2}+R}\end{bmatrix}\begin{bmatrix}\tilde{i}_{L1}(t)\\ \tilde{i}_{L2}(t)\\ \tilde{v}_{C1}(t)\\ \tilde{v}_{C2}(t)\end{bmatrix}+\begin{bmatrix}0 & \frac{-r_{C2}R}{r_{C2}+R} & 0\end{bmatrix}\begin{bmatrix}\tilde{v}_g(t)\\ \tilde{i}_Z(t)\\ \tilde{d}(t)\end{bmatrix}$$

D. Finding Transfer Functions

Referring to (7), fifteen transfer functions can be determined from (13). However, only the expressions of some common transfer functions are derived here. These transfer functions are:

The duty ratio-to-output voltage transfer function

$$G_{dv}(s)=\frac{\tilde{v}_O(s)}{\tilde{d}(s)}=\mathbf{C(sI-A)^{-1}B_d+E_d}=\frac{\eta}{(1-D)^2}\frac{(a_{dv}s^2+b_{dv}s+c_{dv})(d_{dv}s+1)}{as^4+bs^3+cs^2+ds+e} \quad (14\text{-a})$$

The input voltage-to-output voltage transfer function

$$G_{vv}(s)=\frac{\tilde{v}_O(s)}{\tilde{v}_g(s)}=\mathbf{C(sI-A)^{-1}B_{u1}+E_{u1}}=DR\frac{(a_{vv}s^2+b_{vv}s+c_{vv})(d_{vv}s+1)}{as^4+bs^3+cs^2+ds+e} \quad (14\text{-b})$$

The output impedance transfer function

$$G_{zv}(s)=\frac{\tilde{v}_O(s)}{\tilde{i}_Z(s)}=\mathbf{C(sI-A)^{-1}B_{u2}+E_{u2}}=-R\frac{(a_{zv}s^2+b_{zv}s+c_{zv})(d_{zv}s+1)}{as^4+bs^3+cs^2+ds+e} \quad (14\text{-c})$$

The coefficients in (14-a) to (14-c) are listed in TABLE I.

IV. Control of ZETA Converter

A. Description of PWM Feedback Control

Fig. 3(a) shows of a Zeta converter with PWM feedback control. The output voltage, V_O, is fed back and compared with the reference voltage, V_{ref}. The resulting error voltage is processed by a compensator, $G_C(s)$, which produces the control voltage, v_C, to compare with the sawtooth voltage, v_{saw}, at the PWM comparator. As depicted in Fig. 3(b), the MOSFET is turned on when v_C is larger than v_{saw}, and turned off when v_C is smaller than v_{saw}. If V_O is changed, feedback control will respond by adjusting v_C and the duty cycle of the MOSFET until V_O is again equal to V_{ref}.

TABLE I
Coefficients of $G_{DV}(s)$, $G_{VV}(s)$, and $G_{ZV}(s)$

$a_{dv}=L_1C_1[V_g(1-D)(R+r_{L2})-I_ZR[(1-D)r_{C1}+Dr_{L1}]$ $b_{dv}=-V_g[L_1D^2-C_1(1-D)(R+r_{L2})[(1-D)r_{C1}+r_{L1}]]$ $-I_ZR[L_1D(1-D)+r_{C1}^2C_1(1-D)^2+r_{L1}C_1(r_{C1}+r_{L1}D-D^2r_{C1})]$, $c_{dv}=V_g[(1-D)^2(R+r_{L2})-D^2r_{L1}]-I_ZR(1-D)[2Dr_{L1}+r_{C1}(1-D)]$ $d_{dv}=C_2r_{C2}$
$a_{vv}=C_1L_1$, $b_{vv}=C_1[r_{L1}+r_{C1}(1-D)]$, $c_{vv}=1-D$, $d_{vv}=C_2r_{C2}$
$a_{zv}=L_1L_2C_1C_2r_{C2}$ $b_{zv}=L_1C_1(L_2+Dr_{C2}r_{C1}C_2)+(1-D)r_{C1}r_{C2}L_2C_1C_2$ $+(L_1r_{L2}+L_2r_{L1})r_{C2}C_1C_2$ $c_{zv}=(1-D)[(1-D)r_{C2}L_2C_2+r_{C1}C_1(L_2+Dr_{C1}r_{C2}C_2+r_{C2}r_{L2}C_2)]$ $+L_1D(Dr_{C2}C_2+r_{C1}C_1)+C_1[r_{L1}r_{C2}C_2(r_{C1}D+r_{L2})+r_{L1}L_2+r_{L2}L_1]$ $d_{zv}=L_1D^2+(1-D)[(1-D)(L_2+r_{C2}r_{L2}C_2)+Dr_{C1}(r_{C1}C_1+r_{C2}C_2)$ $+r_{C1}r_{L2}C_1]+r_{L1}(C_1r_{L2}+C_1Dr_{C1}+r_{C2}D^2C_2)$ $e_{zv}=r_{C1}D(1-D)+r_{L1}D^2+r_{L2}(1-D)^2$
$a=L_1C_1L_2C_2(R+r_{C2})$ $e=(1-D)^2(R+r_{L2})+r_{C1}D(1-D)+r_{L1}D^2$ $b=L_1C_1(L_2+r_{C2}C_2R)+C_1(R+r_{C2})[r_{C1}L_2C_2(1-D)+Dr_{C1}L_1C_2$ $+C_2(r_{L2}L_1+r_{L1}L_2)]$ $c=(1-D)[[(1-D)L_2+(Dr_{C1}+r_{L2})r_{C1}C_1](r_{C2}+R)C_2$ $+r_{C1}C_1(r_{C2}C_2R+L_2)]+C_2(r_{C2}+R)[L_1D^2+(Dr_{C1}+r_{L2})r_{L1}C_1]$ $+C_1[L_1(Dr_{C1}+R)+r_{L1}L_2+r_{L2}L_1+r_{L1}r_{C2}C_2R]$ $d=L_1D^2+(1-D)^2[L_2+r_{C2}C_2R+r_{L2}C_2(R+r_{C2})]+[r_{C1}(1-D)$ $+r_{L1}D](R+r_{C2})DC_2+[(1-D)r_{C1}+r_{L1}](r_{L2}+Dr_{C1}+R)C_1$

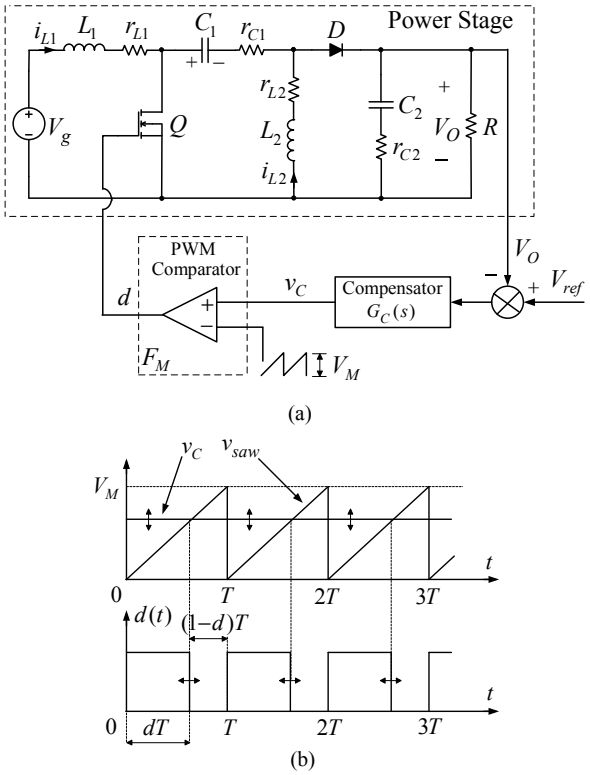


Fig. 3. (a) Zeta converter with PWM feedback control and (b) Waveforms of PWM comparator.

Fig. 4 illustrates a small-signal block diagram of the converter in Fig. 3(a). The power stage is represented by the three transfer functions: $G_{dv}(s)$, $G_{vv}(s)$, and $G_{zv}(s)$ derived in Section 3. The transfer function of the PWM comparator can be derived from the waveform in Fig. 3(b). It is given by:

$$F_M = \frac{\tilde{d}(s)}{\tilde{v}_C(s)} = \frac{1}{V_M} \tag{15}$$

where V_M is amplitude of the sawtooth voltage. From Fig. 4, the open-loop transfer function is defined as:

$$T(s) = G_C(s) G_{dv}(s) F_M \tag{16}$$

Given $G_{dv}(s)$ in (14-a) and F_M in (15), the compensator can be designed by appropriately selecting poles and zeros of $G_C(s)$ so that the open-loop transfer function in (16) has high DC gain, a reasonable value of crossover frequency, and sufficient amount of phase margin [9, 10].

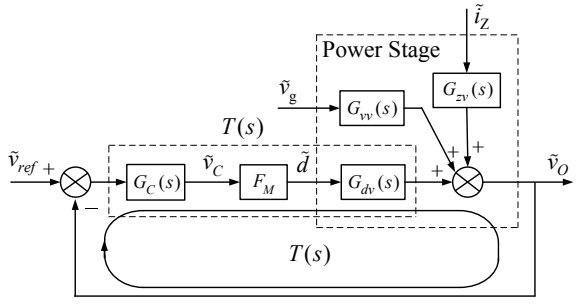


Fig. 4. Small-signal block diagram of Zeta converter with PWM feedback control.

Before proceeding to design the compensator, it is worthwhile to firstly examine the transfer function $G_{dv}(s)$ in (14-a), which has three zeros and four poles. Typically, these four poles are complex poles. It can be proved by the Routh-Hurwitz criterion [11] that these poles are located on the Left-Half Plane (LHP). Meanwhile, the $d_{dv}s+1$ term on the numerator of $G_{dv}(s)$ always gives the LHP zero since d_{dv} is positive. However, there is a possibility that the quadratic term, $a_{dv}s^2+b_{dv}s+c_{dv}$, on the numerator yields a pair of Right-Half-Plane (RHP) zeros. The RHP zeros are undesirable because they contribute additional 180 degrees phase-lag to $G_{dv}(s)$, making feedback loop compensation very difficult. In order to avoid the RHP zeros, the following condition must be satisfied:

$$s_{Z1,2} = \frac{-b_{dv} \pm \sqrt{b_{dv}^2 - 4a_{dv}c_{dv}}}{2a_{dv}} < 0 \tag{17}$$

That is:

$$\begin{cases} b_{dv}^2 < 4a_{dv}c_{dv} \\ b_{dv} > 0 \end{cases} \tag{18}$$

with $a_{dv} = L_1C_1V_g(1-D)(R+r_{L2})$, $c_{dv} = V_g[(1-D)^2(R+r_{L2}) - D^2r_{L1}]$, and $b_{dv} = -V_g[L_1D^2 - C_1(1-D)(R+r_{L2})][(1-D)r_{C1}+r_{L1}]]$.

Note that in the ideal converter where there is no ESRs, b_{dv} will be less than zero. Thus, $G_{dv}(s)$ of the ideal Zeta converter always exhibits RHP zeros.

B. Feedback-Loop Compensation

Table II lists circuit parameters of the Zeta converter. Fig. 5(a) shows Bode plot of $G_{dv}(s)$ expressed in (14-a). The plot depicts $G_{dv}(s)$ for the two extreme cases, with the solid line representing the operation at V_g=15V, R=1Ω and the dashed line at V_g=20V, R=5Ω. To ensure that $G_{dv}(s)$ in (14-a) is accurate, the results obtained from the averaged switch model and PWM-switch model are also presented in Fig. 5(b) and Fig. 5(c) for comparison. The results in Fig. 5(b) and Fig. 5(c) are generated by PSPICE simulation of a Zeta converter circuit having its active switch and diode replaced by averaged switch model and PWM switch model respectively. It can be seen that the three results are closely agreed, proving the accuracy of $G_{dv}(s)$ in (14-a).

Having shown that the derived $G_{dv}(s)$ is accurate, it can now be used in the compensator design. The following design assumes that the converter is operating with V_g=15V and R=1Ω. Substituting the relevant parameters from TABLE II into (14-a) and (15), the control-to-output transfer function, $T_U(s)=F_MG_{dv}(s)$, is given by:

$$T_U(s) = \frac{1.65\text{x}10^4 s^3 + 8.77\text{x}10^8 s^2 + 1.76\text{x}10^{12} s + 6.51\text{x}10^{16}}{s^4 + 8452s^3 + 1.65\text{x}10^8 s^2 + 5.88\text{x}10^{11} s + 4.97\text{x}10^{15}} \tag{19}$$

A PI compensator shown in Fig. 6 is selected to compensate $T_U(s)$ in (19). Its transfer function is given by

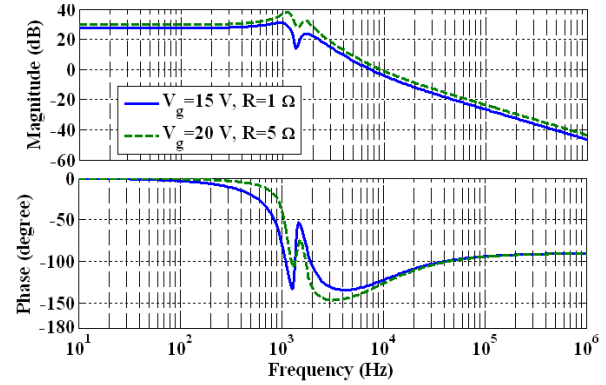
$$G_C(s) = \frac{z_2}{z_1} = \frac{\omega_O}{s}\left(\frac{s}{\omega_Z} + 1\right) \tag{20}$$

where $\omega_O=\frac{1}{R_2C_1}$ and $\omega_Z=\frac{1}{R_1C_1}$.

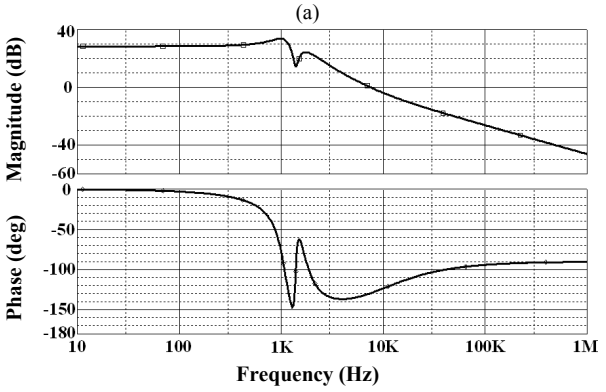
The pole at the origin helps increase the low frequency gain of the open-loop transfer function, $T(s)$. The zero, ω_Z, and gain, ω_O, can be tuned to give $T(s)$ the desirable crossover frequency and phase margin respectively.

TABLE II
CONVERTER PARAMETERS

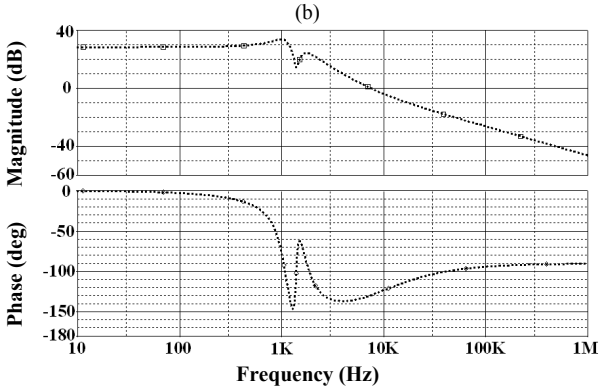
Circuit Parameters	Values
V_g/ V_O	15-20V/ 5V
R	1-5Ω
C_1/ C_2	100/ 200μF
r_{C1}/ r_{C2}	0.19/ 0.095Ω
L_1/ L_2	100/ 55μH
r_{L1}/ r_{L2}	1/ 0.55mΩ
V_M	1.8V
T=1/f	10μs



(a)



(b)



(c)

Fig. 5. Frequency responses of $G_{dv}(s)$: (a) SSA technique, (b) Averaged switch model (V_g=15V, R=1Ω), and (c) PWM-switch model (V_g=15V, R=1Ω).

In designing $G_C(s)$, the objective is to achieve $T(s)$ with the crossover frequency of 10 KHz and phase margin of at least 45 degrees. To accomplish this, the zero of $G_C(s)$ has been set at ω_Z=5x10^{3}rad/s and ω_O=1.47x10^{4}rad/s. Based on these values, PI compensator's component values are calculated, getting: R_1=10KΩ, R_2=3.4KΩ, and C_1=20nF. Substitution of the component values into (20) yields:

$$G_C(s)=\frac{1.47x10^4}{s}\left(\frac{s}{5x10^3}+1\right) \quad (21)$$

Fig. 7 illustrates Bode plots of $G_C(s)$ (dotted line), $T_U(s)$ (dashed line), and $T(s)$ (solid line) for V_g=15V and R=1Ω. It can be seen that $T(s)$ has a crossover frequency of 10 KHz and phase margin of 53.2 degrees, meeting the design objective. The designed compensator also works well in the case of V_g=20V and R=5Ω as shown in Fig. 8. The crossover frequency and phase margin are 13.1 KHz and 56.4 degrees respectively, satisfying the design objective.

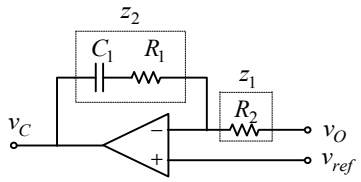


Fig. 6. PI compensator.

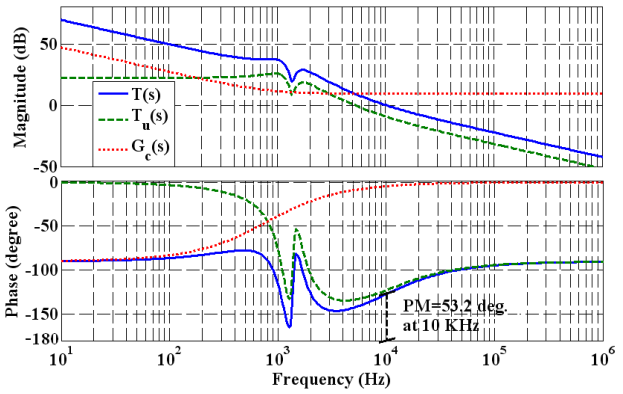


Fig. 7. Frequency responses of $G_C(s)$; $T_U(s)$; T(s) for V_g=15V, R=1Ω.

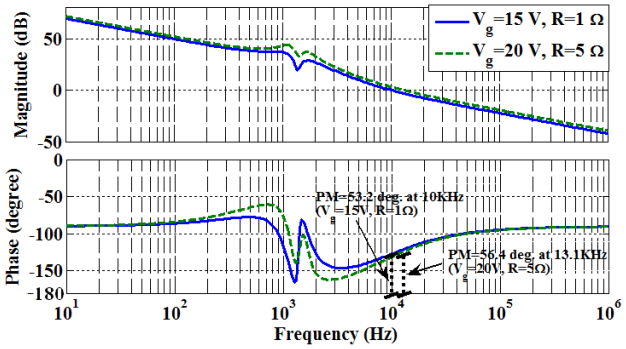


Fig. 8. Frequency responses of T(s) for V_g=15V, R=1Ω; and T(s) for V_g=20V, R=5Ω.

V. RESULTS

A prototype Zeta converter with PWM feedback control was built to verify the performance of the designed PI compensator. Specifications of the prototype circuit are as shown in TABLE II. Fig. 9 depicts waveforms of the drain-source voltage of the MOSFET switch, V_{DS}, and inductor currents, i_{L1} and i_{L2}, when V_g=15V, R=1.25Ω (I_o=4A). Apparently, both inductors are operating in continuous conduction mode. According to (12), the averaged inductor currents, I_{L1} and I_{L2}, are given by (neglecting ESRs):

$$\begin{cases} I_{L1} = \dfrac{D^2 V_g}{R(1-D)^2} \\ I_{L2} = \dfrac{D V_g}{R(1-D)} \end{cases} \tag{22}$$

Substituting D=0.25, V_g=15V, and R=1.25Ω in the above equations, I_{L1} = 1.33A and I_{L2} = 4A are obtained. These values correspond closely with the measured results in Fig. 9.

To determine its output regulation, the output voltage of the prototype Zeta converter was measured at different values of the input voltage and load current. The result is shown in TABLE III. It can be seen that the output voltage is regulated close to 5V throughout the entire operating range of the converter. The output voltage regulation (VR) is defined as:

$$VR = \frac{V_{LL} - V_{FL}}{V_{FL}} \text{x} 100\% \tag{23}$$

where V_{LL} and V_{FL} are the output voltage at light load and full load respectively. From TABLE III, at V_g = 20V, substituting V_{LL} = 4.999V and V_{FL} = 4.831V into (23), the voltage regulation of 3.5% is calculated.

TABLE III
MEASURED OUTPUT VOLTAGE AT DIFFERENT VALUES OF V_G AND I_O

V_g (V)	V_O (V)				
	I_O=1A	I_O=2A	I_O=3A	I_O=4A	I_O=5A
15	4.999	4.926	4.887	4.846	4.835
20	4.999	4.915	4.884	4.845	4.831

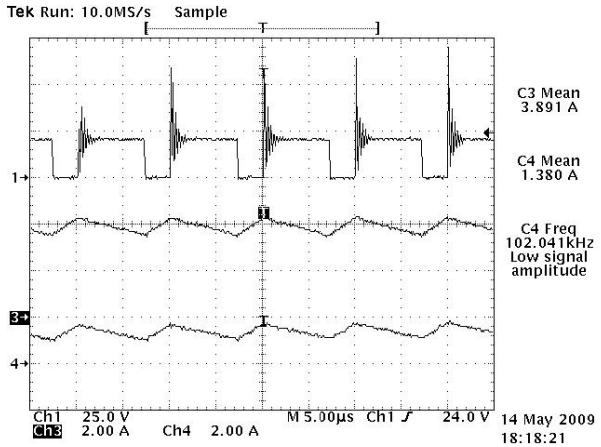


Fig. 9. Waveforms of V_{DS} (top trace: 25V/div), i_{L2} (middle trace: 2A/div), and i_{L1} (bottom trace: 2A/div) for V_g=15V and I_O=4A (R=1.25Ω).

To measure an output voltage response of the converter under a step load change, the load resistance, R, was suddenly switched from 5Ω (I_o =1A) to 1.25Ω (I_o =4A). The captured voltage response is shown in Fig. 10. The maximum voltage drop during the transient is around 0.4V. It takes approximately 300µs for the output voltage to resettle to 5V after the load change. This result indicates that the designed PI compensator not only makes the converter stable under the load current disturbance, but also yields a fast response time.

VI. CONCLUSIONS

In this paper, modeling and control of a Zeta converter operating in Continuous Conduction Mode (CCM) has been presented. The State-Space Averaging (SSA) technique was applied to find the steady-state equations (equation (12)) and small-signal linear dynamic model of the converter (equation (13)). Through the Laplace transform of the small-signal model, some important transfer functions of the converter were derived; i.e. $G_{dv}(s)$ in (14-a), $G_{vv}(s)$ in (14-b), and $G_{zv}(s)$ in (14-c). The duty ratio-to-output voltage transfer function, $G_{dv}(s)$, was particularly useful for feedback control design. It was observed that the quadratic term on the numerator of $G_{dv}(s)$ could be a cause for RHP zeros, if the converter parameters are not selected properly. Hence, the condition in (18) was derived to ensure these quadratic zeros stay on the left-half of the s-plane. To validate the accuracy of the derived $G_{dv}(s)$ in (14-a), it was compared with the results obtained from the averaged switch model and PWM-switch model. The resemblance between these three results confirmed the legitimacy of the derived $G_{dv}(s)$.

Feedback control design of the prototype Zeta converter was illustrated. The PI compensator was selected and designed in the frequency domain by shaping the open-loop transfer function (equation (16)) to attain high DC gain, a crossover frequency of 10 kHz and phase margin of at least 45°. Experimental results show that the prototype Zeta converter employing the design PI compensator exhibits good output voltage regulation and fast transient response to a step-load change.

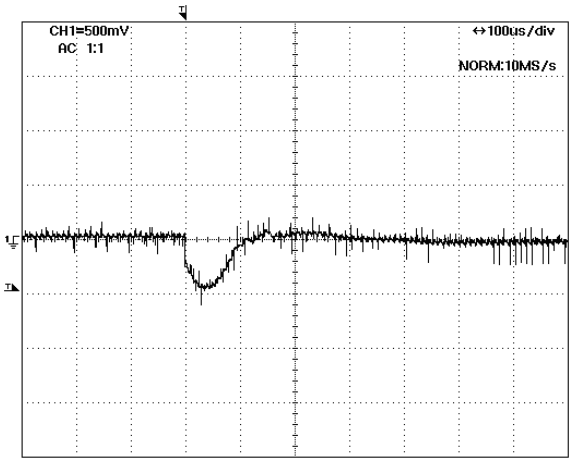


Fig. 10. Output voltage response during the load current switched from 1A to4A.

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