PERFORMANCE EVALUATION OF FLYBACK CONVERTER

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Abstract: Steady-state (DC) analysis of the flyback PWM dc-to-dc converter is performed for continuous conduction mode (CCM). The equations for the device stresses and the component values are derived. The circuit is designed and simulated with the aid of P-SPICE. The effect of transformer leakage inductance and the MOSFET output capacitance on switching losses is investigated. The ringing in the output voltage waveform of the power MOSFET switch is observed. The resonant behavior is analyzed and presented in this work.

Key Words: Flyback PWM dc-to-dc Converter
Continuous Conduction Mode (CCM),
MOSFET Output Capacitance, Transformer
Coupling Coefficient, Switching Losses

I. INTRODUCTION

Flyback converter [1]-[9], an isolated version of buck-boost converter, is widely used for low power applications, typically from 20 to 200 W ranges. A detailed analysis of such a circuit is highly important with respect to the design and selection of devices, specifically power MOSFET, power diode, transformer and the filter capacitor. The objective of this paper is to derive design equations and to investigate the effect of transformer leakage inductance and MOSFET output capacitance on switching losses of the flyback converter for CCM operation. Section II describes the circuit operation and steady-state analysis of the converter for continuous conduction mode (CCM) [1]. The design equations for the energy storing elements are derived and a procedure for selecting the diode and the power MOSFET is suggested in Section III. P-SPICE simulation result based on an example from Section III is also presented. In Section IV, the transformer and the power MOSFET is modeled and the circuit is analyzed to show the effect of parasitics on the switching losses. Switching simulation using P-SPICE and its results follow in Section V.

II. STEADY-STATE (DC) ANALYSIS

The circuit diagram for the classic pulse width modulated (PWM) dc-to-dc flyback converter topology is shown in Fig. 1. The power MOSFET S is used as a controlled switch and the diode D_1 is used as an uncontrolled switch. Capacitor C is the filter capacitor and R_L is the load resistance.

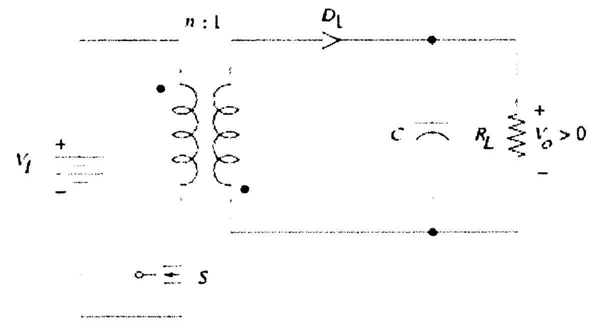

Figure 1. Classic Flyback Converter

The power MOSFET is driven by an external driver. The transformer (coupled inductors) performs two functions: provides dc isolation, stores magnetic energy required for power conversion and changes the voltage level given by the transformer turns ratio n. The polarity of the secondary winding of the transformer is chosen so as to obtain a positive output voltage. In this paper, the analysis is performed assuming the switches are ideal and neglecting the effects of parasitic components. The two time intervals are classified based on the state of the power MOSFET switch. The ratio of t_{on} to T is defined as the duty ratio D, where t_{on} is the ON time of the switch and T is the total time period of one switching cycle.

A. Interval 1 ($0 \leq t \leq DT$)

During the first time interval, the switch S is ON and the diode D_1 is OFF. The equivalent circuit for this time interval is shown in Fig. 2(a). When the switch is ON, the voltage across the diode v_D is equal to $-(V_I/n + V_O)$, causing the diode D_1 to be reverse biased, where V_I is the input voltage, n is the transformer primary to secondary turns ratio, and V_O is the output voltage. Hence, secondary current i_2 and the diode current i_D equals zero. Primary current i_1 is also zero, given by

$$i_1 = -\frac{i_2}{n} = 0. \quad (1)$$

The voltage across the magnetizing inductance L_m is given by

$$v_{Lm} = V_I. \quad (2)$$

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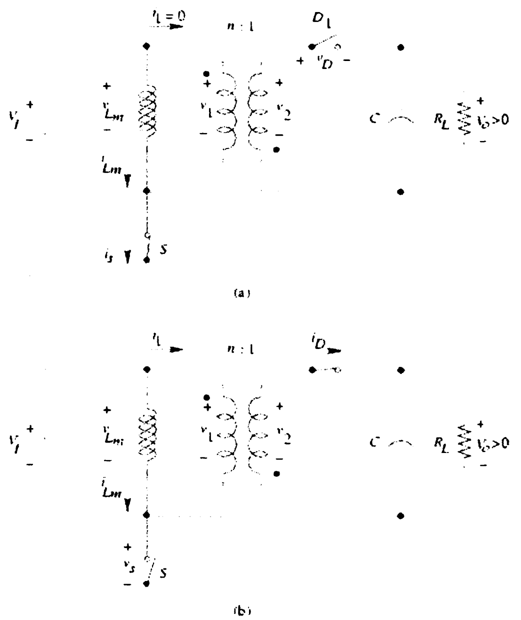

Figure 2. Flyback Equivalent Circuits.
(a) When the Switch is ON. (b) When the Switch is OFF

The current through the magnetizing inductance i_{Lm} ramps up with a slope of V_I / L_m. The switch current i_S equals the magnetizing inductance current i_{Lm} given by

$$i_S = i_{Lm} = \frac{1}{L_m}\int_0^t V_I dt + i_{Lm}(0)$$

$$= \frac{V_I}{L_m}(t) + i_{Lm}(0), \qquad (3)$$

where i_{Lm} (0) is the initial current in the magnetizing inductance at time t = 0. The peak current of the magnetizing inductance is

$$i_{Lm}(DT) = \frac{V_I D}{L_m f_s} + i_{Lm}(0), \qquad (4)$$

where f_s is the switching frequency given by the equation $f_s = 1/T$. The peak-to-peak value of the ripple current Δi_{Lm} through the magnetizing inductance is

$$\Delta i_{Lm} = i_{Lm}(DT) - i_{Lm}(0)$$

$$= \frac{V_I DT}{L_m} = \frac{V_I D}{f_s L_m}. \qquad (5)$$

This time interval is terminated at time $t = DT$, when the switch is turned off by an external driver. The current through the magnetizing inductance is a continuous function of time and as i_{Lm} (DT) is non-zero at switch turn-off, it acts as a current source turning the diode ON. The idealized waveforms for both time intervals are shown in Fig. 3.

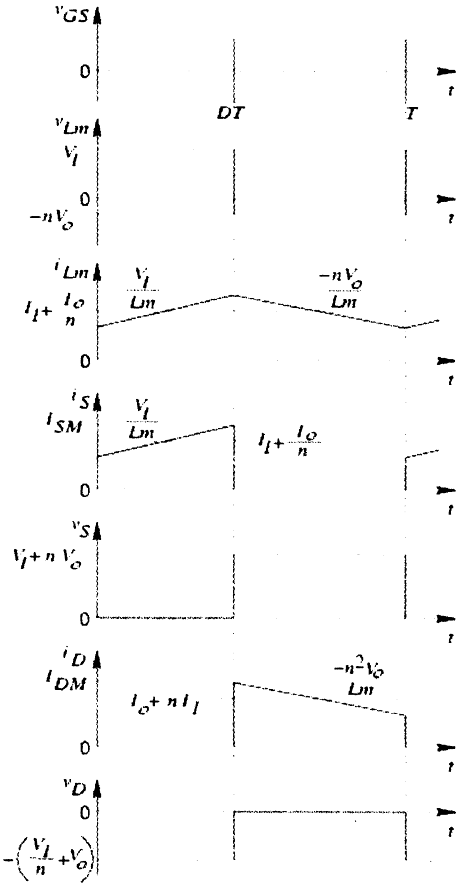

Figure 3. Idealized Voltage and Current Waveforms for CCM Operation.

B. *Interval 2* ($DT \le t \le T$)

During this time interval, the switch S is OFF and the diode D_1 is ON. Fig. 2(b) shows an ideal equivalent circuit for this time interval. The switch current i_S and the diode voltage v_D are zero. The voltage across the secondary of the transformer is

$$v_2 = V_O, \qquad (6)$$

resulting in the voltage across the primary winding of the transformer as

$$v_1 = -nv_2 = -nV_O. \qquad (7)$$

Therefore, the voltage across the magnetizing inductance is

$$v_{Lm} = -nV_O. \qquad (8)$$

The current through the magnetizing inductance is found as

$$i_{Lm} = \frac{1}{L_m}\int_{DT}^t (-nV_O)dt + i_{Lm}(DT)$$

$$= -\frac{nV_O}{L_m}(t-DT) + \frac{V_I D}{f_s L_m} + i_{Lm}(0), \tag{9}$$

where i_{Lm} (DT) is the initial current of the magnetizing inductance at time $t = DT$. The current in the magnetizing inductance falls with a slope of $-nV_O / L_m$. The peak-to-peak value of the ripple current Δi_{Lm} through the magnetizing inductance is

$$\Delta i_{Lm} = i_{Lm}(DT) - i_{Lm}(T)$$

$$= \frac{nV_O T(1-D)}{L_m} = \frac{nV_O(1-D)}{f_s L_m}. \tag{10}$$

As the switch S is open, the switch current i_S is zero. Therefore, the primary current in the ideal transformer is

$$i_1 = -i_{Lm}. \tag{11}$$

This leads to the secondary current i_2 and the diode current i_D as

$$i_D = i_2 = -ni_1 = ni_{Lm}. \tag{12}$$

This time interval is terminated at time $t = T$, when the switch is turned on by an external driver.

III. EQUATIONS FOR DEVICE STRESSES AND COMPONENT VALUES

A. DC Voltage Transfer Function

In order to express the voltage and the current stresses of the diode D_1 and the switch S in terms of the duty ratio D, the dc voltage transfer function of *lossless converter* M_{VDC} for CCM is derived as follows: Referring to the voltage waveform of the magnetizing inductance L_m and applying the volt-second balance from Faraday's law, we have

$$DTV_I = (1-D)TnV_O, \tag{13}$$

resulting in

$$M_{VDC} = \frac{V_O}{V_I} = \frac{D}{n(1-D)}. \tag{14}$$

The dc current transfer function is

$$M_{IDC} = \frac{I_O}{I_I} = \frac{n(1-D)}{D}, \tag{15}$$

where I_O and I_I are the converter output and input currents, respectively. The converter efficiency η is now considered and the dc voltage transfer function of *lossy converter* ($M_{VDC(lossy)}$) is derived as follows: The converter efficiency as a ratio of output power P_O to the input power P_I can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{VDC} M_{IDC}$$

$$= \frac{n(1-D)M_{VDC}}{D}, \tag{16}$$

from which

$$M_{VDC(lossy)} = \frac{\eta}{M_{IDC}} = \frac{\eta D}{n(1-D)}. \tag{17}$$

B. Device Stresses

During the first time interval, the peak value of the diode reverse voltage V_{DM} is

$$V_{DM} = -\left(\frac{V_I}{n} + V_O\right) = -\frac{V_O}{D}, \tag{18}$$

from which

$$V_{DM(\max)} = -\left(\frac{V_{I(\max)}}{n} + V_O\right) = -\frac{V_O}{D_{\min}}. \tag{19}$$

The peak value of the switch current I_{SM} is

$$I_{SM} = I_I + \frac{I_O}{n} + \frac{\Delta i_{Lm}}{2}$$

$$= \frac{I_O}{n(1-D)} + \frac{\Delta i_{Lm}}{2}. \tag{20}$$

This gives

$$I_{SM(\max)} = I_{I(\max)} + \frac{I_O}{n} + \frac{\Delta i_{Lm(\max)}}{2}$$

$$= \frac{I_{O(\max)}}{n(1-D_{\max})} + \frac{\Delta i_{Lm(\max)}}{2}. \tag{21}$$

During the second time interval, the peak voltage across the switch V_{SM} is given by

$$V_{SM} = V_I + nV_O = \frac{nV_O}{D}, \tag{22}$$

resulting in the maximum value of the peak voltage across the switch as

$$V_{SM(\max)} = V_{I(\max)} + nV_O = \frac{nV_O}{D_{\min}}. \tag{23}$$

The peak diode current I_{DM} is

$$I_{DM} = nI_I + I_O + \frac{n\Delta i_{Lm}}{2}$$

$$= \frac{I_O}{(1-D)} + \frac{n\Delta i_{Lm}}{2}, \tag{24}$$

This leads to

$$I_{DM(\max)} = nI_{I(\max)} + I_{O(\max)} + \frac{n\Delta i_{Lm(\max)}}{2}$$

$$= \frac{I_{O(\max)}}{(1-D_{\max})} + \frac{n\Delta i_{Lm(\max)}}{2}. \quad (25)$$

C. Component Values

The minimum value of the magnetizing inductance $L_{m(\min)}$ for CCM operation is derived as follows: Using (10) and (14), the maximum value of peak-to-peak ripple current $\Delta i_{Lm(\max)}$ of the magnetizing inductance is

$$\Delta i_{Lm(\max)} = \frac{nV_O(1-D_{\min})}{f_s L_{m(\min)}}. \quad (26)$$

The dc output power at the boundary P_{OB} of continuous conduction mode (CCM) and discontinuous mode (DCM) is

$$P_{OB} = \frac{W_{OB}}{T} = f_s W_{OB}$$

$$= \frac{f_s L_{m(\min)} \Delta i^2_{Lm(\max)}}{2}, \quad (27)$$

where W_{OB} is the energy transferred from the input dc voltage source V_I to the magnetizing inductance during one cycle for the boundary case. The dc power transferred from the converter to the load R_L can be expressed as

$$P_{OB} = \frac{V_O^2}{R_{L(\max)}}. \quad (28)$$

Substituting (26) into (27) and equating it to (28), the minimum value of the magnetizing inductance $L_{m(\min)}$ is found as

$$L_{m(\min)} = \frac{n^2 R_{L(\max)}(1-D_{\min})^2}{2f_s I_{O(\min)}}. \quad (29)$$

The filter capacitor is modeled by its capacitance C and its equivalent series resistance (ESR) denoted by r_C. The equation for minimum value of filter capacitance is derived as follows: The dc component of the diode current equals the dc load current I_O. The ac component of the diode current is approximated to the peak-to-peak value of the capacitor current I_{Cpp}, which is

$$I_{Cpp} = I_{DM} \approx nI_I + I_O = \frac{I_O}{(1-D)}, \quad (30)$$

resulting in the peak-to-peak value of the voltage across r_C as

$$V_{rcpp} = r_C I_{Cpp} \approx \frac{r_C I_{O(\max)}}{(1-D_{\max})}. \quad (31)$$

The peak-to-peak value of the output ripple voltage V_r is usually specified as a percentage of the output voltage. Hence, the maximum peak-to-peak value of the ac component of the voltage across the capacitance C is found as

$$V_{cpp} \approx V_r - V_{rcpp}. \quad (32)$$

On the other hand, this voltage is approximately given by

$$V_{cpp} = \frac{\Delta Q_{\max}}{C_{\min}}$$

$$= \frac{I_{O(\max)} D_{\max} T}{C_{\min}} = \frac{V_O D_{\max}}{f_s R_{L(\min)} C_{\min}}, \quad (33)$$

where $\Delta Q_{\max}$ is the charge decrease during the time interval from zero to DT. Rearranging (33), we have

$$C_{\min} = \frac{I_{O(\max)} D_{\max}}{f_s V_{cpp}} = \frac{V_O D_{\max}}{f_s R_{L\min} V_{cpp}}. \quad (34)$$

D. Design Example

An example is illustrated for the following design. A power supply that accepts a single-phase line voltage from 85 to 264 V_{rms} at frequencies 50 to 400 Hz is desired. The output voltage V_O required is 5 V, and the load current I_O varies from 1 to 10 A. The output ripple voltage V_r is to be less than or equal to one percent of output voltage V_O.

Design Solution: The maximum and minimum output powers are

$$P_{O(\max)} = V_O I_{O(\max)} = 5\times 10 = 50 \text{ W},$$

$$P_{O(\min)} = V_O I_{O(\min)} = 5\times 1 = 5 \text{ W}. \quad (35)$$

The minimum and maximum load resistances are

$$R_{L(\min)} = \frac{V_O}{I_{O(\max)}} = \frac{5}{10} = 0.5\ \Omega,$$

$$R_{L(\max)} = \frac{V_O}{I_{O(\min)}} = \frac{5}{1} = 5\ \Omega. \quad (36)$$

The minimum and maximum dc input voltages are

$$V_{I(\min)} = 85\times\sqrt{2} = 120.21 \text{ V},$$

$$V_{I(\max)} = 264\times\sqrt{2} = 373.35 \text{ V}. \quad (37)$$

From which, the minimum and the maximum values of dc voltage transfer functions are

$$M_{VDC(\min)} = \frac{V_O}{V_{I(\max)}} = \frac{5}{373.35} = 0.01339,$$

$$M_{VDC(\max)} = \frac{V_O}{V_{I(\min)}} = \frac{5}{120.21} = 0.04159. \quad (38)$$

Assuming the converter efficiency η = 80% and $D_{\max}$ = 0.36, the transformer turns ratio n is found as

$$n = \frac{\eta D_{\max}}{(1-D_{\max})M_{VDC(\max)}} = \frac{0.8\times0.36}{(1-0.36)\times0.04159}$$

$$= 10.83 \quad (39)$$

Let n = 11.

The minimum and maximum duty ratios are

$$D_{\min} = \frac{nM_{VDC(\min)}}{nM_{VDC(\min)}+\eta}$$
$$= \frac{(11\times0.01339)}{(11\times0.01339)+0.8} = 0.1555,$$
$$D_{\max} = \frac{nM_{VDC(\max)}}{nM_{VDC(\max)}+\eta}$$
$$= \frac{(11\times0.04159)}{(11\times0.04159)+0.8} = 0.3638. \quad (40)$$

Assuming the switching frequency f_s = 100 kHz, the minimum magnetizing inductance is

$$L_{m(\min)} = \frac{n^2 R_{L(\max)}(1-D_{\min})^2}{2f_s}$$

$$\frac{11^2\times5\times(1-0.1555)^2}{2\times10^5} = 2.157 \text{ mH}. \quad (41)$$

Using (26), the peak-to-peak value of the ac current through the magnetizing inductance is

$$\Delta i_{Lm(\max)} = 0.1858 \text{ A}. \quad (42)$$

The maximum input current is given by

$$I_{I(\max)} = M_{VDC(\max)} I_{O(\max)}$$
$$= 0.04159\times10 = 0.4159 \text{ A}. \quad (43)$$

From the design specification, the ripple voltage is

$$V_r = \frac{V_O}{100} = \frac{5}{100} = 50 \text{ mV}. \quad (44)$$

Assuming V_{rcpp} = 40 mV and V_{cpp} = 10 mV, the maximum value of the ESR of the filter capacitor is found to be

$$r_{C(\max)} = \frac{V_{rcpp}}{I_{DM(\max)}}$$

$$= \frac{40\times10^{-3}}{15.597} = 2.56 \text{ m}\Omega, \quad (45)$$

and the filter capacitor value is found using (34) as

$$C_{\min} = 3.638 \text{ mF}. \quad (46)$$

In order to choose the power MOSFET and the diode, the stresses are found out using (23), (21) for the MOSFET and (19), (25) for the diode, which are

$$V_{SM(\max)} = 428.35 \text{ V},$$
$$I_{SM(\max)} = 1.418 \text{ A},$$
$$V_{DM(\max)} = 38.94 \text{ V},$$
$$I_{DM(\max)} = 15.597 \text{ A}. \quad (47)$$

E. Selection of Components

Based on the stresses calculated, an International Rectifier IRF840 power MOSFET is chosen whose drain-to-source breakdown voltage V_{DSS} = 500 V, and maximum continuous drain current I_{SM} = 8 A. A Motorola MBR2540 Schottky barrier diode is chosen whose maximum forward current I_{DM} = 25 A, and maximum blocking voltage V_{DM} = 40 V. A standard value of capacitance C = 4 mF, with a breakdown voltage capacity of 25 V and an equivalent series resistance r_C = 2.5 mΩ is chosen. Since the design analysis is performed considering the magnetizing inductance on the primary side of the transformer, a value slightly more than that of the magnetizing inductance is chosen for the primary inductance L_1. Let L_1 = 2.163 mH, from which the value of secondary inductance L_2 is calculated as

$$L_2 = \frac{L_1}{n^2}$$
$$= \frac{2.163\times10^{-3}}{11^2} = 17.876 \ \mu\text{H}. \quad (48)$$

The designed values calculated in Section III C are incorporated in the flyback converter, and the circuit is simulated with P-SPICE [2]. The converter is operated at a maximum duty ratio of D = 0.3638 to get full load current I_O = 10 A. The value of transformer coupling coefficient K = 1 is chosen for ideality. The simulation output voltage V_O and the load current I_O of the converter obtained are shown in Fig. 4.

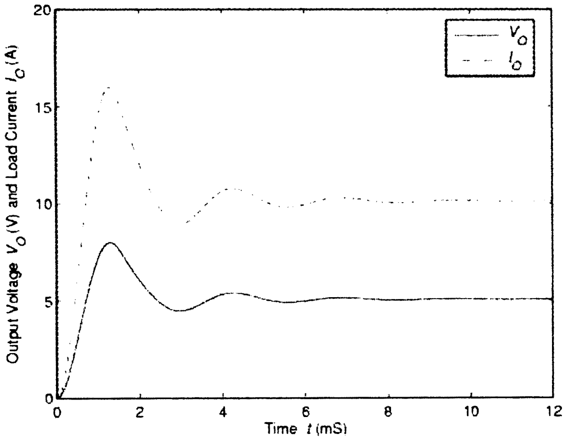

Figure 4. P-SPICE Simulation Output of Flyback Converter for CCM

IV. EFFECT OF PARASITICS ON SWITCHING LOSSES

A simple model of an ideal transformer and its magnetizing inductance L_m is considered for steady state analysis in Section II. Also, the power MOSFET switch is considered ideal. In this section, the transformer and the MOSFET parasitics are included and the MOSFET switching behavior is analyzed. The primary leakage inductance L_{l1} and the secondary leakage inductance L_{l2} is now considered and the transformer is re-modeled as shown in Fig. 5(a). Noting that the primary leakage current i_{Ll1}, magnetizing inductance current i_{Lm} and the primary winding current i_1 is not altered, the primary leakage inductance L_{l1} is moved as shown in Fig. 5(b). The secondary leakage inductance L_{l2} is not moved. From [3], the expression of the primary leakage inductance L_{l1} in terms of the transformer coupling coefficient K is

$$L_{l1} = L_1 - nK\sqrt{L_1 L_2}, \qquad (49)$$

where the transformer mutual inductance M is given by

$$M = K\sqrt{L_1 L_2}. \qquad (50)$$

The power MOSFET is modeled as an output linear capacitance C_O in parallel with the series combination of an ideal switch and the MOSFET on-resistance r_{DS}. When the MOSFET is OFF, the ideal switch is open, charging the parasitic output capacitance C_O. When the MOSFET is ON, the ideal switch is closed, shorting the capacitor C_O through the on-resistance r_{DS}. The energy stored in the capacitor is dissipated in r_{DS} when the switch is on. The OFF-state MOSFET model is shown in Fig. 6. Assuming that the MOSFET output capacitance C_O is linear, the switching loss P_{sw} is expressed as

$$P_{sw} = f_s C_O V_{SM}^2 = f_s C_O (V_I + nV_O)^2. \qquad (51)$$

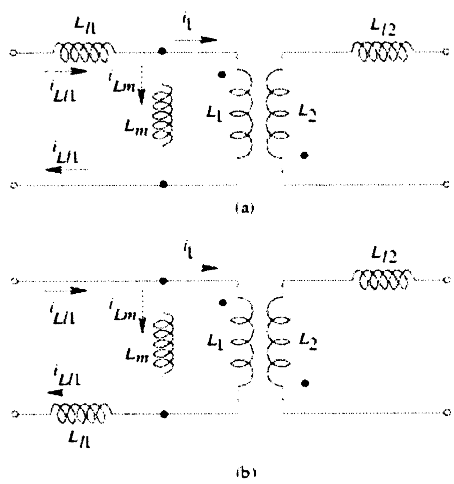

Figure 5. Transformer Models. (a) With Leakage Inductances. (b) Primary Leakage Inductance L_{l1} Moved

Using the transformer model of Fig. 5(b) and the MOSFET OFF-state model of Fig. 6, the flyback equivalent circuit for the time interval $DT \le t \le T$ is shown in Fig. 7. At time $t = DT$, the power MOSFET switch is turned off, resulting in the series combination of transformer primary leakage inductance L_{l1} and the MOSFET output capacitance C_O. The energy of this series resonant circuit is transferred back and forth between L_{l1} and C_O creating high voltage transients across them. The resonating frequency is given by

$$f_r = \frac{1}{2\pi\sqrt{L_{l1} C_O}}. \qquad (52)$$

Since the voltage across the capacitor C_O is the voltage across the switch, the peak switch voltage V_{SM} abruptly increases, thus affecting the switching losses as seen in (51). Also, the voltage stress across the switch is increased. A higher value of primary leakage inductance L_{l1} results in higher energy transfer and hence higher value of peak switch voltage V_{SM}. This energy has to be efficiently snubbed and transferred either to the input source or to the output load to increase the converter efficiency [4].

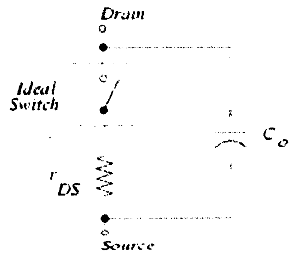

Figure 6. MOSFET OFF-State Model

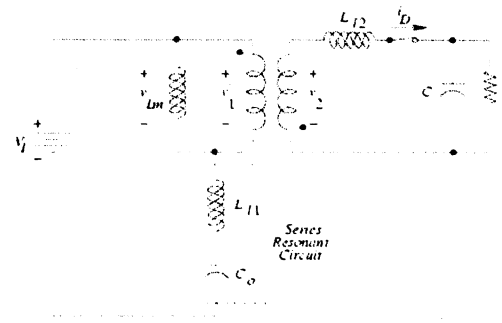

Figure 7. Flyback Equivalent Circuit with Transformer Primary Leakage Inductance and MOSFET Output Capacitance when the Switch is OFF.

V. SWITCHING SIMULATION USING P-SPICE

Coupled inductors are used in place of the ideal transformer for P-SPICE simulation. Since coupled inductors are used, the value of the leakage inductance is easily varied by varying the transformer coupling coefficient K given by (49). The range of K is $0 \leq K \leq 1$.

When the value of $K = 1$, all the flux produced in either or both the transformer windings is linked to the other, resulting in no leakage flux and hence no leakage inductances. Any value of K less than one results in imperfect coupling and hence leakage inductances. The SPICE coupled inductor uses 'k' model [5]. This model assumes that when coupling coefficient is made less than one, the value of the primary leakage inductance equals the secondary leakage inductance. This assumption is valid when the windings of the transformer are physically symmetrical. Although this assumption is valid in rare cases, the coupled inductors are still maintained for the sake of simplicity. Table I shows the simulation values of the peak switch voltage V_{SM} as K is reduced from 1 to 0.98. The output voltage V_O is also observed. K is reduced in steps of 0.0002 from 0.9999 to 0.9989 and in steps of 0.1 from 0.99 to 0.98. Since the peak switch voltage is fairly constant between the values of K from 0.9989 to 0.99, the values in between are omitted. Using (22), the theoretical value of the peak switch voltage, when no leakage inductances are included, is calculated as 175.21 V.

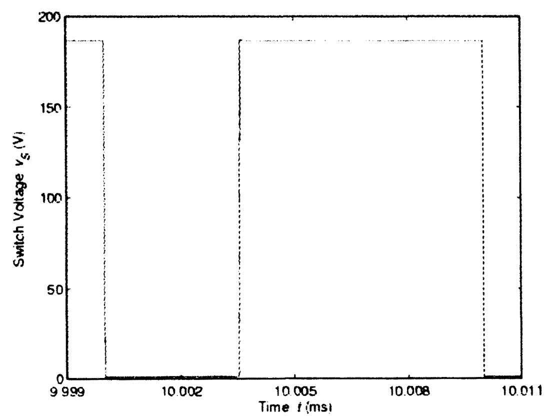

Figure 8. Switch Voltage Waveform for $K = 1$.

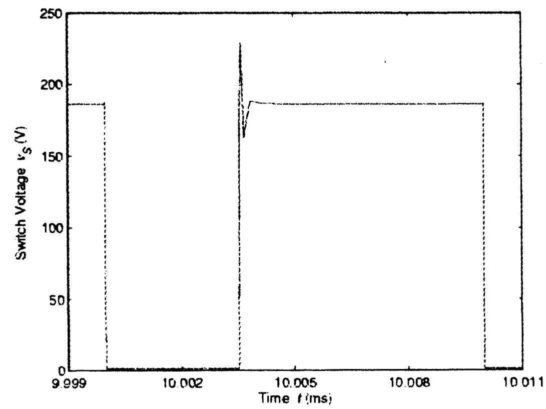

Figure 9. Switch Voltage Waveform for $K = 0.9999$.

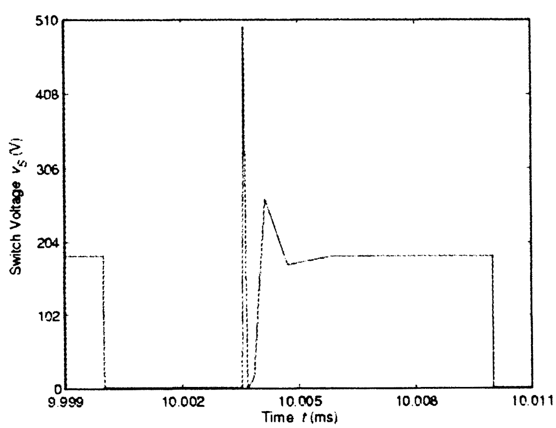

Figure 10. Switch Voltage Waveform for $K = 0.9991$.

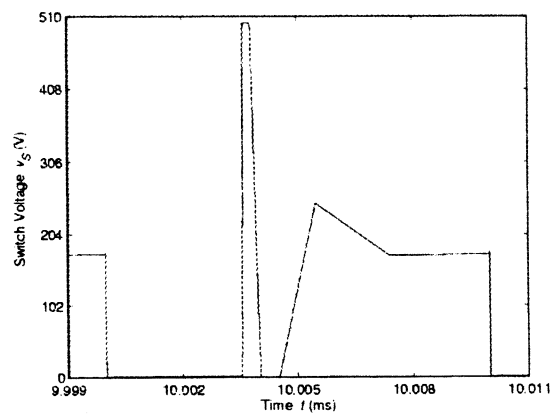

Figure 11. Switch Voltage Waveform for $K = 0.9900$.

TABLE I
PEAK SWITCH VOLTAGES FOR VARIOUS VALUES OF TRANSFORMER COUPLING CO-EFFICIENT

K	$V_{SM}(V)$	$V_O(V)$
1.000	186.568	5.0744
0.9999	229.106	5.0615
0.9997	300.510	5.0356
0.9995	400.088	4.9853
0.9993	439.222	4.9535
0.9991	500.105	4.9372
0.9989	500.131	4.9479
0.9900	500.210	4.3471
0.9800	500.207	3.8888

The simulation value of the peak switch voltage at $K = 1$ is found to be 186.568 V, with an acceptable error of 6.48 %. As seen in Table I, the peak switch voltage V_{SM} increases with a small decrease in the value of coupling coefficient K. Below a certain value of K (say 0.9991 in this case), the value of the peak switch voltage does not increase with decrease in K. This is because the power MOSFET switch IRF840 fails to remain OFF, as its maximum value of breakdown voltage $V_{DSS} = 500$ V. For obvious reasons the output voltage V_O reduces. Figs. 8, 9, 10, and 11 show the waveforms of the switch voltage for selected values of K. Fig. 8 resembles the idealized waveform of the switch voltage whereas ringing is observed in Fig. 9. High voltage transients observed in the distorted switch voltage waveforms are depicted in Figs. 10 and 11. Fig. 12 shows the switching losses as a function primary leakage inductance. Switching loss increases as primary leakage inductance increases until the power MOSFET breaks down, after which it remains constant.

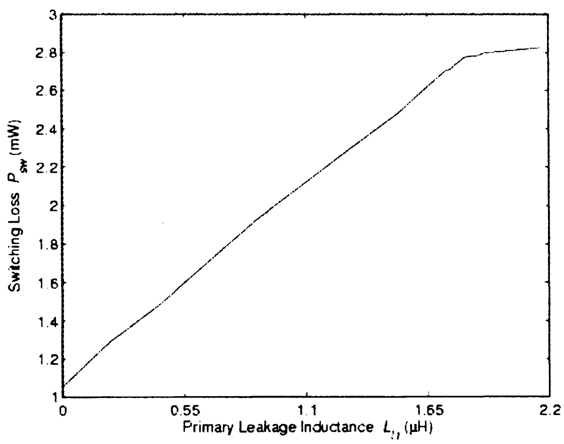

Figure 12. Switching Loss P_{sw} versus Primary Leakage Inductance L_{l1}.

In order to analyze the switching behavior when the power MOSFET does not breakdown, two cases are considered. Since the power MOSFET breakdown voltage is governed by (22), the input voltage is reduced to 60 V, and the switching simulation is performed. In this case, the power MOSFET still breaks down, but at a lesser value of $K = 0.9976$. In the other case, power MOSFET IRFPG50 is used, whose drain-to-source breakdown voltage $V_{DSS} = 1000$ V and switching simulation is performed with input voltage $V_I = 120.21$ V. This power MOSFET also breaks down at a value of $K = 0.9958$, which is lesser than the previous two cases.

VI. CONCLUSIONS

A detailed design procedure of the flyback converter for CCM operation has been presented. An example was illustrated and verified using P-SPICE. The effect of poor transformer coupling leading to an increased value of leakage inductance and hence power MOSFET voltage breakdown was demonstrated. From switching analysis, the transient behavior of the switch voltage due to the variation of coupling coefficient K was confirmed. The peak switch voltage was determined from simulation results and the switching power loss was estimated. From switching simulation, the following can be concluded

1. For a fixed value of input voltage V_I, and the transformer coupling coefficient K, a power MOSFET with higher voltage rating must be selected.

2. For a fixed value of coupling coefficient K, and a specific power MOSFET selected, the input voltage V_I has to be reduced.

3. For a fixed value of input voltage V_I, and a specific power MOSFET selected, the value of transformer coupling coefficient K is limited.

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