Design and Analysis of High Gain Modified SEPIC Converter for Photovoltaic Applications

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***Abstract*— In designing photovoltaic systems connected to the grid system usually DC-DC converter is required to increase the output voltage of the photovoltaic. The most commonly design of DC-DC converters are typically used a converters with high gain static in order to increase the output voltage of the photovoltaic and obtain a high conversion efficiency. One type of converter used is a SEPIC converter topology. However, the conventional DC-DC converter topologies such as SEPIC converters can only increase by 5 times of the input voltage when the Duty Cycle is set to 0.82. Meanwhile, to meet the dc input voltage of the inverter, the input voltage of the converters have to increase above than 10 times. Therefore, to overcome these problems, this paper proposes the design of DC-DC modified SEPIC converter topologies for photovoltaic applications. Modifications to the conventional SEPIC converter is done by adding capacitors and diodes. From the experimental results shows that this converter can increase the output voltage about 10 times and has the efficiency about 91.5%. Furthermore, topology of the this converter can be effectively applied for photovoltaic system.**

Keywords*— DC-DC Converter Modified SEPIC topology, Static High Gain, on Photovoltaic Applications component.

I. INTRODUCTION

Increasing in prices and the limited amount of non-renewable energy sources has led to the use of renewable energy sources is also increasing. One type renewable energy power source that can be used are photovoltaic [1]. At present, renewable energy-based photovoltaic has attracted attention as a future energy because of capable to solve the problems of global warming and the energy crisis caused by the increasing in energy consumption. Photovoltaic-based renewable energy has many advantages because it does not require fuel, pollution-free, and no noises. In addition, photovoltaic modules also have a lifespan of up to 20 years so can reduce the cost of maintenance [2],[3].

To integrate power generation based on photovoltaic system, there are several steps that must be done before the output voltage of photovoltaic connected to the grid system. Conventional schemes are by implementing high frequency step-up transformer or by boosting the voltage of photovoltaic with conventional boost converter. Moreover, the design of DC-DC converters, are typically used conventional converters with high static gain in order to increase the output voltage of the photovoltaic and improve efficiency [3-6]. Recently, several research use SEPIC converter topology. However, the conventional DC-DC converter topologies such as SEPIC converters have static gain with lower output voltage. On the Duty Cycle of 0.82, the SEPIC converter can only increase by 5 times of the input voltage. To meet the standard of high static gain, it needs increase the input voltage by 10 times [3]. Hence, step up transformer is not utilized for the photovoltaic system. To overcome these problems, in this research proposes a DC-DC modified SEPIC converter topologies. Modifications done by adding a diode and a capacitor. Modified SEPIC DC-DC converter able to increase the input voltage up to 10 times.

II. SYSTEM CONFIGURATION

A. Basic Topology of Modified SEPIC Converter

Fig. 1 shows block diagram of the overall converter system. The block diagram consists of a DC source, converters, resistive load, MOSFET drivers, and PI controller. Based on Fig. 1, the input voltage of the converter is from photovoltaic. Therefore, the output power of the photovoltaic is always fluctuated because depends on the solar irradiance. Meanwhile, PWM switching signal to trigger the MOSFET is produced from Arduino Uno. The switching signal generated by this microcontroller has an amplitude of ± 5 V. Typically, the minimum switching signal to make MOSEFET active is 20 V. Therefore in order to make MOSFET on then, the PWM signal from microcontroller has to increase by a MOSFET driver. In order to match the requirement of the voltage in the AC side. In this study, converter output voltage is 340 V and suitable for application of 220V grid connected inverter system. To maintain the output voltage of the converter, in this study PI controller is also utilized to stabilize the output voltage [6]. The topology of modified SEPIC DC-DC converter with high gain is shown in Fig. 2.

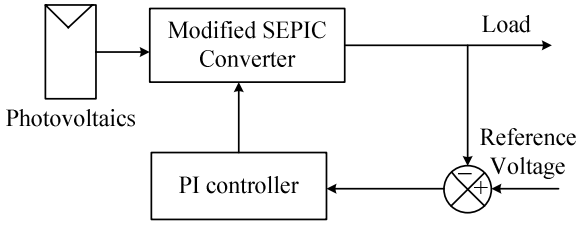

Fig. 1. Block diagram converter system.

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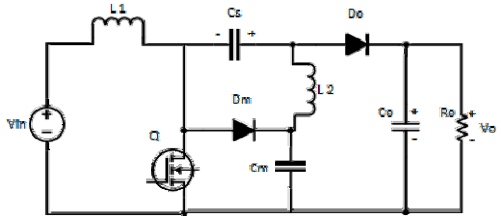

Fig. 2. Modified SEPIC DC-DC converter topology [3].

Topology of converter is modification from conventional SEPIC converter topology which consists of several components, such as inductor L_1, inductor L_2, capacitor C_s, capacitor C_m, switching device Q, diode D_m, diode D_o and capacitor C_o [3].

B. *Operating Mode of Converter*

Modified SEPIC DC-DC converter topology has two modes of operation which are the switch Q is closed and open. Converter operation mode can be analyzed by observing the behavior of each component at steady state conditions. All components are considered in ideal conditions. The voltage in the capacitor is also assumed to be constant during one period of the switching and converter operates in continuous conduction mode (CCM) or the inductor current I_{L1} and I_{L2} always continuous [3]. The waveform of the switching state conditions can be seen in Fig. 3.

1. Operating mode when the switch Q is closed (t_{on})

At the time of the switch Q is closed, the diode D_m and D_o in the reverse-biased condition. Flow of input voltage will flow through the inductor and the switch, and then back toward the voltage source V_{in}. In this condition, the inductor L_1 is charging so that the magnitude of the input voltage will be worth the same as the voltage across the inductor L_1. Beside experiences charging condition in the inductor L_1 by the input voltage, there is also charging inductor L_2 and capacitor C_s by the capacitor C_m. Current supplied from the capacitor C_m is flowing through the switch Q. In this condition, the amount of voltage across the capacitor C_m is equal to the sum of the voltage across the inductor L_2 and capacitor C_s. Fig. 4 shows the current flow when the switch Q is closed.

2. Mode of operation when the switch is open Q (t_{off})

At the time of Q switch is opened, the diode D_m and D_o in the condition of forward-biased. The current from the input voltage will flow through the inductor L_1 to charge the capacitor C_m, and then to the load R_o through the inductor L_2 and diode D_o. Inductor L_1 experiences a discharging mode to charge the capacitor C_m. These condition gives the result the voltage on the capacitor C_m is equal to the sum of the input voltage and the voltage across the inductor L_1. In addition, instead of the discharging process on the inductor L_1, there is also discharging process in the inductor L_2, causing transferring energy to the load R_o. Discharged condition also occurs in the capacitor C_s, causing the voltage on the inductor L_2 is equal to the voltage of V_{Cs}. Fig. 5 shows the current flow when the switch Q is open.

C. *Analysis of Conversion Ratio Rate*

The equation of conversion ratio is obtained when the switch is opened and closed. When the switch is closed, the magnitude of the input voltage to be equal to voltage across the inductor L_1. Then, we get the following equation [3]:

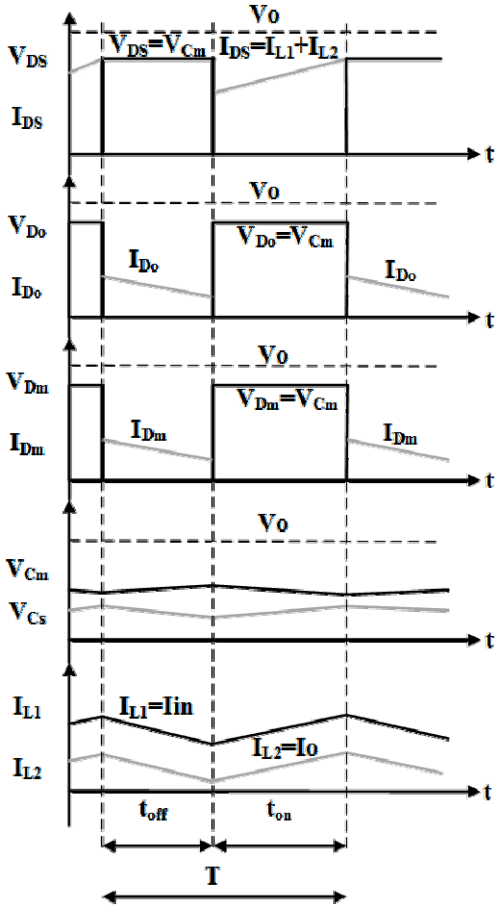

Fig. 3. Waveform of switching characteristics of converter [3].

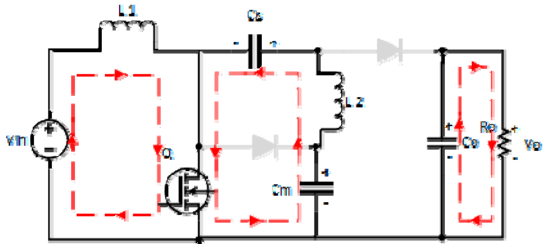

Fig. 4. Operation mode when the switch Q is closed (t_{on})

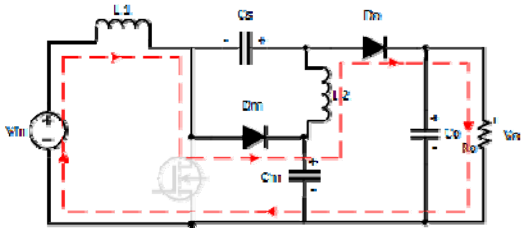

Fig. 5. Operation mode when switch Q is open (t_{off})

$$V_{in} = V_{L1on} \quad (1)$$

$$V_{in} = L_1 \frac{dI_{L1}}{dt}$$

$$V_{in} = L_1 \frac{\Delta I_{L1}}{t_{on}}$$

$$V_{in} \cdot t_{on} = L_1 \cdot \Delta I_{L1} \quad (2)$$

The voltage across the capacitor C_m to be equal to the sum of the voltage across the inductor L_2 and the capacitor C_s. Then, the equation become:

$$V_{Cm} = V_{L2on} + V_{Cs} \quad (3)$$

$$V_{Cm} - L_2 \frac{dI_{L2}}{dt} - V_{Cs}$$

$$V_{Cm} = L_2 \frac{\Delta I_{L2}}{t_{on}} + V_{Cs} \quad (4)$$

When the switch is open, the voltage on the capacitor C_m to be equal to the sum of the input voltage and voltage across the inductor L_1, so we get the following equation:

$$V_{Cm} = V_{in} + V_{L1off} \quad (5)$$

$$V_{Cm} = V_{in} + L_1 \frac{dI_{L1}}{dt}$$

$$V_{Cm} - V_{in} + L_1 \frac{\Delta I_{L1}}{t_{off}} \quad (6)$$

The voltage across the inductor L_2 to be equal to the voltage of V_{Cs}. And it can be explained as follows:

$$V_{Cs} = V_{L2off} \quad (7)$$

$$V_{Cs} = L_2 \frac{dI_{L2}}{dt}$$

$$V_{Cs} = L_2 \frac{\Delta I_{L2}}{t_{off}}$$

$$V_{Cs} \cdot t_{off} = L_2 \cdot \Delta I_{L2} \quad (8)$$

In addition, when the switch is open, the output voltage V_o will be equal to the sum of the voltage across the inductor L_2 and the voltage on the capacitor C_m and can be explained by the following equation:

$$V_o = V_{Cs} + V_{Cm} \quad (9)$$

By substituting equation 2 in equation 6, then obtained the following equation:

$$V_{Cm} = \left(\frac{1}{1-D}\right) V_{in} \quad (10)$$

$$\frac{V_{Cm}}{V_{in}} = \left(\frac{1}{1-D}\right) \quad (11)$$

By substituting equation 8 in the equation 4, then obtained the following equation:

$$V_{Cm} = \left(\frac{1}{D}\right) V_{Cs} \quad (12)$$

By substituting equation 12 in the equation 11, the equation obtained as follows:

$$\frac{V_{Cs}}{V_{in}} = \left(\frac{D}{1-D}\right) \quad (13)$$

$$V_{Cs} = \left(\frac{D}{1-D}\right) V_{in} \quad (14)$$

Based on the equation 9, the output voltage to be equal to the sum of the voltage on the capacitor C_s and the capacitor C_m. By substituting the equations 14 and 12 in the equation 9, then obtained the following equation:

$$V_o = \left(\frac{1+D}{1-D}\right) V_{in} \quad (15)$$

$$\frac{V_o}{V_{in}} = \left(\frac{1-D}{1-D}\right) \quad (16)$$

Equation 16 is the equation to determine the conversion rate of the modified SEPIC converter topology. Thee output voltage is determined by the duty cycle where the value in the range between 0 and 1. The larger the duty cycle, the greater the output voltage of the converter.

III. Design And Experiment

The design of converter has the aims to determine the initial parameters of the converter. Table 1 describes the parameter of the converter. The rated power of the converter is 100 W with the input voltage is 34 V and the output voltage is 340 V.

TABLE I. Preliminary Specifications of Converter

Parameter	Value
Output Power (P_o)	100 Watt
Input Voltage (V_{in})	34 Volt
Output Voltage (V_o)	340 Volt
Switching Frequency	33 kHz
Voltage RippleCs	2.35%
Ripple Voltage Cm	2.35%
Ripple Iin	19%

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In order to increase the input voltage up to 340 V, then, duty cycle and ratio of the converter can be determined by the following equation:

$$\frac{Vo}{Vin} = \frac{340}{34} = 10$$

$$D = \frac{350-34}{350+34} = 0{,}8182$$

Meanwhile, the resistor value is used as a load converter become:

$$R = \frac{V_{out}^{\ 2}}{P_{out}} \frac{340^2}{100} = 1156\,\Omega$$

The value of inductors L_1 and L_2 are determined as follows:

$$I_{L1} = I_{L2} = \frac{V_{in} \cdot D}{\Delta I_L f}$$

$$= \frac{340 \cdot 0{,}8182}{19\% \cdot \frac{V_{in}^{\ 2}}{P} \cdot 33000}$$

$$= \frac{340 \cdot 0{,}818}{19\% \cdot \frac{340^2}{100} \cdot 33000}$$

$$= 1{,}5\,\text{mH}$$

In the inductor L_1, average flowing current to be equal to the input current of converters:

$$I_{L1} = I_{in} = \frac{P_{in}}{V_{in}} = \frac{100}{34} = 2{,}94\,\text{A}$$

Due to the inductor L_1 has a ripple by 19%, then the maximum current that flows is as follows:

$$I_{L1max} = 119\% \cdot 2{,}94 = 3{,}49\,\text{A}$$

In the inductor L_2, the average amount of current that flows to be equal to the output current converters:

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{100}{340} = 0{,}29\,\text{A}$$

In this study, the value of the capacitor C_m and C_s are the same. To determine the value of the capacitor, it requires value of ripple voltage at capacitors C_m as follows:

$$\Delta V_{Cm} = \left(\frac{1}{1-0{,}818}\right).34.2{,}35\%$$

$$\Delta V_{Cm} = 4{,}39\,\text{V}$$

C_m and C_s capacitor value are obtained by the following equation:

$$Cm = Cs = \frac{Io}{\Delta Vc \cdot f}$$

$$Cm = Cs = \frac{0{,}29}{4{,}39 \cdot 33000} = 2\,\mu\text{F}$$

In this case capacitor C_o is set at 50 µF. The voltage on the diode D_m and D_o the same value as the voltage on the capacitor C_m as:

$$V_{Dm} = V_{Do} = V_{Cm} = \left(\frac{1}{1-0{,}818}\right). = 187\,\text{V}$$

While the current flowing in the diode D_m and diode D_o the same value as the output current of converters as follow:

$$I_{Dm} = I_{Do} = I_o = \frac{P_o}{V_o} = \frac{100}{340} = 0{,}29\,\text{A}$$

In the switch device, the voltage value is equal to the voltage on the capacitor C_m:

$$V_{DS} = V_{Cm} = \left(\frac{1}{1-0{,}818}\right). = 187\,\text{V}$$

while the current flowing from the drain to the source is the average amount of current in the inductor L_1 and the inductor L_2:

$$I_{DS} = I_{L1} + I_{L2} = 2{,}94 + 0{,}29 = 3{,}23\,\text{A}$$

Experiment is required to determine the performance of the converter based on design and simulation. Components and parameters during experiment can be seen in Table 2. Meanwhile, the hardware of the converter shown in Fig.6.

TABLE II. COMPONENTS OF CONVERTER

component	Rated
DC voltage source PV	35V
MOSFET	IRFP4332 (1 piece)
Optocoupler	FOD3182 (1 piece)
Diode D_m and D_o	MUR1660 CT (2 pieces)
Capacitor C_o	Polar 50uF 800V
Capacitors C_m	Non Polar 2 uF 400V
Capacitors C_m	Non Polar 2 uF 400V
Inductor L_1	1.503 mH
Inductor L_2	1.495 mH
Resistive load	1156 Ω
Switching Frequency	33 kHz
Inductors Core	TDK-B66335
Output voltage	340V
Duty Cycle	82.35%

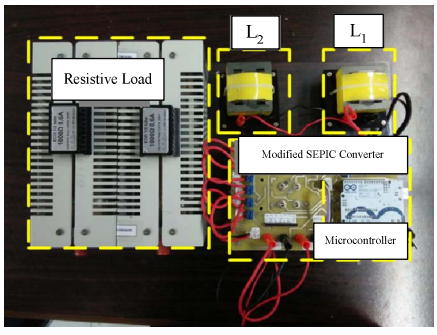

Fig. 6. Prototype of converter.

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IV. Results And Analysis

Fig. 7 explains about the impact of duty cycle to the value of the output voltage. It can be seen that between design and experiment are not exactly similar. This difference because of non ideal factor of each component used for experiment. In each of components such as capacitors, inductors, diodes and MOSFETs have a internal resistance.

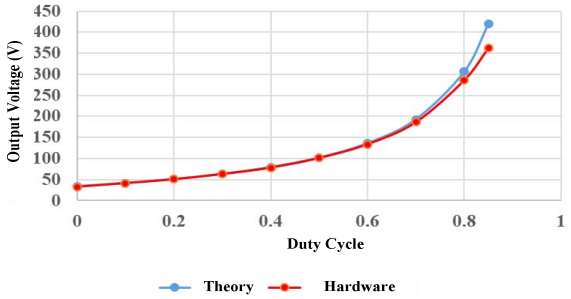

Fig. 7. Conversion ratio

Waveform of switching signal can be seen in Fig. 8. When the gate was triggered by PWM voltage then switch will on condition. The waveform of the drain sources in the MOSFET correspond to the PWM signal. In this mode, the voltage in drain-source becomes zero, causing the current to flow from the drain to the source of the MOSFET. The average current from the drain to the source is 3.49 A. Where, this value is equal to the sum of the value of the inductor current L_1 and L_2. This current is higher than the current in the design due to in ideal components that cause losses. When the switch is opened, the voltage of drain-source is 224 V. In addition, no current flows from the drain toward the sources. Drain-source voltage in the experiment is higher than in the design mainly due to the R_{DS} (resistance between drain and source). In Fig. 10, it appears that switching frequency of 33.06 kHz, so it is the same with the frequency design of 33 kHz.

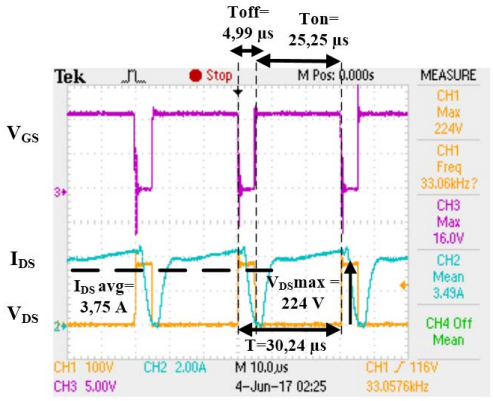

Fig. 8. Switching signal

Fig. 9 shows the shape of the inductor current signals L_1 and L_2. In the inductor current waveform L_1 and L_2, it can be seen that the waveform in accordance with the design and simulation. It is also can be seen that the current at L_1 and L_2 rises up and down simultaneously. It means that the process of charging the inductor L_1 and L_2 occur when the switch is closed and processes of discharging in L_1 and L_2 occur when the switch is open. The current rating on the inductor L_1 is 3.45 A, which is greater than the inductor current L_1 in the design and simulation. It is caused due to losses in certain components, particularly in MOSFETs and inductor winding L_1. Therefore, when generating the output voltage of 400V, a larger current is required compared with in the design and simulation. The same condition is also occurred to the inductor current L_2, which is 0.31 A which is greater than the result of design and simulation. Meanwhile, the inductor L_1 ripple current is 0.56 A and ripple of inductor L_2 is 0.46 A.

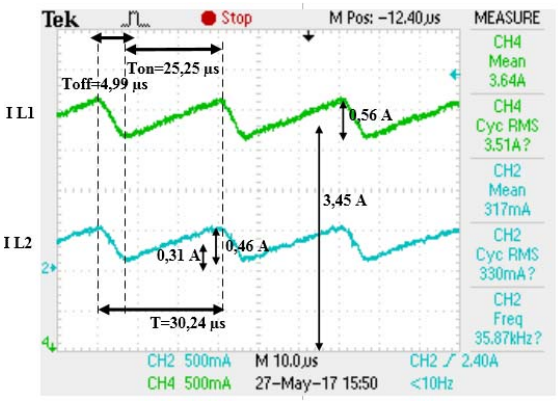

Fig. 9. Inductor current in L_1 and L_2.

The waveform of diode voltage can be seen in Fig. 10. It can be seen that the waveform characteristics of the diode D_m and D_o are similar with the design and simulation. Fig. 11 shows the shape of the voltage waveform across the capacitor C_m and C_s. From these tests, it can be seen that when the switch is open, the capacitor C_m experiences charging mode so that the shape of the voltage across the capacitor C_m is rising up. Meanwhile, at the same time, the capacitor C_s experiences discharging mode.

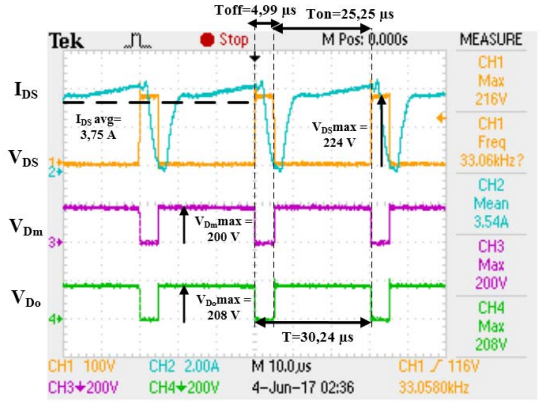

Fig. 10. Voltage waveform in diode D_m and diode D_o.

Efficiency of the converter can be seen in Fig 12. From the figure it can be seen that the converter can work optimally in the power range of 40 to 100 Watt. The greatest power losses mainly occurred in the inductor L_1 and MOSFET. Overall, the average efficiency of the converter is 91.46%. The experimental results using photovoltaic modules can be seen in Fig. 13. It can be analyzed that when 8:00 until 13:00, the power generated by photovoltaic could still reaches the power

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requirements of the load so that the converter is able to achieve a voltage of 340 Volt. However, at 13:00 until 15:00, the converter is not able to achieve the voltage of 340 Volt due to the irradiance is reduced below 1000W/m^2.

Fig. 14. shows effectiveness of the controller to maintain the output voltage when the input voltage is variable. When the input voltage is changed, the output voltage of the converter is maintained constant in 340 V. It can be concluded that the converter able to maintain the output voltage even though the input voltage changes.

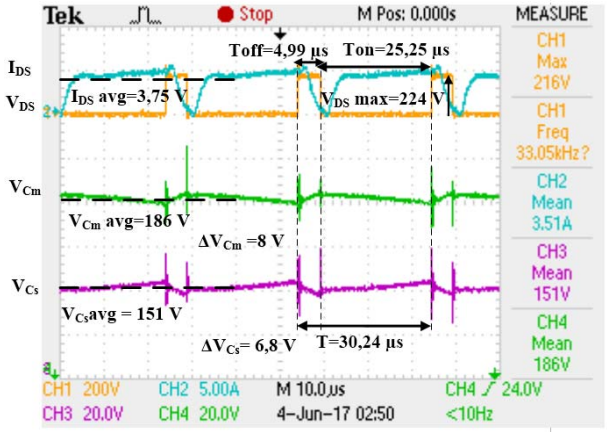

Fig. 11. Voltage waveform of capacitors C_m and C_s.

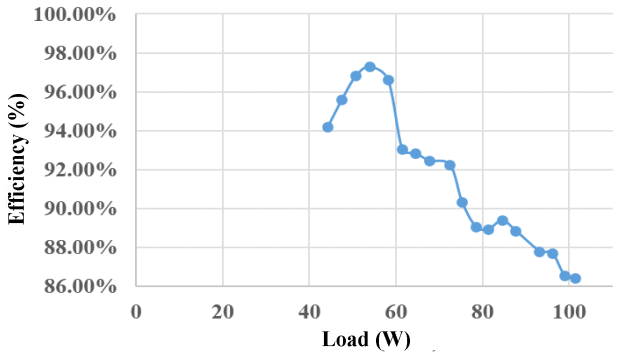

Fig. 12. Converter efficiency

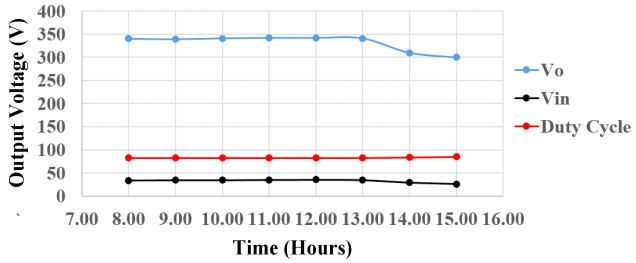

Fig. 13. Testing using photovoltaic modules

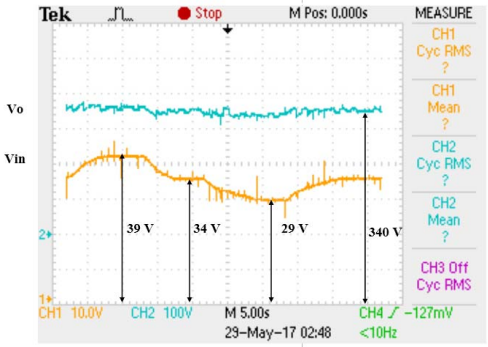

Fig. 14. Dynamic response of converter

V. Conclusion

Based on the results that has been done through simulation and experiment of a modified DC-DC SEPIC converter with high static gain, it can be concluded that modified SEPIC converter topology able to increase the voltage of 34 V to 340 V with full load condition. Thereby, the gain of converter is equal to 10 times. The average efficiency of the modified SEPIC converter is 91.46%. In addition, proposed controller based PI is effectively working to maintain the output voltage of the converter and can be applied for photovoltaic applications.

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