A FAMILY OF MODIFIED ZETA-CONVERTERS WITH HIGH VOLTAGE RATIO FOR SOLAR-PV SYSTEMS

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Abstract

This paper proposes a new family of single-switching DC-DC converters. The proposed converters are based on the classical Zeta-converter combined with two versions of switched inductors/switched capacitors structures. Analysis of the circuits made it possible to choose the most effective variants in terms of increasing the voltage gain. A detailed analysis of the best of the proposed schemes allowed to obtain graphs of the dependence of the voltage gain on the value of the duty cycle in the continuous and discontinuous current modes. Values of voltage stresses on the semiconductor devices are estimated. Theoretical expectations are confirmed by experimental results.

Introduction

An important feature of solar energy sources is their relatively low output voltage. The increase of this voltage is made with the help of dc-dc converters. As is known, both isolated and non-isolated converters are currently used. The particular advantage of non-isolated converters is their small size and weight. Depending on the requirements, one of the known converters is used. Typically, the most important requirement is a high voltage gain with a minimum number of circuit elements. One of the popular types of dc-dc converters used in the solar PV systems is Zeta-converter. It has many advantages, such as input to output DC insulation, non-inverting polarity, buck-boost capability and continuous output current. At the same time, this converter in its classical form has a relatively low voltage gain. In recent decades, a number of solutions have been proposed to increase the voltage gain of various types of DC-DC converters. The use of coupled-inductor can increase the voltage ratio in the various structures such as buck-boost, SEPIC, Cuk and Zeta [1]. Another solution of this problem is the use of the voltage multipliers [2,3]. A significant increase in the voltage gain is achieved through the use of quadratic converters [4, 5]. Very effective, at comparative simplicity, are switching-capacitors introduced into various converter circuits [6]. A variety of options for introducing switching capacitor circuits into Cuk, SEPIC and Zeta converters are presented in [7]. Combination of switching-inductor circuits with Cuk and SEPIC converters is proposed in [8, 9, 10]. Inclusion of the voltage lift component to the SEPIC converter is presented in [11]. This paper is devoted to combination of switched inductor and switched capacitor circuits with the scheme of the classical Zeta-converter.

Proposed schemes, their description and DC analysis

Fig. 1a shows the basic circuit of Zeta-converter and Figs. 1b, 1c depict two switching structures [6] – Up2 and Up3. Combination of these switching structures with the converter circuit allows in a varying degree increasing its voltage gain.

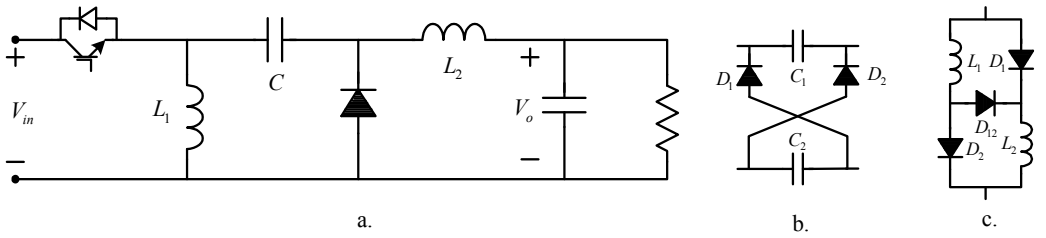

Fig. 1: a:– basic Zeta-converter; b - switched capacitor circuit Up2 [6]; c – switched inductor circuit Up3 [6]

Practically, structure Up2 can be introduced to the basic circuit instead of the capacitor *C* while structure Up3 can replace one (or both) of the inductors L_1, L_2.

Let us analyze briefly the corresponding options of the scheme.

As is known, the voltage gain of the basic Zeta-converter in the continuous current mode is determined as follows

$$M(D)=\frac{V_o}{V_{in}}=\frac{D}{1-D} \tag{1}$$

First, consider the circuit obtained by introducing switching structure Up2 instead of the base capacitor *C*. The corresponding scheme is shown in Fig. 2a.

The voltage-second balances on the inductors L_1 and L_2 can be written as follows

$$for\ L_1:\ \ V_{in}D-V_C(1-D)=0; \tag{2}$$

$$for\ L_2:\ \ (V_{in}+2V_C-V_o)D-(V_C-V_o)(1-D)=0 \tag{3}$$

Substituting the expression for V_C of (2) into (3) we obtain

$$M(D)=\frac{V_o}{V_{in}}=\frac{2D}{1-D} \tag{4}$$

This means that the voltage gain is increased twice in comparison with the basic scheme Fig. 1a.

In the next step, we consider introducing the switching structure Up3. Fig. 2b shows the converter circuit in which the switching structure Up3 replaces the inductor L_1.

The voltage-second balances on the inductors $L_1^{'}$, $L_1^{''}$, and L_2 can be written as follows

$$for\ L_1^{'},L_1^{''}:\ \ V_{in}D-\frac{V_C}{2}(1-D)=0; \tag{5}$$

$$for\ L_2:\ \ (V_{in}+V_C-V_o)D-V_o(1-D)=0 \tag{6}$$

And further

$$M(D)=\frac{V_o}{V_{in}}=\frac{D(1+D)}{1-D} \tag{7}$$

Obviously, this option also allows you to significantly increase the voltage gain, especially at high values of duty cycle *D*.

And now let us replace the output inductor L_2 with a switching structure Up3. The corresponding scheme is presented in the Fig. 2c.

In this case the voltage-second balances on the inductors L_1 and $L_2^{'}$, $L_2^{''}$ can be written as follows

$$for\ L_1:\ \ V_{in}D-V_C(1-D)=0; \tag{8}$$

$$for\ L_2^{'},L_2^{''}:\ \ (V_{in}+V_C-V_o)D-\frac{1}{2}V_o(1-D)=0 \tag{9}$$

So

$$M(D)=\frac{V_o}{V_{in}}=\frac{2D}{1-D^2} \tag{10}$$

This option is less effective in terms of increasing the voltage gain, compared with the circuit Fig. 2a.

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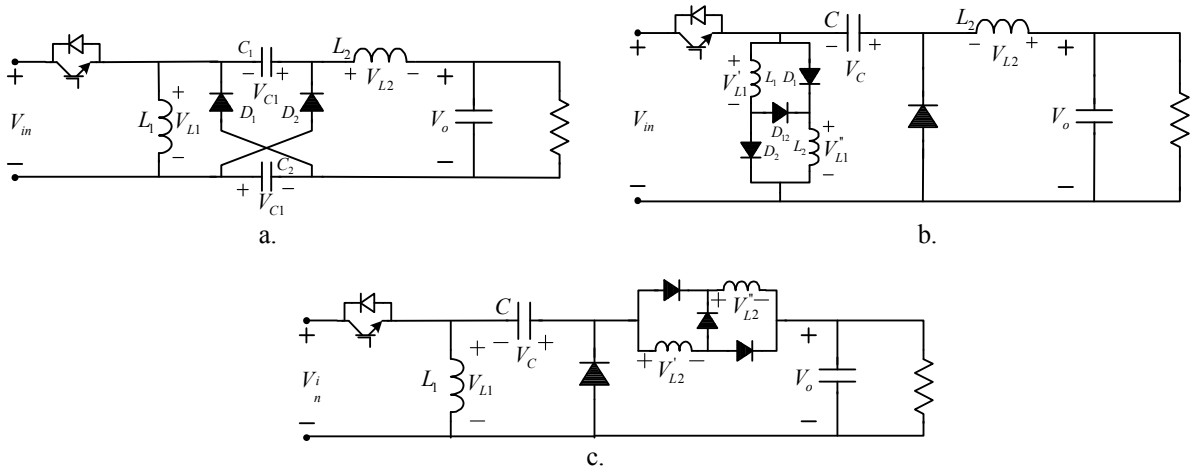

Fig. 2: Three variants of incorporating switching capacitors/switching inductors into Zeta-converter: a – Up2 in place of basic capacitor; b – Up3 in place of input inductor; c – Up3 in place of output inductor

It is of interest to combine switching structures UP2 and UP3 into one circuit. The corresponding scheme and stages of its operation are presented in the Fig. 3. The corresponding timing diagrams are shown in Fig. 4.

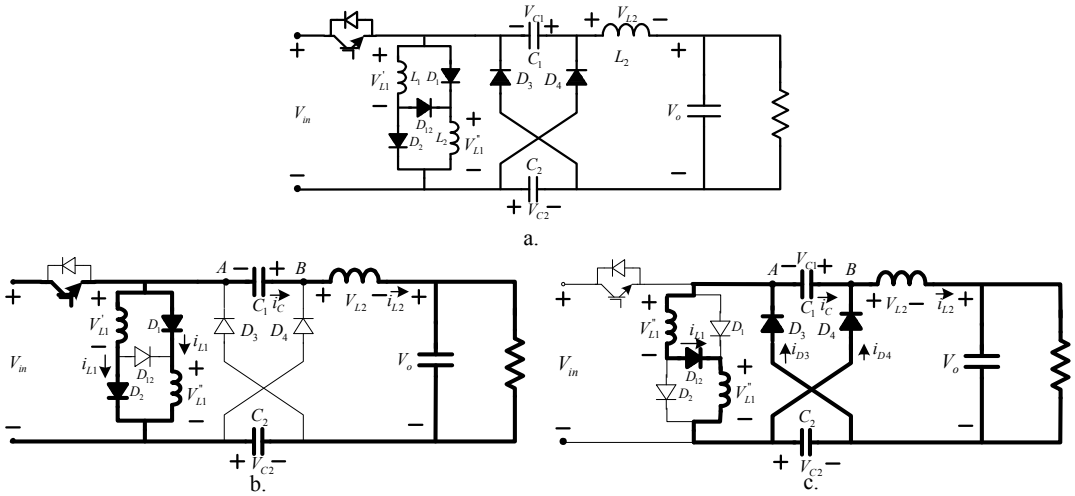

Fig 3: a - Zeta-converter incorporated with switched capacitor circuit Up2 in place of main capacitor and switched inductor circuit Up3 in place of input inductor; b, c- stages of operation for modes “on” and “off” of transistor correspondingly

The voltage-second balances on the inductors $L_1^{'}$, $L_1^{''}$ and L_2 can be written as follows

$$for\ L_1:\ \ V_{in}D-\frac{V_C}{2}(1-D)=0; \tag{11}$$

$$for\ L_2^{'}, L_2^{''}:\ \ (V_{in}+2V_C-V_o)D-(V_C-V_o)(1-D)=0 \tag{12}$$

And finally

$$M(D)=\frac{V_o}{V_{in}}=\frac{D(3+D)}{1-D} \tag{13}$$

As can be seen, this combination of switching structures UP2 and UP3 introduced into the basic scheme of Zeta-converter allowed to significantly increase its voltage gain.

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The graphs in Fig. 5 allow comparing the effectiveness of each of the considered schemes.

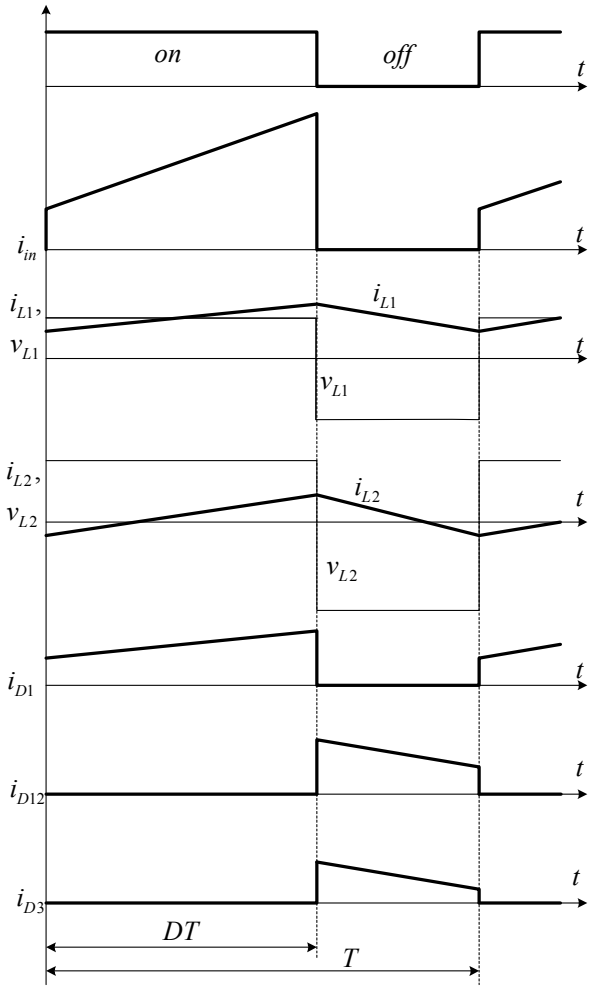

Fig. 4: Switching diagrams of the converter Fig. 3

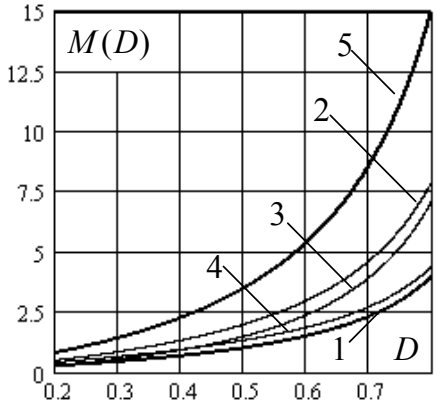

Fig. 5: Voltage ratio of the proposed converters versus duty-cycle for the various options:

1 – original Zeta; 2 –Zeta with Up2; 3 – Zeta with Up3 in place of L_1; 4 - Zeta with Up3 in place of L_2; 5 – Zeta with Up2 in place of C and Up3 in place of L_1

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The resulting expression (13) and the corresponding curves (Fig. 4) are valid only for the continuous current mode (CCM) of the converters.

Let us analyze the operation of the last schema (Fig. 3) in the discontinuous current mode (DCM). Actually this means that the current passing through a pair of diodes D_3, D_4 reaches zero before the beginning of the next switching period. As a result, in the converter operation cycle appears an additional time interval. The corresponding equivalent circuit for this additional interval is shown in Fig. 6.

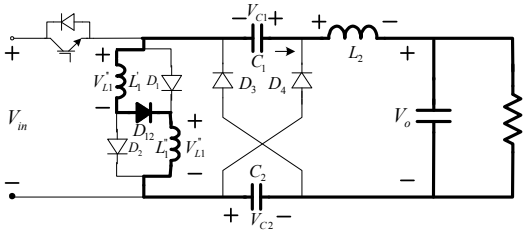

Fig. 6: Additional (third) stage of operation of the circuit Fig. 3 in the DCM

The voltage gain of the converter in DCM depends not only on duty cycle but also on the parameters of the converter elements and switching frequency. In any case, this ratio rises with the deepening of this regime. In this regard, it is extremely important to determine the conditions for ingoing the scheme into the discontinuous operation mode.

The typical graphs of the currents and voltages in the boundary mode are shown in Fig. 7. As can be seen the currents of the diodes D_3, D_4 are end exactly at the beginning of the next switching period. In the following estimations we assume $L_1^{'} = L_1^{''} = L_2 = L$.

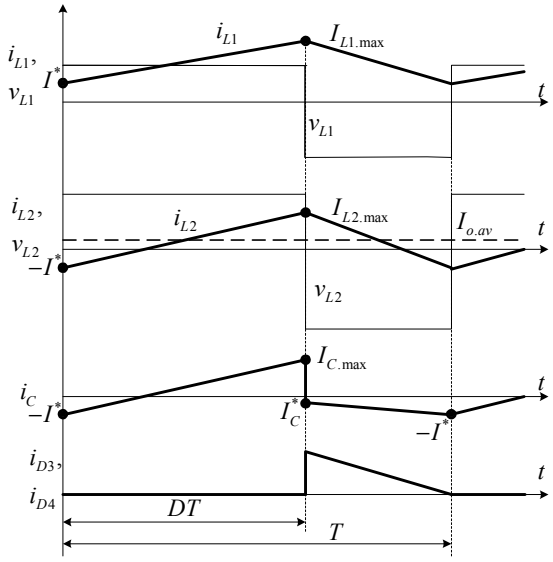

Fig. 7: Switching diagrams in the boundary (CCM-DCM) current mode

In accordance with equivalent circuits Fig. 3b, c and graphs Fig. 7, we can write expressions for maximum values of currents as follow

$$I_{L1.\max} = I^* + \frac{V_{in} D}{fL}; \tag{14}$$

$$I_{L2.\max} = -I^* + \frac{(2V_C - V_o + V_{in})D}{fL} \tag{15}$$

According to (11) and (13)

$$V_C = \frac{2V_{in} D}{1-D};\ V_o = \frac{D(3+D)}{1-D} V_{in} \tag{16}$$

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Substituting (16) to (15) we obtain

$$I_{L2.\max} = I^* + \frac{V_{in}D(1+D)}{fL} \tag{17}$$

As can be seen in the graphs of Fig. 6 at time DT the current through the capacitors jumps from $I_{C.\max}$ to I_C^*. It's obvious that $I_{C.\max} = I_{L2.\max} = I^* + \frac{V_{in}D(1+D)}{fL}$.

Now let us derive the value I_C^*. Two equations of Kirchhoff for two nodes – "A" and "B" (Fig. 3):

$$\begin{aligned} i_{D3} - i_C - i_{L1} = 0; \\ i_{D4} + i_C - i_{L2} = 0 \end{aligned} \tag{18}$$

Note that the circuit is symmetrical and thus $i_{D3} = i_{D4}$. It follows that

$$i_C = \frac{i_{L2} - i_{L1}}{2};\ I_C^* = \frac{I_{L2.\max} - I_{L1.\max}}{2} = -I^* + \frac{V_{in}D(1+D)}{fL} \tag{19}$$

Considering that

$$I_{C.av} = \frac{1}{T}\int_0^T i_C dt = 0 \tag{20}$$

We obtain

$$I_{C.av} = \frac{1}{T}\left[\frac{V_{in}D^2(1+D)}{2fL} + \frac{V_{in}D^2(1-D)}{2fL}\right] - I^* = \frac{V_{in}D^2(3+D)}{4fL} - I^* = 0 \tag{21}$$

And so

$$I^* = \frac{V_{in}D^2(3+D)}{4fL} \tag{22}$$

Now we can calculate the average value of the output current $I_{o.av} = I_{L2.av}$:

$$I_{o.av} = \frac{V_{in}D(1+D)}{2fL} - I^* = \frac{V_{in}D(1+D)}{2fL} - \frac{V_{in}D^2(3+D)}{4fL} = \frac{V_{in}D}{4fL}\left(2 - D(1+D)\right) \tag{23}$$

On the other hand

$$I_{o.av} = \frac{V_o}{R} \tag{24}$$

Comparing (23) and (24), we obtain the expression that determines the condition for the transition from continuous to discontinuous operation mode

$$\frac{R}{fL} = \frac{4(3+D)}{2 - D(3-D^2)} \tag{25}$$

An analytical expression for the dependence of the output voltage on duty cycle in DCM was also obtained. Detailed mathematical analysis of this mode of operation is very complex and the final expression is cumbersome and hardly representable. Therefore, the obtained expressions were used to plot the graphs Fig. 8 - dependences of the voltage ratio *M(D)* against normalized parameter *R/fL* for different values of duty cycle in CCM and DCM considering the formula (25) - boundary between the operation modes.

Component voltage stresses

Voltage stress on the transistor

$$V_{sw.\max} = V_{in} + V_C = V_{in} + V_{in}\frac{2D}{1-D} = V_{in}\frac{1+D}{1-D} = V_o\frac{1+D}{D(3+D)}$$

Voltage stresses on the diodes D_1 and D_2

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$$V_{D1.\max} = V_{D2.\max} = \frac{V_C}{2} = V_{in}\frac{D}{1-D} = V_o\frac{1}{3+D}$$

Voltage stress on the diode D_{12}

$$V_{D12.\max} = V_{in} = V_o\frac{1-D}{D(3+D)}$$

Voltage stresses on the diodes D_3 and D_4

$$V_{D3.\max} = V_{D4.\max} = V_{in} + V_C = V_{in} + V_{in}\frac{2D}{1-D} = V_{in}\frac{1+D}{1-D} = V_o\frac{1+D}{D(3+D)}$$

The graphics in Fig. 9 illustrate the ratio of the voltage stresses across each of the elements to the output voltage versus duty cycle D. As can be seen from the graphs at $D > 0.4$ the voltage stresses on the elements are less than the output voltage.

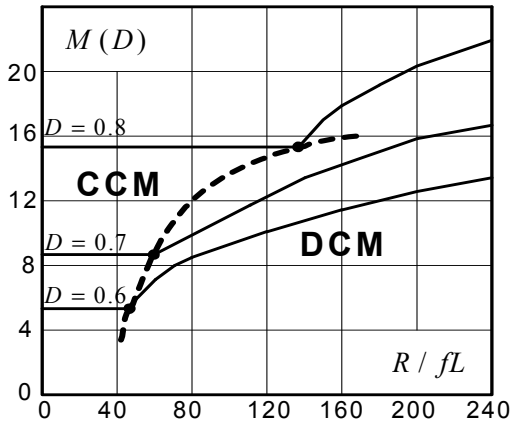

Fig. 8: Voltage ratio $M(D)$ against the normalized parameter R/fL with the boundary between CCM and DCM

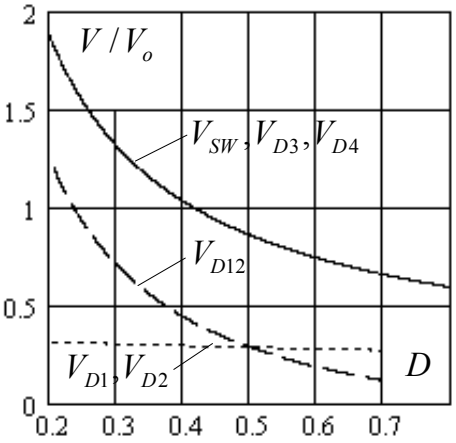

Fig. 9: The ratio of the voltage stress across the elements to the output voltage versus duty cycle D

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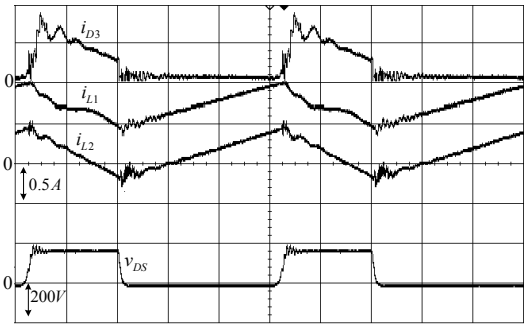
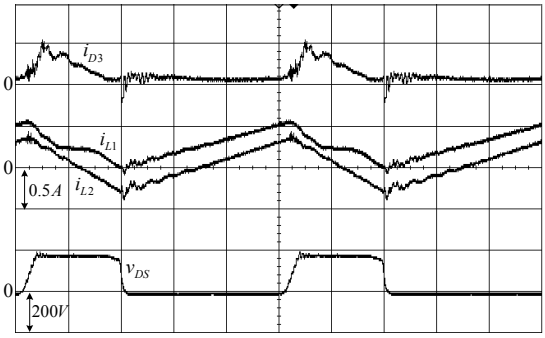
Experimental Results

To confirm the theoretical analysis of the proposed circuit a laboratory prototype was built and tested for V_{in}=50V; $P_{o.max}$= 50 W and f = 100 kHz, with D = 0.6. The parameters of the scheme were as follow: $L_1' = L_1'' = L_2 = 700\mu H$ $C_1 = C_2 = 1\mu F$; $C_o = 10\mu F$ The transistor and diodes were chosen in accordance with the voltage stress mentioned above: transistor was of type *IRFP254PC* and the diodes were of type *SR1660*. The experimental waves are presented in Fig. 8 for the CCM ($R = 1500\Omega$) $V_o = 265V$ and for the DCM ($R = 3200\Omega$) $V_o = 300V$. The actual values of the output voltage are close to their theoretical values. The measured efficiency in CCM was 90%. The use of litz wire in the inductors allowed increasing the efficiency to 91%.



a.



b.

Fig. 10: Experimental waveforms of the converter Fig.3; a – for CCM; b – for DCM

Conclusion

A family of DC-DC converters based on classical Zeta-converter combined with two versions of switched inductors/switched capacitors structures has been introduced. The resulting schemes are quite simple. The most effective scheme is analyzed in detail for both CCM and DCM. It uses only one transistor, five diodes, three inductors and two capacitors This hybrid circuit has a high voltage gain and at the same time, the voltage stresses on the elements are relatively low. The experimental results confirm correctness of the theoretical analysis.

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