ZETA CONVERTER APPLIED IN POWER FACTOR CORRECTION

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ABSTRACT

This paper presents the analysis of the ZETA converter operating in discontinuous conduction mode (DCM) for power factor correction.

The main attractive of ZETA converter is that it is a naturally isolated structure, which allow a regulated output voltage with only one power processing stage.

Principle of operation, mathematical analysis, design procedure and experimental results obtained from a laboratory prototype are presented.

1.INTRODUCTION

Six basic DC-DC converter do exist, namely the Buck, Boost, Buck-Boost, Cùk, Sepic and Zeta.

With the exception of the Zeta converter, all others have been employed to correct the power factor of power supplies, both in continuous and discontinuous current mode. References [1], [2], [3], [4] and [5] have reported on results of researches conducted with the Buck, Boost, Buck-Boost, Cùk and Sepic converters.

All of these converters have their intrinsic limitations. The boost converter for instance, that has been found wide utilization in the industry is not naturally isolated and operates only as a step-up voltage. Yet, it is not capable of protecting itself against a load overcurrent or short-circuit. The Cùk and Sepic converters are naturally isolated and operate as step-down and step-up voltage. However, they do not protect themselves against overload neither. Another practical difficulty that exist with these three converters is that an additional circuit is needed to limit the inrush current.

The Buck converter has the capability of naturally limiting the inrush current and protecting against overload. However, in order to operate at high power factor, the DC output voltage must be much lower than the AC input peak voltage. Consequently the power semiconductor are subjected to high rms current stress. It seems that this converter has no future in power factor correction applications.

The Buck-Boost converter can be easily isolated, operates as step-down and step-up voltage, and is capable of limiting both the load and the inrush current. As a matter of fact, so far, it has been the only converter capable of satisfying all the mentioned specifications simultaneously.

The purpose of this paper is to study the behavior of the Zeta converter in power factor applications. It is demonstrated that it has properties similar to the Flyback converter and that in some particular applications it is the most advantageous over the other DC-DC converters.

2 - PROPOSED CIRCUIT

2.1 - CIRCUIT DESCRIPTION

The proposed topology is shown in Fig. 1, where there are an input standard rectifier bridge, a PWM switch (S1), an isolator transformer (T1), an output inductor (Lo), two capacitors (Co and C1), an output diode (D1), and a Ro that represents the load resistance.

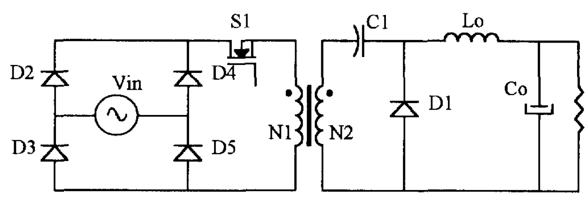

Fig. 1 - Proposed Circuit.

2.2 - OPERATION STAGES

To simplify the analysis the converter will be studied in its non-isolated version, presented in Fig. 2, with the following assumptions:

-The circuit operation is steady state;

-The semiconductors are considered ideals;

-The transformer is considered by its magnetizing inductance and referred to the primary side;

-The capacitor Co is large enough to make its voltage constant and equal to Vo;

-The line voltage is constant in a switching period.

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For a switching period the converter operates as a Zeta DC-DC converter, as follows:

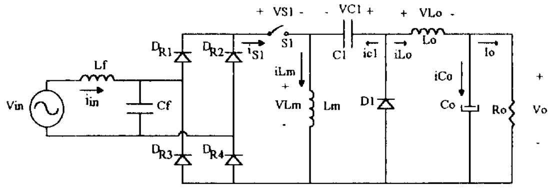

Fig. 2 - Non-isolated Zeta converter.

-First Stage (t0,t1): While switch S1 is conducting, the line source supplies energy to inductor Lm. The energy available in inductor Lo comes from line source and capacitor C1. The currents iLm and iLo increase linearly. Voltages v_{Co} and v_{C1} are considered constant and equal to Vo.

-Second Stage (t1,t2): By the time t1, the switch S1 is turned off and the diode D1 starts to conduct, the energy from Lm and Lo is transferred to C1 and Co respectively. In the second stage there is no energy circulation in the line, which assures that there is not any harmonic distortion in the current line.

-Third Stage (t2,t3): When the currents iLm and iLo become equal, at time t2, the diode D1 turns off and starts the third stage. The voltage applied in the inductances Lm and Lo are zero and their currents are constant until S1 is able to conduct, restarting the operation cycle.

The operation stages illustration are shown in Fig. 3.

The main waveforms for a switching period are shown in Fig. 4. Fig. 5 shows the main waveforms for a line period, in which the line voltage is given by: $v_{in} = Vp\,sin(wt)$.

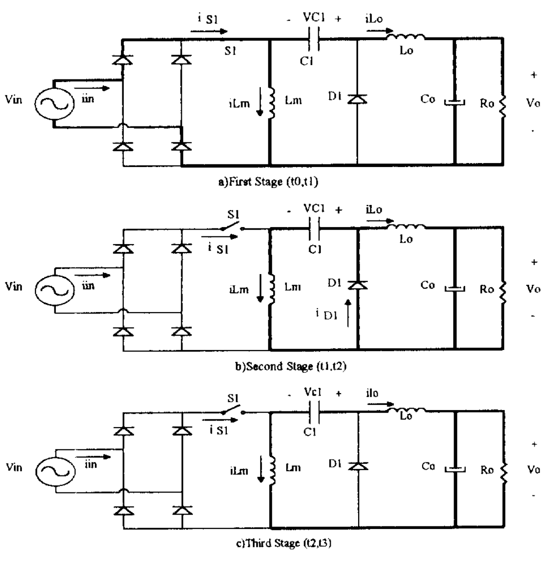

Fig. 3 - Operation Stages.

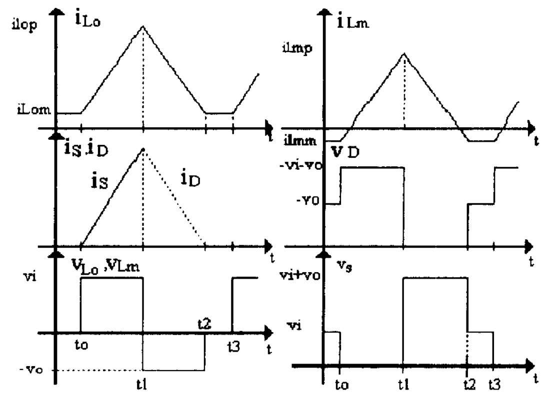

Fig. 4 - The Main Waveforms for a switching period.

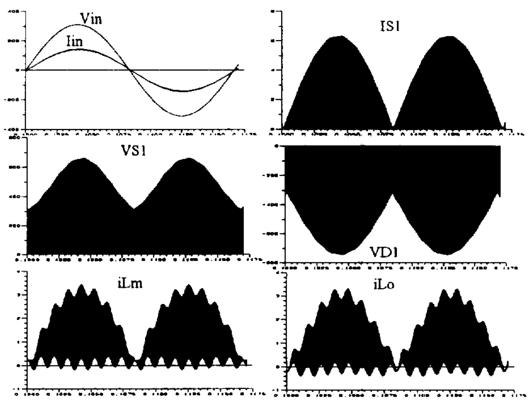

Fig. 5 - The Main Waveforms for a line period.

3 - MATHEMATICAL ANALYSIS

3.1 - LINE CURRENT

In the first stage the currents in the inductances Lo and Lm are defined by:

$$i_{Lm}(t) = \frac{Vp \cdot t}{Lm} sin(wt) - i_{Lm}m \tag{1}$$

$$i_{Lo}(t) = \frac{Vp \cdot t}{Lo} sin(wt) - i_{Lo}m \tag{2}$$

where:

- i_{Lm} = magnetizing current;
- i_{Lo} = output inductance current;
- Vp = line peak voltage;
- $i_{Lm}m$ = minimum magnetizing current;

$-i_{Lo}m$ = minimum output inductance current.

In the second and third stages we do not have any input current circulation, so the current line is given by:

$$i_{in}(t) = i_{Lm}(t) + i_{Lo}(t) \tag{3}$$

The currents $i_{Lm}m$ and $i_{Lo}m$ are equal, but in the opposite directions. Thus the current line will be:

$$i_{in}(t) = \frac{Vp \cdot sin(wt)}{L} \cdot t \tag{4}$$

where L is the equivalent Zeta inductance ($L = Lm//Lo$).

If we consider that the converter has an input filter to eliminate the high frequency harmonics, thus:

$$i_{in}(t) = \frac{Vp \cdot D}{L \cdot fs} sin(wt) \tag{5}$$

where:- $fs = \frac{1}{Ts}$ switching frequency;

- Ts = switching period;
- D = duty cycle.

The expression (5) shows that the converter does not present low order harmonics. The input current is a sinusoidal curve with unity power factor.

3.2 - CRITICAL DUTY CYCLE (Dc)

The critical duty cycle (Dc) is obtained from Fig. 6, when the conduction is critical, the third operation stage does not exist. So the diode current is:

$$i_{D1}(t) = i_{Lm}(t) + i_{Lo}(t) \tag{6}$$

And the current through diode D1 occurs only in the second stage:

$$i_{Lm}(t) = \frac{Vp \cdot tf}{Lm} sin(wt) - \frac{Vo \cdot tc}{Lm} - i_{Lm}m \tag{7}$$

$$i_{Lo}(t) = \frac{Vp \cdot tf}{Lo} sin(wt) - \frac{Vo \cdot tc}{Lo} - i_{Lo}m \tag{8}$$

The critical condition occurs when the input voltage is maximum, where $sin(wt)=1$. Thus:

$$i_{D1}(t) = \frac{Vp \cdot tf}{L} - \frac{Vo \cdot tc}{L} = 0 \tag{9}$$

$$tc = \frac{Vp}{Vo} tf \tag{10}$$

From Fig. 6 we have

$$tc = Ts - tf \tag{11}$$

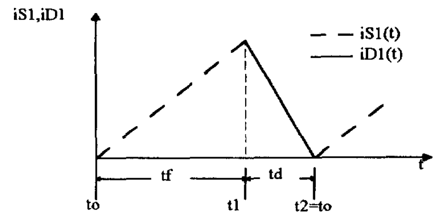

Fig. 6 - Critical conduction.

where $tf = D.Ts$ and $\alpha = \frac{Vp}{Vo}$ (12) , therefore:

$$Dc = \frac{1}{1+\alpha} \tag{13}$$

The Fig. 7 shows the curve of the critical duty cycle.

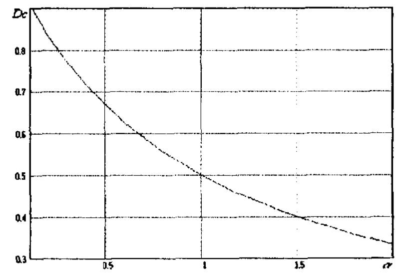

Fig. 7 - Critical duty cycle.

3.3 - OUTPUT CHARACTERISTIC (G)

The average output current Io is equal to the average diode current and are given by:

$$Io = \frac{Vo}{Ro} = I_{D1}av \tag{14}$$

$$I_{D1}av = \frac{\alpha \cdot Vp \cdot D^2}{4 \cdot L \cdot fs} = \frac{Vo}{Ro} \tag{15}$$

Replacing Eq. (12) and Eq. (15) into Eq. (14) is obtained:

$$G = \frac{Vo}{Vp} = \frac{D}{2}\sqrt{\frac{Ro}{L \cdot fs}} \tag{16}$$

Fig. 8 shows the normalized output characteristic curve, where:

$$x = \sqrt{\frac{Ro}{L \cdot fs}}$$

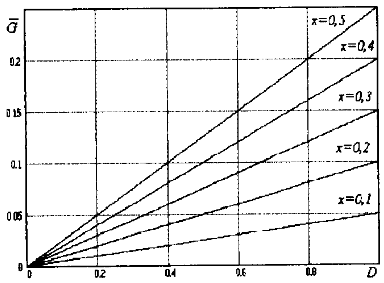

Fig. 8 - Normalized output characteristic.

3.4 - CRITICAL ZETA INDUCTANCE (Lc)

The critical inductance of the Zeta converter for power factor correction is defined from Eq. (14). The average diode current is equal to the average output inductance current. So:

$$i_{Lo}av = i_{D1}av \tag{17}$$

Consequently:

$$Lc = \frac{\alpha \cdot Vp \cdot Dc^2}{4 \cdot Io \cdot fs} \tag{18}$$

The normalized critical Zeta inductance curve is shown in Fig. 9.

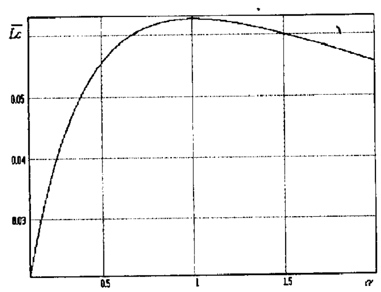

Fig. 9 - Normalized critical Zeta inductance.

The output capacitor Co must eliminate the 120Hz component of the output voltage, and is given by:

$$Co = \frac{D^2 \cdot Vp \cdot \left(\frac{5}{3} + \frac{\alpha \cdot \pi}{4}\right)}{4 \cdot \pi^2 \cdot Lo \cdot \Delta V_{Co} \cdot fs \cdot fi} \tag{19}$$

4 - SIMPLIFIED DESIGN PROCEDURE AND EXAMPLE

The simplified procedure for the converter design is shown as follows.

4.1 - SPECIFICATIONS

To realize the converter design it is necessary to know the following data:

- ***Po = 200W*** (rated output power)
- ***Vo = 72V*** (rated output isolated voltage)
- ***vin = 311.sin(w.t) ± 10%*** (input voltage)
- ***fs = 100kHz*** (switching frequency).

4.2 - CALCULATION

The output current (***Io***) and the turns ratio (***a***) of the transformer are calculated as follows:

$$Io = \frac{Po}{Vo} = \frac{200}{72} = 2.78\,A$$

$$a = \frac{Vo'}{Vo} = 3.89 \text{ (turns ratio)}$$

where ***Vo'=280V*** is the output voltage referred to the primary side of the transformer.

The relation of the voltages are:

$$Vp_{max} = 342V;\ \alpha_{max} = \frac{Vp_{max}}{Vo'} = 1.22$$

$$Vp_{nom} = 311V;\ \alpha_{nom} = 1.11$$

$$Vp_{min} = 280V;\ \alpha_{min} = 1.0$$

From α_{max} it is possible to obtain the critical duty cycle and the critical Zeta inductance, that is:

$$Dc = \frac{1}{1 + \alpha_{max}} = 0.45$$

$$Lc = \frac{\alpha_{min} \cdot Vp_{min} \cdot Dc^2}{4 \cdot Io' \cdot fs} = 198\,\mu H$$

Choosing the value of the Zeta inductance equal to 75% of the *Lc*, ***Lm=Lo*** and keeping 2% of ripple in the output voltage, we obtain:

$$Lm = Lo' = 290\,\mu H$$

$$Lo = \frac{Lo'}{a^2} = 19.2\,\mu H$$

$$Co' = 247\,\mu F$$

$$Co = Co' \cdot a^2 = 3800\,\mu F$$

5 - EXPERIMENTAL RESULTS

With the objective of evaluating the employed methodology, a laboratory prototype was implemented following the same specifications and the same design outlined in the preceding section. The implemented converter is shown in Fig. 10.

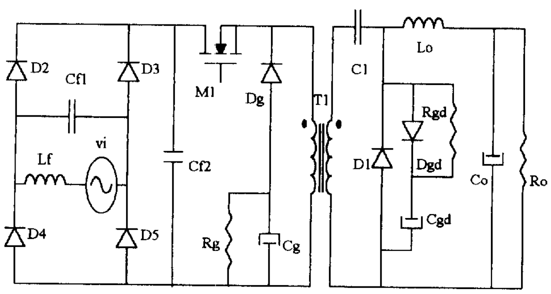

Fig. 10 - Implemented converter.

The specifications of the components employed in the experimental analysis are shown below:

- D_{R1}, D_{R2}, D_{R3}, and D_{R4} = SK1N4004 (Semikron);
- C_{f1} = 15nF / 400V, polypropylene (Icotron - Siemens);
- C_{f2} = 12nF / 400V, polypropylene (Icotron - Siemens);
- L_f = 9.3mH, 248 turns on ferrite core E-42/15 (Thornton);
- S_1 = APT8075BN (Advanced Power Technology);
- Dg = MR817 (Motorola);
- Cg = 2.2μF / 630V, polypropylene (Icotron - Siemens);
- Rg = 6kΩ / 60W;
- T_1 = Transformer on ferrite core E-55/21 (Thornton), N_1/N_2 = 44/12 turns ratio;
- C_1 = 10μF, electrolytic (Icotron - Siemens);
- D_1 = MR851 (Motorola);
- Dgd = 1N4934 (Motorola);
- Rgd = 100kΩ - 1/8W;
- Cgd = 10nF / 250V, polypropylene (Icotron - Siemens);
- Co = 4000μF, electrolytic (Icotron - Siemens) and
- Lo = 20μH, 14 turns on ferrite core E-42/15 (Thornton).

The experimental results are shown in the following figures.

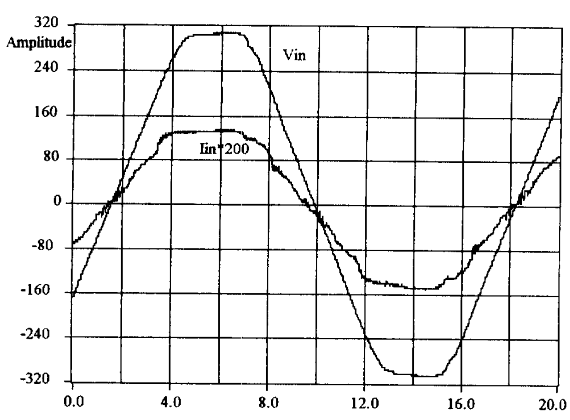

Fig. 11 - Line current and voltage.

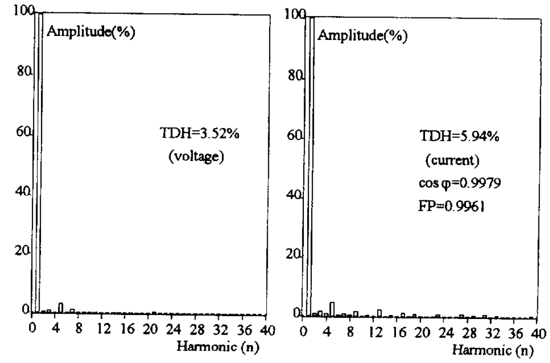

Fig. 12 - TDH of the input voltage and current.

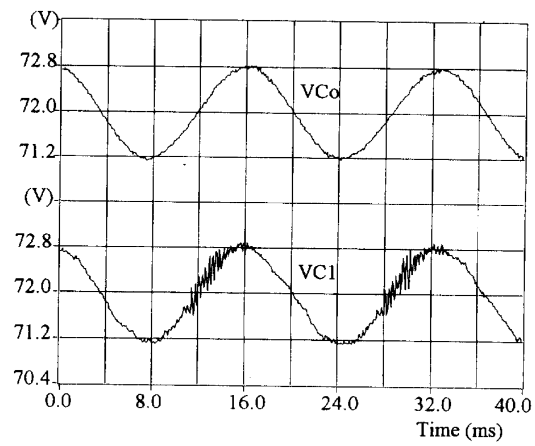

Fig. 13 - Ripple of the voltage in C_1 and Co.

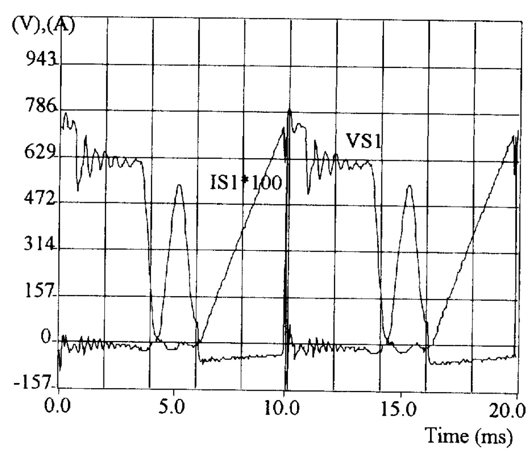

Fig. 14 - Switch voltage and current.

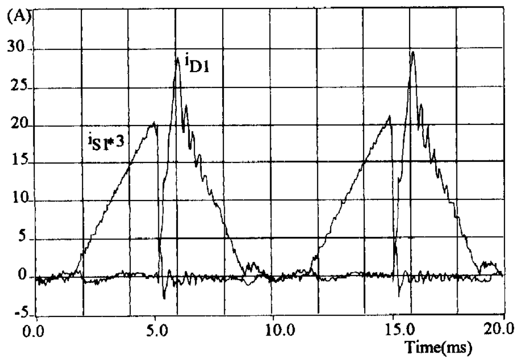

Fig. 15 - D_1 and S_1 current.

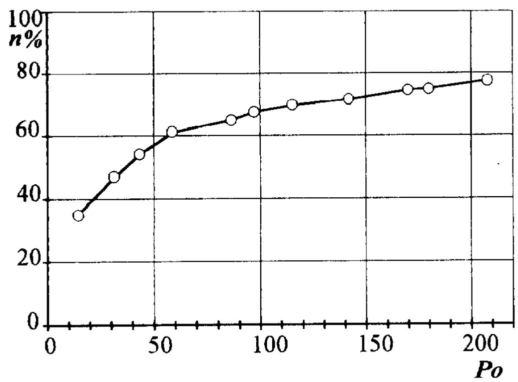

Fig. 16 - Efficiency curve.

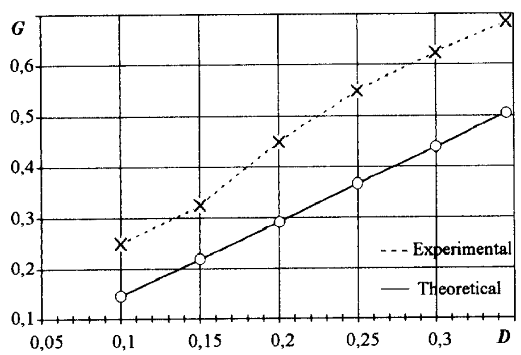

Fig. 17 - Output characteristic.

6 - CONCLUSIONS

The main objective of the study performed in this paper is to investigate the behavior of the Zeta converter in power factor correction applications.

Based on the theoretical and experimental results taken from a laboratory prototype, we can draw the conclusions as follows:

- When operating in discontinuous current mode, driven by a standard PWM integrated circuit, the Zeta converter draws a line current proportional to the input voltage in a manner similar to the Flyback converter, with no harmonic current neither phase displacement.
- The operation in the continuous current mode is also possible, provided that active power factor correction be implemented.
- As the Flyback converter, the Zeta converter provides isolation, high power factor, overload and short-circuit protection, limit of the inrush current and regulation of the output voltage using only one active switch.

7 - REFERENCES

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