A HIGH QUALITY OUTPUT AC/AC CUK CONVERTER

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Abstract. In this paper the design of an AC-AC converter, capable of generating a high-quality output, is described. It is based on the Cuk configuration and, since there are no transformers, it lends itself to a compact and lightweight implementation. An integrated circuit, developed for DC-DC applications, is used to control the converter. Tests performed show that the output exhibits a THD = 3%. The efficiency is slightly higher than 89%, and the average output regulation is 0.3%.

I. INTRODUCTION

Converters with an AC-DC-AC structure have long been used for voltage regulation purposes. Besides efficiency issues, these converters usually include a large electrolytic capacitor in the DC bus, which is a major concern when reliability is an important issue [1]. A better approach involves the use of single stage AC-AC converters. They provide a better power factor and efficiency, lower volume and weight, and better reliability. Any DC/DC configuration can be converted to an AC/AC application, provided that all the switches are substituted by bidirectional devices (and that the gating signal are properly generated). Already several converters based on the buck [2], the boost [3][4][5] and the full bridge [6] converters have been reported. For sag and swell mitigation, the boost and the buck configurations can only be used if a transformer is included, therefore increasing the volume and weight.

Other configurations such as the buck-boost, Cuk, Sepic and Zeta can be used without transformers [7]. A drawback of the buck-boost configuration is that it is modeled as a second-order systems having roots on the right half-plane, which implies an unstable response. On the other hand, although it is modeled as a forth order system, the Cuk configuration does not have roots on the right half-plane. Thus, this configuration will be used to implement the AC/AC converter. In this paper the design of an AC-AC converter based on the Cuk configuration is presented. Since it is a transformerless configuration, it lends itself to a compact and lightweight construction, while providing a high quality output.

II. POWER STAGE

The power stage is shown in Fig. 1, where the transistors are replaced with bidirectional switches. The converter is intended to compensate sags with a maximum depth of 60%; that is, when the input voltage falls to 60% of the nominal input voltage $V_{NOM} = 220V_{RMS}$. The output power is P = 1 kW. It will be assumed that the converter will operate at a switching frequency f_S = 75 kHz, and the maximum duty cycle is $D_{MAX} = 0.63$.

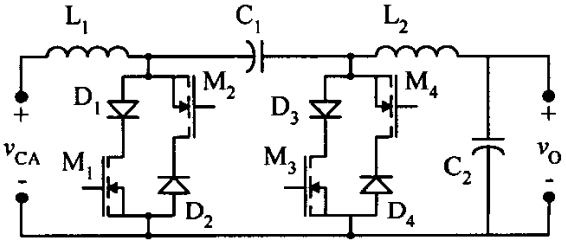

Fig. 1. AC-AC converter power stage

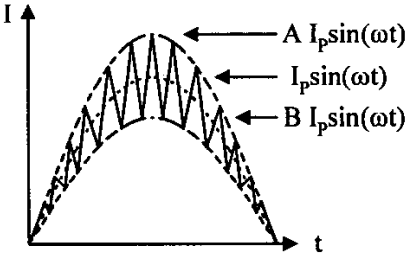

Fig. 2. Current waveform

The current flowing through inductor L_1 is as shown in Fig. 2. Defining the current ripple-factor K_I = A-B, the current ripple can be expressed as:

$$\Delta I = K_I I_P \sin(\omega t) \quad (1)$$

The voltage across inductor L_1 is:

$$V_{L1}=L_1\frac{di}{dt}\cong L_1\frac{\Delta I}{\Delta t} \quad (2)$$

Assuming that $V_{L1}=0.6\sqrt{2}\,V_{NOM}\sin(\omega t)$:

$$0.6\sqrt{2}\,V_{NOM}\sin(\omega t)=\frac{L_1 K_1 I_P \sin(\omega t)}{\Delta t} \quad (3)$$

The term Δt corresponds to the lapse during which the transistor M_1 is on, and can be expressed as:

$$t_1=\frac{D_{MAX}}{f_S} \quad (4)$$

Therefore:

$$0.6\sqrt{2}\,V_{NOM}=\frac{L_1 K_1 I_P}{t_1} \quad (5)$$

The peak current I_P which occurs at the 60% deepest sag, is given by:

$$I_P=\frac{\sqrt{2}\,P}{0.6\,V_{NOM}} \quad (6)$$

Hence:

$$L_1=\frac{0.36\,V_{NOM}^2\,D_{MAX}}{K_1 P f_S} \quad (7)$$

The value of the inductor L_1 depends on the current ripple-factor K_1. The required inductor is 585 μH for $K_1 = 0.25$, and 0.976 μH for $K_1 = 0.15$. On the other hand, from the DC analysis of the converter:

$$\Delta V_{C1}=\frac{I_P\sin(\omega t)\,(1-D)}{C_1 f_S} \quad (8)$$

where the sinusoidal term is introduced because in this case we are dealing with an AC-AC converter. The voltage ripple ΔV_{C1} impressed on C_1 has a waveform similar to that shown in Fig. 1. A voltage ripple-factor K_V can be also be defined, in such a way that:

$$\Delta V_{C1}=K_V V_P \sin(\omega t) \quad (9)$$

where V_P is the peak average voltage. Therefore, from equations (8) and (9), and rearranging:

$$C_1=\frac{I_P(1-D)}{K_V f_S V_P} \quad (10)$$

where I_P is, as before, the input current, at minimum input voltage given by equation (6). This current can also be expressed in terms of the power supplied by the mains as:

$$I_P=\frac{2P}{V_{PP}} \quad (11)$$

Substituting in equation (10):

$$C_1=\frac{2P(1-D)}{K_V f_S V_P^2} \quad (12)$$

Assuming a 10% ripple, $K_V = 0.1$, the value of capacitor C_1 should be 2 μF. Inductor L_O can be calculated using the same equation that applies for L_1. In turn the output capacitor can be calculated assuming a cut-off frequency equal to one tenth the switching frequency. Then:

$$C_O=\frac{100}{4\pi^2 L_O f_S^2} \quad (13)$$

III. COMPENSATOR DESIGN

The compensator frequency response can be obtained by substituting the transistors in the schematic with its PWM model in continuous conduction mode. Once this substitution is performed, the resulting circuit can be analyzed using the electrical circuit standard techniques [8][9]. The converter transfer function, from the control input to the power output, can be expressed as:

$$H(s)=H_0\frac{a_3 s^3+a_2 s^2+a_1 s+a_0}{b_4 s^4+b_3 s^3+b_2 s^2+b_1 s+b_0} \quad (14)$$

Using the calculated values afore, the following results are obtained:

$H_0 = 1.36 \times 10^3$
$z_{1,2} = 0$
$z_3 = -1 \times 10^9$ rad/sec

$$p_{1,2} = 1 \times 10^4 (-0.2362 \pm 0.8929\,j)$$
$$p_{3,4} = 1 \times 10^4 (-0.7972 \pm 5.8016\,j)$$

The Bode diagram is shown in Fig. 3. Since the Cuk converter transfer function involves an unstable response, it is necessary to design a frequency compensating network, such that a closed-loop stable response is obtained. A suitable pole-zero pattern for the compensator is as shown in Fig. 4 [10]. There is a first pole located at the origin, followed by two zeros, located at f_{Z1} and f_{Z2} respectively, and two more poles, at f_{P2} and f_{P3}. The schematic of an active circuit that can provide such a response is shown in Fig. 5.

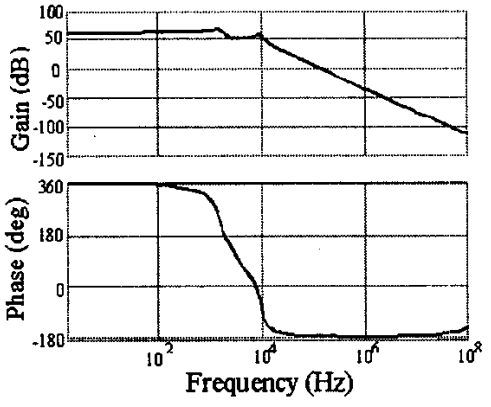

Fig. 3. Bode diagram

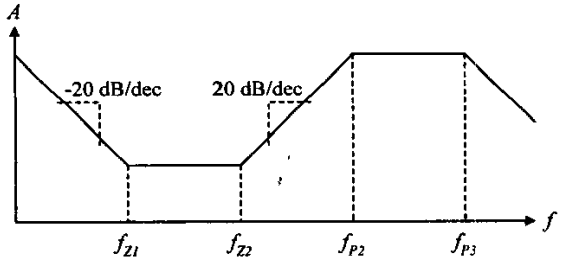

Fig. 4. Pole-zero distribution for the compensating network

The transfer function for the circuit can be obtained through routine analysis. The result is:

$$H(s) = \frac{(sC_2R_2+1)(sC_3(R_1+R_3)+1)}{sR_1(sC_3R_3+1)(C_1+C_2)\left(s\frac{C_1C_2R_2}{C_1+C_2}+1\right)} \quad (15)$$

The elements in the circuit are calculated as follows. As a first step, a crossover frequency f_{XO} is set as:

$$f_{xo} = \frac{f_S}{5} \quad (16)$$

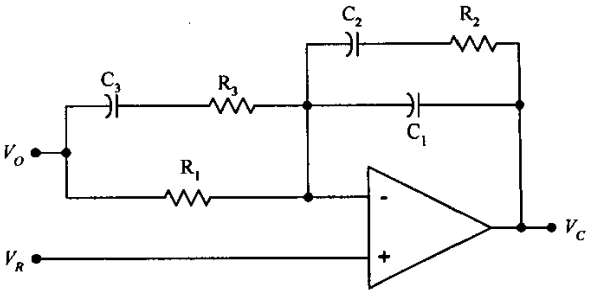

Fig. 5. Compensating circuit.

Let $f_{P(L-C)}$ be the location of the first complex-pair pole in the transfer function. The location of the first zero in the compensator design is set to:

$$f_{Z1} = \frac{f_{P(L-C)}}{5} = \frac{1}{2\pi C_2R_2} \quad (17)$$

The location of the second zero should be within the range $f_{P(L-C)} < f_{Z1} < 1.2\,f_{P(L-C)}$, and:

$$f_{Z2} = \frac{1}{2\pi C_3(R_1+R_3)} \quad (18)$$

The location of the second pole is given by

$$f_{P2} = \frac{1}{2\pi C_3R_3} \quad (19)$$

In turn, the third pole should meet the following criteria:

$$f_{P3} = \frac{C_1+C_2}{2\pi C_1C_2R_2} > 1.5\,f_{XO} \quad (20)$$

For the response of the power stage, a suitable set of values in the compensator is as follows: C_1 = 1.8 pF, C_2 = 10nF, C_3 = 3nF, R_1 = 10 kΩ, R_2 = 100 kΩ, R_3 = 699 Ω. The zeros are located at 18.46 Hz and 4.93 kHz. The first pole is at 75 kHz, while the second is at 2.7 MHz. The closed-loop frequency response, including the compensator, is shown in Fig. 6. As can be seen, the cut-off frequency is at 1.8 MHz and the phase margin is equal to 56°; these values ensure a stable response.

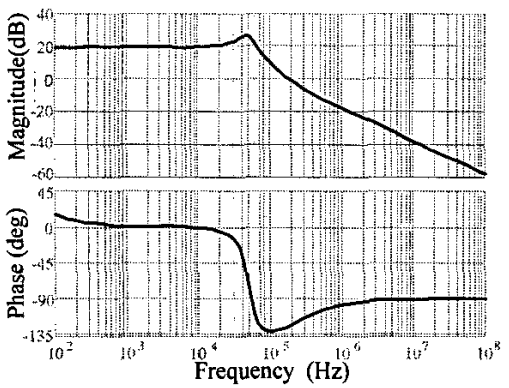

Fig. 6 Closed-loop frequency response.

IV. CONTROL BLOCK

The control block is shown in Fig. 7. It is based on the UC3526, which is an integrated circuit developed for DC-DC converter applications. For this reason, both the set-point and the feedback signal have to be modified to fit the input range of the device. One option involves shifting upwards the bipolar signal. A second option, followed in this design, involves rectifying both signals, in such a way that the integrated circuit only handles positive signals. The blocks within the dotted box are part of the UC3526.

The reference generator block, shown in Fig. 8, generates a rectified sinusoidal wave synchronized with the mains frequency. It is based on a phase-locked loop connected as a frequency-multiplier, with a counter in the feedback loop. It should be noted that, although it is shown as a separated block, the rectifying function is included in the look-up table. This block also provides a mains polarity signal, labeled as POL, which is used for synchronicity purposes.

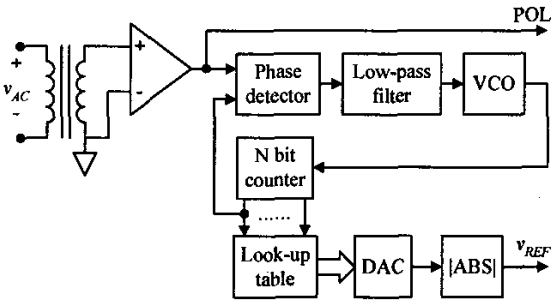

Fig. 8. Reference generator

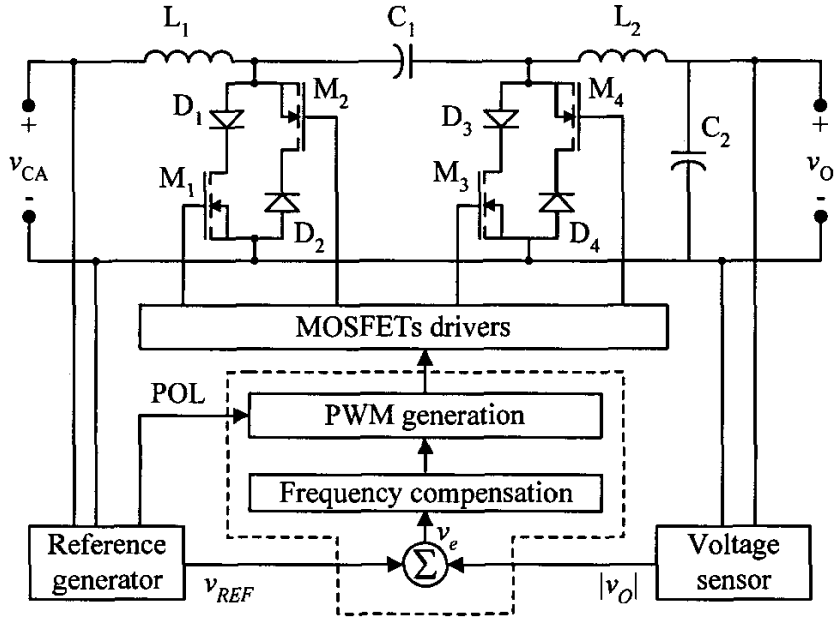

Fig. 7. Control circuit

The reference generator output feeds the error amplifier. The second input from to the error amplifier corresponds to the converter output, after scaling and rectification. Some logic is added at the output of the UC3526, in such a way that, using the POL signal as an enabling signal, transistors M_1 and M_3 are commutated during the mains positive half-cycle, while keeping M_2 and M_4 blocked during this lapse. In

turn, transistors M_2 and M_4 are commutated during the negative half-cycle, while keeping M_1 and M_3 off. The MOSFET drivers include an isolation stage because, except for M_1 and M_3, its sources are connected to different nodes.

V. TESTS AND RESULTS

A 1 kW prototype was build using 800V/17A CoolMOS 3rd generation devices, and its performance tested for 120 V_{RMS} and 220 V_{RMS} inputs. The performance of the converter is illustrated in the following figures. The worst case for a sag occurrence is at the voltage peak, and Fig. 9 illustrates such a case. The nominal output voltage is 120 V_{RMS}, represented by the dotted line. As can be seen, the output returns to the nominal value in about 10 milliseconds. Fig. 10 illustrates the response to a 30% swell. In this case the circuit exhibits a faster response, and the output returns to its nominal value in less than 5 milliseconds. Figure 11 corresponds to a 60% sag, but with a nominal output voltage equal to 220 V_{RMS}. The response takes a bit longer, and the output returns to its nominal value in about 12 milliseconds.

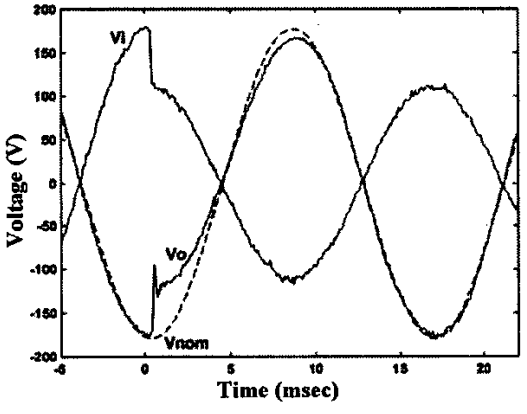

Fig. 9. Regulator response to a 60% sag, with V_{nom} = 120 V_{RMS}

Fig. 12 shows the output voltage regulation as a function of the input voltage, with a 500 W load connected to the regulator. Fig. 13 depicts the converter efficiency as a function of the input voltage, with a 750 W load. Fig. 14 illustrates the efficiency of the converter as a function of the output power. Finally, Fig. 15 shows the response of the converter to a maximum depth sag, and with a 233 VA nonlinear load, according to the standard IEC 62040-3.

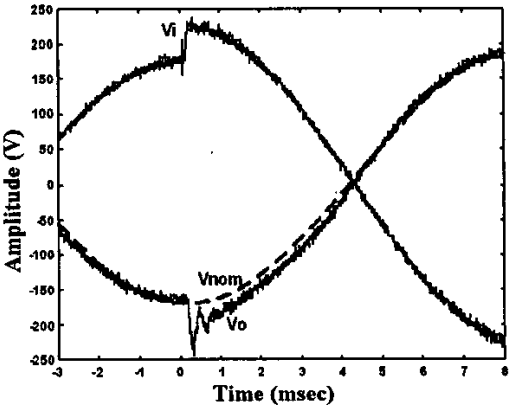

Fig. 10. Regulator response to a 30% swell

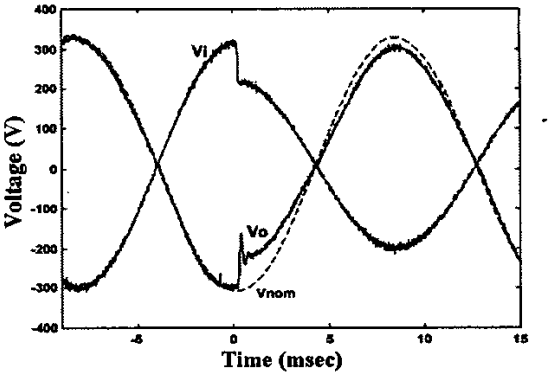

Fig. 11. Regulator response to a 60% sag, with V_{nom} = 220 V_{RMS}

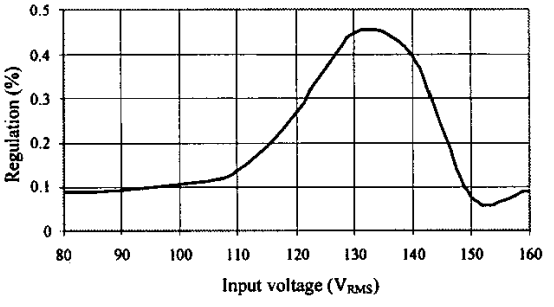

Fig. 12. Voltage regulation as a function of the input voltage

V. CONCLUSIONS

In this paper the design of an AC-AC converter based on the Cuk configuration is described. It is shown that the tools developed for DC-DC converters can be successfully applied to this case. In fact, the frequency compensating network was designed using a technique commonly applied to DC-DC converters.

This is also the case of the control circuit included in the design.

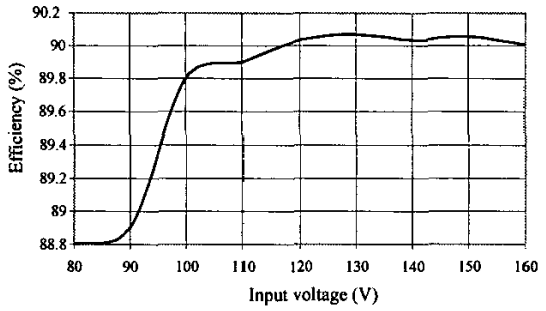

Figure 13. Efficiency as a function of the input voltage

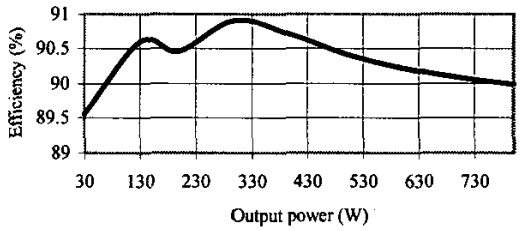

Figure 14. Efficiency as a function of the output power

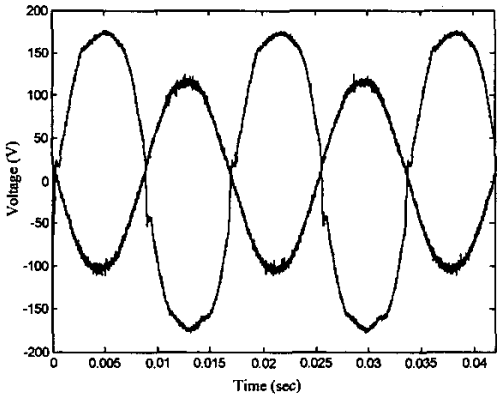

Fig. 15. Behavior with nonlinear load

Since a transformerless configuration was used, the prototype is compact and lightweight. It is capable of correcting sags with deeps down to 60% and swells heights up to 30%. In both cases, the output returns to its nominal value within a mains cycle. Also, the efficiency obtained is much better that that reported for multistage regulators. The maximum THD obtained at the output, with resistive loads, is 3%. The circuit behaves properly for loads down to 30 Watts. Also, its behavior with non-linear load is deemed suitable to energize information-processing equipment.

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