COL 215

HARDWARE ASSIGNMENT 2

RISHABH KUMAR 2021CS10103

RUCHIR SINGH 2021CS10119

APPROACH

- assignment1.vhd:

This component of assignment 2 has been directly used from our COL 215 hardware assignment 1. It is a circuit that takes a 4-digit hexadecimal number (so each number is 4-bit) from switches in the Basys3 board and displayed it on the 4-seven segment displays on the board.

- stopwatch.vhd:

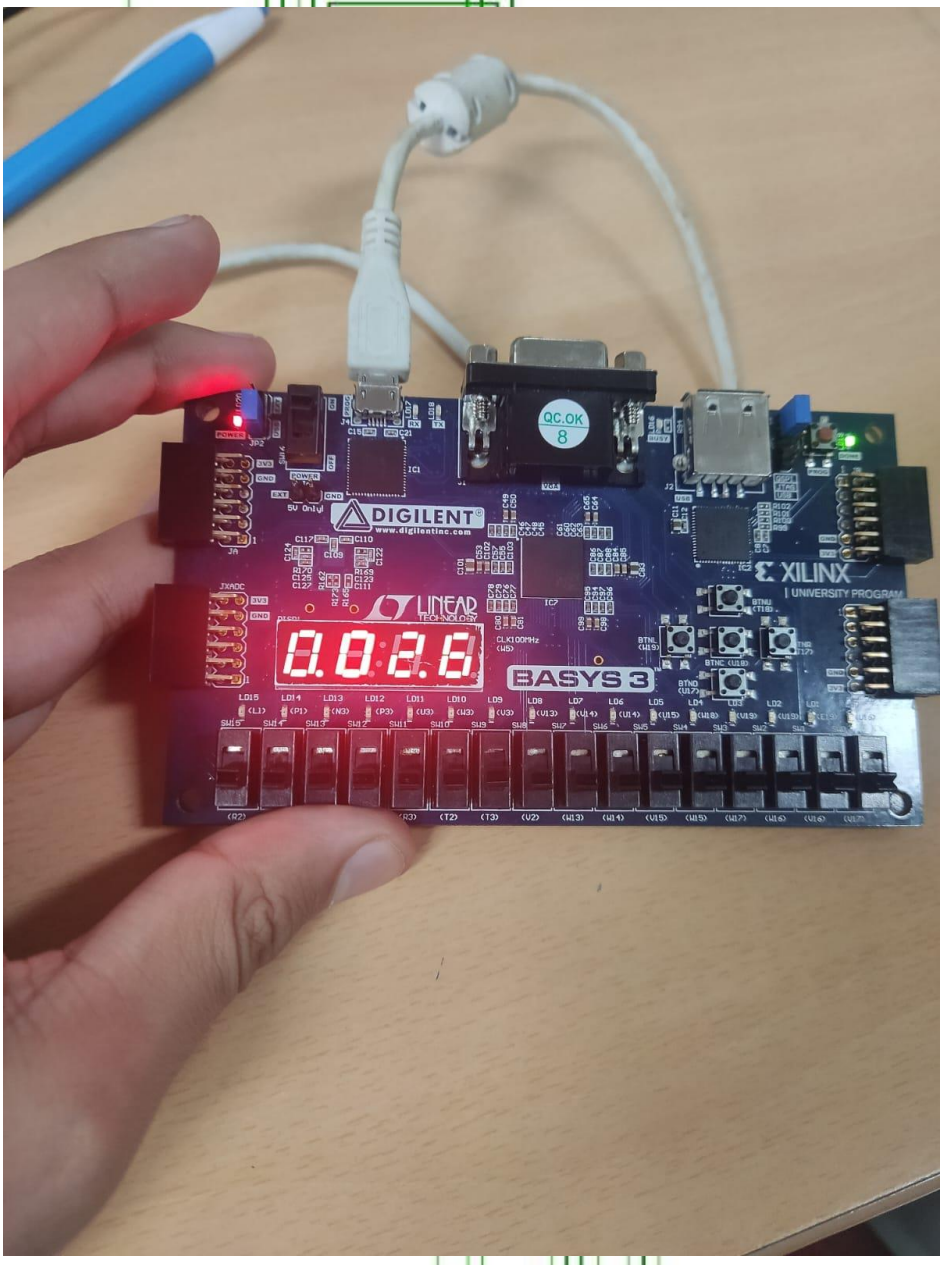
We have created 4 intermediate variables storing the value of the one tenths, the one's digit of seconds, the ten's digit of seconds and the value of minutes. Then using if-else statements, we have created the logic of changing the time according to our counter. After 10^7 cycles of our counter , the time passed/ incremented in our stopwatch is 0.1s (,i.e, has a frequency of 10hz). Now we create 4 vectors, each of 4 bits. These vectors have their value assigned according to minutes,seconds_1,seconds_2,onetenth. These 4 vectors are the output of stopwatch.vhd

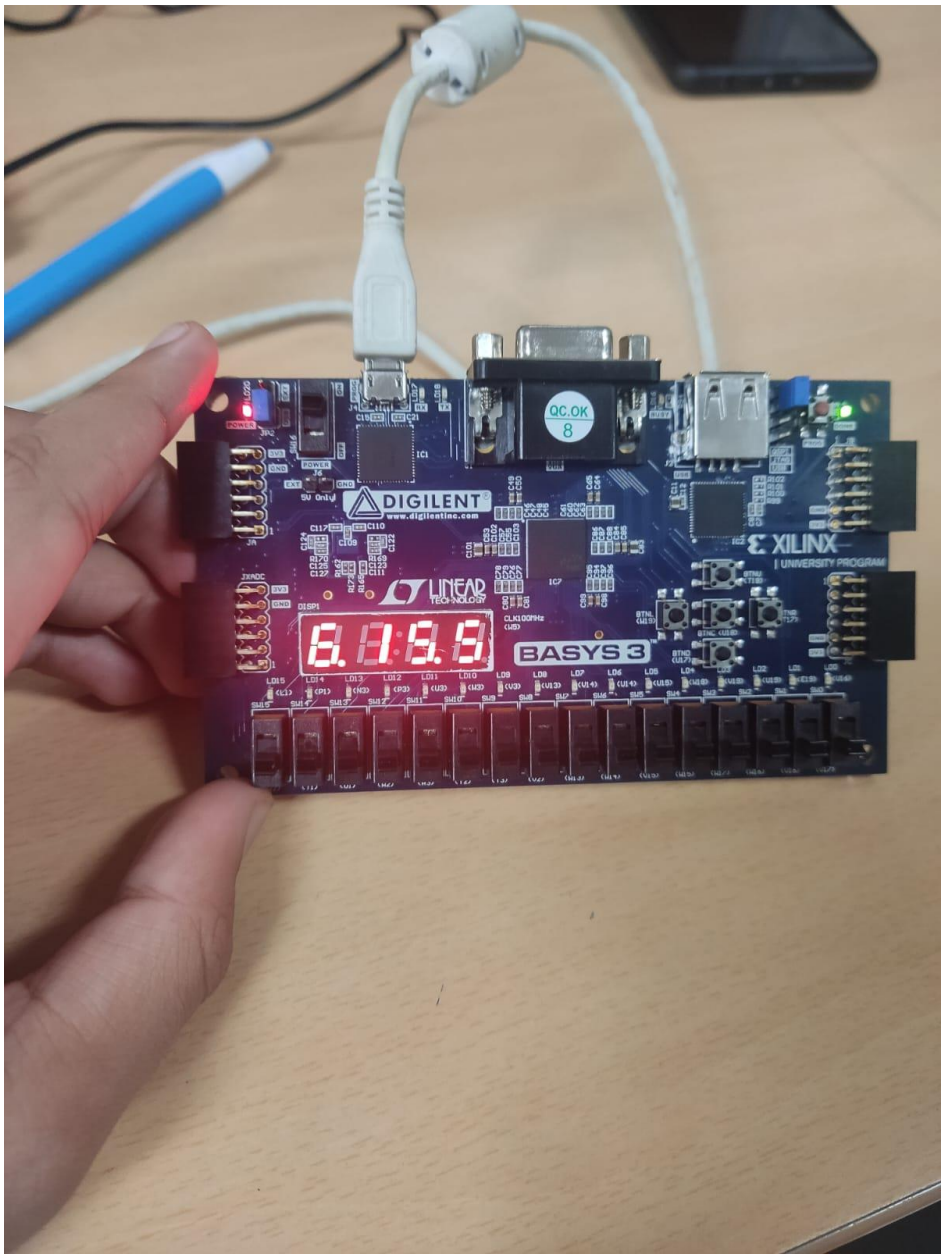
We have also used an intermediate signal called enable_switch to create processes for start switch, pause switch, continue switch and reset switch.

- start: When start switch moves from 0 → 1, then enable watch should be set to HIGH.
- pause: When pause switch moves from 0 → 1, then enable watch is set to LOW.
- continue: When continue switch moves from 0 → 1, then enable watch should be set to HIGH again. Note, continue state should only come after pause.
- reset: On reset from 0 → 1, reset watch should be set to HIGH and the stopwatch counter should be reset to 0:00:0.

- assignment2.vhd:

In this we part , we use assignment 1 and stopwatch as components. We use the output from stopwatch as an input for the assignment 1 which helps us to display this on the BASYS 3 board.


DIGILENT
www.digilentinc.com
XILINX
UNIVERSITY PROGRAM
LINEAR TECHNOLOGY
BASYS 3
QC.OK
8


QC.OK
8
DIGILENT
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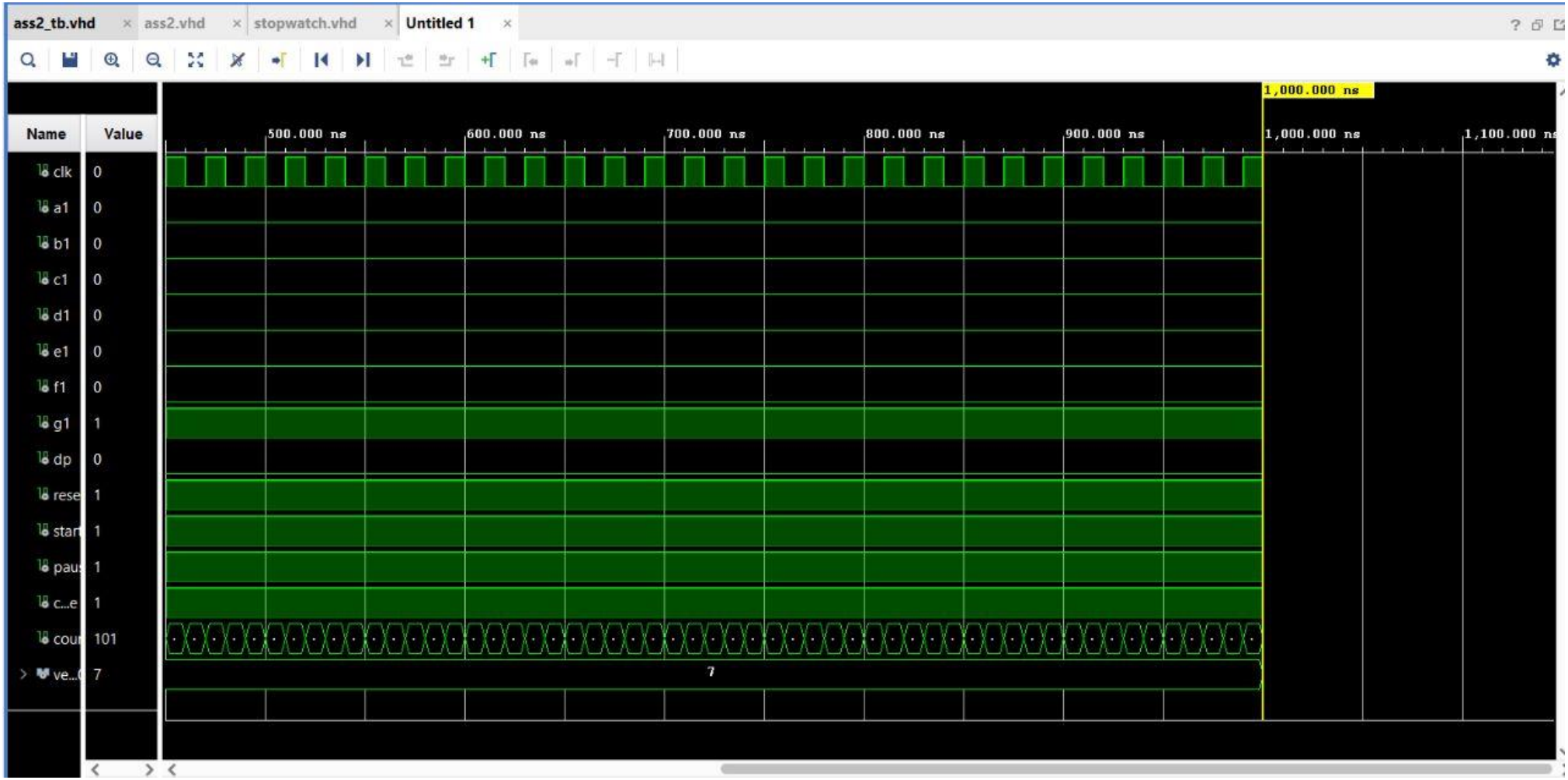
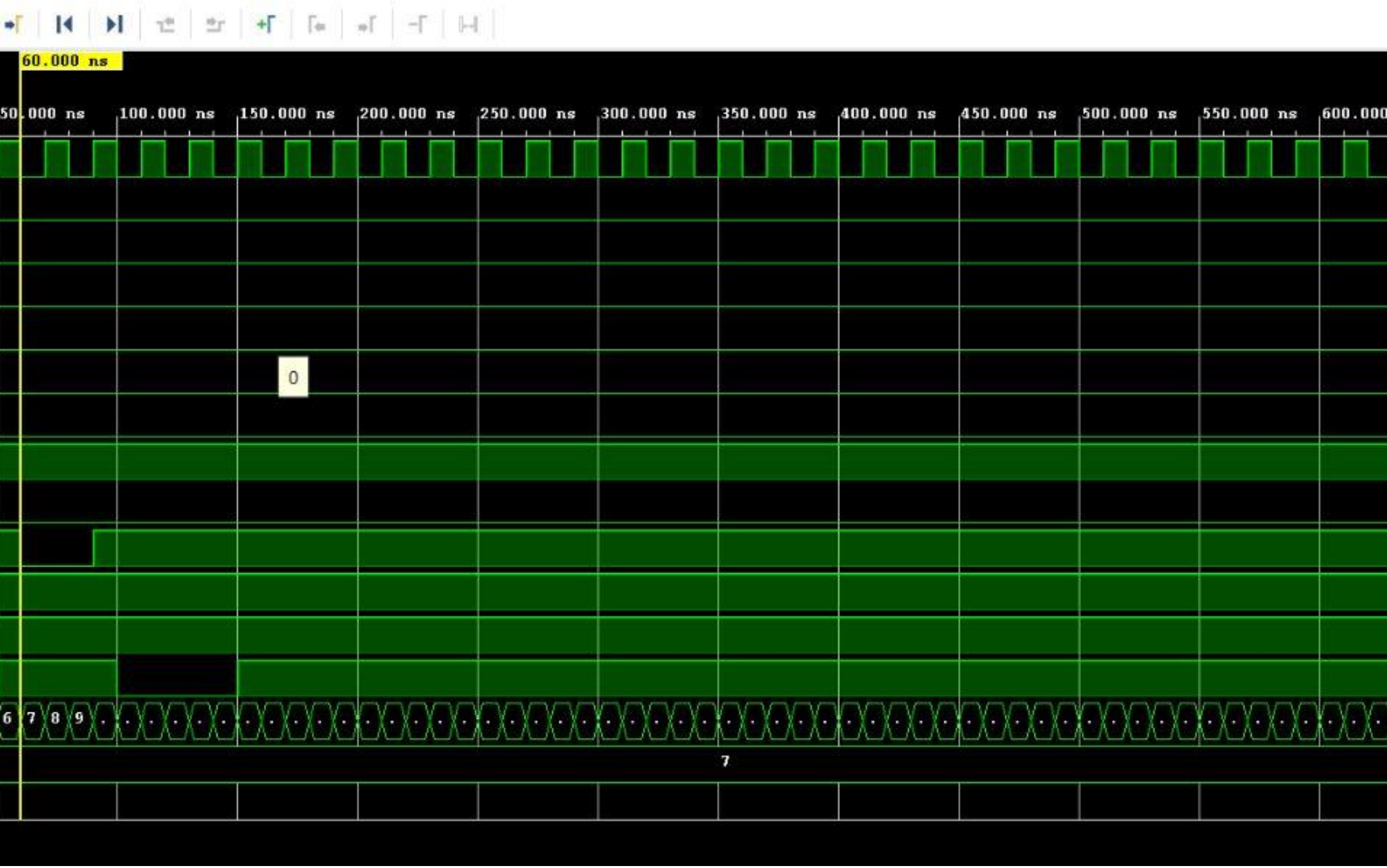

ass2_tb.vhd
ass2.vhd
stopwatch.vhd
Untitled 1
Name
Value
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
1,000.000 ns
1,100.000 ns
clk 0
a1 0
b1 0
c1 0
d1 0
e1 0
f1 0
g1 1
dp 0
rese 1
start 1
paus 1
c...e 1
cou 101
ve... 7
7


60.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns
400.000 ns
450.000 ns
500.000 ns
550.000 ns
600.000
0
6
7
8
9
7

SYNTHESIS REPORT

#---

Vivado v2022.1 (64-bit)

SW Build 3526262 on Mon Apr 18 15:48:16 MDT 2022

IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022

Start of session at: Sun Oct 30 23:38:30 2022

Process ID: 13548

Current directory: C:/Users/akash/rishi/rishi.runs/synth_1

Command line: vivado.exe -log ass2.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source ass2.tcl

Log file: C:/Users/akash/rishi/rishi.runs/synth_1/ass2.vds

Journal file: C:/Users/akash/rishi/rishi.runs/synth_1\vivado.jou

Running On: LAPTOP-B31CR9JH, OS: Windows, CPU Frequency: 3110 MHz, CPU Physical cores: 4, Host memory: 8375 MB

#---

source ass2.tcl -notrace

Command: read_checkpoint -auto_incremental -incremental C:/Users/akash/rishi/rishi.srcs/utils_1/imports/synth_1/ass2_tb.dcp

INFO: [Vivado 12-5825] Read reference checkpoint from C:/Users/akash/rishi/rishi.srcs/utils_1/imports/synth_1/ass2_tb.dcp for incremental synthesis

INFO: [Vivado 12-7989] Please ensure there are no constraint changes

Command: synth_design -top ass2 -part xc7a35tcpg236-1

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'

INFO: [Device 21-403] Loading part xc7a35tcpg236-1

INFO: [Designutils 20-5440] No compile time benefit to using incremental synthesis; A full resynthesis will be run

INFO: [Designutils 20-4379] Flow is switching to default flow due to incremental criteria not met. If you would like to alter this behaviour and have the flow terminate instead, please set the following parameter config_implementation {autoIncr.Synth.RejectBehavior Terminate}

INFO: [Synth 8-7079] Multithreading enabled for synth_design using a maximum of 2 processes.

INFO: [Synth 8-7078] Launching helper process for spawning children vivado processes

INFO: [Synth 8-7075] Helper process launched with PID 15864

Starting RTL Elaboration : Time (s): cpu = 00:00:05 ; elapsed = 00:00:05 . Memory (MB): peak = 1637.258 ; gain = 0.000

INFO: [Synth 8-638] synthesizing module 'ass2' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/ass2.vhd:24]

INFO: [Synth 8-3491] module 'assignment1' declared at 'C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/assignment1.vhd:4' bound to instance 'design1' of component 'assignment1' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/ass2.vhd:59]

INFO: [Synth 8-638] synthesizing module 'assignment1' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/assignment1.vhd:24]

INFO: [Synth 8-256] done synthesizing module 'assignment1' (0#1) [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/assignment1.vhd:24]

INFO: [Synth 8-3491] module 'stopwatch' declared at 'C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/stopwatch.vhd:4' bound to instance 'design2' of component 'stopwatch' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/ass2.vhd:65]

INFO: [Synth 8-638] synthesizing module 'stopwatch' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/stopwatch.vhd:15]

INFO: [Synth 8-256] done synthesizing module 'stopwatch' (0#1) [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/stopwatch.vhd:15]

INFO: [Synth 8-256] done synthesizing module 'ass2' (0#1) [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/ass2.vhd:24]

WARNING: [Synth 8-7129] Port pause in module stopwatch is either unconnected or has no load

WARNING: [Synth 8-7129] Port continue in module stopwatch is either unconnected or has no load

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Finished RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed = 00:00:07 . Memory (MB): peak = 1637.258 ; gain = 0.000

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:07 ; elapsed = 00:00:07 . Memory (MB): peak = 1637.258 ; gain = 0.000

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:07 . Memory (MB): peak = 1637.258 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.010 . Memory (MB): peak = 1637.258 ; gain = 0.000

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/basys3.xdc]

Finished Parsing XDC File [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/basys3.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/basys3.xdc]. These

constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/ass2_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/ass2_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1674.000 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.004 . Memory (MB): peak = 1674.000 ; gain = 0.000

INFO: [Designutils 20-5440] No compile time benefit to using incremental synthesis; A full resynthesis will be run

INFO: [Designutils 20-4379] Flow is switching to default flow due to incremental criteria not met. If you would like to alter this behaviour and have the flow terminate instead, please set the following parameter config_implementation {autoIncr.Synth.RejectBehavior Terminate}

Finished Constraint Validation : Time (s): cpu = 00:00:13 ; elapsed = 00:00:14 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Loading Part and Timing Information

Loading part: xc7a35tcpg236-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:13 ; elapsed = 00:00:14 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Applying 'set_property' XDC Constraints

Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:13 ; elapsed = 00:00:14 . Memory (MB): peak = 1674.000 ; gain = 36.742

WARNING: [Synth 8-327] inferring latch for variable 'var_reg' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/assignment1.vhd:50]

WARNING: [Synth 8-327] inferring latch for variable 'dp_reg' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/assignment1.vhd:49]

WARNING: [Synth 8-327] inferring latch for variable 'vec_reg' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/assignment1.vhd:48]

WARNING: [Synth 8-327] inferring latch for variable 'cw0_reg' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/stopwatch.vhd:163]

WARNING: [Synth 8-327] inferring latch for variable 'cw1_reg' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/stopwatch.vhd:144]

WARNING: [Synth 8-327] inferring latch for variable 'cw2_reg' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/stopwatch.vhd:117]

WARNING: [Synth 8-327] inferring latch for variable 'cw3_reg' [C:/Users/akash/OneDrive - IIT Delhi/Desktop/assign2/stopwatch.vhd:90]

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:14 ; elapsed = 00:00:14 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start RTL Component Statistics

Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 4

2 Input 24 Bit Adders := 1

+---Registers :

32 Bit Registers := 4

24 Bit Registers := 1

1 Bit Registers := 2

+---Muxes :

2 Input 32 Bit Muxes := 13

2 Input 24 Bit Muxes := 1

2 Input 4 Bit Muxes := 3

4 Input 4 Bit Muxes := 1

10 Input 4 Bit Muxes := 3

6 Input 4 Bit Muxes := 1

2 Input 1 Bit Muxes := 20

7 Input 1 Bit Muxes := 1

Finished RTL Component Statistics

Start Part Resource Summary

Part Resources:

DSPs: 90 (col length:60)

BRAMs: 100 (col length: RAMB18 60 RAMB36 30)

Finished Part Resource Summary

Start Cross Boundary and Area Optimization

WARNING: [Synth 8-7080] Parallel synthesis criteria is not met

WARNING: [Synth 8-7129] Port pause in module ass2 is either unconnected or has no load

WARNING: [Synth 8-7129] Port continue in module ass2 is either unconnected or has no load

WARNING: [Synth 8-3332] Sequential element (design2/cw1_reg[0]) is unused and will be removed from module ass2.

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:17 ; elapsed = 00:00:18 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:23 ; elapsed = 00:00:24 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Technology Mapping

WARNING: [Synth 8-3332] Sequential element (design1/var_reg[3]) is unused and will be removed from module ass2.

WARNING: [Synth 8-3332] Sequential element (design1/var_reg[2]) is unused and will be removed from module ass2.

WARNING: [Synth 8-3332] Sequential element (design1/var_reg[1]) is unused and will be removed from module ass2.

WARNING: [Synth 8-3332] Sequential element (design1/var_reg[0]) is unused and will be removed from module ass2.

WARNING: [Synth 8-3332] Sequential element (design1/vec_reg[3]) is unused and will be removed from module ass2.

WARNING: [Synth 8-3332] Sequential element (design1/vec_reg[2]) is unused and will be removed from module ass2.

WARNING: [Synth 8-3332] Sequential element (design1/vec_reg[1]) is unused and will be removed from module ass2.

WARNING: [Synth 8-3332] Sequential element (design1/vec_reg[0]) is unused and will be removed from module ass2.

Finished Technology Mapping : Time (s): cpu = 00:00:23 ; elapsed = 00:00:24 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:27 ; elapsed = 00:00:28 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:27 ; elapsed = 00:00:28 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:27 ; elapsed = 00:00:28 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:27 ; elapsed = 00:00:28 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:27 ; elapsed = 00:00:28 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:27 ; elapsed = 00:00:28 . Memory (MB): peak = 1674.000 ; gain = 36.742

Start Writing Synthesis Report

Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 44|

|3 |LUT1 | 4|

|4 |LUT2 | 74|

|5 |LUT3 | 14|

|6 |LUT4 | 35|

|7 |LUT5 | 14|

|8 |LUT6 | 48|

|9 |FDRE | 175|

|10 |LD | 15|

|11 |LDC | 1|

|12 |IBUF | 3|

|13 |OBUF | 12|

+------+-------+------+

Finished Writing Synthesis Report : Time (s): cpu = 00:00:27 ; elapsed = 00:00:28 . Memory (MB): peak = 1674.000 ; gain = 36.742

Synthesis finished with 0 errors, 0 critical warnings and 19 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:18 ; elapsed = 00:00:26 . Memory (MB): peak = 1674.000 ; gain = 0.000

Synthesis Optimization Complete : Time (s): cpu = 00:00:27 ; elapsed = 00:00:28 . Memory (MB): peak = 1674.000 ; gain = 36.742

INFO: [Project 1-571] Translating synthesized netlist

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.004 . Memory (MB): peak = 1680.086 ; gain = 0.000

INFO: [Netlist 29-17] Analyzing 60 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1684.785 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

A total of 16 instances were transformed.

LD => LDCE: 15 instances

LDC => LDCE: 1 instance

Synth Design complete, checksum: 11d157e9

INFO: [Common 17-83] Releasing license: Synthesis

29 Infos, 21 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:30 ; elapsed = 00:00:32 . Memory (MB): peak = 1684.785 ; gain = 47.527

INFO: [Common 17-1381] The checkpoint 'C:/Users/akash/rishi/rishi.runs/synth_1/ass2.dcp' has been generated.

INFO: [runtcl-4] Executing : report_utilization -file ass2_utilization_synth.rpt -pb ass2_utilization_synth.pb

INFO: [Common 17-206] Exiting Vivado at Sun Oct 30 23:39:11 2022...