# Report HW assignment1

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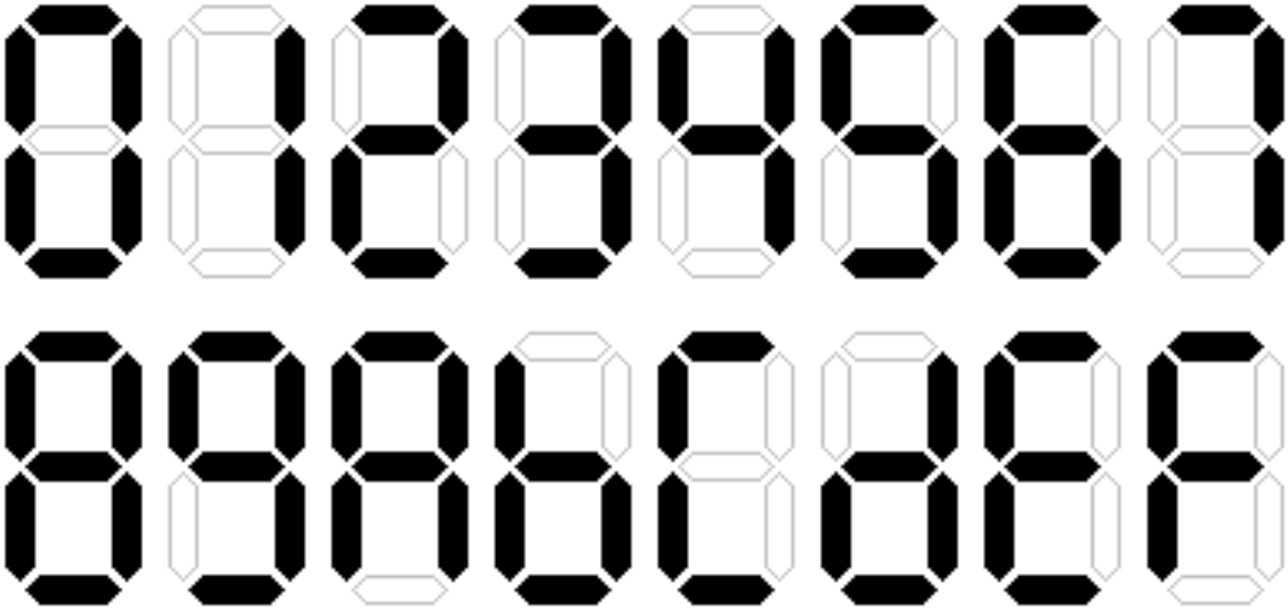
Here, In this assignment we have Designed and implemented a circuit that takes a 4-digit hexadecimal number (so each number is 4-bit) from switches in the Basys3 board and displayed it on the 4-seven segment displays on the board.

## Part 1.

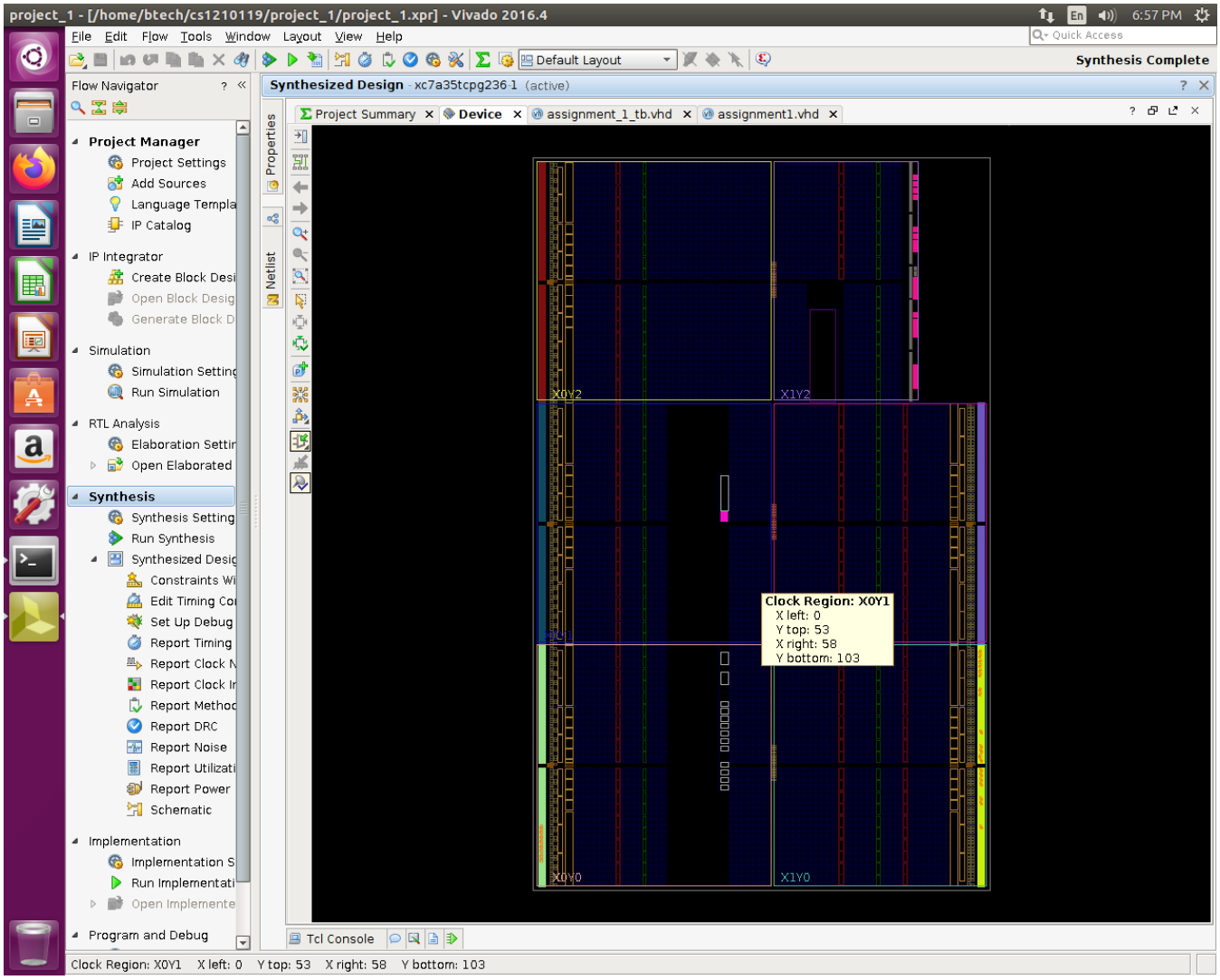
Firstly we have done implementation for 1 digit only using 4 switches on basis board and from the truth table and k-map we have decided its combinational logic (corresponding to all 7 LEDs) with minimum literals. Now in VHDL taking 4 input and 7 output considering the 4-bit anode signal such that our output digit is on first digit of 4, we have implemented the logic and made changes in Basys3 file as required. Here is a picture( from google) illustrating the visuals of digits from 0 to 15 in hexadecimal system-



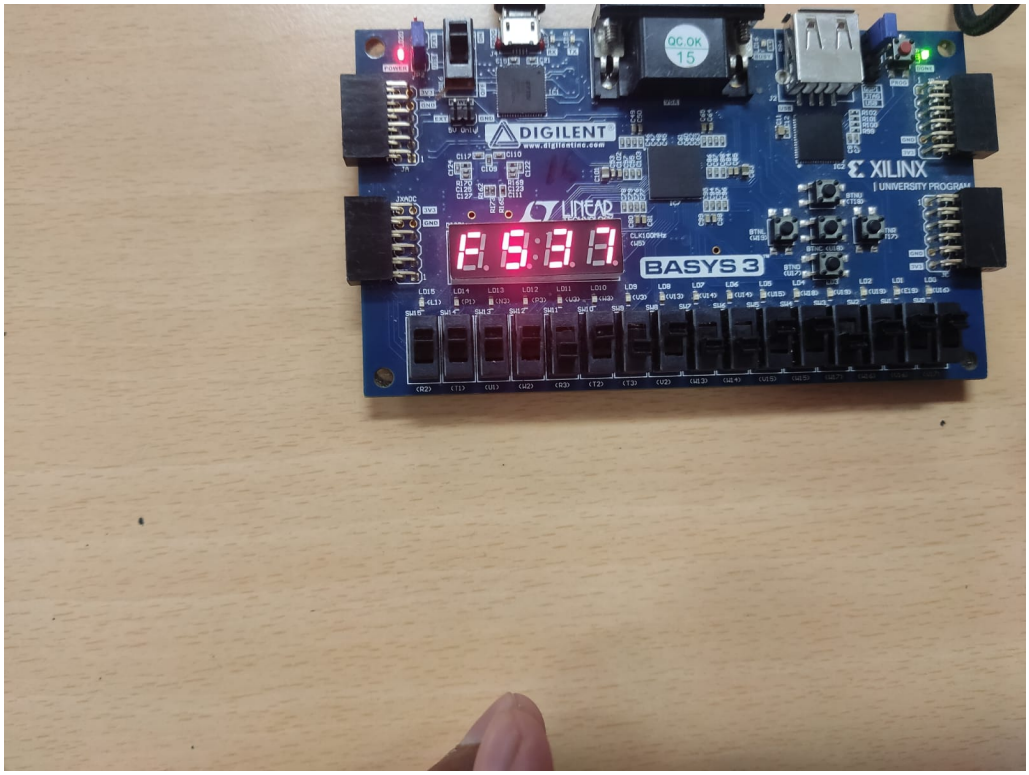
**Part 2.**

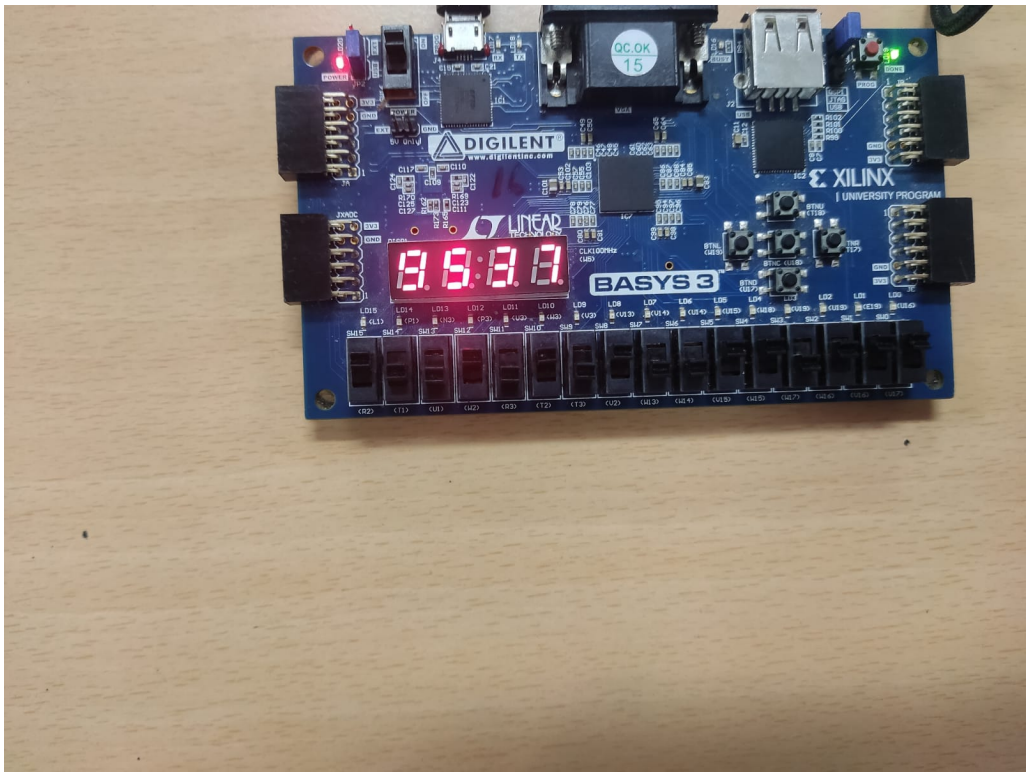
We have an input vector of size 16 , a clk variable which is representing clock, 8 outputs from a1 to g1 and an anode vector “vec” of size 4. Also we have some intermediate values where w,x,y,z are inversion of four input for a digit, var is a vector containing 4 input values for a digit display, s1 and s2 are selectors, counter is a natural number from 0 to 1200000.Now according to rising edge and counter value we will assign the value to s1 and s2. Now these selectors value will tell us that which digit we have to change after deciding the anode vector( which has been decided on the basis of s1 and s2 value).
Now we have implemented the minimised combinational logic for 7-segment display out of our current input of 4-size vector “var”.

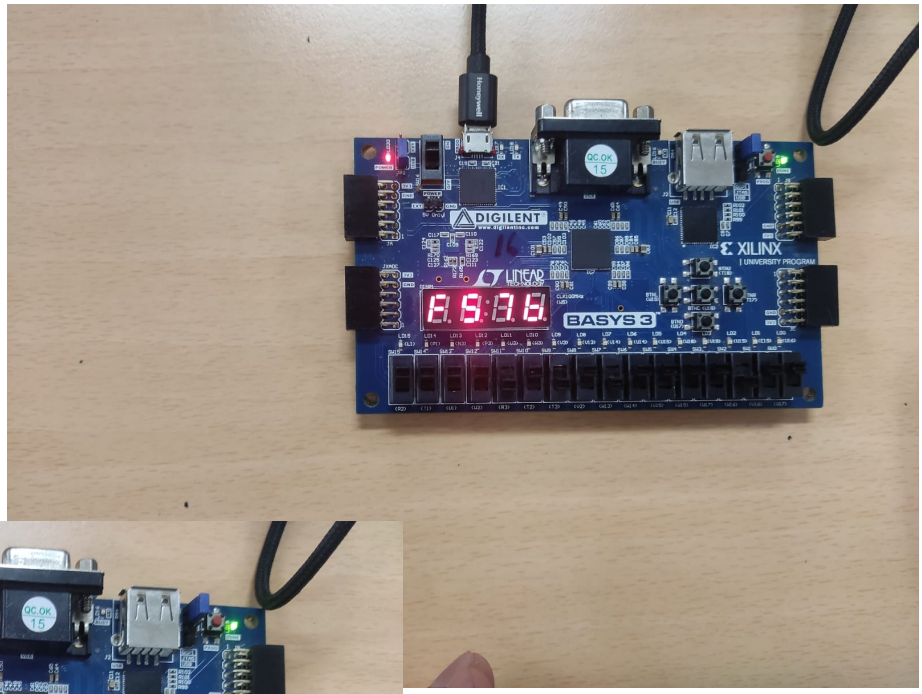
Now here is the synthesised design of my code-

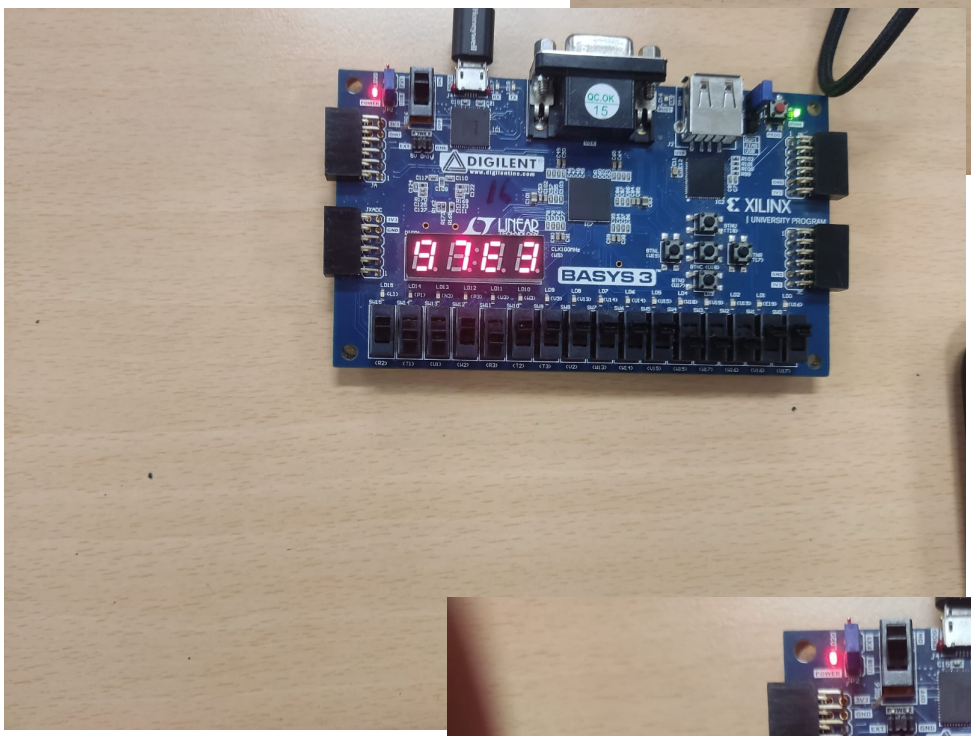


Some Basis Board Outputs-




DIGILENT
XILINX
BASYS 3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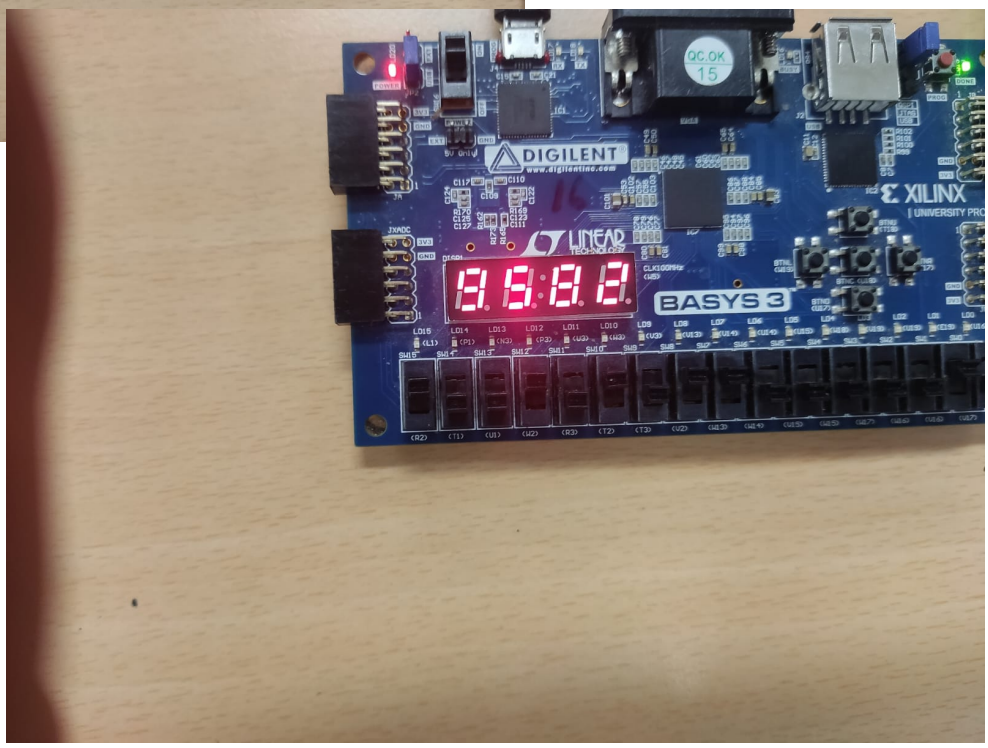
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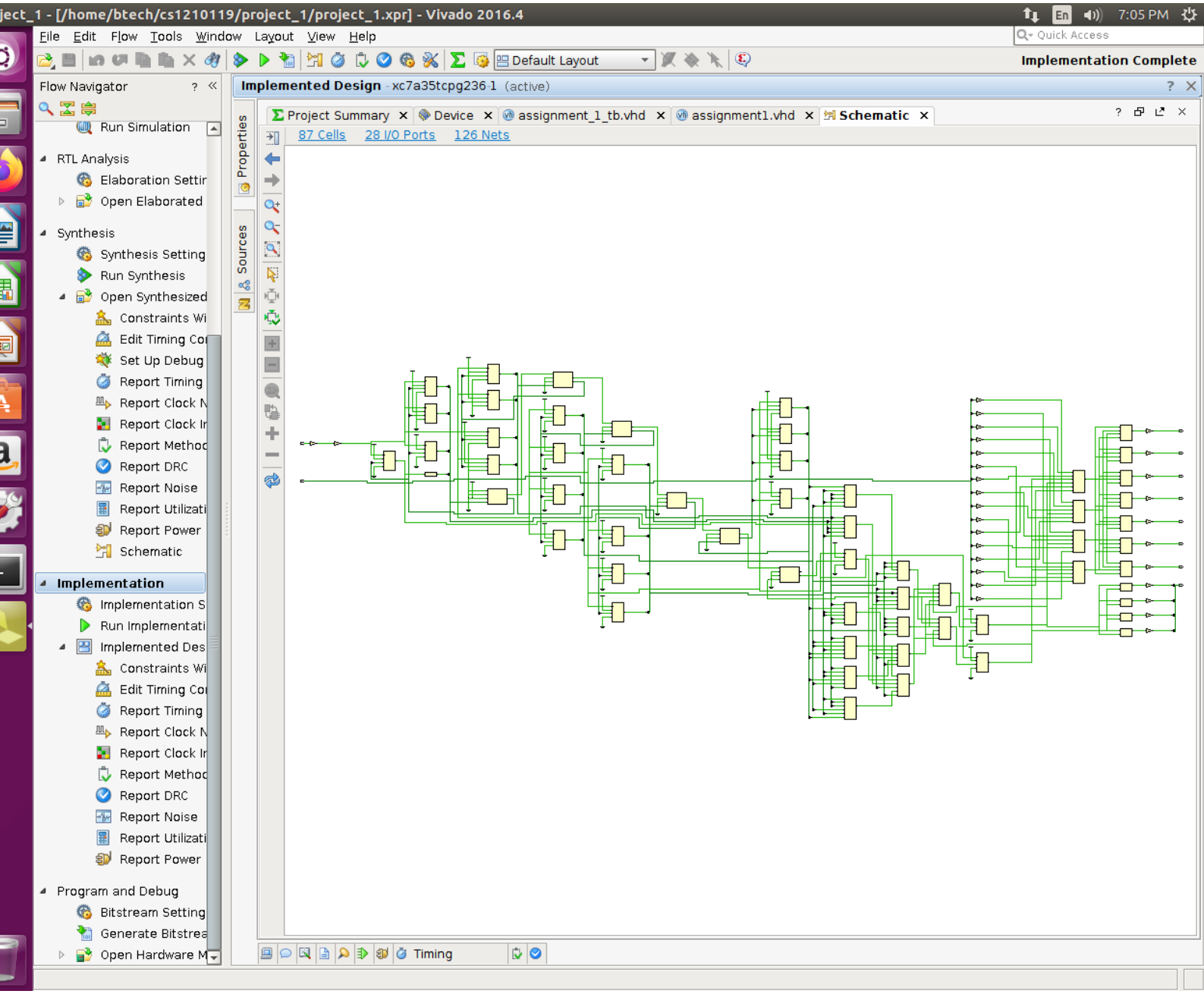
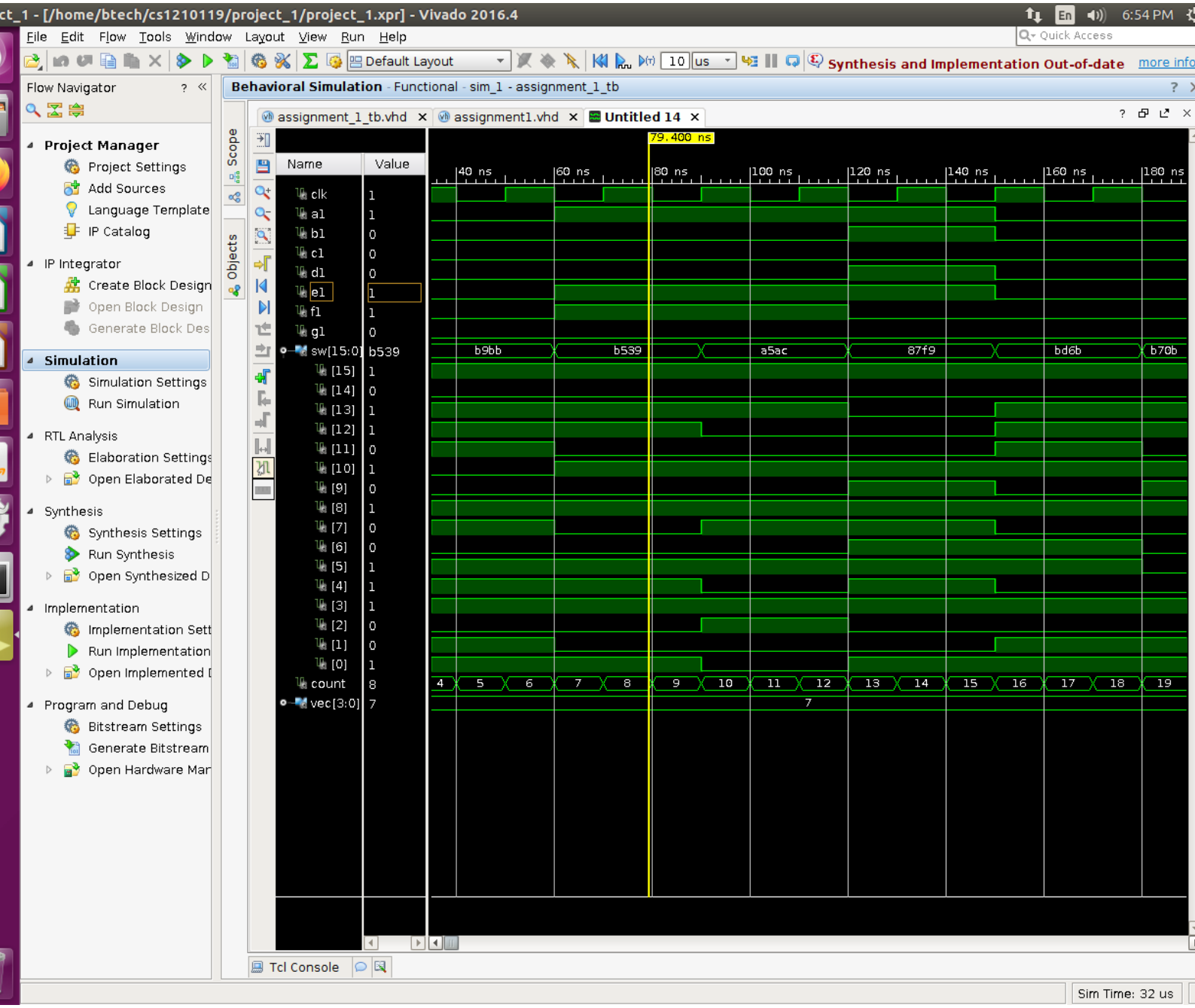
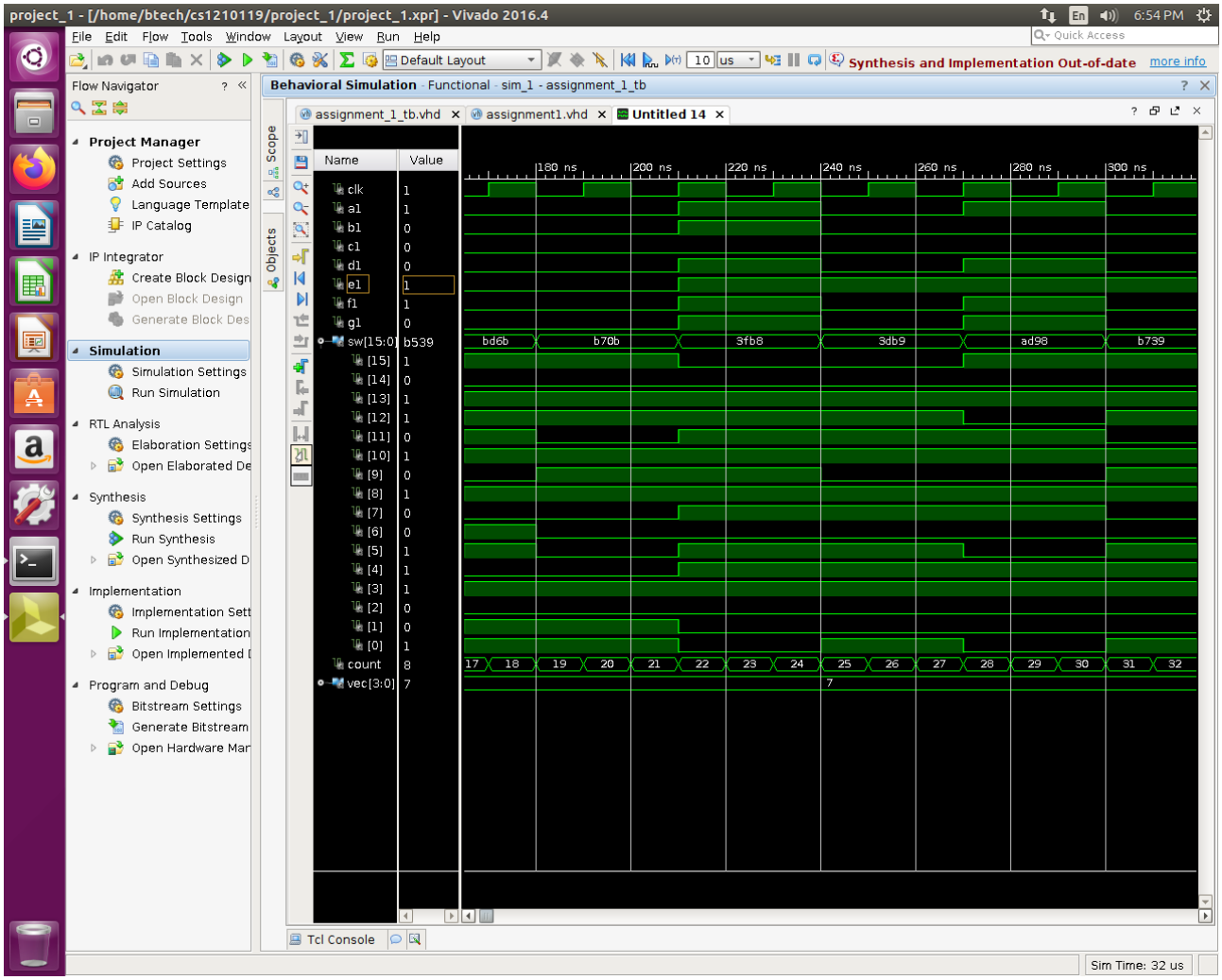
# Implementation-



# Some of simulation after running over testbenches-




project_1 - [/home/btech/cs1210119/project_1/project_1.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Run Help
Default Layout
Synthesis and Implementation Out-of-date
more info
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Des
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated De
Synthesis
Synthesis Settings
Run Synthesis
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Implementation
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Open Implemented D
Program and Debug
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Behavioral Simulation - Functional - sim_1 - assignment_1_tb
assignment_1_tb.vhd
assignment1.vhd
Untitled 14
Scope
Objects
Name
Value
clk 1
a1 1
b1 0
c1 0
d1 0
e1 1
f1 1
g1 0
sw[15:0] b539
[15] 1
[14] 0
[13] 1
[12] 1
[11] 0
[10] 1
[9] 0
[8] 1
[7] 0
[6] 0
[5] 1
[4] 1
[3] 1
[2] 0
[1] 0
[0] 1
count 8
vec[3:0] 7
180 ns
200 ns
220 ns
240 ns
260 ns
280 ns
300 ns
bd6b
b70b
3fb8
3db9
ad98
b739
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
7
Tcl Console
Sim Time: 32 us