	Computer System Architecture	L	T	P	C
Version 1.0		3	0	0	3
Pre-requisites/Exposure	Basic Knowledge of Computers, Digital Electronics				
Co-requisites	--				

Course Objectives

1. To develop understanding of Computer Models and its usage.
2. To develop understanding of ALU Design.
3. To conceptualize the understanding of Control Unit design, Memory, IPC, Control Design.
4. To develop understanding of Memory & Input/output organization Overview.

Course Outcomes

On completion of this course, the students will be able to

CO1 Identify Functional Units, Bus Structure and Addressing Modes.
CO2 Design Digital Components including – Decoder, Multiplexer and Arithmetic Circuits and Design Arithmetic and Control Unit.
CO3 Design the Hardwired & Microprogrammed Control Unit.
CO4 Identify the Memory Hierarchy and its Performance and Interface I/O devices.

Catalog Description

Overview of the structure, elements and analysis of modern enterprise computers. Performance evaluation of commercial computing. Past and emerging technology trends. Impact of parallelism at multiple levels of computer architecture. Memory and storage. Fundamental computer system descriptions, Amdahl's Law, Flynn's Taxonomy.

A senior level elective in computer organization is a standard part of most computer engineering and computer science programs. While all (Civil, CPE and CS students get a basic foundation in computer organization in lower-level required courses, students who wish to pursue careers or graduate study in computer architecture or computer systems need an advanced course that covers the principles and contemporary trends in computer organization.

Course Content

Unit I: Introduction 11 lecture hours
Evolution of Computer Systems, Von Neumann Architecture, Moore's Law, Computer Types, Functional Units, Devices (Input, Output, Storage & Communication Devices), Memory System (RAM, ROM, Cache, VM, etc.), Introduction to Logic Gates, Truth Table, K-Map, Latch Flip Flops (J, K & D), Encoder & Decoder, MUX & DEMUX, Registers & Counters, Binary Number system, Overview of RISC/CISC, RISC vs. CISC.

Unit II: ALU Design 8 lecture hours
Computer Organization and Design, Instruction Codes, Op-Code, Computer registers, Computer Instructions, CPU stack Organization, Instruction Formats, Instruction types, Timing and control, Instruction and Instruction sequencing, Instruction Cycle, Memory Reference Instructions,Addressing modes, Program Control,Types of Interrupts, Adder &Subtractor.

Unit III: Control Unit Design 8 lecture hours
Introduction, Instruction Interpretation & Execution, Control Transfer, Fetch Cycle, Micro programmed Control, Control Memory, Micro programmed vs. Hardwired Control Unit, Nano Programming, Superscalar processing.

Unit IV: Memory Organization 4 lecture hours

Memory Locations & Addresses, Semiconductor Memory, Static and Dynamic Memory, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Secondary Memories: Optical Magnetic Tape, Magnetic Disk and Controllers.

Unit V: Input / Output Organization 5 lecture hours

I/O and their brief description, Bus Interface, Bus arbitration, Data Transfer, Types of Interrupts, I/O Interrupts, Channels, Direct Memory Access, I/O processing.

Text Books

1. "Computer System Architecture", 3rd edition, M. Morris Mano, Pearson Publications.

Reference Books

1. "Computer Organization and Architecture", Sixth Edition, William Stallings, Pearson Publications.

2. "Fundamental of Digital electronics", second edition, A. Anand Kumar, PHI publications

3. "Computer Organization and Architecture", Third Edition, John P. Hayes, TATA McGraw-Hill.

Modes of Evaluation: Quiz/Assignment/ presentation/ extempore/ Written Examination

Examination Scheme:

Components	Internal	Mid Term	ESE	Total
Weightage (%)	30%	20%	50%	100%

Relationship between the Course Outcomes (COs), Program Outcomes (POs) and Program Specific Objectives(PSOs)

Course Outcomes	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2	PS O3
CO1							1								
CO2								2							
CO3									2						
CO4												2			
Average							1	2	2			2			

1: Weak 2: Moderate 3: Strong