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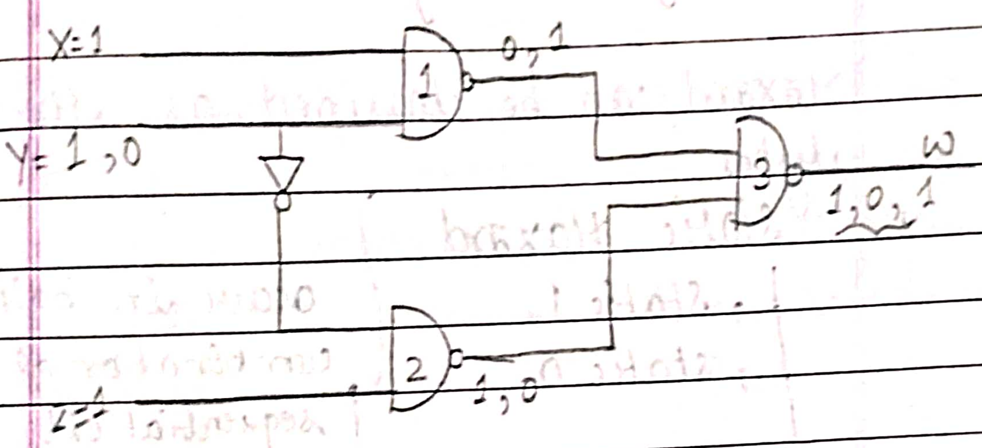
Unit - 3

Hazards



Hazard are unwanted switching transient that may appear at the O/P of ckt bcz different path exhibit different propagation delay such transient are called as 'glitch' Hazard occur both in combinational ckt as well as sequential ckt.

Consider the case when X, Y, Z = 1 the O/P (ω) will be 1, now the I/P Y is changed from 1 to 0, the ckt O/P should remain constant but it may go at logic 0 for a moment if the o/p switch in the following sequence.

- Gate 1 O/P goes to 1, then Gate 3 O/P goes to 0
- When the inverted O/P goes to 1

then Gate 2 output goes to 0 & finally the ckt O/P goes to 1

Classification of Hazards.

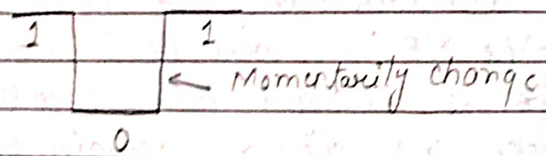
Hazard can be classified as three types :

1. Static Hazard.
   - Static 1
   - Static 0
2. Dynamic Hazard.
3. Essential Hazard

Static Hazard and Dynamic Hazard: occur in both combination as & sequential ckt

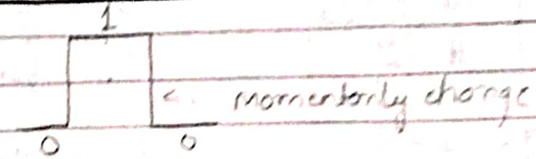
Essential Hazard → occur in sequential ckt.

1 Static 1 Hazard



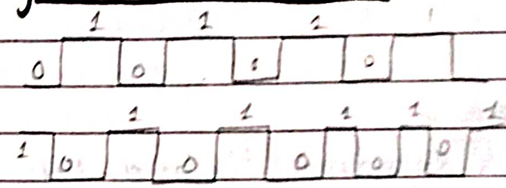
In response to I/P change & for some combination of propogation delay a logic ckt may go to 0 when it should remain constant at 1, this transient is called Static 1 Hazard.

• Static 0 Hazard



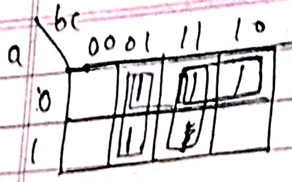
In response to I/P change & some combination propogation delay a logic ckt may go to 1, when it should remain constant at 0. This transient is called as Static 0 Hazard.

• Dynamic Hazard



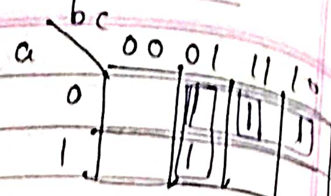
This Hazard appear both in sequential as well as combinational ckt. When the O/P of logic ckt is change from 0 to 1 to 0 or from 1 to 0 to 1. These two O/P may change more no. of time; this transient is called as 'Dynamic Hazard.

Prevention of Static & Dynamic Hazard.



$Y = \bar{a}b + \bar{b}c$

fig.(a)



$Y = \bar{b}c + \bar{a}c + \bar{a}b$

fig.(c)

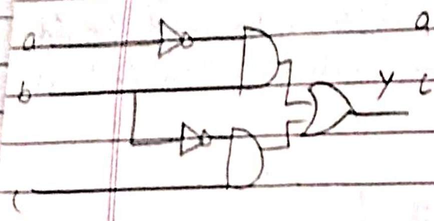
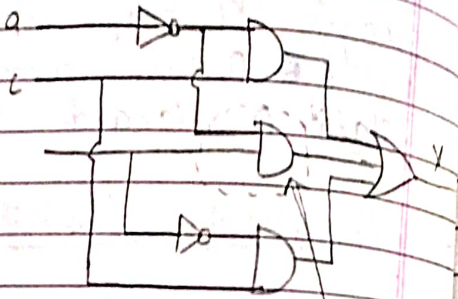


fig (b)

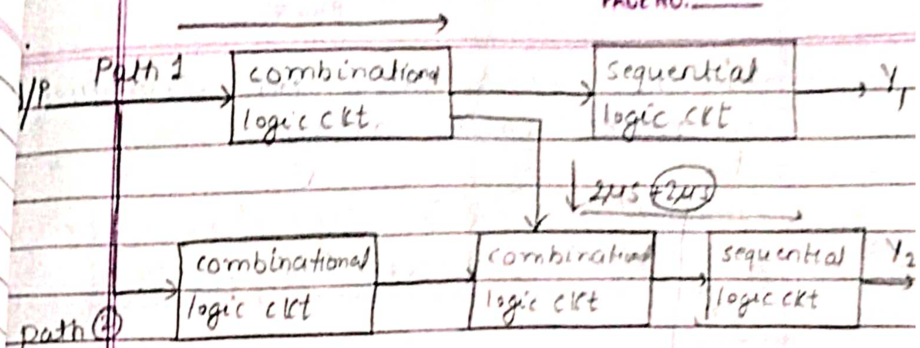


fig(d)

Extra gate

Static & Dynamic Hazard can be prevented by adding extra gate in the ckt as the redundant term. fig (b) shows the logic ckt with Hazard problem which can be prevented by adding extra gate. fig (d) represent the Hazard free logic ckt.

3 Essential Hazard



for preventing Hazard we add it

The static & Dynamic Hazard can occur in combinational as well as sequential ckt while essential Hazard occur only in sequential ckt.

Let there be more than 1 path from the I/P to the O/P of the logic ckt as shown in fig. we find that there are two O/P path that contain combinational logic ckt & sequential logic ckt. It may so happen that certain path may produce more delay than the other. The delay in the O/P is known as Essential Hazard.

The only way to prevent the essential Hazard is by introducing the same amount of delay in all the path from I/P to O/P

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for this extra gates are introduce to make equal delay.

Difference b/w Synchronous & Asynchronous sequential ckt

Synchronous sequential ckt	Asynchronous sequential ckt
• A synchronous ckt is a system whose behaviour is define from a knowledge of its signal at discrete instant of time	• The behaviour of Asynchronous ckt depends upon the order in which the I/P change & the state of ckt can be affected at any instant of time.
• Here the memory element are clocked flip-flop.	• The memory element are either unclocked flip-flop or time delay element
• Synchronisation is employed by the help of clock pulse	• Here, no synchronisation Hence it is a combi ckt with feedback

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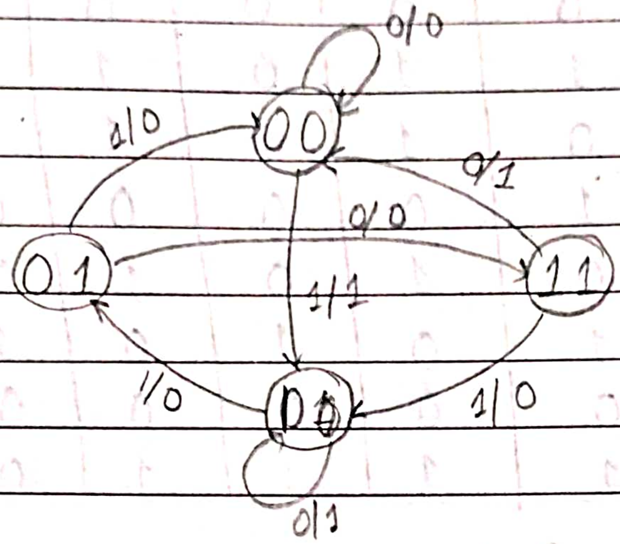
• The max^m operating speed of clock depends on Time delay Envolved.	• Bcz of absence of clock Asynchronous ckt can operate faster than synchronous ckt.
• Easier to Design	• More difficult to design.

Synthesis of Sequential Circuit

Draw the sequential ckt using D-Flip-Flop.



Step-1 : State Table

P.S		N.S				Y	
		x=0		x=1			
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}	x=0	x=1
0	0	0	0	1	0	0	1
0	1	1	1	0	0	0	0
1	0	1	0	0	1	1	0
1	1	0	0	1	0	1	0

Step-2 : Excitation Table of D-Flip-Flop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-3 Excitation Table.

P.S		I/P	N.S		F.F I/P		Y
A_n	B_n	x	A_{n+1}	B_{n+1}	D_A	D_B	
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	1	0
0	1	1	0	0	0	0	0
1	0	0	1	0	1	0	1
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	0

D_A

$A_n \backslash B_n x$	00	01	11	10
0		1		1
1	1		1	

$$D_A = \bar{A}_n\bar{B}_n x + \bar{A}_n B_n \bar{x} + A_n \bar{B}_n \bar{x} + A_n B_n x$$
$$= \bar{A}_n(B_n \oplus x) + A_n(B_n \odot x)$$
$$= \bar{A}_n(B_n \oplus x) + A_n(\overline{B_n \oplus x})$$
$$= x \oplus A_n \oplus B_n$$

D_B

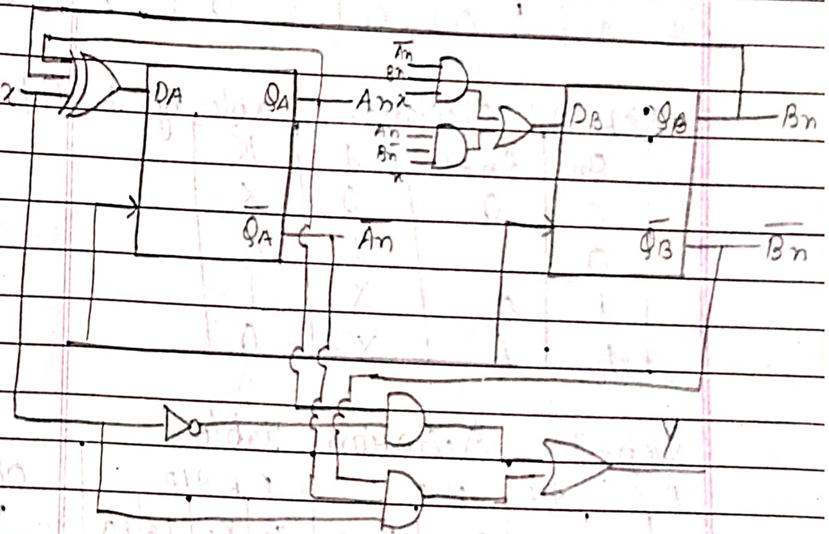
$A_n \backslash B_n x$	00	01	11	10
0				1
1	1			

$$D_B = \bar{A}_n B_n \bar{x} + A_n \bar{B}_n \bar{x}$$

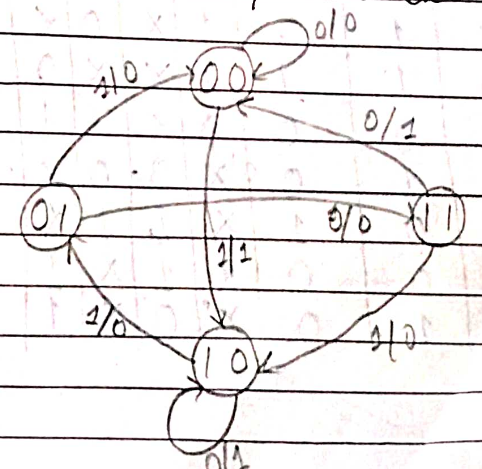
Y

$A_n \backslash B_n x$	00	01	11	10
0		1		1
1	1			1

$$Y = A_n\bar{x} + \bar{A}_n \bar{B}_n x$$



Draw the sequential ckt using JK



Step-1 : state table.

P.S		N.S $x=0$		N.S $x=1$		Y	
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}	$x=0$	$x=1$
0	0	0	0	1	0	0	1
0	1	1	1	0	0	0	0
1	0	1	0	0	1	1	0
1	1	0	0	1	0	1	0

Step-2 : Excitation Table of JK Flip Flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Excitation Table

P.S		I/P	N.S		F.F I/P				O/P (Y)
A_n	B_n	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	Y
0	0	0	0	0	0	X	0	X	0
0	0	1	1	0	1	X	0	X	1
0	1	0	1	1	1	X	X	0	0
0	1	1	0	0	0	X	X	1	0
1	0	0	1	0	X	0	0	X	1
1	0	1	0	1	X	1	1	X	0
1	1	0	0	0	X	1	X	1	1
1	1	1	1	0	X	0	X	1	0

J_A

A_n \ $B_n x$	00	01	11	10
0		1		1
1	X	X	X	X

$J_A = \bar{B_n} x + B_n \bar{x}$

$= x \oplus B_n$

J_B

A_n \ $B_n x$	00	01	11	10
0			X	X
1		1	X	X

$J_B = A_n x$

K_A

A_n \ $B_n x$	00	01	11	10
0	X	X	X	X
1		1		1

$K_A = \bar{B_n} x + B_n \bar{x}$

$= x \oplus B_n$

K_B

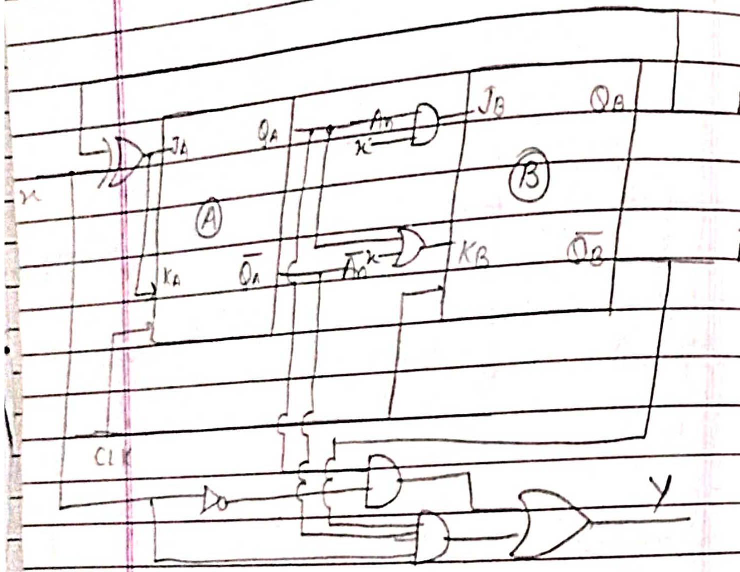
A_n \ $B_n x$	00	01	11	10
0	X	X	1	
1	X	X	1	1

$K_B = \cancel{A_n \bar{x} + B_n x}$

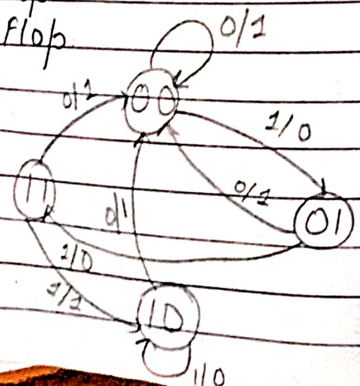
$K_B = A_n + x$

Y: An \ BnX	00	01	11	10
0		1		
1	1			1

$Y = A_n\bar{x} + \bar{A_n}B_n x$



Draw the sequential crt by using
(i) D- Flip Flop
(ii) J-K Flip Flop



Step-1 State Table

P.S		N.S				Y	
		x=0		x=1		x=0	x=1
An	Bn	An+1	Bn+1	An+1	Bn+1		
0	0	0	0	0	1	1	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	1

Step-2 Excitation Table of D-Flip Flop

On	On+1	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-3 Excitation Table

P.S		I/P	N.S		F.F I/P		Y
An	Bn	x	An+1	Bn+1	DA	DB	
0	0	0	0	0	0	0	1
0	0	1	0	0	1	0	0
0	1	0	1	1	1	1	1
0	1	1	0	0	0	0	0
1	0	0	1	0	1	0	1
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	1

DA

$A_n \backslash B_n x$	00	01	11	10
0		1		1
1	1		1	

$DA = A_n\bar{B_n}\bar{x} + \bar{A_n}\bar{B_n}x + A_nB_nx + \bar{A_n}B_n\bar{x}$

=

Step-3 Excitation Table

P.S			N.S		F.F i/p		y
A_n	B_n	x	A_{n+1}	B_{n+1}	DA	DB	
0	0	0	0	0	0	0	1
0	0	1	0	1	0	1	0
0	1	0	0	0	0	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	1

DA

$A_n \backslash B_n x$	00	01	11	10
0			1	
1		1	1	

$DA = A_nx + B_nx$

$= x(A_n + B_n)$

DB

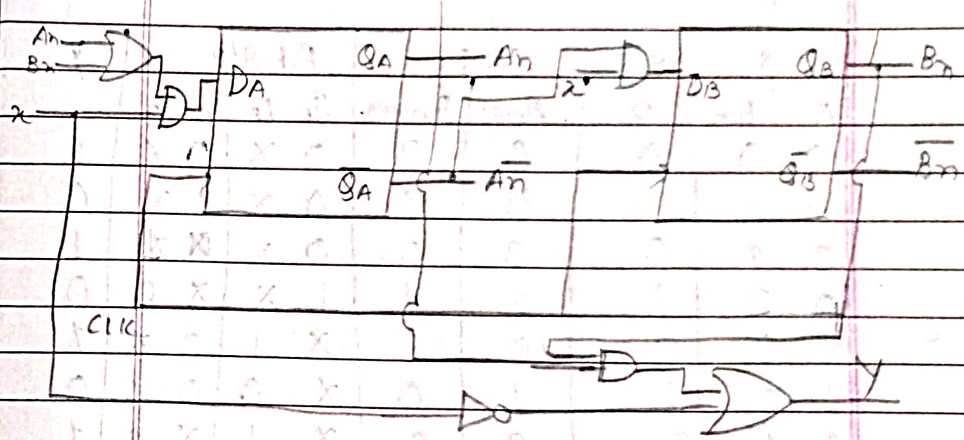
$A_n \backslash B_n x$	00	01	11	10
0		1	1	
1				

$D_B = \bar{A_n}x$

Y

$A_n \backslash B_n x$	00	01	11	10
0	1			1
1	1		1	1

$Y = \bar{x} + A_nB_n$



• Using J K Flip Flop

Step-1 State table

P.S		N.S				Y	
		x=0		x=1			
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}	x=0	x=1
0	0	0	0	0	1	1	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	1

Step-2 Excitation table of J-K flip.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Excitation Table

P.S		I/P	N.S		F.F I/P				Y
A_n	B_n	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	
0	0	0	0	0	0	X	0	X	1
0	0	1	0	1	0	X	1	X	0
0	1	0	0	0	0	X	X	1	1
0	1	1	1	1	1	X	X	0	0
1	0	0	0	0	X	1	0	X	1
1	0	1	1	0	X	0	0	X	0
1	1	0	0	0	X	1	X	1	1
1	1	1	1	0	X	0	X	1	1

J_A

A_n \ $B_n x$	00	01	11	10
0			1	
1	X	X	X	X

$J_A = B_n x$

J_B

A_n \ $B_n x$	00	01	11	10
0		1	X	X
1			X	X

$J_B = \bar{A_n} x$

K_A

A_n \ $B_n x$	00	01	11	10
0	X	X	X	X
1	1			1

$K_A = \bar{x}$

K_B

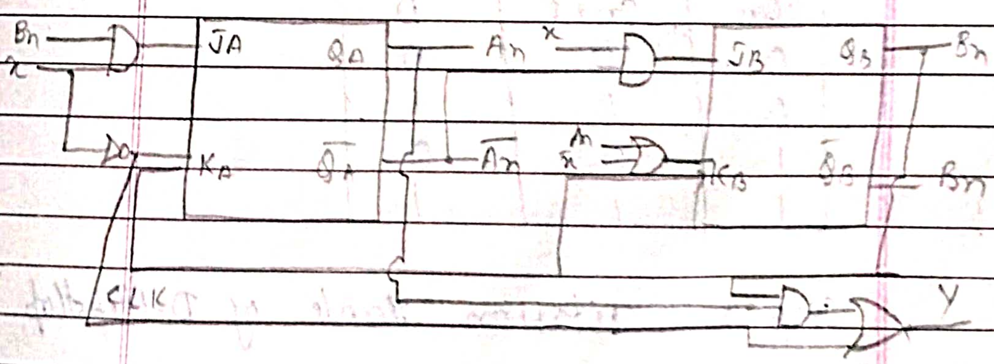
A_n \ $B_n x$	00	01	11	10
0	X	X		X
1	X	X	1	1

$K_B - A_n + \bar{x}$

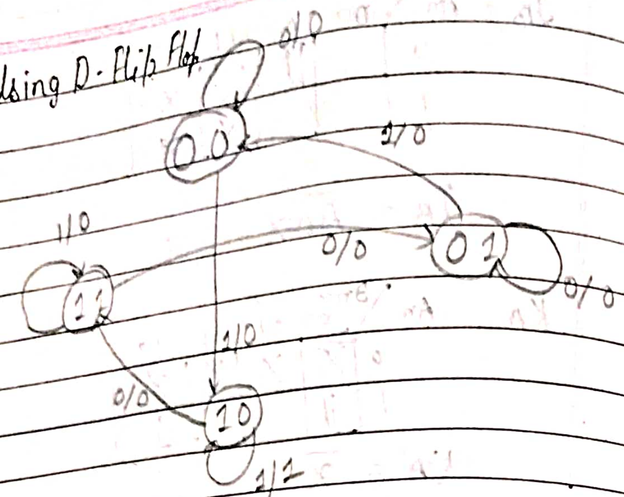
Y

A_n \ $B_n x$	00	01	11	10
0	1			1
1	1		1	1

$Y = \bar{x} + A_n B_n$.



① Using D-Flip Flop



Step-1 State Table

P.S		N.S x = 0		x = 1		O/P (Y)	
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}	x=0	x=1
0	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0
1	0	1	1	1	0	0	1
1	1	0	1	1	1	0	0

Step-2 Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-3 Excitation Table of D-Flip Flop

P.S		I/P	N.S		F.F I/P		O/P
A_n	B_n	x	A_{n+1}	B_{n+1}	D_A	D_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	1	0	1	0
0	1	1	0	0	0	0	0
1	0	0	1	1	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	1	0
1	1	1	1	1	1	1	0

D_A

A_n \ $B_n x$	00	01	11	10
0		1		
1	1	1	1	

$$D_A = A_n\overline{B_n} + A_n x + \overline{B_n} x$$
$$= A_n\overline{B_n} + x(A_n + \overline{B_n})$$

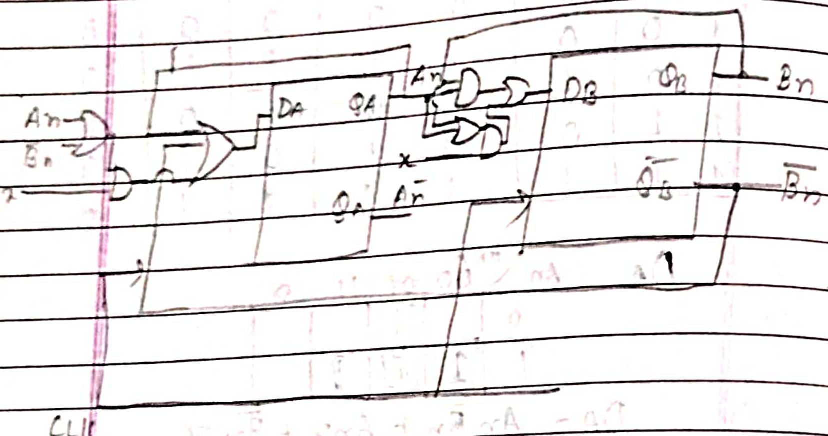
D_B.

A_n \ $B_n x$	00	01	11	10
0				1
1	1		1	1

$$D_B = A_n\bar{x} + A_n B_n + B_n\bar{x}$$
$$= \bar{x}(A_n + B_n) + A_n B_n$$

Y: An \ Bn x	00	01	11	10
0				
1			1	

$Y = A_n \overline{B_n} x$



Using J-K Flip Flop

P-8 Step-1 State Table

P.S		N.S ($x=0$)		N.S ($x=1$)		Y	
An	Bn	An+1	Bn+1	An+1	Bn+1	$x=0$	$x=1$
0	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0
1	0	1	1	1	0	0	1
1	1	0	1	1	1	0	0

Step-2 Excitation Table

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Excitation Table J K Flip Flop

P.S		I/P	N.S		F.F J.K				O/P
An	Bn	x	An+1	Bn+1	JA	KA	JB	KB	Y
0	0	0	0	0	0	X	0	X	0
0	0	1	1	0	1	X	0	X	0
0	1	0	0	1	0	X	X	0	0
0	1	1	0	0	0	X	X	1	0
1	0	0	1	1	X	0	1	X	0
1	0	1	1	0	X	0	0	X	1
1	1	0	0	1	X	1	X	0	0
1	1	1	1	1	X	0	X	0	0

JA

An \ Bn x	00	01	11	10
0		$\boxed{1}$		
1	X	$\boxed{X}$	X	X

$J_A = \overline{B_n} x$

KA

An \ Bn x	00	01	11	10
0	X	X	X	$\boxed{X}$
1				$\boxed{1}$

$K_A = B_n \overline{x}$

J_B

$A_n \backslash B_n x$	00	01	11	10
0			X	X
1	1		X	X

$J_B = A_n \bar{x}$

K_B

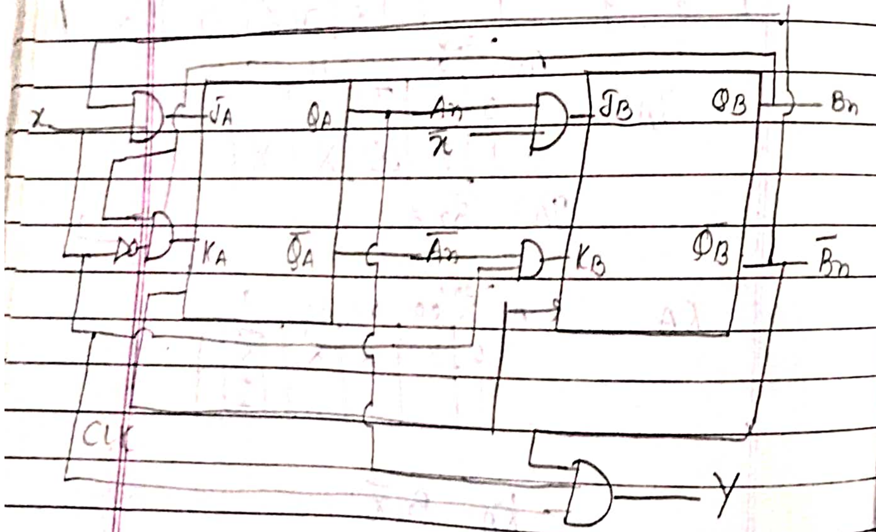
$A_n \backslash B_n x$	00	01	11	10
0	X	X	1	
1	X	X		

$K_B = \bar{A}_n x$

Y

$A_n \backslash B_n x$	00	01	11	10
0				
1		1		

$Y = A_n \bar{B}_n x$



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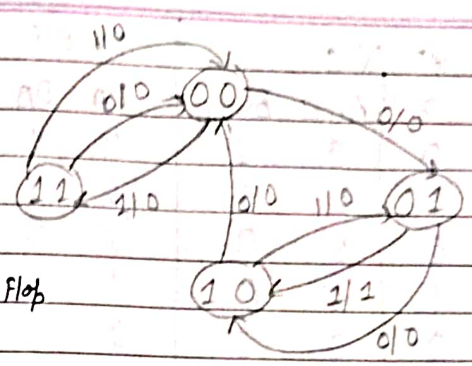


Using D-flip flop

Step-1 State Table

P.S		N.S				O/P Y	
		$x=0$		$x=1$		$x=0$	$x=1$
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}		
0	0	0	1	1	1	0	0
0	1	1	0	1	0	0	1
1	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0

Step-2 Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-3 Excitation Table of D-Flip Flop.

P.S		I/P	N.S		FF I/P		O/P Y
A_n	B_n	x	A_{n+1}	B_{n+1}	D_A	D_B	
0	0	0	0	1	0	1	0
0	0	1	1	1	1	1	0
0	1	0	1	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	0	0	0	0
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0

D_A

$A_n \backslash B_n x$	00	01	11	10
0		1	1	1
1				

$D_A = \bar{A}_n x + \bar{A}_n \cancel{\bar{x}} B_n$

$= A_n \oplus x \; \cancel{B_n}$

D_B

$A_n \backslash B_n x$	00	01	11	10
0	1	1		
1		1		

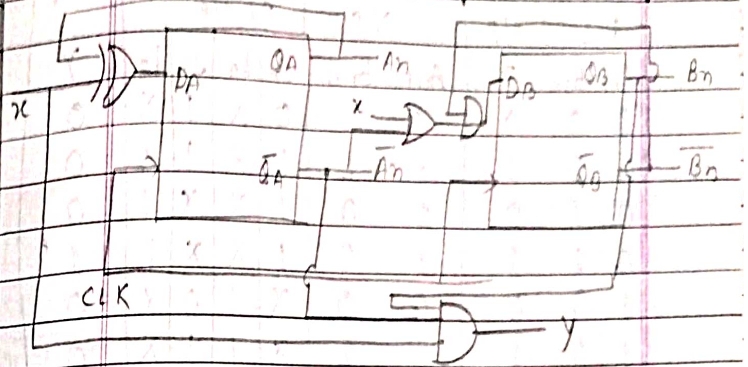
$D_B = \bar{A}_n \bar{B}_n + \bar{B}_n x$

$= \bar{B}_n (\bar{A}_n + x)$

Y

$A_n \backslash B_n x$	00	01	11	10
0			1	
1				

$Y = \bar{A}_n B_n x$



(b) Using J.K Flip Flop.

Step-1 State Table

P.S		N.S				Y	
		$x=0$		$x=1$			
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}	$x=0$	$x=1$
0	0	0	1	1	1	0	0
0	1	1	0	1	0	0	1
1	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0

Step-2 Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Excitation Table J-K Flip Flop.

P.S		I/P	N.S		F.F I/P				Y
A_n	B_n	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	
0	0	0	0	1	0	X	1	X	0
0	0	1	1	1	1	X	1	X	0
0	1	0	1	0	1	X	X	1	0
0	1	1	1	0	1	X	X	1	1
1	0	0	0	0	X	1	0	X	0
1	0	1	0	1	X	1	1	X	0
1	1	0	0	0	X	1	X	1	0
1	1	1	0	0	X	1	X	1	0

J_A

A_n \ $B_n x$	00	01	11	10
0		1	1	1
1	X	X	X	X

$J_A = x + B_n$

J_B

A_n \ $B_n x$	00	01	11	10
0	1	1	X	X
1		1	X	X

$J_B = x + \bar{A_n}\cancel{x}$

K_A

A_n \ $B_n x$	00	01	11	10
0	X	X	X	X
1	1	1	1	1

$K_A =$ ~~An~~ 1

K_B

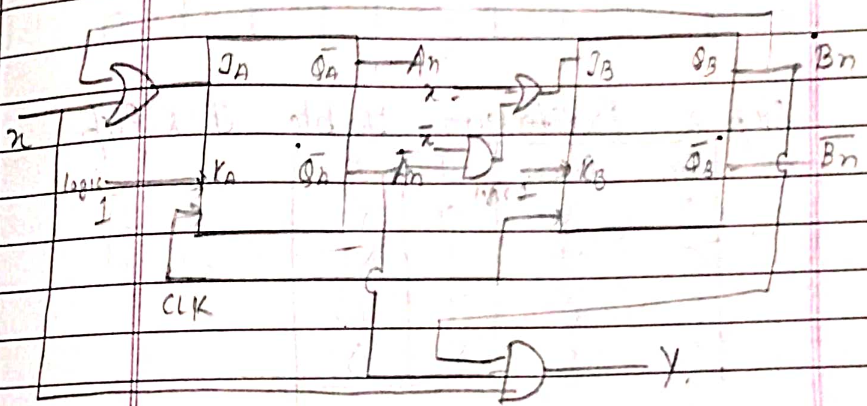
A_n \ $B_n x$	00	01	11	10
0	X	X	1	1
1	X	X	1	1

$K_B =$ ~~Bn~~ 1

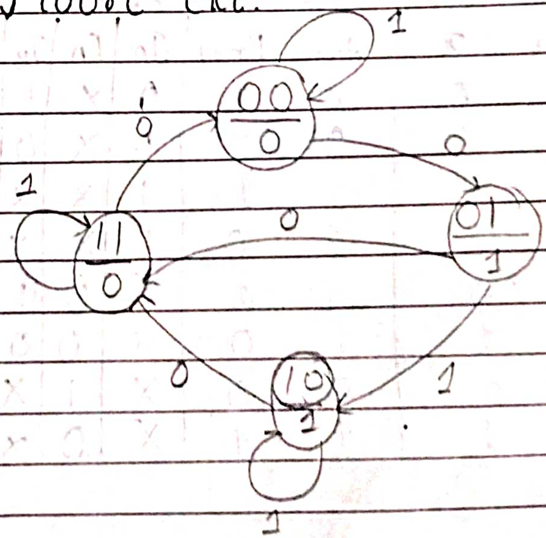
Y

A_n \ $B_n x$	00	01	11	10
0			1	
1				

$Y = \bar{A_n} B_n x$



Moore Ckt.



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Step-1 State Table

P.S		N.S $x=0$		$x=1$		Y
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}	
0	0	0	1	0	0	0
0	1	1	1	1	0	1
1	0	1	1	1	0	1
1	1	0	0	1	1	0

Step-2 Excitation Table · J-K Flip

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Excitation Table J-K Flip-Flop

P.S		I/P	N.S		F.F I/P				Y
A_n	B_n	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	
0	0	0	0	1	0	X	1	X	0
0	0	1	0	0	0	X	0	X	0
0	1	0	1	1	1	X	X	0	1
0	1	1	1	0	1	X	X	1	1
1	0	0	1	1	X	0	1	X	1
1	0	1	1	0	X	0	0	X	1
1	1	0	0	0	X	1	X	1	0
1	1	1	1	1	X	0	X	0	0

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J_A

A_n \ $B_n x$	00	01	11	10
0			1	1
1	X	X	X	X

$J_A = B_n$

K_A

A_n \ $B_n x$	00	01	11	10
0	X	X	X	X
1				1

$K_A = B_n \bar{x}$

J_B

A_n \ $B_n x$	00	01	11	10
0	1		X	X
1	1		X	X

$J_B = \bar{x}$

K_B

A_n \ $B_n x$	00	01	11	10
0	X	X	1	
1	X	X		1

$K_B = \bar{A_n} x + A_n \bar{x}$

$= A_n \oplus x$

Y

A_n \ $B_n x$	00	01	11	10
0			1	1
1	1	1		

$Y = A_n \bar{B_n} + \bar{A_n} B_n$

$= \cancel{A_n \odot} \; A_n \oplus B_n$

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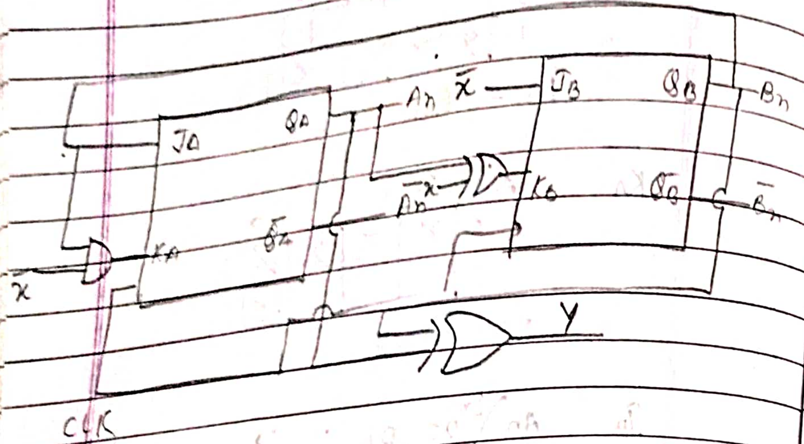
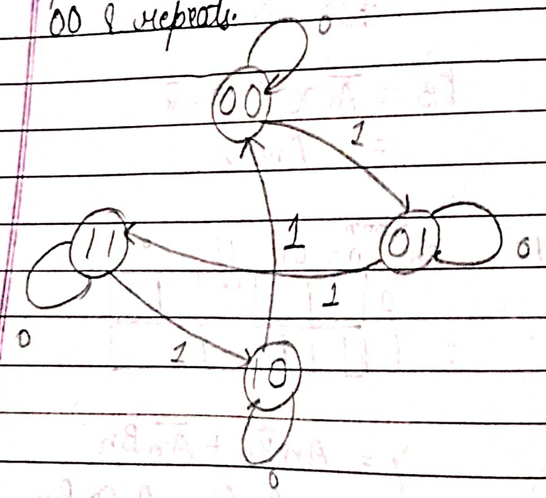


Q Design a sequential ckt with two D-flip flop A & B and 1 input x. When x=0 the state of the ckt remain the same. When x=1, the ckt passes through state transition from 00 to 01 to 11 to 10 back to 00 & repeats.



Step-1 State table

P.S		N.S x=0		x=1	
An	Bn	An+1	Bn+1	An+1	Bn+1
0	0	0	0	0	1
0	1	0	1	1	1
1	0	1	0	0	0
1	1	1	1	1	0

Step-2 Excitation table

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-3 Excitation table of D-flip flop.

P.S		I/P	N.S		F.F I/P	
An	Bn	x	An+1	Bn+1	DA	DB
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	1	1	1
1	0	0	1	0	1	0
1	0	1	0	0	0	0
1	1	0	1	1	1	1
1	1	1	1	0	1	0

D_A

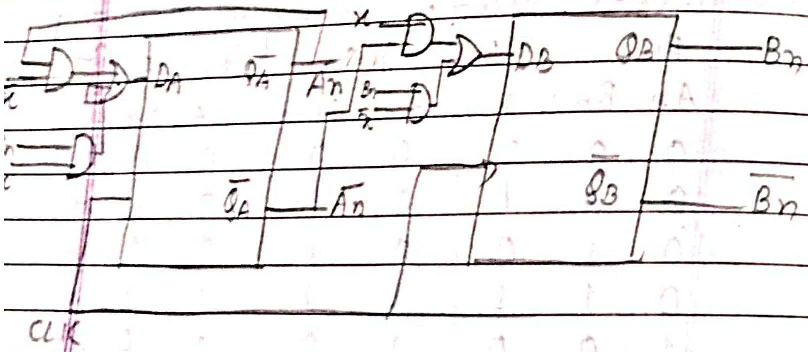
A_n \ $B_n x$	00	01	11	10
0			1	1
1	1		1	

$D_A = A_n\bar{x} + B_n x$

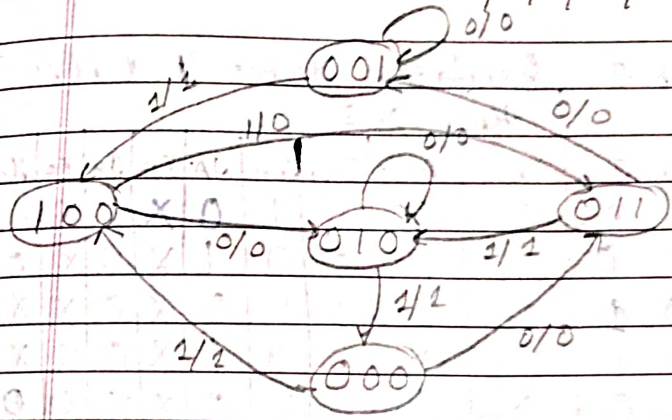
D_B

A_n \ $B_n x$	00	01	11	10
0				
1				

$D_B = \bar{A_n}x + B_n\bar{x}$



Design a sequential ckt that has 3 Flip-Flop A, B & C, 1 input x, 1 output y. The state Diagram is shown in fig. The ckt is to be design by using the unused states as don't care condns. Use J-K Flip flop for designing.



Step-1 State table

P.S			N.S x=0			N.S x=1			Y	
A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}	A_{n+1}	B_{n+1}	C_{n+1}	x=0	x=1
0	0	0	0	1	1	1	0	0	0	1
0	0	1	0	0	1	1	0	0	0	1
0	1	0	0	1	0	0	0	0	0	1
0	1	1	0	0	1	0	1	0	0	1
1	0	0	0	1	0	0	1	1	0	0
~~1~~	~~0~~	~~1~~	0	1	1					
~~1~~	~~1~~	~~0~~								
~~1~~	~~1~~	~~1~~								

Step-2 Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Excitation Table J-K Fli''

P.S A_n	B_n	C_n	I/P x	N.S A_{n+1}	B_{n+1}	C_{n+1}	J_A	K_A	J_B	K_B	J_C	K_C	Y
0	0	0	0	0	1	1	0	X	1	X	1	X	0
0	0	0	1	1	0	0	1	X	0	X	0	X	1
0	0	1	0	0	0	1	0	X	0	X	X	0	0
0	0	1	1	1	0	0	1	X	0	X	X	1	1
0	1	0	0	0	1	0	0	X	X	0	0	X	0
0	1	0	1	0	0	0	0	X	X	1	0	X	1
0	1	1	0	0	0	1	0	X	X	1	X	0	0
0	1	1	1	0	1	0	0	X	X	0	X	1	1
1	0	0	0	0	1	0	X	1	1	X	0	X	0
1	0	0	1	0	1	1	X	1	1	X	1	X	0
1	0	1	0	X	X	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X	X	X

J_A

A_nB_n \ C_nx	00	01	11	10
00		1	1	1
01				
11	X	X	X	X
10	X	X	X	X

$J_A = \overline{B_n}C_n\bar{x} + \overline{B_n}\overline{C_n}x$ $\quad J_A = \overline{B_n}x$

$= \overline{B_n}(C_n\bar{x} + \overline{C_n}x)$

$= \overline{B_n}(C_n \oplus x)$

K_A

A_nB_n \ C_nx	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	1	1	X	X

$K_A = 1$

J_B

A_nB_n \ C_nx	00	01	11	10
00	1			
01	X	X	X	X
11	X	X	X	X
10	1	1	X	X

$J_B = A_n + \overline{C_n}\bar{x}$

K_B

A_nB_n \ C_nx	00	01	11	10
00	X	X	X	X
01		1		1
11	X	X	X	X
10	X	X	X	X

$K_B = \overline{C_n}x + C_n\bar{x} = C_n \oplus x$

J_c

$A_nB_n \backslash C_nx$	00	01	11	10
00	1		X	X
01			X	X
11	X	X	X	X
10	[illegible]	1	X	X

$J_c = A_n x + \overline{A_n B_n \overline{x}}$

K_c

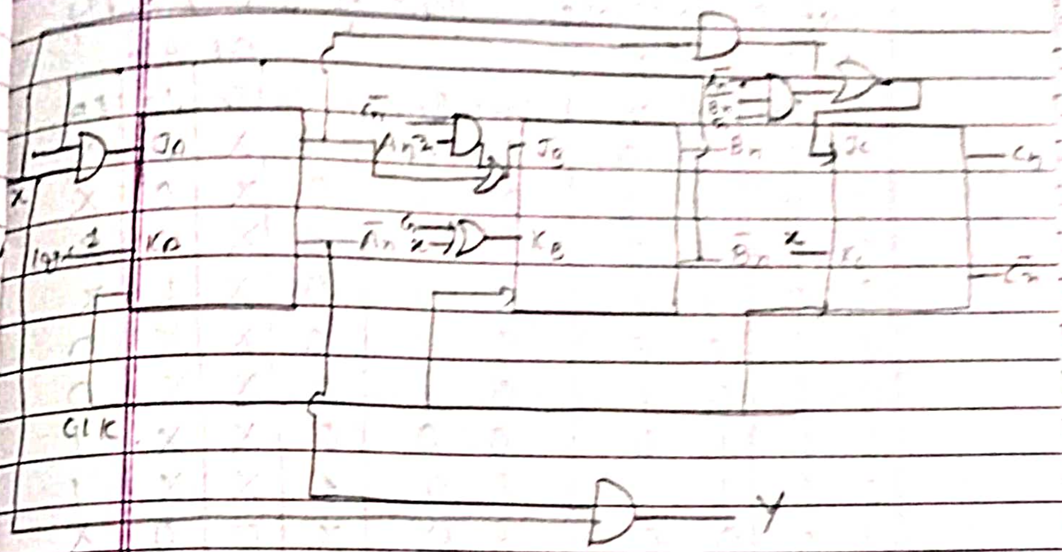
$A_nB_n \backslash C_nx$	00	01	11	10
00	X	X	1	
01	X	X	1	
11	X	X	X	X
10	X	X	X	X

$K_c = x$

Y

$A_nB_n \backslash C_nx$	00	01	11	10
00		1	1	
01		1	1	
11	X	X	X	X
10			X	X

$Y = \overline{A_n} x$



2 Design a sequential ckt with two J-K flip flop A & B & two I/P E x. If E = 0 the sckt remains in the same state regardless of the value of x when E = 1 x = 1 the ckt goes to the transition 00 to 01 to 10 to 11 back to 00 & repeats when E = 1, x = 0 the ckt goes to the transition 00 to 11 to 10 to 01 back to 00 & repeats

Step-1 Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-2 Excitation Table of J K Flip-Flop

P.S		I/P				F.F I/P			
A_n	B_n	E	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	0	0	X	0	X
0	0	1	0	1	1	1	X	1	X
0	0	1	1	0	1	0	X	1	X
0	1	0	0	0	1	0	X	X	0
0	1	0	1	0	1	0	X	X	0
0	1	1	0	0	0	0	X	X	1
0	1	1	1	1	0	1	X	X	1
1	0	0	0	1	0	X	0	0	X
1	0	0	1	1	0	X	0	0	X
1	0	1	0	0	1	X	1	1	X
1	0	1	1	1	1	X	0	1	X
1	1	0	0	1	1	X	0	X	0
1	1	0	1	1	1	X	0	X	0
1	1	1	0	1	0	X	0	X	1
1	1	1	1	0	0	X	1	X	1

J_A

A_nB_n \ Ex	00	01	11	10
00				1
01			1	
11	X	X	X	X
10	X	X	X	X

$J_A = B_n E x + \bar{B_n} E \bar{x}$
$= E(B_n x + \bar{B_n}\bar{x})$
$= E(B_n \odot x)$

K_A

A_nB_n \ Ex	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11			1	
10				1

$K_A = B_n E x + \bar{B_n} E \bar{x}$
$= E(B_n \odot x)$

J_B

A_nB_n \ Ex	00	01	11	10
00			1	1
01	X	X	X	X
11	X	X	X	X
10			1	1

$J_B = E$

K_B

A_nB_n \ Ex	00	01	11	10
00	X	X	X	X
01			1	1
11			1	1
10	X	X	X	X

$K_B = E$

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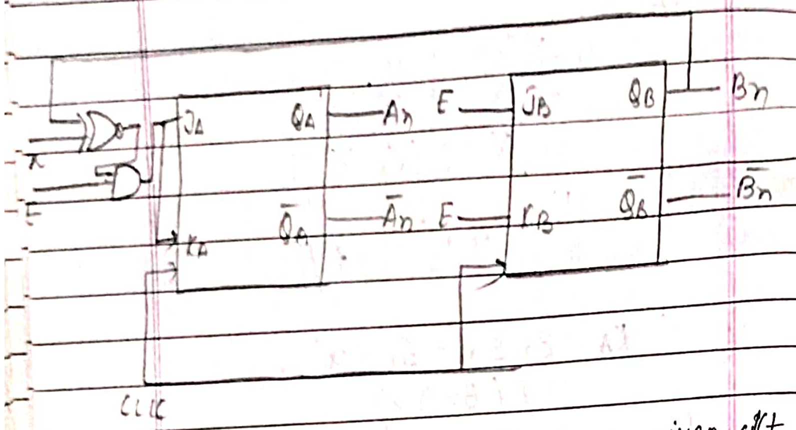
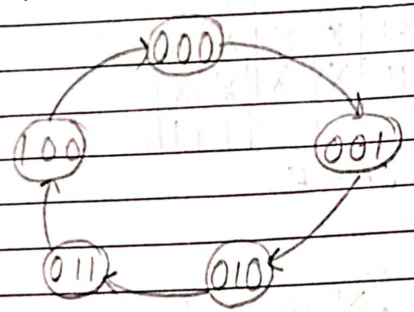


Draw a sequential ckt for a given ckt using JK Flip Flop.



Step-1 State Table

P.S			N.S		
A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0

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Step-2 Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Excitation Table J-K Flip Flop

P.S			N.S			F.F I/P					
A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

J_A

A_n \ B_nC_n	00	01	11	10
0			1	
1	X	X	X	X

$J_A = B_n C_n$

K_A

A_n \ B_nC_n	00	01	11	10
0	X	X	X	X
1	1	X	X	X

$K_A = 1$

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J_B

A_n \ B_nC_n	00	01	11	10
0		1	X	X
1		X	X	X

$J_B = \bar{C_n}$

K_B

A_n \ B_nC_n	00	01	11	10
0	X	X	1	
1	X	X	X	X

$K_B = C_n$.

J_C

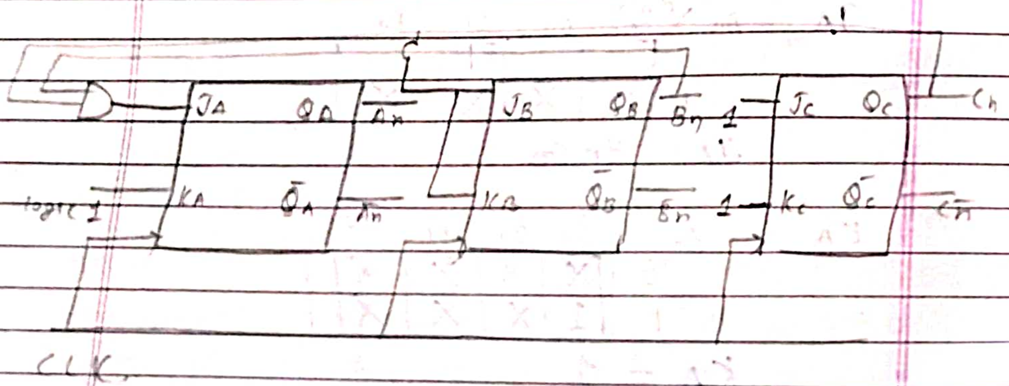
A_n \ B_nC_n	00	01	11	10
0	1	X	X	1
1		X	X	X

$J_C = \bar{A_n}$

K_C

A_n \ B_nC_n	00	01	11	10
0	X	1	1	X
1	X	X	X	X

$K_C = 1$



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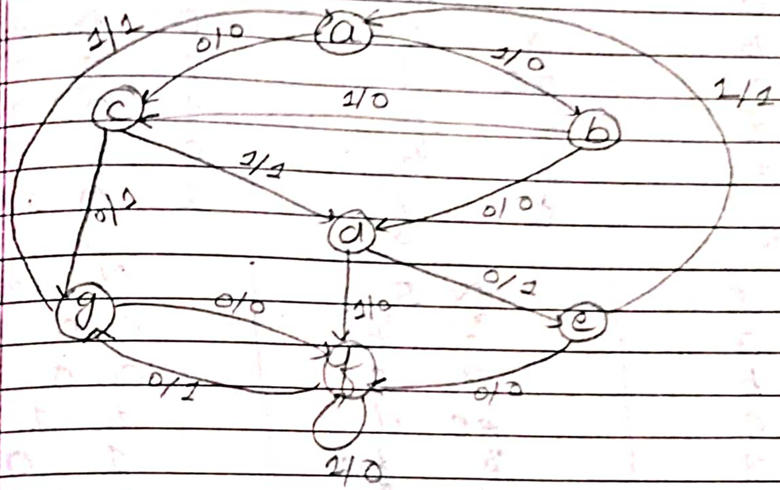
State Assignment



Step-1 State table.

P.S	N.S x=0	N.S x=1	Y x=0	Y x=1
a	c	b	0	0
b	d	c	0	0
c	g	d	1	1
d	e	f	1	0
e	f	a	0	1
f	g	f	1	0
g	f	a	0	1

P.S N.S

a

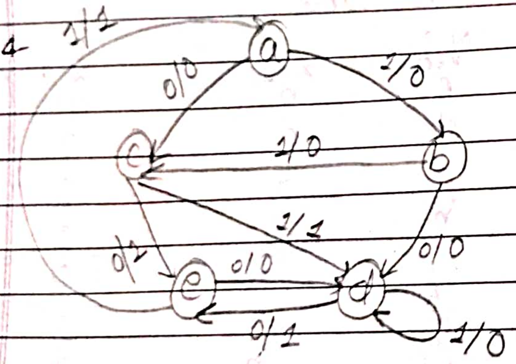
Step-2

P.S	N.S		Y	
a	c	b	0	0
b	d	c	0	0
c	~~g~~e	d	1	1
d	~~g~~	~~f~~ a	1	0
e	~~f~~	a	0	1
~~f~~	~~g~~	~~f~~	1	0

Step-3

P.S	N.S x=0	N.S x=1	Y	
a	c	b	0	0
b	d	c	0	0
c	~~g~~e	d	1	1
d	~~g~~	~~f~~d	1	0
e	d	~~f~~a	0	1

Step-4



Step-5 Assign the value.

a = 000
b = ~~000~~ 001
c = 010
d = 011
e = 100

Step-6 Reduced State Table

P.S	N.S x=0	N.S x=1	Y	
A_n B_n C_n	A_{n+1} B_{n+1} C_{n+1}	A_{n+1} B_{n+1} C_{n+1}	x=0	x=1
0 0 0	0 1 0	0 0 1	0	0
0 0 1	0 1 1	0 1 0	0	0
0 1 0	1 0 0	0 1 1	1	1
0 1 1	1 0 0	0 1 1	1	0
1 0 0	0 1 1	0 0 0	0	1

Step-7 Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-8 Excitation Table

P.S			I/P	N.S			FF I/P			Y
A_n	B_n	C_n	x	A_{n+1}	B_{n+1}	C_{n+1}	D_A	D_B	D_C	
0	0	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0	1	1	0
0	0	1	1	0	1	0	0	1	0	0
0	1	0	0	1	0	0	1	0	0	1
0	1	0	1	0	1	1	0	1	1	1
0	1	1	0	1	0	0	1	0	0	1
0	1	1	1	0	1	1	0	1	1	0
1	0	0	0	0	1	1	0	1	1	0
1	0	0	1	0	0	0	0	0	0	1
1	0	1	0	X	X	X	X	X	X	X

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1	0	1	1	x	x	x	x	x	x	✓
1	1	0	0	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x

D_A

$A_nB_n \backslash C_n x$	00	01	11	10
00				
01	1			1
11	X	X	X	X
10			X	X

$D_A = B_n \bar{x}$

D_B

$A_nB_n \backslash B_n x$	00	01	11	10
00	1		1	1
01		1	1	
11	X	X	X	X
10	1		X	X

$D_B = B_n x + \bar{B_n}\bar{x} + \bar{B_n} C_n$

$= (B_n \odot x) + \bar{B_n} C_n$

D_C

$A_nB_n \backslash C_n x$	00	01	11	10
00		1		1
01		1	1	
11	X	X	X	X
10	1	1	X	X

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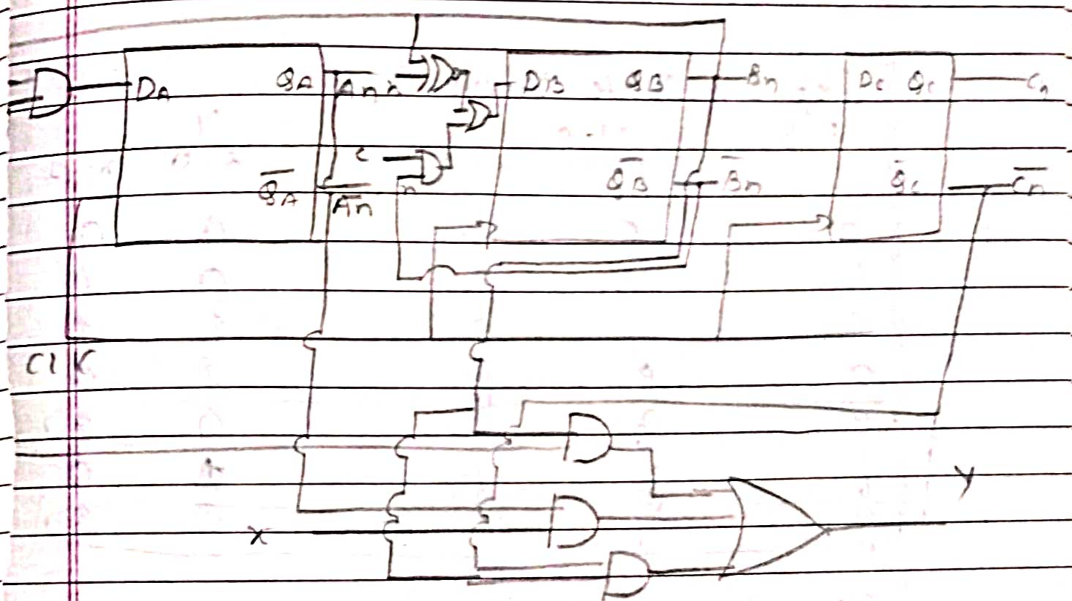
$D_C = A_n\bar{x} + B_n x + \bar{A_n}\bar{C_n}x + \bar{B_n}C_n x$

Y

$A_nB_n \backslash C_n x$	00	01	11	10
00				
01	1	1		1
11	1	X	X	X
10		X	X	

$Y = B_n\bar{x} + A_n x + B_n\bar{C_n}$



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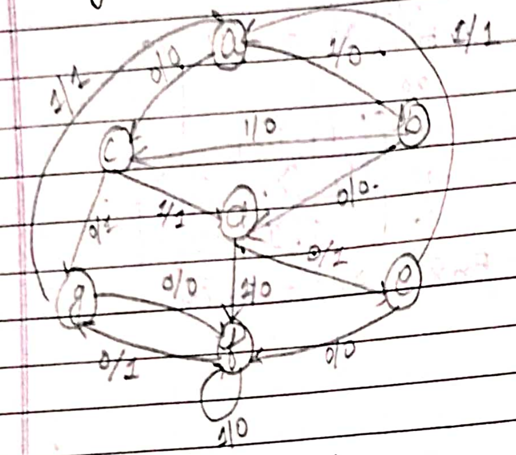
Using J.K Flip Flop



Step-1 State Table

P.S	N.S $x=0$	N.S $x=1$	Y $x=0$	Y $x=1$
a	c	b	0	0
b	d	c	0	0
c	g	d	1	1
d	e	f	1	0
e	g	a	0	1
f	g	f	1	0
g	f	a	0	1

Step-2 Reduction

P.S	N.S $x=0$	N.S $x=1$	Y $x=0$	Y $x=1$
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	f	1	0
e	f	a	0	1
f	e	f	1	0

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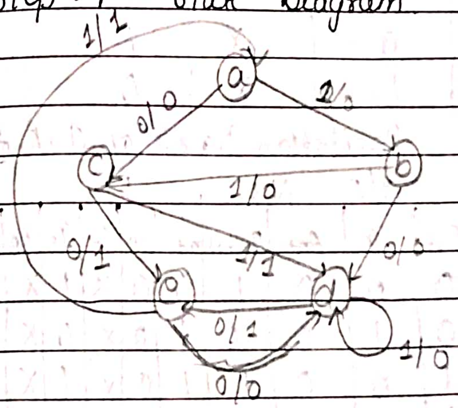
Step-3

P.S.	N.S $x=0$	N.S $x=1$	Y $x=0$	Y $x=1$
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	d	1	0
e	d	a	0	1

Step-4 State Diagram



Step-5 Assign the value

a = 000
b = 001
c = 010
d = 011
e = 100

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Step-6 Reduced state table

P.S			N.S $x=0$			$x=1$			Y $x=0$	$x=1$
A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}	A_{n+1}	B_{n+1}	C_{n+1}		
0	0	0	0	1	0	0	0	1	0	0
0	0	1	0	1	1	0	1	0	0	0
0	1	0	1	0	0	0	1	1	1	1
0	1	1	1	0	0	0	1	1	1	0
1	0	0	0	1	1	0	0	0	0	1

Step-7 Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-8 Excitation Table of J.K ff

P.S			I/P	N.S			F.F						Y
A_n	B_n	C_n	x	A_{n+1}	B_{n+1}	C_{n+1}	J_A	K_A	J_B	K_B	J_C	K_C	
0	0	0	0	0	1	0	0	X	1	X	0	X	0
0	0	0	1	0	0	1	0	X	0	X	1	X	0
0	0	1	0	0	1	1	0	X	1	X	X	0	0
0	0	1	1	0	1	0	0	X	1	X	X	1	0
0	1	0	0	1	0	0	1	X	X	1	0	X	1
0	1	0	1	0	1	1	0	X	X	0	1	X	1
0	1	1	0	1	0	0	1	X	X	1	X	1	1
0	1	1	1	0	1	1	0	X	X	0	X	0	0
1	0	0	0	0	1	1	X	1	1	X	1	X	0
1	0	0	1	0	0	0	X	1	0	X	0	X	1
1	0	1	0	X	X	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X	X	X

J_A

A_nB_n \ C_nx	00	01	11	10
00				
01	1			1
11	X	X	X	X
10	X	X	X	X

$J_A = B_n\bar{x}$

K_A

A_nB_n \ C_nx	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	1	1	X	X

$K_A = 1$

J_B

A_nB_n \ C_nx	00	01	11	10
00	1		1	1
01	X	X	X	X
11	X	X	X	X
10	1	1	X	X

$J_B = \bar{x} + C_n$

K_B

A_nB_n \ C_nx	00	01	11	10
00	X	X	X	X
01	1			1
11	X	X	X	X
10	X	X	X	X

$K_B = \bar{x}$

J_C

A_nB_n \ C_nx	00	01	11	10
00		1	X	X
01		1	X	X
11	X	X	X	X
10	1		X	X

$J_C = A_n\bar{x} + \bar{A_n}x$

$= A_n \oplus x$

K_C

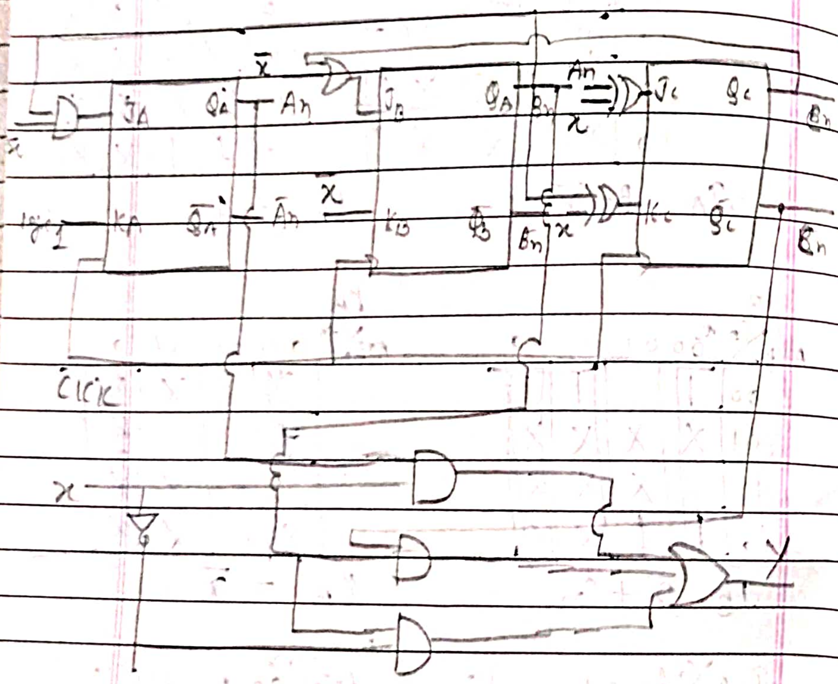
A_nB_n \ C_nx	00	01	11	10
00	X	X	1	
01	X	X		1
11	X	X	X	X
10	X	X	X	X

$K_C = B_n\bar{x} + \bar{B_n}x$

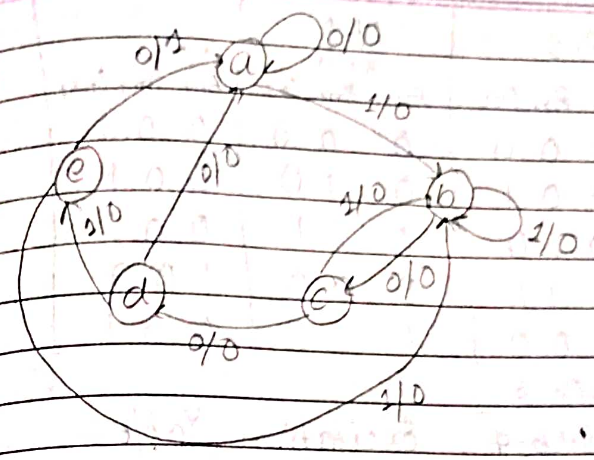
$B_n \oplus x$

Y (A_nB_n \ C_nx)	00	01	11	10
00				
01	1	1		1
11	X	X	X	X
10		1	X	X

$$Y = A_n x + B_n \overline{C_n} + B_n \overline{x}$$



Design a sequential ckt using D or J·K flip flop.



Step-1 State Table

P.S	N.S x=0	N.S x=1	Y x=0	Y x=1
a	a	b	0	0
b	c	b	0	0
c	d	b	0	0
d	a	e	0	0
e	a	b	1	0

Step-2 Assign value

a = 000
b = 001
c = 010
d = 011
e = 100
B = 1001

Step-3 Reduced state table.

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P.S $A_n\ B_n\ C_n$	N.S $x=0$ $A_{n+1}\ B_{n+1}\ C_{n+1}$	$x=1$ $A_{n+1}\ B_{n+1}\ C_{n+1}$	Y $x=0$	$x=1$
0 0 0	0 0 0	0 0 1	0	0
0 0 1	0 1 0	0 0 1	0	0
0 1 0	0 1 1	0 0 1	0	0
0 1 1	0 0 0	1 0 0	0	0
1 0 0	0 0 0	0 0 1	1	0

~~Exec &~~

Step-4 Excitation Table.

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-5 Excitation table of D-

P.S A_n	B_n	C_n	I/P x	N.S A_{n+1}	B_{n+1}	C_{n+1}	F.F I/P D_A	D_B	D_C	Y
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0	1	0	0
0	0	1	1	0	0	1	0	0	1	0
0	1	0	0	0	1	1	0	1	1	0
0	1	0	1	0	0	1	0	0	1	0
0	1	1	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	1	0	0	1	0
1	0	1	0	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X
1	1	0	0							
1	1	0	1				X			
1	1	1	0							
1	1	1	1							

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D_A

A_nB_n \ C_nx	00	01	11	10
00				
01			1	
11	X	X	X	X
10			X	X

$D_A = B_n C_n x$

D_B

A_nB_n \ C_nx	00	01	11	10
00				1
01	1			
11	X	X	X	X
10			X	X

$D_B = B_n\bar{C_n}\bar{x} + \bar{B_n}C_n\bar{x}$

$\bar{x}(B_n\bar{C_n} + \bar{B_n}C_n)$

$\bar{x}(B_n \oplus C_n)$

D_C

A_nB_n \ C_nx	00	01	11	10
00		1	1	
01	1	1		
11	X	X	X	X
10		1	X	X

$D_C = \bar{B_n}x + B_n\bar{C_n}$

Y

A_nB_n \ C_nx	00	01	11	10
00				
01				
11	X	X	X	X
10	1	X	X	X

$Y = A_n\bar{C_n}\bar{x}$

$= A_n\bar{x}$

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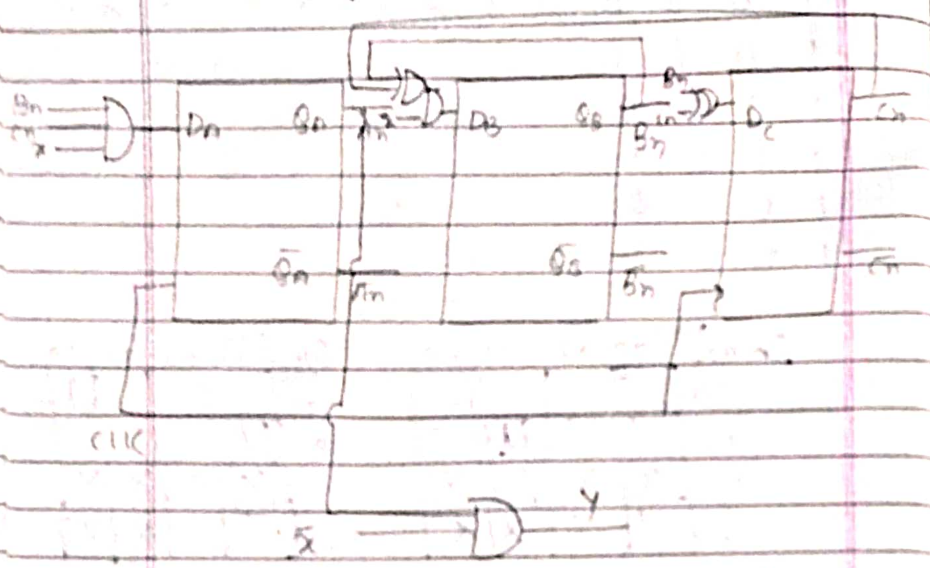

Using J.K

Step-1 State Table

P.S	N.S x=0	N.S x=1	Y x=0	Y x=1
a	a	b	0	0
b	c	b	0	0
c	d	b	0	0
d	a	e	0	0
e	a	b	1	0

Step-2 Assign Value

a = 000
b = 001
c = 010
d = 011
e = 100

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Step-3 Reduced State Table

P.S			N.S x=0			N.S x=1			Y	
An	Bn	Cn	An+1	Bn+1	Cn+1	An+1	Bn+1	Cn+1	x=0	x=1
0	0	0	0	0	0	0	0	1	0	0
0	0	1	0	1	0	0	0	1	0	0
0	1	0	0	1	1	0	0	1	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	0	1	1	0

Step-4 Excitation Table

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-5

P.S			I/P	N.S			FF I/P						Y
An	Bn	Cn	x	An+1	Bn+1	Cn+1	JA	KA	JB	KB	JC	KC	
0	0	0	0	0	0	0	0	X	0	X	0	X	0
0	0	0	1	0	0	1	0	X	0	X	1	X	0
0	0	1	0	0	1	0	0	X	1	X	X	1	0
0	0	1	1	0	0	1	0	X	0	X	X	0	0
0	1	0	0	0	1	1	0	X	X	0	1	X	0
0	1	0	1	0	0	1	0	X	X	1	1	X	0
0	1	1	0	0	0	0	0	X	X	1	X	1	0
0	1	1	1	1	0	0	1	X	X	1	X	1	0
1	0	0	0	0	0	0	X	1	0	X	0	X	1
1	0	0	1	0	0	1	X	1	0	X	1	X	0

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J_A

A_nB_n \ C_nx	00	01	11	10
00				
01			1	
11	X	X	X	X
10	X	X	X	X

$J_A = B_nC_nx$

K_A

A_nB_n \ C_nx	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	1	1	X	X

$K_A = 1$

J_B

	00	01	11	10
00		1		1
01	X	X	X	X
11	X	X	X	X
10			X	X

$J_B = C_n\bar{x}$

	00	01	11	10
00	X	X	X	X
01		1	1	1
11	X	X	X	X
10	X	X	X	X

$K_C = x + C_n$

J_C

A_nB_n \ C_nx	00	01	11	10
00		1	X	X
01	1	1	X	X
11	X	X	X	X
10		1	X	X

A_nB_n \ C_nx	00	01	11	10
00	X	X		1
01	X	X		1
11	X	X	X	X
10	X	X	X	X

$J_C = B_n + x$ $\quad K_C = \bar{x} + B_n$

Y

	X	X	X	X
	1		X	X

$Y = A_n\bar{x}$

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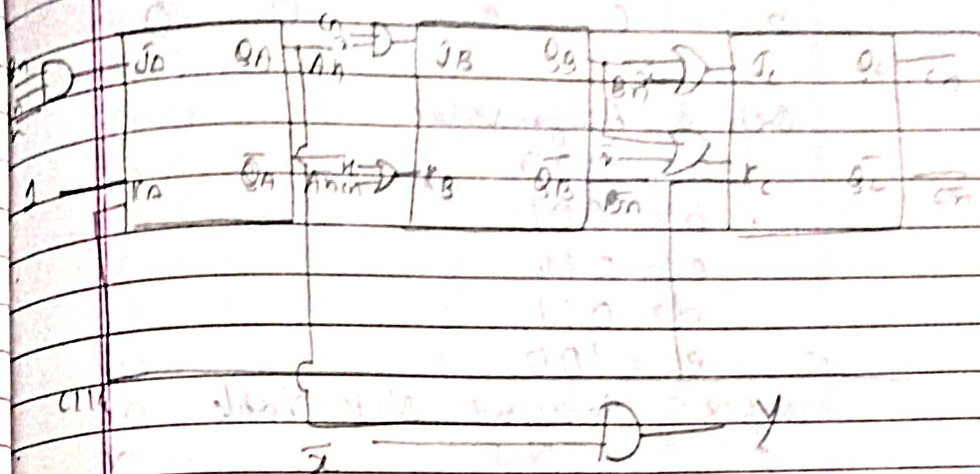
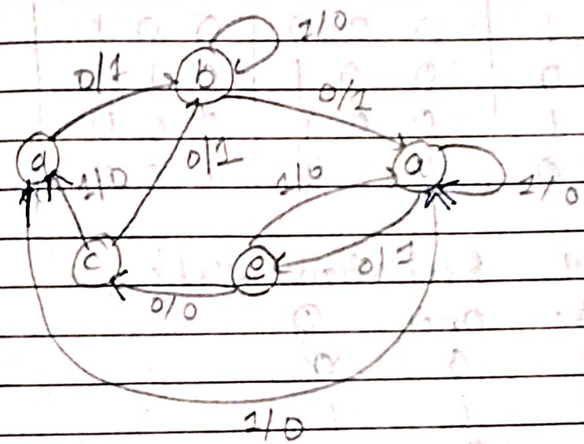




Step.1 State Table

P.S	N.S $x=0$	N.S $x=1$	Y $x=0$	Y $x=1$
a	e	a	1	0
b	a	b	1	0
c	b	d	1	0

d	b	a	1	0
e	c	a	0	0

Step-3 Assign Value.

a = 000
b = 001
c = 010
d = 011
e = 100

Step-3 Reduced State Table.

P.S	N.S		Y	
	$x=0$	$x=1$		
$A_n\ B_n\ C_n$	$A_{n+1}\ B_{n+1}\ C_{n+1}$	$A_{n+1}\ B_{n+1}\ C_{n+1}$	$x=0$	$x=1$
0 0 0	1 0 0	0 0 0	1	0
0 0 1	0 0 0	0 0 1	1	0
0 1 0	0 0 1	0 1 1	1	0
0 1 1	0 0 1	0 0 0	1	0
1 0 0	0 1 0	0 0 0	0	0

Step-4 Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-5 Excitation table of D.

P.S			I/P	N.S			F.F I/P			Y
A_n	B_n	C_n	x	A_{n+1}	B_{n+1}	C_{n+1}	D_A	D_B	D_C	
0	0	0	0	1	0	0	1	0	0	1
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	1	0	0	1	0
0	1	0	0	0	0	1	0	0	1	1
0	1	0	1	0	1	1	0	1	1	0
0	1	1	0	0	0	1	0	0	1	1
0	1	1	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	1	0	0
1	0	0	1	0	0	0	0	0	0	0

D_A

$A_nB_n \backslash C_nx$	00	01	11	10
00	1			
01				
11	X	X	X	X
10			X	X

$D_A = \bar{A_n}\bar{B_n}\bar{C_n}\bar{x}$

$A_nB_n \backslash C_nx$	00	01	11	10
00				
01		1		
11	X	X	X	X
10	1		X	X

$D_B = A_n\bar{x} + B_n\bar{C_n}x$

D_C

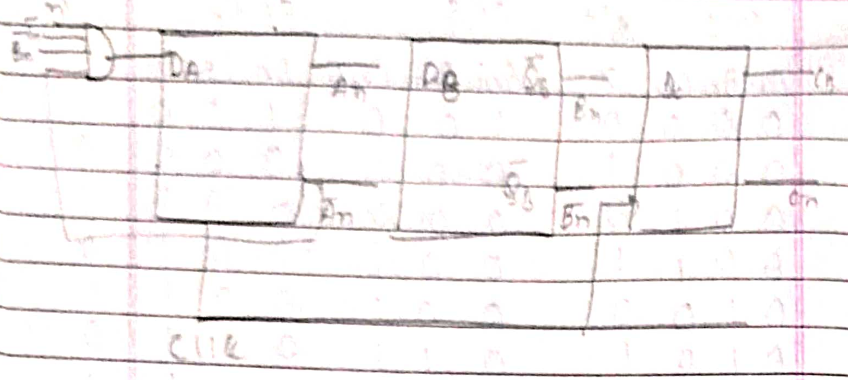
$A_nB_n \backslash C_nx$	00	01	11	10
00			1	
01	1	1		1
11	X	X	X	X
10			X	X

Y

	1			1
	1			1
	X	X	X	X
			X	X

$D_C = B_n\bar{x} + B_n\bar{C_n} + \bar{B_n}C_nx$ $Y = \bar{A_n}\bar{x}$

(10)



Using J-K

Step-3 Reduced table

P.S A_n	B_n	C_n	N.S $x=0$ A_{n+1}	B_{n+1}	C_{n+1}	$x=1$ A_{n+1}			Y $x=0$	$x=1$
0	0	0	1	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1	0
0	1	0	0	0	1	0	1	1	1	0
0	1	1	0	0	1	0	0	0	1	0
1	0	0	0	1	0	0	0	0	0	0

Step-4 J-K flip flop Excitation

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(11)

P.S A_n	B_n	C_n	I/P x	N.S A_{n+1}	B_{n+1}	C_{n+1}	F.F J_A	K_A	J_B	K_B	J_C	K_C	Y
0	0	0	0	1	0	0	1	X	0	X	0	X	1
0	0	0	1	0	0	0	0	X	0	X	0	X	0
0	0	1	0	0	0	0	0	X	0	X	X	1	1
0	0	1	1	0	0	1	0	X	0	X	X	0	0
0	1	0	0	0	0	1	0	X	X	1	1	X	1
0	1	0	1	0	1	1	0	X	X	0	1	X	0
0	1	1	0	0	0	1	0	X	X	1	X	0	1
0	1	1	1	0	0	0	0	X	X	1	X	1	0
1	0	0	0	0	1	0	X	1	1	X	0	X	0
1	0	0	1	0	0	0	X	1	0	X	0	X	0

J_A

A_nB_n \ C_nx	00	01	11	10
00	1			
01				
11	X	X	X	X
10	X	X	X	X

$J_A = \bar{B_n}\bar{C_n}\bar{x}$

A_nB_n \ C_nx	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	1		X	X

$K_A = \bar{x}$

J_B

A_nB_n \ C_nx	00	01	11	10
00				
01	X	X	X	X
11	X	X	X	X
10	1		X	X

A_nB_n \ C_nx	00	01	11	10
00	X	X	X	X
01	1		1	1
11	X	X	X	X
10	X	X	X	X

$J_B = A_n\bar{x}$

$K_B = \bar{x} + C_n$

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J_C

A_nB_n \ x	00	01	11	10
00			X	X
01	1	1	X	X
11	X	X	X	X
10			X	X

$J_C = B_n$

	00	01	11	10
00	X	X		1
01	X	X	1	
11	X	X	X	X
10	X	X	X	X

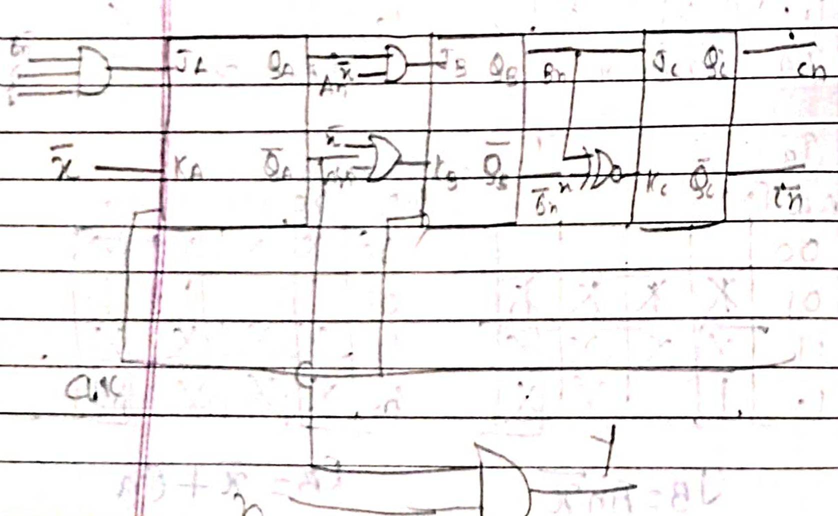
$K_C = B_n x + \bar{B}_n \bar{x}$

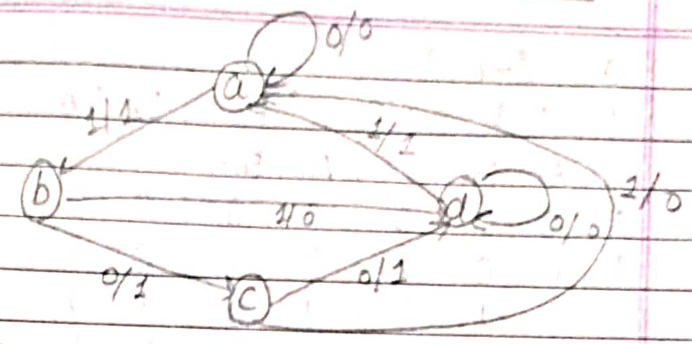
$B_n \odot x$

Y

A_nB_n \ x	00	01	11	10
00	1			1
01	1			1
11	X	X	X	X
10			X	X

$Y = A_n x$





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Step-1 State Table.

P.S	N.S $x=0$	N.S $x=1$	Y $x=0$	Y $x=1$
a	a	b	0	1
b	c	d	1	0
c	d	a	1	0
d	d	a	0	1

Step-2 Assign Value.

a = 00
b = 01
c = 10
d = 11

Step-3 Reduced table

P.S A_n	P.S B_n	N.S $x=0$ A_{n+1}	N.S $x=0$ B_{n+1}	N.S $x=1$ A_{n+1}	N.S $x=1$ B_{n+1}	Y $x=0$	Y $x=1$
0	0	0	0	0	1	0	1
0	1	1	0	1	1	1	0
1	0	1	1	0	0	1	0
1	1	1	1	0	0	0	1

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Step-4

P.S		g/p	N.S				
A_n	B_n	x	A_{n+1}	B_{n+1}	D_A	D_B	Y
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	1
0	1	0	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	0	0	0	0
1	1	0	1	1	1	1	0
1	1	1	0	0	0	0	1

D_A

A_n \ $B_n x$	00	01	11	10
0			1	1
1	1			1

$D_A = \bar{A}_n B_n + A_n \bar{x}$

A_n \ $B_n x$	00	01	11	10
0		1	1	
1	1			1

$D_B = A_n \bar{x} + \bar{A}_n x$

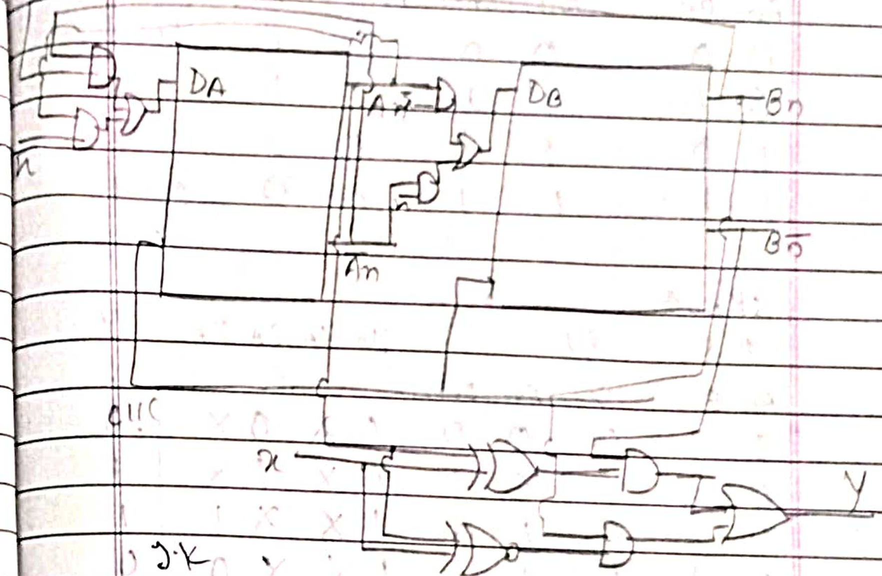
Y

	00	01	11	10
0		1		1
1	1		1	

$Y = A_n \bar{B}_n \bar{x} + \bar{A}_n \bar{B}_n x + A_n B_n x + \bar{A}_n B_n \bar{x}$

$\bar{B}_n (A_n \bar{x} + \bar{A}_n x) + B_n (A_n x + \bar{A}_n \bar{x})$

$\bar{B}_n (A_n \oplus x) + B_n (A_n \odot x)$



J.K

Step-1 State Table

P.S	N.S $x=0$	N.S $x=1$	Y $x=0$	Y $x=1$
a	a	b	0	1
b	c	d	1	0
c	d	a	1	0
d	d	a	0	1

Step-2 Assign value

a = 00

b = 01

c = 10

d = 11

Step-3 Reduced State

P.S		N.S $x=0$		N.S $x=1$		Y $x=0$	Y $x=1$
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}		
0	0	0	0	0	1	0	1
0	1	1	0	1	1	1	0
1	0	1	1	0	0	1	0
1	1	1	1	0	0	0	1

Step-4

P.S		I/P							Y
A_n	B_n	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	
0	0	0	0	0	0	X	0	X	0
0	0	1	0	1	0	X	1	X	1
0	1	0	1	0	1	X	X	1	1
0	1	1	1	1	1	X	X	0	0
1	0	0	1	1	X	0	1	X	1
1	0	1	0	0	X	1	0	X	0
1	1	0	1	1	X	0	X	0	0
1	1	1	0	0	X	1	X	1	1

Step-5

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J_A

A_n \ $B_n x$	00	01	11	10
0			1	1
1	X	X	X	X

$J_A = B_n$

K_A

A_n \ $B_n x$	00	01	11	10
0	X	X	X	X
1		1	1	

$K_A = x$

J_B

A_n \ $B_n x$	00	01	11	10
0		1	X	X
1	1		X	X

$J_B = \bar{A_n}x + A_n\bar{x}$

$= A_n \oplus x$

	00	01	11	10
0	X	X		1
1	X	X	1	

$K_B = A_n x + \bar{A_n}\bar{x}$

$= A_n \odot x$

Y

A_n \ $B_n x$	00	01	11	10
0		1		1
1	1		1	

$= A_n\bar{B_n}\bar{x} + \bar{A_n}\bar{B_n}x + A_nB_nx + A_nB_n\bar{x}$

$= \bar{B_n}(A_n \oplus x) + A_nB_n$

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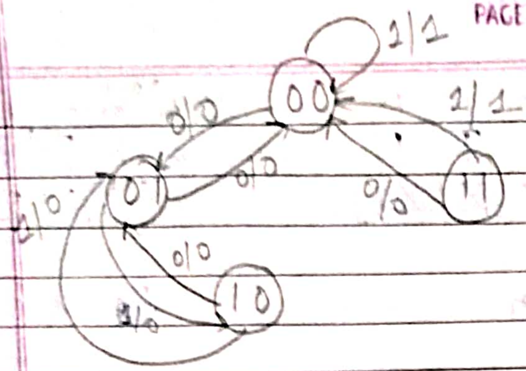


Step-1 State Table

P.S		N.S x=0		N.S x=1		Y x=0	Y x=1
An	Bn	An+1	Bn+1	An+1	Bn+1		
0	0	0	1	0	0	0	1
0	1	0	0	1	0	0	0
1	0	0	1	0	0	0	0
1	1	0	0	0	0	0	1

Step-2 Excitation Table D-

P.S		
Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-3 Excitation table of D-flip

P.S		I/P	N.S		F.F I/P		Y
An	Bn	x	An+1	Bn+1	DA	DB	
0	0	0	0	1	0	1	0
0	0	1	0	0	0	0	1
0	1	0	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	0	1

DA: An \ Bn x	00	01	11	10
0			1	
1				

DB: An \ Bn x	00	01	11	10
0	1			
1	1	1		

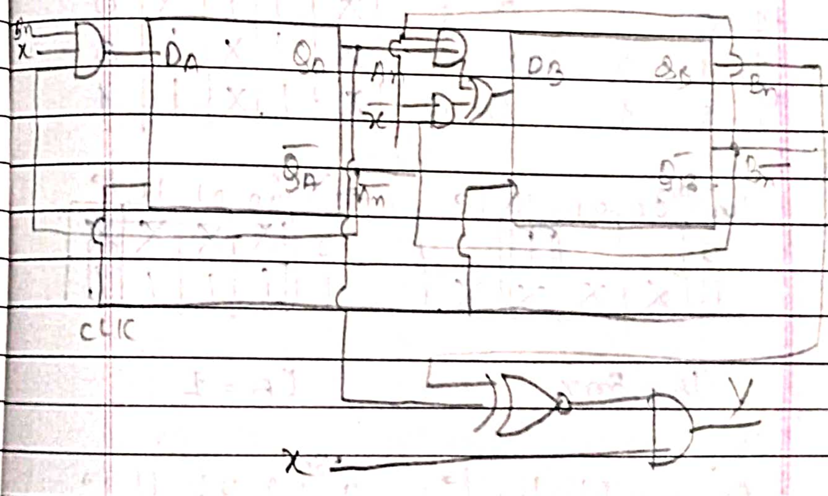
$D_A = \overline{A_n} B_n x$

$D_B = A_n \overline{B_n} + \overline{B_n}\,\overline{x}$

Y: An \ Bn x	00	01	11	10
0		1		
1			1	

$Y = \overline{A_n}\,\overline{B_n} x + A_n B_n x$

$= x (A_n \odot B_n)$



Using J.K

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Step-2 Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Excitation Table of J-K Flip

P.S		I/P	N.S						Y
A_n	B_n	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	
0	0	0	0	1	0	X	1	X	0
0	0	1	0	0	0	X	0	X	1
0	1	0	0	0	0	X	X	1	0
0	1	1	1	0	1	X	X	1	0
1	0	0	0	1	X	1	1	X	0
1	0	1	0	1	X	1	1	X	0
1	1	0	0	0	X	1	X	1	0
1	1	1	0	0	X	1	X	1	1

J_A: A_n \ $B_n x$	00	01	11	10
0			1	
1	X	X	X	X

K_A: A_n \ $B_n x$	00	01	11	10
0	X	X	X	X
1	1	1	1	1

$J_A = B_n x$ $\qquad$ $K_A = 1$

J_B: A_n \ $B_n x$	00	01	11	10
0	1		X	X
1	1	1	X	X

K_B: A_n \ $B_n x$	00	01	11	10
0	X	X	1	1
1	X	X	1	1

$J_B = A_n + \bar{x}$ $\qquad$ $K_B = 1$

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Y: x \				
0		1		
1			1	

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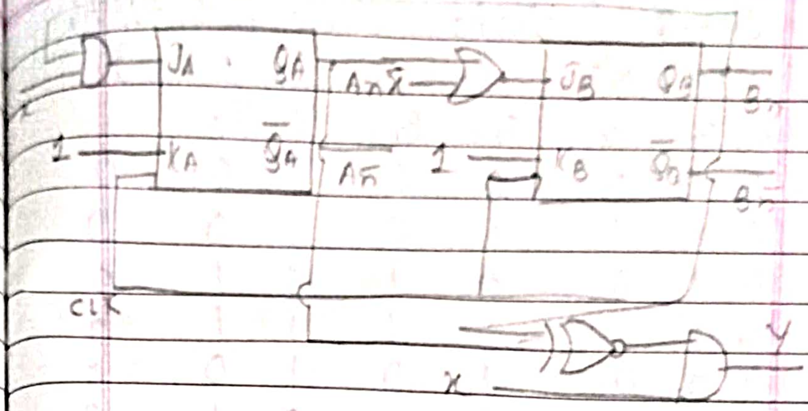
$A_n \bar{B}_n x + A_n B_n x$
$x(A_n \odot B_n)$



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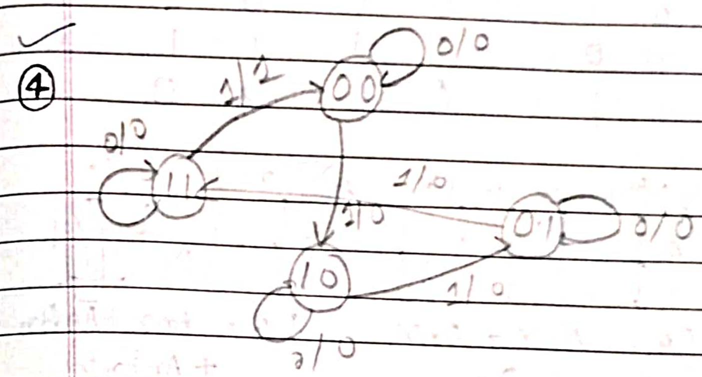

Step-1 State Table

P.S		N.S x=0		x=1		Y x=0	x=1
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}		
0	0	0	0	1	0	0	0
0	1	0	1	1	1	0	0
1	0	1	0	0	1	0	0
1	1	1	1	0	0	0	1

Step-2 Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

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Step-3 Excitation Table of D flip flop

P.S		I/P	N.S		FF I/P		Y
A_n	B_n	x	A_{n+1}	B_{n+1}	D_A	D_B	
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	1	0	1	0
0	1	1	1	1	1	1	0
1	0	0	1	0	1	0	0
1	0	1	0	1	0	1	0
1	1	0	1	1	1	1	0
1	1	1	0	0	0	0	1

D_A

A_n \ $B_n x$	00	01	11	10
0		1	1	
1	1			1

A_n \ $B_n x$	00	01	11	10
0			1	1
1		1		1

$D_A = \bar{A}_n x + A_n \bar{x}$

$= A_n \oplus x$

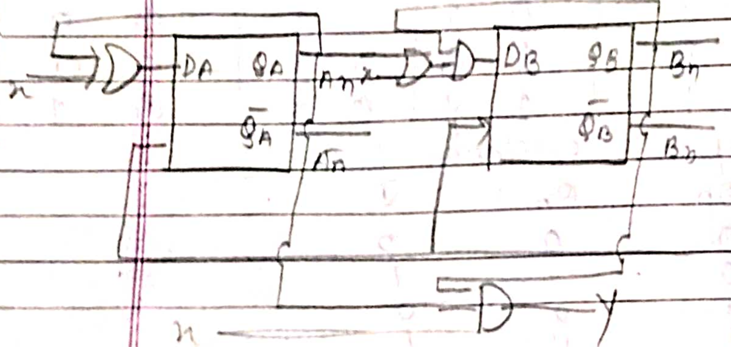
$D_B = B_n\bar{x} + \bar{A}_n B_n + A_n \bar{B}_n x$

$= B_n(\bar{x} + A_n) + A_n\bar{B}_n x$

Y

A_n \ $B_n x$	00	01	11	10
0				
1			1	

$Y = A_n B_n x$



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Using J-K Flip Flop
Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Excitation Table of J-K

P.S		I/P	N.S		FF I/P				Y
A_n	B_n	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	
0	0	0	0	0	0	X	0	X	0
0	0	1	1	0	1	X	0	X	0
0	1	0	0	1	0	X	X	0	0
0	1	1	1	1	1	X	X	0	0
1	0	0	1	0	X	0	0	X	0
1	0	1	0	1	X	1	1	X	0
1	1	0	1	1	X	0	X	0	0
1	1	1	0	0	X	1	X	1	1

J_A

A_n \ $B_n x$	00	01	11	10
0		1	1	
1	X	X	X	X

$J_A = x$

K_A

A_n \ $B_n x$	00	01	11	10
0	X	X	X	X
1		1	1	

$K_A = x$

J_B

A_n \ $B_n x$	00	01	11	10
0			X	X
1		1	X	X

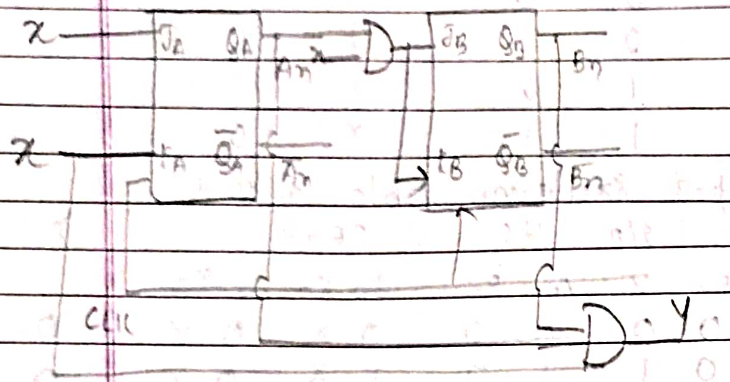
$J_B = A_n x$

A_n \ $B_n x$	00	01	11	10
0	X	X		
1	X	X	1	

$K_B = A_n x$

Y	$B_n x$: 00	01	11	10
A_n = 0				
1			1	

$Y = A_n B_n x$



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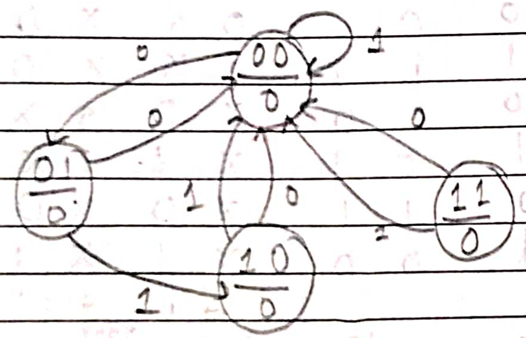


D-flip flop

Step-1 State Table

P·S		N·S x=0		x=1		Y
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}	
0	0	0	1	0	0	0
0	1	0	0	1	0	0
1	0	0	0	0	0	0
1	1	0	0	0	0	0

Step-2 Excitation flip flop

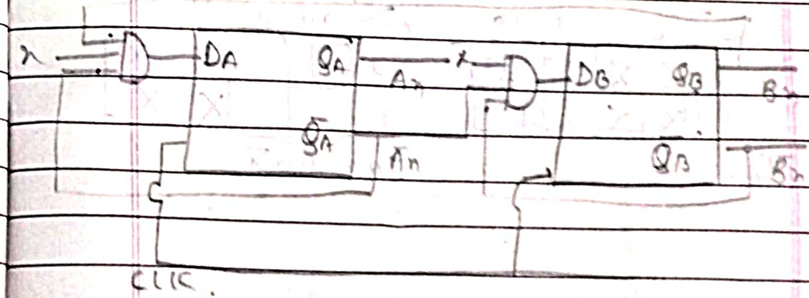
P·S		i/p	N·S				Y
A_n	B_n	x	A_{n+1}	B_{n+1}	D_A	D_B	
0	0	0	0	1	0	1	0
0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0

D_A	$B_n x$: 00	01	11	10
A_n = 0			1	
1				

$D_A = \bar{A}_n B_n x$

D_B	$B_n x$: 00	01	11	10
A_n = 0	1			
1				

$D_B = \bar{A}_n \bar{B}_n \bar{x}$



Using JK flip flop

Step-2 Excitation of J K flip flop

P.S		I/P	N S						Y
A_n	B_n	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	0
0	0	0	0	1	0	X	1	X	0
0	0	1	0	0	0	X	0	X	0
0	1	0	0	0	0	X	X	1	0
0	1	1	1	0	1	X	X	1	0
1	0	0	0	0	X	1	0	X	0
1	0	1	0	0	X	1	0	X	0
1	1	0	0	0	X	1	X	1	0
1	1	1	0	0	X	1	X	1	0

J_A: A_n \ $B_n x$	00	01	11	10
0			1	
1	X	X	X	X

$J_A = B_n x$

K_A: A_n \ $B_n x$	00	01	11	10
0	X	X	X	X
1	1	1	1	1

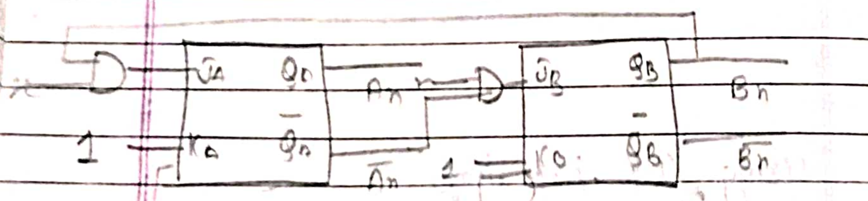
$K_A = 1$

K_B: A_n \ $B_n x$	00	01	11	10
0	X	X	1	1
1	X	X	1	1

$K_B = 1$

J_B: A_n \ $B_n x$	00	01	11	10
0	1		X	X
1			X	X

$J_B = \overline{A_n}\,\overline{x}$



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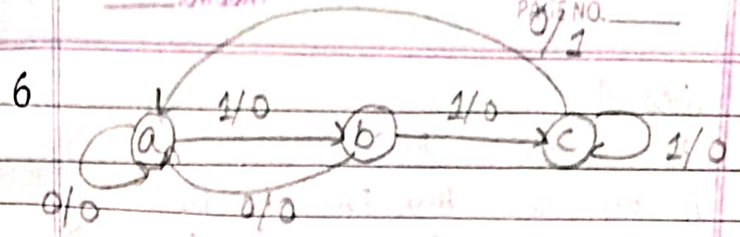


Using D- Flip Flop

Step-1 State Table

P.S	N.S x=0	N.S x=1	Y x=0	Y x=1
a	a	b	0	0
b	a	c	0	0
c	a	c	1	0

Step-2 Assign Value

a = 00

b = 01

c = 10

Step-3 Reduced State Table

P.S	N.S x=0	N.S x=1	Y x=0	Y x=1
00	0 0	0 1	0	0
01	0 0	1 0	0	0
10	0 0	1 0	1	0

Step-4 Excitation Table of D-ff

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Step-4

P.S		I/P	N.S				Y
A_n	B_n	x	A_{n+1}	B_{n+1}	D_A	D_B	
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	1
1	0	1	1	0	1	0	0
1	1	0	X	X	X	X	X
1	1	1	X	X	X	X	X

D_A

$A_n \backslash B_n x$	00	01	11	10
0			1	
1		1	X	X

D_B

$A_n \backslash B_n x$	00	01	11	10
0		1		X
1			X	X

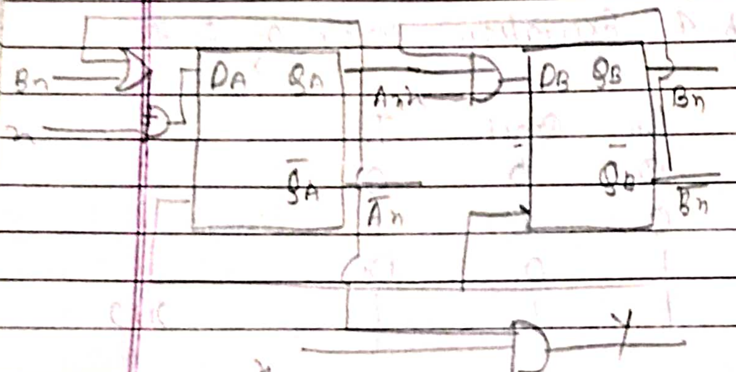
$D_A = A_n x + B_n x$
$= x(A_n + B_n)$

$D_B = \overline{A_n}\,\overline{B_n}\,x$

Y

	00	01	11	10
0				
1	1		X	X

$Y = A_n \overline{x}$



Using J-K flip-flop

Step-3 Excitation of J K

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-4

P.S		I/P	N.S						Y
A_n	B_n	x	A_{n+1}	B_{n+1}	J_A	K_A	J_B	K_B	
0	0	0	0	0	0	X	0	X	0
0	0	1	0	1	0	X	1	X	0
0	1	0	0	0	0	X	X	1	0
0	1	1	1	0	1	X	X	1	0
1	0	0	0	0	X	1	0	X	1
1	0	1	1	0	X	0	0	X	0
1	1	0	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X

J_A

$A_n \backslash B_n x$	00	01	11	10
0			1	
1	X	X	X	X

$J_A = B_n x$

K_A

$A_n \backslash B_n x$	00	01	11	10
0	X	X	X	X
1	1		X	X

$K_A = \overline{x}$

J_B

	00	01	11	10
0		1	X	X
1			X	X

J_B $\overline{A_n} x$

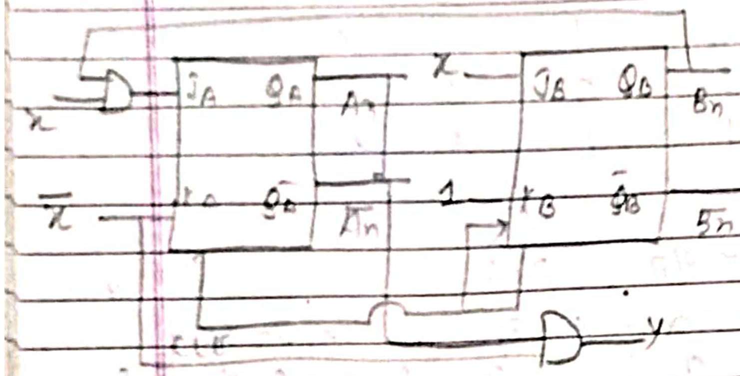
K_B

	00	01	11	10
0	X	X	1	1
1	X	X	X	X

$K_B = 1$

y	00	01	11	10
0				
1	1		X	X

$y = A_n\bar{x}$



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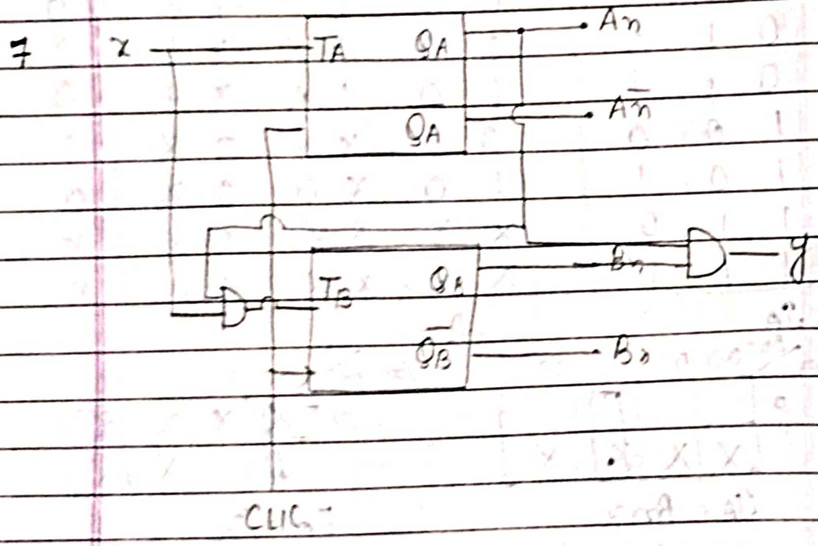


Step- 1 for F.F (A) $T_A = x$

for F/F (B) $T_B = xA_n$

Step - 2 Next State eq^n

$Q_{n+1} = T\bar{Q}_n + \bar{T}Q_n$

$A_{n+1} = T_A\bar{A}_n + \bar{T}_A A_n$

$= x\bar{A}_n + \bar{x}A_n$

$= x \oplus A_n$

$B_{n+1} = T_B\bar{B}_n + \bar{T}_B B_n$

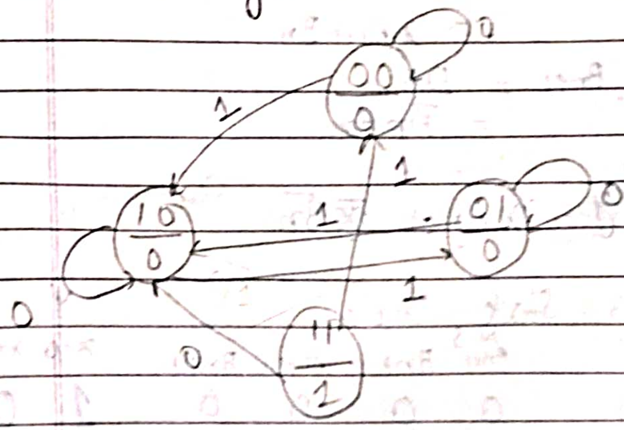
$= xA_n\bar{B}_n + \bar{x}\bar{A}_n B_n$

O/P $y = A_n B_n$

Step - 3 State Table

P.S		N.S x=0		N.S x=1		O/P y
A_n	B_n	A_{n+1}	B_{n+1}	A_{n+1}	B_{n+1}	x=0 x=1
0	0	0	0	1	0	0
0	1	0	1	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

State Diagram



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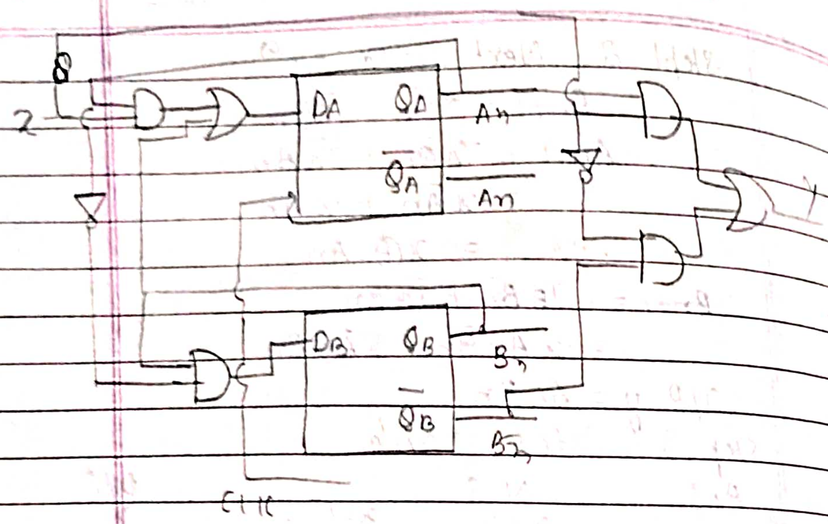

Step-1 F.F.I.

for FF (A) $DA = xA_n + B_n$

$DB = \overline{A_n} B_n$

Step-2 Next state

$Q_{n+1} = D$

$A_{n+1} = DA$

$= xA_n + B_n$

$B_{n+1} = DB$

$= \overline{A_n} B_n$

O/P

$y = xA_n + \bar{x}\overline{B_n}$

Step-3 State Table

A_n	B_n	N.S x=0 A_{n+1}	x=0 B_{n+1}	x=1 A_{n+1}	x=1 B_{n+1}	Y x=0	Y x=1
0	0	0	0	0	0	1	0
0	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1
1	1	1	0	1	0	0	1

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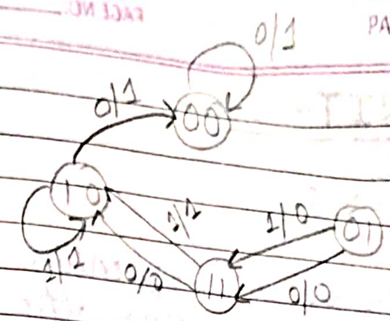


4.9 MEALY MODEL SEQUENTIAL CIRCUIT

Fig. 4.22 shows the clocked synchronous sequential Mealy machine. The output of mealy machine is the function of present inputs and present state (Flip flop outputs). If X is input, Q_n is the present state and the next state is $Q_{(n+1)}$, the output of Mealy function (Z) is given below.

$$Z = f(X, Q_n)$$

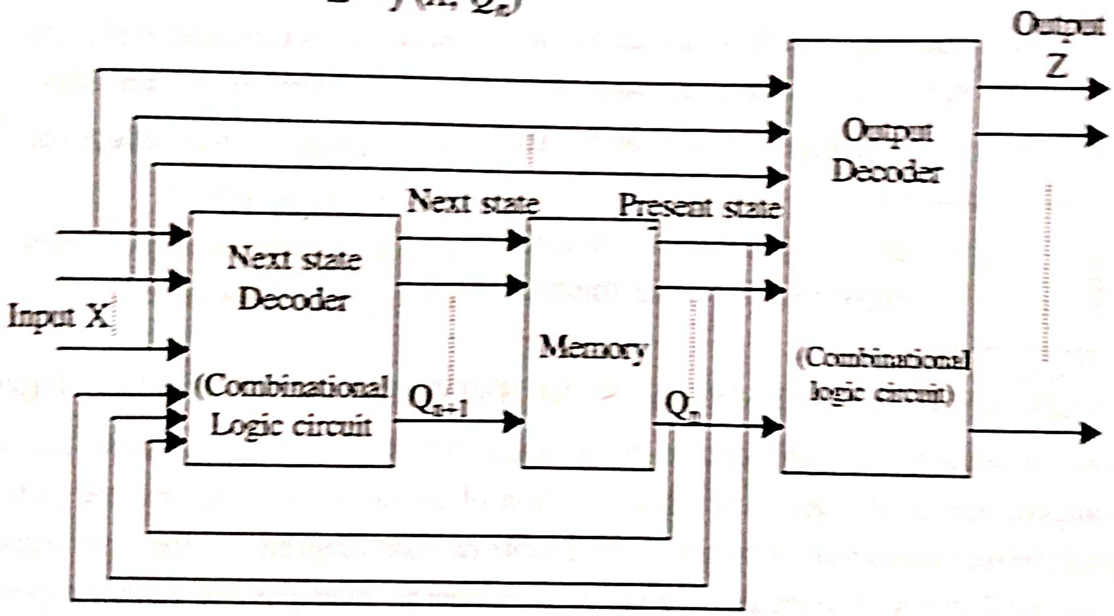


Fig. 4.22 Block diagram of sequential Mealy machine.

The output of memory element is connected to the input of output decoder and next state decoder circuit. The output of memory element is considered as present state.

4.10 MOORE MODE SEQUENTIAL CIRCUIT

Fig. 4.23 shows the block diagram of a Moore machine. The output of Moore machine depends only on the present state. So the output of Moore machine is a function of its present state (Q_n). If the input is X, the next state is $Q_{(n+1)}$ and the present state is Q_n, the output of Moore machine is represen mathematically as

$$Z = f(Q_n)$$

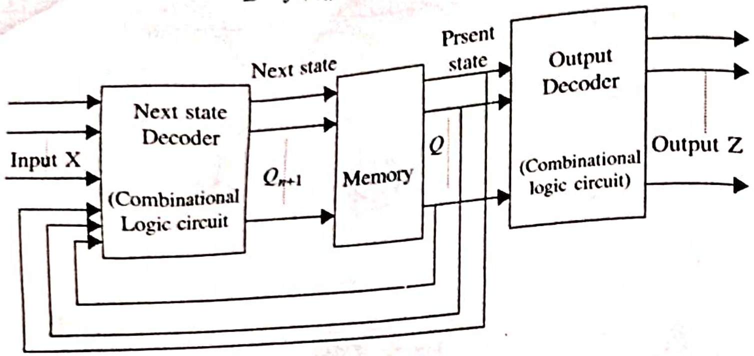


Fig. 4.23 Block diagram of sequential Moore machine.

The difference between the Moore machine and Mealy machine are tabulated as follows

S.No.	*Moore machine*	*Mealy machine*
1.	The output of this machine is the function of the present state only.	Its output is function of present input as well as present state
2.	Input changes do not affect the output	Input changes may affect the output of the circuit
3.	It requires more number of states for implementing same function	It requires less number of states for implementing same function

4.11 ANALYSIS AND SYNTHESIS OF SYNCHRONOUS SEQUENTIAL CIRCUITS

The behaviour of sequential circuit can be determined from the inputs, the output and state of its f flops. The outputs and next state are both a function of its inputs and the present state. The analy of a sequential circuit consists of obtaining a state table or state diagram for the time sequence of inp outputs and internal states. The success of analysis or design of sequential circuit depends on the a and systematic techniques such as state table, state diagram and state equations used in these process The analysis of the clocked sequential circuits can be done by following the procedure as show Fig. 4.24. The reverse process of analysis is known as synthesis of clocked sequential logic circu

For the analysis of sequential circuit, we start with the logic diagram. The excitation equatio Boolean expression of each flip-flop is derived from this logic diagram. Then, to obtain the next s equation, we insert the excitation equations into the characteristic equations. The output equations be derived from the schematic. We can generate the state table using output and next state equati

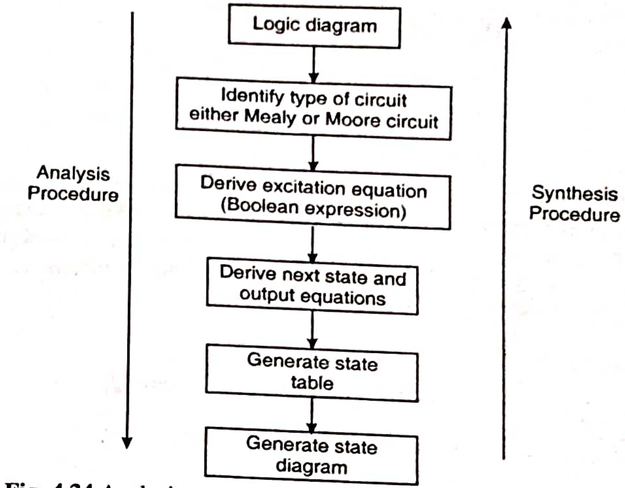


Fig. 4.24 Analysis and synthesis procedure of sequential circuits.

4.11.1 Analysis of Example Sequential Logic Circuit

Figure 4.25 shows a clocked sequential circuit. It has one input variable X, output variable Y and two clocked JK flip flops. The flip flops are labelled as A and B and their outputs are labelled as A and $\overline{A}$, B and $\overline{B}$ respectively.

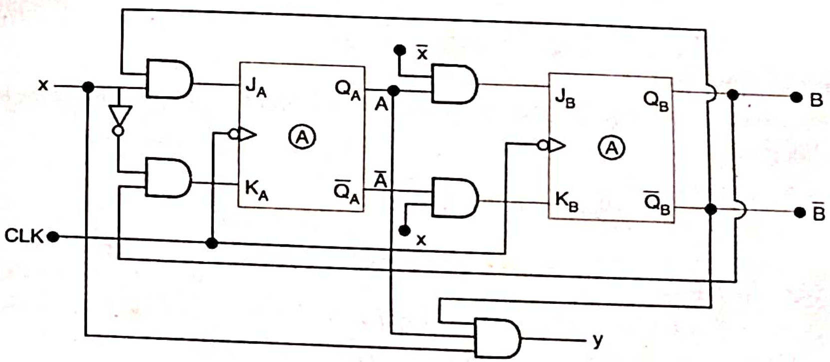


Fig. 4.25 An example of sequential circuit.

Step 1 : Type of circuit

The output (y) of given logic circuit (Fig. 4.25) depends on present input and also on present state (Flip flop outputs) of flip flops, so the given sequential logic circuit is Mealy sequential machine.

Step 2 : Excitation equations

The excitation equations or Boolean expressions of flip flops A and B are obtained. The equations will be in the form of present states A and B and external input x. Since there are two JK flip flops which have output A and B. Therefore the excitation equation (equation formed for flip flop input)

For Flip flop – A $\quad J_A = x\bar{B}$

$K_A = \bar{x}B$

For flip flop – B $\quad J_B = \bar{x}A$

$K_B = x\bar{A}$

Step 3 : Next state equations

The state equations can be derived directly from the logic diagram. Looking at Fig. 4.25, we can see th... the signal for J input of the flip flop A is generated by the function $\bar{B}x$ and the signal for input K by t... function $B\bar{x}$. Substituting $J = \bar{B}x$ and $K = B\bar{x}$ into a JK flip flop characteristic equation given by

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

Stage equation for flip flop A $\quad$ where $Q_n = A$

$$A_{n+1} = (\bar{B}x)\bar{Q}_n + (\overline{B\bar{x}})Q_n$$

$$= \bar{B}x\bar{A} + \overline{B\bar{x}}A$$

$$= \bar{A}\bar{B}x + A(\overline{B\bar{x}})$$

$$= \bar{A}\bar{B}x + A(\bar{B}+x)$$

$$= \bar{A}\bar{B}x + A\bar{B} + Ax$$

$$= A\bar{B} + x(A + \bar{A}\bar{B})$$

$$= A\bar{B} + x(A+\bar{B}) \qquad \because (A + \bar{A}\bar{B} = A + \bar{B}$$

$$\boxed{A_{n+1} = A\bar{B} + Ax + \bar{B}x}$$

State equation for flip flop B

Similarly, we can find the state equation for flip flop B, $J = A\bar{x}$ and $K = \bar{A}x$. Therefore the state equati... of flip flop B is given as

$$B_{n+1} = A\bar{x}\bar{B} + (\overline{\bar{A}x})B$$

$$= A\bar{x}\bar{B} + (A+\bar{x})B$$

$$= A\bar{x}\bar{B} + AB + B\bar{x}$$

$$= \bar{x}(A\bar{B} + B) + AB$$

$$= \bar{x}(A+B) + AB$$

$$\boxed{B_{n+1} = A\bar{x} + B\bar{x} + AB}$$

Output equation

The given sequential circuit has ouput y. The output equation can be found fron the Fig. 4.25, wh... is derived using three input AND gate

$$\boxed{y = A\bar{B}x}$$

Step 4 : State table

Table 4.20 shows the state table for the given sequential logic circuit. It represents the relationship between input, output and flipflop states. It consists of three columns : present state, next state and ouput.

Present state : It specifies the state of the flip flop before occurance of a clock pulse.

Next state : It is the state of flip flop after the application of a clock pulse.

Output : This section gives the value of the output variables during the present state. Both next state and output section have two columns representing two possible input conditions $x = 0$ and $x = 1$.

Table 4.20

Present state	Next state		Output	
	AB	AB	y	
AB	$x = 0$	$x = 1$	$x = 0$	$x = 1$
00	00	10	0	0
01	01	00	0	0
10	11	10	0	1
11	01	11	0	0

We can derive the stae table as follows

(*i*) If present state $AB = 00$, $x = 0$

When a present state is 00 *i.e.* $A = 0$ and $B = 0$ and input $x = 0$, the next state is obtained by using next state equation

Next state for flip flop A

$$A_{n+1} = A\bar{B} + Ax + \bar{B}x$$

$$= 01 + 0.0 + 1.0$$

$$= 0$$

Next state for flip flop B

$$B_{n+1} = A\bar{x} + B\bar{x} + AB$$

$$= 0.1 + 0.1 + 0.0$$

$$= 0$$

$\boxed{\text{Next state for this case } AB = 00}$

(*ii*) If present state $AB = 00$, $x = 1$

Next state for flip-flop A

$$A_{n+1} = A\bar{B} + Ax + \bar{B}x$$

$$= 0.1 + 0.1 + 1.1$$

$$= 1$$

Next state flip flop B $\quad B_{n+1} = A\bar{x} + b\bar{x} + AB$

$$= 0.0 + 0.0 + 0.0$$

$$= 0$$

$\boxed{\text{Next state for this case } AB = 10}$

Similarly, we can obtain the next state for all this different case as shown in table.

(iii) Determine the entries in the output section. For this, we have to examine AND gate for all possible present states and input.

(a) If a present state $AB = 00$, $x = 0$

$$\text{Output } y = A\bar{B}x$$
$$= 0.10$$
$$\boxed{y = 0}$$

(b) If a present state $AB = 00$, $x = 1$

$$\text{output } y = A\bar{B}x$$
$$= 0.11$$
$$\boxed{y = 0}$$

Thus, the state table of any sequential circuit can be obtained by the same procedure used in the above example. This example contains 2 flip flops and one input, and one output, producing four rows, two columns in the next state and output sections. In general, a sequential circuit with m flip-flops and n-input variables produces 2^m rows and one for each state and 2^n columns, one for each input combination in the next state and output sections of the state table.

Step 5 State diagram

State diagram is a graphical representation of a state table. Fig. 4.26 shows the state diagram for sequential circuit. Here each state is represented by a circle, and transition between states is indicated by directed lines connecting the circles. The binary number inside each circle identifies the state represented by the circle. The directed lines are labelled with two binary numbrs separated by a symbol '/' (slash). The input value that causes the state transtion is labelled first and output value is next.

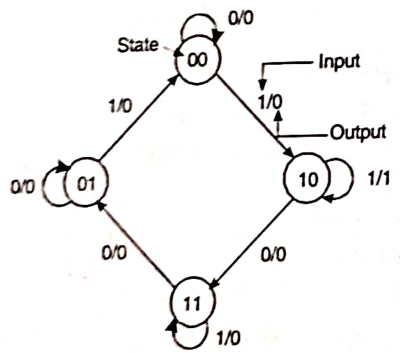


Fig. 4.26 State diagram.

Example 4.8 Derive the state table and state diagram for the sequential circuit shown in Fig. Ex. 4.8(a)

Solution.

Step 1 : Type of circuit

The output y of given sequential circuit (Fig. Ex. 4.8) depends on present input and also present state (flip flop output) of flip flops, so the given sequential logic circuit is Mealy sequential machine

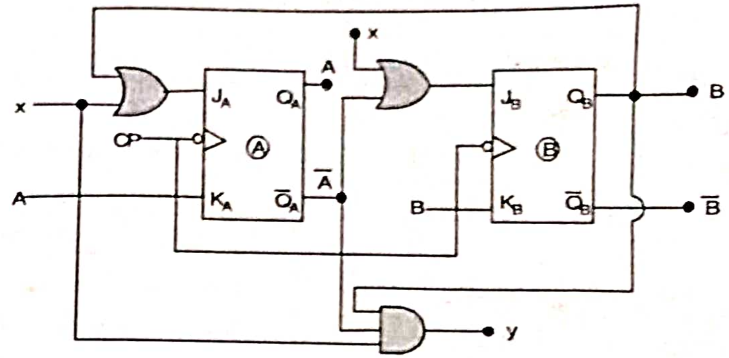


Fig. Ex. 4.8(a)

Step 2 : Excitation equation

For flip flop A

$$J_A = x + B$$
$$K_A = A$$

For flip flop B

$$J_B = \bar{A} + x$$
$$K_B = B$$

Step 3

We know that characteristic equation of JK flip flop

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

State equation for flip flop A

$$A_{n+1} = (x+B)\bar{Q}_n + \bar{A}Q_n \text{ (where } Q_n = A \text{ for flip flop } A)$$
$$= (x+B)\bar{A} + \bar{A}A$$
$$= \bar{A}x + \bar{A}B + 0$$
$$A_{n+1} = \bar{A}x + \bar{A}B$$

State equation for flip flop B

$$B_{n+1} = (\bar{A}+x)\bar{Q}_n + \bar{B}Q_n \text{ (where } Q_n = B \text{ for flip flop } B)$$
$$= (\bar{A}+x)\bar{B} + \bar{B}B$$
$$B_{n+1} = \bar{A}\,\bar{B} + \bar{B}x$$

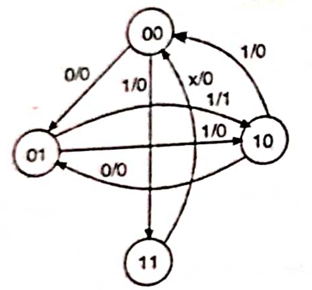
Output equation

$$y = \bar{A}Bx$$

Step 4 : State table

Present state	*Next state*		*Output*	
	$x = 0$	$x = 1$	y	
AB	*AB*	*AB*	$x = 0$	$x = 1$
00	01	11	0	0
01	10	10	0	1
10	01	00	0	0
11	00	00	0	0

Step 5 : State diagram



Note : where x indicates either 0 or 1

Fig. Ex. 4.8(*b*) State diagram of Fig. Ex. 4,8(*a*)

Example 4.9 Derive the state table and state diagram for the sequential circuit shown in Fig. Ex.4.9

Solution.

Step 1 : Type of circuit

The output of a given circuit (See Fig. Ex. 4.9) depends on present input and also on present state so the given sequential logic circuit is mealy machines

Step 2 : Excitation Equation

For flip flop *A* $D_A = Ax + Bx$

For Flip flip *B* $D_B = \bar{A}x$

For output $y = AB + \bar{x}$

Step 3 :

We know that characteristic equation of *D* flip flop (next state depends on input *D*)

$$A_{n+1} = D_A$$

$$\boxed{A_{n+1} = Ax + Bx}$$

$$B_{n+1} = D_B$$

$$\boxed{B_{n+1} = \bar{A}x}$$

$$y = AB + \bar{x}$$

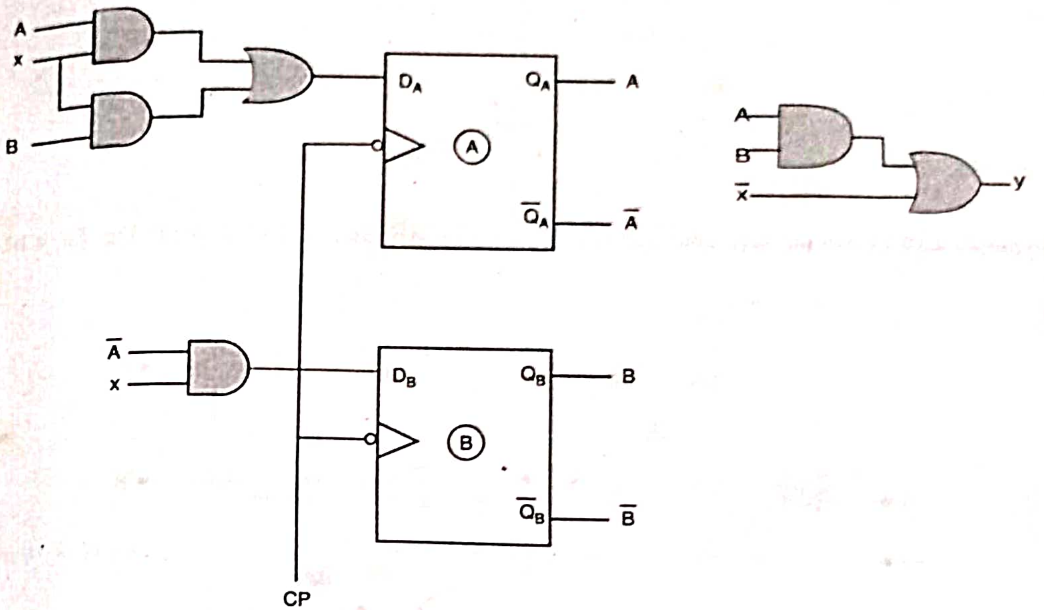


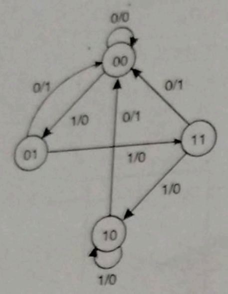
Fig. Ex. 4.9

Step 4 : State table

The state table contains four rows and three columns, the next state and output has two sub columns.

Present state	***Next state***		***Output***	
	$x = 0$	$x = 1$	y	
AB	*AB*	*AB*	$x = 0$	$x = 1$
00	00	01	0	0
01	00	11	1	0
10	00	10	1	0
11	00	10	1	0

Step 5 : State Diagram



Example 4.10 Derive the state table and state diagram for sequential circuit shown in Fig. Ex. 4.10

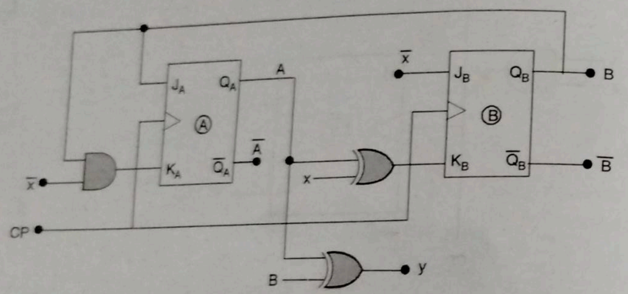


Fig. Ex. 4.10

Solution.

Step 1 : Type of circuit

The output y of the sequential circuit depends on present state only, so the given logic circuit is the moore type circuit.

Step 2 : Excitation equations

For Flip flop A $\quad J_A = B$

$K_A = B\overline{x}$

For Flip flop B $\quad J_B = \overline{x}$

$K_B = A \oplus x$

For output y $\quad y = A \oplus B$

Step 3

We know that characteristics equation of *JK* flip flop

$$A_{n+1} = J\overline{Q}_n + \overline{K}Q_n$$

State equation for flip flop A: $A_{n+1} = B\overline{A} + \left(\overline{B\overline{x}}\right)A \qquad (\because Q_n = A)$

$$= B\overline{A} + A\left(\overline{B} + x\right)$$

$$= B\overline{A} + A\overline{B} + x$$

$$\boxed{A_{n+1} = (A \oplus B) + x}$$

State equation for flip flop B : $B_{n+1} = \overline{x}\overline{B} + \left(\overline{A \oplus x}\right)B \qquad (\because Q_n = B)$

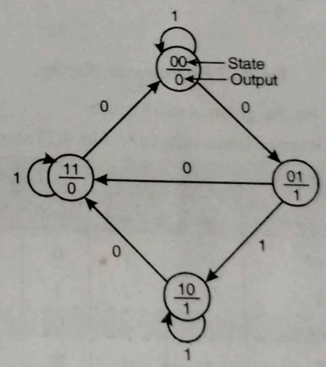
$$= \overline{x}\overline{B} + \left(Ax + \overline{A}\overline{x}\right)B$$

$$\boxed{B_{n+1} = \overline{x}\overline{B} + AxB + \overline{A}\overline{x}B}$$

Step 4 : State table

Present state	Next state		Output
	$x = 0$	$x = 1$	Y
AB	AB	AB	
00	01	00	0
01	11	10	1
10	11	10	1
11	00	11	0

State diagram



Note : The state diagram for Moore machine is different from Mealy machine. Here each circle is coded with state binary number/output.

4.12 STATE REDUCTION

Any logic design process must consider the problem of minimizing the cost of the final circuit. One way to reduce the cost is by reducing the number of flip flops, *i.e.* by reducing the number of states. The state reduction technique basically avoids the introduction of redundant equivalent states. The reduction of redundant states reduces the number of flip flops and logic gates required, thus reducing the cost of the final circuit. Two states are said to be redundant or equivalent, if every possible set of inputs generate exactly the same outputs and the same next states. When two states are equivalent one of them can be removed without altering input output relationship. Let us consider the state diagram as shown in Fig. 4.27. The states are denoted by letter symbols instead of their binary values because in state reduction technique internal states are important, but input output sequences are important. The procedure contains two steps.

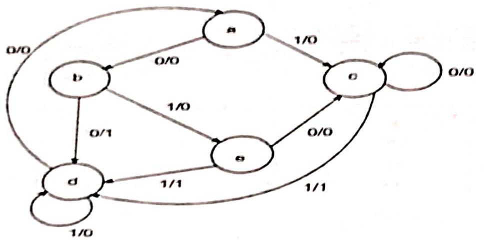


Fig. 4.27 Example state diagram.

Step 1 : Finding the state table for the given state diagram

First the given state diagram is converted into a state table. Fig. 4.27 shows the example of state diagram

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	*b*	*c*	0	0
b	*d*	*e*	1	0
c	*c*	*d*	0	1
d	*a*	*d*	0	0
e	*c*	*d*	0	1

Both are equivalent states because of state *c* and *e* having same next state and same output

Step 2 : Finding equivalent states

The two present states go to the same next state and have the same output for both the input combinations. We can easily find this from the state table, states *c* and *e* are equivalent. This is because both *c* and *e* states go to states *c* and *d* outputs of 0 and 1 for $x = 0$, $x = 1$ respectively. Therefore, the state *e* can be removed and replaced by *c*. The final reduced table and state diagram are given in the table 4.21 and Fig.4.28. The second row have *e* state for the input $x = 1$, it is replaced by *c* because the states *c* and *e* are equivalent.

Table 4.21 Reduced state table

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	*b*	*c*	0	0
b	*d*	*c*	1	0
c	*c*	*d*	0	1
d	*a*	*d*	0	0

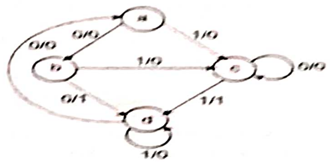


Fig. 4.28 Reduced state diagram.

Example 4.11 Obtain the reduced state table and reduced state diagram for a sequential circuit whose state diagram is shown in Fig. Ex. 4.11(*a*).

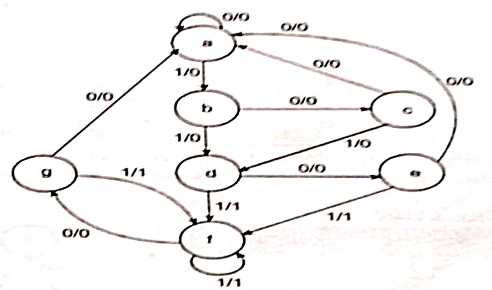


Fig. Ex. 4.11(*a*)

Solution. The given diagram has seven states, one input and one output. As per the step 1, the given state diagram is converted to state table.

State table

Table Ex. 4.11(a)

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Both are equivalent states because of state e and g having same next state and same output.

From the above state table, it is clear that states e and g are equivalent. So the state g is replaced by state e. The reduced state table is shown in Ex. 4.11(b).

Reduced state Table

Table Ex. 4.11(b)

Table Ex. 4.11(b)

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

Both are equivalent states

From the above reduced table, states d and f are equivalent, hence 'f' can be replaced by d and it can be removed. Then finally reduced state table is shown in Tabel Ex. 4.11(c)

Final reduced table

Table Ex 4.11(c)

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

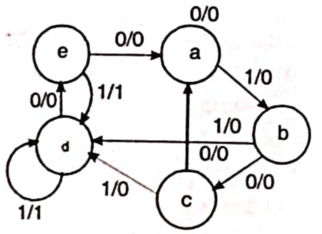


Fig. Ex. 4.11(b) State diagram

The state diagram of the reduced state table is shown in Fig. Ex. 4.11(b).

4.13 STATE ASSIGNMENT

In sequential circuits we know that the behaviour of the circuit is defined in terms of its inputs, present state, next state and outputs. To generate the desired next state at particular present state and inputs, it is necessary to have specific flip flop inputs. These flip flop inputs are described by a set of Boolean functions called flip flop input functions. To determine the flip flop input functions, it is necessary to represent states in the state diagram using binary values instead of alphabets. This procedure is known as state assignment. The following rules are used in state assignment.

***Rule* 1. States having the same next states for a given input condition should have assignments which can be grouped into logically adjacent cells in a K-map.**

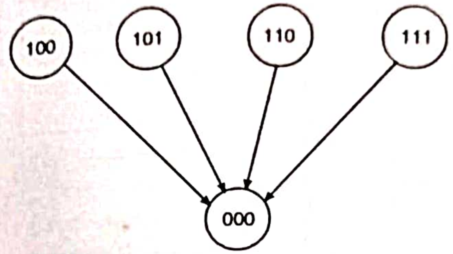


Fig. 4.29 State assignment rule 1 state diagram.

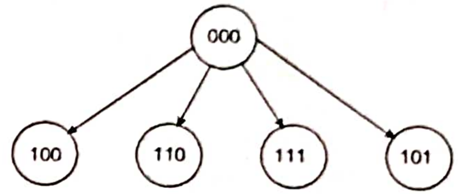


Fig. 4.30 State assignment rule 2 state diagram.

***Rule* 2. States having different next states should have assignment which can be grouped into logically adjacent cells in K-map**

Example 4.12 Design a sequential circuit using D flip flop for a state diagram given below. Use state assignment rules for assigning states and compare the required combinational circuit with random state assignment.

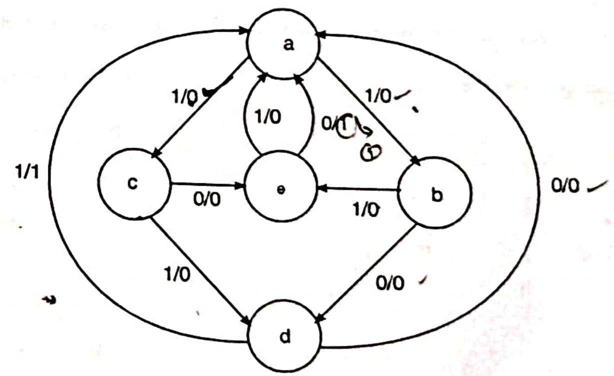


Fig. Ex. 4.12(a)

Solution. The states are a, b, c, d and e. Each states is randomly assigned.

a = 000, b = 001, c = 010, d = 011, e =100. The remaining combinations are considered as don't care conditions.

Excitation table

Present state			Input	Next State			Output
A	B	C	X	A_{n+1}	B_{n+1}	C_{n+1}	Z
0	0	0	0	0	0	1	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	1	0
0	0	1	1	1	0	0	0
0	1	0	0	1	0	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	1
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

K-map simplification

The D flip flop input is equal to next state and the flip flop expression is obtained directly.

Expression for flip flop input D_A

AB \ Cx	00	01	11	10
00	0	1	3 1	2
01	4 1	5	7	6
11	12 X	13 X	15 X	14 X
10	8	9	11 X	10 X

$D_A = B\bar{C}\bar{x} + \bar{B}Cx$

Expression for flip flop input D_B

AB \ Cx	00	01	11	10
00	0	1 1	3	2 1
01	4	5 1	7	6
11	12 X	13 X	15 X	14 X
10	8	9	11 X	10 X

$D_B = \bar{A}C\bar{x} + \bar{B}C\bar{x}$

Expression for flip flop input D_C

AB \ Cx	00	01	11	10
00	0 1	1	3	2 1
01	4	5 1	7	6
11	12 X	13 X	15 X	14 X
10	8	9	11 X	10 X

$D_C = \bar{A}\bar{B}\bar{x} + B\bar{C}x$

Expression for Output Z

AB \ Cx	00	01	11	10
00	0 1	1	3	2 1
01	4	5	7 1	6
11	12 X	13 X	15 X	14 X
10	8 1	9	11 X	10 X

$Z = BCx + A\bar{x}$

The random assignment requires
7 three input AND gates
1 two input AND gates
4 two input OR gates
Total 12 gates with 31 inputs and 3 flip flops are required to construct the sequential logic circuit.

Now we apply state assignment rules, then follow the above steps.

From Rule 1. The states e and d must be adjacent

From the Rule 2, states b and c must be adjacent we form the adjacent cells in the 3 variable K-map.

A \ BC	00	01	11	10
0	0 a	1 b	3 c	2
1	4	5 d	7 e	6

Excitation table

Present state			Input	Next state			Output
A	B	C	X	A_{n+1}	B_{n+1}	C_{n+1}	Z
0	0	0	0	0	0	1	0
0	0	0	1	0	1	1	0
0	0	1	0	1	0	1	0
0	0	1	1	1	1	1	0
0	1	0	0	X	X	X	X
0	1	0	1	X	X	X	X
0	1	1	0	1	1	1	0
0	1	1	1	1	0	1	0

1	0	0	0	X	X	X	X
1	0	0	1	X	X	X	X
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	0

K-Map simplification

Expression for flip flop input D_A

AB \ Cx	00	01	11	10
00	0	1	3: 1	2: 1
01	4: X	5: X	7: 1	6: 1
11	12: X	13: X	15	14
10	8: X	9: X	11	10

$D_A = \bar{A}C$

Expression for flip flop input D_B

AB \ Cx	00	01	11	10
00	0	1: 1	3: 1	2
01	4: X	5: X	7	6: 1
11	12: X	13: X	15	14
10	8: X	9: X	11	10

$D_B = \bar{A}\bar{B}x + \bar{A}B\bar{x}$

Expression for flip flop input D_C

AB \ Cx	00	01	11	10
00	0: 1	1: 1	3: 1	2: 1
01	4: X	5: X	7: 1	6: 1
11	12: X	13: X	15: X	14
10	8: X	9: X	11	10

$D_C = \bar{A}$

Expression for Output Z

AB \ Cx	00	01	11	10
00	0	1	3	2
01	4: X	5: X	7	6
11	12: X	13: X	15	14: 1
10	8: X	9: X	11: 1	10

$Z = AB\bar{x} + A\bar{B}x$

Under the state assignment rules, we require

4 three input AND gates

1 two input AND gate

2 two input OR gates

A total of 7 gates with 18 inputs and 3 flip flops are required to construct the sequential logic circuit based on the state assignment rules.

4.14 DESIGN PROCEDURE

The following steps are followed to design the clocked sequential logic circuit.

1. Obtain the state table from the given circuit information such as a state diagram, a timing diagram or description.
2. The number of states may be reduced by state reduction technique.
3. Assign binary values to each state in the state table.
4. Determine the number of flip flops required and assign a letter symbol to each flip flop.
5. Choose the flip flop type to be used according to the application.
6. Derive the excitation table from the reduced state table.
7. Derive the expression for flip flop inputs and outputs using k-map simplification (The present state and inputs are considered for k-map simplification) and draw logic circuit using flip flops and gates.

4.15 SYNTHESIS OF CLOCKED SEQUENTIAL LOGIC CIRCUITS

Synthesis means that, it is reverse process of analysing a sequential logic circuit. In this synthesis, we get a logic circuit from the information of state diagram, word description etc. The detailed steps are given in the example. Now we will see the detailed description of each step.

A state diagram is obtained from the word description, timing diagram or other pertinent information. From this state diagram, we can form a state table.

The reduction of number of states and binary value assignment to each state gives the reduction in combinational circuit requirement. The number of flip flops required to design any sequential logic circuit depends on the number of states. The type of flip-flops used depends on the application of the designing circuit.

- Use D flip flop for applications such as transfer of data
- Use T flip flop in the application involving complementation (toggling).
- Use JK flip flop for general applications.

The external output information is specified in the output sections of the state table. From it, we can derive the circuit output functions. By using excitation table, we can obtain the flip flop input equation.

Example 4.13 A sequential circuit has one input and one output and its state diagram is shown Fig. Ex. 4.13(*a*). Design the sequential circuit using (*i*) *D* flip flop and (*ii*) *JK* flip flop.

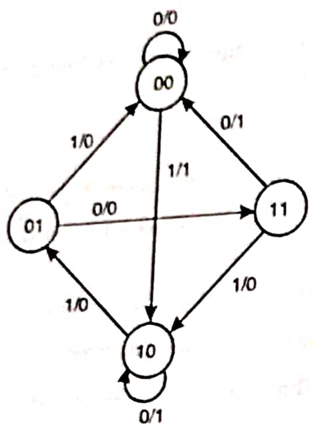


Fig. Ex. 4.13(*a*)

Solution. The given state diagram consist of four states. It has one input (x) and one output y. The st table for the given state diagram is shown in Table Ex. 4.13(*a*). It is clear that there are no equival states. Therefore, there is no reduction in the state diagram. As the state diagram contains 4-states requires 2 flip-flop which are named as *A* and *B*.

Table Ex. 4.13(*a*)

Present state	*Next state*		*Output*	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
AB	*AB*	*AB*	*y*	*y*
00	00	10	0	1
01	11	00	0	0
10	10	01	1	0
11	00	10	1	0

(*i*) Design using *D*-flip flop

For the design of circuit using *D* flip flop (or any flip flop), we need the excitation table. Ta Ex. 4.13(*b*) shows the excitation table of *D* flip flop from which we can develop excitation ta for the required circuit as shown in table Ex. 4.13(*c*).

Table Ex. 4.13(*b*) Excitation table for D-flip flop

Present state	*Next state*	*Flip flop input*
Q_n	Q_{n+1}	*D*
0	0	0
0	1	1
1	0	0
1	1	1

Table Ex. 4.13(*c*) Excitation table

Present state		*Input*	*Next state*		*Flip flop input*		*Output*
A	*B*	*x*	*A*	*B*	D_A	D_B	*y*
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	1	0
0	1	1	0	0	0	0	0
1	0	0	1	0	1	0	1
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	0

The flip-flop input function and the circuit output functions are obtained by using K-map simplification.

Input equation (or) function for flip flop *A* (D_A)

A \ Bx	00	01	11	10
0	0	1 1	3	2 1
1	4 1	5	7 1	6

$$D_A = \overline{A}\overline{B}x + \overline{A}B\overline{x} + A\overline{B}\overline{x} + ABx$$

$$= \overline{A}\left(\overline{B}x + B\overline{x}\right) + A\left(\overline{B}\overline{x} + Bx\right)$$

Let us consider $z = \overline{B}x + B\overline{x}$, then $\overline{B}\overline{x} + Bx = \overline{z}$. Simiplify the above equaiton

$$D_A = \overline{A}z + A\overline{z}$$

$$= A \oplus z$$

Substitue $z = \bar{B}x + B\bar{x} = B \oplus x$ in the above equation

$$\boxed{D_A = A \oplus B \oplus x}$$

Input equation for flip flop B (D_B)

A \ Bx	00	01	11	10
0	0	1	3	2: 1
1	4	5: 1	7	6

$D_B = \bar{A}B\bar{x} + A\bar{B}x$

Output function y

A \ Bx	00	01	11	10
0	0	1: 1	3	2
1	4: 1	5	7	6: 1

$y = A\bar{x} + \bar{A}\bar{B}x$

The input equation for flip flop and output equation are summarized as follows

$$D_A = A \oplus B \oplus x$$

$$D_B = \bar{A}B\bar{x} + A\bar{B}x$$

$$y = A\bar{x} + \bar{A}Bx$$

A sequential circuit using D flip-flop is obtained by using above equations as shown in Fig. Ex.4.13(b).

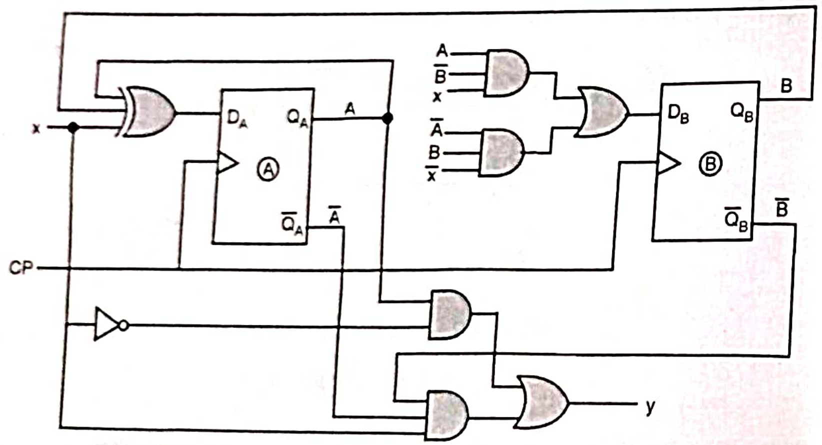


Fig. Ex. 4.13(*b*) Sequential logic diagram using *D* flip-flop.

(*ii*) Design using JK flip flop

Excitation table for JK flip flop

Present state	Next state	Flip flop inputs	
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Excitation stable is developed for the required sequential logic circuit

Present state		Input	Next state		Flip flop Inputs				Output
A	B	x	A	B	J_A	K_A	J_B	K_B	y
0	0	0	0	0	0	x	0	x	0
0	0	1	1	0	1	x	0	x	1
0	1	0	1	1	1	x	x	0	0
0	1	1	0	0	0	x	x	1	0
1	0	0	1	0	x	0	0	x	1
1	0	1	0	1	x	1	1	x	0
1	1	0	0	0	x	1	x	1	1
1	1	1	1	0	x	0	x	1	0

The flip flop input functions and the circuit functions are obtained by using k-map simplification.

Input function for flip flop A

For J_A

A \ Bx	00	01	11	10
0	0	1: 1	3	2: 1
1	4: X	5: X	7: X	6: X

$\bar{B}x$ $\quad B\bar{x}$

$J_A = \bar{B}x + B\bar{x}$

$$\boxed{J_A = B \oplus x}$$

For K_A

A \ Bx	00	01	11	10
0	0: X	1: X	3: X	2: X
1	4	5: 1	7	6: 1

$\bar{B}x$ $\quad B\bar{x}$

$K_A = \bar{B}x + B\bar{x}$

$$\boxed{K_A = B \oplus x}$$

Input function for flip flop B

For J_B

$A \backslash Bx$	00	01	11	10
0	0	1	3 X	2 X
1	4	5 1	7 X	6 X

$B\bar{x}$

$\boxed{J_B = Ax}$

For K_B

$A \backslash Bx$	00	01	11	10
0	0 X	1 X	3 1	4
1	4 X	5 X	7 1	6 1

x A

$\boxed{K_B = A + x}$

For output function y

$A \backslash Bx$	00	01	11	10
0	0	1 1	3	2
1	4 1	5	7	6 1

$\bar{A}\bar{B}x$

$A\bar{x}$

$\boxed{y = A\bar{x} + \bar{A}\bar{B}x}$

The input functions and output function for flip flops are summarized as follows.

$$J_A = B \oplus x$$

$$K_A = B \oplus x$$

$$J_B = Ax$$

$$K_B = A + x$$

$$y = A\bar{x} + \bar{A}\bar{B}x$$

Fig. Ex. 4.13(*c*) shows the logic diagram of a sequential logic circuit

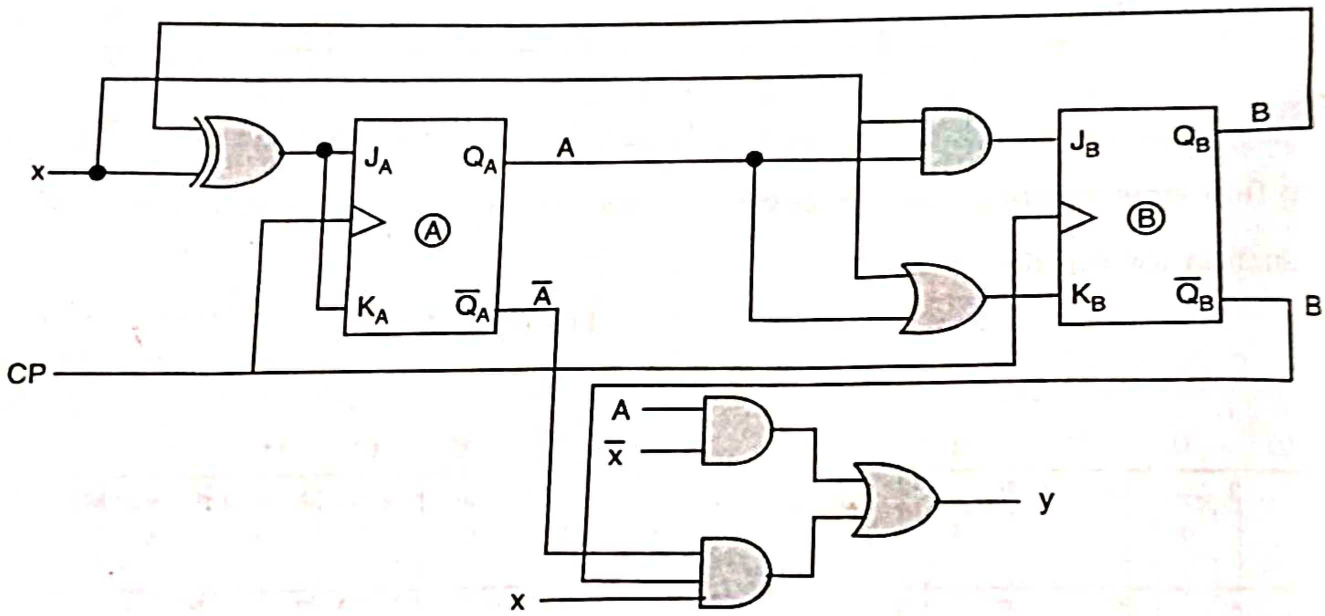


Fig. Ex. 4.13(*c*) Logic diagram using JK flip flop.

4.16 SEQUENCE GENERATOR

A sequential circuit which generates a prescribed sequence of bits, synchronous with the cl referred to as a sequence generator. We can construct sequence generators by two ways

1. Sequence generators using counters
2. Sequence generators using shift registers