

(1/3)

Characteristics of logic family (families)

Some of the important parameters or properties of various logic families are listed as follows:-

- (1) Speed of operation (Propagation delay t_p)
- (2) Power dissipation
- (3) Fan-In
- (4) Fan-Out
- (5) Noise immunity
- (6) Operating temperature
- (7) Power supply requirements.

Propagation delay: The speed of operation of an IC is expressed in terms of propagation delay. Propagation delay is defined as the time taken for the output of a gate to change after the inputs have changed.

It is measured in nsec.

⇒ Propagation delay is always measured from 50% ^{voltage level} value of the

of the input and output waveforms.

⇒ In Transistor ON to OFF time is more compare to OFF to ON time due to saturation or storage time.

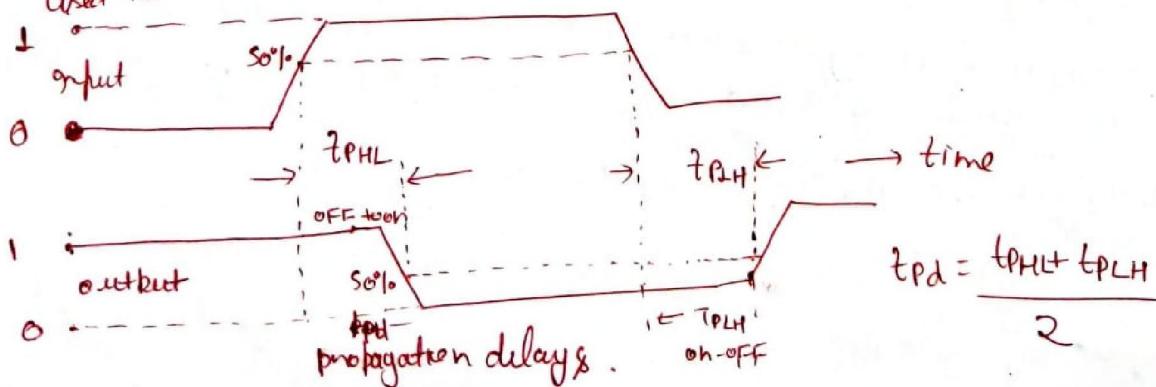
$$t_{PLH} > t_{PHL}$$

t_{PLH} ⇒ It is the propagation delay time in going from logical low (0 state) to logical High (1 state).

t_{PHL} ⇒ It is the propagation delay time in going from logical High (1 state) to logical low (0 state).

The average ~~propagation delay~~ of the above two propagation delays.

• $(t_{PLH} + t_{PHL})/2$ is called the average propagation delay and is used to rate the circuit.



Q) Power dissipation: Power dissipation is a measure of the power consumed by the logic gate when fully driven by all its inputs. and it is expressed in milliwatts (mw) or nanowatts (nw).

⇒ The d.c. or average power dissipation is the product of dc supply voltage and the mean current taken from that supply.

$$P_{diss} = V_{cc} \times I_{cavg}$$

$$I_{cavg} = \frac{I_{con} + I_{off}}{2}$$

③ Figure of merit (Fom)

Fom is a product of propagation delay and power dissipation. It is measured in terms of Pico-joule (pjoule). It is called as speed power.

Product. The ~~small~~ Fom should be as low as possible. = The Fom is always a compromise b/w speed and power dissipation. means if we reduce the propagation delay then the power dissipation will increase and vice-versa.

$$Fom = P_{diss} \times t_{pd}$$

J2L have best Fom., value of Fom is low the logic family is best

④ Fan IN: Fan in refers to the number of inputs in a digital logic gate family. For example given in the figure below. The EXOR gate has three inputs. So Fan-In for the given EXOR gate is 3.

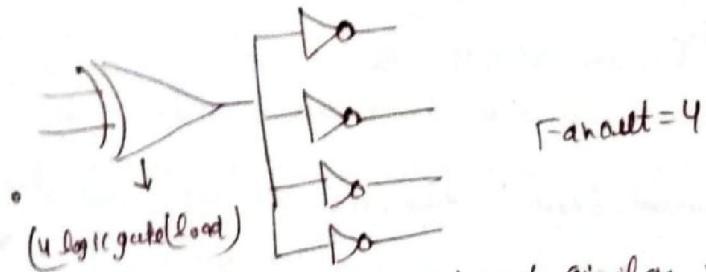


$$\text{Fan IN} = 3.$$

* the FAN-IN of a gate is the number of inputs connected to the gate without any degradation in the voltage levels. This parameter determines the functional capabilities of a logic circuit.

⑤ FAN out: Fan out refers to the number of outputs that is driven by the O/P of another logic gate. For example, the following circuit has an EXOR gate, which drives 4 NOT

gates so fanout of EXOR gate is 4.



Fanout is the maximum number of similar logic gates that a gate can drive without any degradation in voltage levels.

Both FANH & FANL values are given by the manufacturer at the time of designing and the data is specified in the datasheet.

$$(F_{\text{fanout}})_H = \frac{I_{OH}}{I_{OL}}$$

$$F_{\text{anout}}_L = \frac{J_{OL}}{J_{OL}}$$

Noise immunity:-

It is an unwanted signal that is superimposed on the normal operating signal. Noise may be due to various factors like operating environment, radiations, stray electrical and magnetic fields.

⇒ Noise margin is the max. noise voltage that can be added to the input of the logic family which will not affect the O/P. Noise margin allows the logic device to function properly within the specified limits.

$$NM_H = V_{OH} - V_{IH}$$

Overall noise margin (NM_{m_H})

$$NM_L = V_{IL} - V_{OL}$$

• Operating Temperature:- all IC gates are semiconductor devices that are temperature sensitive by nature. The operating temperature ranges for an IC vary from 0°C to 70°C for consumer and industrial applications and from -55°C to 125°C for military applications.

Power supply requirement

V_{IH} (High level I/O voltage) → at it the minimum voltage level requirement for a logical 1 at an input, its minimum value is 2V.

- Low level input voltage (V_{IL}) :-
 It is the maximum input voltage required for a logical 0 (low) at an input.
 Its minimum value is 0.8V.
- $V_{OH} \Rightarrow$ min 2.4V
- $V_{OL} = \text{max } 0.4V$
- High level input current (I_{IH}) :- the current that flows through an input when a specified high-level voltage is applied to that input.
- Low-level output current (I_{IL}) :- the current that flows through an input when a specified low-level voltage is applied to that input.

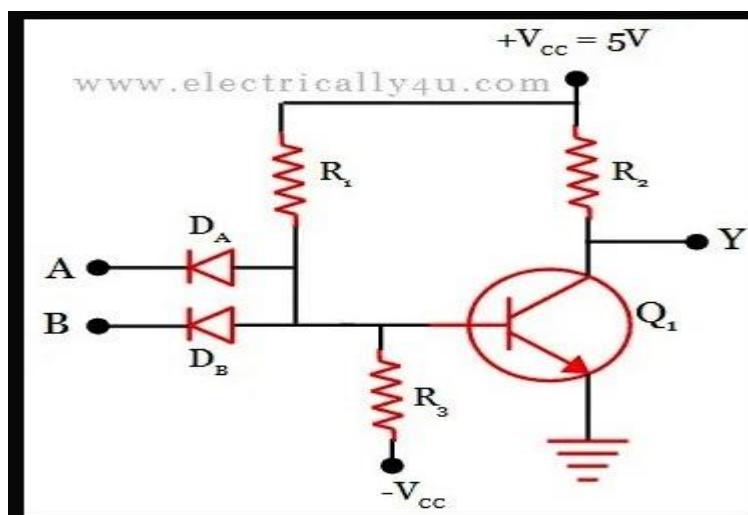
DIODE TRANSISTOR LOGIC (DTL):

The DTL family eliminates the problem of decreasing output voltage with increasing load.

Diode transistor logic(DTL) belongs to the digital logic family. This logic circuit has diodes at the input side and transistor at the output side and so the name diode transistor logic. It has more advantages than resistor transistor logic(RTL).

Logic circuit of 2-input DTL NAND gate

The following figure shows the circuit for the 2-input DTL NAND gate. It consists of two diodes and a transistor. The two diodes D_A , D_B and the resistor R_1 form the input side of the logic circuit. The common emitter configuration of transistor Q_1 and resistor R_2 forms the output side.



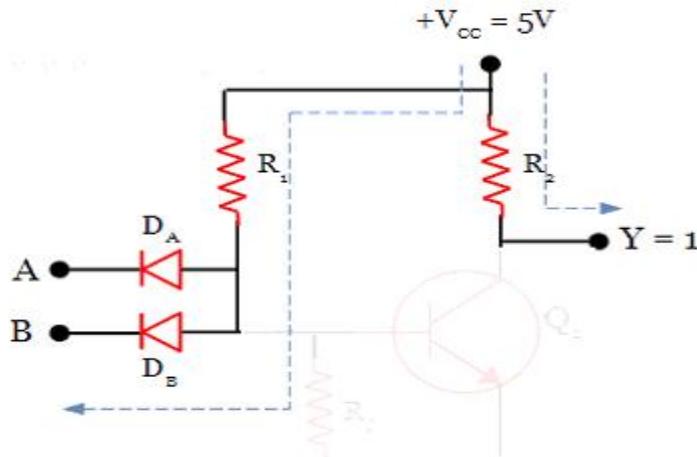
Circuit of 2-input DTL NAND gate

How does a 2-input DTL NAND gate operate?

When both the inputs A and B are LOW, the diodes DA and DB become forward biased and so both diodes will conduct in the forward direction. So the current due to the supply voltage $+V_{CC} = 5\text{ V}$ will go to the ground through R1 and the two diodes DA and DB.

The supply voltage gets dropped in the resistor R1 and it will not be sufficient to turn ON the transistor. So the transistor will be in cut off mode.

Therefore, the output at the terminal Y will have HIGH value, that is Logic 1. The operation of the gate with the current flow path is shown in the below figure.



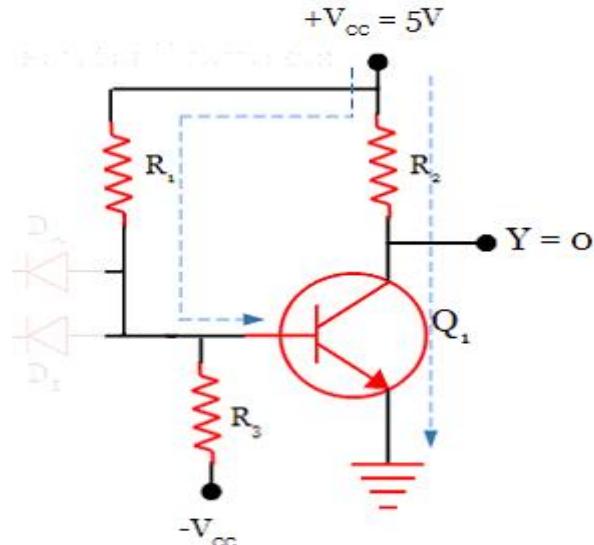
Case:1 When both inputs are low, the output is high

Now, if anyone of the input, either A or B is given LOW, which makes the corresponding diode to be forward biased. In this case, the same operation will take place.

Since any one of the diodes is forward biased, the current will go the ground through the forward-biased diode and so the transistor will be in cut off mode. The output at the terminal Y will also be at logic 1.

When both the inputs A and B are HIGH, which will reverse bias both the diode. So both diodes will not conduct. In this case, the voltage from the supply $+V_{CC}$, will be enough to drive the transistor into conduction mode.

Thus the transistor will conduct through collector and emitter. The entire voltage gets dropped in the resistor R2 and the output at the terminal Y will have LOW output, which is considered as logic 0. This operation is shown in the below figure.



Case:2 When both inputs are high, the output is low

Propagation delay:

The turn off delay is considerably larger than the turn on delay, often by a factor of 2 or 3. The propagation delay of DTL is 25 ns.

Fan-Out: A fan out as high as 8 is possible with the DTL family because of the high input impedance of the subsequent gate in the logic 1 state.

Fan-IN : It has a fan in of 8.

Advantages

It has better advantages than RTL Logic. The Diode Transistor Logic has improved noise margin, greater fan-out. However, the propagation delay is more for this device, when compared to Transistor-transistor logic(TTL). But the speed is better than RTL.

Emitter Coupled Logic (ECL) or (Non Saturating Logic): (current mode logic family)

Emitter-coupled logic is the fastest of all digital logic families. It was invented by Hannon S. Yourke in the year 1956 at IBM. It is also called as current mode logic. The design of ECL circuit consists of transistors and resistors.

By preventing the transistor from entering into saturation, the high-speed operation is achieved in ECL logic family. Very small voltage swing is necessary to switch between the two different voltage levels. This cannot be achieved in transistor-transistor logic, as the transistors enter into saturation mode, while in operation.

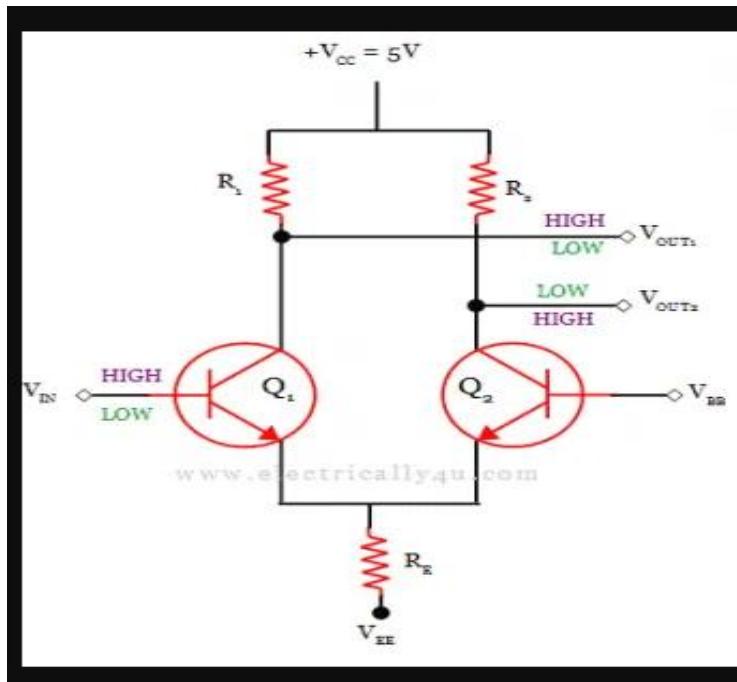
Emitter-coupled logic family offers an *incredible propagation delay of 1ns*. The delay is more reduced in the latest ECL families.

Inverter circuit of emitter-coupled logic

The circuit shown below represents the emitter-coupled logic circuit of an inverter. It has two NPN transistors connected in differential single-ended input mode.

Both the emitters are connected together with common resistance R_E . It is a current limiting resistance, used to prevent the transistor from entering into saturation.

It has two outputs: inverting output(V_{OUT1}) and non-inverting output(V_{OUT2}). V_{IN} is the input terminal, where LOW or HIGH input is given.



When the input is HIGH, it will turn ON the transistor Q1 but not saturated and the transistor Q2 is turned OFF. This will pull the output V_{OUT2} to HIGH but due to the drop in resistor R_1 , the output at terminal V_{OUT1} will be at LOW value.

On the other side, when the input V_{IN} is given LOW value, it will turn OFF the transistor Q1 and the transistor Q2 is turned ON. The transistor Q2 will not enter into saturation.

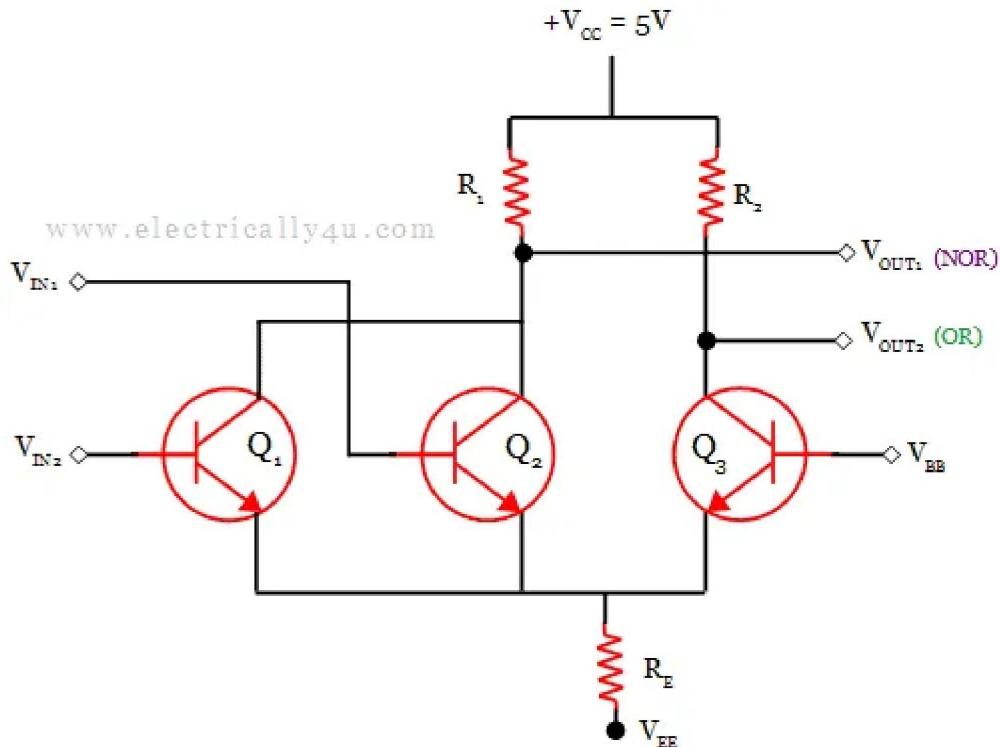
It will make the output at terminal V_{OUT1} to be pulled HIGH value. Due to the drop in resistance R_2 , the output at terminal V_{OUT2} will have LOW value.

Two input ECL OR/NOR gate

The following circuit is the Emitter-coupled logic circuit of the 2-input OR/NOR gate. It is the slight modification of the inverter circuit given above. In this, an additional transistor is used at the input side.

The operation is simple. If the input at both the transistors Q1 and Q2 are LOW, it will make V_{OUT1} to HIGH value. It corresponds to the NOR gate output. At the same time, transistor Q3 is turned ON, which will make the V_{OUT2} to be LOW. It corresponds to the OR gate output.

Similarly, if both the input of transistors Q1 and Q2 are HIGH, it will turn on both the transistors. It will drive the output at terminal V_{OUT1} to be LOW. The transistor Q3 is turned OFF during this operation. It will drive the output at terminal V_{OUT2} to be HIGH.



The truth table for OR/NOR gate is shown below.

Inputs		OR	NOR
A	B	Y	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Advantages

- High-speed operation is possible and so the fastest logic family.

- Since transistors are not allowed to enter into saturation, which reduces the storage delay.
- Fan-out capability is high.

Apart from the advantages, it also has its own disadvantage. For the fast switching of transistors, the low and high logic levels are kept close. It reduces the noise margin. Since transistors are not allowed to enter into saturation, the power consumption is more.

ECL characteristics:

The characteristics of an ECL circuit are as follows:

- (1) The logic levels are nominally -0.8v for logic 1 and -1.70v for logic 0.
- (2) The transistors never saturate i.e storage delay in ECL circuit is eliminated and hence switching speed is very high.
- (3) Because of the low noise margin 250milli volt, ECL circuits are not reliable in heavy industrial environments.
- (4) An ECL logic block usually produces an output and its complement. This eliminates the need for inverters.
- (5) Fan-Out are typically around 25.
- (6) Typical power dissipation for a basic ECL gate is 40 mW.

Transistor Transistor Logic (TTL):

The Transistor-Transistor Logic (TTL) is a logic family made up of BJTs (bipolar junction transistors). As the name suggests, the transistor performs two functions like logic as well as amplifying. The best examples of TTL are logic gates namely the 7402 NOR Gate & the 7400 NAND gate.

TTL logic includes several transistors that have several emitters as well as several inputs. The types of TTL or transistor-transistor logic mainly include Standard TTL, Fast TTL, Schottky TTL, High power TTL, Low power TTL & Advanced Schottky TTL.

The designing of TTL logic gates can be done with resistors and BJTs. There are several variants of TTL which are developed for different purposes such as the radiation-hardened TTL packages for space applications and Low power Schottky diodes that can provide an excellent combination of speed and lesser power consumption.

TTL family is a modification to the DTL. It has come to existence so as to overcome the speed limitations of DTL family. The basic gate of this family is TTL NAND gate.

TTL inputs: multiple-emitter standard TTL NAND gate:

A two input standard TTL NAND gate is a multiple emitter transistor for the inputs A and B. the output transistors Q3 and Q4 form a totem-pole output arrangement. This is the two input TTL

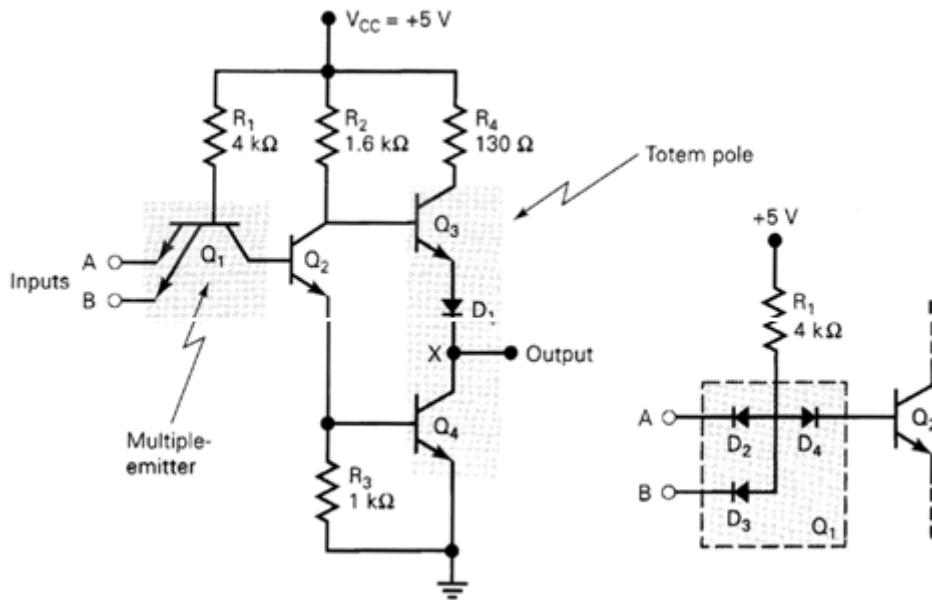
NAND gate circuit. It consists of four transistors Q1,Q2, Q3 and Q4. It also consists of four resistors R1,R2,R3,R4 and a diode D.

Transistor Q1 consists of 2 emitters, two inputs are given through this 2 emitters. Q3 and Q4 transistors together form the output. To increase the number of inputs, the number of emitters at transistor Q1 is increased accordingly.

Operation:

If A or B is low, the base-emitter junction of Q1 is forward biased and its base-collector junction is reverse biased. Then there is a current from Vcc through R1 to the base emitter junction of Q1 and into the LOW input, which provides a path to the ground for the current. Hence there is no current into the base of Q2 and making it into cut-off. The collector of Q2 is HIGH and turns Q3 into saturation. Since Q3 acts as a emitter follower, by providing a low impedance path from Vcc to the output, making the output into HIGH. At the same time, the emitter of Q2 is at ground potential, keeping Q4 OFF.

When A and B are high, the two input base emitter junctions of Q1 are reverse biased and its base collector junction is forward biased. This permits current through R1 and the base collector junction of Q1 into the base of Q2, thus driving Q2 into saturation. As a result Q4 is turned ON by Q2, and producing LOW output which is near ground potential. At the same time, the collector of Q2 is sufficiently at LOW voltage level to keep Q3 OFF.



TTL outputs: Totem pole/ active pull-up

It is possible in TTL gates the charging of output capacitance without corresponding increase in power dissipation with the help of an output circuit arrangement referred to as an active pull-up or totem-pole output.

Totem Pole means the addition of an active pull up the circuit in the output of the Gate which results in a reduction of propagation delay.

Logic operation is the same as the open collector output. The use of transistors Q4 and diode is to provide quick charging and discharging of parasitic capacitance across Q3. The resistor is used to keep the output current to a safe value.

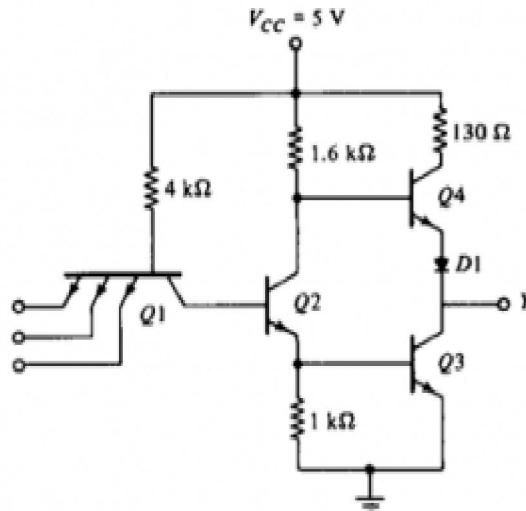


Table 5.6.1. Operation of a TTL inverter

Inputs		Transistors				Output
A	B	Q ₁	Q ₂	Q ₃	Q ₄	V _o
		Emitter junction, A	Emitter junction, B			
0	0	Forward bias (ON)	Forward bias (ON)	OFF	OFF	ON
0	1	Forward bias (ON)	Reverse bias (OFF)	OFF	OFF	ON
1	0	Reverse bias (OFF)	Forward bias (ON)	OFF	OFF	ON
1	1	Reverse bias (OFF)	Reverse bias (OFF)	ON	ON	OFF

Characteristics of TTL:

Fan in and Fan out:

Number of inputs and outputs connected to the gate, which does not affect the usual performance and does not degrade the voltage. Fan out is 10 for TTL.

Power dissipation:

It is amount of power the device needs. It is the product of the voltage which is supplied and current needed to produce the output. It is measured in mW. Usually it is 10mW for TTL

Noise Margin:

It is the amount of noise voltage allowed at the input and it should not affect the output. The noise margin is 0.4V.

Propagation Delay:

It is the time taken from applying the input to the output produce

Advantages:

- Power dissipation is less compared to DTL and RTL
- Less expensive
- Noise Margin and Fan out are better

Disadvantages:

- It cannot be used in high performance processors
- It is not used in high end electronic devices.

Applications:

- It is used in the processors in computers
- It is used in controller circuits
- Used in remote and light controller
- Used in microprocessor and microcontrollers

Que 5.5. | Describe the construction and operation of TTL inverter gate (NOT gate).

Answer

Fig. 5.5.1 shows a standard TTL circuit for an inverter. Transistor, Q_1 is the input coupling transistor, and D_1 is the input clamp diode. Transistor, Q_2 is called a phase splitter, and the combination of Q_3 and Q_4 forms the output circuit often referred to as a totem-pole arrangement.

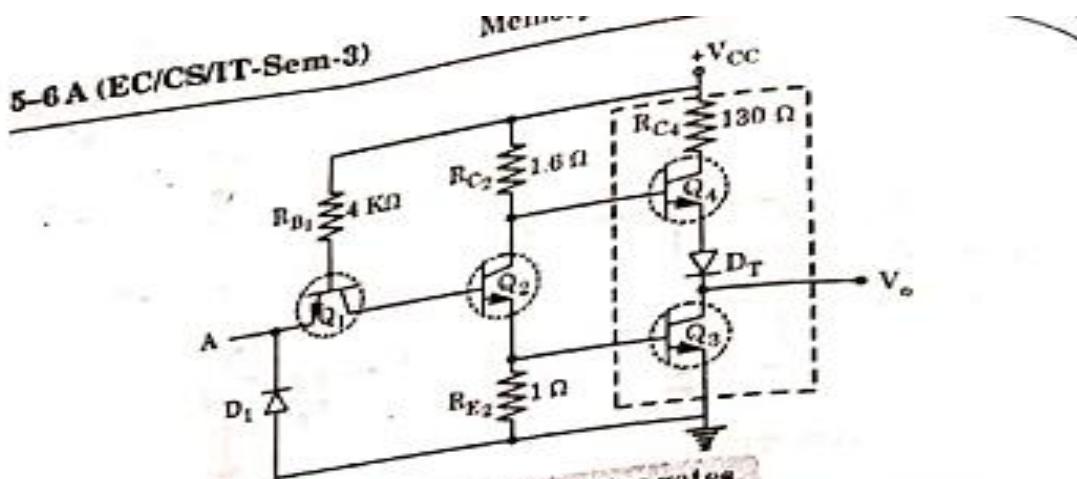


Fig. 5.5.1. TTL inverter gates.

2. When the input is a HIGH, the base-emitter junction of transistor, Q_1 is reverse-biased and the base-collector junction is forward-biased.
3. This condition permits current to flow through R_{B_1} and the base-collector junction of transistor, Q_1 into the base of transistor, Q_2 .
4. It drives transistor, Q_2 into saturation. As a result, transistor, Q_3 is turned ON due to ON state of transistor, Q_2 and its collector voltage, which is the output, is near to ground potential.
5. Therefore a LOW output is produced for a HIGH input. At the same time, the collector of transistor, Q_2 is at a sufficiently LOW voltage level to keep transistor, Q_4 OFF.
6. When the input is LOW, the base-emitter junction of transistor, Q_1 is forward-biased, and the base-collector junction is reverse-biased.
7. The current flows through resistor, R_{B_1} and the base-emitter junction of transistor, Q_1 , to the LOW input. A LOW provides a path to ground for the current.
8. No current flows into the base of transistor, Q_2 , so it is OFF. The collector of transistor, Q_2 is HIGH, thus turning transistor, Q_4 ON. A saturated transistor, Q_4 provides a low-resistance path from V_{CC} to the output.
9. Therefore, a HIGH on the output is produced for a LOW on the input. At the same time, the emitter of transistor, Q_2 is at ground potential, keeping transistor, Q_3 OFF.

Table 5.5.1. Operation of TTL inverter.

Inputs	Transistors				Output V_o
	Q_1	Q_2	Q_3	Q_4	
	Emitter junction, A				
Logic 0	Forward bias (ON)	OFF	OFF	ON	Logic 1
Logic 1	Reverse bias (OFF)	ON	ON	OFF	Logic 0

Que 5.7. Describe the construction and operation of TTL NOR gate.

Answer

TTL NOR gate :

- The circuit of the two-input TTL NOR gate is shown in Fig. 5.7.1. Two input transistors Q_A and Q_B are emitter transistors.

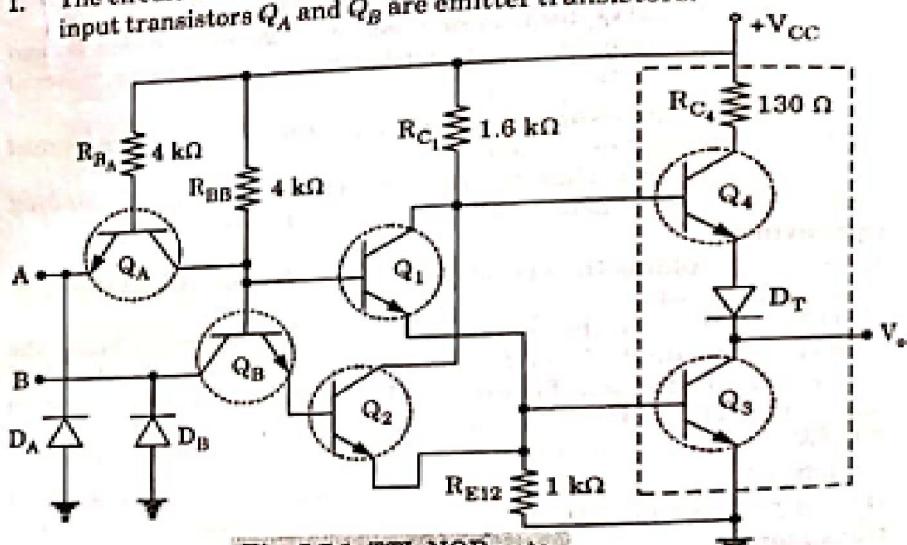


Fig. 5.7.1. TTL NOR gate.

Digital Logic Design

... I.E.C/CSIT-Sem-3)

- Transistor Q_1 and Q_2 are called the phase splitters. Emitter of transistor Q_1 is connected to collector of transistor Q_4 through diode D_T .
- Transistors Q_3 and Q_4 form a totem-pole arrangement. Diodes D_A and D_B protect transistor Q_1 from being damaged by the negative spikes of voltages at the inputs.
- When negative spikes appear at the input terminals, the diodes conduct and bypass the spikes to ground.
- Diode D_T ensures that transistors Q_3 and Q_4 do not conduct simultaneously. Transistor Q_3 acts as an emitter follower.

Operation :

Table 5.7.1. Operation of TTL NOR gate.

Inputs		Transistors						Output
A	B	Q_A	Q_3	Q_1	Q_2	Q_3	Q_4	V_o
		Emitter junction, A	Emitter junction, B					
	0	Forward bias (ON)	Forward bias (ON)	OFF	OFF	OFF	ON	1
0	1	Forward bias (ON)	Reverse bias (OFF)	OFF	ON	ON	OFF	0
0	0	Reverse bias (OFF)	Forward bias (ON)	ON	OFF	ON	OFF	0
1	1	Reverse bias (OFF)	Reverse bias (OFF)	ON	ON	ON	OFF	0

Various TTL parameters in brief.

Que 5.4. | Explain direct coupled transistor logic (DCTL) of logic family.

Answer

Fig. 5.4.1(a) shows the circuit for DCTL-NOR gate and Fig. 5.4.1(b) shows the circuit for DCTL-NAND gates.

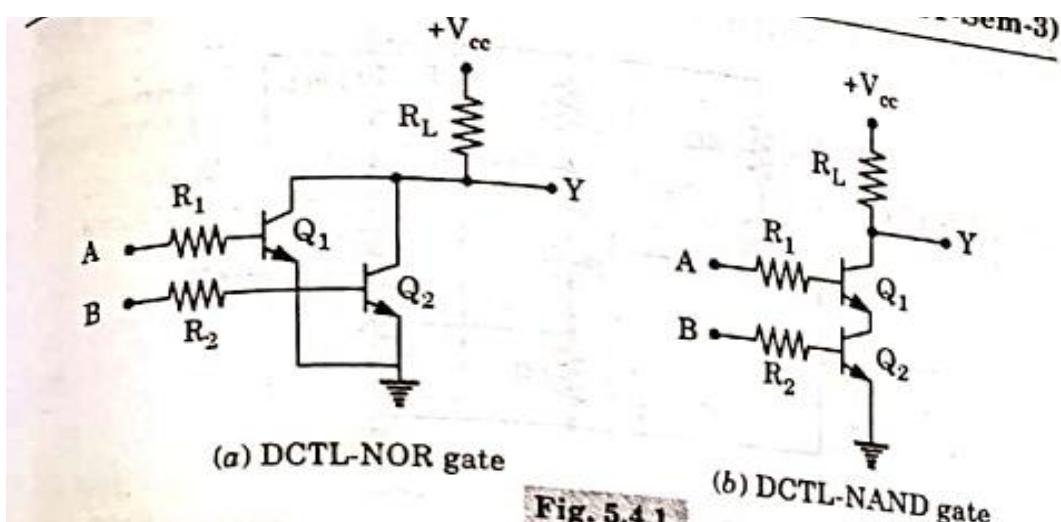


Fig. 5.4.1.

- 2 In DCTL - two input NOR gate of Fig. 5.4.1(a), there are two transistors Q_1 and Q_2 which share a common load resistor R_L .
- 3 If any one or both inputs A and B are high at level '1', then base current will be supplied to one or both the transistors, causing them to conduct and thus collector current will flow through load resistor R_L .
- 4 This makes the output voltage at Y to go low. Whereas when both A and B are low, both transistors Q_1 and Q_2 remain in cut-off state and thus the output at Y approaches that of the supply voltage V_{cc} at high level.
- 5 In the DCTL - two input NAND gate of Fig. 5.4.1(b), both the transistors Q_1 and Q_2 are connected in series.
- 6 Only when both inputs A and B are high, both transistors Q_1 and Q_2 will conduct, as they are in series. This causes output voltage at Y to go low.
- 7 When any one or both inputs A and B are low, both transistors Q_1 and Q_2 cannot conduct. Therefore the output voltage at Y remains high.
- 8 The transistor with lower input impedance draws more current than the other transistors.
- 9 The transistors which draw less current will not turn on properly and give rise to malfunctioning of the circuit. This phenomenon is known as current hogging or more precisely as base current hogging.

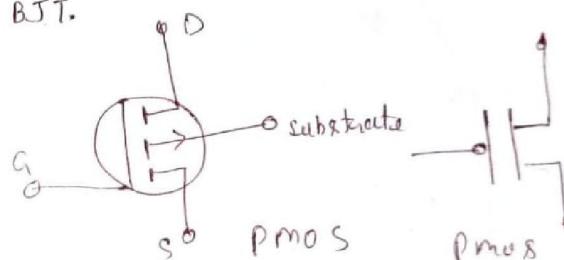
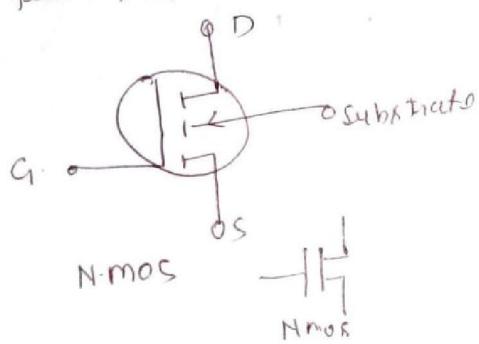
Cmos :- Complementary metal oxide semiconductor.

= CMOS is the semiconductor technology used in most of today integrated circuit (IC), also known as chips or microchips. CMOS transistors are based on MOSFET technology.

⇒ CMOS is a combination of NMOS and PMOS transistors that operate under the applied electrical field. The structure of CMOS was initially developed for high density and low power logic gates.

⇒ The CMOS transistors are used in various applications, such as amplifier, switching circuit, logic circuit, integrated circuit chips, microprocessors etc.

⇒ The importance of CMOS in semiconductor technology is its low power dissipation and low operating currents. Its manufacturing requires fewer steps as compared to the BJT.



⇒ The NMOS transistors are designed to work as positive logic elements, while PMOS would act as negative logic element. It means that both the transistors in a CMOS perform complementary logic functions.

Features of CMOS logic gates :- The features of CMOS logic gates are listed below.

(1) Reduced cost as it requires only a single power supply.

(2) Large logic swing.

(3) Very high noise margin.

(4) Lower propagation delay.

(5) High speed as compared to NMOS transistors.

(6) Lower power dissipation.

Excellent temperature stability.

(b) less packaging density.

N-channel:

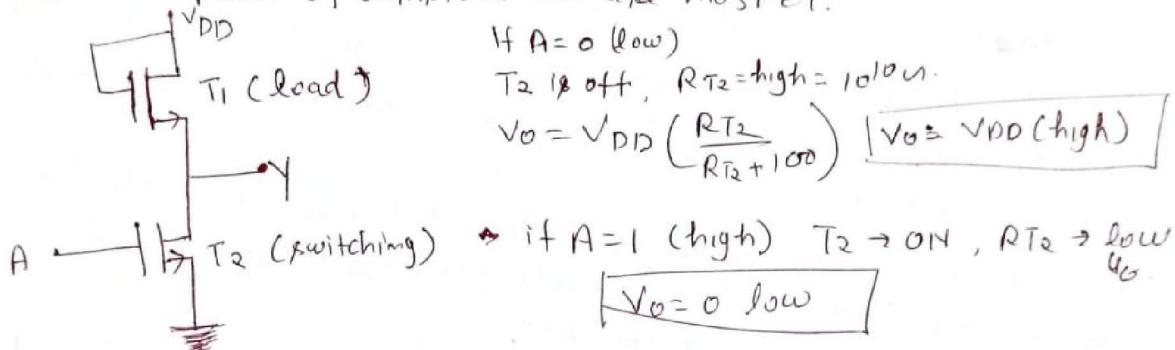
logic 0 = off

logic 1 = on

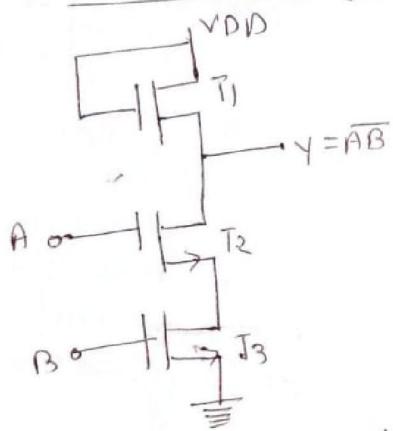
PMOS: logic 0 = on

logic 1 = off

→ since FET is voltage variable resistor (VVR) hence in MOS circuit in place of resistors we use mosFET.



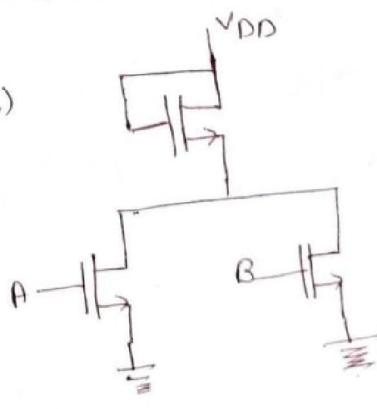
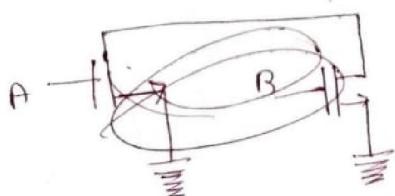
* NMOS NAND gate:

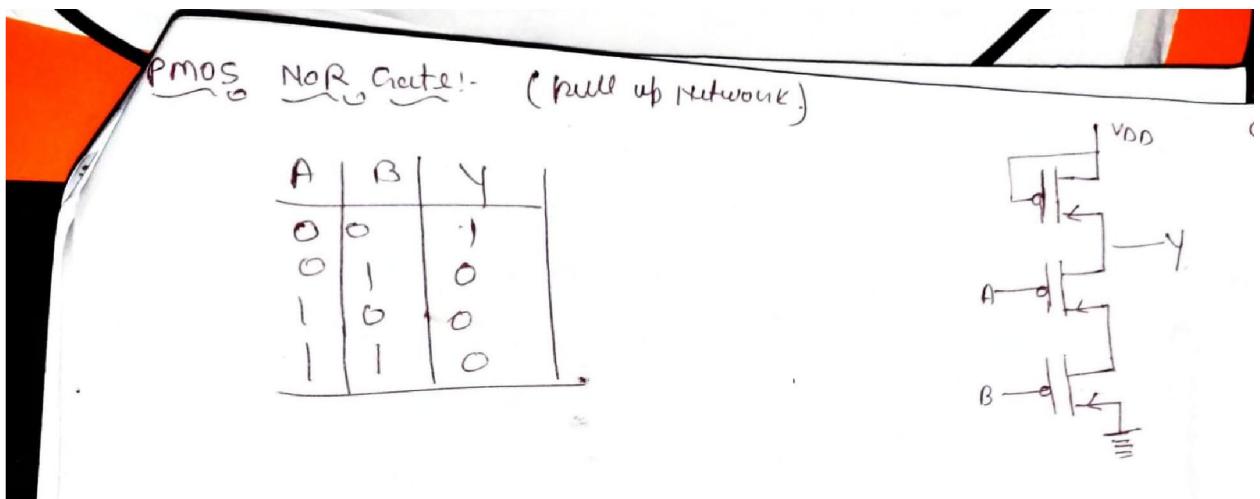


A	B	T_2	T_3	Y
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

When both J/P are high, both mosFET are ON so Y is get connect to ground.

NMOS NOR gate (pull down N/W)





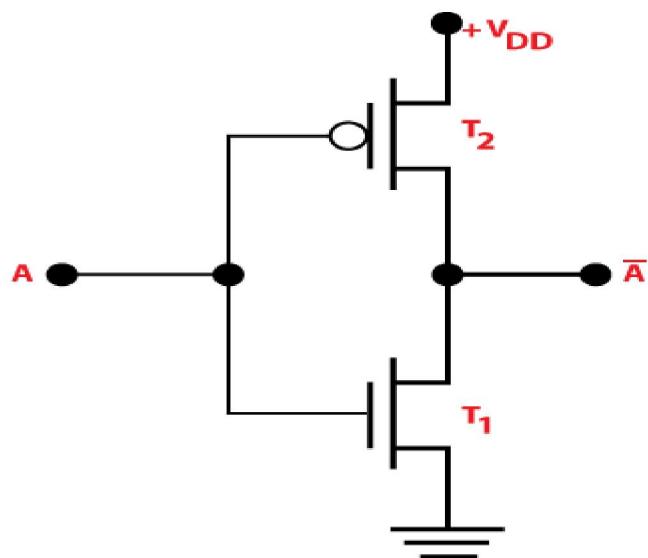
Types of CMOS logic gates

The Complementary Metal Oxide Semiconductors are categorized as:

- CMOS Inverter
- CMOS NAND
- CMOS NOR
- CMOS Operational Amplifiers

CMOS Inverter

The CMOS inverter is formed by connecting the PMOS and NMOS transistors in cascade, as shown below:



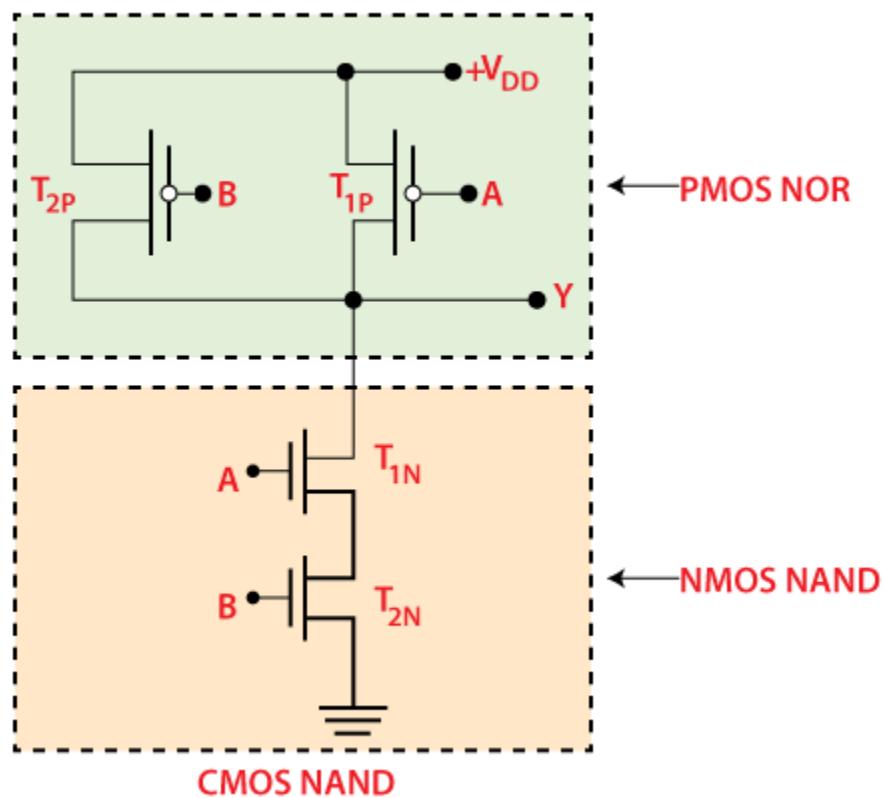
The top of the CMOS inverter is the PMOS transistor, while the bottom transistor is NMOS. The positive voltage of $+V_{DD}$ at the gate input of the NMOS transistors will turn it ON, while the same positive voltage at the gate input of the PMOS transistor will keep it OFF. Similarly, the voltage of 0 volts at the gate input of the NMOS transistors will keep it OFF, while the same 0 at the gate input of the PMOS transistor will turn it ON.

It means that NMOS transmits logic 1 or V_{DD} , and PMOS transmits logic 0.

CMOS NAND

CMOS NAND is a combination of **NMOS NAND** and **PMOS NOR**. It consists of an NMOS NAND gate with the PMOS NOR as its load. CMOS NAND gate can also include a PMOS NOR with the NMOS NAND as its load. It means that NMOS and PMOS transistors' combination in the desired manner forms a CMOS logic gate.

The circuit diagram of CMOS NAND is shown below:



The input terminal of the transistors is A and B, as shown above. If $A = 0$ and $B = 0$, the NMOS transistors will remain off, and the two PMOS transistors will conduct.

Consider the NOR table shown below:

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

It clearly shows that the output is 1 when the two inputs are 0. Hence, PMOS NOR will conduct. The output Y will be:

$$Y = \text{logic 1} = VDD$$

Similarly, when both the input is 1, the NMOS NAND will conduct, and PMOS NOR will remain OFF. But, the output will be 0 because the power will pass to the ground.

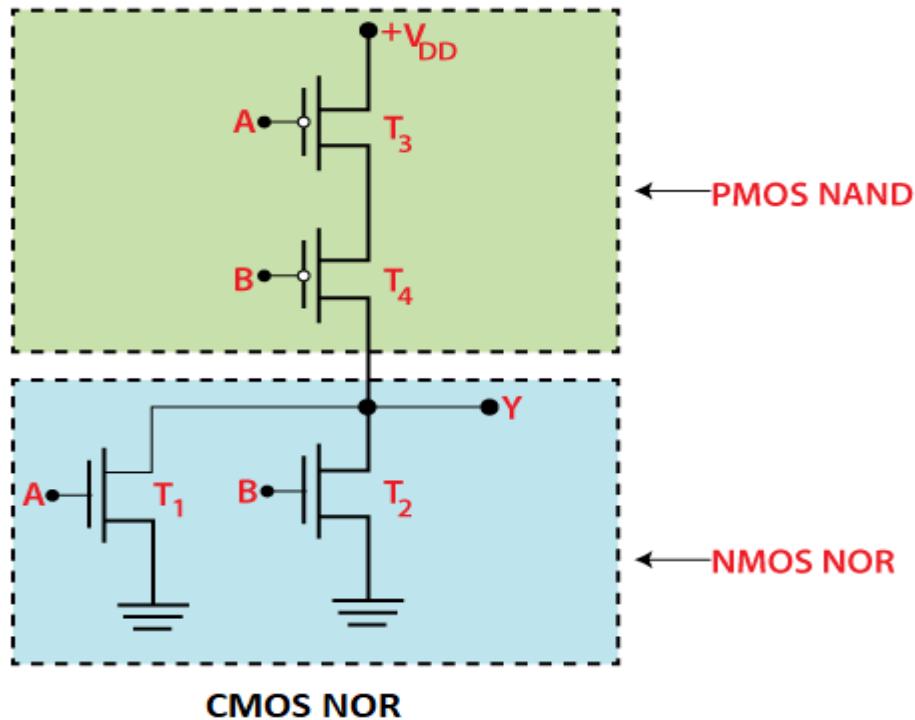
Consider the CMOS NAND table shown below:

A	B	CMOS NAND
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NOR

CMOS NOR logic gate is a combination of NMOS NOR and PMOS NAND. The circuit diagram is shown below:

When both the input A and B are 0, NMOS NOR will remain OFF, and PMOS NAND will conduct. It means that transistors T1 and T2 will be OFF, while T3 and T4 will conduct. Thus, the output will be logic 1 when the voltage VDD reaches through the conduction of transistors T3 and T4.



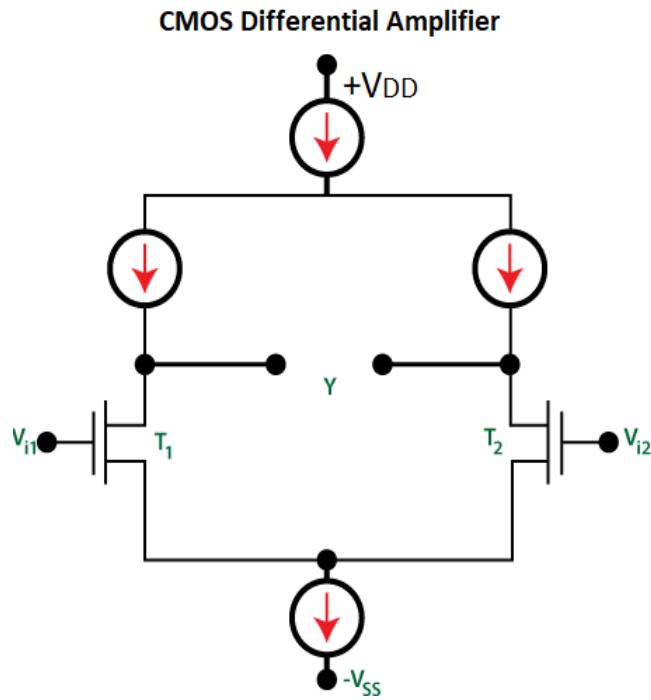
CMOS NOR will conduct only when both the inputs are 0 as discussed above. At all the other input conditions, the output will be 0, as listed below:

A	B	CMOS NOR
0	0	1
0	1	0
1	0	0
1d	1	0

CMOS Operational Amplifiers

The CMOS structures can also be used as an amplifier when the operating point is fixed in the active region.

Let's consider an example of a CMOS differential amplifier using constant current sources.



Advantages of CMOS

Let's discuss the advantages of the Complementary Metal Oxide Semiconductor, which are listed below:

Very low power dissipation

There is no continuous current path from the positive terminal of the transistor to its negative terminal throughout the circuit except the switching instants. Hence, it has the least amount of power dissipation.

Reduced circuit complexity

CMOS requires fewer components, due to which the circuit complexity reduces.

Produces very less heat

CMOS produces significantly less heat as compared to other transistors, such as NMOS and TTL (Transistor-Transistor Logic). Other transistors have some standing current even in the unchanged state, while CMOS does not have.

Low static power Consumption

In an ideal state, CMOS dissipates almost zero or no power as compared to other circuits. It means that it only dissipates power while switching. The lesser dissipation results in lower power consumption. Hence, CMOS has very low static power consumption.

Temperature stability

CMOS family is stable in a wider temperature range compared to other logic circuits, such as TTL. The operating range of CMOS is around -55 degrees Celsius to 125 degrees, while TTL is 25 to 70 degrees Celsius.

Improved Noise immunity

Noise immunity refers to the ability of a system to function in the presence of noise interference. CMOS has the highest noise immunity as compared to the circuit of logic families. Hence, it is highly preferred in high noise automotive applications.

High fan-out

Fan out specifies the input gates driven by the output of the other gate. It means the highest number of input gates of a particular type to which the output can be connected. The fan-out feature measures the load driving ability of a logic gate. Thus, CMOS has a high fan out.

Applications of CMOS

The applications of CMOS are listed below:

Integrated Circuits

CMOS consumes less current than other logic devices, such as TTL. Hence, the use of CMOS in the Integrated Circuit applications forms the production of ICs that has lower consumption and low dissipation.

Chip designing

The use of CMOS in chip designing allows the high-density logic functions to be integrated on a chip.

Microprocessor designing

CMOS requires current only during the switching state. It means that CMOS uses the power efficiently. Hence, CMOS is used in most modern processors, such as microprocessors.

ASIC designing

It stands for Application Specific Integrated Circuits. CMOS is considered the standard transistor for the fabrication of chips. Hence, it is used in ASIC designing.

CPU Memories

The two major advantages of CMOS are high noise immunity and low static power consumption. Due to this, it is used in the CPU (Central Processing Units) Memories.

CMOS vs. NMOS

Let's discuss some differences between CMOS and NMOS for a better understanding. It will help us to analyze the applications of both these transistors in electronics.

Category	CMOS	NMOS
Full Form	Complementary Metal Oxide Semiconductor.	N-type Metal Oxide Semiconductor.
Formation	It is a combination of NMOS and PMOS.	It only consists of NMOS.
Logic transmission	CMOS transmits both logic 1 and logic 0.	NMOS transmits only logic 1.
Advantages	High fan-out, lower power dissipation, etc.	Lowest required diffusion steps, etc.
Applications	Batteries, sensors, cameras, etc.	Logic gates and digital circuits.

Programmable Logic Devices

Programmable Logic Devices *PLDs* are the integrated circuits. They contain an array of AND gates & another array of OR gates. There are three kinds of PLDs based on the type of array *s*, which has programmable feature.

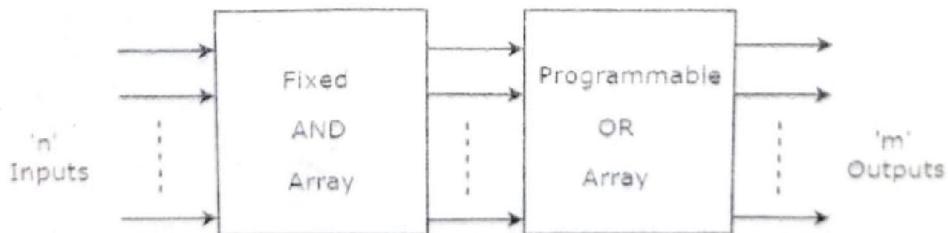
- Programmable Read Only Memory
- Programmable Array Logic
- Programmable Logic Array

The process of entering the information into these devices is known as **programming**. Basically, users can program these devices or ICs electrically in order to implement the Boolean functions based on the requirement. Here, the term programming refers to hardware programming but not software programming.

Programmable Read Only Memory *PROM*

Read Only Memory *ROM* is a memory device, which stores the binary information permanently. That means, we can't change that stored information by any means later. If the ROM has programmable feature, then it is called as **Programmable ROM** *PROM*. The user has the flexibility to program the binary information electrically once by using PROM programmer.

PROM is a programmable logic device that has fixed AND array & Programmable OR array. The **block diagram** of PROM is shown in the following figure.



Here, the inputs of AND gates are not of programmable type. So, we have to generate 2^n product terms by using 2^n AND gates having n inputs each. We can implement these product terms by using $n \times 2^n$ decoder. So, this decoder generates ' n ' min terms.

Here, the inputs of OR gates are programmable. That means, we can program any number of required product terms, since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PROM will be in the form of **sum of min terms**.

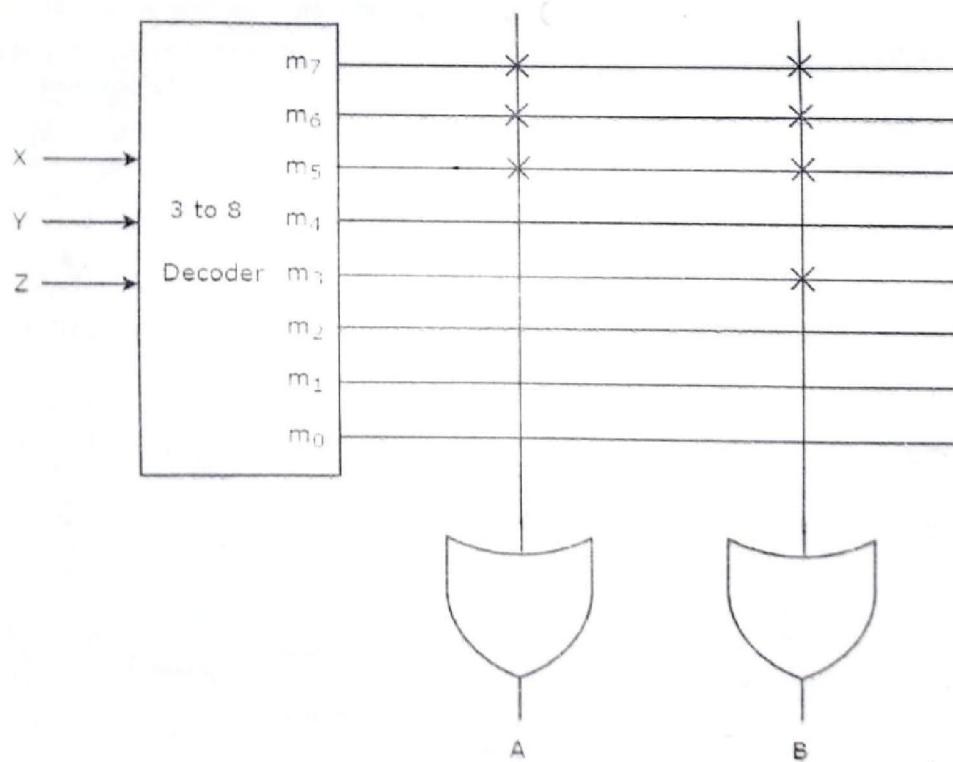
Example

Let us implement the following **Boolean functions** using PROM.

$$A(X, Y, Z) = \sum m(5, 6, 7)$$

$$B(X, Y, Z) = \sum m(3, 5, 6, 7)$$

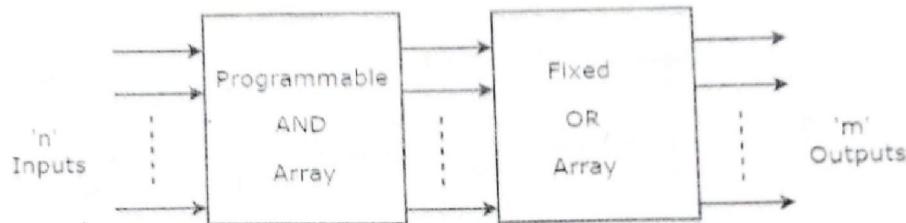
The given two functions are in sum of min terms form and each function is having three variables X, Y & Z. So, we require a 3 to 8 decoder and two programmable OR gates for producing these two functions. The corresponding **PROM** is shown in the following figure.



Here, 3 to 8 decoder generates eight min terms. The two programmable OR gates have the access of all these min terms. But, only the required min terms are programmed in order to produce the respective Boolean functions by each OR gate. The symbol 'X' is used for programmable connections.

Programmable Array Logic *PAL*

PAL is a programmable logic device that has Programmable AND array & fixed OR array. The advantage of PAL is that we can generate only the required product terms of Boolean function instead of generating all the min terms by using programmable AND gates. The **block diagram** of PAL is shown in the following figure.



Here, the inputs of AND gates are programmable. That means each AND gate has both normal and complemented inputs of variables. So, based on the requirement, we can program any of those inputs. So, we can generate only the required **product terms** by using these AND gates.

Here, the inputs of OR gates are not of programmable type. So, the number of inputs to each OR gate will be of fixed type. Hence, apply those required product terms to each OR gate as inputs. Therefore, the outputs of PAL will be in the form of **sum of products form**.

Example

Let us implement the following Boolean functions using PAL.

$$A = XY + XZ'$$

$$B = XY' + YZ'$$

The given two functions are in sum of products form. There are two product terms present in each Boolean function. So, we require four programmable AND gates & two fixed OR gates for producing those two functions. The corresponding **PAL** is shown in the following figure.

those inputs. So, we can generate only the required product terms by using these AND gates. Here, the inputs of OR gates are also programmable. So, we can program any number of required product terms, since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PAL will be in the form of sum of products form.

Example

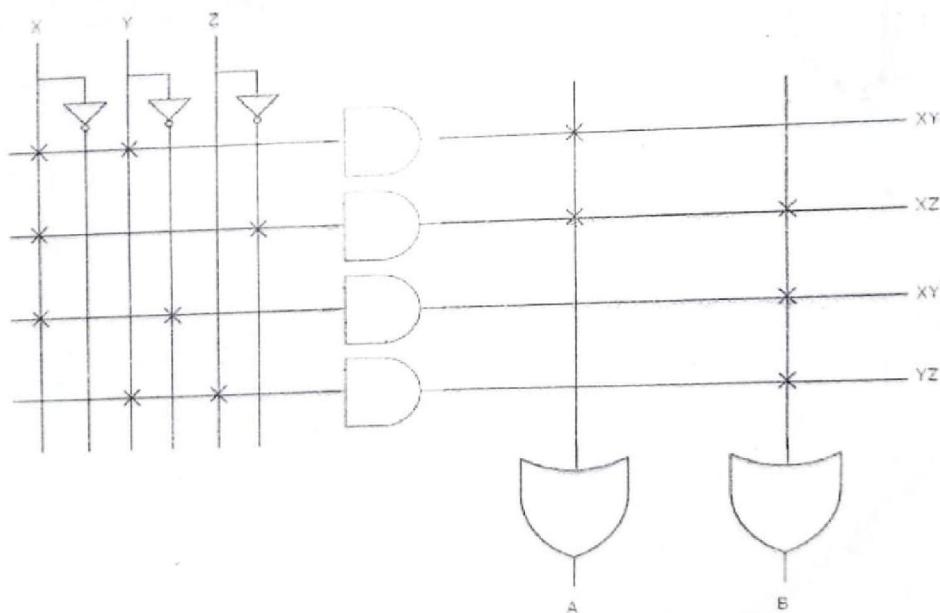
Let us implement the following **Boolean functions** using PLA.

$$A = XY + XZ'$$

$$B = XY' + YZ + XZ'$$

The given two functions are in sum of products form. The number of product terms present in the given Boolean functions A & B are two and three respectively. One product term, $Z'X$ is common in each function.

So, we require four programmable AND gates & two programmable OR gates for producing those two functions. The corresponding **PLA** is shown in the following figure.



The **programmable AND gates** have the access of both normal and complemented inputs of variables. In the above figure, the inputs X, X', Y, Y', Z & Z' , are available at the

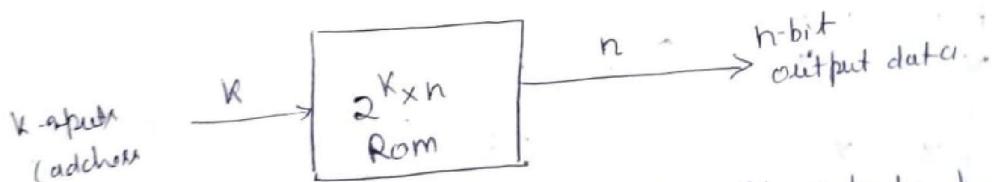
inputs of each AND gate. So, program only the required literals in order to generate one product term by each AND gate.

All these product terms are available at the inputs of each **programmable OR gate**. But, only program the required product terms in order to produce the respective Boolean functions by each OR gate. The symbol 'X' is used for programmable connections.

Programmable logic device A programmable logic device is a general name for a digital integrated circuit capable of being programmed to provide a variety of digital logic functions. A variety of combinational and sequential logic circuit are implemented within a single chip. There are three types of PLD.

- ① Read only memory (Rom)
- ② Programmable logic Array (PLA)
- ③ Programmable array logic (PAL)
- ④ Field Programmable Gate Arrays (FPGA).

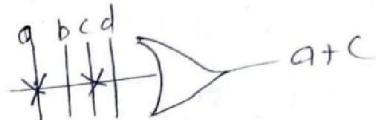
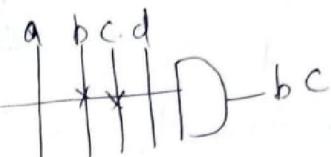
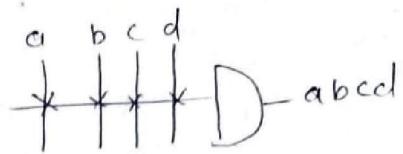
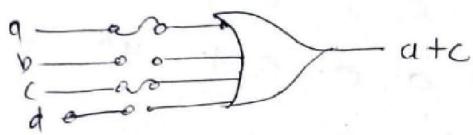
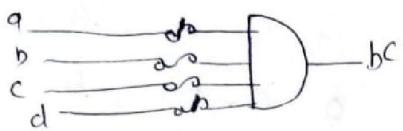
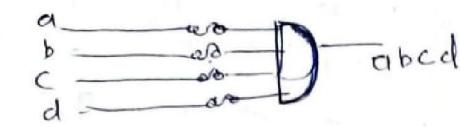
Read only memory (Rom) A Rom is a memory device in which permanent binary information is stored. Binary information must be specified by the designer and is then interconnected in the unit to form the required interconnection pattern. Once the pattern is established, it stays within the unit even when power is turned off.



It consists of K inputs and n outputs. The inputs provide the address for the memory and output give the data bits of the stored word which is selected by the address.

→ the number of words in a Rom is determined from the fact that K-address input lines are needed to specify 2^K words. Rom does not have a write operation.

symbol representation of PLD:



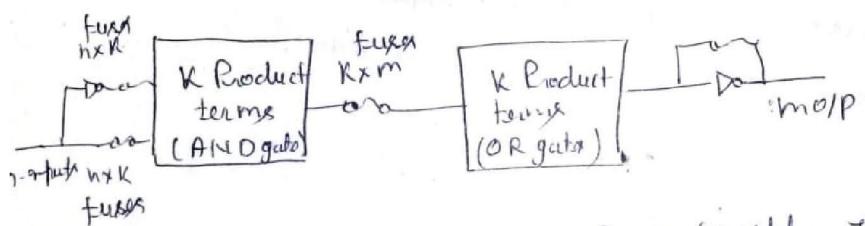
Ans: A combinational logic circuit has 4 inputs and two outputs F_1 & F_2 . The O/P F_1 gives high O/P when the input combinational is greater than or equal to 1001, otherwise low output. The output F_2 gives high O/P when the input combinational is less than 1001 otherwise the O/P F_2 is low.

Input				Output	
A	B	C	D	F_1	F_2
0	0	0	0	0	1
0	0	0	1	0	1

= first determine the table \Rightarrow solve K-map for O/P F_1 & F_2
and draw the connection.

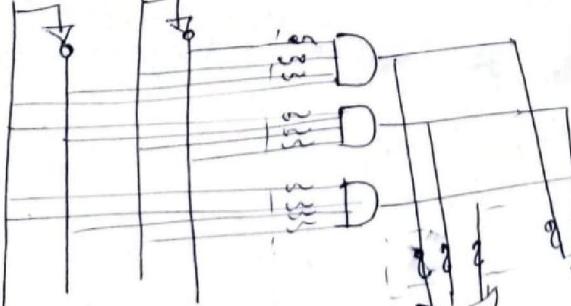
Inputs	Decimal equivalent	Outputs	Decimal equivalent							
A ₂	A ₁	A ₀	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1	1
0	1	0	0	0	0	1	0	0	4	4
0	1	1	0	0	1	0	0	1	9	9
1	0	0	0	0	1	0	0	1	16	16
1	0	1	0	1	1	0	0	1	25	25
1	1	0	1	0	0	1	0	0	36	36
1	1	1	1	1	0	0	0	1	49	49

Programmable logic Array (PLA)



The PLA is similar to the ROM concept. The decoder is replaced by an AND array which realizes selected product terms of the input variables. In this PLA, the AND array and OR array both are programmable.

A B AND programming



OR programming

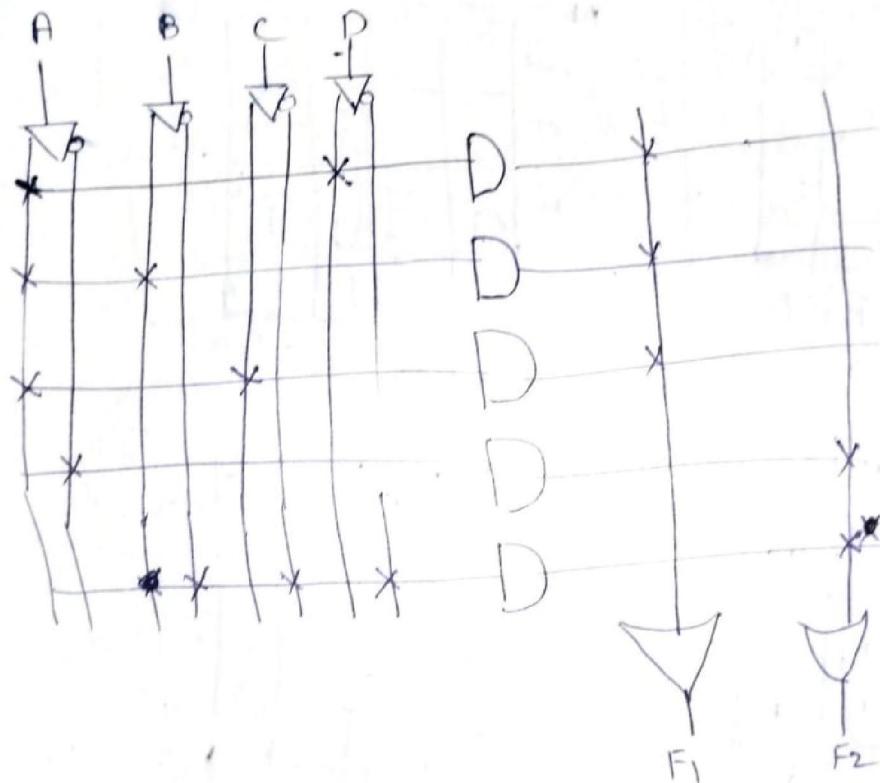


P			
00	01	11	10
00	0	1	0
01	0	1	0
11	1	1	1
10	1	1	1

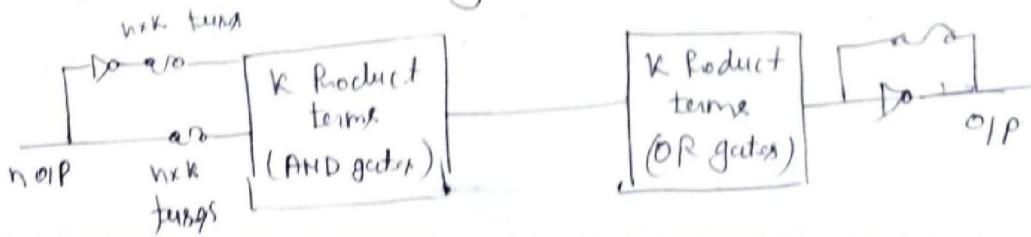
P			
00	01	11	10
00	1	1	1
01	1	1	1
11	1	1	1
10	1	1	1

$$F_1 = AB + AD + AC$$

$$F_2 = \overline{A} + \overline{B}C\overline{D}$$



Programmable Array Logic (PAL): the PAL is a special type of PLD. In this PAL, the AND array is programmable and the OR array is fixed.



Ques Implement the following function using PAL. (uptu 2007 - 10)

$$W(A, B, C, D) = \sum(2, 13, 15)$$

$$X(A, B, C, D) = \sum(7, 8, 9, 10, 11, 12, 13, 14, 15)$$

$$Y(A, B, C, D) = \sum(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$$

$$Z(A, B, C, D) = \sum(1, 2, 8, 12, 13)$$

Ans

AB	CD	00	01	11	10
00		0	1	3	11
01		4	5	7	6
11		11	12	13	15
10		8	9	11	10

$$W = AB\bar{C} + \bar{A}\bar{B}\bar{C}\bar{D}$$

AB	CD	00	01	11	10
00		0	1	1	1
01		1	1	1	1
11		1	1	1	1
10		1	1	1	1

$$X = A + BCD$$

AB	CD	00	01	11	10
00		1	1	1	1
01		1	1	1	1
11		1	1	1	1
10		1	1	1	1

$$Y = \bar{A}B + CD + \bar{B}\bar{D}$$

AB	CD	00	01	11	10
00		1	1	1	1
01		1	1	1	1
11		1	1	1	1
10		1	1	1	1

$$Z = ABC + A\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{A}\bar{C}\bar{D}$$

$$= W + A\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}$$

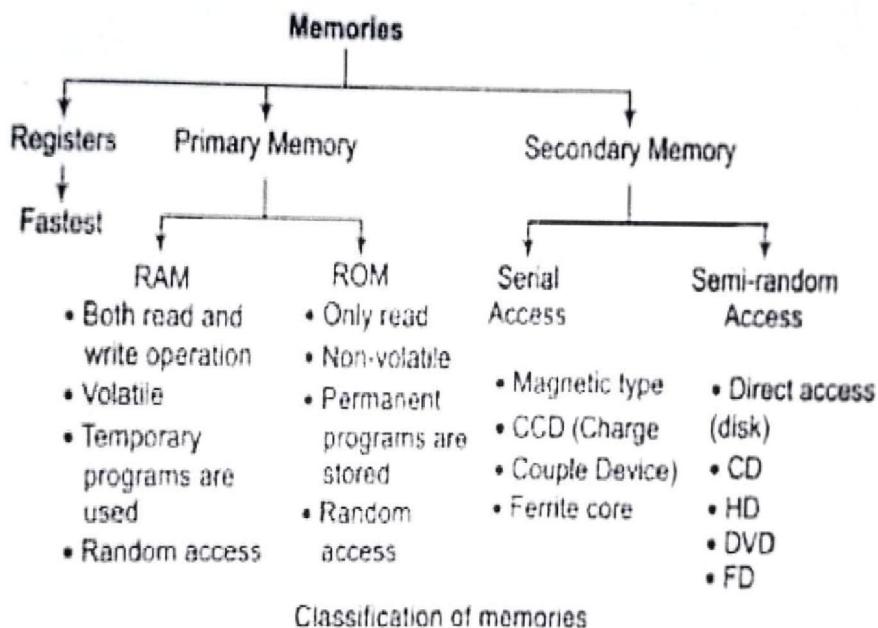
draw the diagram

Semiconductor Memories

In this article, Candidates can find **study notes on semiconductor memories** which cover the topics such as **memory, RAM and ROM and some basic concepts related to PLA, PAL and FPFA.**

1. Memory

- A memory is a semiconductor or magnetic device used for storage of digital data.
- A memory location is a group of storage devices that will hold one data word.
- A data word length of 8-bits is called a byte.
- Each memory location can store a different data word and has a unique address.
- Memory can hold one or more bits of information to store the Data, Instruction, and Addresses.
- Memory can be classified into the following three groups.



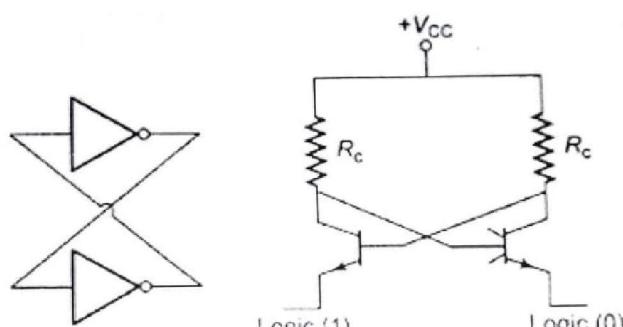
- **Registers:** Registers are memories located within the Central Processing Unit (CPU). Various types of registers are available within CPU. Registers are small but CPU can access it quickly. Some of the registers available in the system are given below.
 - Instruction Register, ALU I/O registers, Status Register, Stack pointer register, Program counter, etc.
- **Primary Memory:** It is classified into two types, namely RAM and ROM.

- **Secondary Memory:** Disk memory is used to hold programs and data over the longer term. The contents of a disk are NOT lost if the power is turned off. Disks are much slower than Register.

Random Access Memory (RAM): The time taken to transfer information to or from any desired location is always same hence it is called Random Access Memory (RAM).

- Memory size = $2^n \times m$, where n: address line, m: data
- RAM can be classified into two types, namely Static RAM and Dynamic RAM.

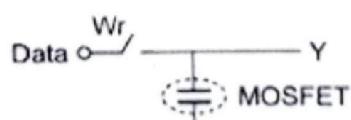
Static RAM (SRAM): In this type of RAM, data is retained as long as there is the power supply.



Symbol and circuit diagram of SRAM

- Data is stored in flip flop like structure.
- It can be implemented with BJT or MOSFET.
- It is Faster.
- Dissipates more power.
- The memory capacity of Static RAM is less.
- It can be used as Cache memory.
- No refreshing required.

Dynamic RAM (DRAM): In this type of RAM, data is stored on capacitors and requires periodic refreshment.



Circuit diagram of DRAM

- Data is stored in MOS capacity.
- Only MOSFET is used for implementation.
- It is Slow compared to Static RAM.
- Dissipate less power.
- The memory capacity of Dynamic RAM is more.
- It can be used as Main memory.
- Refreshing is required.

Advantages of static RAM over Dynamic RAM:

- The access time of SRAM is less and thus these memories are faster memories.
- As SRAM consists of flip-flops thus, refreshing is not required.
- Less number of memory cells are required in SRAM for a unit area.

Read Only Memory (ROM): It is non-volatile memory, implemented using the combinational circuit. It is also known as masked memory.

Classification of ROM's:

1. **Mask programmed ROM:** The required contents of the memory are programmed during fabrication. Data stored this way can never be altered. It can be implemented using Fixed AND Fixed OR Circuit.
2. **PROM (Programmable ROM):** Required content is written in a permanent way by burning out internal interconnections (fuses). It is a one-off procedure. It can be implemented using Fixed AND Programmable OR Circuit.
3. **EPROM (Erasable PROM):** Data is stored as a charge on an isolated gate capacitor ("floating gate"). Data is removed by exposing the PROM to the ultraviolet light.
4. **EEPROM (Electrically Erasable PROM):** It is also called as Flash Memory. The content can be re-programmed by applying suitable voltages to the EEPROM pins. The Flash Memories are very important data storage devices for mobile applications.

PLDs (Programmable Logic Devices): Programmable logic devices are the special type of IC's used by the USE. Different type of logic functions can be implemented using a single programmed IC chip of PLD. PLDs can be reprogrammed because these are based on rewritable memory technologies. PLDs are divided into three types. They are PLA, PAL and FPGA. **PLA (Programmable Logic Array):**

- PLA is implemented using AND-OR gate arrays and programmed for specific logic functions.
- It is used where the number of don't care conditions are excessive.
- In PLA's both AND and OR arrays are programmable.
- The AND and OR gates are fixed for any PLA chip.
- It depends on the number of inputs and outputs of PLA.
- Combinational circuits, Sequential Circuits, Compact circuits can be implemented using PLAs.

PAL (Programmable Array Logic):

- PAL is implemented using AND gate arrays are programmable and OR gate arrays are fixed.
- Because only AND gates are programmable, the PAL is easier to program, but it is not as flexible as the PLA (programmable logic array).

PGA or FPGA (Field Programmable Gate Array):

- It is a semiconductor device that is comprised of a different number of logic elements, interconnects, and Input / Output blocks. All these components are user-configurable.