EE537 Circuit Simulation Lab
Experiment 8

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AIM : Design of an inverting amplifier using a two stage OTA

Design an inverting amplifier using a 2 stage miller compensated OTA. Fig. 1 shows the schematic of the inverting amplifier to be designed.

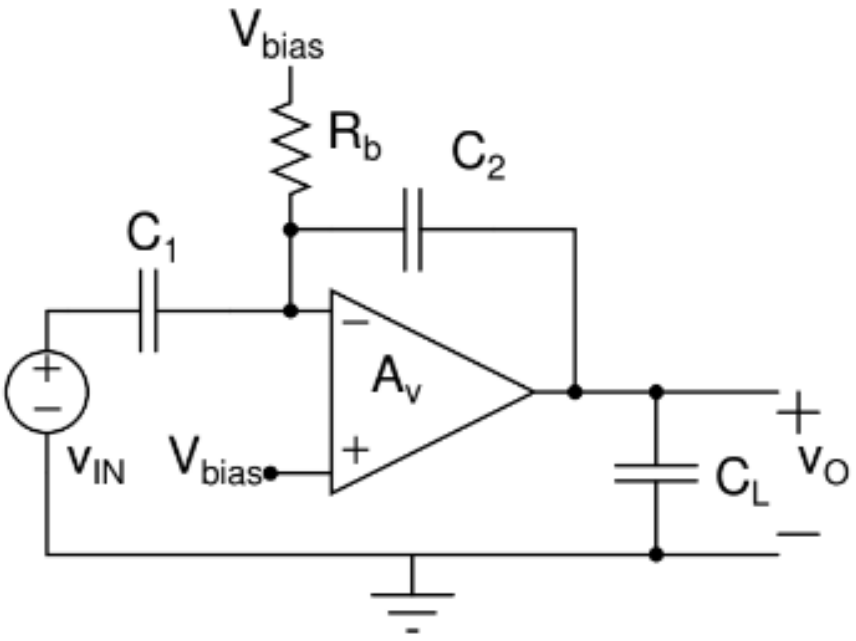

Figure 1: Inverting amplifier with capacitive voltage feedback

Target Specification

Specification	Value
Midband Gain	20dB
Bandwidth	$> 1MHz$
Input Capacitance	1pF
Load Capacitance	10pF
Slew Rate	$\geq 10V/\mu s$
Gain error	0.1
Phase Margen	$\geq 65^oC$
Operating temperature range	$(0 - 70)^oC$

Table 1: Specification Table

1 Implement the 2 stage using a miller compensated 2 stage OTA. Show the calculations used for all the specifications and detailed design procedure.

An unbuffered Op-Amp is referred to as an OTA. It is frequently referred to as simply "Op-Amp" in CMOS circuit literature .Op-Amp stands for operational amplifier, whereas OTA stands for operational transconductance amplifier. Op-Amp output resistance is greater than OTA output impedance ($R_{out} = \infty$) is the same as zero.

1.1 Uncompensation of two stage OTA

Because the two poles of an uncompensated network are near to one another, the phase margin and gain are both relatively low. Prior to the phase plot reaching zero, the magnitude plot must cross the 0dB mark for stability.

The resulting small signal model explain us that two results comes from adding the compensation capacitor C_C. First , the effective capacitance is shunting R_1 is increased by the adding some amount of approximation $g_{m2}R_2C_C$. This moves P_1 closer to the origin of complex frequency plane by a significant amount. the folowing uncompansated poles are.

$$P_1 = \frac{-1}{RC} = \frac{-1}{C_{01}(r_{04}||r_{02})}$$

Second P_2 is moved away from the origin of complex frequency plane resulting from the negative feedback reducing the output resistance of the second stage.

$$P_2 = \frac{-1}{RC} = \frac{-1}{C_L(r_{07}||r_{06})}$$

1.2 Miller compensation of two stage OTA

Therefore, in order to improve stability, we employ a variety of frequency compensation strategies. One such approach is the Miller compensation technique, which involves connecting a capacitor between stages 1 and 2.

In the Miller compensating approach, we use the pole splitting method to increase stability. This involves moving the first pole nearer the origin and the second pole away from the origin, or far away from the unity gain frequency.

The phase we need to raise has to be increased appropriately because if we increase the phase by a huge number, the system will become slow instead of producing oscillation.

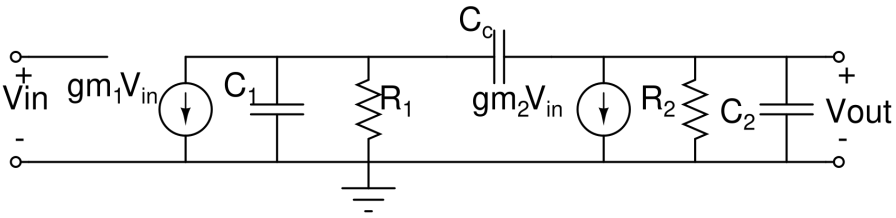

Figure 2: Small signal of Miller compensation network

For 2 poles and 1 zero we got the transfer function is

$$L(S) = -\frac{A_0(1-\frac{S}{Z_1})}{(1+\frac{S}{P_1})(1+\frac{S}{P_2})} \approx \frac{-A_0}{(1+\frac{S}{P_1})(1+\frac{S}{P_2}))} \tag{1}$$

In the above equation A_0= DC Gain and As given Zero is very far away so we can neglect Zero, so the above equation shows approximately

For calculating Phase margin(PM) which is taken as approximately 65 degree

$$PM = 180 - tan^{-1}(\frac{w_u}{w_{p1}}) - tan^{-1}(\frac{w_u}{w_{p2}} - tan^{-1}(\frac{w_u}{w_z})) \tag{2}$$

for obtaining relation between w_u and w_{p2} Pole splitting is and here $\frac{w_u}{w_{p2}}$

$$65 = 180 - 90 - tan^{-1}(\frac{w_u}{w_{p2}})$$

$$tan^{-1}(\frac{w_u}{w_{p2}}) = 25^o$$

By solving this we get

$$w_p{=}2.23w_u$$

for simulations we took phase margin to be 75^o thus obtaining a relation $w_p{=}\ 4w_u$ As zero appears so far from the w_u frequency so we assume $w_z{=}10w_u$

We know that open loop gain of the given circuit is given by $A_S * \beta = 1$

$$\frac{A_0}{1+\frac{S}{P_1}} * \frac{C_2}{C_1+C_C} = 1$$

Put $s = j\omega$ and taking mode value to neglecting negative value we get

$$\frac{A_0 P_1}{|j\omega|} * \frac{C_2}{C_1+C_2} = 1$$

Solving foe ω we got

$$\omega = A_0 \frac{C_2}{C_1+C_2} * P_1$$

Here $\frac{C_2}{C_1+C_2} = \beta$

$$\omega = (LG)$$

LG is loop gain

$$\omega = \frac{|g_{m1}(r_{02}||r_{04}) * g_{m7}(r_{06}||r_{07})| * \frac{C_2}{C_1+C_2}}{g_{m7}C_C(r_{02}||r_{04})(r_{06}||r_{07})} \tag{3}$$

So we got the bandwidth

$$BW = \omega = \frac{g_{m1}}{C_C} * \frac{C_2}{C_1 + C_2} \tag{4}$$

By intuitively for w_{p1}

$$w_{p1} = \frac{1}{A * C_c(r_{02}||r_{04})} = \frac{1}{g_{m7}(r_{06}||r_{07})(r_{02}||r_{04})} \tag{5}$$

For w_{p2} we get

$$w_{p2} = \frac{g_{m7}}{C_L} \tag{6}$$

It is seen that the zero occurs on the positive real axis of the complex frequency plane and is due to the feed-forward path through C_C the right half-plane zero is located at

$$w_{Z1} = \frac{g_{m7}}{C_C} \tag{7}$$

Putting the value of w_Z in equation 6 we get

$$\frac{g_{m7}}{C_L} = \frac{10g_{m1}}{C_C} * \frac{C_2}{C_1+C_2}$$

Here$\frac{C_2}{C_1+C_2} = 1$ so we get a relation between g_{m7} and g_{m1}

$$g_{m7} = g_{m1}$$

For $w_{p2}{=}w_u * \frac{C_2}{C_1+C_2}$

$$\frac{g_{m7}}{C_L} = \frac{4g_{m1}}{C_C} * (0.1)$$

$$C_C = 0.4C_L$$

As per the question C_L=10p

Now for calculating current at M5 and M6 with the help of slew rate

$$SR = \frac{10V}{\mu S} = \frac{I_{d5}}{C_C} = \frac{I_{d6}}{C_C+C_L+\frac{C_1C_2}{C_1+C_2}} \approx \frac{I_{d6}}{C_C+C_L}$$

Here $\frac{C_1C_2}{C_1+C_2} = \approx 0.1$

$$I_{d5} = 10^7 * 4 * 10^{-12} = 40\mu \tag{8}$$

As for the current I_{d6}

$$I_{d6} = 10^7(C_C + C_L) = 10^7(14p) = 140\mu \tag{9}$$

For finding the $\frac{W}{L}_5$ from the current I_{d5} from equation 8 we get

$$I_{d5} = \frac{\mu_n C_{ox}}{2} \frac{W}{L}_5 (V_{GS} - V_{th})^2 \tag{10}$$

$$\frac{W}{L}_5 = \frac{80}{3}$$

For finding the $\frac{W}{L}_6$ from the current I_{d6} from equation 9 we get

$$I_{d6} = \frac{\mu_n C_{ox}}{2} \frac{W}{L}_6 (V_{GS} - V_{th})^2 \tag{11}$$

$$\frac{W}{L}_6 = \frac{280}{3}$$

For other values of current

$$I_{d1} = I_{d2} = \frac{I_{d5}}{2} = 20\mu$$

By putting the value of I_{d1} and I_{d2} in current equation we get

$$I_{d1,2} = \frac{\mu_n C_{ox}}{2} \frac{W}{L}_{1,2} (V_{GS} - V_{th})^2 = \frac{40}{3} \tag{12}$$

Assuming current through M3 and M4 equal as M5 , So $I_{d3} = I_{d4} = 20\mu A$

$$I_{d3,4} = \frac{\mu_n C_{op}}{2} \frac{W}{L}_{3,4} (|V_{GS}| - |V_{th}|)^2 = \frac{80}{3} \tag{13}$$

Assuming current through M7 equal as M6 , So $I_{d7} = 20\mu A$

$$I_{d7} = \frac{\mu_n C_{op}}{2} \frac{W}{L}_7 (|V_{GS}| - |V_{th}|)^2 = \frac{560}{3} \tag{14}$$

Putting all these values of $\frac{W}{L}$in the simulation we got the values of all

2 Show all the plots required to verify the achieved specifications.

For Open Loop

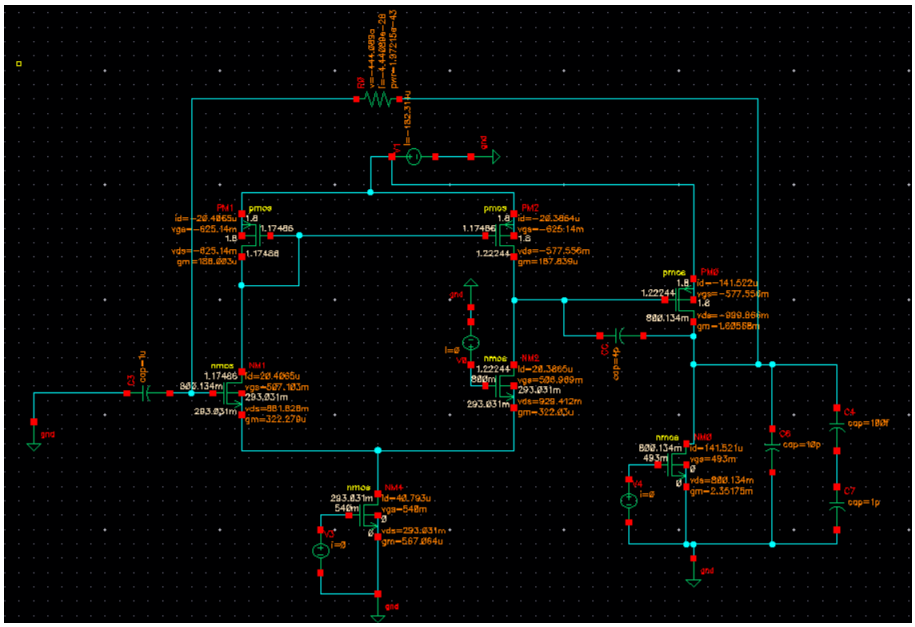

Figure 3: Open Loop circuit

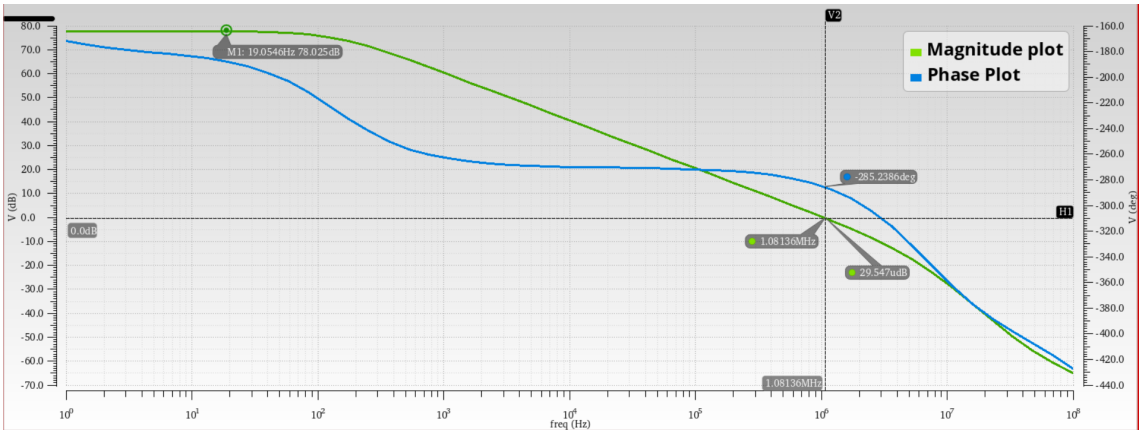

Figure 4: Phase and Magnitude plot of open loop

From plot we observe that the phase margin is obtained by 75^o which is clearly greater then 65^o so the phase margin criteria is satisfied.

From in Observation we got the $I_{d5} = 40\mu$ and $I_{d6} = 140\mu$ which we have obtained from slew rate so over Slew rate is $\frac{10V}{\mu s}$

Now for Close Loop

2.1 SLEW RATE VERIFICATION

From the DC aalysis obtained, it can be seen that I_d5 is equal to 40μA and I_d6 is equal to 141μA. From the slew rate expression,

$$Slewrate = I_{d5}/C_c = 40\mu A/4pF = 10V/\mu S \tag{15}$$

Thus slew rate is 10V/uS.

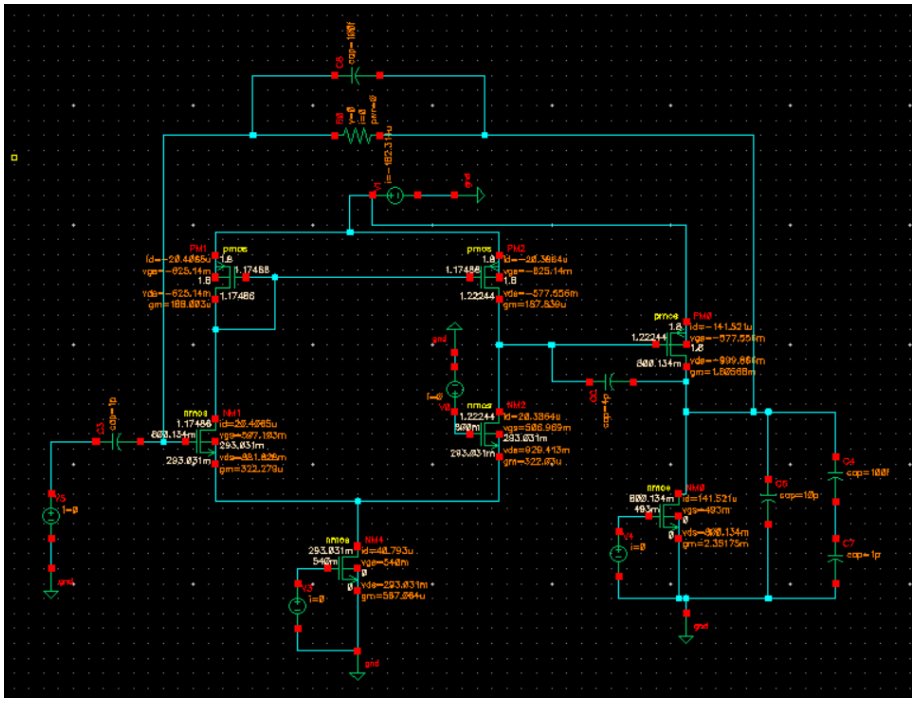

Figure 5: Close Loop Circuit

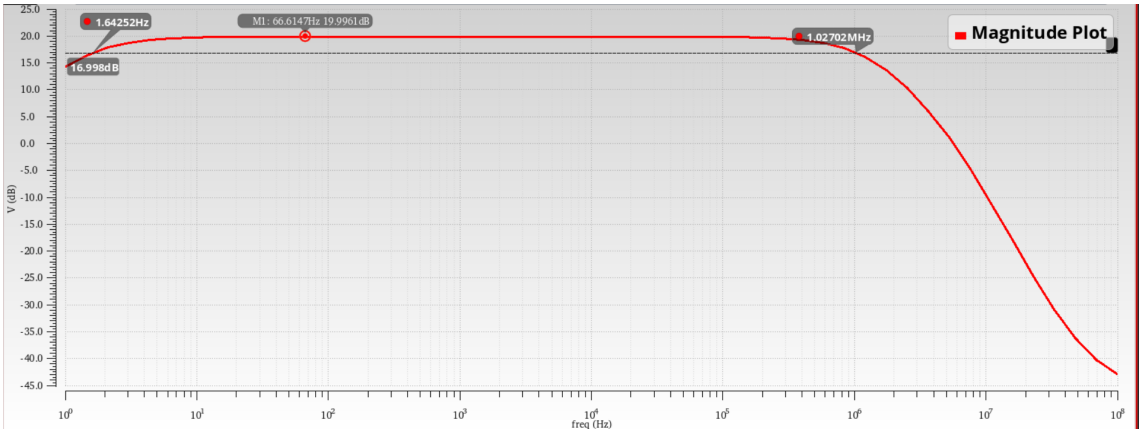

Figure 6: Magnitude plot of close loop

from the simulation we obtain the magnitude is 1.034MHz which is nearby equal to 20dB and over bandwidth 1.02MHz so it is also satisfied all the conditions. **Calculation of % gain error:**

$$A_{CL} = \frac{A}{1 + A\beta} \tag{16}$$

$$\Delta A_{CL} = \frac{-1}{\beta(1 + A\beta)} \tag{17}$$

$$\%gainerror = \frac{\Delta A}{A} * 100 = \frac{1}{A\beta} * 100 \tag{18}$$

loop gain, A*β=78.025dB=7966.177

$$\%gainerror = \frac{1}{7966.171} * 100 = 0.0125\% \tag{19}$$

NOTE : The experiment is carried out at 27^{o}C which is inside the given range.