Review and Simulation of A Low Power, Low Noise, Single-Ended to Differential TIA for Ultrasound Imaging Probes

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***Abstract*—This paper is all about the brief discussion on a low power, Low Noise Amplifier (LNA) in Cadence 0.18μm CMOS technology is for ultrasound imaging Test.This fully analyzations of the proposed circuit is for Low Noise Amplifier(LNA) is based on a Trans-Impedance Amplifier(TIA) which is Single ended to Differential Transformation is noticed by dividing the proposed circuit into two parts first part is Common Gate(CG) and the second one is Common Source(CS) based structure. The noise cancelation in the second part The CS transistor has a noise canceling technique with the help of resistive feedback. The suggested structure eliminates the noise from both the CG and CS transistors as well as the CG stage load resistor, in difference to the traditional CG-CS structure, which can only remove the noise from the CG transistor. This all feedback process helps us to reduce the power consumption in the main circuit .We get the results from this whole simulation is shown a TIA gain 50.36dB, with a f_{-3dB} bandwidth as 86.3548MHz , R_{in} is $225\Omega$and Input Referred Noise is $2.112 * 10^{-19}$ at 1KHz , the the whole power consumed in this circuit is $32.67\mu W$ from a 1.8V of V_{DD} .**

***Index Terms*—Low Noise Amplifier , Transimpedance Amplifier , The Basic CS-CG Structure (Proposed Circuit) , Common Gate(CG) , Common Source(CS) , Capacitive Feedback , Resistive Feedback, Noise Canceling , Low Power , Ultrasound Imaging Probes .**

I. Introduction

The real-time three-dimensional (3D) ultrasound imaging systems involve two-dimensional (2D) transducer arrays with a very narrow pitch in addition to a huge number of components. An picture is created by a transducer, which generates sound waves that echo off bodily tissues and create echoes. Due to its high resolution, low cost, and lack of danger to humans, ultrasound imaging is frequently used for medical imaging diagnostics. This (fig(1)) is taken from the main paper[1].

In the fig(1) of Ultrasound receiver the first component (LNA) that interfaces directly with the transducer is a Low Noise Amplifier (LNA), which plays a main role in the receiver's performance. The LNA circuit's linearity, gain, bandwidth, and noise performance are very important components. The transducer's characteristics determine the LNA design to

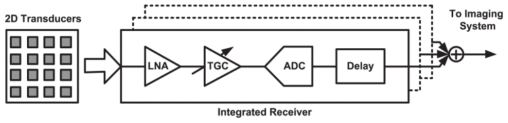

Fig. 1.

use for its many benefits, such as its larger bandwidth, more sensitivity, simplicity of integration, the Capacitive Micromachined Ultrasound Transducer (CMUT) has been present as a strong challenger to the traditional Piezoelectric transducers. A proportionate current signal is produced by the CMUT from an auditory wave. LNA based on Trans-Impedance Amplifier (TIA) are suited for CMUT applications in order to change the signals form current to voltage domain and vise-versa. Additionally, low input impedance in the CMUT readout is preferred to optimize received current and reduce undesired effects of electric and auditory coupling. Additionally, the CMUTs' output current is a single-ended signal because of the nature of electrochemical systems.

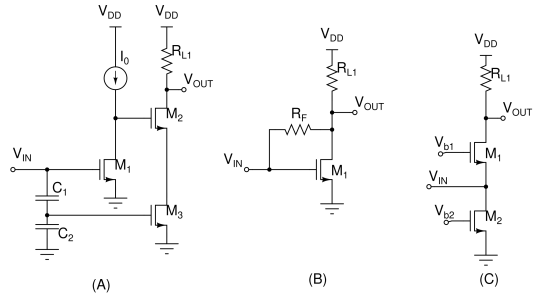

Fig. 2. Trans-Impedance Amplifier structures (A) Capacitive feedback-TIA (B) Resistive feedback TIA (C)Common Gate TIA

As seen in the above (fig(2)), there are several Transimpedance amplifier(TIA) architectures that are as three primary types but in those three the capacitive feedback tran-

simpedance amplifier (fig(2.A)) offers better noise performance than the other two shown in (fig(2)) Common Gate and resistive feedback .

Since the transistor's RF transconductance must be increased to get the required input impedance, the RF-TIA (fig.(2.B))has a high power consuming transistor for low input impedance and low noise and,

In The (fig(2.C)) Common Gate transimpedance amplifier(CG-TIA) offers better linearity, stability, and low input impedance across a large frequency range. In order to achieve low input impedance, the Common Gate transimpedance amplifier (CG-TIA) has a some high power consumption then the other two shown in (fig(2)).

From the reference[2] it states that the negative feedback in the Common Gate(CG) TIA has been improved the access of higher power consumption as compared to the other amplifer the Common gate(CG) is easier then the other two transistor but have much noiser then the others for improving this access noise we change the common gate transiotor as a single input to differential outputs which make it attractive for Capacitive Micromachined Ultrasound Transducer(CMUT). However The CS transistor's noise hasn't been eliminated in the circuit of CG-CS arrangement, but it was only possible to provide acceptable noise performance at the expense of the CS transistor's enormous transconductance and therefore high power consumption.

II. BACKGROUND

Among all the different types of structures in Transimpedance amplifier(TIA) the Common Gate(CG) amplifier is most commonly used in the 3D Ultrasound Imaging Probes because the reason behind this is Common Gate(CG) have a capability to perform a single ended to differential transformation . Form (fig.1(C)) the gain of the Input Impedance of the Common Gate(CG) is "$\frac{1}{g_{m1}}$" and the gain of the Transimpedance of the Common gate(CG) is "R_L" respectively . Now for calculating the input referred current noise by making a small signal of (fig(2.C))

first we have to calculate the current gain

$$I_{in} + g_m Z_S I_{in} + \frac{V_O + Z_S I_{in}}{r_{01}}$$

$$I_{in}(1 + g_m Z_s + \frac{Z_s}{r_{01}}) = \frac{-V_0}{r_{01}} \quad (1)$$

$$\frac{V_O + Z_S I_{in}}{r_{01}} = \frac{Z_S I_{in}}{r_{01}} + I_{out}$$

$$\frac{-V_O}{r_{01}} = \frac{Z_S I_{in}}{r_{01}} + I_{out}$$

$$V_0 = -(Z_s I_{in} + r_0 I_{out})$$

By putting the value of V_0 in equation 1 we get

$$I_{in}(1 + g_m Z_S + \frac{Z_S}{r_{01}}) = \frac{Z_S I_{in}}{r_{01}} + I_0$$

$$I_{in}(1 + g_m Z_S) = I_{out}$$

$$(1 + g_m Z_S) = \frac{I_{out}}{I_{in}}$$

From here we get current gain is

$$\frac{I_{out}}{I_{in}} = Z_S(\frac{1}{Z_S} + g_m) \quad (2)$$

By applying current division to get the noise current that flow to output node V_{op} we get,

$$\overline{I^2_{out,m1}} = \overline{I^2_{in,m1}}(\frac{Z_s}{\frac{1}{Z_s}} + Z_s)^2 \quad (3)$$

By dividing eq.3 by eq. 2 to get input noise of M_1 we get

$$= \frac{4KTgm1(g_{m1}g_{m2})}{(g_{m1}+\frac{1}{Z_S})^2}$$

So as further calculations we can get the another noise at input node as

$$= \frac{4KT(\gamma g_{m1}(\frac{1}{Z_S^2}))}{(g_{m1}+\frac{1}{Z_S})^2}$$

By solving and equation all the values we get the final input noise of the fig(2.C)we get

$$\overline{I^2_{in,n}} = 4KT\frac{\gamma g_{m1}(g_{m1} * g_{m2} + \frac{1}{Z_s^2})}{(g_{m1} + \frac{1}{Z_s})^2} + \frac{1}{R_L} \quad (4)$$

Here γ is the thermal noise coefficient and the trans-impedance of the M_i is g_{mi} and source impedance is$Z_s.g_{m1}$ must be increased in order to obtain low input impedance, which increases the bias current. However, the new CMOS technology processes have low supply voltage and a low load resistor value(R_L) is enforced by a large value of bias current, which decreases the trans-impedance gain and increases noise.

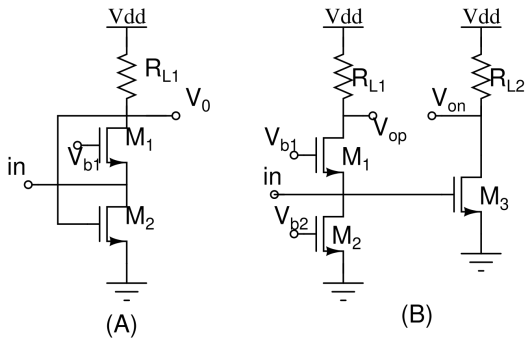

Fig. 3. (A)Model of CG feedback structure (B) Model of CG-CS

By applying -ive feedback in fig(3.A) is reduced the value of g_m because of this the trade off between g_m and input impedance is interrupted .

The input impedance is given as

$$R_{in} = \frac{1}{g_{m1}(1+g_{m2}R_L)}$$

Now, giving the transimpedance gain as

$$Z_{TIA} = \frac{R_L}{1+g_{m2}R_L}$$

and

The input reference noise is given as

$$\overline{I^2_{in,n}} = 4KT\frac{(1+g_{m2}R_L)^2}{(g_{m1}(1+g_{m2}R_L)+\frac{1}{Z_S})^2}$$

$$(\gamma g_{m1}(g_{m1}g_{m2} + \frac{1}{Z_S^2}) + \frac{(g_{m1}+\frac{1}{Z_S})^2}{R_L})$$

As per standard the power taken by the Common Gate(CG) is reducing because of decreasing the value of g_{m1} and the bias current and due to which load resistance will be increased .

In the fig(3.B) it is demonstrate that the common gate and common source have a capability to convert single input to the differential output.The noise of the Common Gate(CG) transistor may be cancelled by using this arrangement, which is referred as a noise canceling system.

The gain of the main circuit shown in fig.4 is for the common gate gain=$g_m R_D(1+\eta)$ and here $\eta = \frac{g_{mb}}{g_m}$ and the gain of the common source is $= -g_m R_D$.

III. DESIGN METHODOLOGY OF THE PROPOSED CIRCUIT

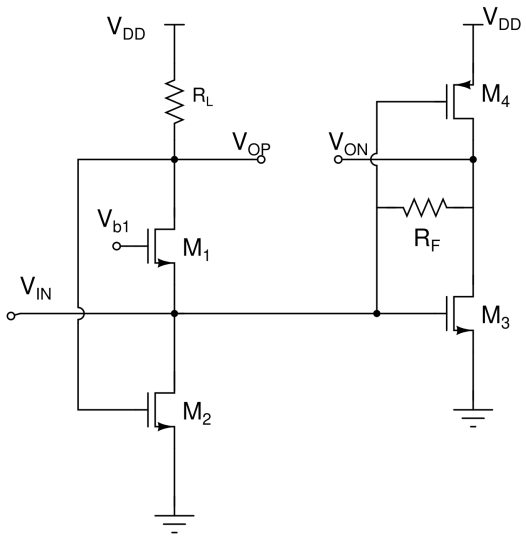

Fig. 4. Model of the Main Circuit

A. *Main Idea*

The primary objective is to enhance the noise performance of the Common Gate(CG) and Common Source(CS) structures through a specific technique while maintaining its power consumption. The basic concept behind this is to introducing a noise cancellation path to the Common Source(CS) stage without adding the other stages in the circuit. In the fig.2 of proposed circuit shows a additional feedback resistor is taken in Common Source(CS) stage.

This new approach is not only for eliminating noise generated by the Common Gate(CG) transistor but also for canceling out noise from the Common Source(CS) transistor at the differential outputs which is effected by R_F. For further reduction in power consumption we are using the negative feedback technology in the Common Gate(CG) stage.

B. *Input Impedance*

In this proposed circuit we seen that the whole circuit is build up on two different types of circuit Common Gate (CG) and Common Source (CS) and both types are connected in parallel so we calculated the Input Impedance one by one Consider the equivalent circuit of a simple small signal, which includes $\lambda = 0$ **and** $\gamma = 0$.

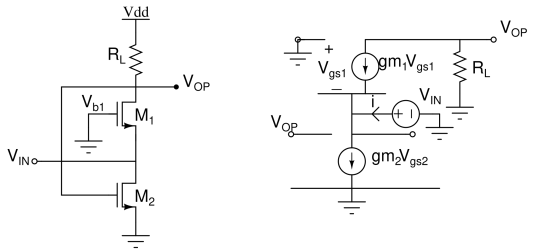

Fig. 5. Schematic of common gate Circuit and the small signal of common gate circuit

First take Common Gate(CG) for calculating the Input Impedance .

$$-I + g_{m2}V_{gs2} - g_{m1}V_{gs1} = 0$$

HERE

$V_{gs1} = -V_{in}$ and $V_{gs2} = V_0$

$$-I + g_{m2}V_0 - g_{m1}(-V_{in}) = 0$$
$$-I + g_{m2}V_0 + g_{m1}V_{in} = 0$$
$$\frac{V_0}{R_L} = -g_{m1} * V_{gs1}$$
$$V_0 = -R_L(g_{m1} * V_{gs1})$$

Putting this value in above equation we got;

$$I = g_{m2}(-R_L(g_{m1} * V_{gs1})) + g_{m1}V_{in}$$

here$V_{gs1} = V_{in}$

$$I = g_{m1}(1 + g_{m2*R_L})V_{in}$$

So, we got

$$\frac{V_{in}}{I} = \frac{1}{g_{m1}(1+g_{m2}*R_L)} = R_a$$

Now we solve the Common Source(CS) part of the proposed circuit.

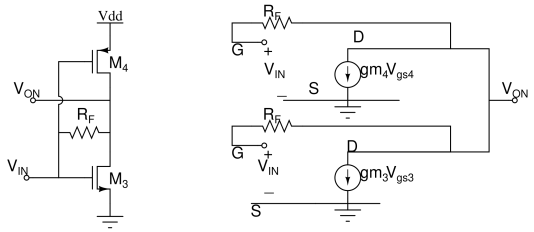

Fig. 6. Model of common source circuit and the small signal of common source circuit

$$-I + g_{m4} * V_{gs4} + g_{m3} * V_{gs3} = 0$$
$$-I + g_{m4} * V_{in} + g_{m3} * V_{in} = 0$$
$$\frac{V_{in}}{I} = \frac{1}{g_{m3}+g_{m4}} = R_b$$

Here

$$R = R_a || R_b$$

So, finally the input impedance is

$$R_{in} = \frac{1}{g_{m1}(1 + g_{m2} * R_L) + g_{m3} + g_{m4}} \tag{5}$$

But if we include channel length modulation and body effect then $\lambda \neq 0$**and** $\gamma \neq 0$

$$R_{in}^{-1} = (g_{m1} + g_{mb1} + \frac{1}{r_{01}})(1 + (g_{m2} - \frac{1}{r_{01}}) * (R_L || r_{01}) + \frac{1}{r_{02}} + (g_{m3} + g_{m4} - \frac{1}{r_{03}} - \frac{1}{r_{04}}) \frac{1}{(1 + R_F(\frac{1}{r_{03}} + \frac{1}{r_{04}}))} \tag{6}$$

From the above equation(5) of input impedance is compared to the fundamental CG-CS structure that needed g_m value for the Common Gate(CG) transistor is reduced. In real the g_m of the tail transistor M_5 adds to the input impedance through with the help of negative feedback, in addition to the g_m of the CG transistor. Additionally, the final two components are added to the denominator in (5) by the feedback resistor in the Common Source stage, which supports in the decreasing value of the input impedance. Smaller values of g_{m1} can be used to obtain low input impedance, which results in decreasing of power usage by the whole circuit. It's important to note that the current source transistor in the denominator realizes the coefficient $(1 + g_m R_L)$ without the need of any extra components, which lowers the circuit's power and noise.

C. *Gain and Bandwidth*

The gain of the Common Source(CS) and Common Gate(CG) stages must be equivalent but opposite in sign in order to execute single-ended to differential conversion. The following equations are used to calculate each branch's gain.

First we have to calculate the gain of the Common Gate(CG) stage;

For calculating $\frac{V_{OP}}{I_{IN}}$

$$\frac{V_{OP}}{R_L} = -g_{m1} * (V_{gs})$$

Here $V_{gs} = -V_{in}$

$$\frac{V_{OP}}{R_L} = g_{m1} * V_{in}$$

So,

$$V_{OP} = g_{m1} * V_{in} * R_L$$

but we calculated that $\frac{V_{in}}{I_{in}} = R_{in}$

So, from there $V_{in} = I_{in} * R_{in}$

then we got;

$$V_{OP} = g_{m1} * R_L * I_{in} * R_{in}$$

$$\frac{V_{OP}}{I_{in}} = g_{m1} * R_L * R_{in} \tag{7}$$

By taking $\lambda \neq 0$ and $\gamma \neq 0$ then we got

$$\frac{V_{OP}}{I_{in}} = (g_{m1} + g_{mb1} + \frac{1}{r_{01}}) * (R_L || r_{01}) * R_{in} \tag{8}$$

Now for calculate the gain of the Common Source(CS) stage;

For calculating $\frac{V_{ON}}{I_{IN}}$

$$\frac{V_{in} - V_{on}}{R_F} = g_{m4} V_{in} + g_{m3} V_{in}$$

$$\frac{V_{on}}{R_F} = \frac{V_{in}}{R_F} - (g_{m3} V_{in} + g_{m4} V_{in})$$

$$\frac{V_{on}}{I_{in}} = -V_{in}(-\frac{1}{R_F} + g_{m3} + g_{m4})$$

$$\frac{V_{ON}}{I_{in}} = (g_{m3} + g_{m4} - \frac{1}{R_F}) * R_F * R_{in} \tag{9}$$

By taking $\lambda \neq 0$ and $\gamma \neq 0$ then we got

$$\frac{V_{ON}}{I_{in}} = (g_{m3} + g_{m4} - \frac{1}{R_F}) * (R_F || \frac{1}{r_{03}} || \frac{1}{r_{04}} * R_{in} \tag{10}$$

Gain imbalance is defined as the voltage gain ratio between the Common Source(CS) and Common Gate(CG) stages when the $\lambda \neq 0$ and $\gamma \neq 0$

$$\Delta A_v = 20log(\frac{\frac{V_{OP}}{I_{in}}}{\frac{V_{ON}}{I_{in}}})$$

After putting the values form equation 5 and 7 we get;

$$\Delta A_v = 20log(\frac{(g_{m1} + g_{mb1} + \frac{1}{r_{01}}) * (R_L || r_{01}) * R_{in}}{(g_{m3} + g_{m4} - \frac{1}{R_F}) * (R_F || \frac{1}{r_{03}} || \frac{1}{r_{04}} * R_{in}}) \tag{11}$$

The Trans-impedance of the proposed circuit is given by

$$Z_{TIA} = \frac{V_{OP} + V_{ON}}{I_{in}}$$

After putting the values of $\frac{V_{OP}}{I_{in}}$ and $\frac{V_{ON}}{I_{in}}$ form equation 5 and 7 we get;

$$Z_{TIA} = (g_{m1} + g_{mb1} + \frac{1}{r_{01}})(R_L || r_{01}) * R_{in}$$

$$+ (g_{m3} + g_{m4} - \frac{1}{R_F}) * (R_F || \frac{1}{r_{03}} || \frac{1}{r_{04}} * R_{in} \tag{12}$$

As per equation 11 the value of r_0 is reducing the gain which can be transformed by neglecting the value of $\frac{1}{r_0}$ which is much much greater then the value of R_L and R_F . By assuming the $\gamma = 0$ and $\lambda = 0$ in equation 11 we got the gain as

$$Z_{TIA} = 2 g_{m1} R_L R_{in} \tag{13}$$

In the main circuit the output node is taken as to calculate the f_{-3dB} bandwidth which is examine by using the dominant pole by taking a roughly guess in the design at output node.

$$f_{-3dB} = \frac{1}{2\pi(R_L || R_F || \frac{1}{r_{01}} || \frac{1}{r_{03}} || \frac{1}{r_{04}})(C_L || C_P)} \tag{14}$$

Here

Paracitic capacitance C_P is at output node.

and

Paracitic capacitance C_L is at receiver side

In conclusion, this topology is quite capable of maintaining a reasonable gain and bandwidth with the right circuit design.

D. Noise Analysis

The noise cancellation plan for the suggested circuit's resistor Resistive Load R_L, transistors M1, M3, and M4 is shown in Fig. 7(a).The Fig. 7(a) illustrates how the noise current of M1 produces noise voltages at its source and drain positive output voltage(V_{op}) terminals that are out of phase yet correlated.

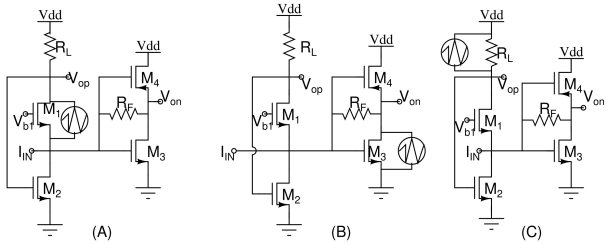

Fig. 7. Noise Circuits

An out phase noise voltage at negative output voltage(V_{on}) is the consequence of the Common Source(CS) stage amplifying the noise voltage at the source terminal. The circuit therefore eliminates the noise from M1 as common mode noise.

Transfer function of M1 has to be calculated as

$$T_{i,M1} = \frac{V_{OP}-V_{ON}}{I_{n,M1}}$$

$$T_{i,M1} = (R_{in}||Z_s)R_L(g_{m1}(1+g_{m2}R_L)-(g_{m3}+g_{m4})-\frac{1}{Z_s}) \quad (15)$$

On the other hand, the noise current of M3,4 produces correlated and in phase noise voltages at their gate terminal and drain negative output voltage(V_{on}) with the help of R_F. The Common Gate(CG) stage amplifies the noise that is communicated to the gate terminal, creating a noise voltage in the positive output voltage(V_{op}) that is in phase with the noise generated at negative output voltage(V_{on}) (Fig. 7(b)).As a result, M3,4 noise can be cancelled as a common mode noise. Because of the negative feedback and the Common Source(CS) stage.

Transfer function of M3 and M4 is

$$T_{i,M3,4} = \frac{V_{OP}-V_{ON}}{I_{n,M3,4}}$$

$$T_{i,M3,4} = R_F - 2g_{m1}R_L(R_{in}||Z_s) \quad (16)$$

The noise of load resistance(R_L) is also cancelled. The voltage noise produced by load resistance(R_L) at the positive output voltage(V_{op}) is amplified by M2, and an out-of-phase noise is produced at the source of M1, as seen in Fig. 7(c). As such, it is cancelled, much like the M1 noise.

Transfer function of R_L is

$$T_{i,R_L} = \frac{V_{OP}-V_{ON}}{I_{n,R_L}}$$

$$T_{i,R_L} = (R_{in}||Z_s)R_L(g_{m1}(g_{m2}R_L-1)-(g_{m3}+g_{m4})-\frac{1}{Z_s}) \quad (17)$$

Here Equation 15,16 and 17 support the noise-cancelling design of the main circuit.

The reduced small signal equal circuit is taken into consideration in order to examine the noise performance. Phase and amplitude errors the two pathways are caused by the r_o of parasitic capacitors and transistors, which results in insufficient noise canceling. Even so, they are ignored in the quest for improved intuition because of their small values. The noise transfer function (Ti) is computed taking into account zero gain imbalance .

Transfer function of M2

$$T_{i,M2} = \frac{V_{OP}-V_{ON}}{I_{n,M2}}$$

$$T_{i,M2} = 2g_{m1}R_L(R_{in}||Z_s) \quad (18)$$

Transfer function of R_F

$$T_{i,R_F} = \frac{V_{OP}-V_{ON}}{I_{n,R_F}} = R_F \quad (19)$$

Here R_i represents the thermal noise of the resistors and $I_{n,Mi}$ represents the thermal noise and flicker noises of Mi.

IV. Circuit Analysis and Results and Conclusions

This main circuit fig(4) of LNA is made and simulated in the 180 nm CMOS technology in the Cadence . In this whole circuit the circuit is mainly divided into two parts first is in Common Gate which neglected all the noise from it and second is of common source which neglected the noise from it.

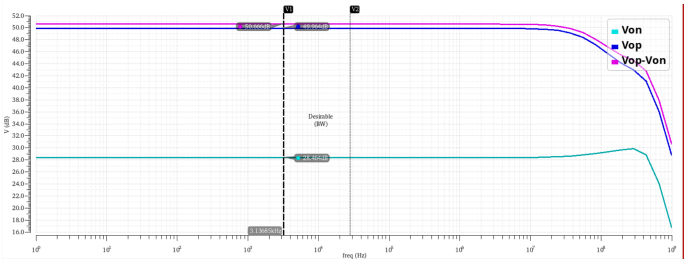

Fig. 8. Gain Plot of the main circuit

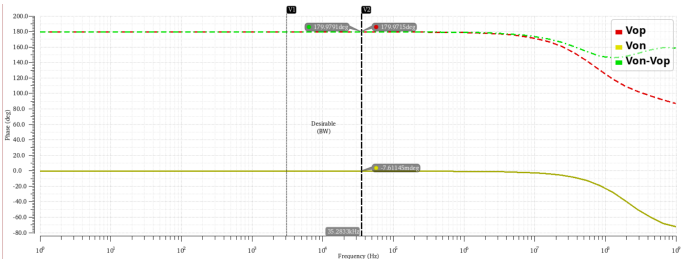

Fig. 9. Phase vs. Frequency Plot

The designed value of the main circuit is shown in Table 1 in the sizing of transistor we noticed that if we increase the value of length of transistor the flicker noise is increased and

Device	$M_1(W/L)$	$M_2(W/L)$	$M_3(W/L)$	$M_4(W/L)$	R_L	R_F
Values	20	2.8	25	10	30K	100K

TABLE I
THE PREDICTED DEVICE VALUES OF PROPOSED CIRCUIT

if we reduced the value of length of transistor it decrease the parasitic capacitance and increase the bandwidth of the circuit . The whole TIA consumes the 132.64μW from a 1.8V of V_{DD} .

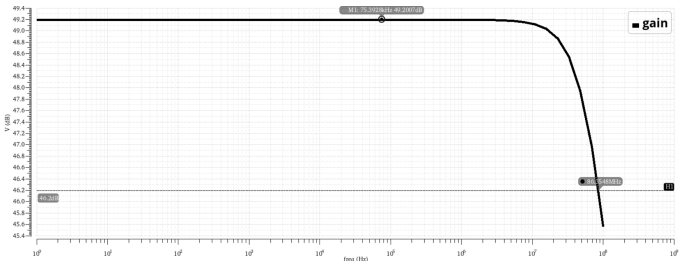

Fig. 10. f_{-3dB} Plot

Device	NM1	NM2	NM3	PM4
Noise Summery	5.8796*10^{-11}	2.782*10^{-11}	8.029*10^{-11}	2.764*10^{-12}

TABLE II
NOISE SUMMERY OF THE MAIN CIRCUIT

In the fig 10 the f_{-3dB} is at 86.3586MHz at the gain of 46.2dB . after this the Total noise summery is calculated is $2.1677 * 10^{-10}$ and the Input referred noise is $2.1120 * 10^{-19}$

Noise Parameters	NM1	NM2	NM3	PM4
f_n	58.796*10^{-12}	27.82*10^{-12}	80.29*10^{-12}	2.764*10^{-12}
i_d	76.89*10^{-15}	1.76*10^{-15}	16.89*10^{-15}	4.947*10^{-15}
r_d	14.393*10^{-21}	24.44*10^{-24}	37.25^{-24}	52.806*10^{-24}
r_s	6.848*10^{-18}	0.558*10^{-18}	3.910*10^{-18}	0.5607*10^{-18}
Total	58.873*10^{-12}	27.822*10^{-12}	80.308*10^{-12}	2.764*10^{-12}

TABLE III
NOISE PARAMETERS OF THE MAIN CIRCUIT

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