Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator

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***Abstract*—The Requirement for the Ultra Low-Power , Area efficient and High integrated and programmable analog-to-digital converter(ADCs) it sill pushing towards the dynamic comparators to maximize speed of the power efficiency.This research will provide an examination of the dynamic comparators , delay and produce analytical expressions.Through the use of analytical expressions, designers examine the trade-off in dynamic comparator design and get an intuitive understanding of the primary factors contributing to comparator delay. The circuit of a double-tail dynamic comparator is adjusted for low-power and quick operation even at low supply voltages in order to create a new dynamic comparator that is suggested based on the analysis that has been given.By adding some few transistors , we get the positive feedback through when regeneration is strengthened this gives a reduction in delay time . The simulation is done in 180nm CMOS technology and we noticed that in the proposed circuit the delay is reducing by reducing the supply voltage but mainly we use supply voltage is 0.8V .**

***Index Terms*—Double-tail comparator, High-speed ADC, Low-power analog design , Dynamic comparator .**

I. INTRODUCTION

In analog to digital Convertor (ADC) the comparator is one of the main building block in the circuit , mostly circuits requires to have a high performance , less delay , less area , less power dissipation types circuits with a less power supply . But there is a big chalange to make a high performance comparator in a smaller in supply voltage and in other words in a 180nm CMOS technology it is difficult to achieve a high speed because of large size of transistor is used in the circuit which helps to compensate the supply voltage so it needed more area and power . excluding these things some circuits work on low voltage for a limiting common mode input range which is needed mostly in high speed ADC circuits . There are many types of methods to solve this from that one is the Supply boosting Method its helps to solve input-range and switching issues, two methods called ”boost” and ”bootstrapping” are based on increasing the supply, reference, or clock voltage. Even though these methods are efficient, they have problems with dependability, particularly with UDSM CMOS technology. The body-driven MOSFET, which Blalock used, functions as a depletion-type device by eliminating the threshold voltage need.

Apart from this this paper is explaining about the types of comperators ,analysis of comparators in different types of designs like double tail comparator and new comparators which does not wants boosted voltages . In this we seen that by adding some small area transistor we neglect a large amount of delay in the circuits due to which we also save some power disipation in the circuit . In conventional clocked regenerative comparators we discussed all the parameters using in it presence of delay, numerical methods to calculate the delays of the comparators and the other one in proposed double tail comparator and then we discussed about the design problems and at the end we calculate some parameters and make a table to compare all the things which we have done in this paper.

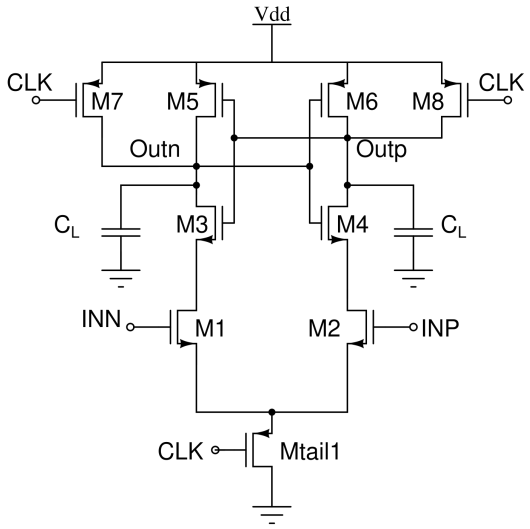

Fig. 1. Figure of the Conventional Dynamic Comparator

II. CLOCKED REGENERATIVE COMPARATORS

This type of comparators are widely used in the ADCs because they have positive feedback system which helps in

to give fast results or take fast decision , in this paper we perform this comparator to see from different aspects such as delay , offset , noise and random decision error .

A. *Conventional Dynamic Comparator*

The Conventional Dynamic Comparator is mostely used in Anlog to Digital converters which have high input impedance with rail-to-rail output swing and it don't have any static power consumption . Therer are a two phases in a comparator one is Reset Phase and second one in Comparision Phase .

In Reset Phase the Clock is low and Clock bar is high and M_{tail} is low means OFF when the Comparator is in reset phase then the MOS (M7 and M8) is on and it charges the output node (Out_n and Out_p) to V_{DD} .

In Comparision Phase when the Clock is high CLK=V_{DD} then the MOS (M7 and M8) is off and M_{tail} is ON and the Output Voltage Nodes (Out_p, Out_n) which get pre-charged to V_{DD} .

In this circuit we assume the positive input is greater then the negative input so due to this positive output discharge faster then the negative output here charge at positive output node will discharge through the M2 transistor and it will discharges till V_{th} and the other side the negative output node will discharges through the M1 transistor .

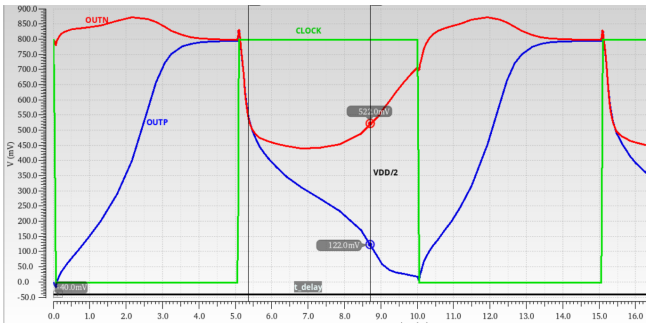

Fig. 2. Output of the Conventional Dynamic Comparator for $V_{cm} = 0.7V$ and $V_{DD} = 0.8V$

TABLE I
OUTPUTS OF FIGURE 1

Item	Value
Technology	180 nm CMOS
Supply Voltage	0.8V
Average power dissipation	$60.2\mu W$
Worst case delay (V_{cm} = 0.7V , ΔV_{in} = 1 mV)	309.7 ps
Delay/log(ΔV_{in})	77.425 ps/dec

Here me take the transistor size is approximate same and the tail transistor have a larger value then the others and the $V_{DD} = 0.8V$ and is equal to (CLK=0.8V) and the parameters of M_{tail1} is equal to 3μ

From the above result of conventional dynamic comparator we get a delay is 3.097ps and the power disipate by this schematic (fig.1) is $6.2\mu W$

Thus the Discharge Delay (t_0) is given by

$$t_0 = \frac{C_L|V_{thp}|}{I_2} \approx 2\frac{C_L|V_{thp}|}{I_{tail}} \quad (1)$$

In equation 1 we consedering that ,

$$I_2 = \frac{I_{tail}}{2} + \Delta V_{in}$$

$$I_2 = \frac{I_{tail}}{2} + gm_{1,2} \times \Delta V_{in}$$

From this we noticed that for the small difference input (ΔV_{in}) , I_2 is approx. continious and equal to the half of tail current (I_{tail})

In this case the delay t_{latch} which is taken from the two cross-coupled inverters which is (M7-M9) and (M8-M10) and in this we assumed that a voltage swing between the output nodes (Out_n and Out_p) is ,

$$\Delta V_{out} = \frac{V_{DD}}{2}$$

it is taken from the initial voltage difference ΔV_0 at the drop down output and the latch delay time is calculated to go to V_{out} for cros-coupled inverter.

$$\Delta V_{out} = \Delta V_0 e^{\frac{A_v - 1}{t_0} t_{latch}}$$

$$\frac{\Delta V_{out}}{\Delta V_0} = e^{\frac{A_v - 1}{t_0} t_{latch}}$$

$$ln(\frac{\Delta V_{out}}{\Delta V_0}) = \frac{A_v - 1}{t_0} t_{latch}$$

$$t_{latch} = \frac{A_v - 1}{t_0} ln(\frac{\Delta V_{out}}{\Delta V_0})$$

Here A_v is much much greater then 1 so we neglect them and A_v is equal to $R_L C_L$ and t_0 is $g_{m,eff} R_L$ so ,

$$t_{latch} = \frac{C_L}{g_{m,eff}} \times ln(\frac{\Delta V_{out}}{\Delta V_0}) = \frac{C_L}{g_{m,eff}} \times ln(\frac{\frac{V_{DD}}{2}}{\Delta V_0}) \quad (2)$$

Here;

$g_{m,eff}$ = The effective transconductance of back to back inverter and it will increase as when the power will be increased

and this t_{latch} delay basically depends upon the previous output voltage difference which is noted down from the first simulation when ($t = t_0$).

According to the (eq. 1) now ΔV_0 is calculated as .

$$\Delta V_0 = |V_{outp}(t = t_0) - V_{outn}(t = t_0)|$$

$$\Delta V_0 = |V_{thp}| - \frac{I_2 t_0}{C_L} = |V_{thp}|(1 - \frac{I_2}{I_1}) \quad (3)$$

We noticed that the current I_1 and I_2 are approximate near to each other so the difference between the current I_1 and I_2 so ,

$$\Delta I_{in} = I_1 - I_2$$

from this I_1 is approximated equal by the current $I_{tail}/2$ so the (equation.3) can be modified as

$$\Delta V_0 = |V_{thp}| \frac{\Delta I_{in}}{I_1}$$

$$\Delta V_0 \approx 2|V_{thp}| \frac{\Delta I_{in}}{I_{tail}}$$

$$= 2|V_{thp}|\frac{\sqrt{\beta_{1,2}I_{tail}}}{I_{tail}}\Delta V_{in}$$

$$\Delta V_0 = 2|V_{thp}|\sqrt{\frac{\beta_{1,2}}{I_{tail}}}\Delta V_{in} \quad (4)$$

In the above equation $\beta = \mu_n C_{ox}$ of the transistor M1 and M2 which is input transistor and having the current factor I_{tail} this is a common-mode supply voltage (V_{cm}) . For calculating the delay for conventional dynamic comparator we put the equation .4 in this and take t_0 as we calculated above,

$$\tau_{delay} = t_0 + t_{latch}$$

$$\tau_{delay} = \frac{C_L|V_{thp}|}{I_2} + \frac{C_L}{g_{m,eff}} ln(\frac{\Delta V_{out}}{\Delta V_0})$$

$$\tau_{delay} = 2\frac{C_L|V_{thp}|}{I_2} + \frac{C_L}{g_{m,eff}} ln(\frac{\frac{\Delta V_{DD}}{2}}{\Delta V_0})$$

$$\tau_{delay} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} ln(\frac{\Delta V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}) \quad (5)$$

The above equation effect the different parameters like

$$\tau_{total} \ \alpha \ \frac{C_L}{\Delta V_{in}}$$

and delay is also change with the V_{cm}

$$t_0 \ \alpha \ V_{cm}$$

From this expression we identified that by small change in input voltage V_{cm} by bias current I_{tail} changes at M_{tail} .

In the structure of conventional double-tail dynamic comparator has an advantages like high I/P impedance having rail to rail O/P swing don't have any static power consumption and having a large validity for mismatch and noise . To minimizing the offset we have to take large input transistor and the parasitic capacitors of the input transistors dose not effects the switching speed and in charging and discharging .

The main disadvantage of the (fig.3) in this structure they have only one current path through the tail transistor M_{tail} this current path has for both differential as well as the cross coupled inverters . While a modest tail current is desired to maintain the differential pair in weak inversion, produce a long integration interval, and improve the $\frac{G_m}{I}$ ratio and the tail current would be ideal to allow for quick latch regeneration. Furthermore, since M_{tail} mostly functions in the triode region but regeneration is not facilitated by the tail current's dependence on the V_{cm}.

TABLE II
OUTPUTS OF FIGURE 1

Item	Value
Technology	180 nm CMOS
Supply Voltage	0.8V
Average power dissipation	78.9μW
Worst case delay (V_{cm} = 0.7V , ΔV_{in} = 1 mV)	472.58 ps
Delay/log(ΔV_{in})	118.145 ps/dec

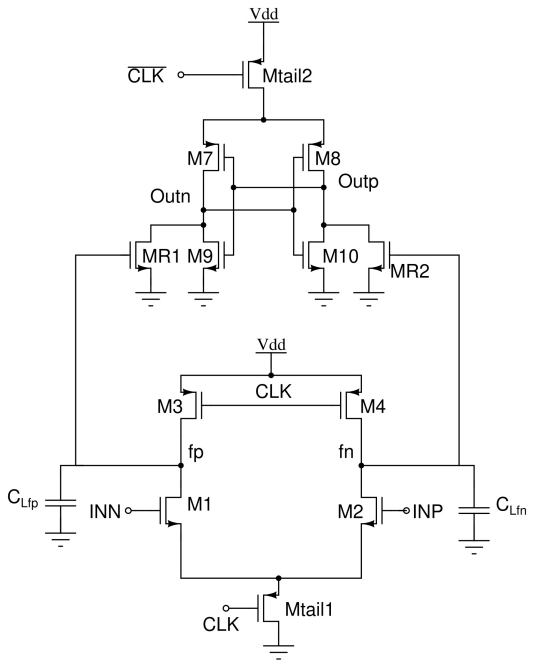

Fig. 3. Figure of Conventional Double-tail Dynamic Comparator

B. Conventional Double-Tail Dynamic Comparator

In this Conventional double-tail Comparator which is shown in (fig3) we comparing the supply voltage in this architecture to the traditional dynamic comparator, it can function at lower supply voltages since there is less pile-up as compaired to the traditional dynamic comparator. The double tail technique is used for giving the larger current in latching stage and have a widening of M_{tail2} and its helps in fast latching as well as getting small current in M_{tail1} .

The **Operation** of this conventional double-tail dynamic comparator is follows in two different phases first in reset phase the CLK is equal to 0 so the both the tail M_{tail1} and M_{tail2} both are off . When the CLK is off due to which the Pmos M3 and M4 has pre-charged the node fn and fp till V_{DD} due to which the transistor M_{R1} and M_{R2} is on which drains out the voltage at output node to the ground . In another case when CLK is equal to V_{DD} so now both the tail turns on M_{tail1} and M_{tail2} and both the pmos M3 and M4 will off now so the voltage stored at node fn and fp will start draining out with the rate off M_{tail1}/C_{Lfn} and in the upper part of circuit the transistor M_{R1} and M_{R2} helps to passes the voltage $\Delta V_{fn,fp}$ to the cross-coupled inverters which helps to cancel out the kickback noise . So as compaired to the conventional dynamic comparator the delay was reduced by to many things like due to t_0 and t_{latch}

$$t_0 = \frac{C_{Lout}V_{thn}}{I_{B1}} \approx 2\frac{C_{Lout}V_{thn}}{I_{tail2}} \quad (6)$$

Here the delay t_0 appears for the capacitance of the capacitive charge C_{Lout} and C_{Lout} is C_{Lfp} and C_{Lfn} .

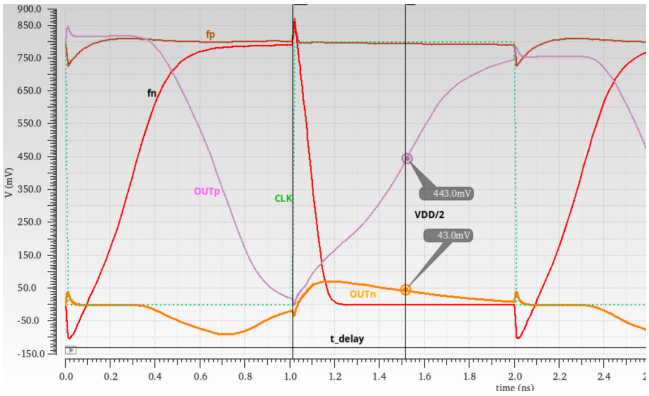

Fig. 4. Output of Conventional Double-tail Dynamic Comparator for ΔV_{in} = 5 mV , $V_{cm} = 0.7V$ and $V_{DD} = 0.8V$

After the latch transistor (M9) will turns on then the charge stored at the output node Out_n will discharges through ground this leads the other transistor (M8) which starts charging the positive output node Out_p till V_{DD} . Now at time t_0 we calculating the voltage difference ΔV_0 for this we have

$$\Delta V_0 = |V_{outp}(t = t_0) - V_{outn}(t = t_0)| = V_{thn} - \frac{I_{B2}t_0}{C_{Lout}}$$

$$\Delta V_0 = V_{thn}(1 - \frac{I_{B2}}{I_{B1}}) \tag{7}$$

Here the current I_{B1} and I_{B2} is from the right of left branch of the second stage of the comparator , now considere

$$\Delta I_{latch} = |I_{B1} - I_{B2}| = g_{mR1,2}\Delta V_{fn/fp}$$

this (eq. 7) can be rewrite as

$$\Delta V_0 = \frac{V_{thn}\Delta I_{latch}}{I_{B1}}$$

$$\Delta V_0 = \frac{2V_{thn}\Delta I_{latch}}{I_{tail2}}$$

$$\Delta V_0 = \frac{2V_{thn} \times g_m R_{1,2}}{I_{tail2}} \times \frac{\Delta V_{fn}}{\Delta V_{fp}} \tag{8}$$

The difference the voltage across the nodes fn and fp ($\Delta V_{fn/fp}$) at time t_0 . This fn and fp are the two main parameters which effect the input as well as output voltage difference due to which both the stages the intermediate stage when the clock is high and the second stge when the clock is low they both having different output voltage difference and effect the node voltage fn and fp.

$$\Delta V_{fn/fp} = |V_{fn}(t = t_0) - V_{fp}(t = t_0)|$$

$$\Delta V_{fn/fp} = \frac{t_0(I_{N1} - I_{N2})}{C_{L,fn,fp}}$$

$$\Delta V_{fn/fp} = \frac{t_0(g_{m1,2} \times \Delta V_{in})}{C_{L,fn,fp}} \tag{9}$$

Here the current I_{N1} and I_{N2} is the input MOS M1 and M2 current which is fully depend on the input voltage $\Delta I_N = g_{m1,2} \times \Delta V_{in}$.

So, by putting the above equation 9 in the equation 8 we will get

$$\Delta V_0 = \frac{2V_{thn} \times gm_{R1,2}}{I_{tail2}}\Delta V_{in}$$

$$\Delta V_0 = (\frac{2V_{thn}}{I_{tail2}})^2 \times \frac{C_{Lout}}{C_{L,fn,fp}} \times g_{mR1,2} \times g_{m1,2} \times \Delta V_{in} \tag{10}$$

For finding the τ_{delay} for the double tail conventional dynamic comparator we have to put the ΔV_0 in the τ_{delay} equation which we have calculated in the conventional dynamic comparator , so we get ,

$$\tau_{delay} = t_0 + t_{latch}$$

$$\tau_{delay} = 2\frac{C_L V_{thn}}{I_{tail2}} + \frac{C_L}{g_{m,eff}} ln(\frac{\frac{\Delta V_{DD}}{2}}{\Delta V_0})$$

$$\tau_{delay} = 2\frac{C_L V_{thn}}{I_{tail2}} + \frac{C_L}{g_{m,eff}} \times$$

$$ln(\frac{V_{DD} \times I_{tail2}^2 \times C_{L,fn,fp}}{8V_{thn}^2 \times C_{Lout} \times g_{mR1,2} \times g_{m1,2}\Delta V_{in}}) \tag{11}$$

NOTE : In this double tail conventional dynamic comparator we noticed that the intermediate transistor will be in the cut-off region when both the nodes fn and fp will discharge through ground hence both the transistor dose not play a significant role to improve the effective trans-conductance of the latch and in the other case when it is in reset phase both the nodes fn and fp will charge from ground to V_{DD} in needs some power to charge these points till V_{DD} all these parameters describe how the propose double tail comperator works and improved the performance from the other comparators.

III. Proposed Double-Tail Dynamic Comparator

The proposed double-tail dynamic comparator is shown in (fig 5) and in (fig 6). The double-tail comaprator is made to give a better outputs in the low voltage applied the (fig 5) is to increase the $\Delta V fn/fp$ with respect to the speed of latch regeneration and in (fig 6) both the PMOS M_{c1} and M_{c2} is denote as control transistor which is placed in parallel with the transistor M3 ans the transistor M4 but in the cross-coupled situation.

A. *Operation of the Proposed Comparator*

The operation of a conventional double-tail dynamic comparator is done as ,

During this reset phase the clock is low due to which $M_{tail1,2}$ is off and it helps M3 and M4 to charge the node fn and fp thill V_{DD} and the transistor $M_{c1,c2}$ are off .

In other phase when CLK is high means equal to V_{DD} so due to this now $M_{tail1,2}$ is on now and the transistor M3 and M4 will turns off . Both the nodes fn and fp drains at the potential as per the input voltage is applied at the transistor M1 and M2 . First assume the case when input supply Vin_p is greater then Vin_n in this case the node charge fn drop faster then the node fp because M2 provides more current supply then the transistor M1 as the node voltage fn fall down in a constant speed at some instance the transistor M_{c1} turns on and the node fn to discharge and it recharge the node fp till V_{DD} and the other transistor M_{c2} will remain off till the node

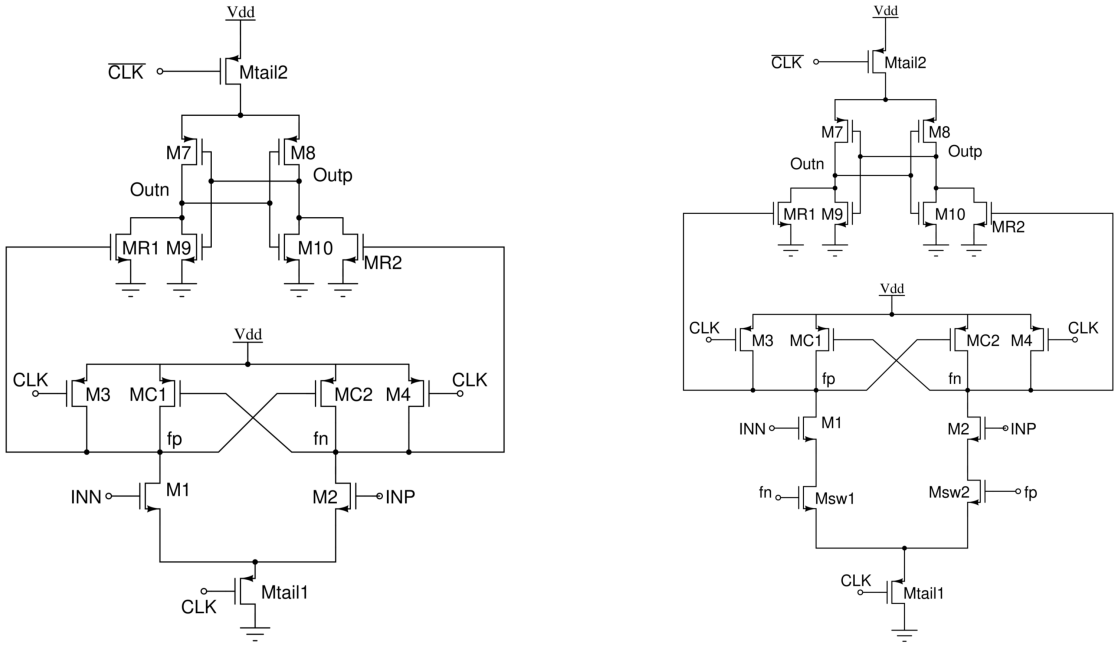

Fig. 5. Figure of proposed dynamic comparator (A) Main idea (B) Final Structure

fn fully discharge . Stated differently, the proposed structure differs from the conventional double-tail dynamic comparator in that a pMOS M_{c1} is activated as soon as the comparator detects a change in node behavior, such as fn discharging more quickly. This action pulls the other node, fp, back to the V_{DD}.The difference between fn and fp $\Delta V_{fn/fp}$ therefore grows exponentially over time, resulting in a decrease in latch regeneration time.

From immune this effect we use two transistor M_{sw1} and M_{sw2} below to both the input transistors .

As in first phase the node fn and node fp has precharget till V_{DD} and during this phase both as in the circuit the control transistor detects that the fn and fp discharges at the speed of discharging which one is faster according to this the control transistor acts and automatically increase in the input voltage difference.Assuming that fp is approaching the V_{DD} and that fn needs to be fully discharged, the switch in fp charging route will be opened to stop any current from being pulled from the V_{DD}, while the other switch that is connected to the node fn will be closed to let assume the node fn to be fully discharged.

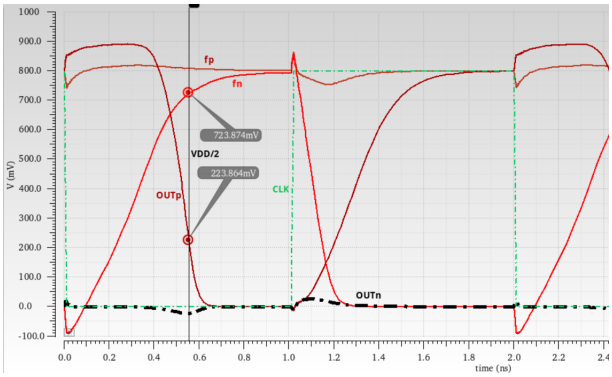

Fig. 6. Transient result of the proposed double-tail comparator main idea for ΔV_{in} = 5 mV , $V_{cm} = 0.7V$ and $V_{DD} = 0.8V$

B. *Delay Analysis*

The reduction in delay for the propose circuit (fig 6)has been calculated theoretically is approximately same as we calculated earlier in conventional dynamic comperator and in double tail dynamic comparator , but this proposed dynamic comparator improves the speed and efficiency of the double

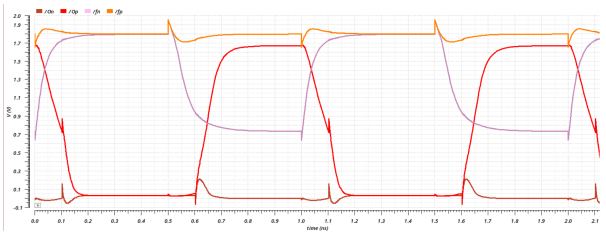

Fig. 7. Transient result of the proposed double-tail comparator of final structure for ΔV_{in} = 5 mV , $V_{cm} = 0.7V$ and $V_{DD} = 0.8V$

tail comparator by increasing the difference between the initial output voltage (ΔV_0) when the ($t = t_0$) and its also increase the practical trans-conductance (g_{meff}) of the latch , both the factors has been calculated in details has been done like similar as we calculated before .

Effect to increasing the ΔV_0 , as we done before for t_0 after the starting in latch regeneration . Latching regeneration begins at t0, which is the time interval after which the first NMOS transistor of the cascaded inverters turns on, lowering one of the outputs and starting regeneration.

$$\Delta V_0 = V_{thn}\frac{\Delta I_{latch}}{I_{B1}}$$

$$\Delta V_0 \approx 2V_{thn}\frac{\Delta I_{latch}}{I_{tail2}}$$

$$\Delta V_0 = 2V_{thn}\frac{g_{mR1,2}}{I_{tail2}}\Delta V_{fn/fp} \tag{12}$$

Using the control transistors $_{c1}$ and M_{c2} in conjunction with the two serial switches transistors $M_{sw1,2}$ now simulates the behavior of a transistor in back-to-back inverter pair, which is necessary to determine $\Delta V_{fn/fp}$ at t = t_0 so we get

$$\Delta V_{fn/fp} = \Delta V_{fn,fp} exp((A - v - 1)\frac{t}{\tau}) \tag{13}$$

In the above equation $\frac{\tau}{A_v - 1} \approx \frac{C_{L,fn,fp}}{g_{m,eff}}$ and the pre-voltage difference between both the nodes fn and fp is calculated as $\Delta V_{fn,fp}$ at some instance of time both the PMOS M_{C1} and M_{C2} turns on and it follows the output voltage difference at initial point is $\Delta V_{fn,fp}$ it is obtained by the corrosponding equation

$$\Delta V_{fn,fp} = 2|V_{thp}|\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}} \tag{14}$$

By substituting the (eq 13) in (eq 12) we get

$$\Delta V_0 = \frac{2V_{thn}g_{mR1,2}}{I_{tail2}}\Delta V_{fn/fp}$$

$$\Delta V_0 = 4V_{thn}\frac{|V_{thp}|g_{mR1,2}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}} \times exp(\frac{G_{m,eff1} \times t_0}{C_{L,fn,fp}}) \tag{15}$$

The voltage difference we calculated in conventional dynamic comparator is less then the voltage difference between in the proposed double-tail dynamic comparator which is remarkable in the exponential form it is shown by comparing by the (eq 10) and (eq 15) .

The effect for

$$t_{latch} = \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \times ln(\frac{\Delta V_{out}}{\Delta V_0})$$

Here $\Delta V_{out} = \frac{V_{DD}}{2}$

$$t_{latch} = \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \times ln(\frac{\frac{V_{DD}}{2}}{\Delta V_0}) \tag{16}$$

By including all the effects the total delay in the proposed comparator is given as and calculated as we calculated before by using

$$\tau_{delay} = t_0 + t_{latch}$$

$$\tau_{delay} = \frac{2V_{thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}} \times ln(\frac{\frac{V_{DD}}{2}}{\Delta V_0})$$

$$\tau_{delay} = \frac{2V_{thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}}$$

$$ln(\frac{\frac{V_{DD}}{2}}{4V_{thn}|V_{thp}|\frac{g_{mR1,2}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}} \times exp(\frac{G_{m,eff}t_0}{C_{L,fn,fp}})}) \tag{17}$$

IV. Design Consideration

While calculating the size of the tail transistors M_{tail1} and M_{tail2} of our proposed circuit some issues must be considered and design it like so the on-off or switching time of the transistor is less the t_0.

$$t_{on,Mc1,Mc2} < t_0 \rightarrow \frac{|V_{thp}|C_{L,fn,fp}}{I_{n1,n2}} < \frac{V_{thn}C_{Lout}}{I_{B1}}$$

$$\rightarrow \frac{|V_{thp}|C_{L,fn,fp}}{\frac{Itail1}{2}} < \frac{V_{thn}C_{Lout}}{\frac{I_{tail2}}{2}} \tag{18}$$

The drain-source voltage of the nMOS switches, which are positioned underneath the input transistors, must be taken into account while designing them since it may reduce the voltage headroom and hence limit their usefulness in low-voltage applications.NMOS switches with low on-resistance are needed to mitigate this impact. Put differently, big transistors have to be employed. The nodes fn and fp haveing parasitic capacitances are unaffected by the parasitic capacitances of these switches, hence it is feasible to choose the size of the NMOS switch transistors in a manner that maintains low-voltage and low-power operations.

A. *Calculation of* $\frac{W}{L}$:

For calculating $\frac{W}{L}$ of the transistor we have to first assume the current flowing through M1 , M2 and M_{tail1} so for this we assume $I_{tail1} < 1mA$ and $V_{in,CM}$=0.9V and V_{th}=0.4V

First case when CLK is high then the M1 and M2 is in saturation and M_{taikl1} is in linear region so for M_{tail1}

$$V_{DS} \leq V_{in,CM} - V_{th}$$
$$V_{DS} \leq 0.9V - 0.4V$$
$$V_{DS} \leq 0.5V$$

so let us assume V_{DS} = 0.3V

now current equation for M_{tail1} when it is in linear region and we assuming total current flow through $M_{tail1} = \frac{I_1}{2} + \frac{I_2}{2}$

$$I_{tail1} = \mu_n C_{ox}\frac{W}{L}_{tail1}[(V_{gs} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}] \tag{19}$$

$$10^{-3} = 4.5 \times 10^{-3}\frac{W}{L}_{tail1}[(0.9 - 0.4)0.3 - \frac{0.3^2}{2}]$$

So $\frac{W}{L}_{tail1} \geq 4.23$ so we assume the $\frac{W}{L}_{tail1} = 5$

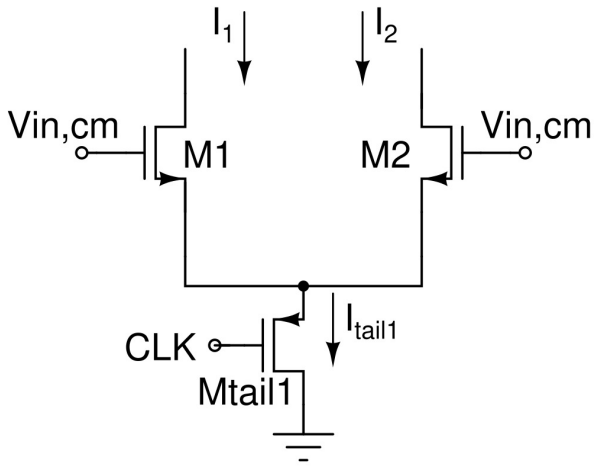

Fig. 8. Assuming the current flow for Calculating W/L

Now we have to calculate $\frac{W}{L}_{1,2}$ both have same area and have common input and both is in saturation region so the current equation for saturation region is

$$I_{1,2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}_{1,2}(V_{gs} - V_{th})^2 \tag{20}$$

$$0.5 \times 10^{-3} = \tfrac{1}{2} \times 4.5 \times 10^{-3}\tfrac{W}{L}_{1,2}(0.9 - 0.3 - 0.4)^2$$

so $\frac{W}{L}_{1,2} \geq 5.55$ so we assume $\frac{W}{L}_{1,2} = 6$

In the proposed circuit we use two transistor to control these we applied the two transistor below the input transistor which approximately have the same current so they also have same W/L

$$I_{sw1,2} = \tfrac{1}{2}\mu_n \times C_{ox}\tfrac{W}{L}_{sw1,2}(V_{GS} - V_{th})^2$$
$$M_{sw1,2} = 6$$

Earlier we assume the clock is high so the Pmos transistors will on and the cross-coupled inverters starts working the source is at V_{DD} and the gate voltage is equal to V_{DD} so the mos is in saturation region because its satisfied the saturation region condition $V_{DS} > (V_{GS} - V_{th})$.

$$I_{M3,M4} = \tfrac{1}{2}\mu_n C_{ox}\tfrac{W}{L}_{M3,M4}(V_{gs} - V_{th})^2 = 2.25 \approx 2.5$$

and the mos $M_{c1,c2}$ also have the same parameters so it is approximately have a smae parameters so,

$$\frac{W}{L}_{c1,c2} = 2.25 \approx 2$$

In the back to back inverter $M_{7,8}$ and $M_{9,10}$ have same current and having a approximately double in the parameters pMOS have a double parameter then the nMOS and all are in saturation region . Assuming current is greater then 1mA

$$I_{M7,M8} = \tfrac{1}{2}\mu_n C_{ox}\tfrac{W}{L}_{M7,M8}(V_{gs} - V_{th})^2$$
$$10^{-3} = \tfrac{1}{2} \times 4.5 \times 10^{-3}\tfrac{W}{L}_{M7,M8}(0.9 - 0.4)^2 = 2.25 \approx 2.5$$

and $M_{9,10}$ is twice the $M_{7,8}$ so $M_{9,10}$ = 5

B. Mismatch Analysis

As a general rule, the effects of managing transistors' threshold voltage mismatch $V_{thc1,c2}$ and current factor mismatch are essentially nonexistent, with the exception of the scenario when the input differential voltage of the transistor M1 and M2 is extremely less and the discharge rates of fn and fp are approximately neglected.

V_{th} mismatch effect on the transistor M_{C1} and M_{C2} and we denote this mismatch with $\Delta V_{th,C1,C2}$. The mismatch in threshold voltage gives the differential current I_{diff} through transistor M_{C1} and M_{C2} .

$$I_{diff} = g_{mc1,c2}\Delta V_{thc1,2} \tag{21}$$

where $g_{m,c1,c2}$ is trans-conductance of the of the transistor M_{C1} and M_{C2} so due to this transistor we also have some input-referred offset voltage is obtained as

$$\Delta V_{eq,due\Delta V_{thc1,c2}} = \tfrac{g_{mc1,c2}\Delta V_{thc1,c2}}{g_{m1,m2}}$$
$$= \frac{\mu_p W_{C1,C2} \times V_{ODC1,C2}}{\mu_p W_{C1,C2} \times V_{ODC1,C2}}\Delta V_{thc1,c2} \tag{22}$$

here V_{OD} is equal to overdrive voltage of the transistor M_{C1} and M_{C2}.

Now we seen the Mismatch of current factor in the transistor M_{C1} and M_{C2} which is $\Delta\beta_{C1,C2}$: for calculating this current mismatch in order to input-referred mismatch due to the transistor M_{C1} and M_{C2} so the $\Delta\beta_{C1,C2}$ is figured as the depend on the channel length mismatch ΔW that is $\frac{\Delta\beta}{\beta} = \frac{\Delta W}{W}$ is generation of mismatch due to the width is calculated as

$$I_{diff} = \frac{1}{2}\mu_p \times C_{OX}\frac{\Delta W}{L}(V_{gsc1,c2} - V_{thc1,c2}) \tag{23}$$

Here the $V_{gsc1,c2}$ is the difference between the gate and source of the transistor M_{C1} and M_{C2} and,

$V_{thc1,c2}$ is the difference between the threshold voltage of the transistor M_{C1} and M_{C2} .

Note : That the transistor M_{C1} and M_{C2} are in the saturation region as we seen that $|V_{GDc1,c2}| = |V_{fn} - V_{fp}| < |V_{thp}|$ so according to this we calculate the input referred offset occurs due to mismatch in current we calculate it as

$$\Delta V_{eq,due\Delta\beta_{C1,C2}} = \tfrac{i_{diff}}{g_{m1,2}}$$
$$= \tfrac{0.5\mu_p \times W_{C1,C2}(V_{gsc1,c2} - V_{thp})^2}{\mu_n W_{1,2}(V_{gs1,2} - V_{thn})}$$
$$= \frac{0.5\mu_p \times W_{C1,C2} \times V_{ODc1,c2}^2}{\mu_n W_{1,2}(V_{cm} - R_{CLK}K_{nC1,C2} \times V_{ODc1,c2}^2 - V_{thn})} \tag{24}$$

Here V_{cm} is common voltage across both the input transistor and the R_{CLK} is the equivalent resistance of both the tail transistor M_{tail1} and M_{tail2} .

we noticed that from (eq.22) and (eq.24) the $\frac{W_{C1,C2}}{W_{1,2}}$ is reducing the effect of offset voltage so for increasing the difference in input voltage we will increasing the size of input transistor and which helps in to reducing in the control transistor mismatch M_{C1} and M_{C2}.

and the total input referred offset is calculated as

$$\sigma_{total} = \sqrt{\sigma^2_{\Delta V_{thC1,C2}} + \sigma^2_{\Delta \beta_{C1,C2}}} \tag{25}$$

C. *Kickback Noise*

The huge voltage differences on the regeneration nodes are related to the comparator's input, primarily in latch comparators, because of the parasitic capacitances of the transistors. Because of the non-zero output impedance of the circuit before it, the input voltage is thrown off, which might impair the converter's accuracy. "Kickback noise" is the common term used to describe this problem and we noticed that comparators with the quickest speeds and highest power efficiency produce greater kickback noise.Although our proposed circuit and the typical dynamic comparator have almost comparable kickback noise, the double-tail construction utilizes input-output isolation to minimize it.

Since the control transistors in our proposed comparator aren't meant to be as robust as the latch transistors in a traditional dynamic comparator, the size of those transistors can be chosen to maintain the benefits of power reduction and speed enhancement while lowering kickback noise. Furthermore, basic kickback reduction strategies may be used for some situations where kickback becomes significant.

V. Simulation Result

While simulating the different types of comparators we done all this simulation in 0.18μm CMOS technology and take V_{DD} = 0.8V at the V_{cm} = 0.7V and first all the compatrators were put in the calculated parameters to get proper offset , kickback noise , delay and all for all this we seen that how we nullifying the disadvantages of to maintain all the parameters equal as per there configurations.

TABLE III
Summary of the Comparator Performance

Item	Value
Technology	180 nm CMOS
Supply Voltage	0.8V
Average power dissipation	356.2μW
Worst case delay (V_{cm} = 0.7V , ΔV_{in} = 1 mV)	602 ps
Delay/log(ΔV_{in})	77 ps/dec
Energy Efficiency	0.66pJ

When compared to a standard dynamic circuit, the comparator's latency in double-tail topologies is often less affected by changes in the input common-mode voltage, resulting in a broader common-mode range. There is almost similar power usage.

The suggested double-tail dynamic comparator has a much shorter latency in low-voltage applications than the other two configurations . It is evident that all topologies work roughly similarly at high supply voltages, with a clock-to-output latency of 200 ps (including the clock buffer) and an 8 mV offset of 0.65 pJ/bit conversion. Nevertheless, three structures begin to act differently as the supply voltage is lowered. It is clear that, while using about the same amount

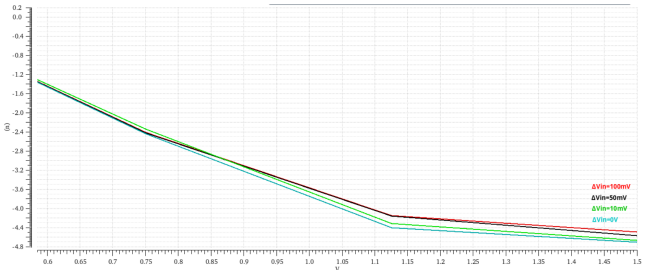

Fig. 9. Calculation of delay vs. Supply Voltage with different value of ΔV_{in}

of power as a traditional dynamic comparator, the double-tail design can function more quickly and at lower supply voltages. In comparison to the traditional double-tail topology, the justification for the suggested comparator is considerably better.

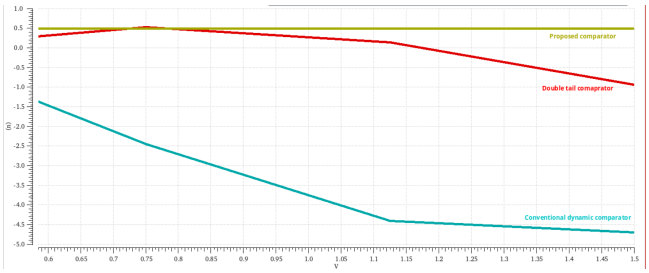

Fig. 10. Delay of all the comparators $\Delta V_{in} = 50mV$ and V_{DD} = 0.8V

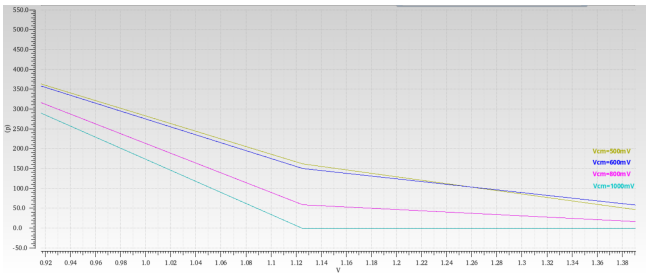

Fig. 11. Delay of proposed circuit vs. ΔV_{in} for differnent value of V_{cm}

TABLE IV
COMPARISION TABLE

Comparator Structure	**Conventional Dynamic Comparator**	**Double-tail Dynamic Comparator**	**Proposed Dynamic Comparator**
Technology CMOS	180nm	180nm	180nm
Supply Voltage (V)	0.8V	0.8V	0.8V
Delay/log(ΔV_{in})(ps/dec.)	77.425	310	430.75
Power dissipation (μW)	60.2	78.9	101.634
Kickback Noise Voltage at (ΔV_{in} = 10mV)	86 mV	101 mV	94 mV
Energy per Conversion (J)	0.39p	0.29p	0.27p
Input-referred offset voltage (mV)	8.96	9.47	8.265

VI. CONCLUSION

In this work, we developed expressions and performed a thorough delay analysis for timed dynamic comparators. We examined the two widely used designs of conventional double-tail dynamic comparators and conventional dynamic comparators. A novel dynamic comparator with low-voltage, low-power capacity was also introduced in an effort to enhance comparator performance. Theoretical calculations were used to build this comparator. The post-layout simulation results validate that the suggested comparator significantly reduces both the energy per conversion and latency when compared to the traditional dynamic comparator and double-tail comparator in 0.18μm CMOS technology.

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