ECE 385 Lab 3 Report Outline

- **Introduction**
  - Summarize what high-level function your circuit performs. What operations can the processor do? How many bits can it operate on? Etc. The introduction should be approximately 3 - 5 sentences.
- **Answers to pre-lab questions. These are restated below for convenience**
  - Describe the simplest (two-input one-output) circuit that can optionally invert a signal (i.e., one input determines if the output is equal to the other input or equal to the other input inverted). Sketch your circuit.
  - Explain how a modular design such as that presented above improves testability and cuts down development time. Propose an approach that could be used to troubleshoot the modular circuit above if it appeared to be completing the computation cycle correctly but was not giving the correct output. (Be specific.)
- **Operation of the logic processor**
  - Describe the sequence of switches the user must flip to load data into the A and B registers.
  - Describe the sequence of switches the user must flip to initiate a computation and routing operation.
- **Written description, block diagram and state machine diagram of logic processor**
  - Written Description
    - Describe in words each block in the high-level diagram (a short paragraph for at least he register unit, computation unit, routing unit, and control unit).
  - Block Diagram
    - Include a high-level block diagram. It's OK to use the one in the lab manual (copied below).

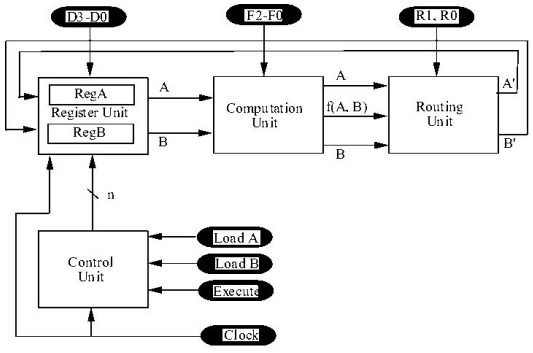

Figure 1: Block Diagram

  - State Machine Diagram
    - Explicitly state if you used a Mealy or Moore machine (or some weird hybrid)
    - Label each state (bubble)
      - Give each state a meaningful name
      - Specify the binary flip-flop values associated with each state.

        - ❑ If you are using a Moore Machine, label the values of all meaningful outputs associated with each state.
    - ❑ Label each arc
        - ❑ The combination of inputs which trigger the arc
        - ❑ If you are using a Mealy Machine, label the values of all meaningful outputs associated with each arc.
    - ❑ It is OK to label each bubble/arc with a single identifier and put the rest of the requested info in a table to reduce clutter.
- ❑ **Design steps taken and detailed circuit schematic diagram**
    - ❑ Design Steps Taken
        - ❑ If you used k-maps or truth tables during design, include them here. (If you didn't need them, you don't need to include them). K-maps are usually only helpful for creating the next-state logic in the control unit.
        - ❑ Written description of the design considerations taken (did you consider multiple implementations of the same circuit and the tradeoffs of each?)
    - ❑ Detailed Circuit Schematic
        - ❑ Draw a gate level schematic of your circuit. A gate-level diagram has components like 

and NOT like 

. It is OK to use small standard blocks like MUXes, flip-flops, and shift registers, but custom blocks like your control unit must have a gate level schematic.
        - ❑ If the schematic becomes too large, components such as the control unit can be represented as black boxes on the top level schematic, and a detailed schematic of that component can be included below
- ❑ **Layout sheet**
    - ❑ Use the template in GG.20 or compose a similar layout sheet yourself.
    - ❑ Items you do NOT need to label in the component layout
        - ❑ Vcc and GND pins
        - ❑ Unconnected pins (such as those on unused gates)
        - ❑ Mode pins tied to Vcc or GND (such as strobes and resets).
    - ❑ Items you DO need to label
        - ❑ Switch inputs
        - ❑ LED outputs
        - ❑ Intermediate logic signals (try to use the same naming conventions as your gate-level and high-level diagrams.
        - ❑ Mode pins that are driven by a switch or another chip (such as strobes and resets).
- ❑ **Description of all bugs encountered and corrective measures taken**

- ❑ **Conclusion**
    - ❑ Summarize the lab in a few sentences