EE6320 RF Integrated Circuits
Project: LNA Design

Performance Summary Table

Design metric	Measurement	Simulation Result	Requirement
Input matching	Worst case S11 in the specified band	-30dB	< −10dB
	Band over which S11 ≤ −10dB	4.4GHz to 6.3GHz	5.17GHz to 5.32GHz
	Band over which S11 ≤ −15dB	4.77GHz to 5.79GHz	-
Voltage Gain	Minimum Gain in the specified band	32.7dB	≥ 20dB
	Maximum Gain in the specified band	34dB	≥ 20dB
	Gain flatness in specified band [Max-Min Gain]	1.3dB	≤ 2dB
	3dB Bandwidth	270MHz	-
	Load Capacitance [Differential]	100fF	100f F
Noise Figure	Maximum Noise Figure in the specified band	1.9dB	≤ 3dB
	Minimum Noise Figure in the specified band	1.7dB	-
	Band over which NF ≤ 3dB	3.45GHz	-
Linearity	IIP3 Tones used	1MHz apart	-
	Input power used for extrapolation	-50dBm	-
	Power of Fundamental Tone at output (at chosen input power)	-51.25dBm	-
	Power of IM3 Tone at output (at chosen input power)	-144.6dBm	-
	Extrapolated IIP3	-3.3dBm	≥ -10dBm
Power	LNA DC power consumption [Excluding Bias]	1.62mW	Minimize
	Bias circuit power consumption	0.36mW	Minimize
Other	Sum of all on-chip inductances	12.4nF	-
	Sum of all off-chip inductances (2 Lg's)	3.8nF	-
	Sum of all resistances [Including bias]	110.6k	-
	Sum of all capacitances [Including AC coupling, excluding load]	2u in coupling 540fF additional	-
	Simulator Used	Cadence	-

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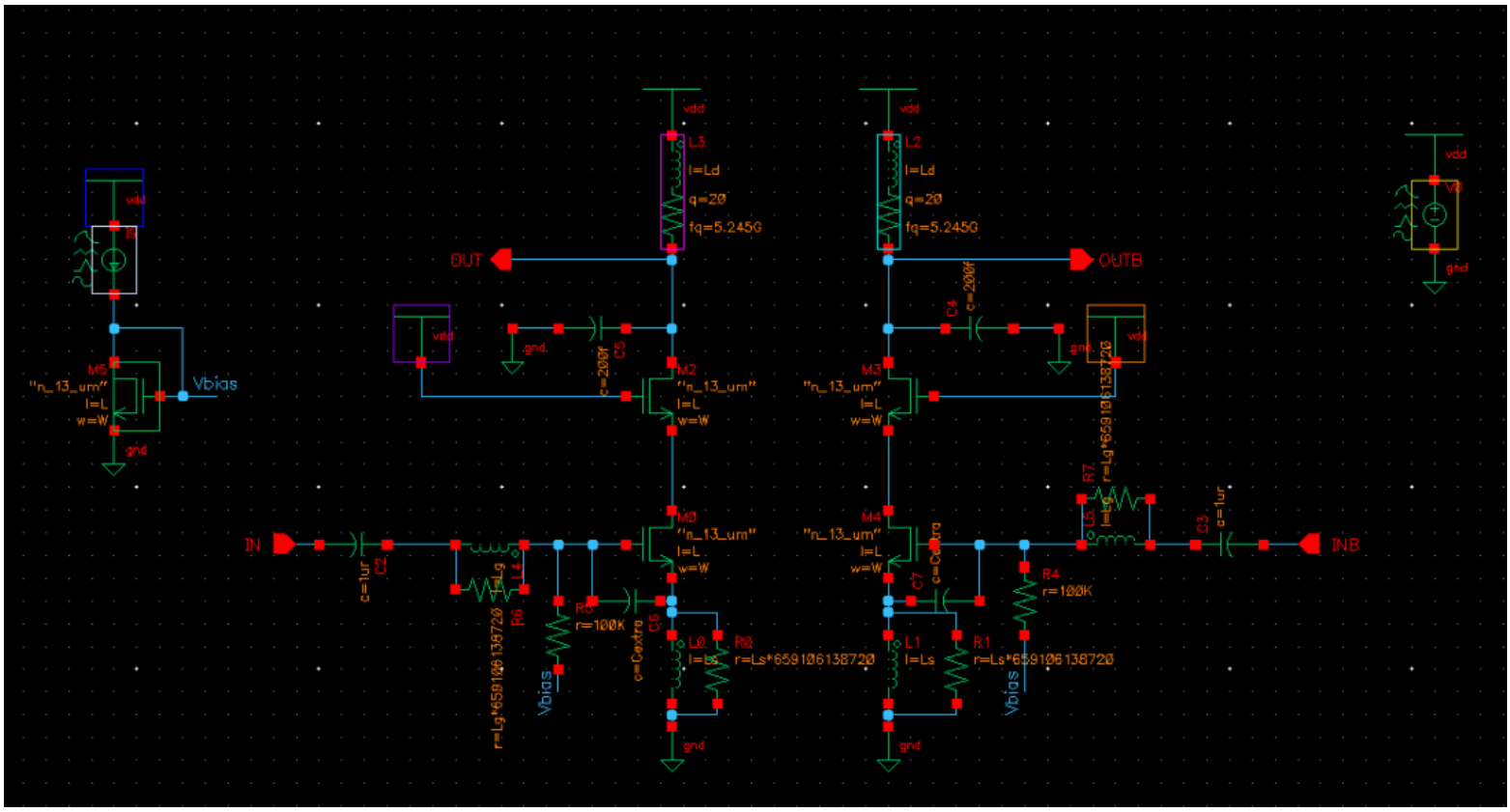
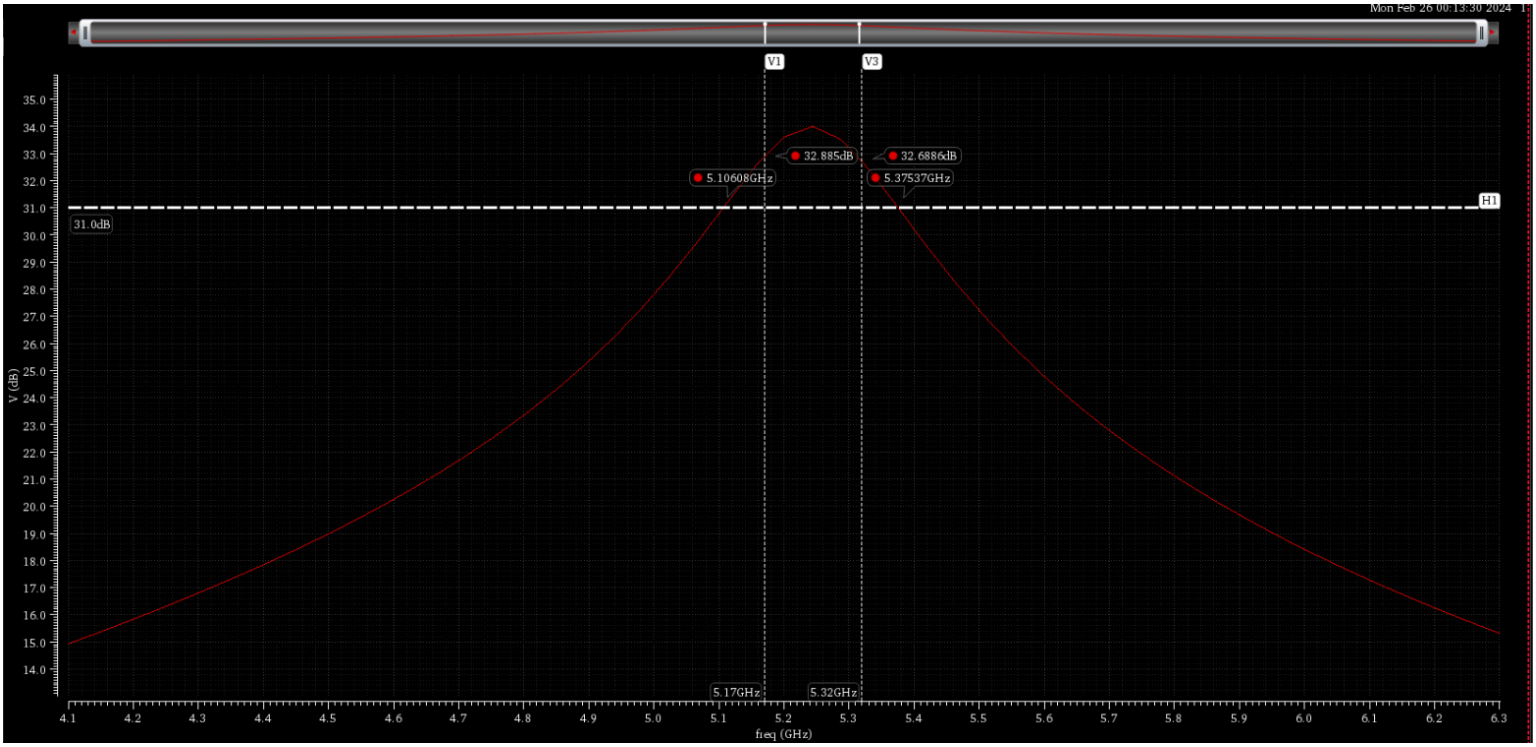
LNA Schematic



Component Values (one side values)		
Design Component	**Hand Calculated Value**	**Simulated Value**
Lg (gate inductance)	1.975nH	1.99nH
Ls (source inductance)	1.609nH	1.609nH
Ld (drain inductance)	4.475nH	4.6nH
Rd* (drain resistance)	2.95k	3.03k
R_ls* (res. parallel with Ls)	1.06k	1.06k
Rg* (res. parallel with Lg)	1.3k	1.31k

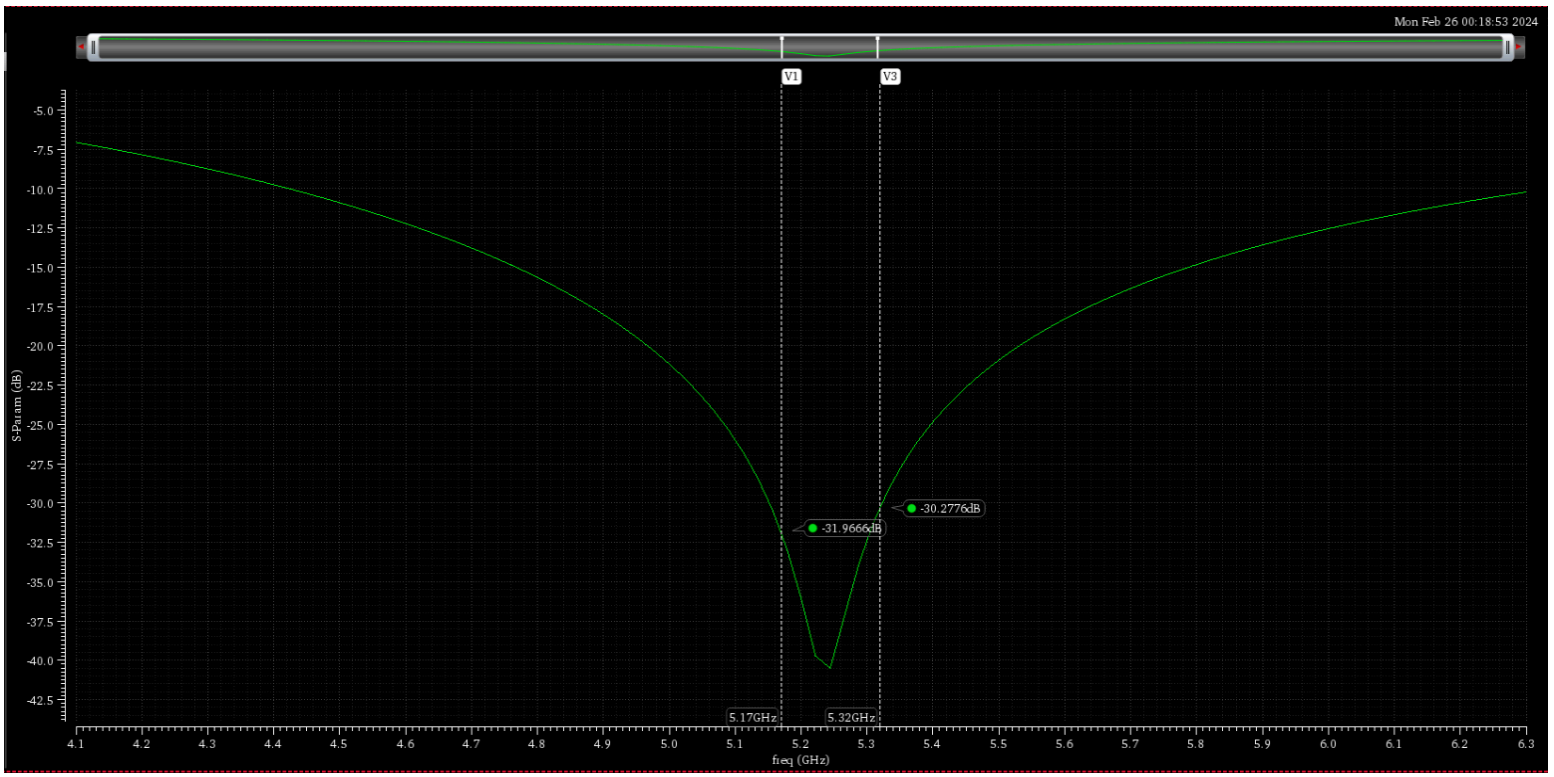
Fixed Constant Parameters
• **LNA MOS parameters: W = 15.66um, L = 0.18um**
• **Current Mirror MOS parameters: W = 15.66um, L = 0.18um**
• **I_bias (current): 541uA in mirror, results in 555uA in cascode**
• **C_coupling: 1uF**

Gain Plot

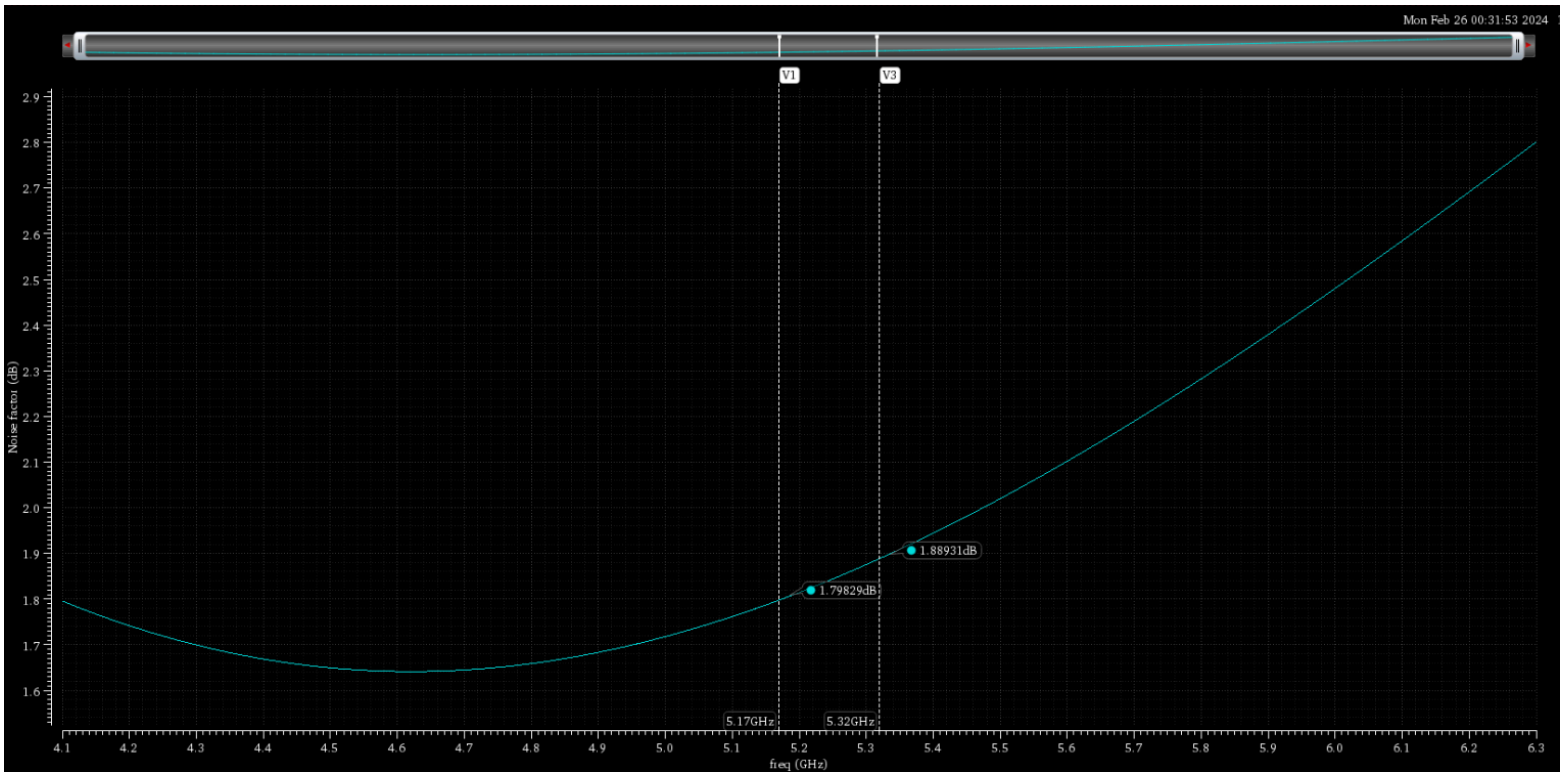


Max Gain through hand calculation: 24dB
Max Gain from the simulation: 34dB
-3dB Gain comes out to be: 31dB
From the figure, 3dB bandwidth comes out to be: 270MHz

S11 Plot

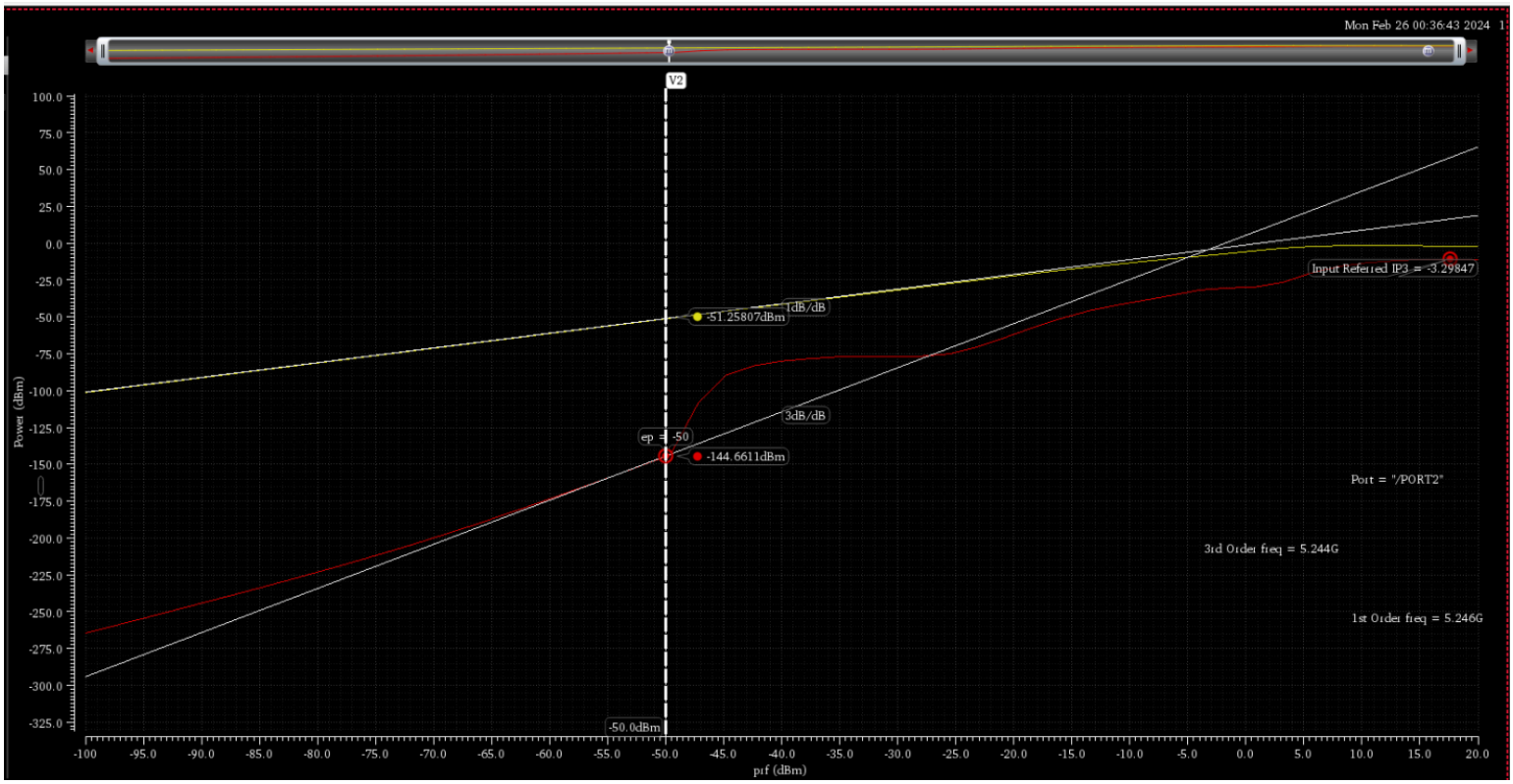


NF Plot



From the plot, NF comes out to be: 1.9dB

Linearity Plot (IIP3 Computation)



Tones used: 5.245GHz and 5.245GHz + 1MHz

IIP3 point comes out to be: -3.3dBm

Design of CMOS 0.13um RF Front-End

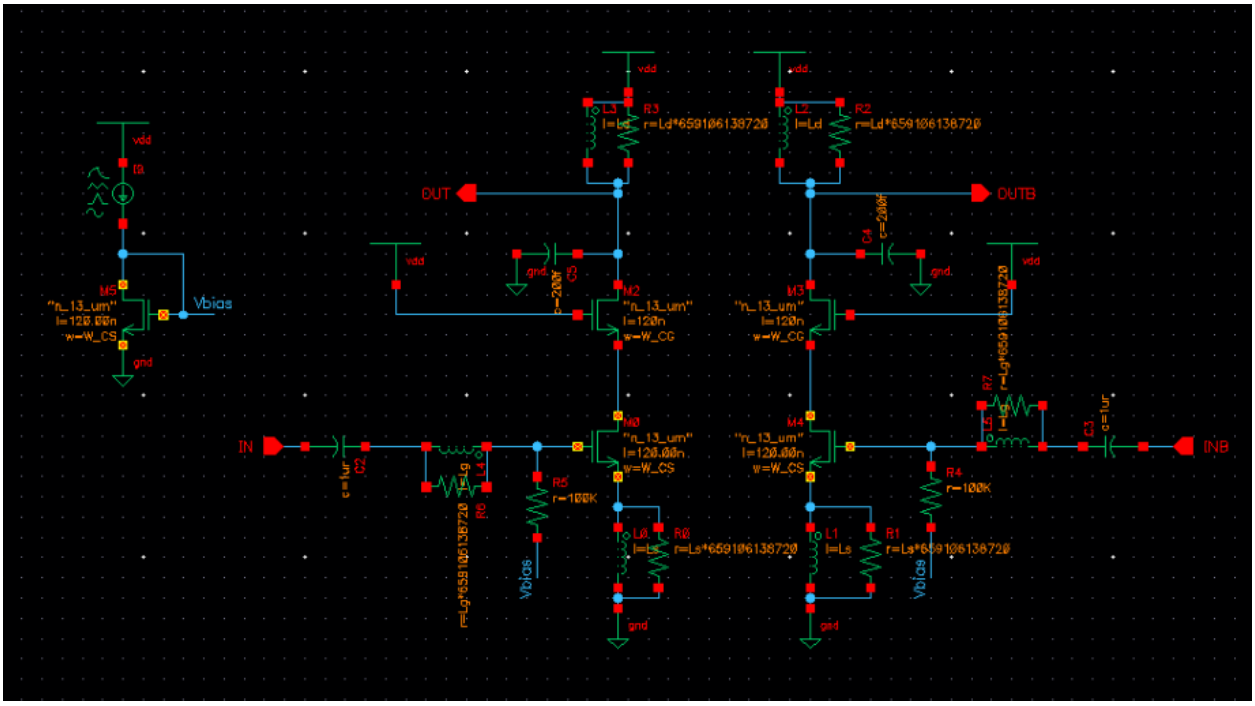
Rishi Nandha V - EE21B111

EE6320 : RF IC Design

February 25, 2024

1 Low Noise Amplifier

1.1 Schematic with Variables



1.2 Semi-Hand Calculations

We hand-calculate the values we should use. Note here that the Inductors having a parasitic resistance of $Q = 20$ requires us to recalculate most of the hand-expressions. Moreover, we need to Characterize the $g_m, C_{gs}, g_{ds}, C_{ds}$ against W, I_D for our Cascode for the $0.13\mu m$ technology too, because we cannot just rely on the Level I Model of MOSFET at this Frequency and when using a Short-Channel Device. Below is a 5-step procedure on starting from the Power Consumption as our starting point and maximizing the linearity, gain and input-matching from there. (Note that this procedure is slighty different than what was discussed in class)

1.2.1 Deciding the Bias Current with a Power Consumption Specification

The Problem in-hand does not specify a Power Consumption Specification. So let us just take $0.65mW$ as the Power Specification per Cascode for a starting point. This seems to be a practical and feasible value as seen in a similar LNA discussed in this IEEE Paper (assuming $1.3mW$ is distributed evenly between the two differential halves. This sets:

$$I_{bias} = 541\mu\text{A}$$

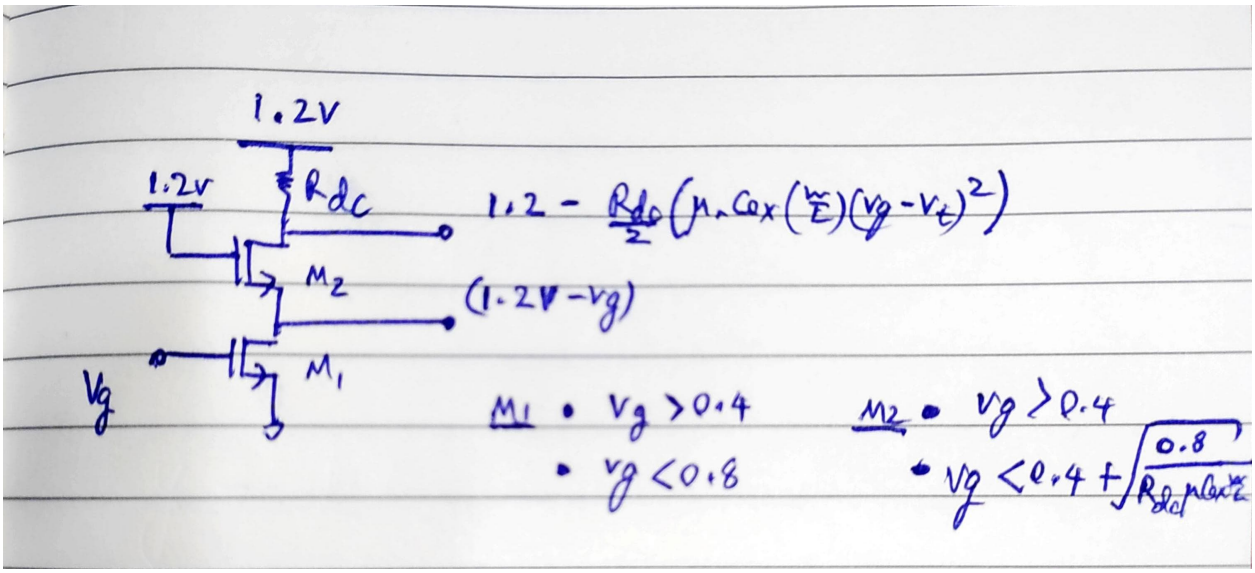
1.2.2 Setting L_D to Resonate Out C_{load}

Inductor to resonate out the given equivalent single-ended Load would be such that $\omega^2 = \frac{1}{L_D C_{load}}$ where C_{load} from the mirror has been estimated to be 200fF. Thus this sets:

$$L_D = 4.6\text{nH}$$

1.2.3 Setting Width/Length of the Transistors

The two transistors in the Cascode have to have the same Widths. The width should be determined such that for the current we have set we are at the centre of Swing Limits of these MOSFETs.



Choice of $Vgs = 0.55V$ sits well between the constraints. Picking a smaller Vgs will also increase our g_m:

$$V_{gs} = 0.55V \implies \left(\frac{W}{L}\right) = 87$$

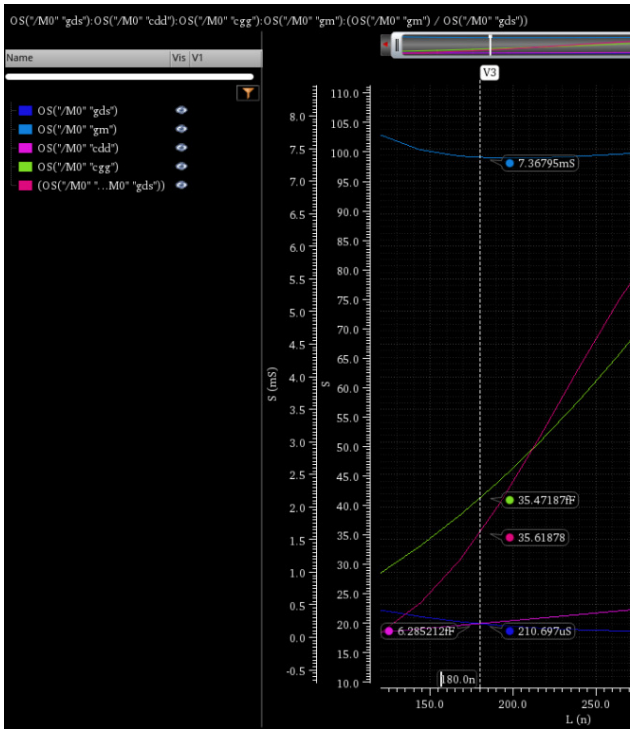
1.2.4 Scaling up Width and Length for the desired Gain and minimizing Area

We have a desired gain of 20dB which is limited by the intrinsic gain $\frac{g_m}{g_{ds}}$, which is dictated by the transistor dimensions. The C_{gs} also need to be a tangible value for L_g to be small and so there's an area trade-off between L_g and W, L too which favours that we increase transistor dimensions. $R_D = 40\pi f_0 L_D = 2949.5\Omega$. $G_{GD} = \left(\frac{2\cdot(541\mu)}{0.15}\right)\frac{1}{\left(g_{ds}+\frac{1}{2949.5}\right)} > 10$

$$g_{ds} \leq 0.3mS \implies \frac{g_m}{g_{ds}} \geq 24$$

Now we simulate the DC point of the MOSFET to find the scaling required for an intrinsic gain of about 20. From simulation we get:

$$L = 0.18\mu m$$



1.2.5 Input Impedance Matching

Like noted before the parasitic resistance R_S requires us to recalculate the L_S we need for the input impedance to be matched to 50Ω in single-ended (Thus, 100 Ω in Differential). To reduce the inductors required we will add a capacitor. This can either be added to ground from gate or between gate and source.

$$Z = \frac{j\omega L_s R_s}{R_s + j\omega L_s}$$

$$Z_g = \frac{1 + g_m Z}{j\omega(C_{gs} + C_{option\ 2})} + Z$$

$$Z_{in} = \left(Z_g || \frac{1}{j\omega C_{option\ 1}} \right) + \frac{jR_g \omega L_g}{jL_g \omega + R_g} = 50$$

Gradient Descent was performed to find which would be better. For option 1, the values obtained where $L_s = 3.55nH$, $L_g = 7.3nH$ and $C_{option\ 1} = 103fF$. For Option 2, we obtain, $L_s = 1.609nH$, $L_g = 1.975nH$ and $C_{option\ 2} = 227fF$. We'll go with the second.

```
x = np.array([s_normalized,g_normalized,Cextra_normalized])
for i in range(500):
    x, cost = GDE(f, 0.001, x, lambda x: grad(f,x,0.0001))
    print(x, cost, end='\r')
```

```
[  1.60860806   1.97463934 227.00009534] [0.00064584]
```

This gives a voltage gain of about 4dB too.

1.2.6 Summary of Semi-Hand Calculated Values

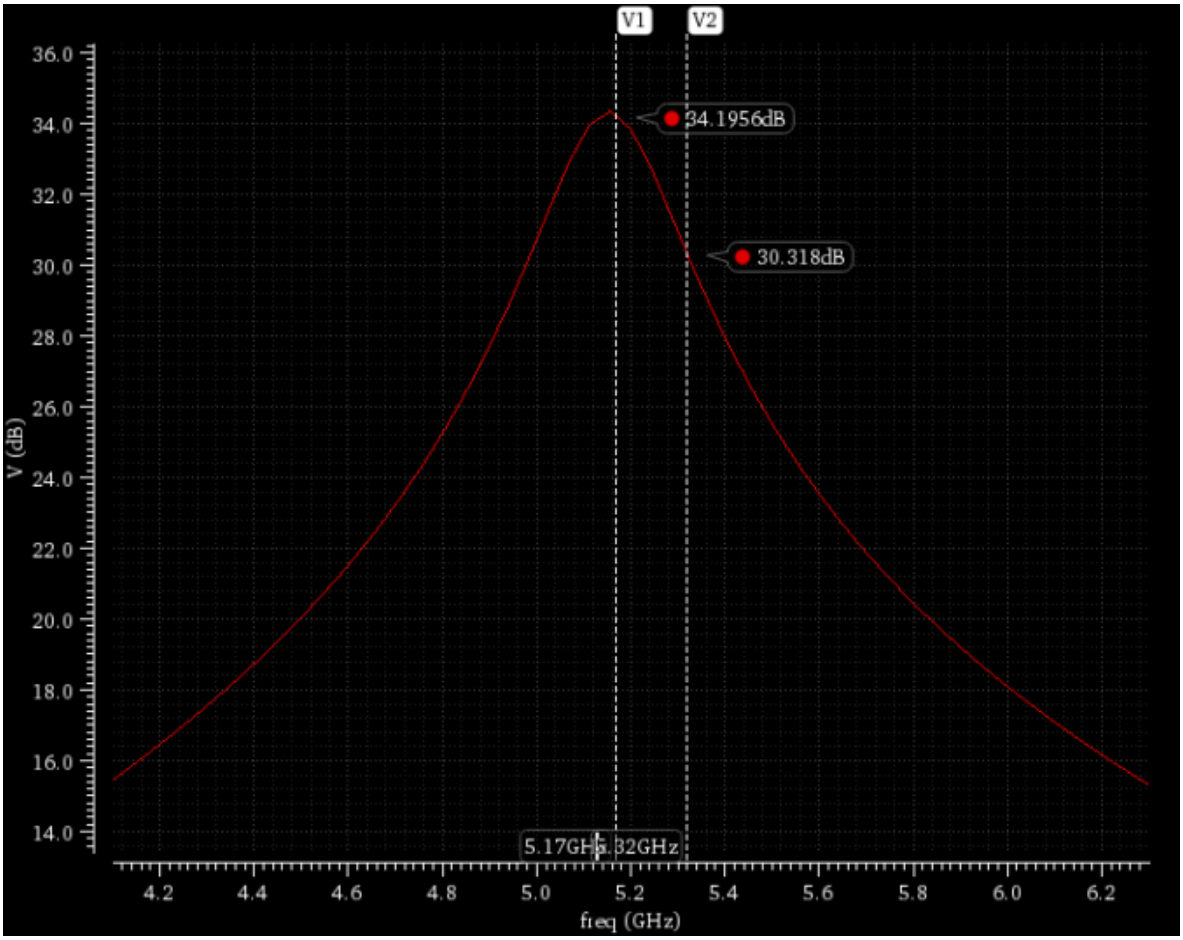
$$\boxed{I_{bias} = 541\mu A} \quad \boxed{L_D = 4.6nH} \quad \boxed{W = 15.66\mu m}$$

$$\boxed{L = 0.18\mu m} \quad \boxed{L_g = 1.975nH} \quad \boxed{L_s = 1.609nH} \quad \boxed{C_{gs,extra} = 227fF}$$

1.3 Fine-Tuning of Hand Calculated Values

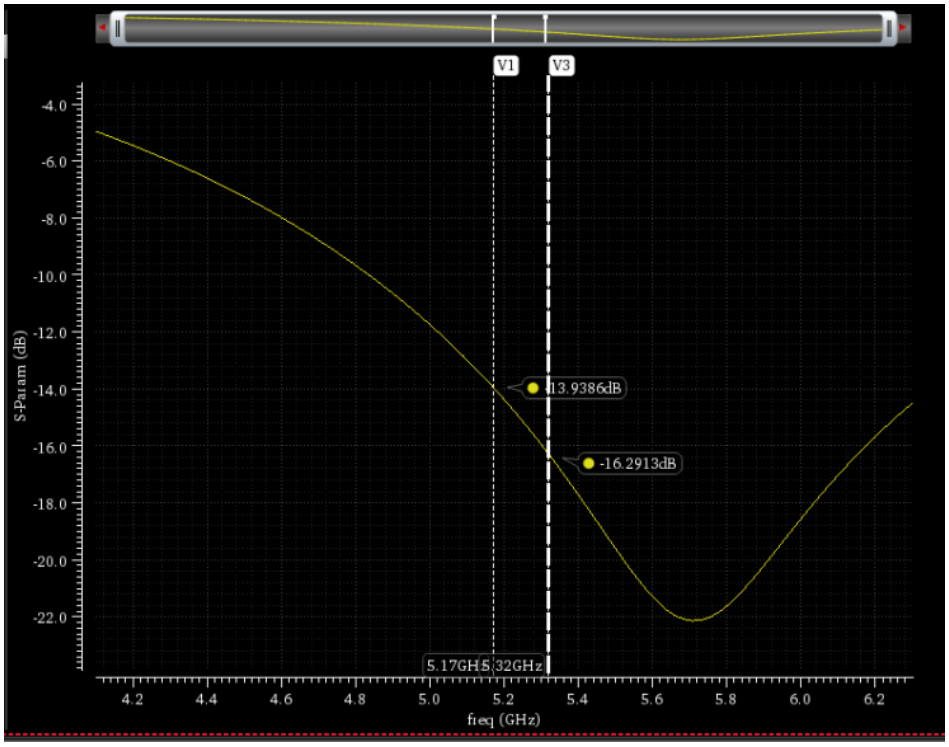
The hand-calculated values gave a really good IIP_3 of $-3.5dV$ value as expected due to the fixing of V_{gs} between the swing limits. But the $S_1 1$ and Gain are centered at a incorrect centre frequency owing to how we neglected effects of the Short-Channel MOSFET.

1. The Gain Flatness is not sufficient, caused by the Peak Occurring outside the Bandwidth



Hence we will vary L_D and see the behaviour of S_{11}.

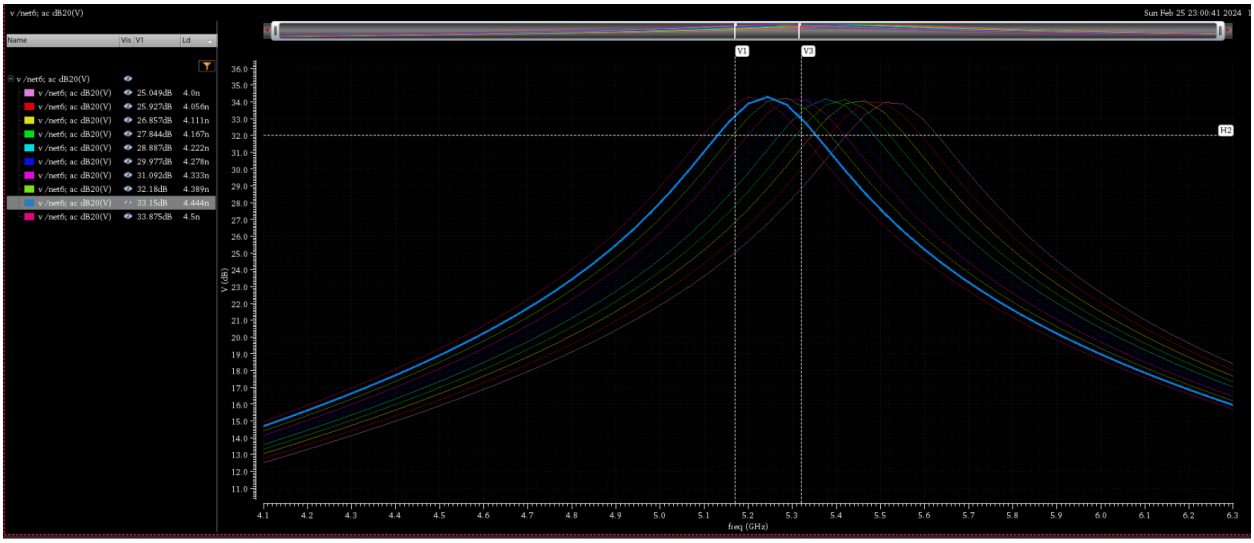
2. S_{11} is centred at a different centre frequency which can be improved if we move the peak



Hence we will vary L_g, L_s and C_{extra} and see the behaviour of S11

1.3.1 Optimizing Gain varying L_D

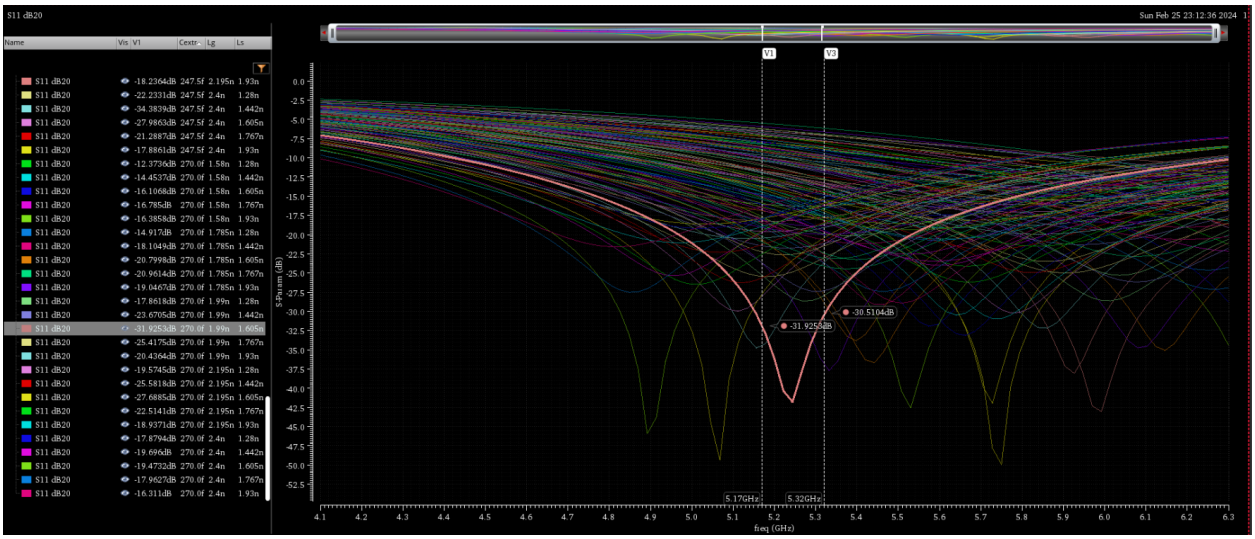
Below is the curve obtained which achieves flatness less than 2dB and a gain of more than 20dB as required



$$\boxed{L_D = 4.444nH}$$

1.3.2 Varying C_{extra}, L_g and L_s to Optimize S_{11}

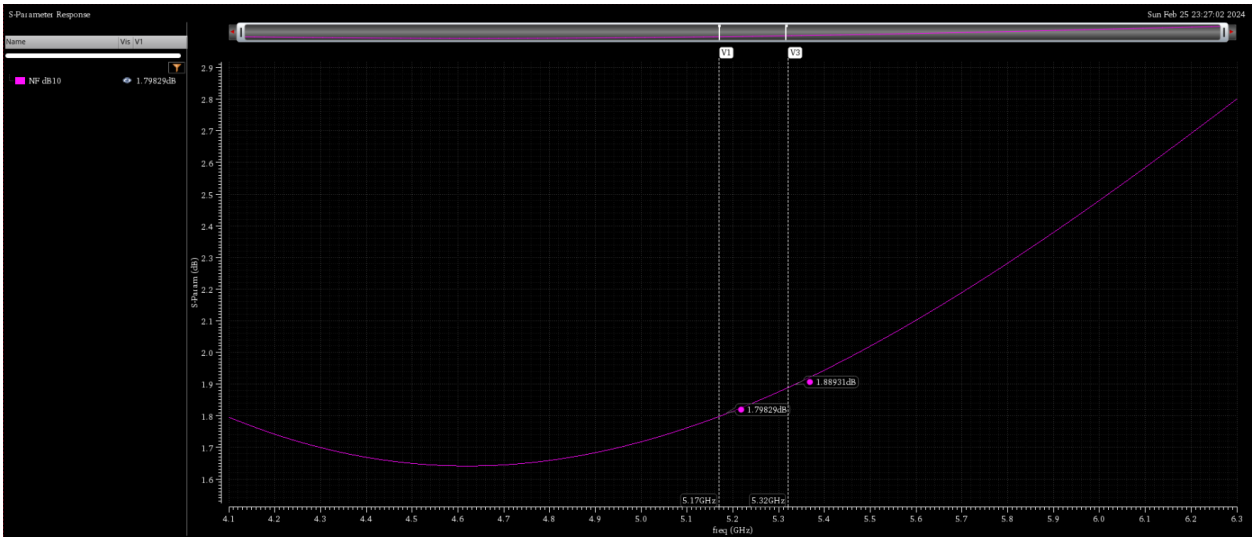
Below is the obtained S11 which is well below -10dB as required



$$\boxed{L_g = 1.99nH} \quad \boxed{C_{extra} = 270fF} \quad \boxed{L_s = 1.609nH}$$

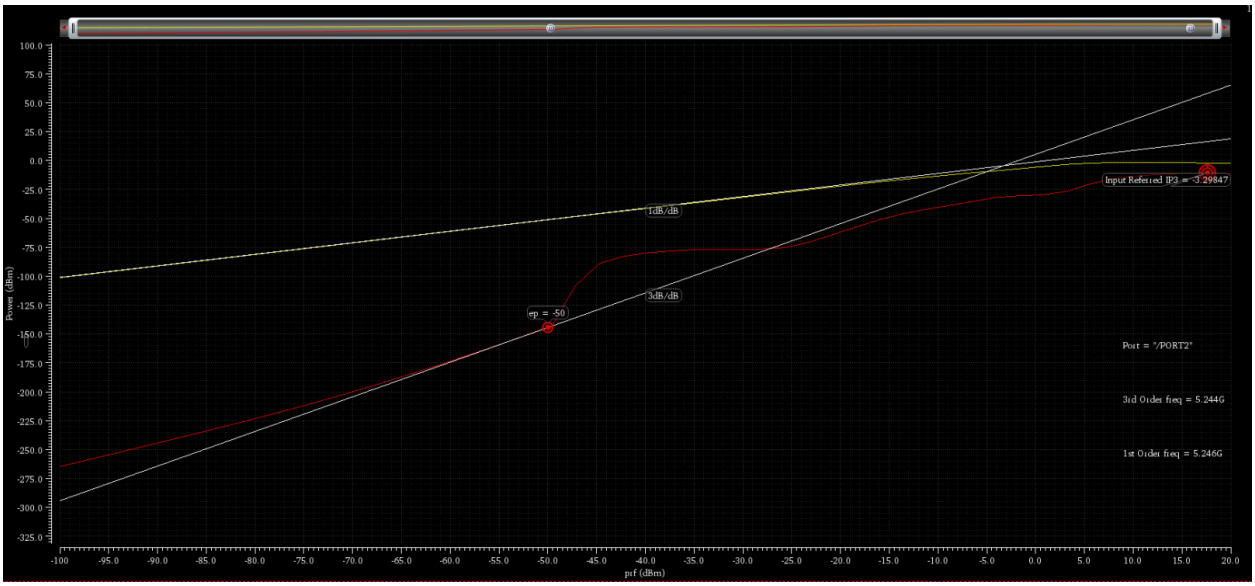
1.3.3 Noise Factor Simulation

Below is the obtained Noise Factor simulator which is well within the required bound of 3dB



1.3.4 IIP_3 Simulation

The obtained IIP3 is well above -10dBm as required



1.3.5 Power Consumed Simulation

Power simulated with DC points came out to be $1.98mW$ including the current mirror and $1.62mW$ without power drawn by the current mirror

1.4 Final Schematic