

EE6320 RF Integrated Circuits

Project: Mixer Design

Mixer Performance Summary Table

	<u>Design Metric</u>	<u>Performance</u>	<u>Specification</u>
<u>Conversion Gain</u>	Minimum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	18.16dB	>15 dB
	Maximum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	18.24dB	>15 dB
	Peak Gain flatness in specified band [Max-Min Gain]	0.0855dB	-
	Minimum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10MHz$]	18.15dB	>15 dB
	Maximum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10MHz$]	18.23dB	>15 dB
<u>Noise Figure</u>	Maximum SSB Noise Figure for $f_{LO} = 5.17GHz$	6.037dB	≤ 10 dB
	Maximum SSB Noise Figure for $f_{LO} = 5.245GHz$	6.051dB	≤ 10 dB
	Maximum SSB Noise Figure for $f_{LO} = 5.32GHz$	6.066dB	≤ 10 dB
<u>Linearity - IIP₂</u>	Input power used for extrapolation	-40dBm	-
	Power of Fundamental Tone at output (at chosen input power)	-21.82dBm	-
	Power of IM_2 Tone at output (at chosen input power)	-91.98dBm	-
	Extrapolated IIP ₂	30.16dBm	$\geq +30dBm$
<u>Linearity - IIP₃</u>	Input power used for extrapolation	-40dBm	-
	Power of Fundamental Tone at output (at chosen input power)	-21.82dBm	-
	Power of IM_3 Tone at output (at chosen input power)	-93.6dBm	-
	Extrapolated IIP ₃	-4.11dBm	$\geq -5dBm$
<u>Power</u>	Power consumed in DC	2.5mW	Minimize
	Power consumed due to Switching Current	0.35mW	
	Power consumed by everything except Current Mirror	2.85mW	
	Power consumed by the Current Mirror	0.8mW	
<u>Other</u>	Sum of all resistances [excluding bias]	1800	-
	Sum of biasing resistances	20k	-
	Sum of all capacitances [Including AC coupling]	200.02pF	-
	Sum of all inductances	0.2nH	-
	Load chosen (each R_load)	1800	-
	Differential Mixer Input Capacitance (C_gs Caps)	36fF	-
	Simulator Used	Cadence	-

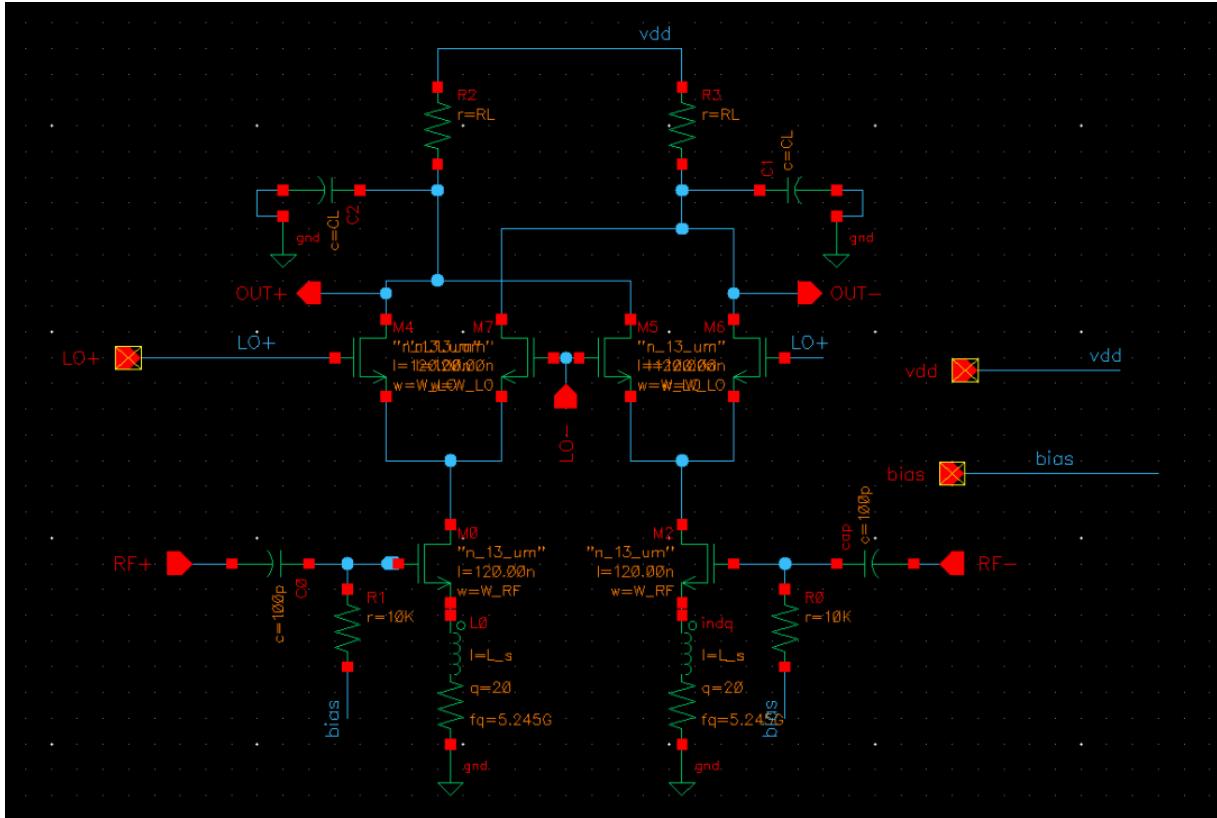
Name: Rishi Nandha V

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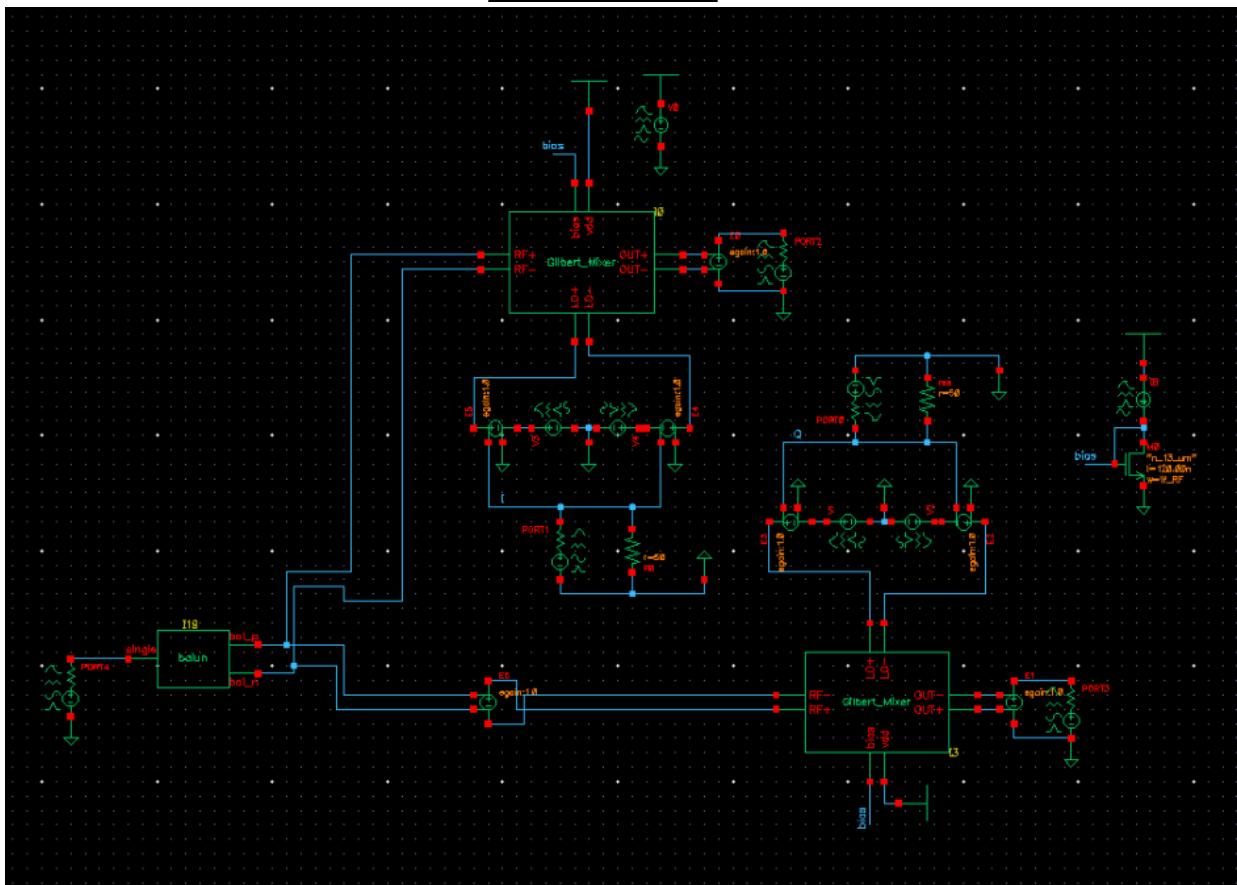
LNA + Mixer Performance Summary Table

	<u>Design Metric</u>	<u>LNA</u>	<u>Mixer</u>	<u>Cascade</u>	
				<u>Expected</u>	<u>Simulated</u>
Conversion Gain	$f_{IN} = f_{LO}, f_{LO} = 5.17\text{GHz}$	32.88dB	18.24dB	51.12	34.11
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 5.17\text{GHz}$	32.88dB	18.23dB	51.11	34.16
	$f_{IN} = f_{LO}, f_{LO} = 5.245\text{GHz}$	34dB	18.20dB	52.20	33.98
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 5.245\text{GHz}$	34dB	18.19dB	52.19	34.03
	$f_{IN} = f_{LO}, f_{LO} = 5.32\text{GHz}$	32.7dB	18.16dB	50.86	33.77
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 5.32\text{GHz}$	32.7dB	18.15dB	50.85	33.82
Noise Figure	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 5.17\text{GHz}$	1.7	6.04	1.90	4.36
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 5.245\text{GHz}$	1.8	6.05	1.97	4.44
	$f_{IN} = f_{LO} + 10\text{MHz}, f_{LO} = 5.32\text{GHz}$	1.9	6.07	2.09	4.56
Linearity IIP3	Input power used for extrapolation			-40dBm	
	Power of Fundamental Tone at output (at chosen input power)			-6dBm	
	Power of $I M_3$ Tone at output (at chosen input power)			-48dBm	
	Extrapolated IIP3			-18.89dBm	
Power	Total Power Consumed			4.166mW	
	Total power consumption [Excluding Bias]			2.716mW	
	Bias circuit power consumption			1.450mW	

Mixer Schematic



Mixer Testbench



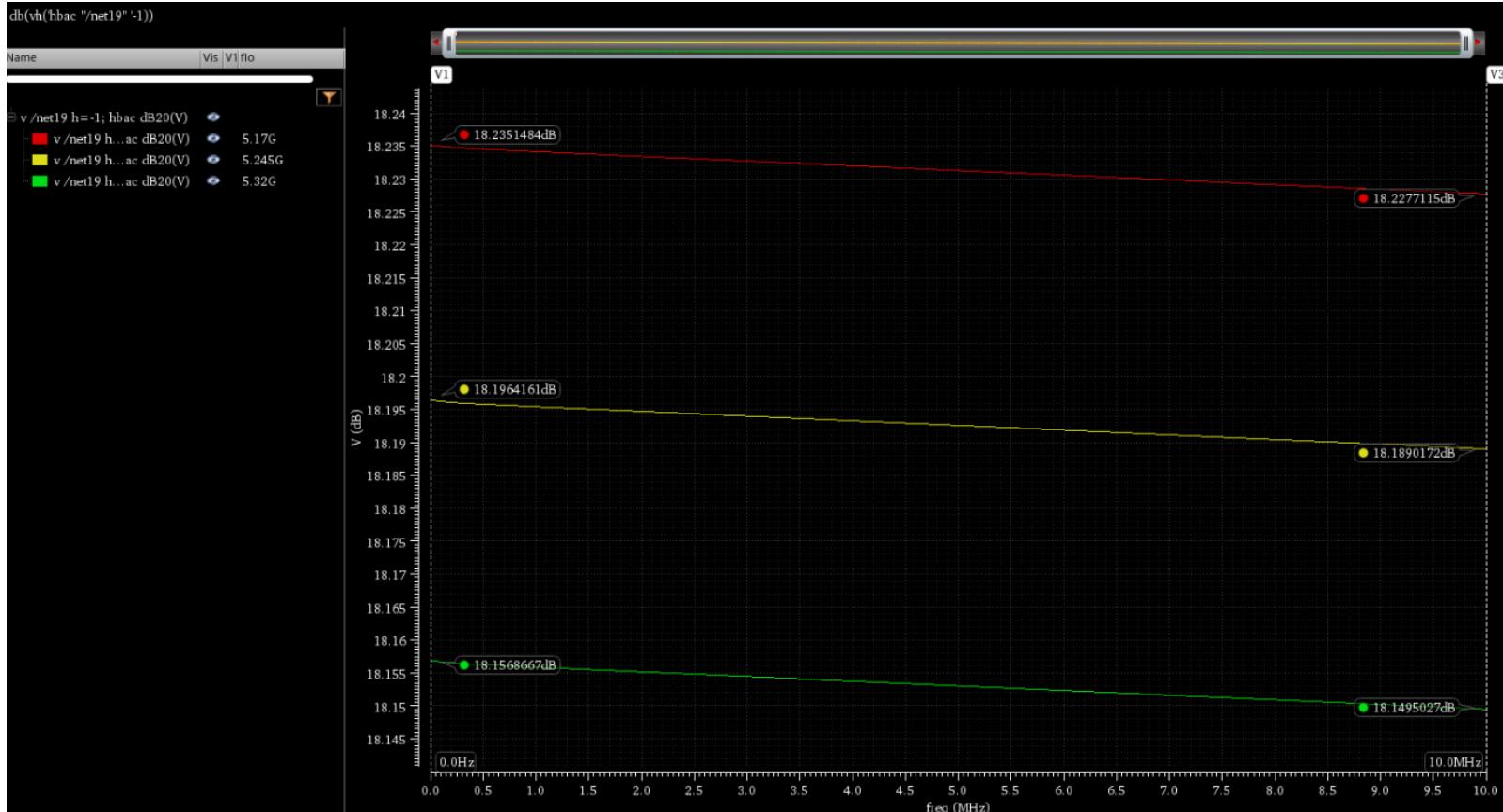
Design Variable Values

<u>Design Variable</u>	<u>Value</u>
Resistance (load, each side)	900 Ohms
Length of all MOS	0.12um
Width of Switch MOS (all 4)	45um
Width of Transconductance MOS (both MOS)	45um
Bias Current	667 uA
V_LO Amplitude	0.8Vpp (0.2V to 1V from VCO Project doc)

Fixed Constant Parameters

- Transconductance MOS C_gs: 72fF from the NMOS, 65fF additional added
- Current Mirror MOS: W = 45um, L = 0.12um
- Coupling capacitances: 100pF
- Bias Resistances: 10k (each)

Conversion Gain of Mixer at 5.17GHz Conversion Gain of Mixer at 5.245GHz Conversion Gain of Mixer at 5.32GHz

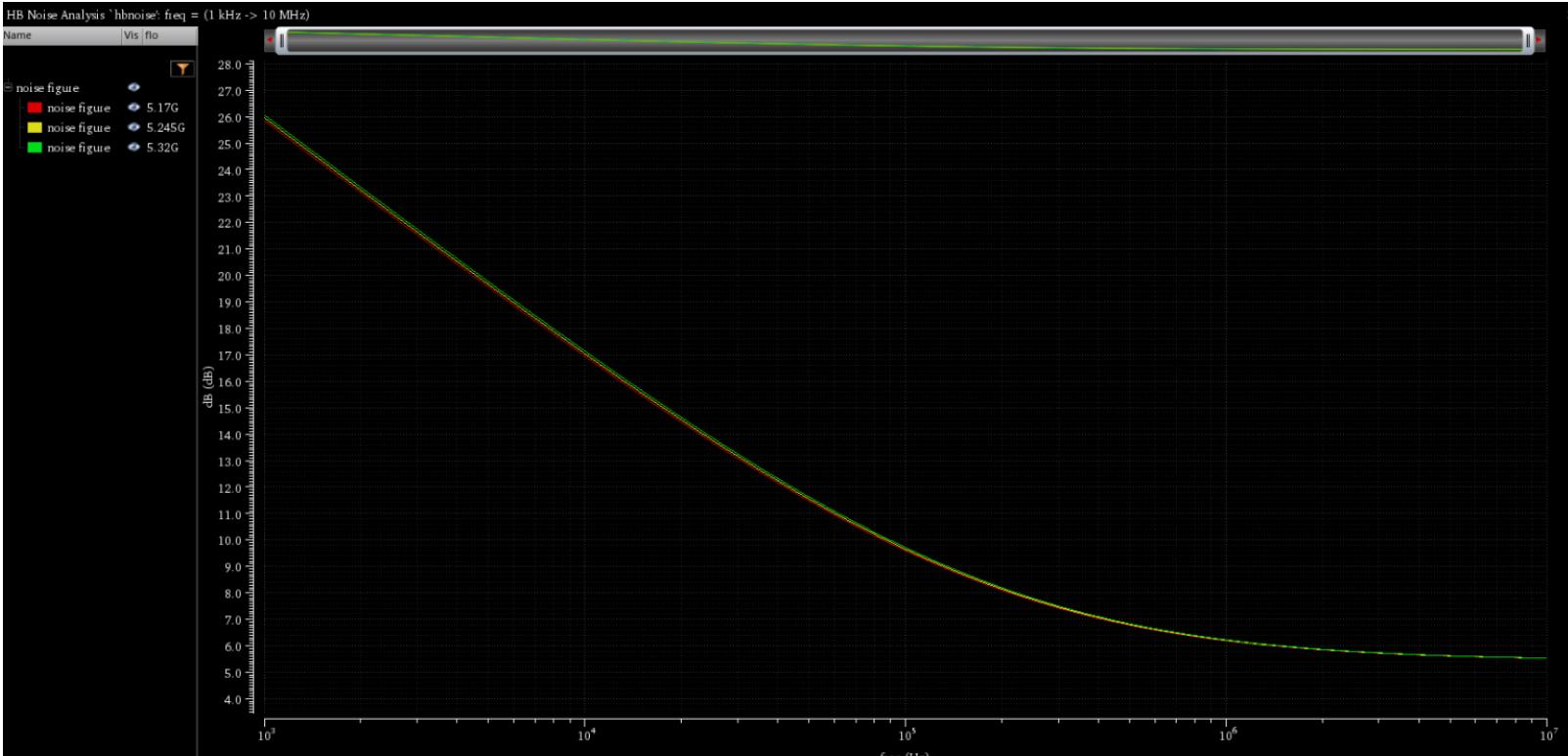


Noise Figure of Mixer at 5.17GHz

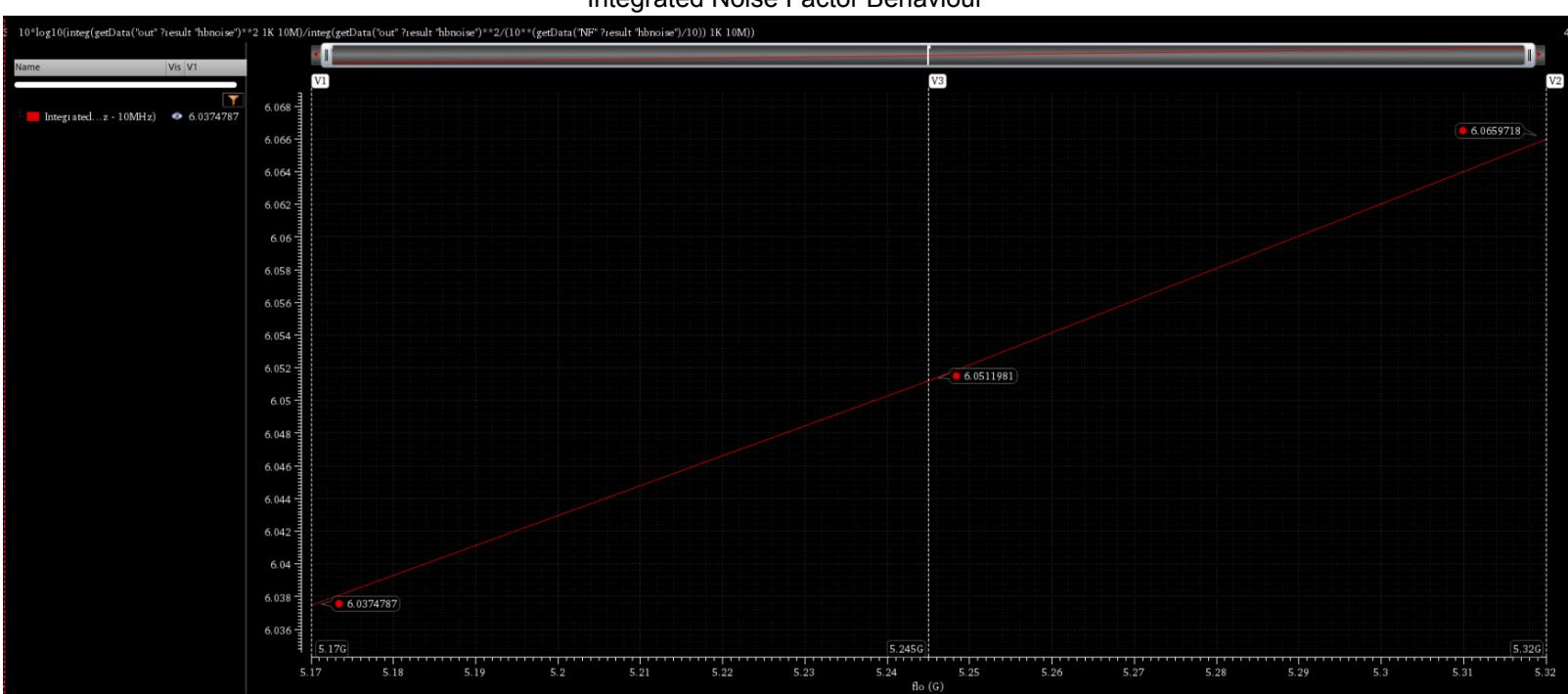
Noise Figure of Mixer at 5.245GHz

Noise Figure of Mixer at 5.32GHz

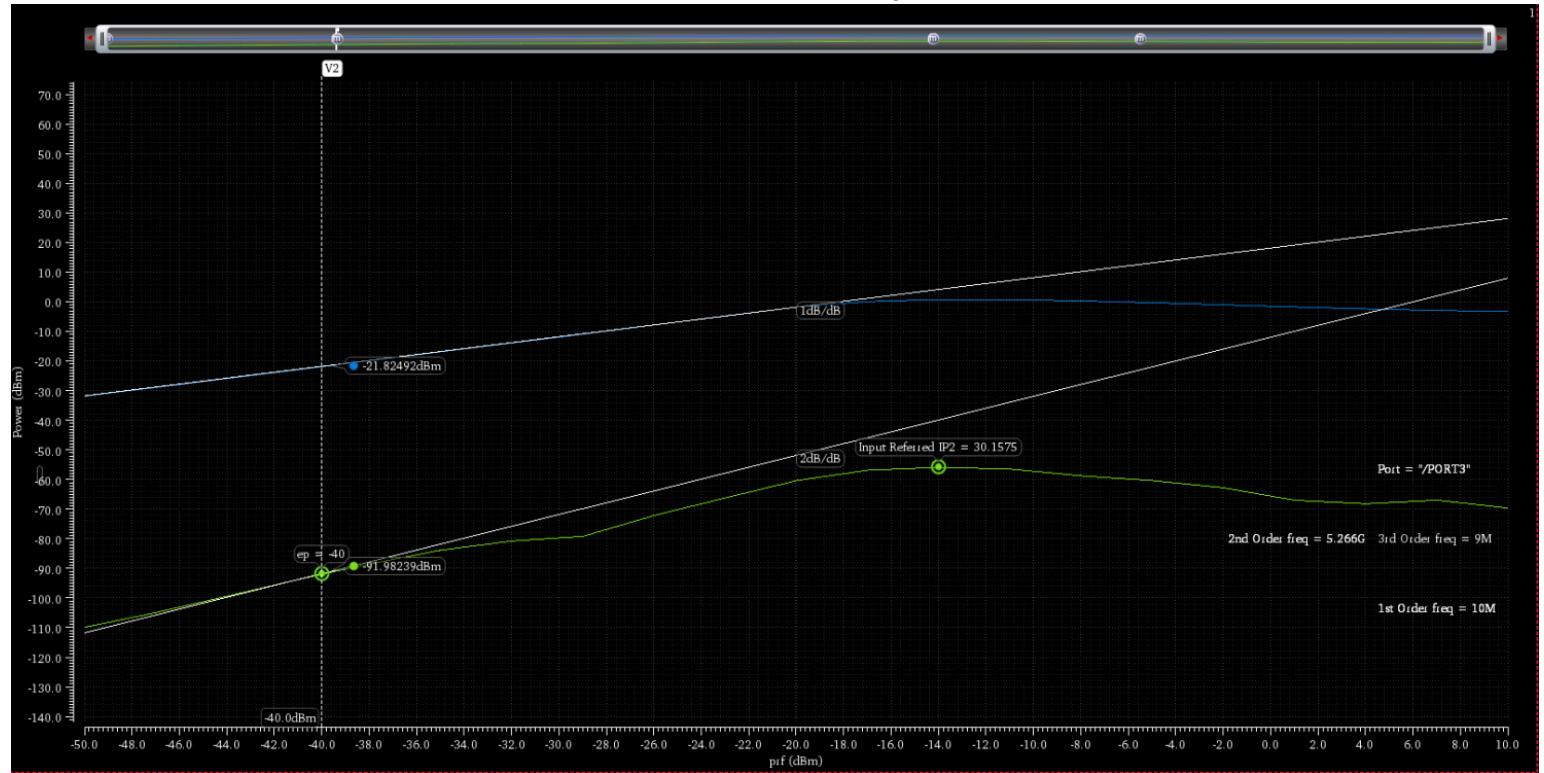
HB Noise curve is the same for all three frequencies



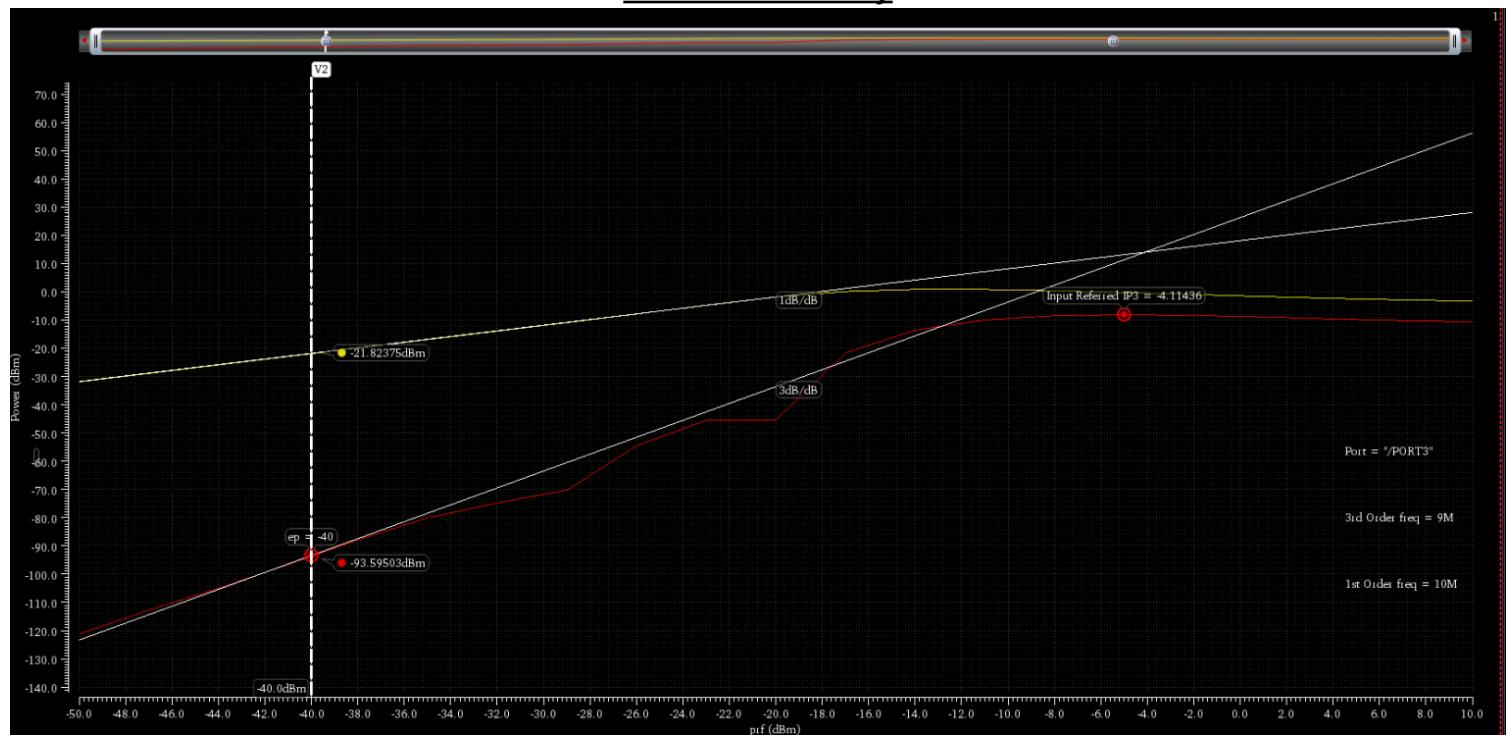
Integrated Noise Factor Behaviour



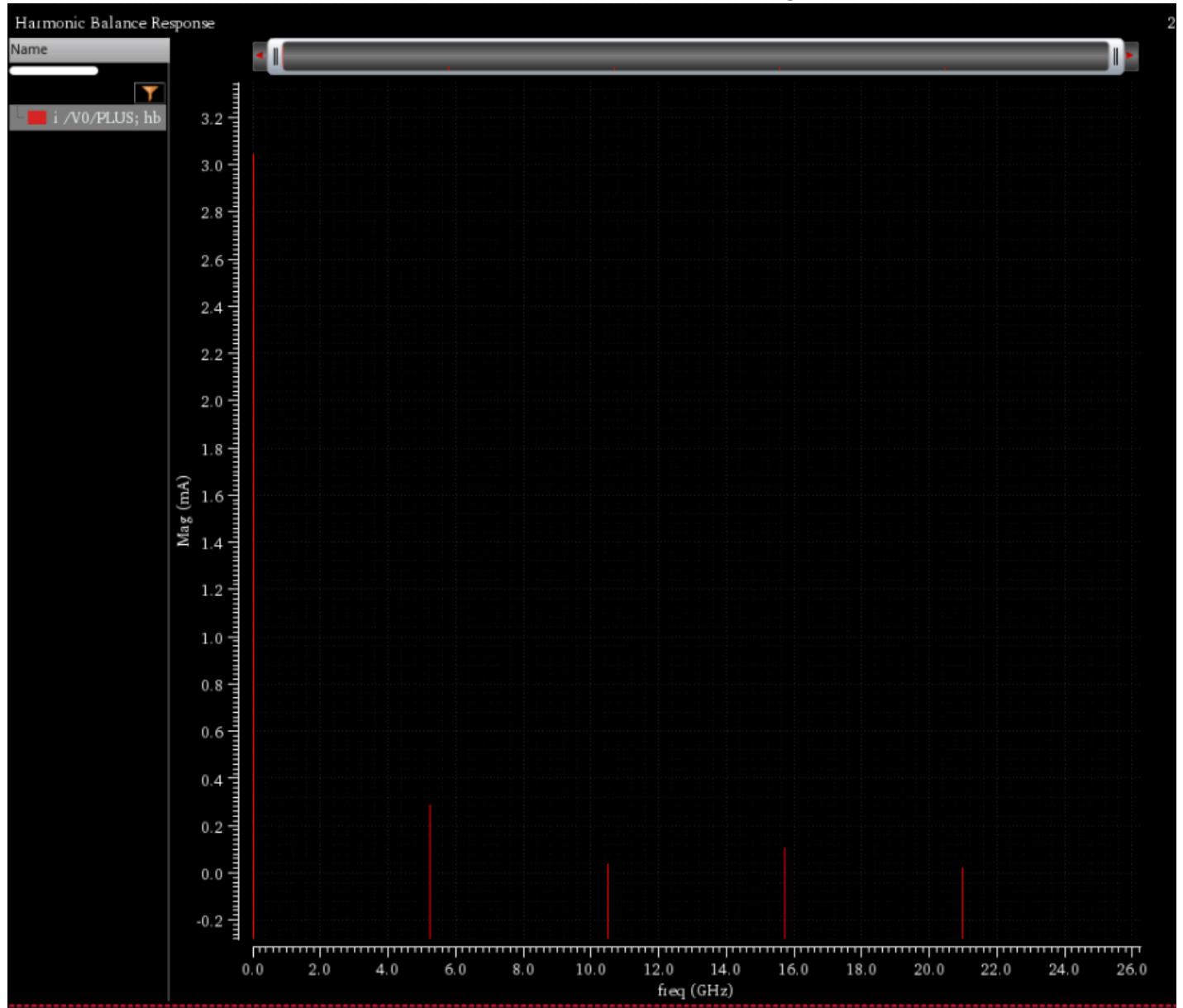
Mixer IIP2 Linearity



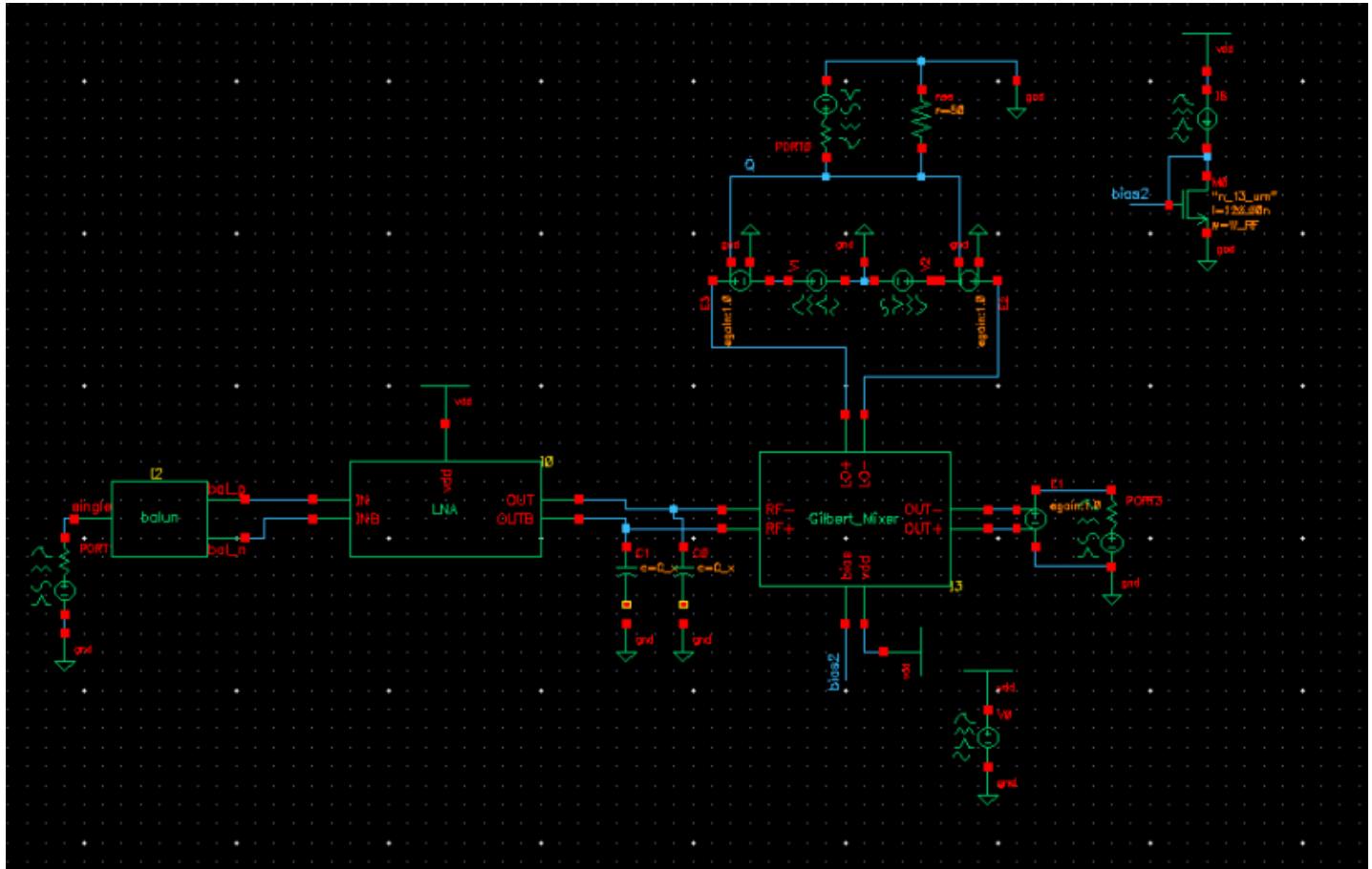
Mixer IIP3 Linearity



Mixer DC Power Consumption [Excluding Bias]



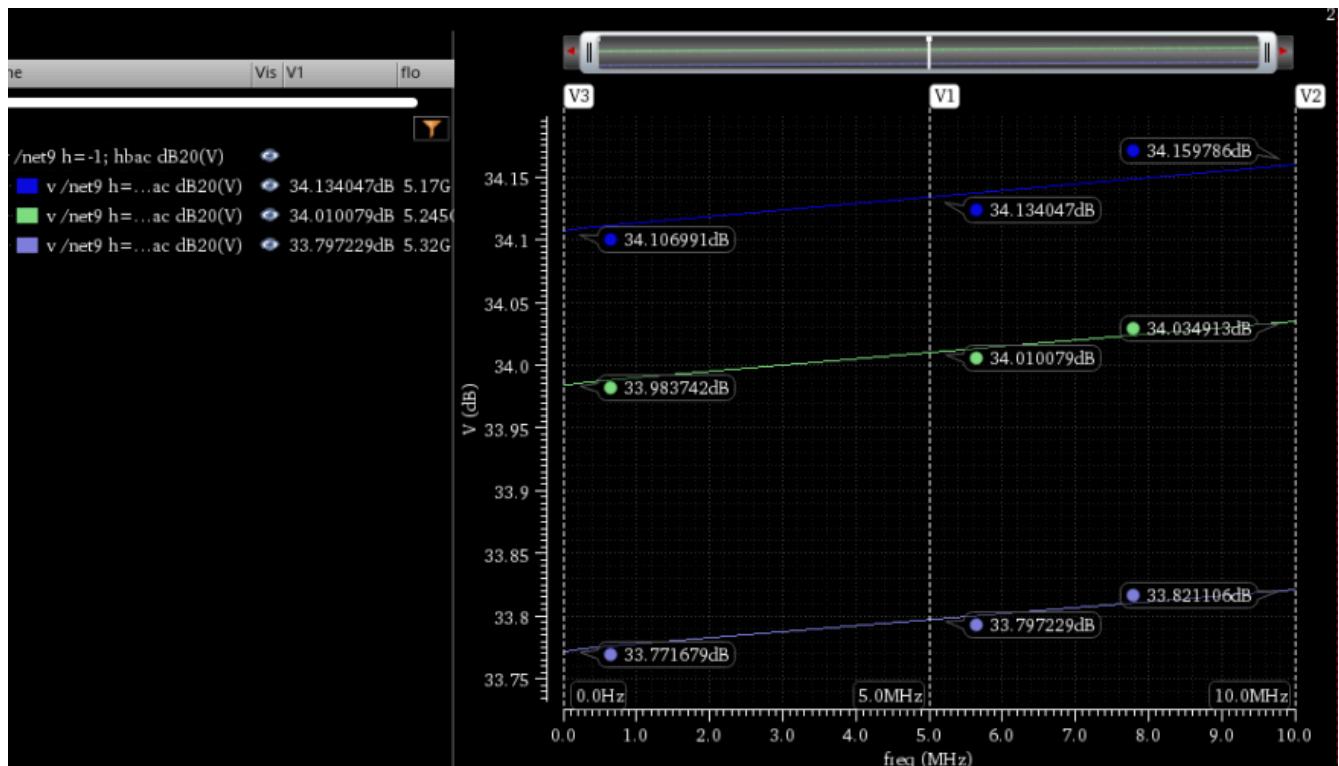
LNA + Mixer Testbench



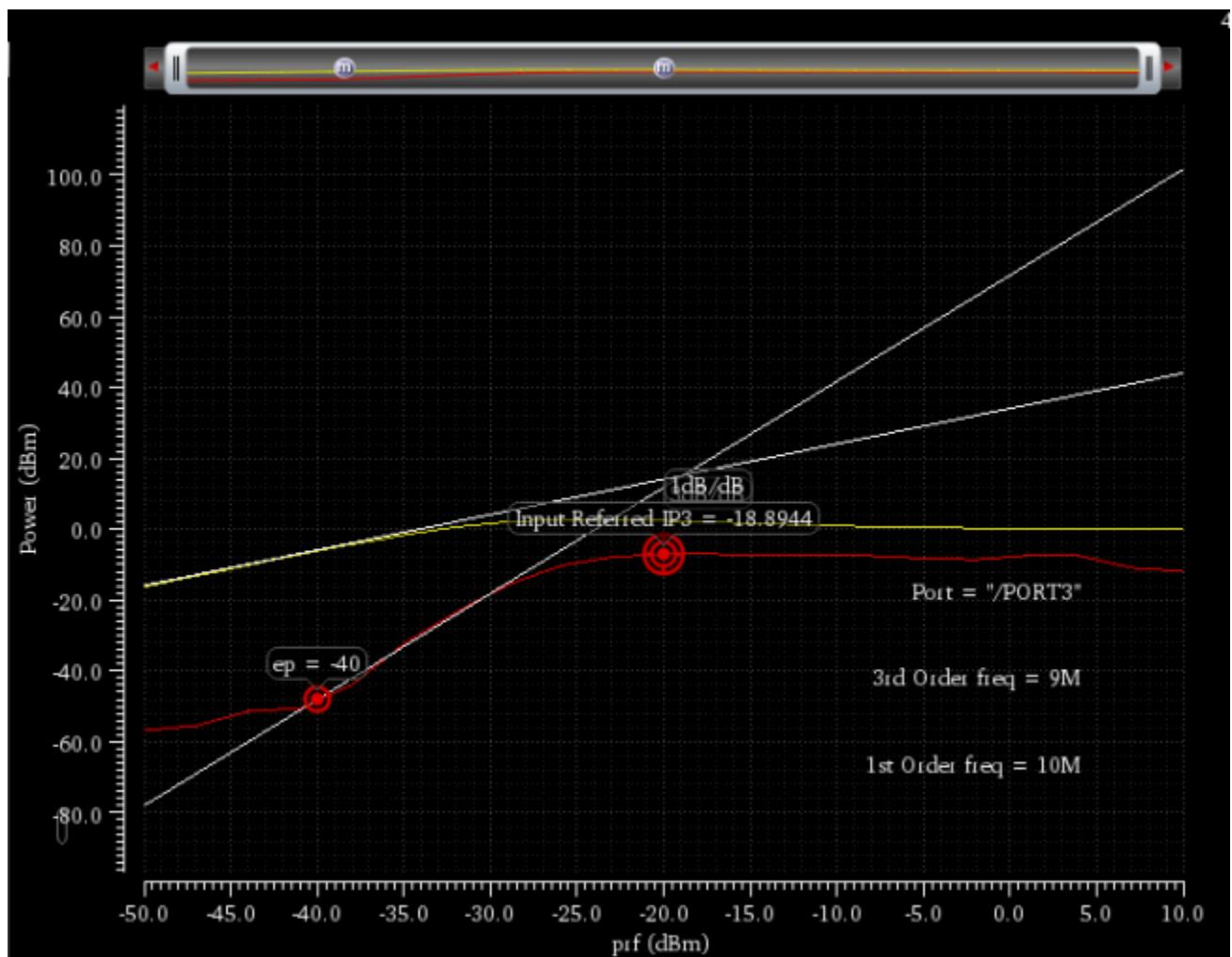
LNA + Mixer Conversion Gain at 5.17GHz

LNA + Mixer Conversion Gain at 5.245GHz

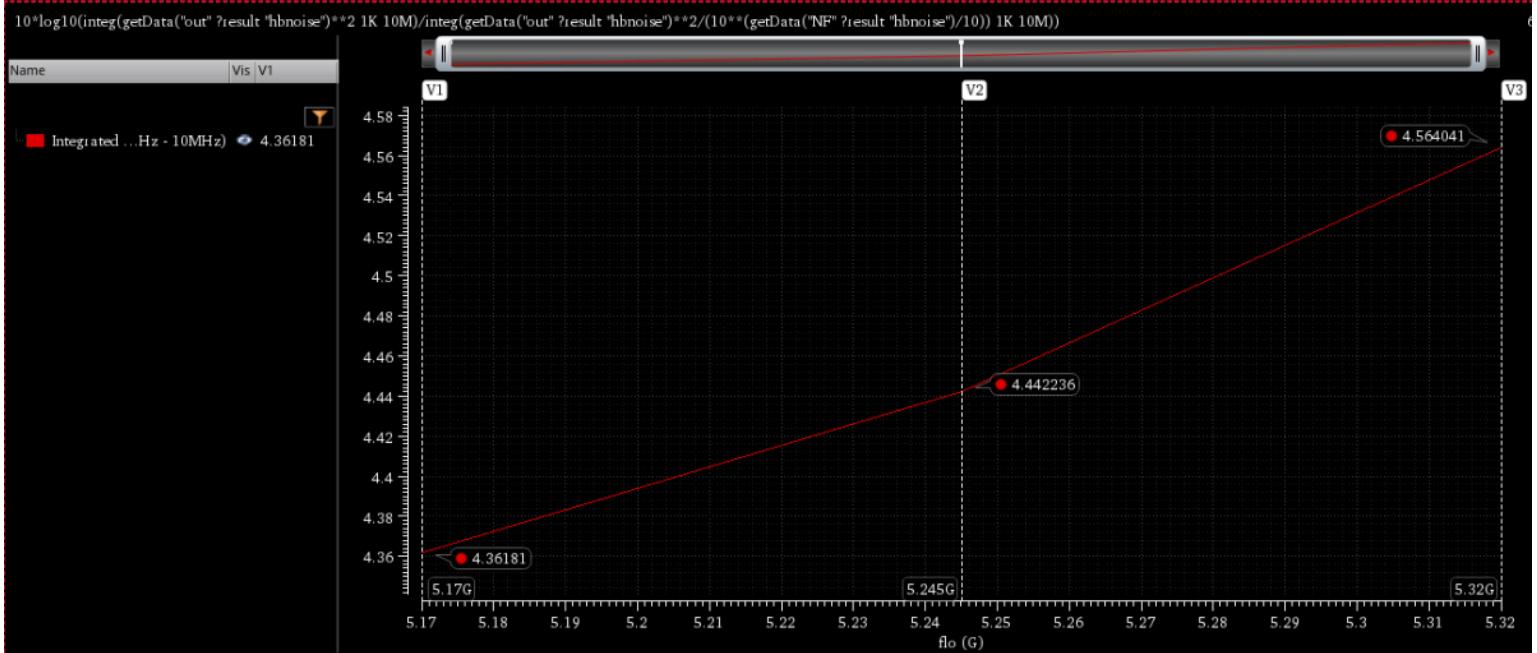
LNA + Mixer Conversion Gain at 5.32GHz



LNA + Mixer IIP3 Linearity



LNA + Mixer Noise Figure at 5.17GHz
LNA + Mixer Noise Figure at 5.245GHz
LNA + Mixer Noise Figure at 5.32GHz



LO Waveform Characteristics

Characteristics taken are (for generalized manner, as flo varies for various analysis):

- Frequency: 5.245GHz
- Time period: 190ps
- Delay time: 0s (for I Lo signal), 47.5ps (for Q Lo signal)
- Pulse Width: 76ps
- Rise/Fall Time: 19ps

Path to the Project Files

~/cadence_project/RFIC

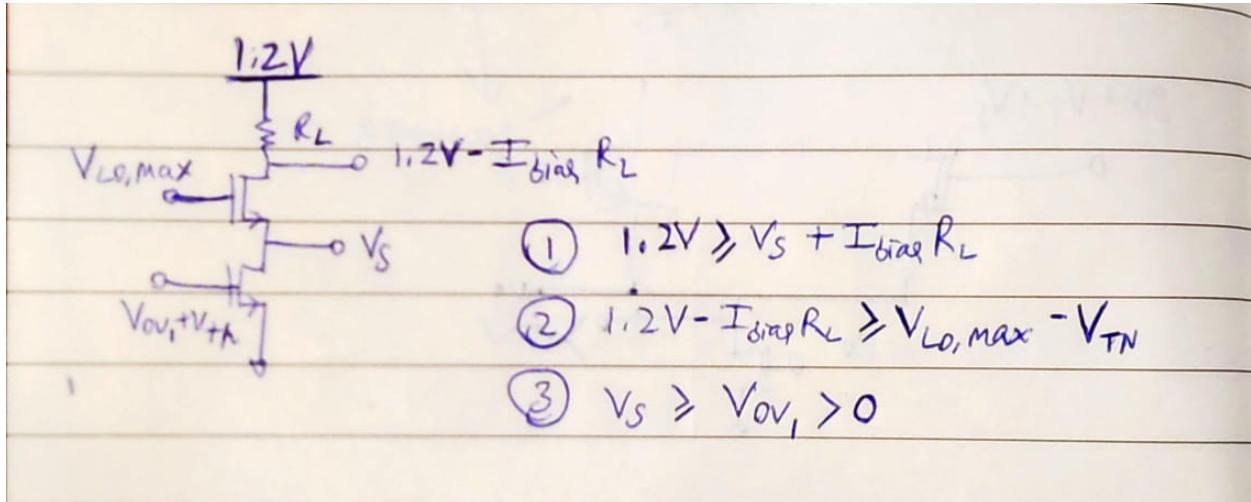
Design Procedure and Hand Calculations adopted follows in the next few pages:

2 Gilbert Cell Mixer

2.1 Hand Calculations

2.1.1 Setting Overdrive Voltages and Headroom using Gain Specification

From the VCO Project document, we can estimate the V_{LO} to swing between 0.2V and 1V. Thus the Overdrive voltage of the ON transistor will be $V_{LO,max} - V_{tn} = 1V - 0.4V$



In the above diagram, if we make sure V_s is set right in between the linear region bounded by the swing limits and $1.2 - I_{bias}R_L$ lies within its swing limits, we will get a good IIP2 and IIP3 response.

$$0 \leq V_{OV1} \leq V_s \leq 0.6V$$

To keep Headroom to a good amount, let's choose it to be 0.4V, because this will work even if the VCO goes upto 1.2V. So we have

$$I_{bias}R_L = 0.4V$$

Now we decide overdrive such that the MOSFETs still lie in a fairly linear region.

$$V_{OV1} = 0.1V$$

We check if the gain specification will be met using these values before we proceed and tune it if not:

$$\frac{2I_{bias}R_L}{V_{OV1}} > 10$$

So we tune it a little:

$$I_{bias}R_L = 0.416V$$

$$V_{OV1} = 0.084V$$

$$V_s = 0.516V$$

2.1.2 Decision of g_m , R_L & I_{bias} from Noise Factor

The below are the constraints we have on g_m , R_L & I_{bias}

$$\text{Noise Factor} = 1 + \frac{\pi^2}{4} \left(\frac{2}{g_m^2 R_L R_S} + \frac{\gamma}{g_m R_s} + \frac{2\gamma I_{bias}}{\pi V_{LO} g_m^2 R_L^2 R_S} \right) \leq 10^1$$

For typical values we can club the whole expression to be very crudely say:

$$\frac{2}{g_m R_S} \leq 4.05$$

$$g_m > 9.8mS$$

So we set R_L such that $g_m = 10mS$, this gives a good R_L such that this assumption that the middle term dominates over others works. So we have:

$$R_L = 986\Omega$$

$$I_{bias} = 422\mu A$$

2.1.3 Widths

The decisions above dictate Width already.

$$W_{g_m} = 25\mu m$$

It's a good idea to make the LO transistors wider, this gives it more drive strength in comparison to the parasitics added by the RF transistors

$$W_{g_m} = 26.2\mu m$$

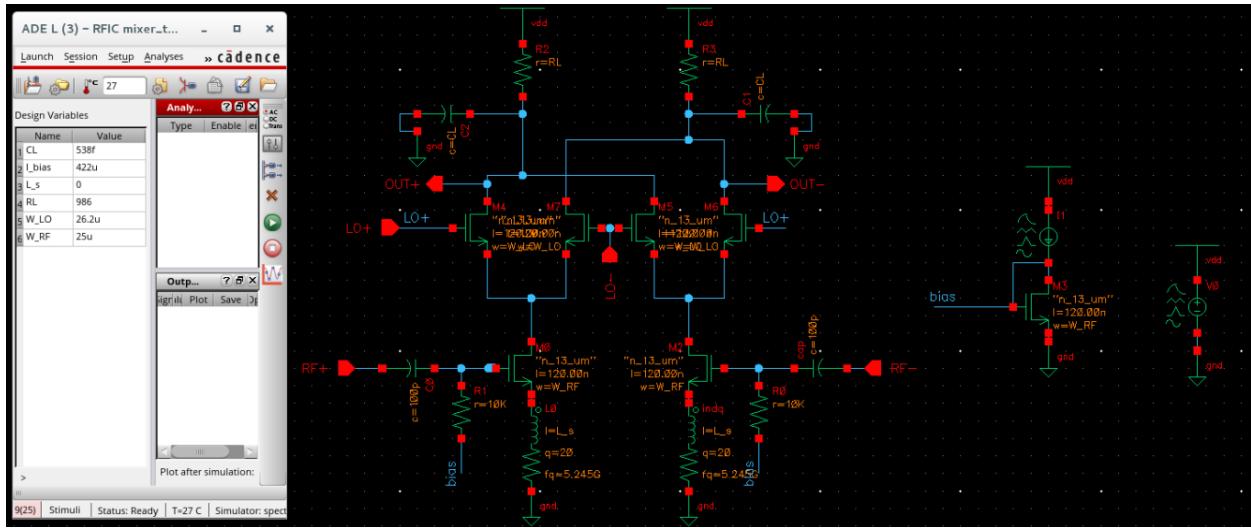
2.1.4 Capacitors to filter the LO fundamental at output

We can realize a low-pass to cut anything beyond about 300MHz which can remove all the harmonics of LO that might feedthrough.

$$\frac{1}{2\pi R_L C} = 300 \cdot 10^6$$

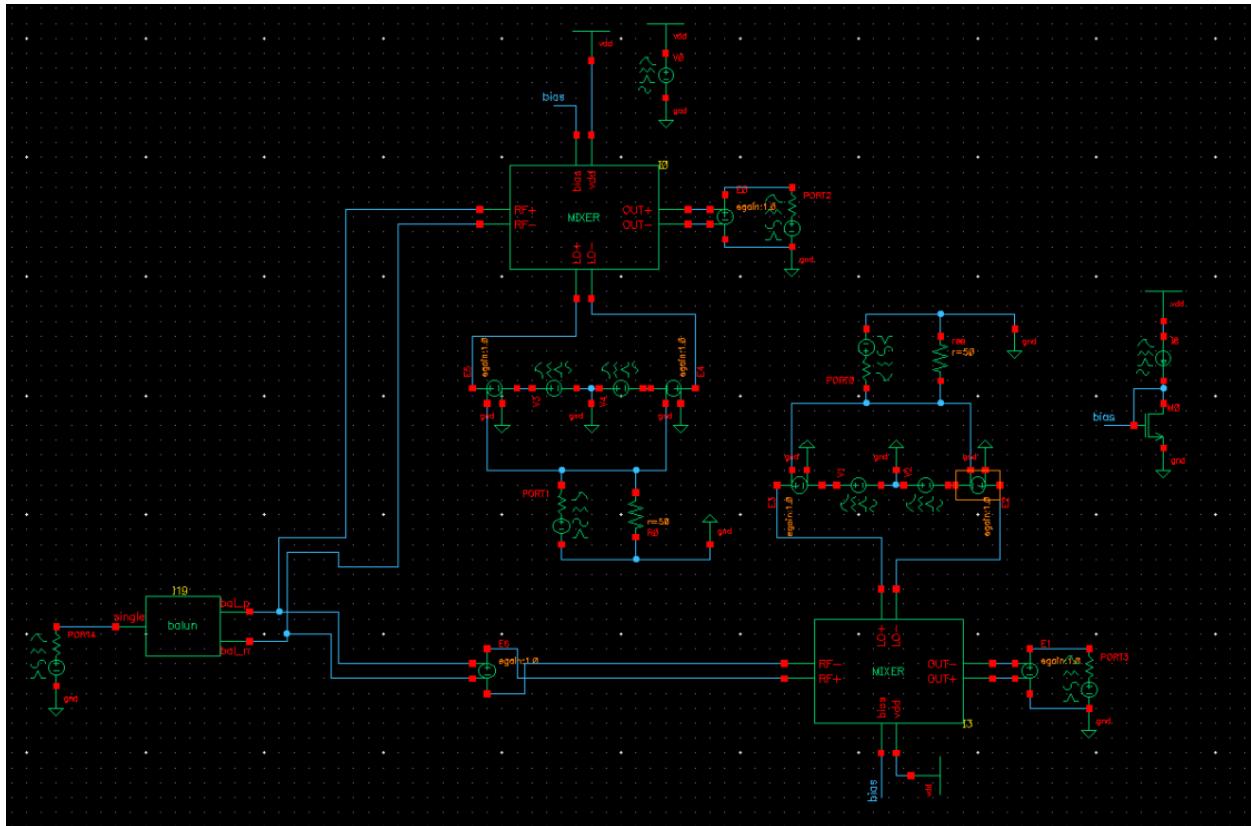
$$C = 0.538pF$$

2.1.5 Schematic after Hand-calculations



2.2 Simulations & Fine-Tuning

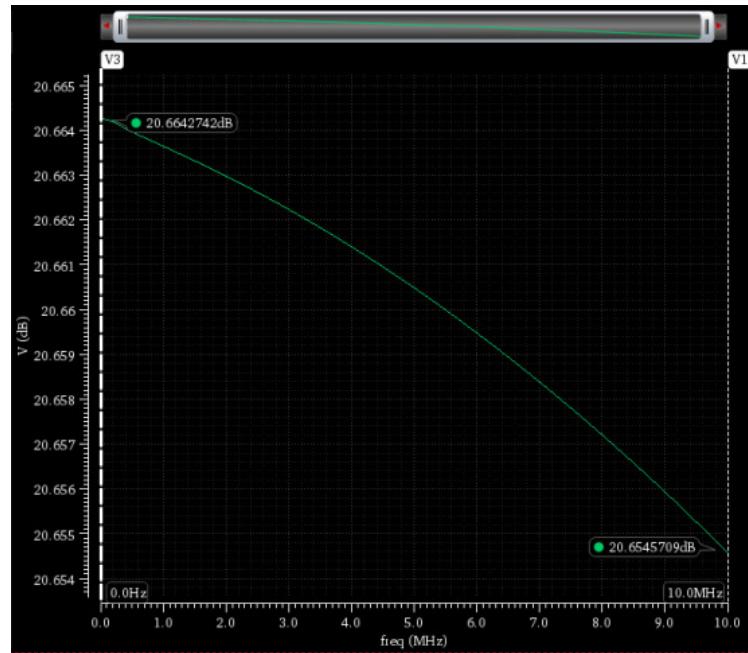
2.2.1 Testbench



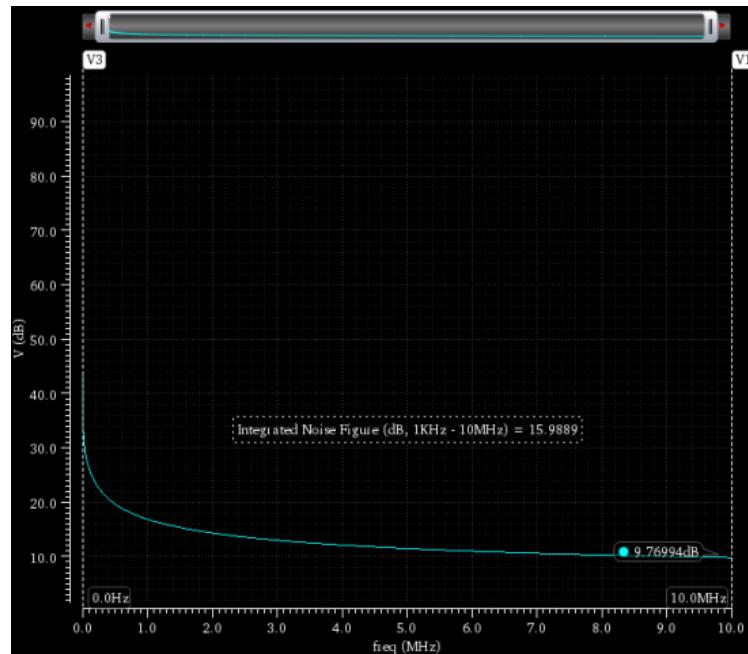
2.2.2 Initial set of simulations

After the first set of simulations using the hand-calculated values, it was found that the gain achieved overshot what we aimed for by a large margin but the noise center came out to be much worse.

Gain plot:



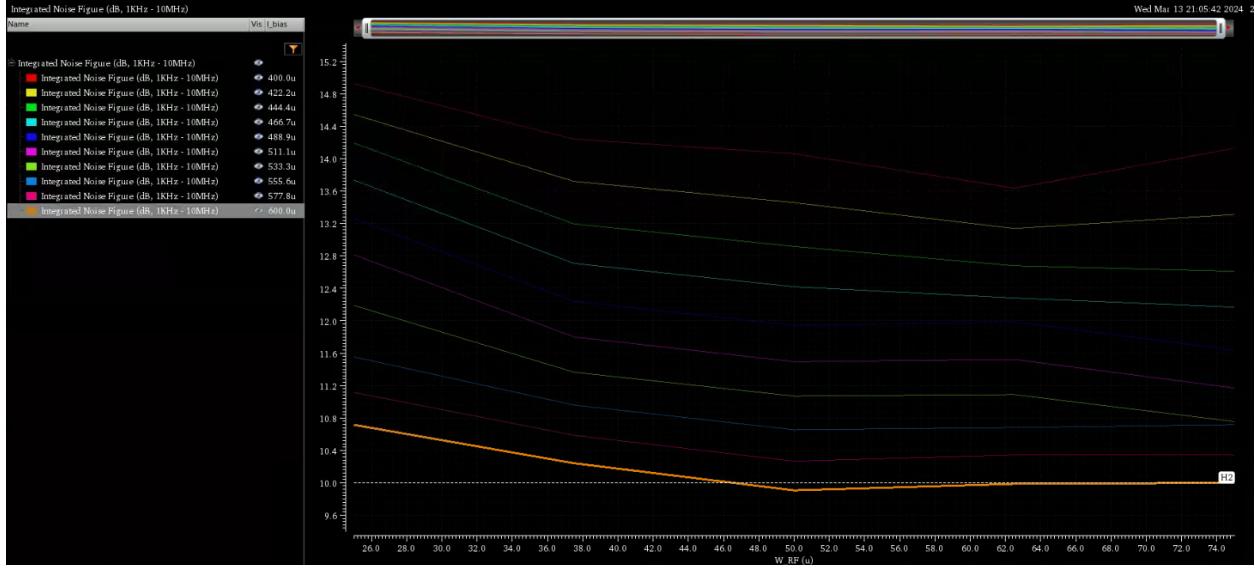
Noise Plot:



Linearities came out to be good enough.

2.2.3 Fixing the Issues

For our swing of LO we will be able to accomodate a larger $I_{bias}R_L$ than this. And in that case, we can increase the I_{bias} and see so that this increases the g_m which will bring down the noise factor.



This $I_{bias}R_L$ would still keep the MOSFET within a linear region (since threshhold for a wider 130nm MOSFET is slightly more than 0.45V, 0.4V is for a minimum sized MOSFET)

Further we can do some additional sweeping and optimize more:



We stick to 650 so that we still keep the above MOSFET well above Triode

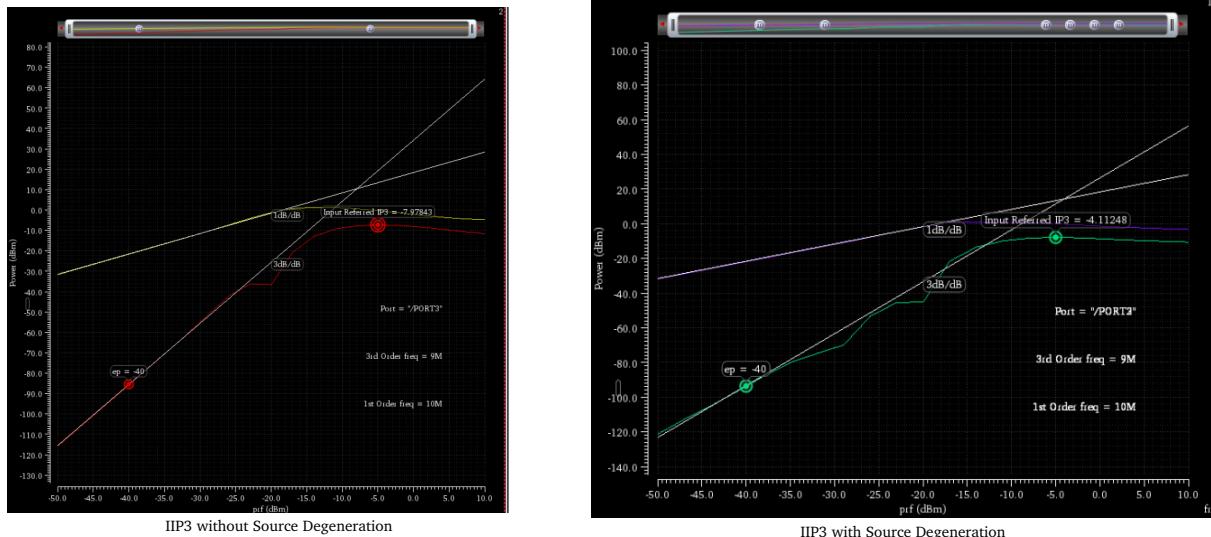
$$I_{bias} = 667\mu A \quad R_L = 900\Omega$$

2.2.4 Source Degeneration

With the original hand calculations, IIP3 came out to be -4dBm, but after the tuning above it have some down to -9dBm. We have a fairly high gain already, we can degenerate the source a little to get better linearity. We also decrease the widths, the widths don't contribute as much to the other specs as bias current or resistor did.

$$W_{RF} = W_{LO} = 45\mu m \quad L_s = 0.1nH$$

This gives an NF = 6dB, IIP3 = -4dBm, Conversion Gain = 18dB. Thus we will proceed with these



2.3 Final Values

