Rishi Nandha Vanchinathan

https://rishinandha.github.io/ | rishinandhav@smail.iitm.ac.in

EDUCATION

Indian Institute of Technology, Madras (IIT Madras) Jun 2026 (expected)

Integrated Masters (B.Tech + M.Tech) in Electrical Engineering

CGPA: **8.93**/10 (As of 23 Nov 2025)

Thesis: CMOS RF Front-End for Wide-band Same-Channel Full-Duplex at 7 GHz

Courses: Devices for AI and Neuromorphic Computing, Digital IC Design, Analog IC Design, RF IC Design

Tools:
- Circuit Design: Cadence Virtuoso, EMX, Genus, Innovus
- System Design: Cadence Allegro, OrCAD, Ansys HFSS
- Deep Learning: PyTorch, HuggingFace, LangChain

CONFERENCE PRESENTATIONS & CHIP TAPE-OUTS

[1] *"Wide-band Full-Duplex Transceiver at 7 GHz in CMOS 65nm"* – expected MPW submission for tape-out in Early Feb 2026 (Dec. 2024 - ongoing)

[2] *"Multi-channel TeraHertz System"*, exhibited at *Indian Mobile Congress (IMC) 2024*, New Delhi, India, Oct. 2024.

RESEARCH EXPERIENCE

Wide-Band Same-Channel Full-Duplex Transceiver Chip at 7GHz Dec 2024 - Ongoing

Supervisor: Prof. Sankaran Aniruddhan ICS Group, IIT Madras

- Demonstrating single-antenna full-duplex at 7 GHz with 300 MHz (single-sided) bandwidth by extending the approach of Kumar et al. (TCAS-I, Oct-2018), originally reported at 2.4 GHz with 10 MHz bandwidth.
- Responsible for complete design flow including schematic, layout, synthesis, place-and-route and testing
- Designing a network to mimic an antenna's spiral Z-smith profile; projected wideband isolation of 42 dB

High Speed Clock Distribution Boards for 5G-NR & 6G Research May 2023 – Nov 2024

Supervisor: Prof. Radha Krishna Ganti 5G Testbed, IIT Madras

- Contributed as the RF clock boards designer for supporting 5G/6G research activities in the lab
- Designed multi-PLL clock trees for physical-layer data protocols in the group's 5G-NR and 5G+ RRHs
- Designed and assembled an RF board to provide reference clocks for TeraHertz Systems; supplied clocks at 100s of MHz for the lab's demonstration of a 270 GHz P2P Wireless Link at Indian Mobile Congress 2024.

TEACHING EXPERIENCE

Teaching Assistant: Devices for AI & Neuromorphic Computing Aug - Nov 2025

EE6347 Course Instructor: Prof. Bhaswar Chakrabarti IIT Madras

- Delivered supplementary lectures on designing and simulating silicon neurons such as the Adaptive Low-Power Integrate-and-Fire (Indiveri, 2003) and the Tau Cell Neuron (van Schaik et al., 2010).
- Conducted tutorials on compact modeling and simulation of FeFET, RRAM, and FeCAP devices
- Demonstrated simulation of synapses made of 1T-1R cells and DenRAM (Payvand et al., 2024) cells.

TECHNICAL PROJECTS

Quantization-aware Neural Network for Inference with Passive RRAM Synaptic Array Aug - Oct 2024

EE6347 Course Instructor: Prof. Bhaswar Chakrabarti IIT Madras

- Extended the course project on using passive RRAM arrays for inference of a neural network, by replacing the post-training quantization with training a quantization-aware neural network using sigmoid weights

Physical Design of a Digital Decimation Filter for a Delta-Sigma ADC in 180nm Nov - Dec 2025

Inter IIT Contest 2025, Problem Statement promoted by ISRO (Indian Space Research Organisation) IIT Madras

- Register Transfer Logic, Synthesis, Place-and-Route and Static Time Analysis of a decimation filter for a 20-bit ADC with 19 ENOBs over a 1 kHz bandwidth with simulated data from a 4-bit CIFF delta-sigma loop

- Implemented asynchronous FIFOs for clock domain crossings and a scheduled multiplier for MAC

8-Bit Carry-Save Multiplier With Pipelining in CMOS 22nm Sep - Nov 2023
EE5311 Course Instructor: Prof. Janakiraman Viraraghavan IIT Madras

- Designed custom transistor-level layout for a multiplier operating at 2.8 GHz with 0.32 ns critical delay
- Implemented pipelining using C2MOS D flip-flops, improving maximum frequency by 67%

Fully Differential OpAmp with Common-Mode Feedback in CMOS 130nm Feb - Apr 2024
EE5320 Course Instructor: Prof. Nagendra Krishnapura IIT Madras

- Designed a 2-stage Miller op-amp in 130nm CMOS with a phase margin of 72 degrees
- Designed a common-mode feedback with 14 MHz bandwidth and 80 degrees phase margin

Retrieval-Augmented Chatbot Assistant with a Locally Hosted LLM Nov - Dec 2024
AI Club, Centre For Innovation (Student-Run Innovation Centre, IIT Madras) IIT Madras

- Built a QA assistant bot that retrieves context through semantic search with BERT embeddings
- Utilized a zero-shot classification of user task, KV token caching and generation with a local T5 LLM

AWARDS, HONOURS & FUNDING

Research supported by Ministry of Electronics & IT (MeitY), India Fall 2025
Master's Thesis tapeout, supervised by Prof. Sankaran Aniruddhan (PI).

Lab Group supported by Department of Telecommunications (DoT), India Fall 2024
Undergraduate research at the IITM 5G Testbed, supervised by Prof. Radha Krishna Ganti (PI).

Institute Day Certificate of Merit, IIT Madras Apr 2022
Awarded for securing All India Rank 332 in IIT-JEE Advanced 2021.

Gold Medal, Online Physics Olympiad (OPhO) Jun 2021
For placing 6th globally among international participants

INDUSTRY EXPERIENCE

Software Engineering Internship May - Jul 2025
Microsoft [Windows + Devices] Hyderabad, India

- Developed an MCP server enabling Agentic AI workflows to interface with legacy software components.
- Contributed to the open-source MCP TypeScript SDK, focusing on automation of engineering tasks

Open-Source Contribution to IBM Qiskit Feb - Apr 2025
Supervisors: Dr. Dhinakaran Vinayagamurthy (IBM), Prof. Chandrashekar Lakshmi Narayanan (IITM)

- Contributed a quantum dataset for benchmarking Variational Fast-Forwarding (Model introduced in 2020)
- Exhibited fast-forwarding of molecular hamiltonians with a Jordan–Wigner mapping on NISQ run-times

LEADERSHIP & VOLUNTEERING

Executive Head & Technical Lead Apr 2023 - Mar 2024
Sahaay - Social Innovation Club, IIT Madras

- Directed five student projects in animal welfare, assistive technology, and agricultural technology.
- Mentored student teams on edge inference of neural networks such as YOLO and CNNs for assistive tech
- Conducted workshops for 54 freshmen on transfer learning, data augmentation, and model evaluation.

Department Committee Representative Nov 2021 - Jun 2025
Electrical Engineering Department, IIT Madras

- Assisted the Head of Department with curriculum rearrangement; Represented undergrads at town halls
- Assisted the Dean of Students of IIT Madras on measures & initiatives for women's safety in campus

Mobile Application for Animal Distress Call Response Aug 2024 - Present

- Collaborating with members from Animal Welfare Board of India and Blue Cross of India for developing a full-stack application for decentralizing animal distress call response