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Research Statement

Motivation and Vision: To reform the current paradigm of computing, to reduce every watt our deep learning models burn, is indispensable to the pursuit of fair and accessible technology today. In a world constrained by resources, powering such models with a disproportionate amount of energy is unjust. The desire for justice in technology drives my focus on in-memory and neuromorphic computing. My research interests can be broadly framed as:

1. Neuromorphic accelerators that reduce power demands for both edge inference and large-scale server-side deployment.
2. Analog/Mixed-Signal In-Memory Computing structures for such accelerators

Grounded in an RF IC design background, I also am excited to explore neuromorphic computing from an RF-informed and RF-inspired perspective for addressing energy bottlenecks

Origin of Interest: In 2023, as part of a five-member team, I co-developed a pre-incubated assistive mobility device for visually- and auditorily-impaired individuals navigating complex environments in India. Our system relied on deep learning inference at the edge. However, the power consumption incurred in the current paradigm of GPU-based inference made it infeasible to meet our energy budget. This firsthand challenge motivated me to explore computing paradigms that can enable efficient edge intelligence without compromising accessibility or performance.

Exploration of Emerging Paradigms: To pursue this goal, I explored emerging paradigms of computing through coursework at IIT Madras. As part of a collaboration with IBM Research, India, our team contributed quantum computing datasets to the IBM Qiskit framework.

I also undertook the course Devices for AI and Neuromorphic Computing (offered by Prof. Bhaswar Chakrabarti), which introduced me to RRAM/FeFET-based non-volatile memories and spiking neuron circuits. For my project, I investigated 1-bit passive RRAM arrays for neural inference, training hardware-aware networks as a replacement for post-training quantization.

I currently serve as a teaching assistance in the next offering of the course. These experiences have collectively strengthened my belief that in-memory and neuromorphic computing can reform the energy landscape of AI.

Foundation in RF IC Design: Coming from a background in RF integrated circuit design, I have learned to operate at the edge of technological limits: perspectives I aim to carry forward in my approach towards energy-aware architectures. My ongoing master's thesis, under the supervision of Prof. Aniruddhan Sankaran, involves the tape-out of a 7 GHz transceiver in 65 nm CMOS technology. Being responsible for the complete design flow, I have gained hands-on experience across specification, simulation, layout, verification, and measurement. This end-to-end exposure has provided me with the design discipline I'd like to utilize in designing energy-efficient neuromorphic chips.

Future Direction: My pursuit of accessible technology and my experiences drive me toward pursuing doctoral studies with focus on energy-aware analog design for neuromorphic and in-memory systems. I look forward to advancing this vision of energy efficiency.