

## SKILLS

**SOFTWARE** | Cadence Virtuoso, Spectre, OrCAD & Allegro • Keysight ADS • ANSYS Electronics  
• Electric VLSI • LTSpice • Xilinx Vivaldo    **LANGUAGES** | Python • C • C++ • MATLAB • Verilog  
**HARDWARE** | ZCU102 FPGA • Tiva C Evaluation Board • Arduino • Raspberry Pi • Jetson Nano  
**OTHER SKILLS** | Sound Synthesis • Digital Audio De-Noising • PCB Soldering • Deep Learning

## PROFESSIONAL EXPERIENCES

**R&D OF A 7GHZ CMOS 65NM FULL DUPLEX TRANSCEIVER<sup>5</sup>** | CADENCE VIRTUOSO

May 2024 – Current | Research Project, Guide: Prof. Aniruddhan Sankaran

- Developing a **single-channel full-duplex transceiver** improvising Kumar et al. (TCAS1 2018) design
- Designed & simulated a 3-terminal capacitance bridge in TSMC 65nm process with **>50dB isolation**
- Researching on improving RX chain with **Balun Low Noise Amplifier & active mixer** architectures

**RESEARCH ASSOCIATE AT 5G TESTBED** | APLLS, DPLLs<sup>7</sup>, RF PCB, ORCAD & ALLEGRO

May 2023 – Current | 5G Testbed, IIT Madras. Funded by GOI<sup>8</sup> Department of Telecommunications

- Designed an **IEEE1588 Compliant RF Clock Structure** to synchronize data interfaces & global clock
- Reviewed literature on modern **Advanced-5G & 6G RRHs** & encoding techniques in data interfaces
- Designed & **Tested a Multi-PLL Architecture** for SyncE, IEEE-1588, and JESD204B Synchronization
- Achieved **Return Loss of -26dB, Insertion Loss -0.1dB** & Delay-Tuning  $\pm 6\text{ps}$  in the Fabricated PCB
- Integrating the design with a new RRH<sup>6</sup>; Attended the **National Communications Conference 2024**

## TECHNICAL PROJECTS

**DESIGN OF A CMOS 120NM ANALOG FRONT END FOR 5GHZ WLAN** | VIRTUOSO

Feb - Apr 2024 | Course Project. Guide: Prof. Sankaran Aniruddhan

- Designed a **Cascoded Common-Source LNA** with In-Band  $S_{11} < -30\text{dB}$ ,  $NF < 1.9\text{dB}$  &  $\text{Gain} > 32\text{dB}$
- Designed an **Active Gilbert Cell Mixer** with In-Band  $\text{Gain} > 18.1\text{ dB}$ ,  $\text{IIP3} = -4.1\text{ dBm}$  &  $NF < 6.1\text{ dB}$
- Designed a **Cross-Coupled VCO** with  $V_{pp} > 2.8\text{V}$ ,  $1\text{MHz}$  phase noise  $< -123\text{ dBc/Hz}$  &  $\Delta K_{VCO} < 3\%$
- Designed a **Cascoded Power Amplifier** with  $P_{1dB} > 11.4\text{ dBm}$  & **AM-PM Deviation at  $P_{1dB} < 3.4^\circ$**

**DESIGN OF A DIFFERENTIAL MILLER OPAMP** | LTSPICE, COMMON MODE FEEDBACK

Feb – Apr 2024 | Course Project. Guide: Prof. Nagendra Krishnapura

- Designed OpAmp of desired Load Capacity, Bandwidth & Phase Margin with **Current-Mode CMFBs<sup>12</sup>**
- Simulated design for Noise PSDs<sup>13</sup>, Slew Rate, Swing Limits, & CMFB Gain Crossover & Phase Margin

**VACUUM TUBE TRIODE GUITAR PEDAL** | HANDMADE PROTOTYPE, CLASS-A AMPLIFIER

Nov 2023 – Jan 2024 | Self Project

- Designed **2-Stage Class-A Amplifier with 12AT7 Tube**; chose DC Points for Max Harmonic Distortion
- **Soldered circuit by hand**, Verified **Power-Integrity** & Tested the Pedal with a Guitar & Hi-Z Speakers
- **Rediscovered F.Langford(1934)'s Solution to In-Band DC-DC Converter Feedthrough** with LC Shunt

**LAYOUT & SIMULATION OF A CMOS 22NM CARRY SAVE MULTIPLIER** | ELECTRIC VLSI

Aug – Dec 2023 | Course Project. Guide: Janakiraman Viraraghavan

- Designed **Layout** of a 8-Bit CSM operating at **2.8 GHz Clock & 0.32ns simulated Propagation Delay**
- Identified the **Critical Path Delay**, Simulated and Optimized the delay by **scaling the Standard Cells**
- Achieved a **67% increase in Max Frequency & 21% decrease in Delay** by **Pipelining** using Flipflops

**KRLS<sup>9</sup> FOR SELF INTERFERENCE CANCELLATION IN MIMO ANTENNAS** | PYTORCH

Aug – Nov 2023 | Course Project. Based on C. Auer et al. 2021

- Implemented the Kernel Method proposed by C. Auer et al. for **Noise Cancellation in 5G Antennas**
- Compared how different sparsification methods respond to **sudden changes in the Noise Profile**
- Achieved **>30dB Isolation in 32-Channel Array** by Ensemble Parallelization using PyTorch Tensors

## POSITIONS OF RESPONSIBILITIES

**EXECUTIVE HEAD & SOFTWARE LEAD** | SAHAAY - SOCIAL INNOVATION CLUB

Apr 2023 – Mar 2024 | Centre for Innovation, IIT Madras

- Executed **5 Socially Relevant Projects** impacting Animal Welfare, Agriculture Tech. & Assistive Tech.
- **Reformed club's PR<sup>11</sup>** to see a **growth** in member & application count of about **400% & 900%** resp.
- **Reformed the Club Structure** & formalized member recruitment & project management practices

## MENTORSHIP EXPERIENCE

**DEPUTY COORDINATORS WORKSHOP** | SAHAAY - SOCIAL INNOVATION CLUB

- **Trained 54 Freshmen** in Product Design & Development, Deep Learning, Electronics & Fusion 360
- Conducted Sessions on **CNNs, Transfer Learning, Data Augmentation & Model Evaluation Metrics**
- Facilitated the Program to progress in a **Hackathon format** using our project AWS<sup>10</sup> as a Case Study



## EDUCATION

**IIT MADRAS**

**DUAL DEGREE (B.TECH + M.TECH IN ELECTRICAL ENGINEERING)**

**CGPA: 8.72 / 10**

2021 - 2026<sup>#</sup>

**CLASS XII**

**CBSE, MATHEMATICS & COMPUTER SCIENCE**

**Score: 94.0 %**

2021

**CLASS X**

**CENTRAL BOARD OF SECONDARY EDUCATION**

**Score: 90.8 %**

2019

## SCHOLASTIC ACHIEVEMENTS

**AIR<sup>1</sup> 332 IN JEE ADVANCED 2021**

Among 0.14 million candidates

**TOP 35 AIR<sup>1</sup> IN CMI ENTRANCE 2021**

Thereby qualifying for Admission in  
Chennai Mathematical Institute (CMI), India

**SECURED Gold Tier IN OPHO<sup>2</sup> 2021**

By placing 6th among 800 Teams from Physics  
Communities around the Globe

**PLACED 7th IN PHYSICS BRAWL 2021**

Organized by FYKOS, Charles University, Prague

## COURSEWORK

**GRADUATE**

RF IC Design  
Analog IC Design  
Digital IC Design  
Multirate Digital Signal Processing  
Adaptive Signal Processing<sup>5</sup>

**UNDERGRADUATE**

Analog Systems Lab<sup>5</sup>  
Digital Systems Lab  
Fundamentals of Audio Engg.<sup>@</sup>

## INTERESTS

**GUITARIST & MUSICIAN** by hobby.

Graduated Trinity Grade 3 in Piano and Grade 4 in Theory. Played with IIT Madras Band and won 1st in IIM-B's Unmaad, 3rd in IIT-B's Mood Indigo, Sold-out a live show with our Originals & Opened shows for Masala Coffee & Guitar Prasanna

**ULTIMATE FRISBEE** Reserve in Insti<sup>3</sup> Team

## VOLUNTEERING

**STUDENT LEADER** of Volunteer Group that aided Dean of Students & SLC<sup>4</sup> on Improving Safety Measures for Women On-Campus

**REPRESENTATIVE** of Students-View in the Academic Restructuring of the Elec. Engg. Curriculum for Batches 2023 Onwards

**MENTOR** for five Freshers as part of Saathi

**ANIMAL WELFARE** Enthusiast

#. Ongoing 1. All India Rank 2. Online Physics Olympiad @. Online \$. Highest Grade in Class 3. Institute 4. Student Legislative Council 5. Radio Frequency Integrated Circuit 6. Remote Radio Head 7. Analog PLLs & Nested Digital PLLs 8. Government of India 9. Kernel Recursive Least Squares 10. Automatic Waste Segregator 11. Public Relations 12. Common Mode Feedbacks 13. Power Spectral Density