



TAPEOUT/FABRICATION PORTFOLIO

- **FULL DUPLEXING 6G TRANSCEIVER IN TSMC65 GP** (Submitted for Fabrication)
- **HIGH-SPEED CLOCK SYNCHRONIZATION PCB** (Used by 5G Testbed on a 5G BBU)
- **GPS-SYNC CLOCK SYNTHESIS PCB** (Showcased in Indian Mobile Congress 2024)

SKILLS

CAD | Cadence Virtuoso • Spectre • Allegro • Innovus • Genus • Keysight ADS • Ansys HFSS • EMX
LANGUAGES | Verilog HDL • C • C++ • AVR Assembly • ARM Assembly • Python • Typescript • C#
OTHER SKILLS | Design Automation with Parameter Search • Deep Learning with Torch & CUDA
COURSES | Digital IC Design • RF IC Design • Devices for AI & Neuromorphic Computing • Analog IC

RESEARCH PROJECTS

R&D OF A FULL DUPLEX 6G TRANSCEIVER AT 7 GHZ

Jun 2024 – Current | Research Project, Guide: Prof. Aniruddhan Sankaran

- Designed a **single-antenna RX+TX** with on-chip duplexing based on Kumar et al.'s **TCAS1** design
- Designed a passive balun and **simulated the complete chip's electromagnetics** at 7GHz with EMX
- **Synthesized SPI registers** and initiated PnR for input matching and frequency divider calibration
- Achieved an **RX-TX Isolation of -50dB** in simulation. Design submitted for **tapeout in TSMC 65GP**

SOM CLOCK DISTRIBUTION FOR PHYSICAL LAYER PROTOCOLS

May 2023 – Nov 2024 | 5G Testbed, Funded by GOI⁵ Department of Telecommunications

- Designed an **IEEE1588 Compliant RF Clock Structure** to synchronize data interfaces & GPS clocks
- Designed & Tested a **Multi-PLL Architecture** for SyncE, IEEE-1588, and JESD204B Synchronization
- Achieved **Return Loss of -26dB**, Insertion Loss -0.1dB & **Delay-Tuning ± 6 ps** in the assembled PCB
- Achieve a **phase noise of -132dBc/Hz** at 100kHz offset for a 400MHz clock; showcased in IMC 2024

COURSE PROJECTS

IN-MEMORY COMPUTATION OF A NEURAL NETWORK WITH SYNAPTIC ARRAYS

Devices for AI & Neuromorphic Compute (Fall 2024) - Prof. Bhaswar Chakrabarti

- Implemented a neural network with **RRAM Crossbars for dense layers** and OpAmps for activation
- Introduced a hardware-aware soft-binary model to train ex-situ with minimal quantization error
- Demonstrated a reduction of quantization-induced errors <2% on **inference of about 640 images**

LAYOUT OF AN 8-BIT MULTIPLIER WITH PIPELINING IN CMOS 22NM

Digital IC Design (Fall 2023) - Prof. Janakiraman Viraraghavan

- Designed a Carry Save Multiplier operating at a 2.8 GHz Clock with a 0.32ns critical path delay
- Designed **C2MOS D-Flipflops for Clocked Pipelining** for faster operation & decreased race paths
- Achieved a 67% increase in Max Frequency & 21% decrease in critical path delay with pipelining

DESIGN OF AN RF FRONT END FOR 5GHZ WLAN IN CMOS 130NM

RF IC Design (Spring 2024) - Prof. Sankaran Aniruddhan

- Designed a Cascoded Common-Source LNA with In-Band $S_{11} < -30$ dB, NF < 1.9dB & Gain > 32dB
- Designed an Active Gilbert Cell Mixer with In-Band Gain > 18.1 dB, IIP3 = -4.1 dBm & NF < 6.1 dB
- Designed a Cross-Coupled VCO with $V_{pp} > 2.8$ V, 1MHz phase noise < -123 dBc/Hz & $\Delta K_{VCO} < 3\%$
- Designed a Cascoded Power Amplifier with $P_{1dB} > 11.4$ dBm & AM-PM Deviation at $P_{1dB} < 3.4^\circ$

PROFESSIONAL EXPERIENCES

SOFTWARE INTERNSHIP | MICROSOFT [WINDOWS + DEVICES]

May - Jul 2025 | Hyderabad, India

- Devised ways to interface existing programs with an LLM; Automated routines such as local setup
- Experience includes designing server-side for maintainability and testability with SOLID principles

LEADERSHIP & TEACHING EXPERIENCES

EXECUTIVE HEAD | Sahaay - Social Innovation Club, CFI, IIT Madras (Apr 2023 – Mar 2024)

- **Reformed the Club** and achieved a growth of **400%** in members and **900%** in applications inflow
- Directed **5 Socially Impactful projects** including Animal Welfare, Assistive Technology & AgriTech
- Guided 2 teams closely on **Jetson Nano-based edge computing** and **Embedded C Programming**
- **Trained 54 Freshmen** on Deep Learning, Transfer Learning, Data Augmentation & Model Evaluation

TEACHING ASSISTANT | Devices for AI & Neuromorphic Computing (Fall 2025)

- Collaborated with Professor to renovate course assignments to include **Spiking Neural Networks**
- Introduced focus on **Leaky Integrate-and-Fire neurons** and improved hardware-aware methods

EDUCATION

IIT MADRAS

DUAL DEGREE (B.TECH + M.TECH IN ELECTRICAL ENGINEERING)

CGPA: 8.93 / 10

2021 - 2026

CLASS XII

CBSE, MATHEMATICS & COMPUTER SCIENCE

Score: 94.0 %

2021

CLASS X

CENTRAL BOARD OF SECONDARY EDUCATION

Score: 90.8 %

2019

SCHOLASTIC ACHIEVEMENTS

AWARDED IN INSTITUTE DAY 2022

with Certificate Of Merit by Dean Of Academics

AIR¹ 332 IN JEE ADVANCED 2021

Among 0.14 million candidates

TOP 35 AIR¹ IN CMI ENTRANCE 2021

Thereby qualifying for Admission in Chennai Mathematical Institute (CMI), India

SECURED Gold Tier IN OPHO² 2021

Placed 6th among 800 Teams across the world

PLACED 7th IN PHYSICS BRAWL 2021

Organized by FYKOS, Charles University, Prague

OPEN SOURCE

IBM QISKIT MACHINE LEARNING

Contributed 3 natively Quantum datasets to a library with 830k+ downloads (2025)

MODEL CONTEXT PROTOCOL SDK

Added samples to an SDK with 3k+ stars (2025)

CHATBOT FOR JEE ASPIRANTS

Developed an Open Source IRC bot adopted by 120+ aspirants with 10+ MAU till date (2021)

INTERESTS

GUITARIST & MUSICIAN Graduated Trinity Grade 3 in Piano. Performed with IIT Madras Band and won 1st in IIM-B's Unmaad and 3rd in IIT-B's Mood Indigo. Showcased 3 original songs as the opener for the fusion band **Masala Coffee** and **Guitar Prasanna**. Sold-out our own show in 2023

ULTIMATE FRISBEE Reserve in Insti³ Team

VOLUNTEERING

STUDENT LEADER of Volunteer Group that aided Dean of Students & SLC⁴ on Improving Measures for Women Safety On-Campus (2022)

UG COUNCIL REPRESENTATIVE in the Academic Restructuring of the Elec. Engg. Curriculum for Batches 2023 Onwards (2023)

ANIMAL WELFARE ENTHUSIAST

Collaborating with Animal Welfare Board of India to deploy an app for Distress Call Response.