ECE284 FA25 Final Progress Report

1. Fill the table below. This helps us to understand your current progress status.

Item	Current Status	Status during Poster Presentation Complete In Progress Incomplete	Note
Part1	In Progress	Train model (4-bit) Hardware design Make testbench + verification FPGA synth	Nearly complete. We've struggled with the timing for the testbench design
Part2	In Progress	Train model (2-bit) Hardware design Edit testbench to test all changes	Testbench for Part 2 builds on Part 1, and we were unable to complete it
Part3	In Progress	Hardware design Edit testbench to test all changes	Testbench for Part 3 builds on Part 1, and we were unable to complete it
Alpha 1 (Leaky ReLU)	Complete	Leaky ReLU instead of ReLU to preserve negative gradients and prevent dead neurons	
Alpha 2 (Cosine Annealing LR Scheduler)	Complete	Smooth change in learning rate to improve convergence stability and accuracy	
Alpha 3 (Activation Aware Pruning)	Complete	Pruned based on weight magnitude and average activation magnitudes	
Alpha 4 (Add Layers Before Bottleneck)	Complete	Gradual layer change before and after the 8-channel bottleneck (512->128->32->8->32->128->512)	