

1. Bringing a block up from memory only speeds up loads because write through caches already write in both the cache and memory for stores. Therefore, there is no advantages to allocating a new cache block on a store instruction.
2.  $2\text{ns hit L1} + (10\% \text{ miss L1} * (10\text{ns hit L2} + (0\% \text{ miss} * 0))) = 3\text{ ns}$
3.  $2^{64} / 2^{15} = 2^{49}$  Virtual Pages
4.  $2^{32} / 2^{15} = 2^{17}$  Physical Pages
5.  $\text{Log}_2(2^{49}) = 49$  bits for VPN  
 $\text{Log}_2(2^{17}) = 17$  bits for PPN
6. **According to Edstem #998 Edison Ooi, we are to assume the PTE Size is 4B**
7.  $2^{15} / 4 = 8192$  PTE per page
8.  $32\text{KB} / 8\text{B} = 4\text{K}$  pointers per page
9.  $2^{49} * 4 = 2^{51}$  size of flat page table for single process
10. 15032 to binary (least significant 15 bits) : 011 1010 1011 1000  
25012 to binary (least significant 15 bits) : 110 0001 1011 0100
11. False, a TLB miss means a translation is not found in the TLB, but it could be in the page table in main memory, only if it does not exist in main memory as well will a page fault occur.