

# Computer Architecture - CS2323

## Lab-3 RISC-V Disassembler

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## 1 Introduction

The aim of this assignment is to convert a given RISC-V machine code to its equivalent assembly syntax. The code of this assignment is written in C language.

## 2 Methodology

An input file has to be given and the instructions in it are read line by line. The 32 bit hexadecimal instructions are first converted to decimal and then to binary. The opcode of an instruction is extracted from the binary format and based on the value of opcode the type of instruction is identified and the respective functions are called. In the functions for each instruction the values of source registers, destination register, immediate are extracted as per their location and presence in that type of instruction. Two functions are used for this extraction

One gives the signed result

Other gives unsigned result

One of these functions is called according to the requirement.

### For Labels

An ordered Linked List is used to identify the labels. Structures in this linked list store the program counter of the instruction corresponding to a label and the label number.

In case of B-type and J-type instructions, the offset is added to present program counter and if the resulted value doesn't have a label already then a new node is created with a label number and the value of program counter corresponding to the instruction to be label and inserted into the linked list at appropriate location.

While the instructions are being read from the file the program counter gets incremented for every instruction and those instructions whose program counter matches with any node in the linked list will get a label printed with the corresponding label number.

**It is considered that the offset in B-type and J-type instructions is positive.**

### 3 Results

Various input files have been used for checking the efficiency of the code and the results are cross-checked in RIPES simulator.