1. 1) Page size = 16KB = 2^14 Bytes. So the offset should be 14.

So the index and tag for virtual address and physical address is 40-14 and 32-14= 26 and 18.

The TLB each entry should be 26+18+4=48

TLB total size= TLB entries\*TLB entry size= 8\*48=384 bits

2) PTE= 4+ physical page= 4+ 18=22

PTE’s total number = 2^26

Page table size= PTE size\*PTE’s total number= 22\* 2^26 bits

1. Since there are 16 Kbytes of addressable entries per page, there are nearly 2^14 bytes. So the offset is 14 bits. For virtual page is 40-14=26, physical page is 30-14=16. So the TLB entries is 16+14 =30 bits. So there are 2^8\*2^14 =2^22entries that can be quickly translated by TLB.
2. 1) clock rate of 2 GHz, since the memory access time is 200ns, so the clock number is 400. Effective CPI= 1+0.03\*400=13

2) Secondary cache clock is 10\*2=20 cycles. Effective CPI= 1+3%\*20+1%\*400=5.6

Rate = 13/5.6=2.32 times.

1. A) Performance of P1= 2.5\*10^9/1.0

B)

C)