數位系統設計與實習

Chap 0 課程簡介與軟硬體安裝設定

銘傳大學電子工程學系

黃炳森 教授

目錄

0-1 課程簡介

- **Class times**
  - 12:50-15:40 Turesday, S301 電子二乙
  - 09:10-12:00 Wednesday, S302 電子二甲
- **Instructor office hours**
  - Prof. Pingsheng Huang(黃炳森), pshuang@mail.mcu.edu.tw
  - Office: S635
  - Phone: ext. 3435
  - Office Hours: Thursday, 09:10-12:00, Thursday, 12:50-15:40,

0-1 課程簡介

Evaluation and Grading

- **Approximately:**
  - –50% Experiment Report
  - –30% Midterm Exam
  - –20% Final Exam

- Participating in these is important to your understanding of the topic and **your grade**!

0-1 課程簡介

Course Purposes

- This course introduces the student to the design of **digital logic circuits**, both **combinational** and **sequential**, and the design of digital systems in a hierarchical, top-down manner.
- The student is also introduced to the use of **computer-aided design tools** to develop complex digital circuits and to prototyping designs using programmable logic devices and field-programmable gate arrays(FPGA).

0-1 課程簡介

What You Should Already Know

- **Principles of basic digital logic design (Digital Logic Design)**
  - Number representations
  - Boolean algebra
  - Gate-level design
  - K-Map minimization
  - Combinational logic
  - Synchronous sequential logic
  - Registers and counters

0-1 課程簡介

Text Book:

- 黃英叡, 黃稚存 編譯, Verilog 硬體描述語言(附範例光碟片)(第二版), 全華圖書, 2022

Referred Books and Websites:

- 劉紹漢, 數位邏輯設計與晶片實務(Verilog)(第三版), 2019年8月.(全華圖書)
- 並木秀明著, 吳炘廷譯, 正確學會 Verilog 的 16 堂課, 旗標圖書, 2012.
- http://www.terasic.com.tw and http://www.altera.com

0-1 課程簡介

- Simulation software
  - **Quartus II**, **ModelSim-Altera**, **NIOS II**
  - Altera: **Quartus II 13.0sp1**
  - Remember to download **Web Edition** (free)
  - Plenty of resources available on the Web.
  - Quartus II is used for writing Verilog HDL, VHDL, Simulation, and Synthesis.
  - Terasic DE1 & DE0 boards are used for implementation
  - Check MCU Moodle system for more course materials!

0-1 課程簡介

- Useful Resources
  - Verilog 從放棄到有趣 系列
  - FPGA Academic Program Teaching Materials
  - FPGA 4 student
  - [野火]FPGA Verilog开发实战指南——基于Altera EP4CE10 征途Mini开发板

0-1 課程簡介

Course Overview

- Review of Logic Design Fundamentals
- Introduction to Programmable Logic Devices
- Introduction to DE1 & DE0, Quartus II and ModelSim-Altera
- Introduction to Verilog HDL
- Digital Logic Design Examples (Combinational & Sequential Circuits)
- DE1 & DE0 Design Examples
- Small Project Design

0-1 課程簡介

What You Should Do?

- **In Class**
  - Listen carefully and be concentrated
  - Practice hard during the assigned time slot
- **After Class**
  - Study hard for those information from the book and the internet
  - Practice actively by yourself!!
  - Practice, Practice, and Practice!!!

Q & A

0-2 硬體平台簡介

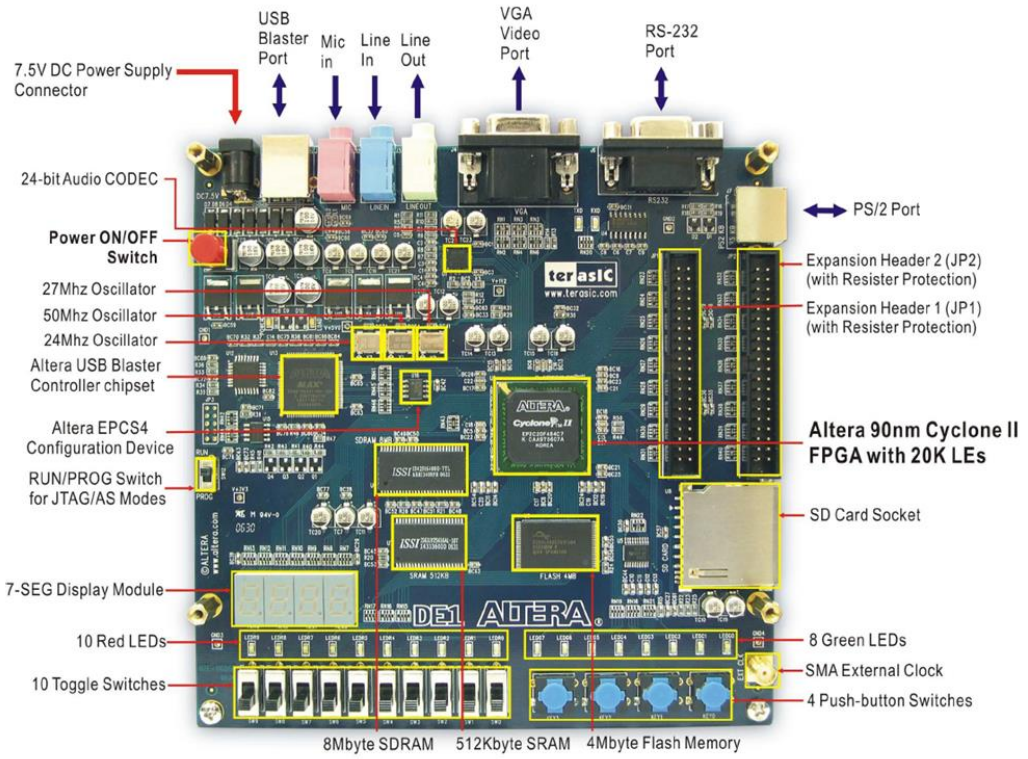
- **硬體(http://www.terasic.com.tw)**
  - 友晶科技 (Terasic) Altera DE系列實驗板

Board	Device Name
DE0	Cyclone III EP3C16F484C6
DE0-Nano	Cyclone IVE EP4CE22F17C6
DE1	Cyclone II EP2C20F484C7
DE2	Cyclone II EP2C35F672C6
DE2-70	Cyclone II EP2C70F896C6
DE2-115	Cyclone IVE EP4CE115F29C7

表 1-1 DE系列實驗板FPGA名稱

0-2 硬體平台簡介

- Simulation hardware
  - terasIC(友晶科技) DE1



0-2 硬體平台簡介

- **硬體**
  - **友晶科技 Altera DE1多媒體開發平台**
    - FPGA型號 ”Cyclone II EP2C20F484”
    - 具有20,000個邏輯單元(LEs)
    - 外接記憶體 8M byte的SDRAM
    - 512 Kbyte(256Kx16)的SRAM
    - 4M byte的Flash記憶體
    - 支援SPI以及SD 1-bit兩種SD Card讀取模式的SD card插槽。

0-2 硬體平台簡介

- **硬體**
  - **友晶科技 (Terasic) Altera DE1 實驗板介面**
  - 內建USB Blaster電路
    - 使用於 FPGA 程式下載或控制
  - Altera 序列配置器(Altera EPCS4 序列EEPROM)
  - 4個壓按開關與10個指撥開關
  - 8 個綠色LED、10 個紅色LED與4個七段顯示器
  - 50M、24M與27MHz三種時脈輸入
  - VGA 輸出(4-bit 電阻式 DAC)
  - Audio 輸入與輸出(24-bit CD品質與麥克風輸入接頭)

0-2 硬體平台簡介

- **硬體**
  - **友晶科技 (Terasic) Altera DE1 實驗板介面**
  - 序列接頭
    - 一組 RS-232訊號接腳與一組PS/2接頭
  - 兩組40-腳擴充槽
    - 72 個 3.3V I/O 接腳以及8個電源與接地接腳
    - 用於40個接腳擴充槽的排線可利用 IDE 硬碟專用的40個接腳的排線

0-2 硬體平台簡介

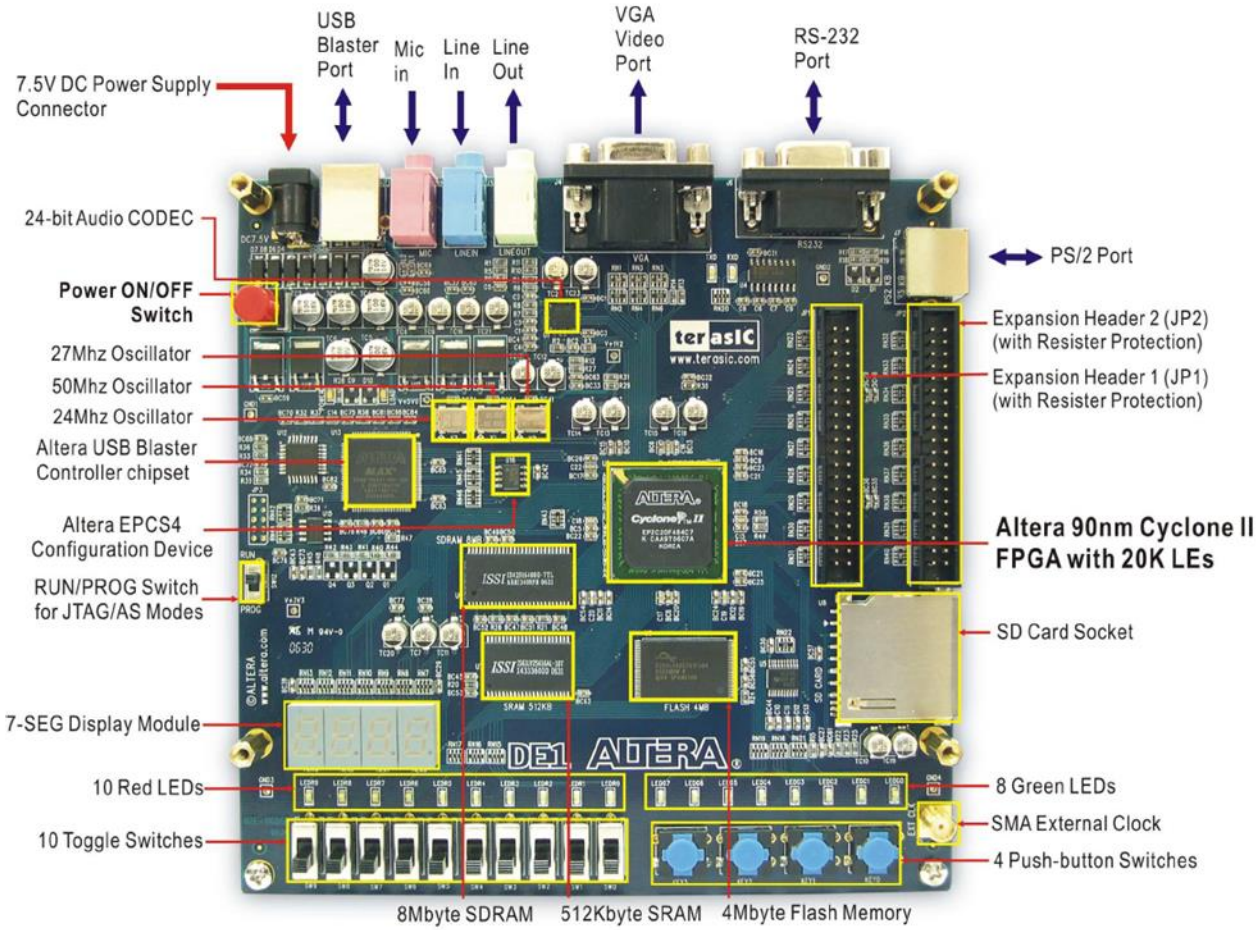


圖 1-1　友晶科技DE1開發板

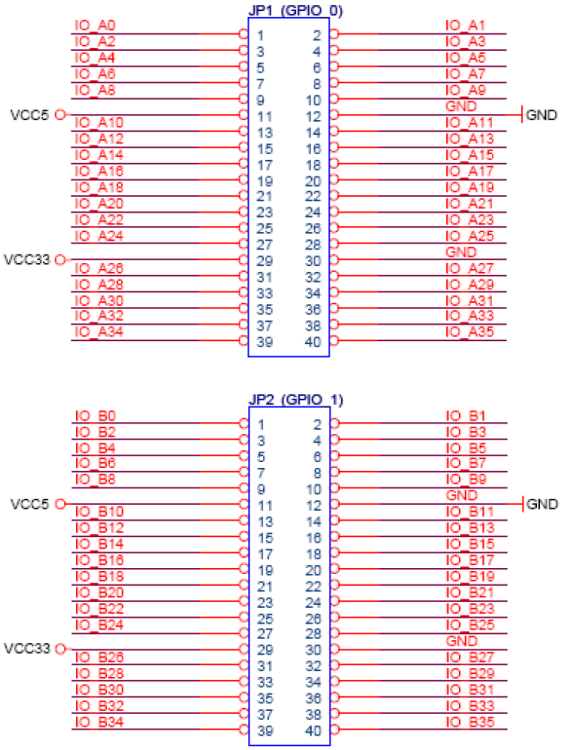


圖 1-2　DE1 GPIO接腳圖

0-2 硬體平台簡介

- 硬體
  - DE1元件與FPGA Cyclone II 腳位對應
    - 七段顯示器：模擬板上有四個七段顯示器裝置，已與Cyclone元件連接，當Cyclone腳位送出0準位才會讓七段顯示器亮，小數點未連接。

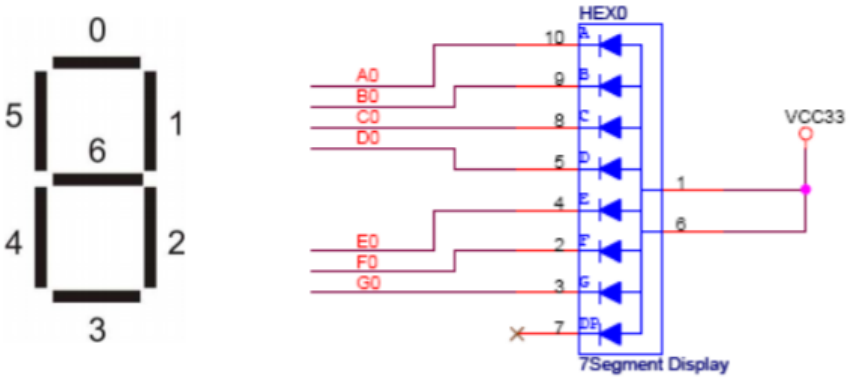


圖 1-3　七段顯示器HEX0接腳圖

0-2 硬體平台簡介

- 硬體
  - 七段顯示器與FPGA Cyclone II 腳位對應表

七段	FPGA	七段	FPGA	七段	FPGA	七段	FPGA
HEX3[0]	PIN_F4	HEX2[0]	PIN_G5	HEX1[0]	PIN_E1	HEX0[0]	PIN_J2
HEX3[1]	PIN_D5	HEX2[1]	PIN_G6	HEX1[1]	PIN_H6	HEX0[1]	PIN_J1
HEX3[2]	PIN_D6	HEX2[2]	PIN_C2	HEX1[2]	PIN_H5	HEX0[2]	PIN_H2
HEX3[3]	PIN_J4	HEX2[3]	PIN_C1	HEX1[3]	PIN_H4	HEX0[3]	PIN_H1
HEX3[4]	PIN_L8	HEX2[4]	PIN_E3	HEX1[4]	PIN_G3	HEX0[4]	PIN_F2
HEX3[5]	PIN_F3	HEX2[5]	PIN_E4	HEX1[5]	PIN_D2	HEX0[5]	PIN_F1
HEX3[6]	PIN_D4	HEX2[6]	PIN_D3	HEX1[6]	PIN_D1	HEX0[6]	PIN_E2

表 1-2　七段顯示器腳位對應表

0-2 硬體平台簡介

- 硬體
  - 十個指撥開關與FPGA Cyclone II 腳位對應表

指撥	FPGA	指撥	FPGA
SW[0]	PIN_L22	SW[5]	PIN_U12
SW[1]	PIN_L21	SW[6]	PIN_U11
SW[2]	PIN_M22	SW[7]	PIN_M2
SW[3]	PIN_V12	SW[8]	PIN_M1
SW[4]	PIN_W12	SW[9]	PIN_L2

表 1-3　指撥開關腳位對應表

0-2 硬體平台簡介

- 硬體
  - 四個按壓開關與FPGA Cyclone II 腳位對應表

按壓	FPGA
KEY[0]	PIN_R22
KEY[1]	PIN_R21
KEY[2]	PIN_T22
KEY[3]	PIN_T21

表 1-4　按壓開關腳位對應表

0-2 硬體平台簡介

- 硬體
  - 紅與綠LED與FPGA Cyclone II 腳位對應表

紅LED	FPGA	紅LED	FPGA	綠LED	FPGA	綠LED	FPGA
LEDR[0]	PIN_R20	LEDR[5]	PIN_V19	LEDG[0]	PIN_U22	LEDG[4]	PIN_W22
LEDR[1]	PIN_R19	LEDR[6]	PIN_Y18	LEDG[1]	PIN_U21	LEDG[5]	PIN_W21
LEDR[2]	PIN_U19	LEDR[7]	PIN_U18	LEDG[2]	PIN_V22	LEDG[6]	PIN_Y22
LEDR[3]	PIN_Y19	LEDR[8]	PIN_R18	LEDG[3]	PIN_V21	LEDG[7]	PIN_Y21
LEDR[4]	PIN_T18	LEDR[9]	PIN_R17				

表 1-5　紅與綠LED腳位對應表

0-2 硬體平台簡介

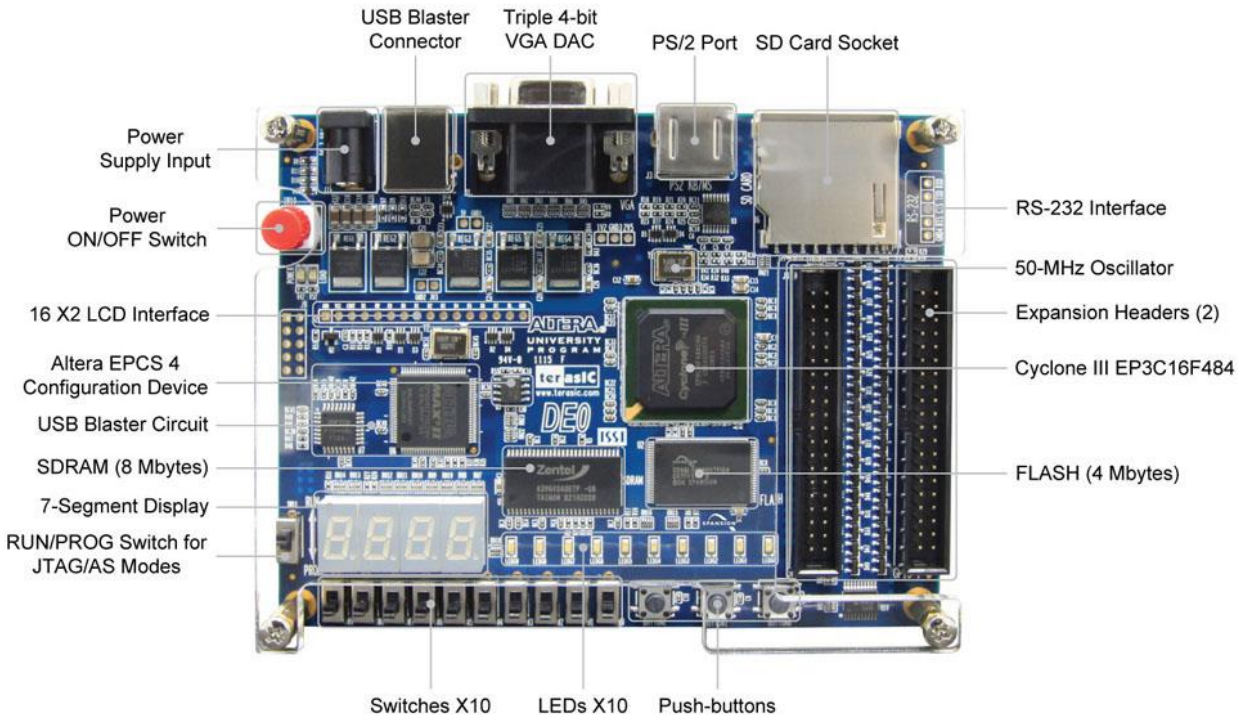
- 硬體
  - 時脈輸入與FPGA Cyclone II 腳位對應表
  - 其餘元件腳位對應表請參考Excel檔案 DE1_pin_assignments.csv與DE1 User Manual內容

時脈輸入	FPGA
CLOCK_27	PIN_D12, PIN_E12
CLOCK_50	PIN_L1
CLOCK_24	PIN_A12, PINB12
EXT_CLOCK	PIN_M21

表 1-6　時脈輸入腳位對應表

0-2 硬體平台簡介

- Simulation hardware
  - terasIC(友晶科技) DE0



0-2 硬體平台簡介

- **硬體**
  - **友晶科技 Altera DE0多媒體開發平台**
    - FPGA型號 ” Cyclone III EP3C16F484”
    - 具有15,048個邏輯單元(LEs)
    - 外接記憶體 8M byte的SDRAM
    - 504 K RAM bits
    - 4M byte的NOR Flash記憶體
    - 支援SPI以及SD 1-bit兩種SD Card讀取模式的SD card插槽。

0-2 硬體平台簡介

- **硬體**
  - **友晶科技 (Terasic) Altera DE0 實驗板介面**
  - 內建USB Blaster電路
    - 使用於 FPGA 程式下載或控制
  - Altera 序列配置器(Altera EPCS4 序列EEPROM)
  - 3個壓按開關與10個指撥開關
  - 10 個綠色LED與4個七段顯示器
  - 50M 時脈輸入
  - VGA 輸出(4-bit 電阻式 DAC)

0-2 硬體平台簡介

- **硬體**
  - **友晶科技 (Terasic) Altera DE0 實驗板介面**
  - 序列接頭
    - 一組 RS-232訊號接腳與一組PS/2接頭
  - 兩組40-腳擴充槽
    - 72 個 3.3V I/O 接腳以及8個電源與接地接腳
    - 用於40個接腳擴充槽的排線可利用 IDE 硬碟專用的40個接腳的排線

0-2 硬體平台簡介

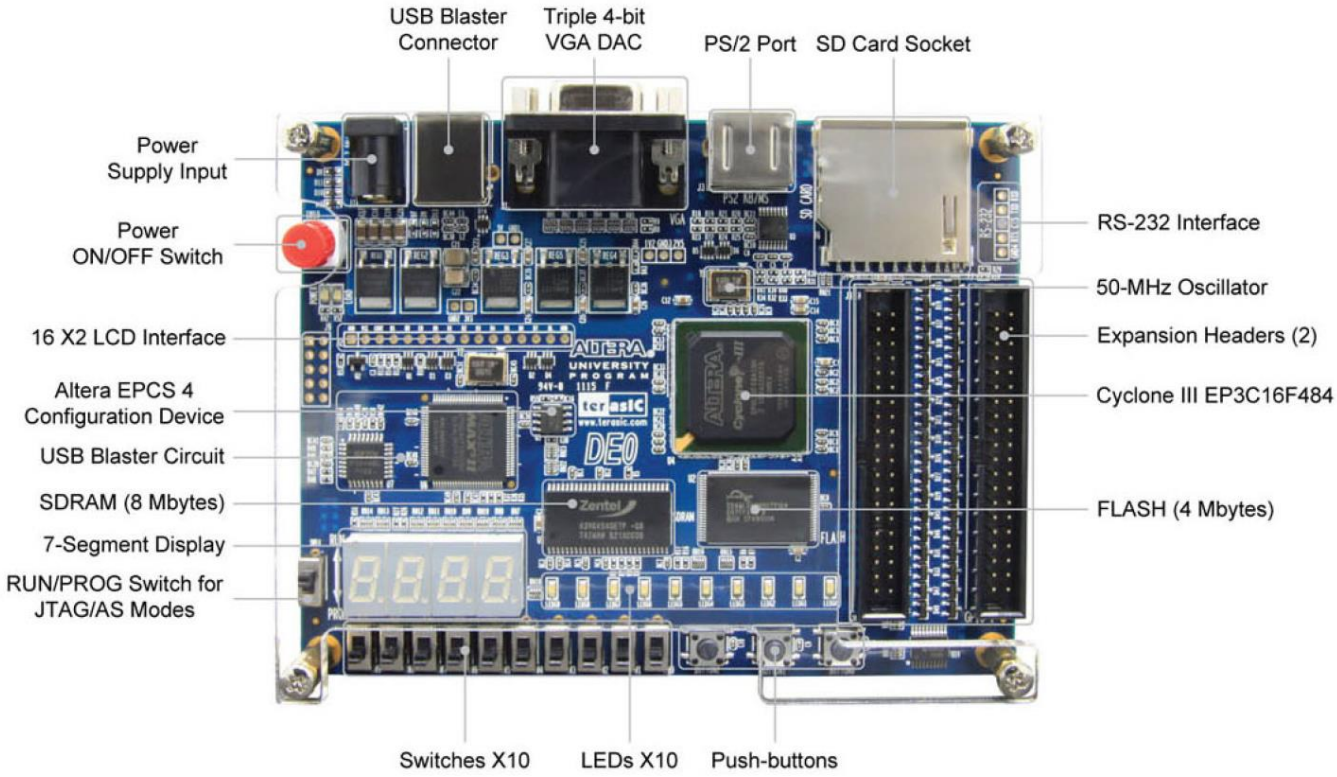


圖 1-4　友晶科技DE0開發板

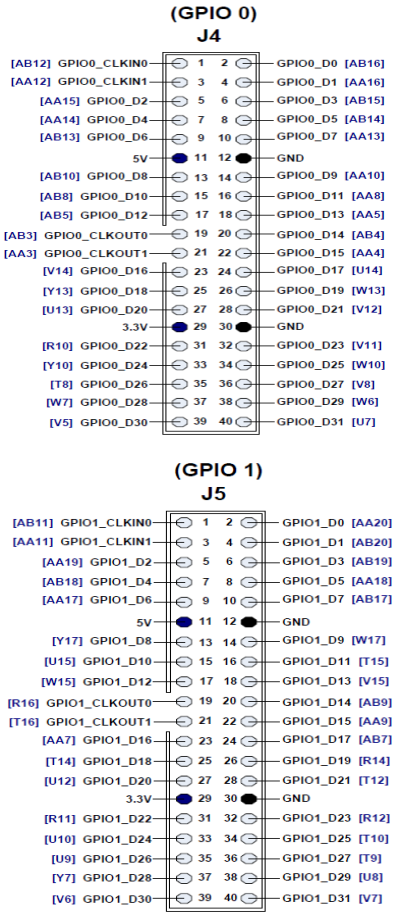


圖 1-5　DE0 GPIO接腳圖

0-2 硬體平台簡介

- 硬體
  - DE0元件與FPGA Cyclone III 腳位對應
    - 七段顯示器：模擬板上有四個七段顯示器裝置，已與Cyclone元件連接，當Cyclone腳位送出0準位才會讓七段顯示器亮，小數點有連接。

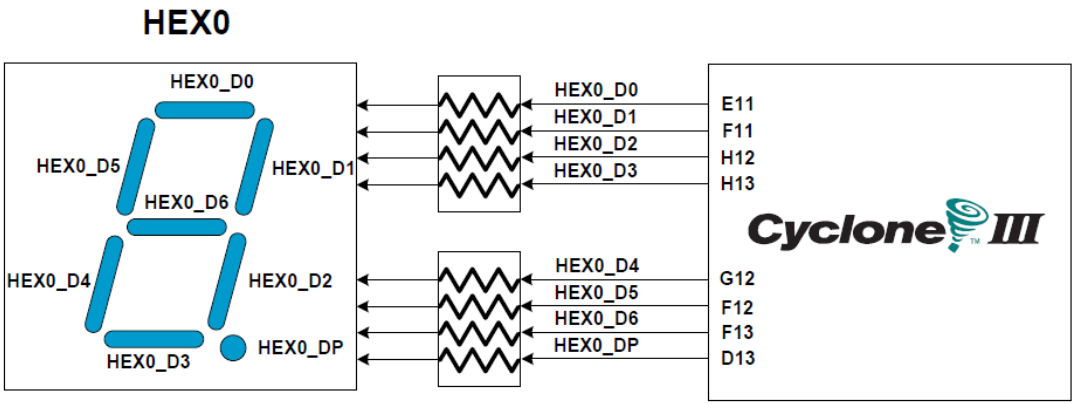


圖 1-6　七段顯示器HEX0接腳圖

0-2 硬體平台簡介

- 七段顯示器與FPGA Cyclone III 腳位對應表

七段	FPGA	七段	FPGA	七段	FPGA	七段	FPGA
HEX3_D[0]	PIN_B18	HEX2_D[0]	PIN_D15	HEX1_D[0]	PIN_A13	HEX0_D[0]	PIN_E11
HEX3_D[1]	PIN_F15	HEX2_D[1]	PIN_A16	HEX1_D[1]	PIN_B13	HEX0_D[1]	PIN_F11
HEX3_D[2]	PIN_A19	HEX2_D[2]	PIN_B16	HEX1_D[2]	PIN_C13	HEX0_D[2]	PIN_H12
HEX3_D[3]	PIN_B19	HEX2_D[3]	PIN_E15	HEX1_D[3]	PIN_A14	HEX0_D[3]	PIN_H13
HEX3_D[4]	PIN_C19	HEX2_D[4]	PIN_A17	HEX1_D[4]	PIN_B14	HEX0_D[4]	PIN_G12
HEX3_D[5]	PIN_D19	HEX2_D[5]	PIN_B17	HEX1_D[5]	PIN_E14	HEX0_D[5]	PIN_F12
HEX3_D[6]	PIN_G15	HEX2_D[6]	PIN_F14	HEX1_D[6]	PIN_A15	HEX0_D[6]	PIN_F13
HEX3_DP	PIN_G16	HEX2_DP	PIN_A18	HEX1_DP	PIN_B15	HEX0_DP	PIN_D13

表 1-7　七段顯示器腳位對應表

0-2 硬體平台簡介

- 硬體
  - 十個指撥開關與FPGA Cyclone III 腳位對應表

指撥	FPGA	指撥	FPGA
SW[0]	PIN_J6	SW[5]	PIN_J7
SW[1]	PIN_H5	SW[6]	PIN_H7
SW[2]	PIN_H6	SW[7]	PIN_E3
SW[3]	PIN_G4	SW[8]	PIN_E4
SW[4]	PIN_G5	SW[9]	PIN_D2

表 1-8　指撥開關腳位對應表

0-2 硬體平台簡介

- 硬體
  - 三個按壓開關與FPGA Cyclone III 腳位對應表

按壓	FPGA
BUTTON[0]	PIN_H2
BUTTON[1]	PIN_G3
BUTTON[2]	PIN_F1

表 1-9　按壓開關腳位對應表

0-2 硬體平台簡介

- 硬體
  - 綠LED與FPGA Cyclone III 腳位對應表

綠LED	FPGA	綠LED	FPGA
LEDG[0]	PIN_J1	LEDG[5]	PIN_E1
LEDG[1]	PIN_J2	LEDG[6]	PIN_C1
LEDG[2]	PIN_J3	LEDG[7]	PIN_C2
LEDG[3]	PIN_H1	LEDG[8]	PIN_B2
LEDG[4]	PIN_F2	LEDG[9]	PIN_B1

表 1-10　綠LED腳位對應表

0-2 硬體平台簡介

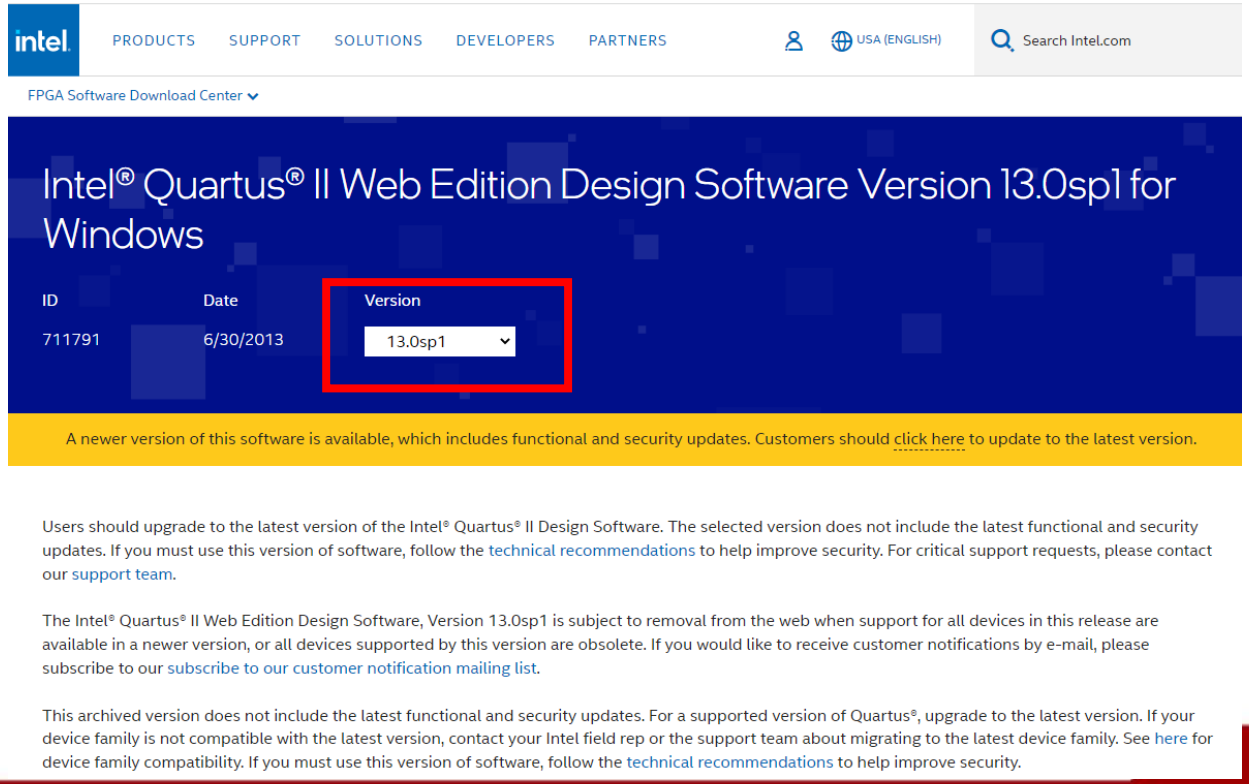
- 硬體
  - 時脈輸入與FPGA Cyclone III 腳位對應表
  - 其餘元件腳位對應表請參考Excel檔案 DE0_pin_assignments.csv與DE0 User Manual內容

時脈輸入	FPGA
CLOCK_50	PIN_G21
CLOCK_50_2	PIN_B12

表 1-11　時脈輸入腳位對應表

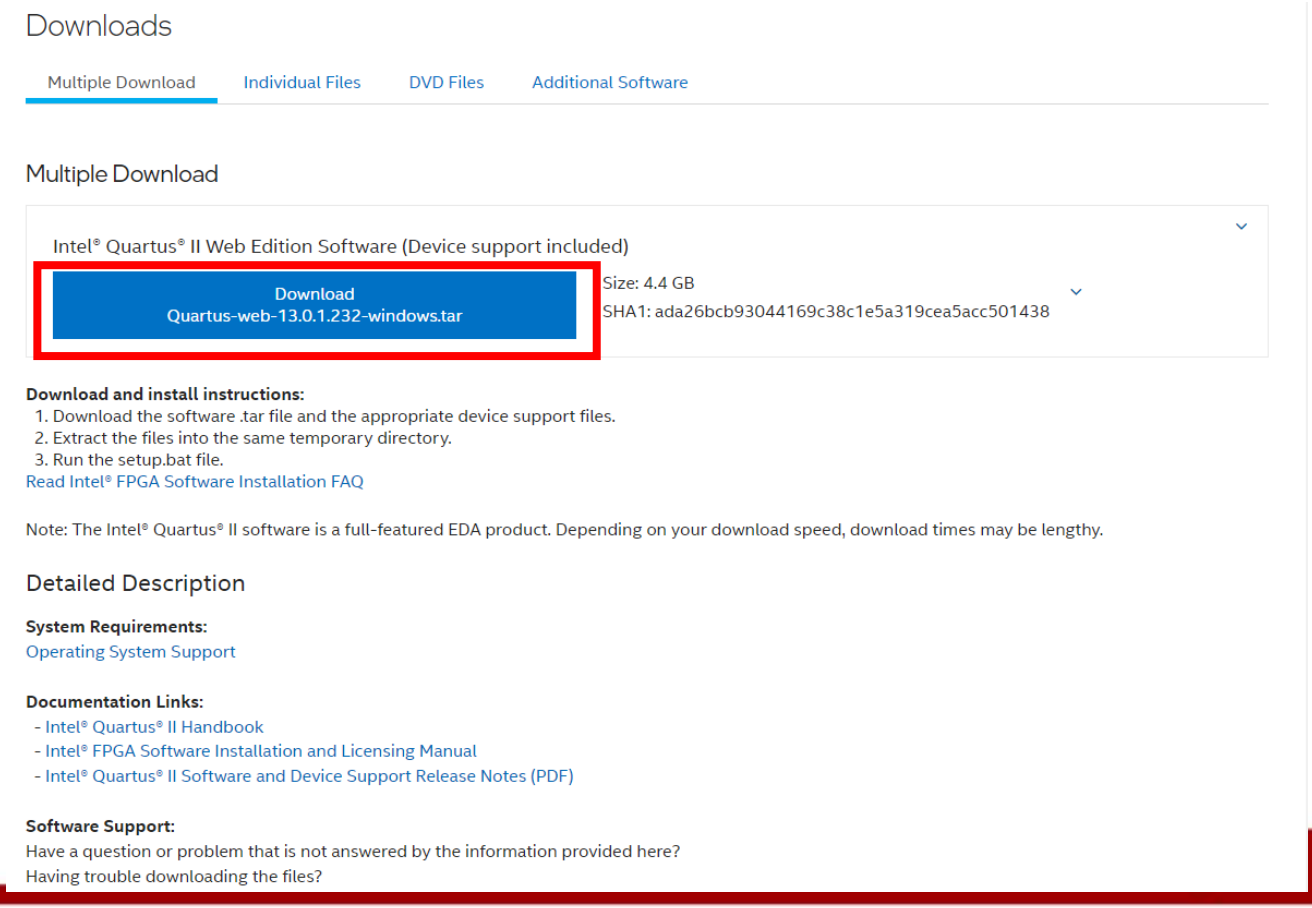
0-3 軟體下載

- Simulation software
  - Quartus II Web Edition 13.0sp1 for Windows



0-3 軟體下載

- Simulation software



Downloads

Multiple Download | Individual Files | DVD Files | Additional Software

Multiple Download

Intel® Quartus® II Web Edition Software (Device support included)

Download
Quartus-web-13.0.1.232-windows.tar

Size: 4.4 GB
SHA1: ada26bcb93044169c38c1e5a319cea5acc501438

Download and install instructions:
1. Download the software .tar file and the appropriate device support files.
2. Extract the files into the same temporary directory.
3. Run the setup.bat file.

Read Intel® FPGA Software Installation FAQ

Note: The Intel® Quartus® II software is a full-featured EDA product. Depending on your download speed, download times may be lengthy.

Detailed Description

System Requirements:
Operating System Support

Documentation Links:
- Intel® Quartus® II Handbook
- Intel® FPGA Software Installation and Licensing Manual
- Intel® Quartus® II Software and Device Support Release Notes (PDF)

Software Support:
Have a question or problem that is not answered by the information provided here?
Having trouble downloading the files?

0-3 軟體下載

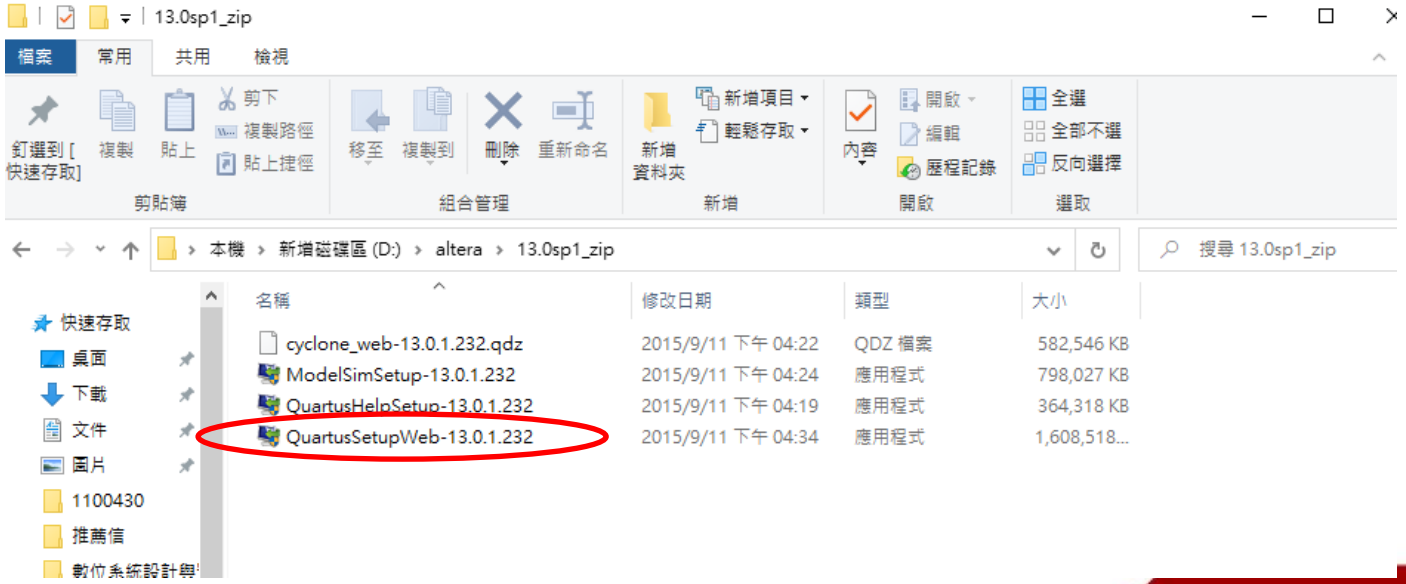
- Simulation software
- 下載 **Quartus II 13.0sp1 Web Edition(free)**

  –解壓縮檔案共有四個:約3.2GB

  1. QuartusSetupWeb-13.0.1.232.exe
  2. ModelSimSetup-13.0.1.232.exe
  3. cyclone_web-13.0.1.232.qdz
  4. QuartusHelpSetup-13.0.1.232.exe

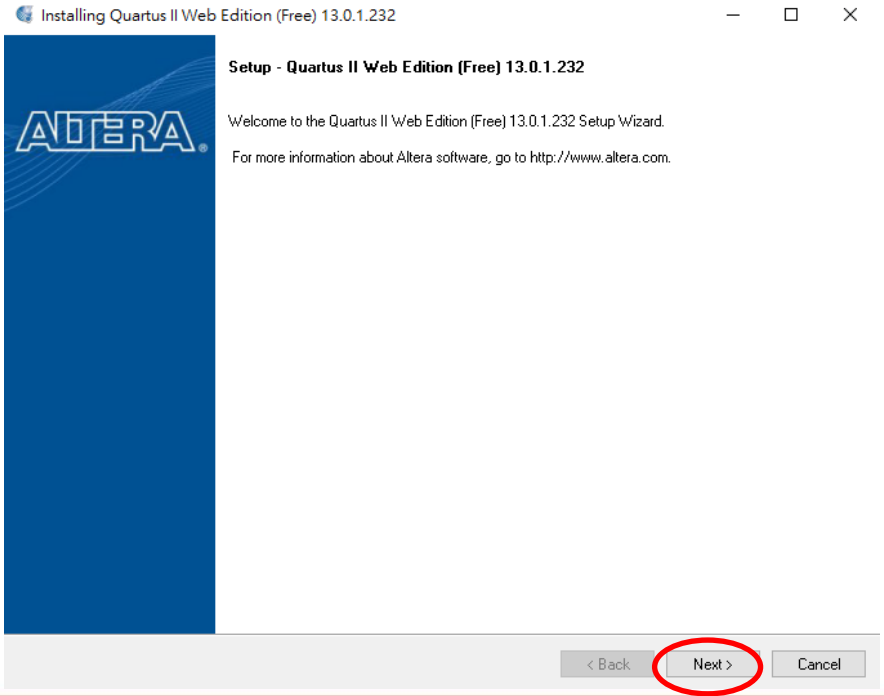
0-4 軟體安裝與設定

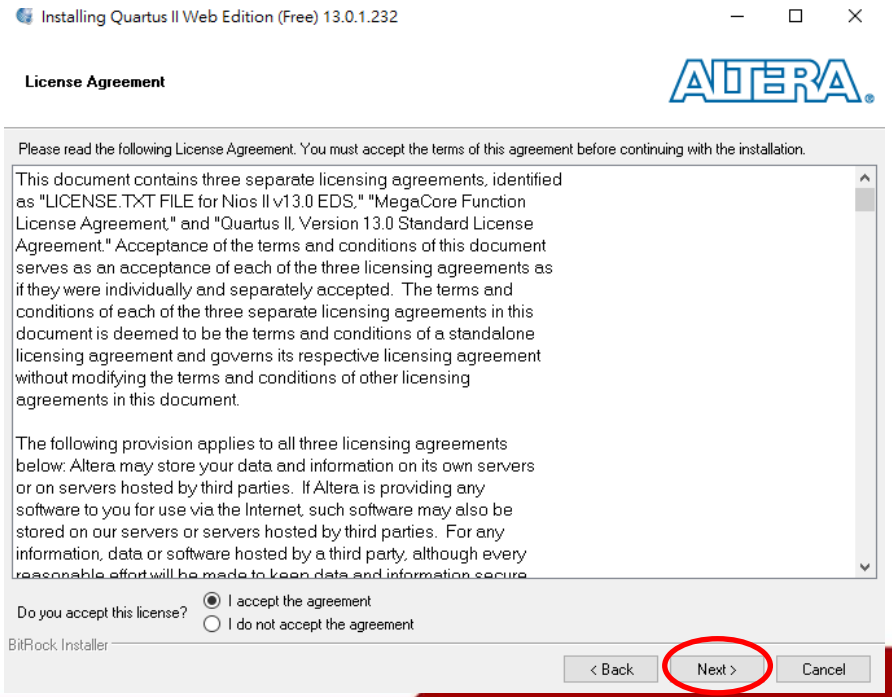
- 安裝 Quartus II 13.0 Service Pack 1 Web Edition(free)
  - 開啟下載Quartus II 13.0 sp1 Web Edition四個檔案置放之資料夾(Windows 10畫面)
  - 點選"QuartusSetupWeb-13.0.1.232.exe"



0-4 軟體安裝與設定

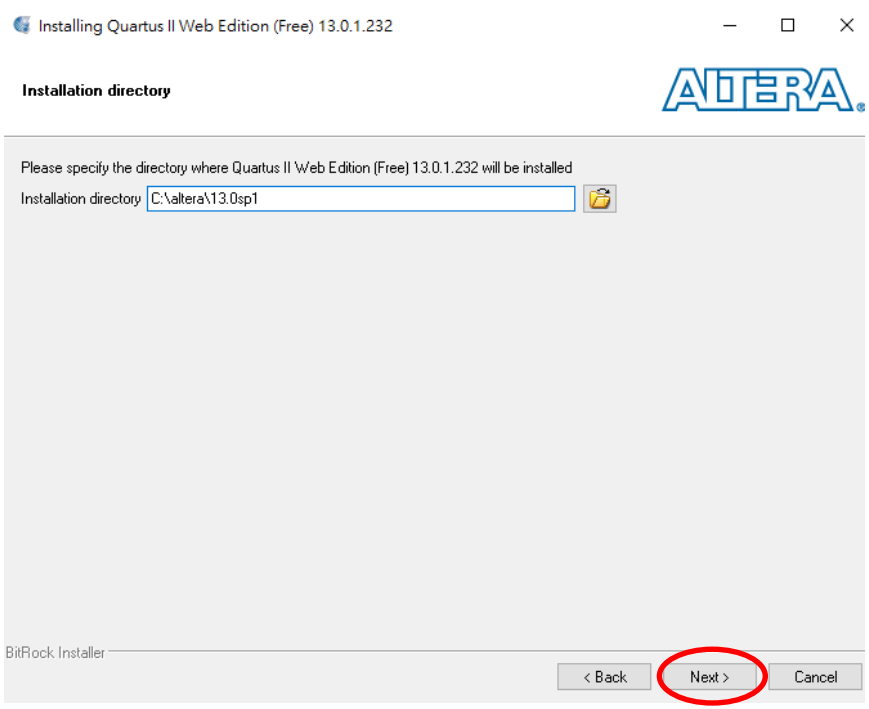
- 安裝 Quartus II 13.0 Service Pack 1 Web Edition(free)
  - 執行"QuartusSetupWeb-13.0.1.232.exe"，出現以下所示之開始安裝及授權畫面。

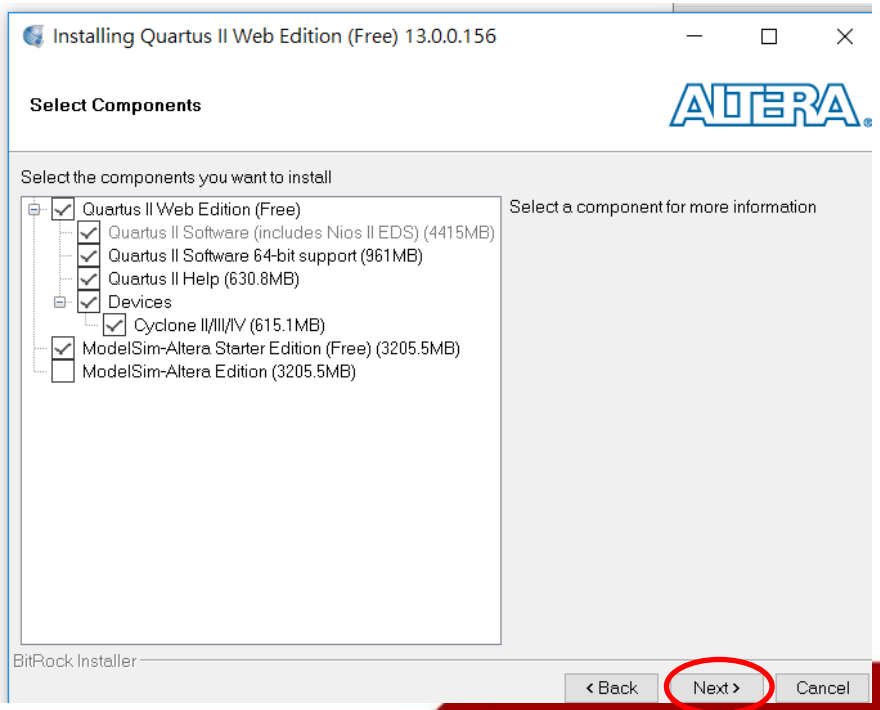




0-4 軟體安裝與設定

- 安裝 Quartus II 13.0 Service Pack 1 Web Edition(free)
  - 選擇欲安裝之目錄及軟體元件，這裡會將ModelSim-Altera Starter Edition(Free)一併安裝。

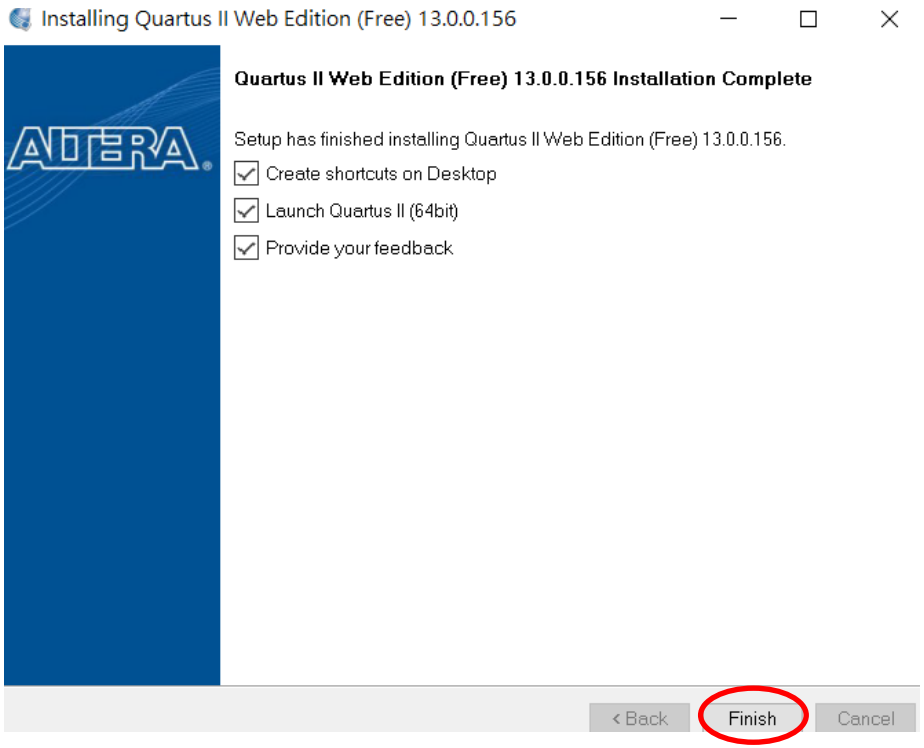


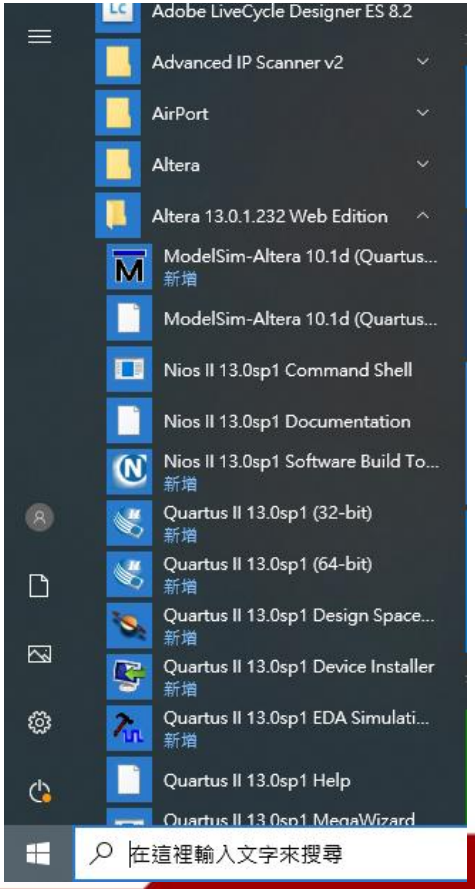


0-4 軟體安裝與設定

- 安裝 Quartus II 13.0 Service Pack 1 Web Edition(free)

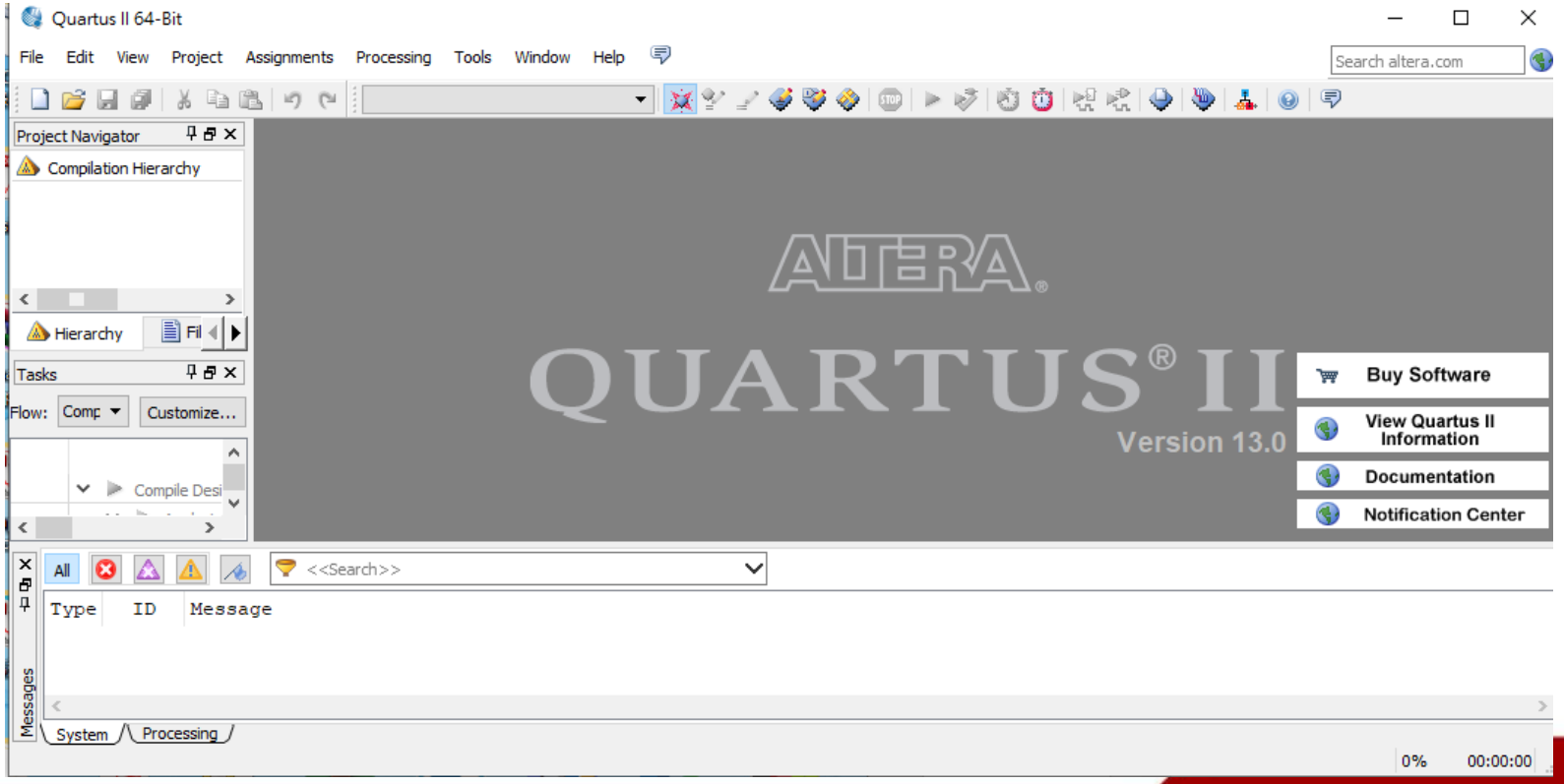
  －安裝完畢及所有元件清單畫面





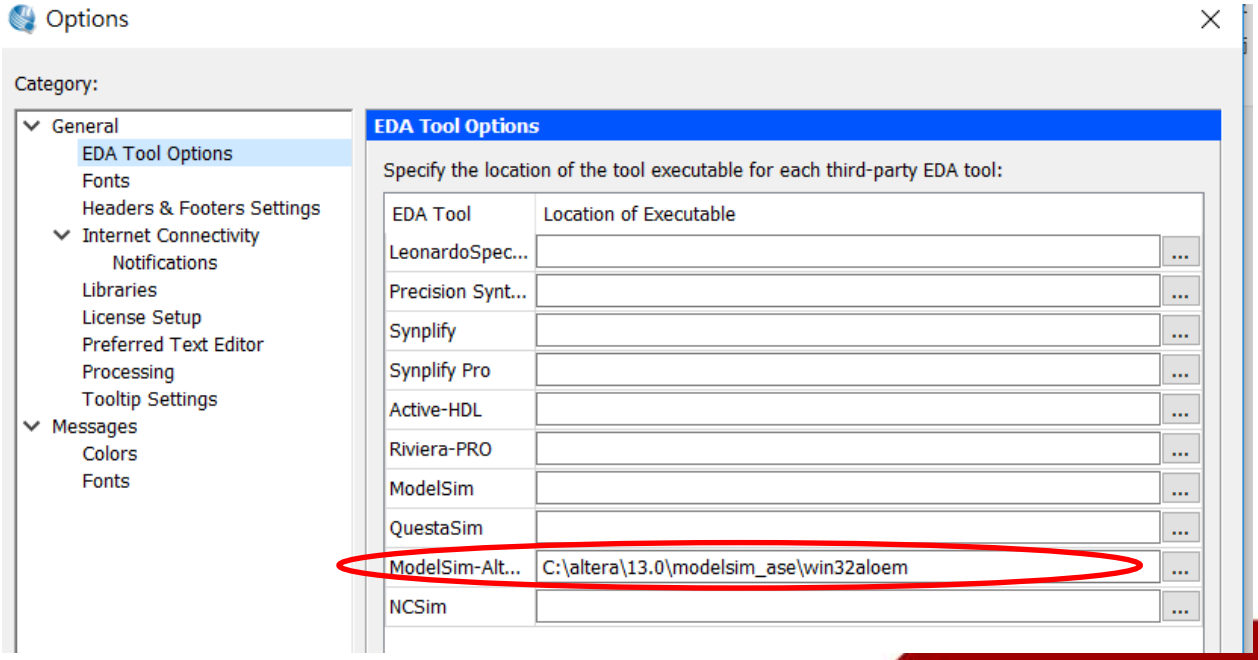
0-4 軟體安裝與設定

- 安裝 Quartus II 13.0 Service Pack 1 Web Edition(free)
  - 啟動Quartus II 13.0畫面



0-4 軟體安裝與設定

- 檢查與設定ModelSim-Altera所在目錄
  - 從啟動畫面的上排選項選擇 Tools -> Options -> General -> EDA Tool Options, 確認ModelSim-Altera目錄路徑



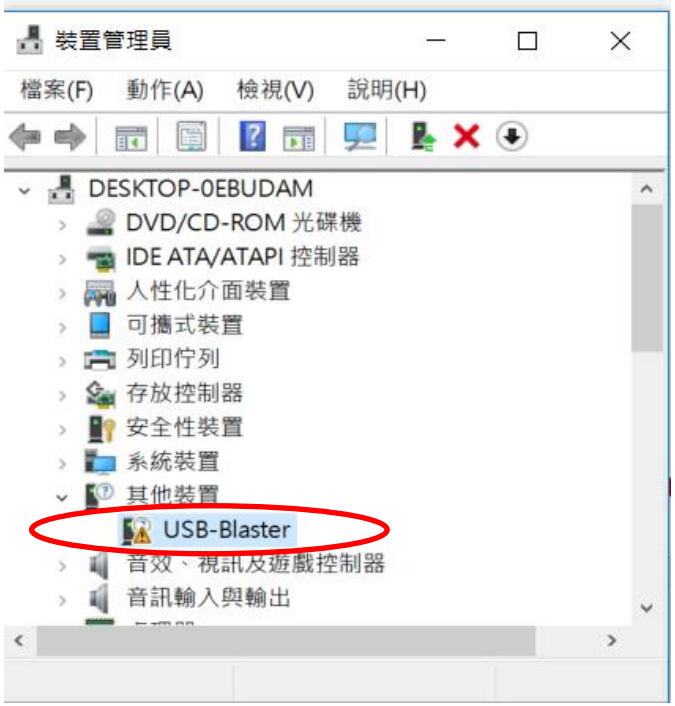
0-5 安裝USB-Blaster驅動程式

- **FPGA數位電路設計主要步驟**
  - 使用 Quartus II 工具完成電路設計與編譯
  - 利用 ModelSim-Altera 工具完成時序功能模擬
  - 將電路燒錄至硬體平台(DE1)上之FPGA晶片進行實測
- **電路燒錄主要步驟**
  - 使用USB接線連結硬體平台與電腦
  - 開啟硬體平台開關
  - 啟動Quartus II Programmer 工具進行燒錄

  (燒錄進行前須安裝USB-Blaster驅動程式)

0-5 安裝USB-Blaster驅動程式

- 安裝USB-Blaster驅動程式步驟
  - 使用USB接線連結硬體平台與電腦
  - 開啟硬體平台開關
  - 開啟Windows裝置管理員
  - 點選其他裝置->USB-Blaster

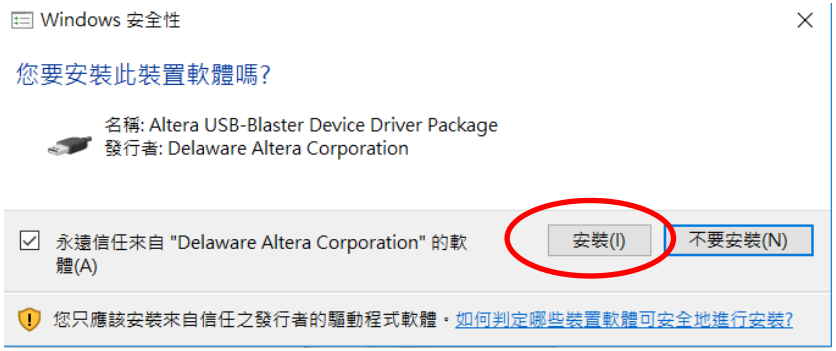


0-5 安裝USB-Blaster驅動程式

- 安裝USB-Blaster驅動程式步驟
  - 在”USB-Blaster內容”點選”更新驅動程式”
  - 在”更新驅動程式- USB-Blaster”點選”瀏覽電腦上的驅動程式軟體”

0-5 安裝USB-Blaster驅動程式

- 安裝USB-Blaster驅動程式步驟
  - 在”更新驅動程式- USB-Blaster”瀏覽空格內加入路徑
  - 點選下一步後選擇”安裝”軟體後即可完成



0-5 安裝USB-Blaster驅動程式

- 安裝USB-Blaster驅動程式步驟
  - 出現下列畫面即代表驅動程式更新完成，可以開始燒錄電路。