37245 數位系統設計與實習

銘傳大學電子工程學系
黃炳森 教授

Course Information

- **Class times**
  - 12:50-15:40 Tuesday S301 電子二乙
  - 09:10-12:00 Wednesday S301 電子二甲
- **Instructor office hours**
  - Prof. Ping-Sheng Huang(黃炳森), pshuang@mail.mcu.edu.tw
  - Office: S635
  - Phone: ext. 3435
  - Office Hours: Tuesday & Wednesday, 15:50-16:50, Thursday, 09:00-12:00

Evaluation and Grading

- **Approximately:**
  - 70% Experiment performance and report
  - 30% Midterm exam

- Participating in these is important to your understanding of the topic and **your grade**!

Course Purposes

- This is an advanced version for the undergraduate course of "數位系統設計與實習", and the design of digital systems in a hierarchical, top-down manner.
- The student is also introduced to the use of **computer-aided design tools** to develop complex digital circuits and to prototyping designs using programmable logic devices and field-programmable gate arrays(FPGA).

What You Should Already Know

- **Principles of basic digital logic design (Digital Logic Design)**
  - Number representations
  - Boolean algebra
  - Gate-level design
  - K-Map minimization
  - Combinational logic
  - Synchronous sequential logic
  - Registers and counters
  - Memory and programmable logic

Course Overview

Textbook:

- 黃英叡, 黃稚存 編譯, Verilog 硬體描述語言(附範例光碟片)(第二版), 2019年8月.(全華圖書)

Referred Books and Websites:

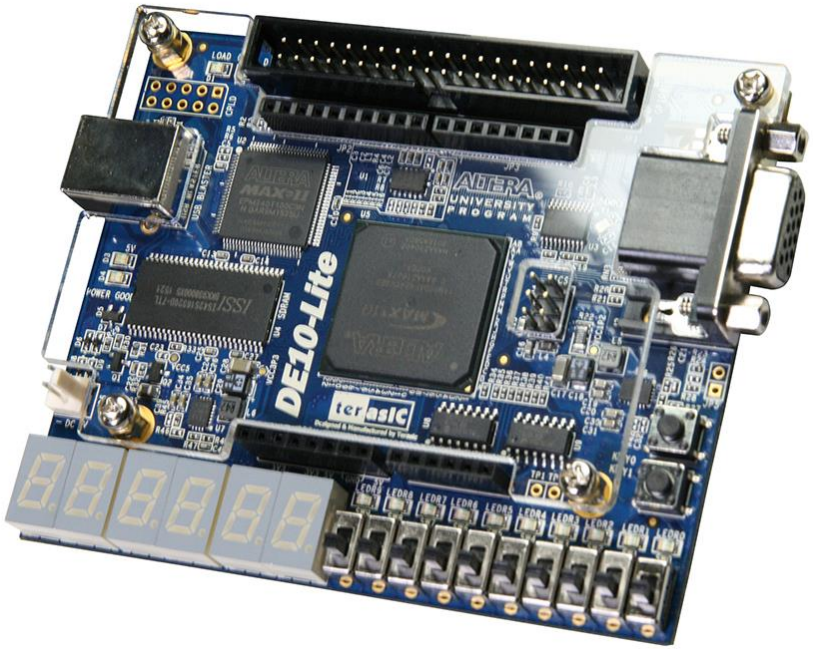
- 林銘波, FPGA系統設計實務入門－使用Verilog HDL:Intel/Altera Quartus, 2018年9月.(全華圖書)
- 並木秀明著, 吳炘廷譯, 正確學會Verilog的16堂課, 旗標圖書, 2012.
- FPGA4student
- fpga4fun
- Youtube: FPGA Projects
- Verilog HDL 教學講義

Course Overview

- Review of Logic Design Fundamentals
- Introduction to Programmable Logic Devices
- Introduction to DE10-Lite, Quartus II and ModelSim-Altera
- Introduction to Verilog HDL
- Digital Logic Design Examples (Combinational & Sequential Circuits)
- DE10-Lite Design Examples
- Small Project Design

Course Overview

- Simulation hardware
  - terasIC(友晶科技)　　DE10-Lite Board開發平台



Course Overview

- Simulation hardware (Demo)

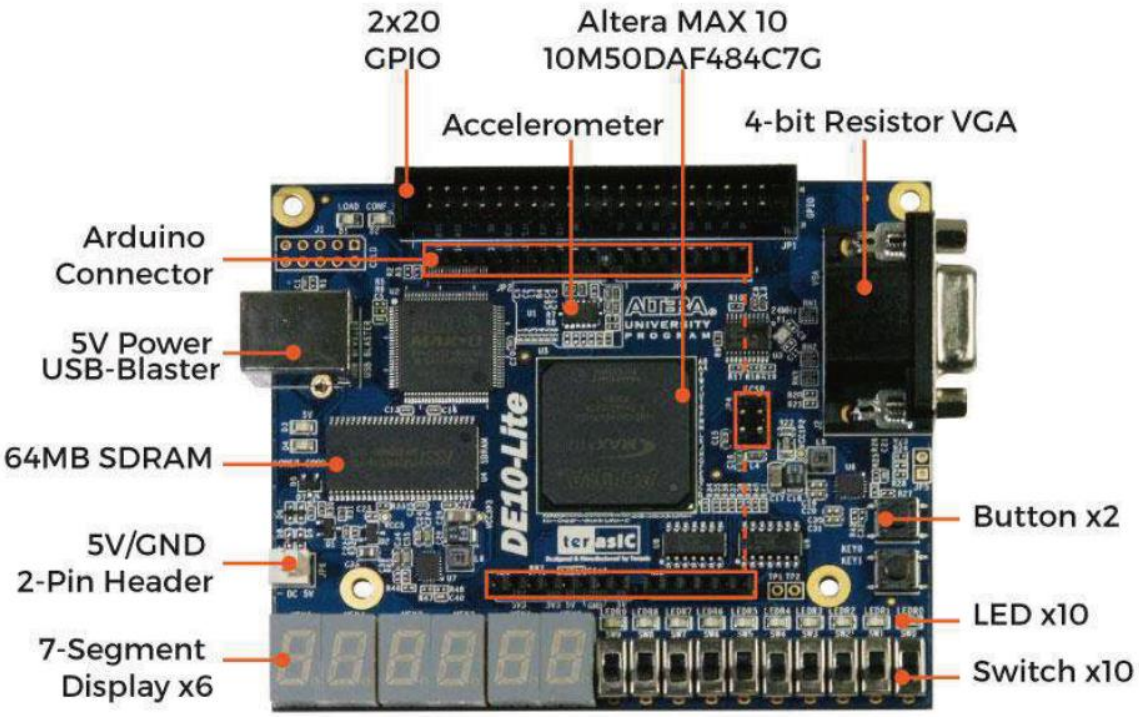


Figure 1-2 Development Board (top view)

Course Overview

- Simulation hardware

Figure 1-3 Development Board (bottom view)

Course Overview

- Simulation software
  - **Intel® Quartus® Prime Lite Edition(includes Nios II EDS), Questa*-Intel® FPGA Edition (Version 18.1)**
  - Plenty of resources available on the Web.
  - Quartus is used for writing Verilog HDL, VHDL, Simulation, and Synthesis.
  - The Altera DE10-Lite board is used for implementation
  - Check MCU Moodle system for more course materials!

What You Should Do?

- **In Class**
  - Listen carefully and be concentrated
  - Practice hard during the assigned time slot
- **After Class**
  - Study hard for those information from the book and the internet
  - Practice actively by yourself!!
  - Practice, Practice, and Practice!!!

Q & A

硬體平台簡介

- 硬體(http://www.terasic.com.tw)
  - 友晶科技 (Terasic) Altera DE系列實驗板

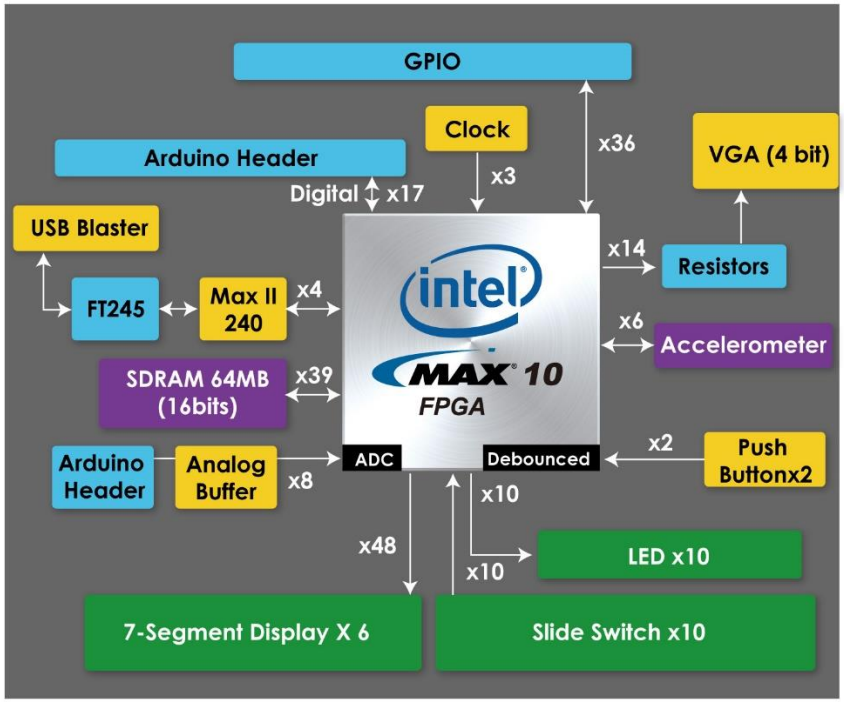
Board	Device Name
DE0	Cyclone III EP3C16F484C6
DE0-Nano	Cyclone IVE EP4CE22F17C6
DE1	Cyclone II EP2C20F484C7
DE2	Cyclone II EP2C35F672C6
DE2-70	Cyclone II EP2C70F896C6
DE2-115	Cyclone IVE EP4CE115F29C7

表 1-1 DE系列實驗板FPGA名稱

MAX 10	10M50DAF484C7G

硬體平台簡介

- 硬體
  - 友晶科技 DE10-Lite 開發板Block Diagram



硬體平台簡介

- **硬體**
  - **友晶科技 DE10-Lite 開發板**
    - FPGA型號 ”MAX 10 10M50DAF484C7G”
    - 具有50K個邏輯單元(LEs)
    - 外接記憶體 64MB的SDRAM，x16 bits data bus
    - 1,638 Kbit M9K Memory
    - 5,888 Kbits user Flash記憶體
    - 144 個 18x18 乘法器
    - 4 個鎖相環(PLLs)
    - 5V DC input

硬體平台簡介

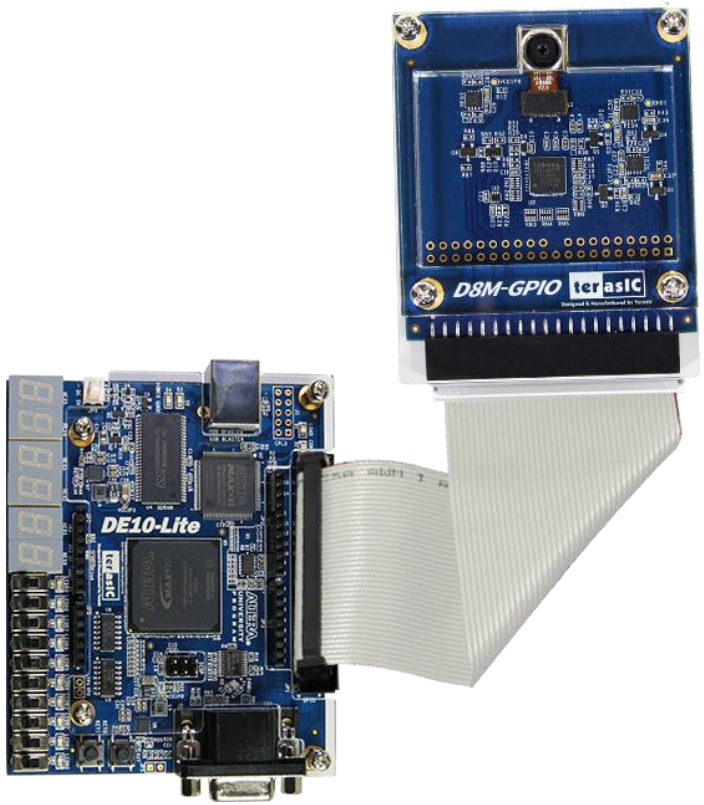
- **硬體**
  - **友晶科技 DE10-Lite 開發板**
    - 內建加速規(accelerometer)感測器
    - 2x20 GPIO 連接器
    - Arduino Uno R3 連接器，包含 6 個 ADC 通道
    - 4 位電阻式 VGAA
    - 10 個 LED
    - 10 個滑動開關
    - 2 個去抖動按鈕
    - 6 個七段顯示器

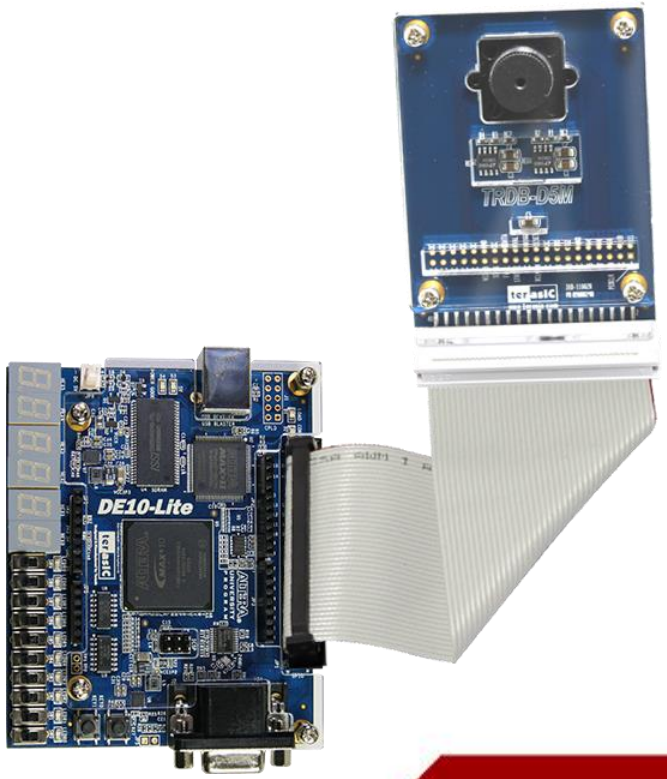
硬體平台簡介

- MTL2(Multi-Touch LCD) 與 DE10-Lite 連接示意圖

硬體平台簡介

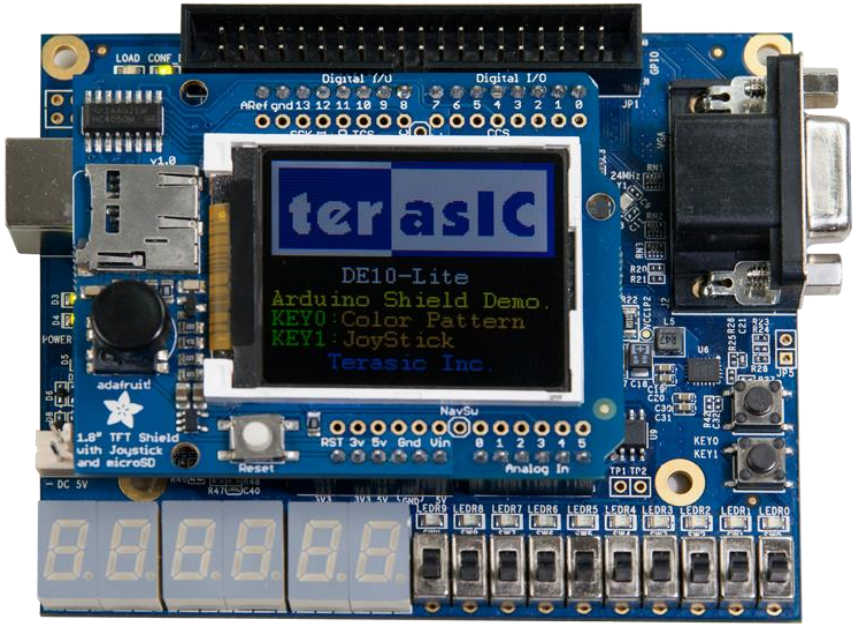
- Camera (D8M-GPIO 與 D5M) 與 DE10-Lite 連接





硬體平台簡介

- Arduino Shield 與 DE10-Lite 連接



硬體平台簡介

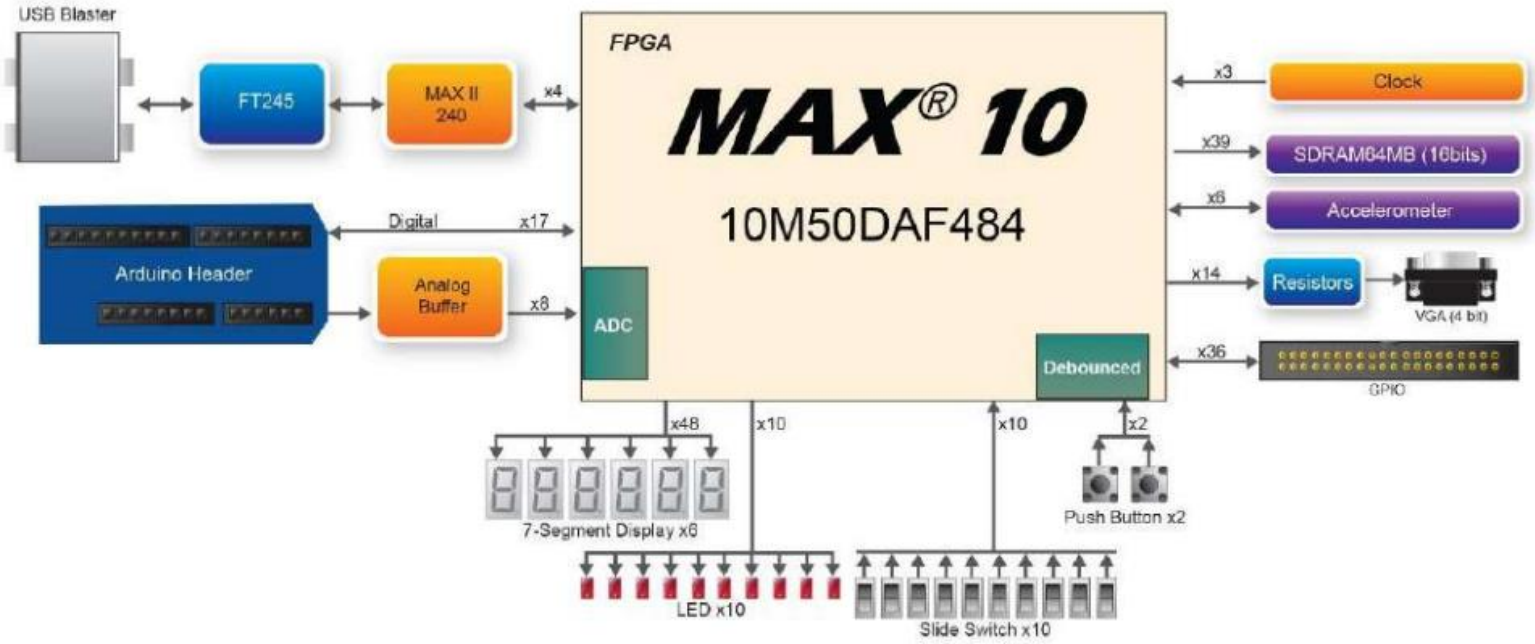


圖 1-4 DE10-Lite 開發板方塊圖

硬體平台簡介

- 時脈電路(Clock Circuitry)

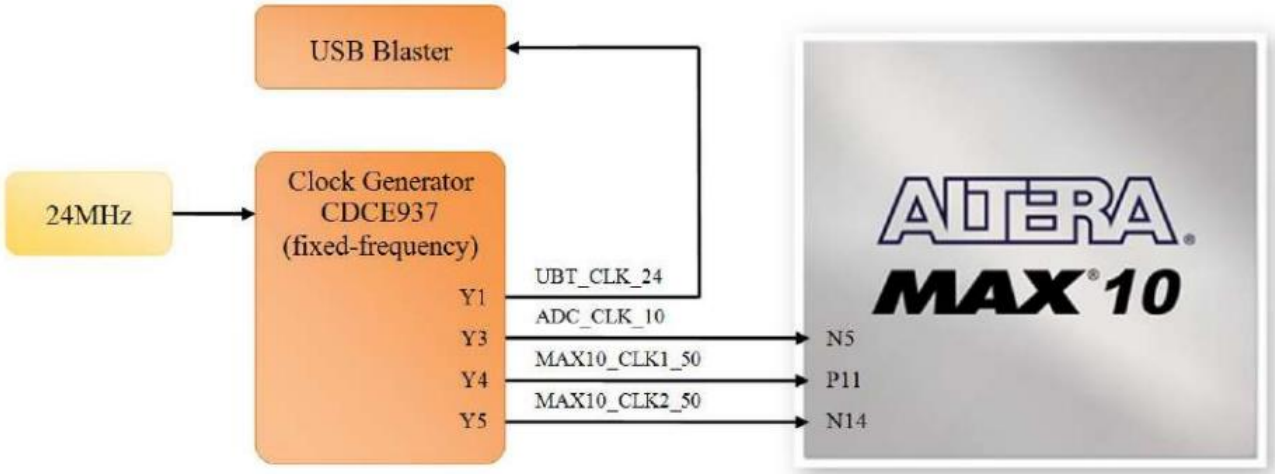


Table 3-2 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description	I/O Standard
ADC_CLK_10	PIN_N5	10 MHz clock input for ADC (Bank 3B)	3.3-V LVTTL
MAX10_CLK1_50	PIN_P11	50 MHz clock input(Bank 3B)	3.3-V LVTTL
MAX10_CLK2_50	PIN_N14	50 MHz clock input(Bank 3B)	3.3-V LVTTL

硬體平台簡介

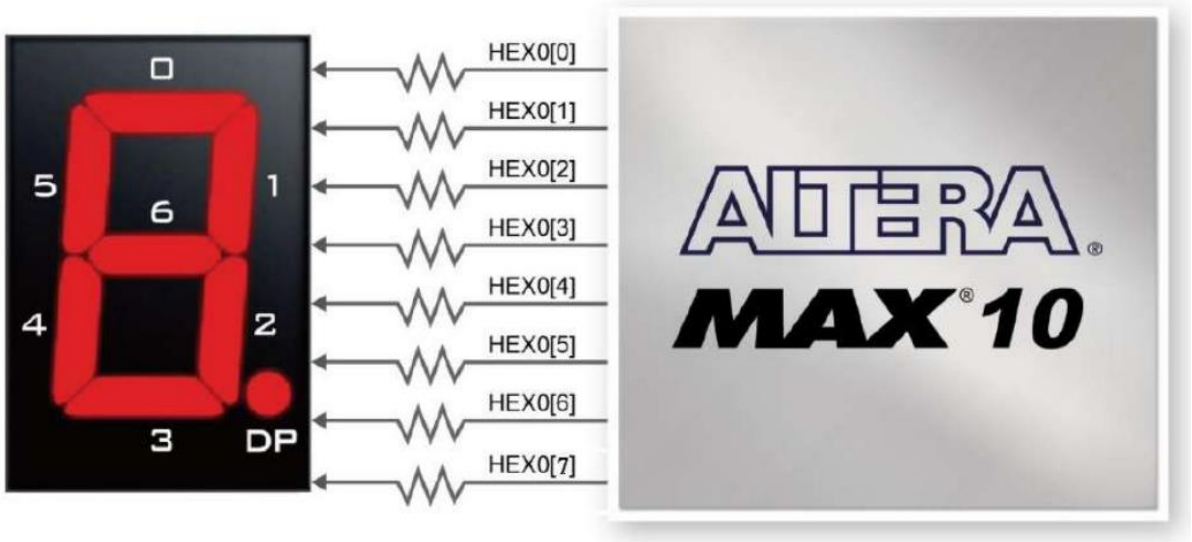
- **LED**
  - DE10-Lite共有10顆紅色LED，每顆都有單腳連接FPGA

Table 3-5 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR0	PIN_A8	LED [0]	3.3-V LVTTL
LEDR1	PIN_A9	LED [1]	3.3-V LVTTL
LEDR2	PIN_A10	LED [2]	3.3-V LVTTL
LEDR3	PIN_B10	LED [3]	3.3-V LVTTL
LEDR4	PIN_D13	LED [4]	3.3-V LVTTL
LEDR5	PIN_C13	LED [5]	3.3-V LVTTL
LEDR6	PIN_E14	LED [6]	3.3-V LVTTL
LEDR7	PIN_D14	LED [7]	3.3-V LVTTL
LEDR8	PIN_A11	LED [8]	3.3-V LVTTL
LEDR9	PIN_B11	LED [9]	3.3-V LVTTL

硬體平台簡介

- 七段顯示器
  - DE10-Lite共有6個七段顯示器，每段編號從0到6，還有DP



硬體平台簡介

- 七段顯示器(HEX00-HEX57對應腳)

Table 3-6 Pin Assignment of 7-segment Displays

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX00	PIN_C14	Seven Segment Digit 0[0]	3.3-V LVTTL
HEX01	PIN_E15	Seven Segment Digit 0[1]	3.3-V LVTTL
HEX02	PIN_C15	Seven Segment Digit 0[2]	3.3-V LVTTL
HEX03	PIN_C16	Seven Segment Digit 0[3]	3.3-V LVTTL
HEX04	PIN_E16	Seven Segment Digit 0[4]	3.3-V LVTTL
HEX05	PIN_D17	Seven Segment Digit 0[5]	3.3-V LVTTL
HEX06	PIN_C17	Seven Segment Digit 0[6]	3.3-V LVTTL
HEX07	PIN_D15	Seven Segment Digit 0[7], DP	3.3-V LVTTL
HEX10	PIN_C18	Seven Segment Digit 1[0]	3.3-V LVTTL
HEX11	PIN_D18	Seven Segment Digit 1[1]	3.3-V LVTTL
HEX12	PIN_E18	Seven Segment Digit 1[2]	3.3-V LVTTL
HEX13	PIN_B16	Seven Segment Digit 1[3]	3.3-V LVTTL

硬體平台簡介

- 七段顯示器(HEX00-HEX57對應腳)

HEX14	PIN_A17	Seven Segment Digit 1[4]	3.3-V LVTTL
HEX15	PIN_A18	Seven Segment Digit 1[5]	3.3-V LVTTL
HEX16	PIN_B17	Seven Segment Digit 1[6]	3.3-V LVTTL
HEX17	PIN_A16	Seven Segment Digit 1[7] , DP	3.3-V LVTTL
HEX20	PIN_B20	Seven Segment Digit 2[0]	3.3-V LVTTL
HEX21	PIN_A20	Seven Segment Digit 2[1]	3.3-V LVTTL
HEX22	PIN_B19	Seven Segment Digit 2[2]	3.3-V LVTTL
HEX23	PIN_A21	Seven Segment Digit 2[3]	3.3-V LVTTL
HEX24	PIN_B21	Seven Segment Digit 2[4]	3.3-V LVTTL
HEX25	PIN_C22	Seven Segment Digit 2[5]	3.3-V LVTTL
HEX26	PIN_B22	Seven Segment Digit 2[6]	3.3-V LVTTL
HEX27	PIN_A19	Seven Segment Digit 2[7] , DP	3.3-V LVTTL
HEX30	PIN_F21	Seven Segment Digit 3[0]	3.3-V LVTTL
HEX31	PIN_E22	Seven Segment Digit 3[1]	3.3-V LVTTL
HEX32	PIN_E21	Seven Segment Digit 3[2]	3.3-V LVTTL
HEX33	PIN_C19	Seven Segment Digit 3[3]	3.3-V LVTTL
HEX34	PIN_C20	Seven Segment Digit 3[4]	3.3-V LVTTL
HEX35	PIN_D19	Seven Segment Digit 3[5]	3.3-V LVTTL
HEX36	PIN_E17	Seven Segment Digit 3[6]	3.3-V LVTTL
HEX37	PIN_D22	Seven Segment Digit 3[7] , DP	3.3-V LVTTL

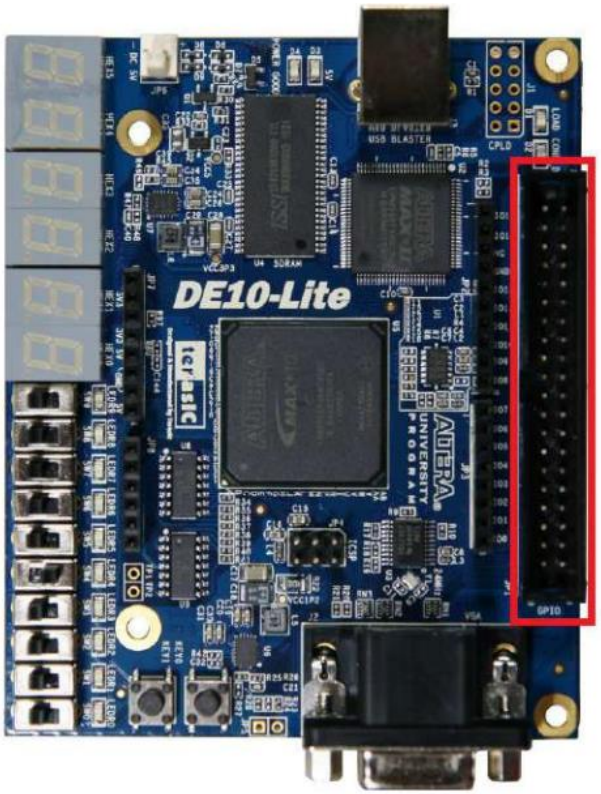
硬體平台簡介

- 七段顯示器(HEX00-HEX57對應腳)

HEX40	PIN_F18	Seven Segment Digit 4[0]	3.3-V LVTTL
HEX41	PIN_E20	Seven Segment Digit 4[1]	3.3-V LVTTL
HEX42	PIN_E19	Seven Segment Digit 4[2]	3.3-V LVTTL
HEX43	PIN_J18	Seven Segment Digit 4[3]	3.3-V LVTTL
HEX44	PIN_H19	Seven Segment Digit 4[4]	3.3-V LVTTL
HEX45	PIN_F19	Seven Segment Digit 4[5]	3.3-V LVTTL
HEX46	PIN_F20	Seven Segment Digit 4[6]	3.3-V LVTTL
HEX47	PIN_F17	Seven Segment Digit 4[7] , DP	3.3-V LVTTL
HEX50	PIN_J20	Seven Segment Digit 5[0]	3.3-V LVTTL
HEX51	PIN_K20	Seven Segment Digit 5[1]	3.3-V LVTTL
HEX52	PIN_L18	Seven Segment Digit 5[2]	3.3-V LVTTL
HEX53	PIN_N18	Seven Segment Digit 5[3]	3.3-V LVTTL
HEX54	PIN_M20	Seven Segment Digit 5[4]	3.3-V LVTTL
HEX55	PIN_N19	Seven Segment Digit 5[5]	3.3-V LVTTL
HEX56	PIN_N20	Seven Segment Digit 5[6]	3.3-V LVTTL
HEX57	PIN_L19	Seven Segment Digit 5[7] , DP	3.3-V LVTTL

硬體平台簡介

- **2x20 GPIO 擴充接腳**



GPIO (JP1)

PIN_V10	GPIO_[0]	1	2	GPIO_[1]	PIN_W10
PIN_V9	GPIO_[2]	3	4	GPIO_[3]	PIN_W9
PIN_V8	GPIO_[4]	5	6	GPIO_[5]	PIN_W8
PIN_V7	GPIO_[6]	7	8	GPIO_[7]	PIN_W7
PIN_W6	GPIO_[8]	9	10	GPIO_[9]	PIN_V5
	5V	11	12	GND	
PIN_W5	GPIO_[10]	13	14	GPIO_[11]	PIN_AA15
PIN_AA14	GPIO_[12]	15	16	GPIO_[13]	PIN_W13
PIN_W12	GPIO_[14]	17	18	GPIO_[15]	PIN_AB13
PIN_AB12	GPIO_[16]	19	20	GPIO_[17]	PIN_Y11
PIN_AB11	GPIO_[18]	21	22	GPIO_[19]	PIN_W11
PIN_AB10	GPIO_[20]	23	24	GPIO_[21]	PIN_AA10
PIN_AA9	GPIO_[22]	25	26	GPIO_[23]	PIN_Y8
PIN_AA8	GPIO_[24]	27	28	GPIO_[25]	PIN_Y7
	3.3V	29	30	GND	
PIN_AA7	GPIO_[26]	31	32	GPIO_[27]	PIN_Y6
PIN_AA6	GPIO_[28]	33	34	GPIO_[29]	PIN_Y5
PIN_AA5	GPIO_[30]	35	36	GPIO_[31]	PIN_Y4
PIN_AB3	GPIO_[32]	37	38	GPIO_[33]	PIN_Y3
PIN_AB2	GPIO_[34]	39	40	GPIO_[35]	PIN_AA2

圖 3-18 DE10-Lite GPIO接腳圖

硬體平台簡介

- **2x20 GPIO 擴充接腳**

Table 3-7 Show all Pin Assignment of Expansion Headers

Signal Name	FPGA Pin No.	Description	I/O Standard
GPIO_0	PIN_V10	GPIO Connection [0]	3.3-V LVTTL
GPIO_1	PIN_W10	GPIO Connection [1]	3.3-V LVTTL
GPIO_2	PIN_V9	GPIO Connection [2]	3.3-V LVTTL
GPIO_3	PIN_W9	GPIO Connection [3]	3.3-V LVTTL
GPIO_4	PIN_V8	GPIO Connection [4]	3.3-V LVTTL
GPIO_5	PIN_W8	GPIO Connection [5]	3.3-V LVTTL
GPIO_6	PIN_V7	GPIO Connection [6]	3.3-V LVTTL
GPIO_7	PIN_W7	GPIO Connection [7]	3.3-V LVTTL
GPIO_8	PIN_W6	GPIO Connection [8]	3.3-V LVTTL
GPIO_9	PIN_V5	GPIO Connection [9]	3.3-V LVTTL
GPIO_10	PIN_W5	GPIO Connection [10]	3.3-V LVTTL
GPIO_11	PIN_AA15	GPIO Connection [11]	3.3-V LVTTL
GPIO_12	PIN_AA14	GPIO Connection [12]	3.3-V LVTTL
GPIO_13	PIN_W13	GPIO Connection [13]	3.3-V LVTTL
GPIO_14	PIN_W12	GPIO Connection [14]	3.3-V LVTTL
GPIO_15	PIN_AB13	GPIO Connection [15]	3.3-V LVTTL
GPIO_16	PIN_AB12	GPIO Connection [16]	3.3-V LVTTL
GPIO_17	PIN_Y11	GPIO Connection [17]	3.3-V LVTTL

硬體平台簡介

- **2x20 GPIO 擴充接腳**

GPIO_18	PIN_AB11	GPIO Connection [18]	3.3-V LVTTL
GPIO_19	PIN_W11	GPIO Connection [19]	3.3-V LVTTL
GPIO_20	PIN_AB10	GPIO Connection [20]	3.3-V LVTTL
GPIO_21	PIN_AA10	GPIO Connection [21]	3.3-V LVTTL
GPIO_22	PIN_AA9	GPIO Connection [22]	3.3-V LVTTL
GPIO_23	PIN_Y8	GPIO Connection [23]	3.3-V LVTTL
GPIO_24	PIN_AA8	GPIO Connection [24]	3.3-V LVTTL
GPIO_25	PIN_Y7	GPIO Connection [25]	3.3-V LVTTL
GPIO_26	PIN_AA7	GPIO Connection [26]	3.3-V LVTTL
GPIO_27	PIN_Y6	GPIO Connection [27]	3.3-V LVTTL
GPIO_28	PIN_AA6	GPIO Connection [28]	3.3-V LVTTL
GPIO_29	PIN_Y5	GPIO Connection [29]	3.3-V LVTTL
GPIO_30	PIN_AA5	GPIO Connection [30]	3.3-V LVTTL
GPIO_31	PIN_Y4	GPIO Connection [31]	3.3-V LVTTL
GPIO_32	PIN_AB3	GPIO Connection [32]	3.3-V LVTTL
GPIO_33	PIN_Y3	GPIO Connection [33]	3.3-V LVTTL
GPIO_34	PIN_AB2	GPIO Connection [34]	3.3-V LVTTL
GPIO_35	PIN_AA2	GPIO Connection [35]	3.3-V LVTTL

硬體平台簡介

- **按鈕(Button)**
  - DE10-Lite共有兩個按鈕，這些按鈕都接上了施密特觸發器(Schmitt trigger)來對按鈕去除彈跳 (debounce)。

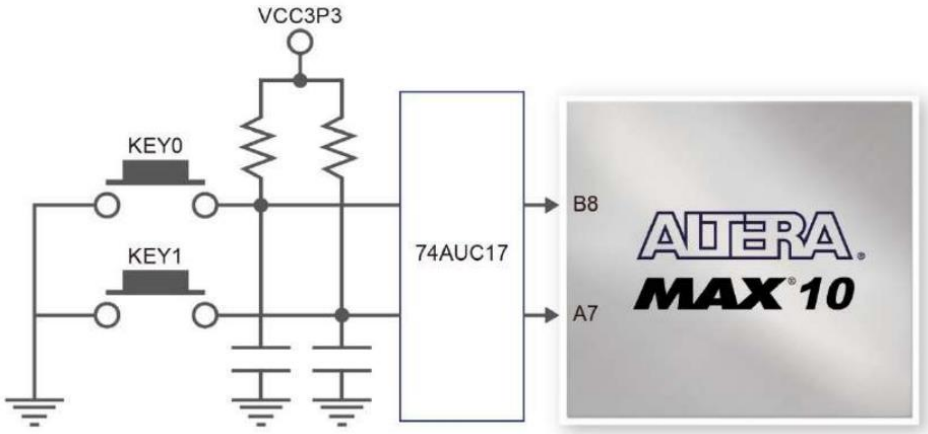


Table 3-3 Pin Assignment of Push-buttons

Signal Name	FPGA Pin No.	Description	I/O Standard
KEY0	PIN_B8	Push-button[0]	3.3 V SCHMITT TRIGGER"
KEY1	PIN_A7	Push-button[1]	3.3 V SCHMITT TRIGGER"

硬體平台簡介

- **指撥開關(Switch)**
  - DE10-Lite有10個指撥開關(slide switches)，這些開關並未接上施密特觸發器，也因此不具有防彈跳的功能。

Table 3-4 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTL
SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTL
SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTL
SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTL
SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTL
SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTL
SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTL
SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTL
SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTL
SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTL

硬體平台簡介

- **VGA**
  - DE10-Lite支援標準 VGA 解析度 (640x480 pixels, at 25 MHz)。

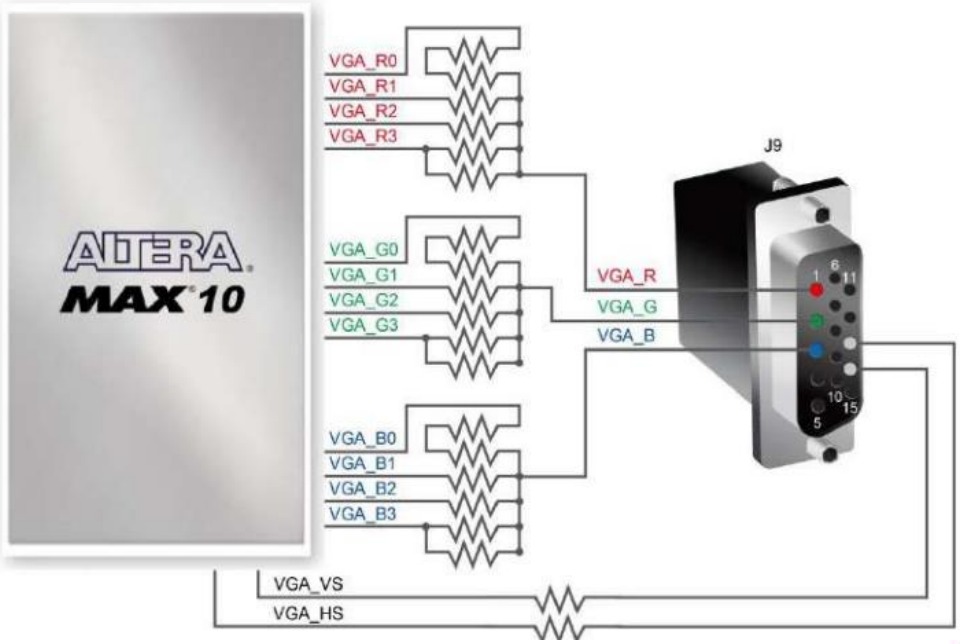


圖 3-21 DE10-Lite 與 VGA連接圖

硬體平台簡介

- **VGA**
  - VGA水平與垂直時序規格

Table 3-9 VGA Horizontal Timing Specification

VGA mode		*Horizontal Timing Spec*				
Configuration	*Resolution(HxV)*	*a(pixel clock cycle)*	*b(pixel clock cycle)*	*c(pixel clock cycle)*	*d(pixel clock cycle)*	*Pixel clock(MHz)*
VGA(60Hz)	640x480	96	48	640	16	25

Table 3-10 VGA Vertical Timing Specification

VGA mode		*Vertical Timing Spec*				
Configuration	*Resolution(HxV)*	*a(lines)*	*b(lines)*	*c(lines)*	*d(lines)*	*Pixel clock(MHz)*
VGA(60Hz)	640x480	2	33	480	10	25

硬體平台簡介

- **VGA(pin assignment for 4-bit DAC)**
  - 要控制 VGA 要知道 FGPA 拉出來的接腳

Table 3-11 Pin Assignment of VGA

Signal Name	FPGA Pin No.	Description	I/O Standard
VGA_R0	PIN_AA1	VGA Red[0]	3.3-V LVTTL
VGA_R1	PIN_V1	VGA Red[1]	3.3-V LVTTL
VGA_R2	PIN_Y2	VGA Red[2]	3.3-V LVTTL
VGA_R3	PIN_Y1	VGA Red[3]	3.3-V LVTTL
VGA_G0	PIN_W1	VGA Green[0]	3.3-V LVTTL
VGA_G1	PIN_T2	VGA Green[1]	3.3-V LVTTL
VGA_G2	PIN_R2	VGA Green[2]	3.3-V LVTTL
VGA_G3	PIN_R1	VGA Green[3]	3.3-V LVTTL
VGA_B0	PIN_P1	VGA Blue[0]	3.3-V LVTTL
VGA_B1	PIN_T1	VGA Blue[1]	3.3-V LVTTL
VGA_B2	PIN_P4	VGA Blue[2]	3.3-V LVTTL
VGA_B3	PIN_N2	VGA Blue[3]	3.3-V LVTTL
VGA_HS	PIN_N3	VGA Horizontal sync	3.3-V LVTTL
VGA_VS	PIN_N1	VGA Vertical sync	3.3-V LVTTL

硬體平台簡介

- **64MB SDRAM (32Mx16)**

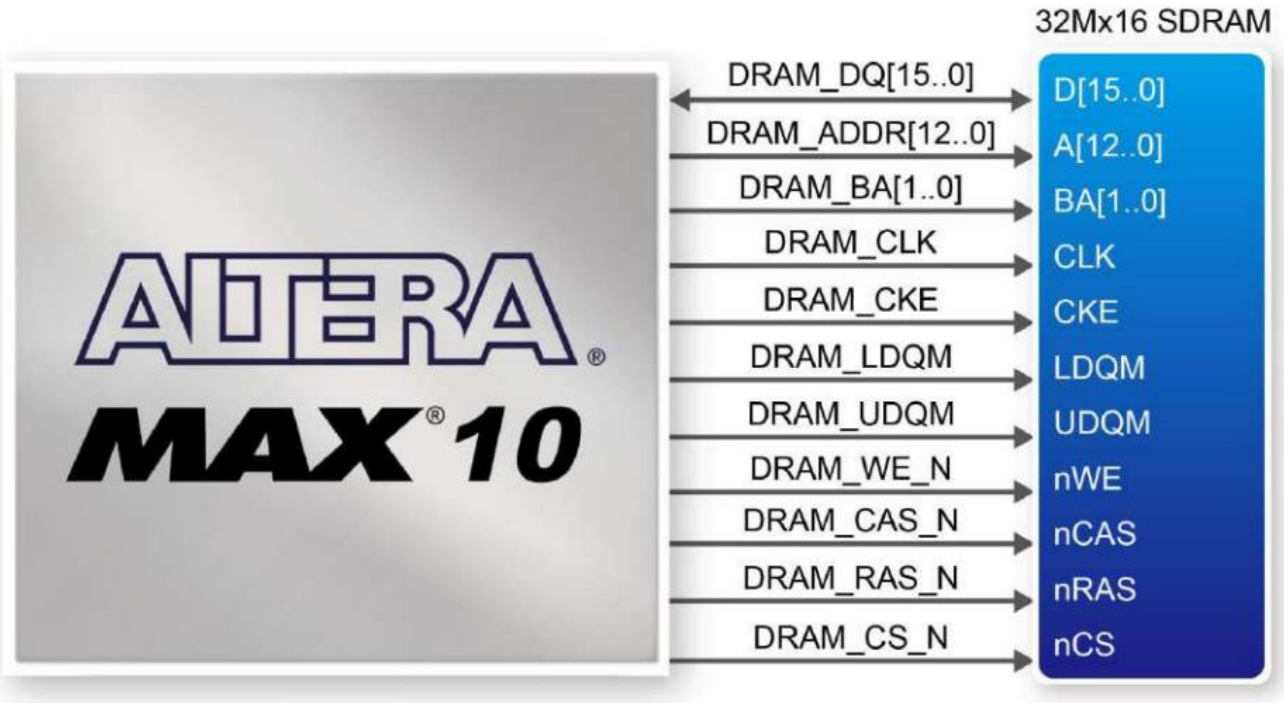


圖 3-21 DE10-Lite 與 SDRAM 連接圖

硬體平台簡介

- **64MB SDRAM (pin assignment)**

Signal Name	FPGA Pin No.	Description	I/O Standard
DRAM_ADDR0	PIN_U17	SDRAM Address[0]	3.3-V LVTTL
DRAM_ADDR1	PIN_W19	SDRAM Address[1]	3.3-V LVTTL
DRAM_ADDR2	PIN_V18	SDRAM Address[2]	3.3-V LVTTL
DRAM_ADDR3	PIN_U18	SDRAM Address[3]	3.3-V LVTTL
DRAM_ADDR4	PIN_U19	SDRAM Address[4]	3.3-V LVTTL
DRAM_ADDR5	PIN_T18	SDRAM Address[5]	3.3-V LVTTL
DRAM_ADDR6	PIN_T19	SDRAM Address[6]	3.3-V LVTTL
DRAM_ADDR7	PIN_R18	SDRAM Address[7]	3.3-V LVTTL
DRAM_ADDR8	PIN_P18	SDRAM Address[8]	3.3-V LVTTL
DRAM_ADDR9	PIN_P19	SDRAM Address[9]	3.3-V LVTTL
DRAM_ADDR10	PIN_T20	SDRAM Address[10]	3.3-V LVTTL
DRAM_ADDR11	PIN_P20	SDRAM Address[11]	3.3-V LVTTL
DRAM_ADDR12	PIN_R20	SDRAM Address[12]	3.3-V LVTTL
DRAM_DQ0	PIN_Y21	SDRAM Data[0]	3.3-V LVTTL
DRAM_DQ1	PIN_Y20	SDRAM Data[1]	3.3-V LVTTL
DRAM_DQ2	PIN_AA22	SDRAM Data[2]	3.3-V LVTTL
DRAM_DQ3	PIN_AA21	SDRAM Data[3]	3.3-V LVTTL
DRAM_DQ4	PIN_Y22	SDRAM Data[4]	3.3-V LVTTL
DRAM_DQ5	PIN_W22	SDRAM Data[5]	3.3-V LVTTL
DRAM_DQ6	PIN_W20	SDRAM Data[6]	3.3-V LVTTL

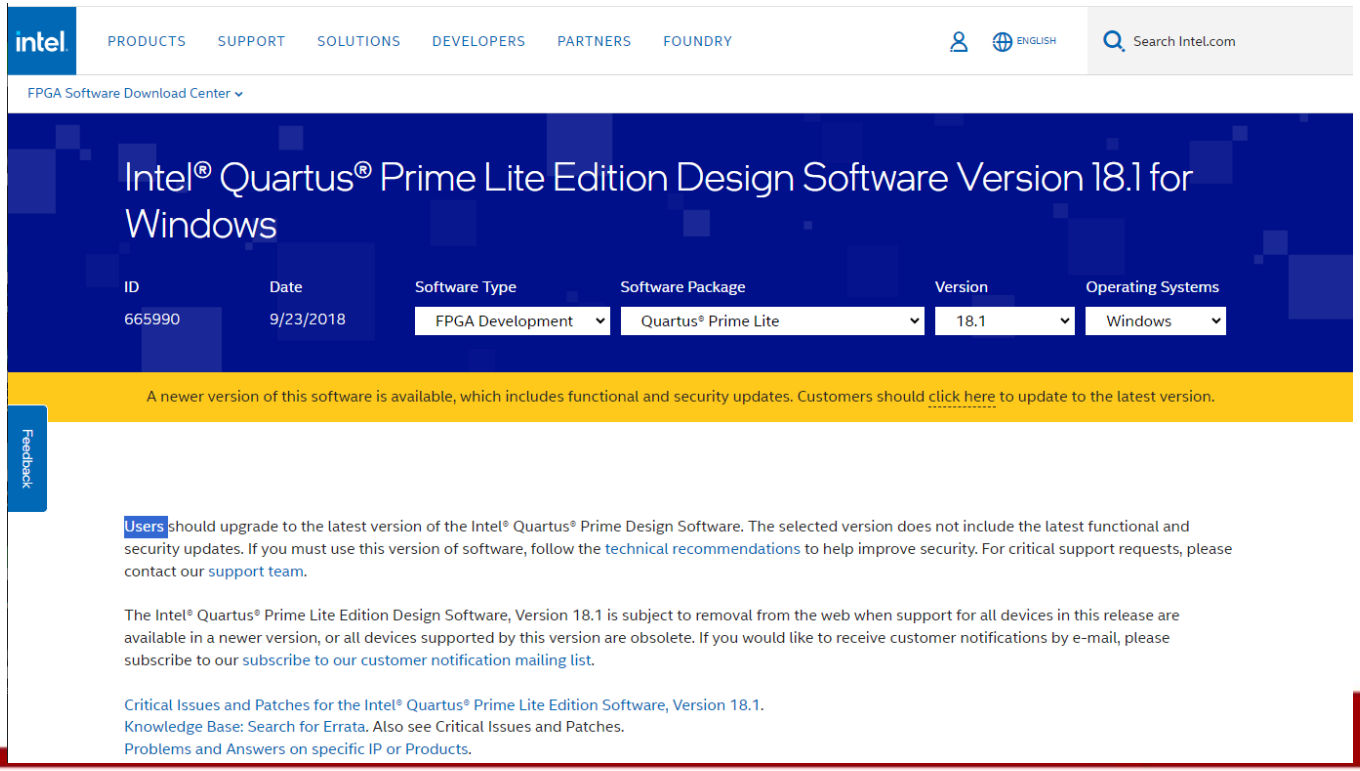
硬體平台簡介

- **64MB SDRAM (pin assignment)**

DRAM_DQ7	PIN_V21	SDRAM Data[7]	3.3-V LVTTL
DRAM_DQ8	PIN_P21	SDRAM Data[8]	3.3-V LVTTL
DRAM_DQ9	PIN_J22	SDRAM Data[9]	3.3-V LVTTL
DRAM_DQ10	PIN_H21	SDRAM Data[10]	3.3-V LVTTL
DRAM_DQ11	PIN_H22	SDRAM Data[11]	3.3-V LVTTL
DRAM_DQ12	PIN_G22	SDRAM Data[12]	3.3-V LVTTL
DRAM_DQ13	PIN_G20	SDRAM Data[13]	3.3-V LVTTL
DRAM_DQ14	PIN_G19	SDRAM Data[14]	3.3-V LVTTL
DRAM_DQ15	PIN_F22	SDRAM Data[15]	3.3-V LVTTL
DRAM_BA0	PIN_T21	SDRAM Bank Address[0]	3.3-V LVTTL
DRAM_BA1	PIN_T22	SDRAM Bank Address[1]	3.3-V LVTTL
DRAM_LDQM	PIN_V22	SDRAM byte Data Mask[0]	3.3-V LVTTL
DRAM_UDQM	PIN_J21	SDRAM byte Data Mask[1]	3.3-V LVTTL
DRAM_RAS_N	PIN_U22	SDRAM Row Address Strobe	3.3-V LVTTL
DRAM_CAS_N	PIN_U21	SDRAM Column Address Strobe	3.3-V LVTTL
DRAM_CKE	PIN_N22	SDRAM Clock Enable	3.3-V LVTTL
DRAM_CLK	PIN_L14	SDRAM Clock	3.3-V LVTTL
DRAM_WE_N	PIN_V20	SDRAM Write Enable	3.3-V LVTTL
DRAM_CS_N	PIN_U20	SDRAM Chip Select	3.3-V LVTTL

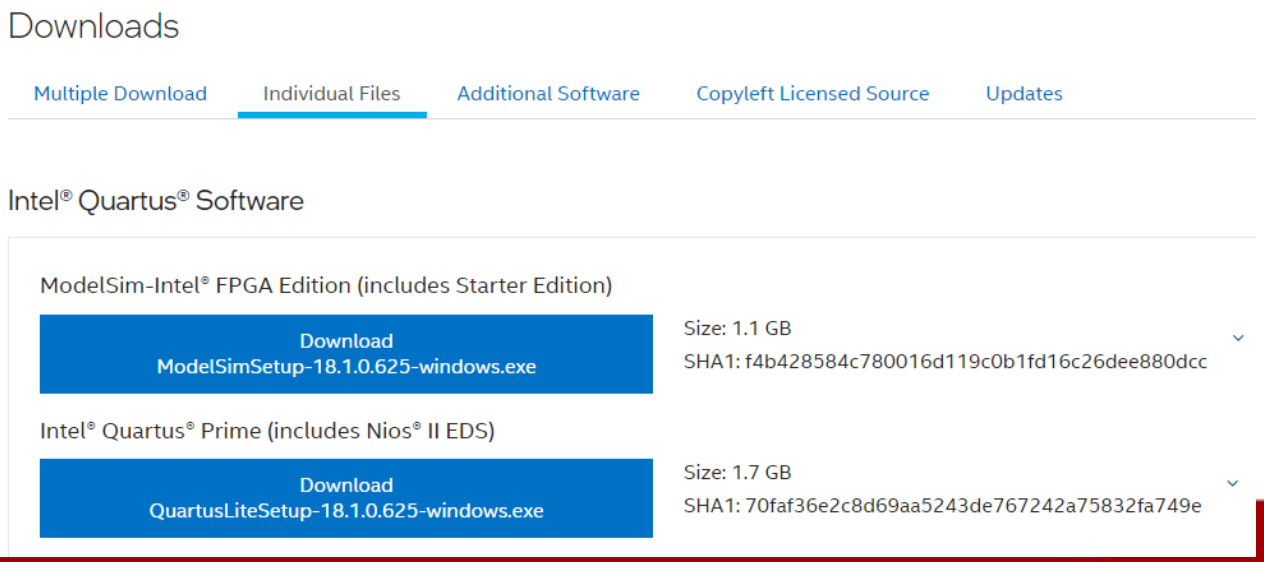
Software Installation

1) Download and install "Intel® Quartus® Prime Lite Edition Version 18.1 for Windows" (Free)



Software Installation

- Download the following, on "Individual Files" tab:
  - ModelSim-Intel® FPGA Edition (includes Starter Edition)
  - Intel® Quartus® Prime (includes Nios® II EDS)
  - Devices - Intel® MAX® 10 Device Support

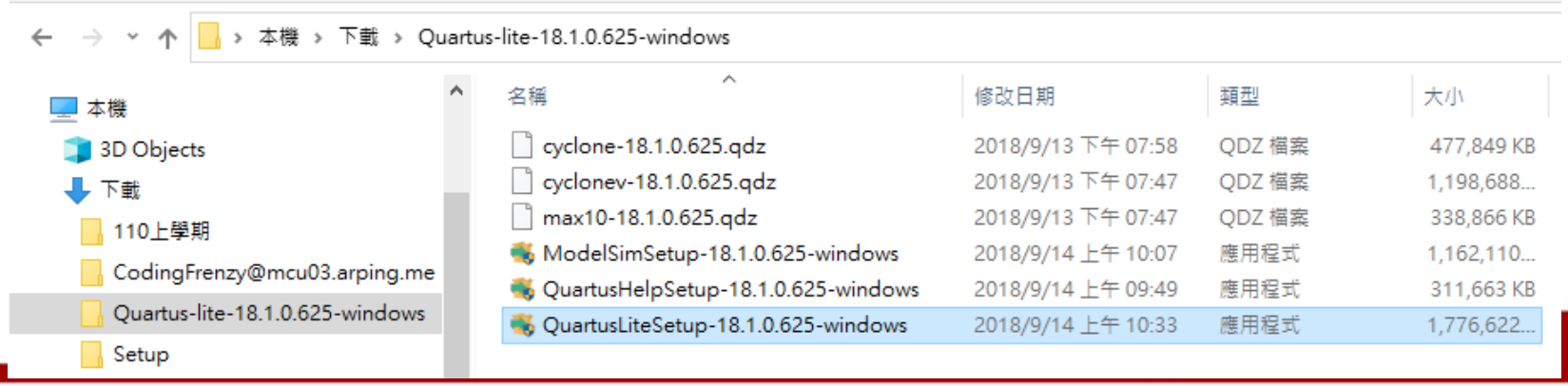


Software Installation

- Once you downloaded the above three files, install QuartusLiteSetup-18.1.0.625-windows.exe, which will select to install the other two as well. In my case, all were installed in: C:\intelFPGA_lite\18.1

Minimum Disk

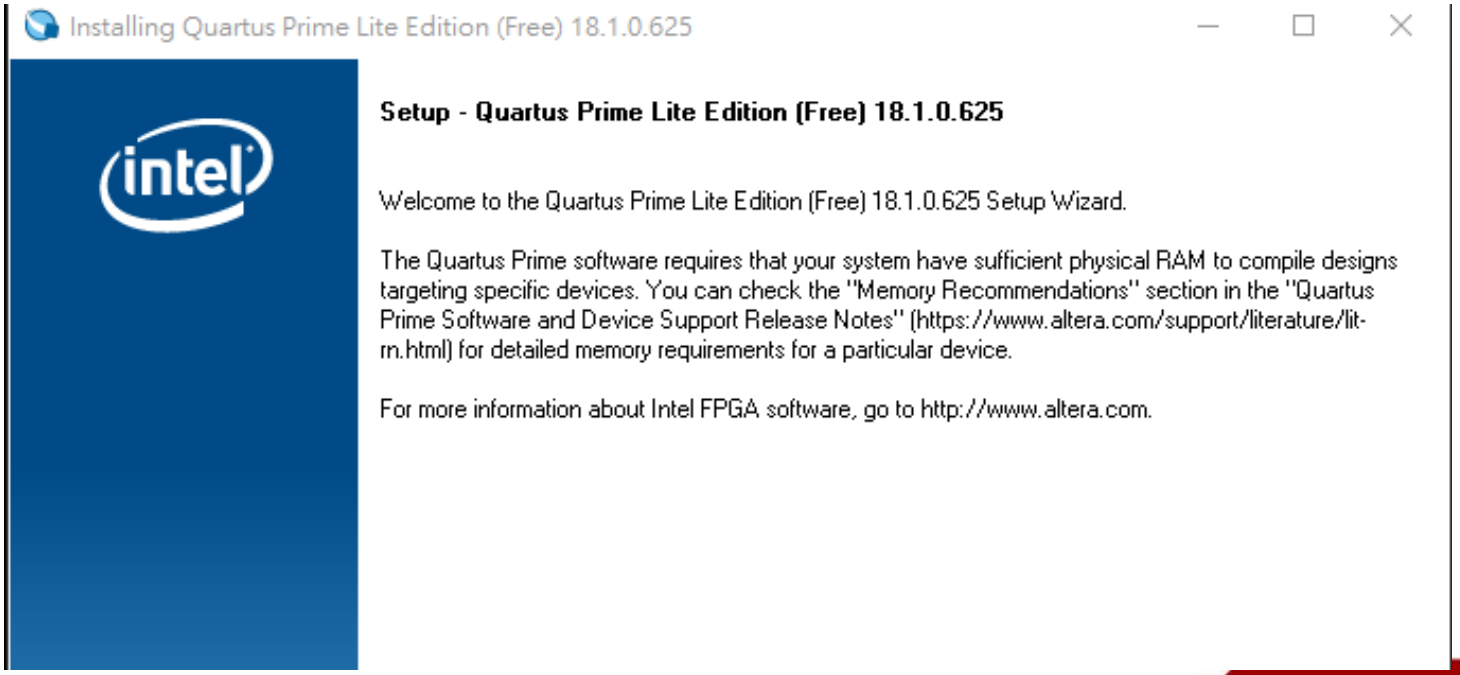
- Intel® Quartus® Prime Lite Edition Design Software (14 GB)



Software Installation

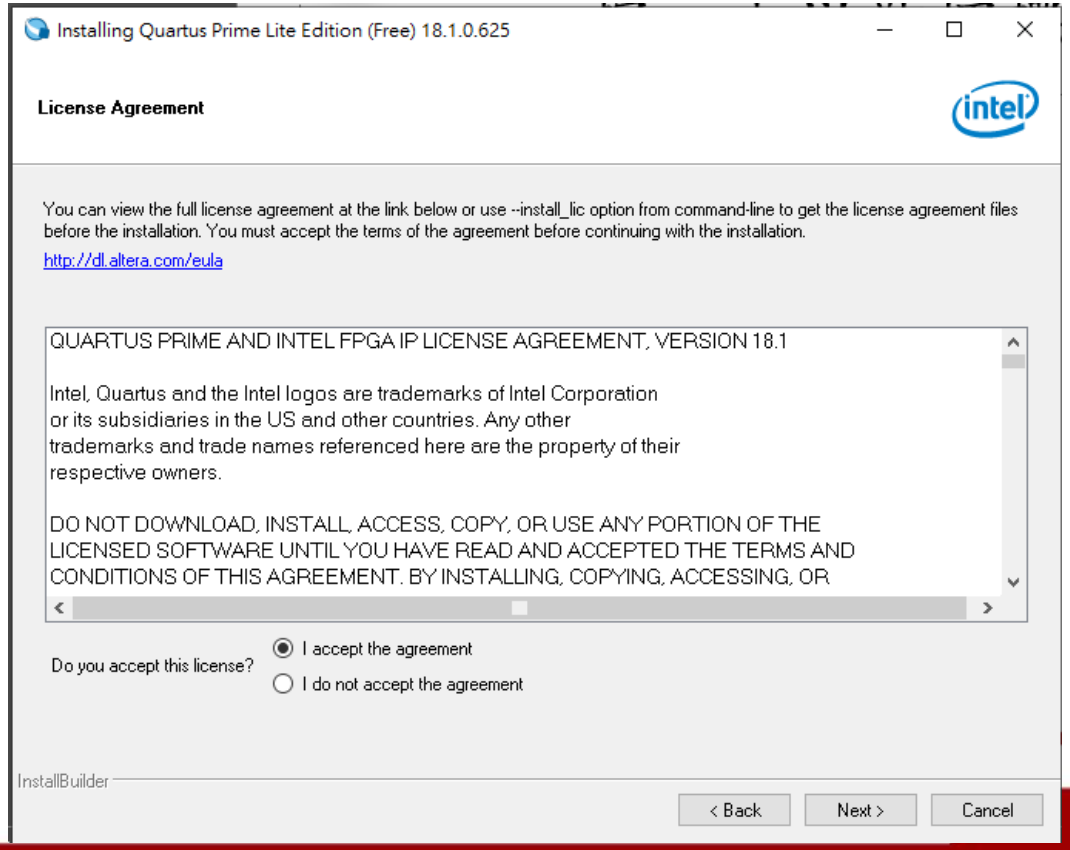
- The first page of installing

QuartusLiteSetup-18.1.0.625-windows.exe



Software Installation

- License agreement

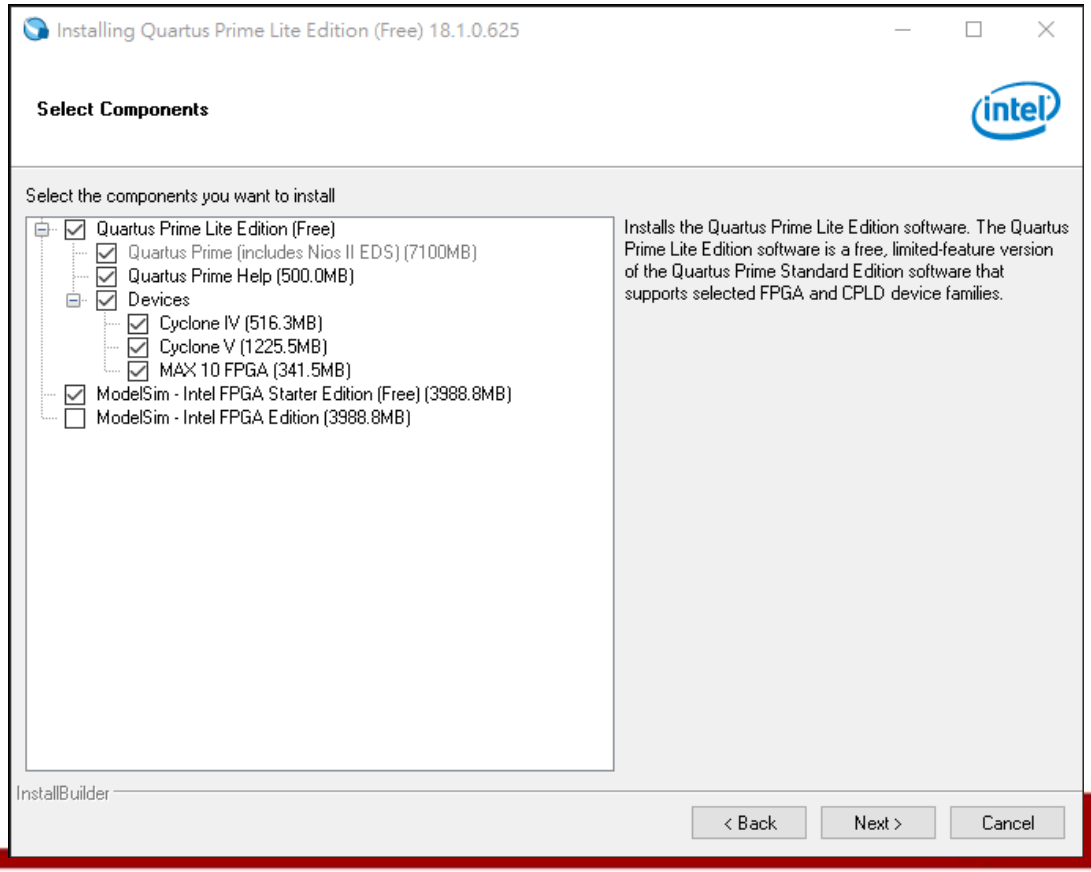


Software Installation

- Select installation directory in:
  C:\intelFPGA_lite\18.1

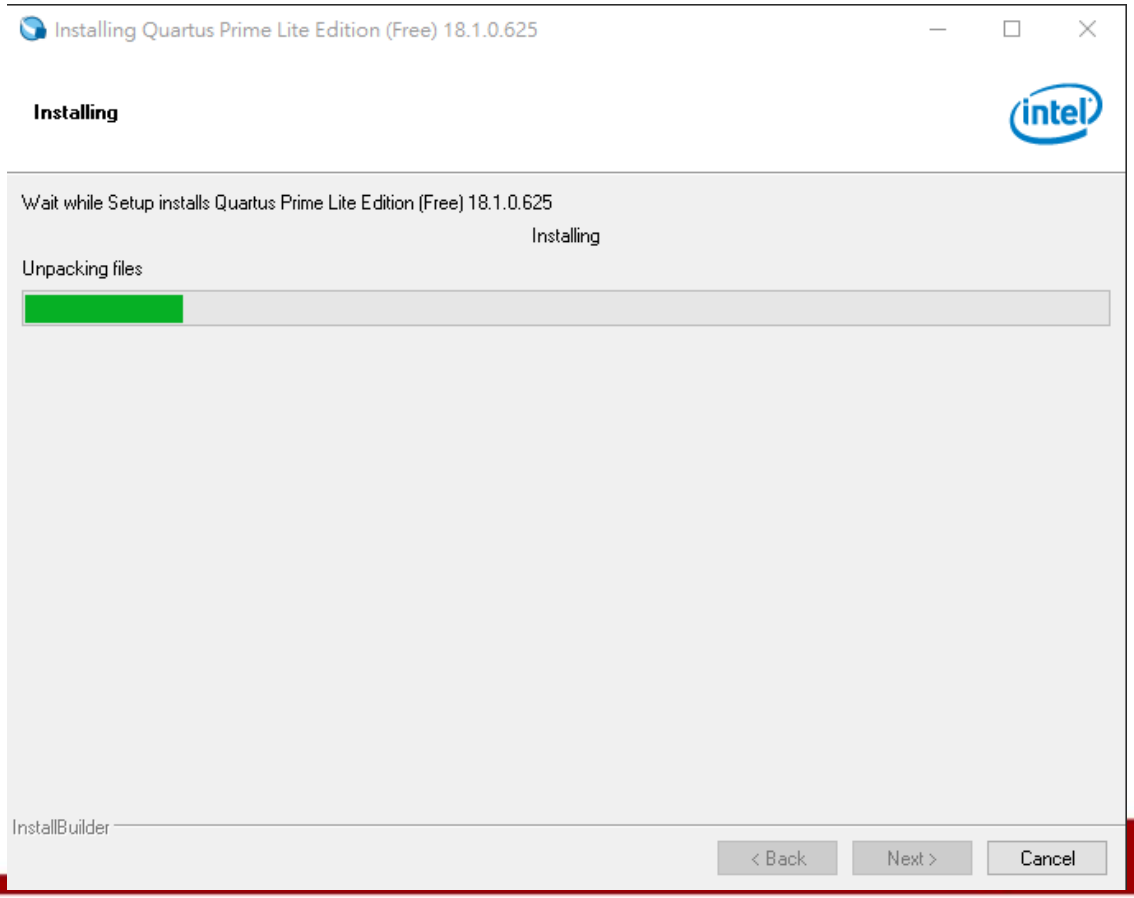
Software Installation

- Select Components



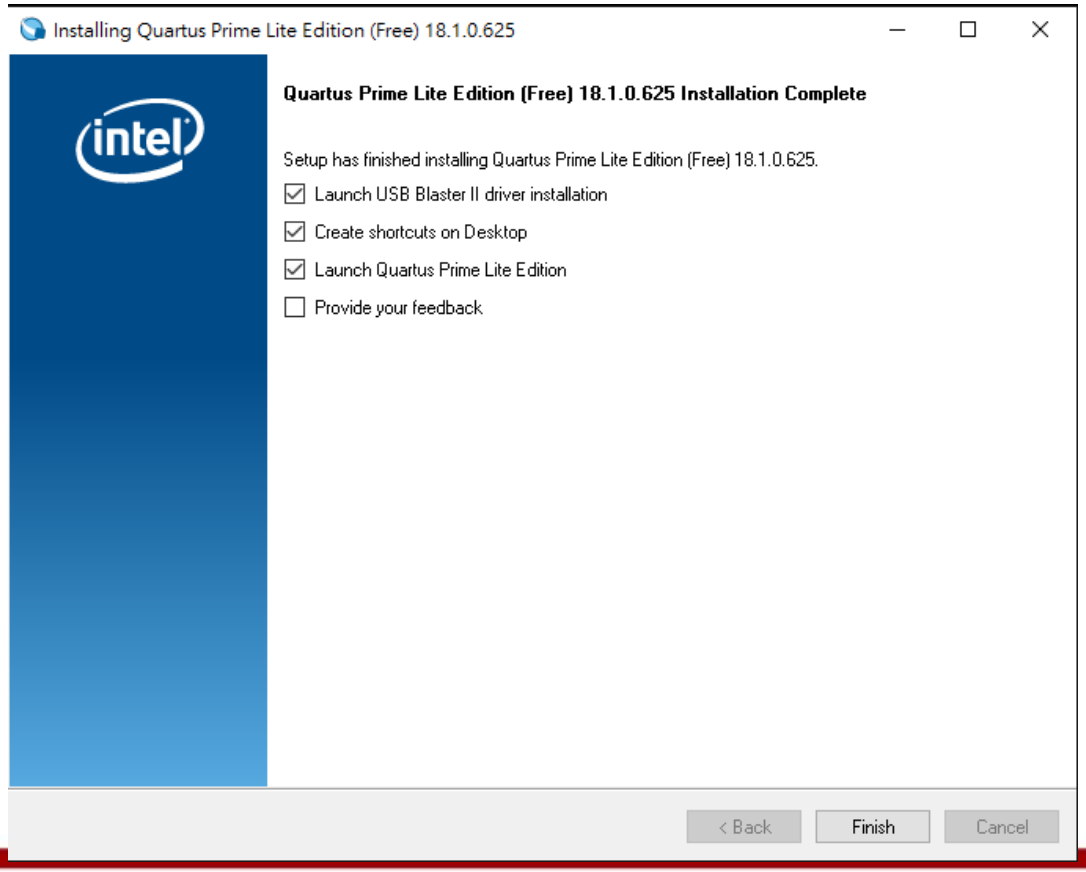
Software Installation

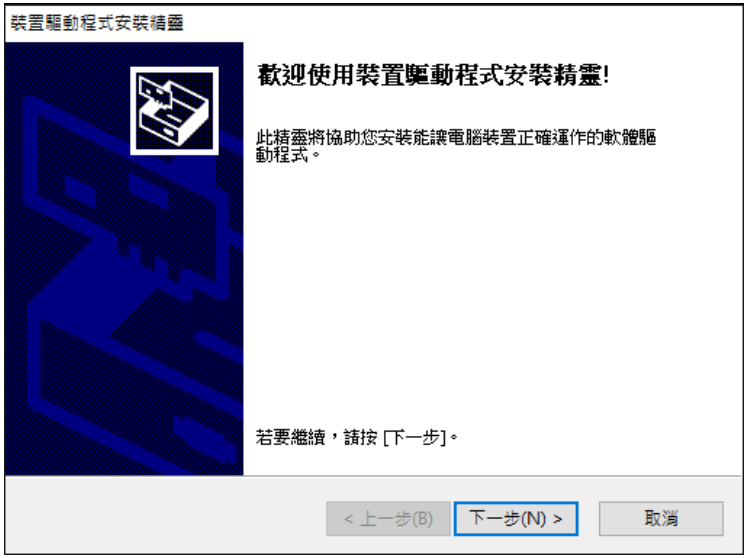
- Installing



Software Installation

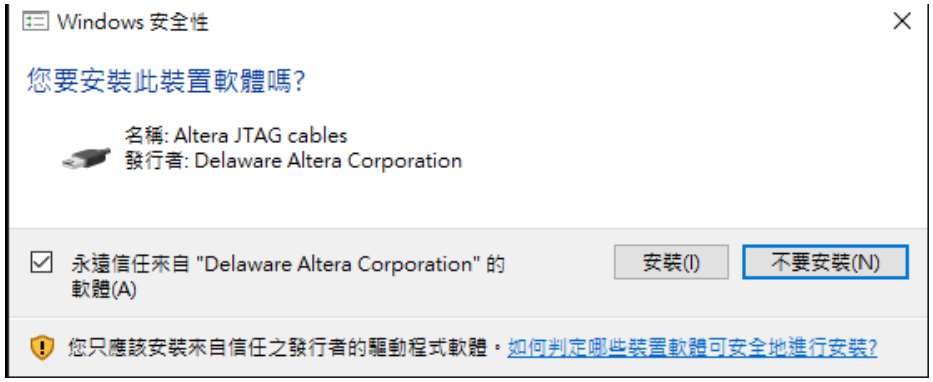
- Installation Complete and 啟動驅動程式安裝

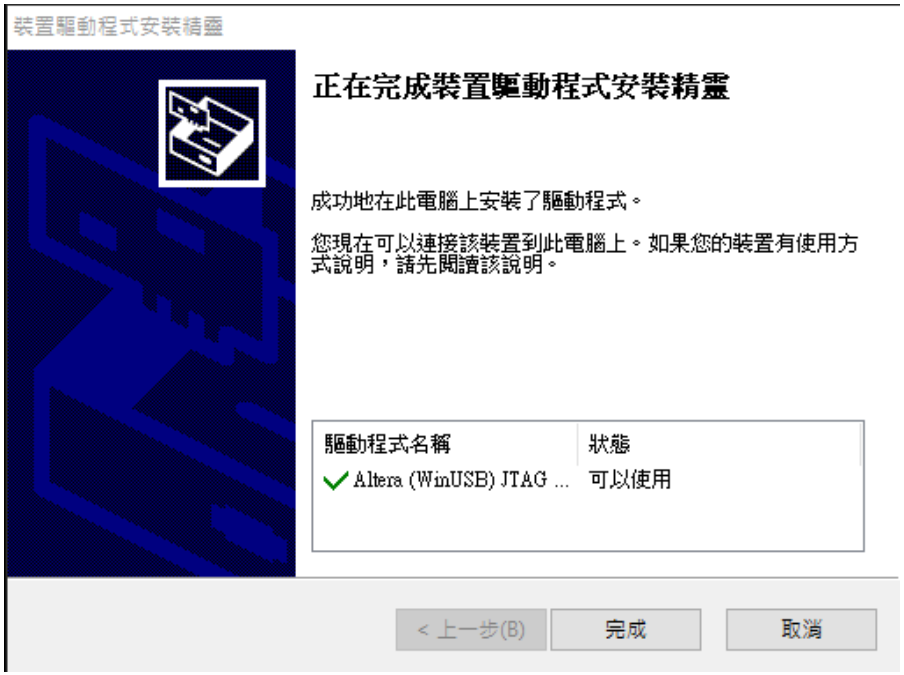




Software Installation

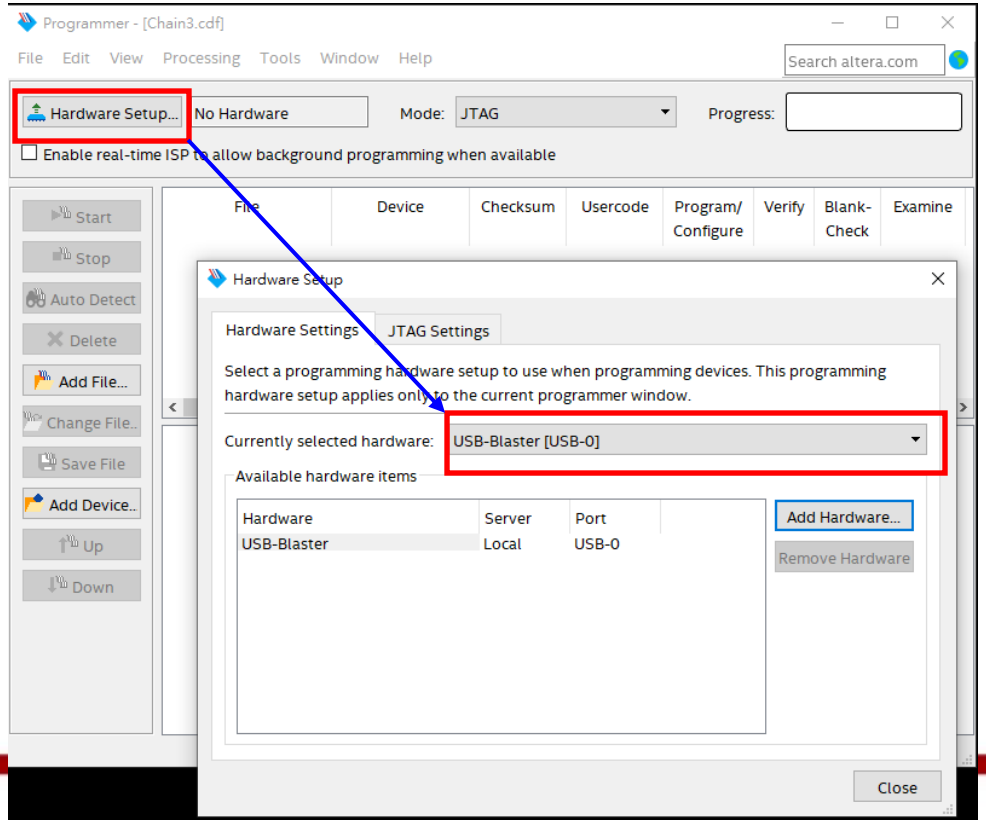
- Installation Complete and 啟動驅動程式安裝

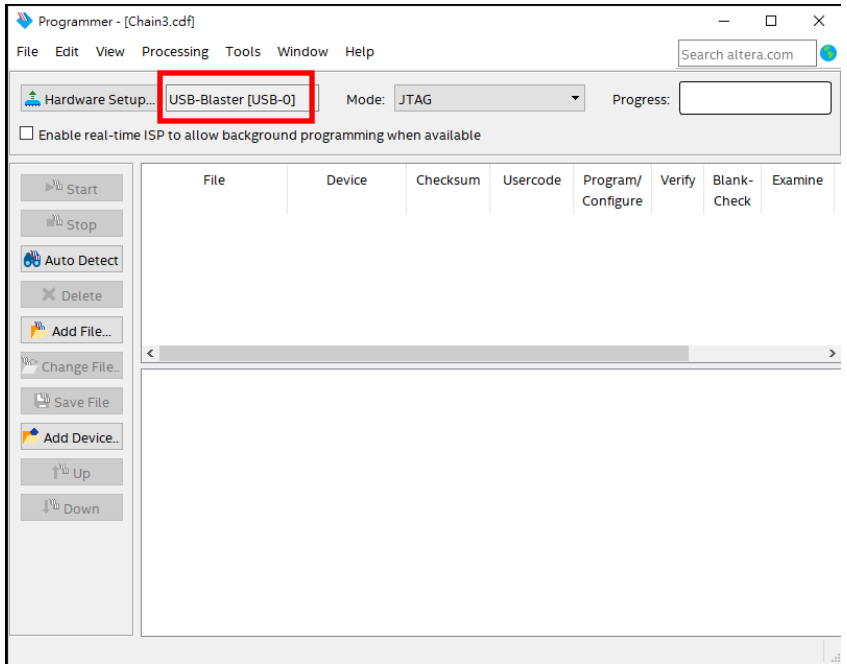




Software Installation

- 啟動驅動程式安裝成功確認(必須插上FPGA板)
  - 安裝成功確認方式可點選Tools->Programmer再指定



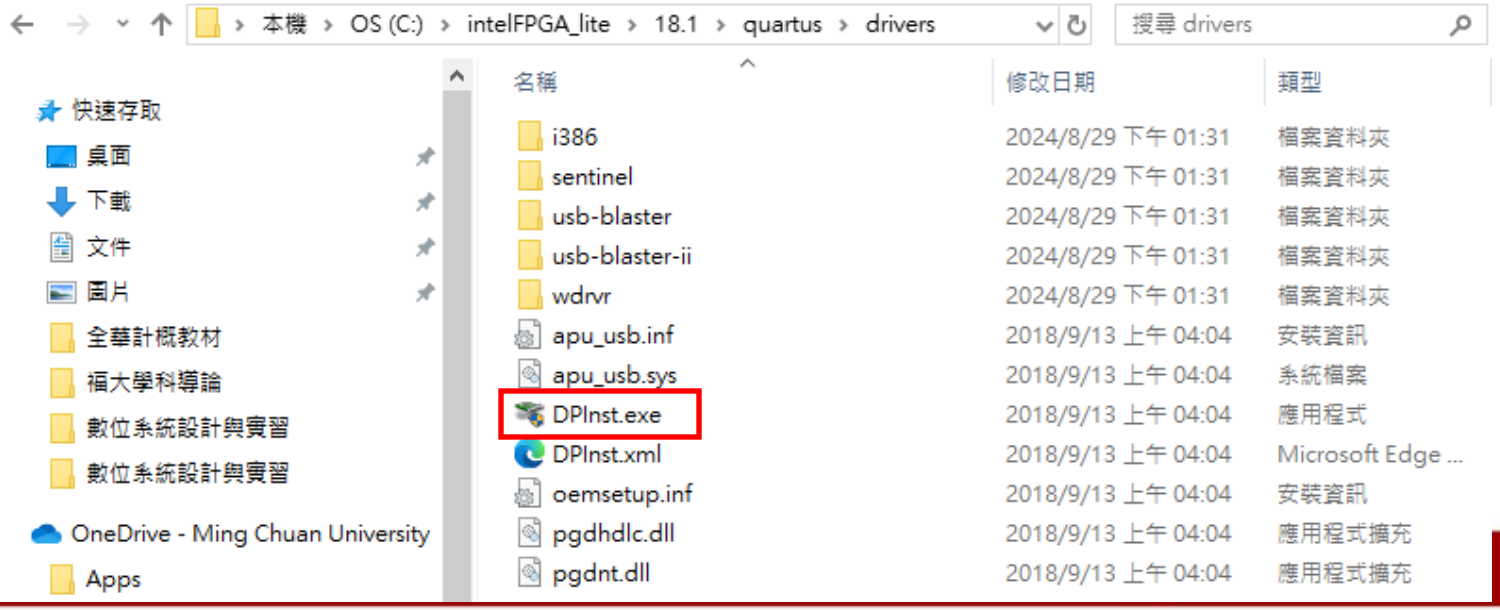


Software Installation

- 啟動驅動程式安裝(必須插上FPGA板)
  - 若當初安裝Quartus時未安裝，可進入以下檔案子目錄

    C:\intelFPGA_lite\18.1\quartus\drivers

    點選執行 DPInst.exe 後即可安裝



牛刀小試

- 使用Quartus® Prime Lite Edition Version 18.1進行軟體模擬
  - 撰寫Verilog HDL電路程式碼
  - 編譯程式及觀看合成電路(RTL Viewer)
  - 撰寫Verilog HDL電路測試程式碼(testbench)
  - 執行電路測試程式碼，觀看模擬波形
- 使用Quartus® Prime Lite Edition Version 18.1進行硬體模擬