ModelSim

Ren-Der Chen (陳仁德)
Department of Computer Science and Information Engineering
National Changhua University of Education
E-mail: rdchen@cc.ncue.edu.tw
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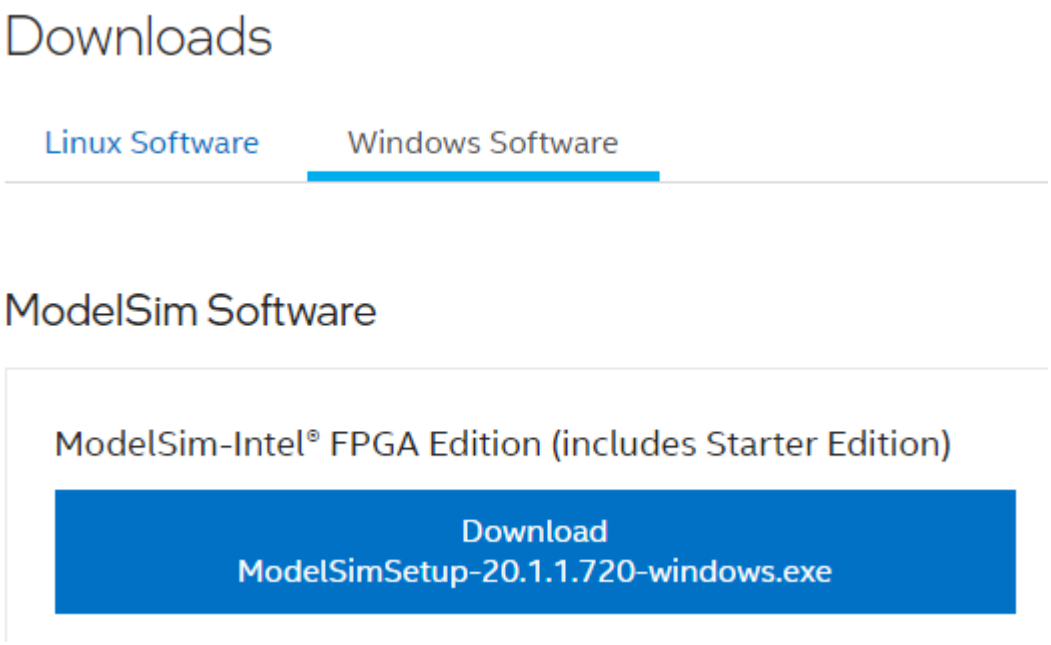
ModelSim Download

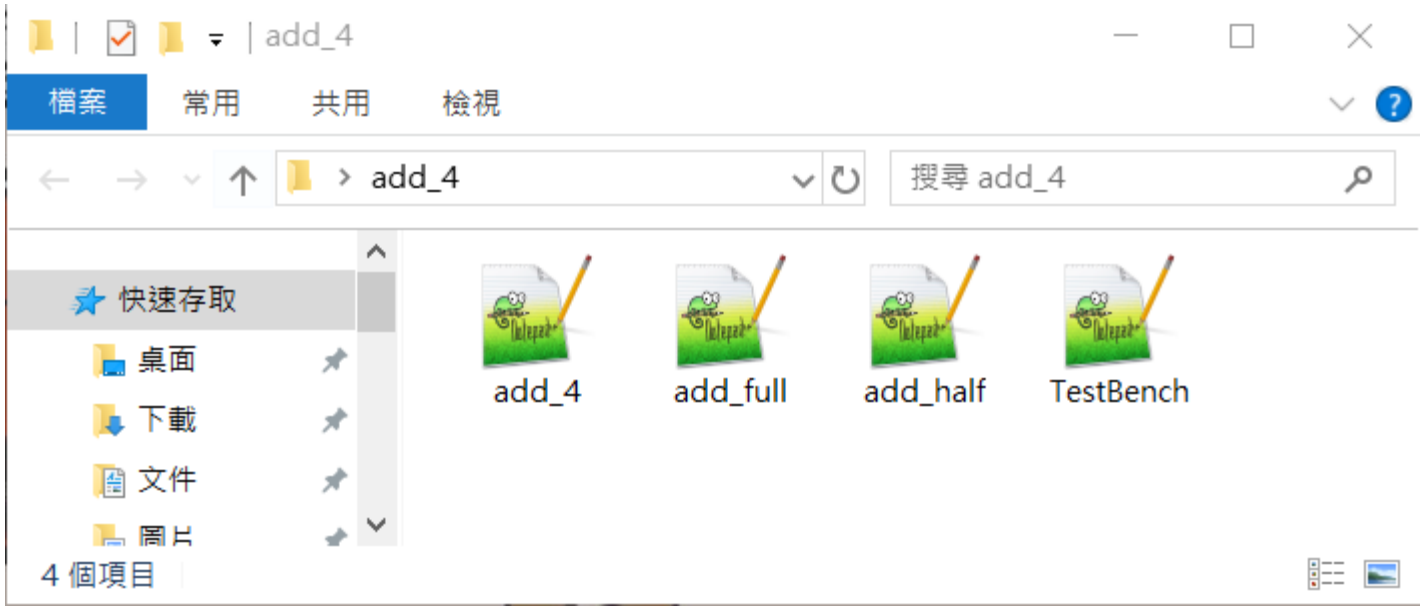
- https://www.intel.com/content/www/us/en/software-kit/750666/modelsim-intel-fpgas-standard-edition-software-version-20-1-1.html



Design Example: 4-Bit Adder

- Half Adder (add_half.v)
- Full Adder (add_full.v)
- 4-Bit Adder (add_4.v)
- Testbench File (add_4_tb.v)

測試



Half Adder (add_half.v)

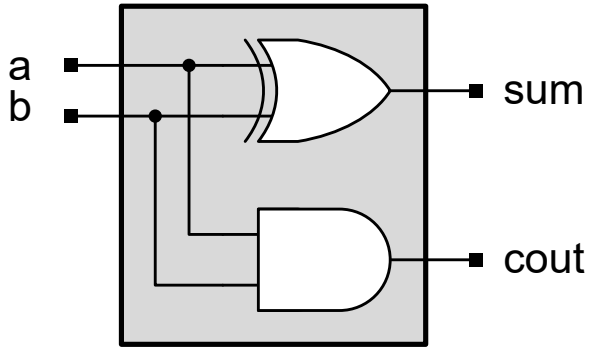
```
module add_half (a, b, cout, sum);

input   a, b;
output  cout, sum;

assign  cout = a & b;
assign  sum = a ^ b;
endmodule
```

a\b	0	1
0	0	1
1	1	0

sum=a⊕b

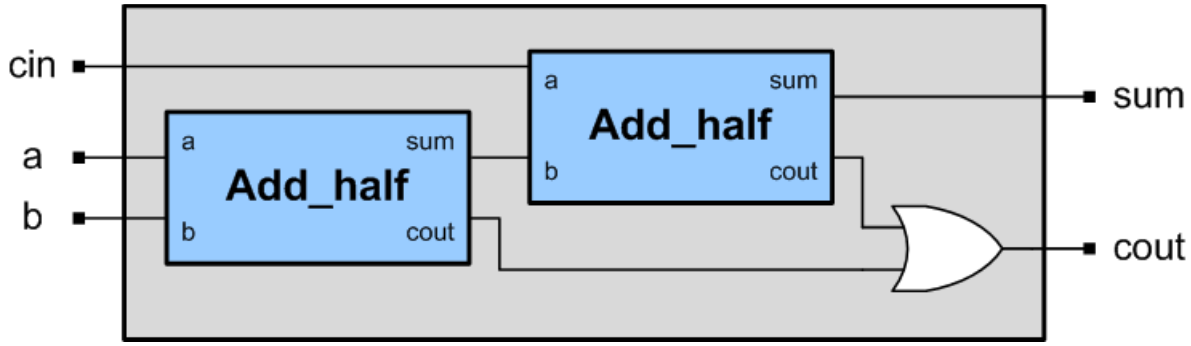
a\b	0	1
0	0	0
1	0	1

cout=a·b



Full Adder (add_full.v)

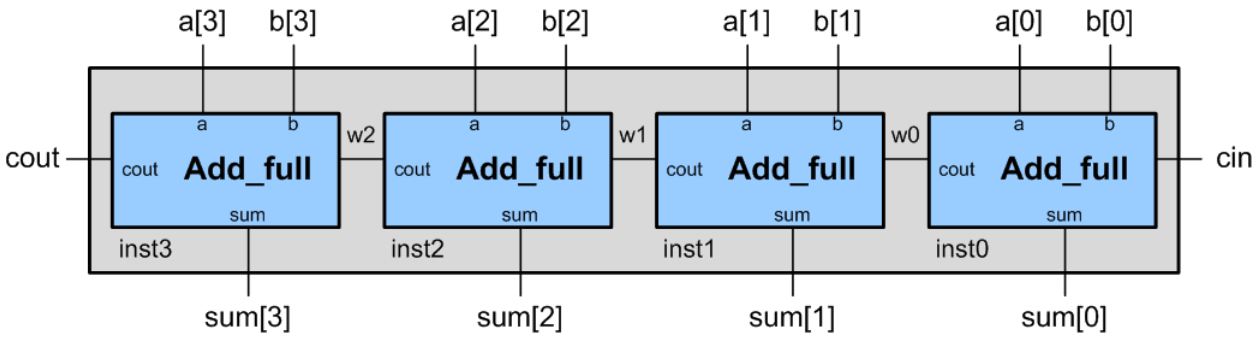
```
module add_full (a, b, cin, cout, sum);

input    a, b, cin;
output   cout, sum;
wire     w0, w1, w2;
```




```
add_half    inst0 (a, b, w2, w0);
add_half    inst1 (cin, w0, w1, sum);
assign      cout = w1 | w2;

endmodule
```

4-Bit Adder (add_4.v)

```
module add_4 (a, b, cin, cout, sum);
input   [3:0]   a, b;
input           cin;
output          cout;
output  [3:0]   sum;
wire            w0, w1, w2;
```




```
add_full inst0 (a[0], b[0], cin, w0,   sum[0]);
add_full inst1 (a[1], b[1], w0,  w1,   sum[1]);
add_full inst2 (a[2], b[2], w1,  w2,   sum[2]);
add_full inst3 (a[3], b[3], w2,  cout, sum[3]);
endmodule
```

Testbench File (add_4_tb.v) (1/2)

```
module add_4_tb;
  reg   [3:0] a, b;
  reg         cin;
  wire        cout;
  wire  [3:0] sum;

  add_4 m0 (a, b, cin, cout, sum);

  initial
    $monitor("Time: %3t ns,  Inputs: a = %2d  b = %2d  cin = %b, \
      Outputs: cout = %b  sum = %2d", $time, a, b, cin, cout, sum);
```

Inputs

Outputs

Top module

print 銀幕

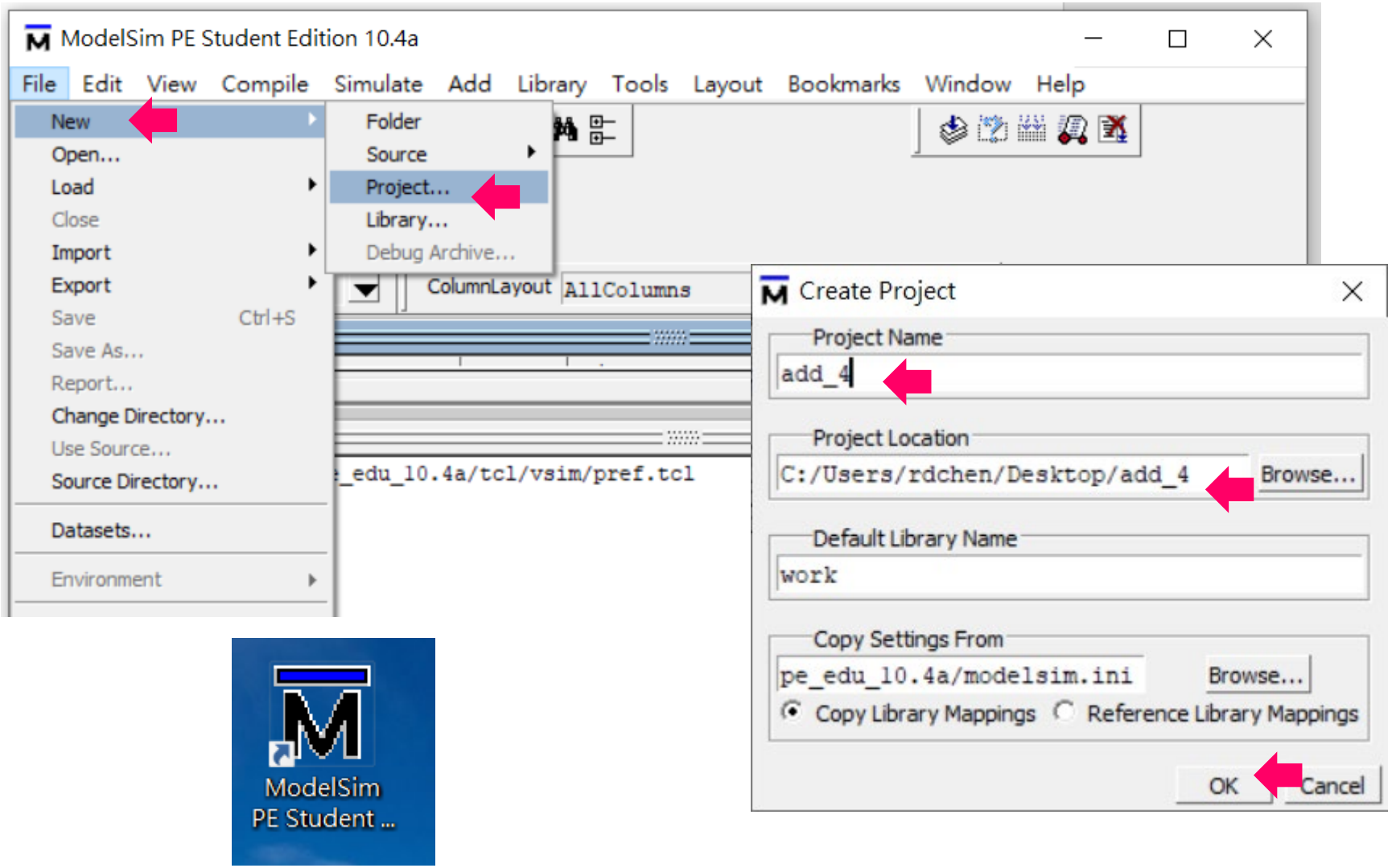
Text message

Testbench File (add_4_tb.v) (2/2)

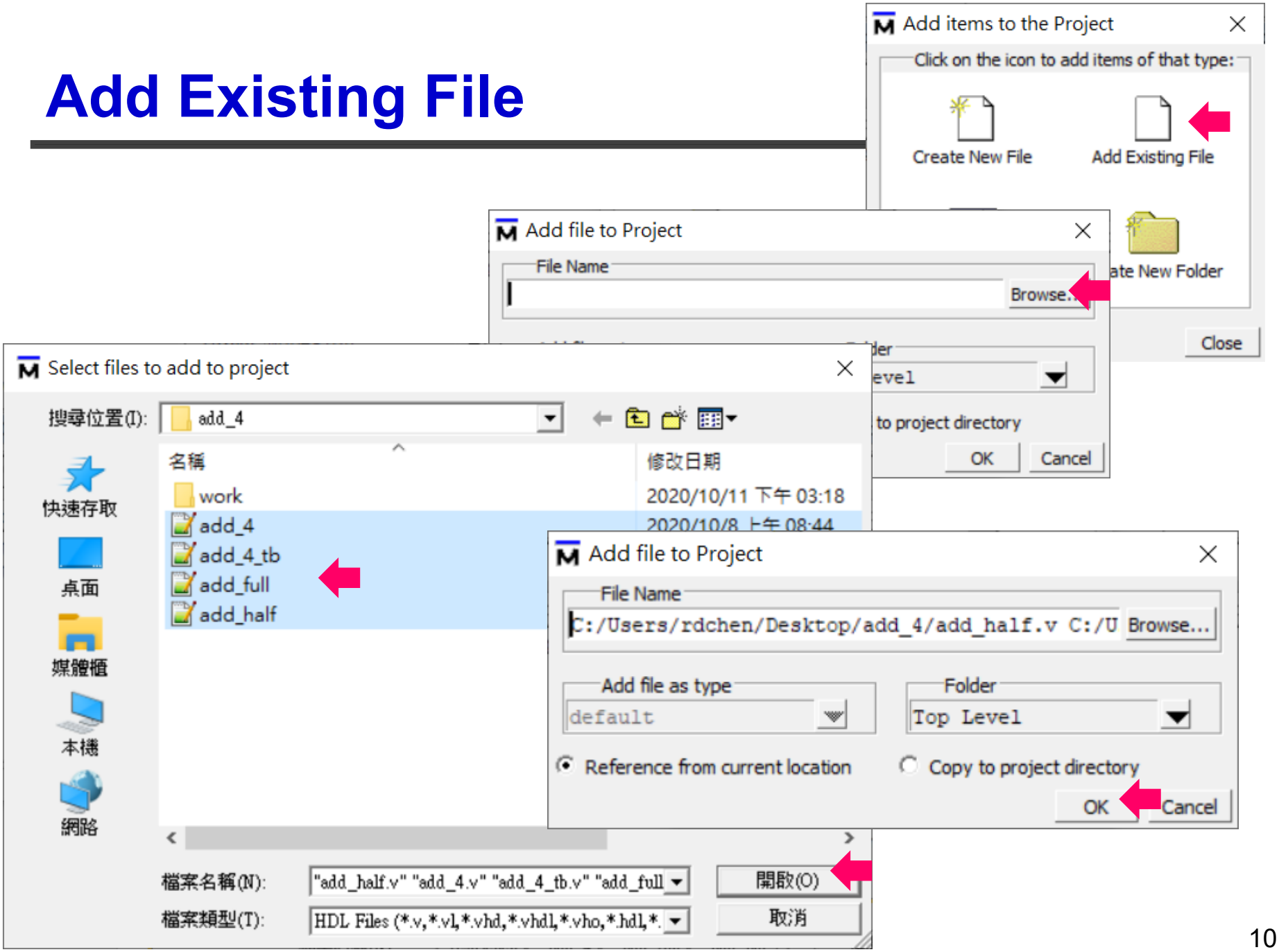
Input values

```
initial begin
    #10 a = 4'd0;  b = 4'd0;   cin = 1'b0;
    #20 a = 4'd0;  b = 4'd1;   cin = 1'b0;
    #20 a = 4'd2;  b = 4'd1;   cin = 1'b1;
    #20 a = 4'd4;  b = 4'd5;   cin = 1'b0;
    #20 a = 4'd6;  b = 4'd5;   cin = 1'b1;
    #20 a = 4'd8;  b = 4'd9;   cin = 1'b0;
    #20 a = 4'd10; b = 4'd9;   cin = 1'b1;
    #20 a = 4'd12; b = 4'd13;  cin = 1'b0;
    #20 a = 4'd14; b = 4'd13;  cin = 1'b1;
    #20 $finish;
  end
endmodule
```

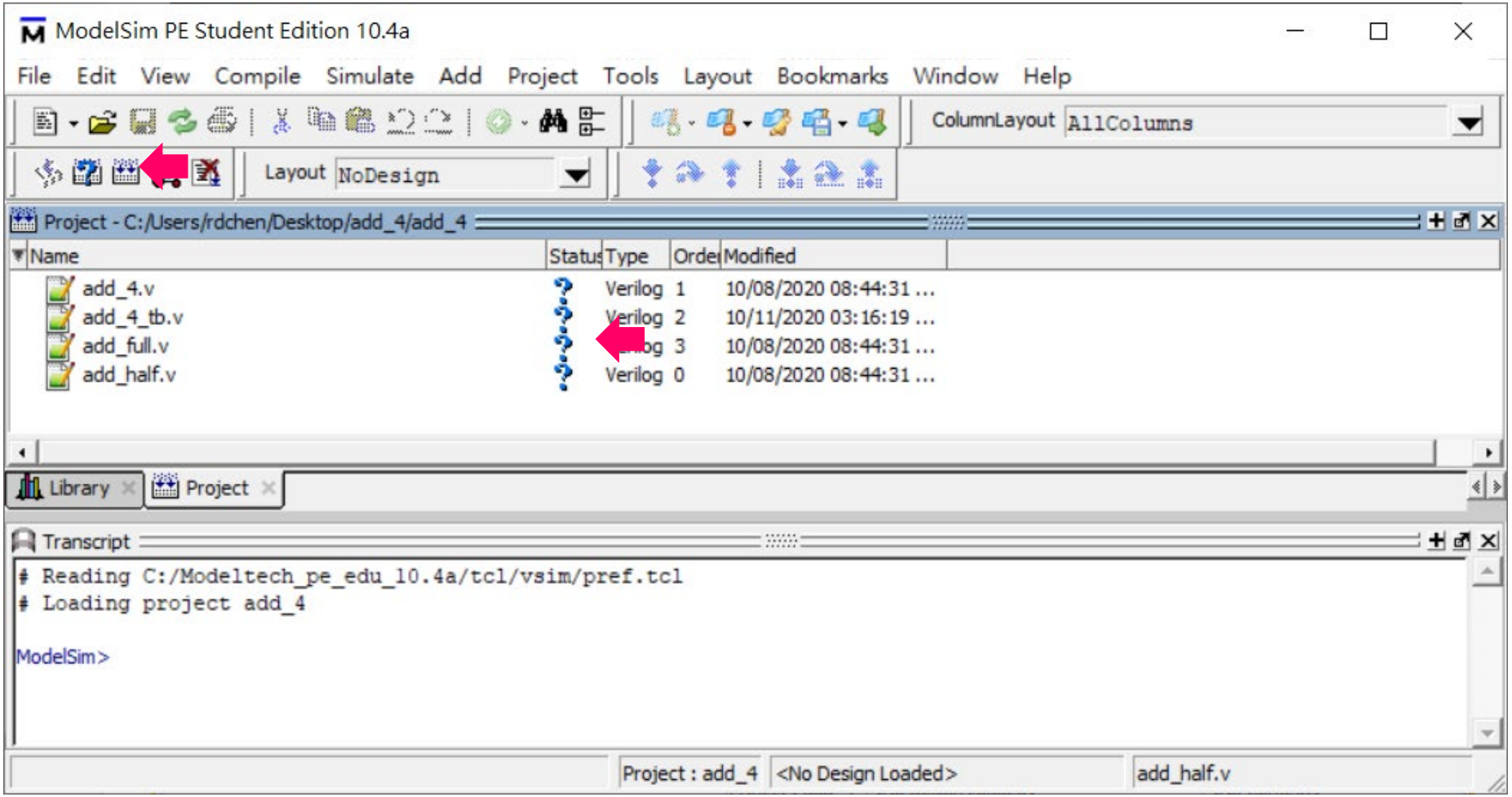
Create New Project



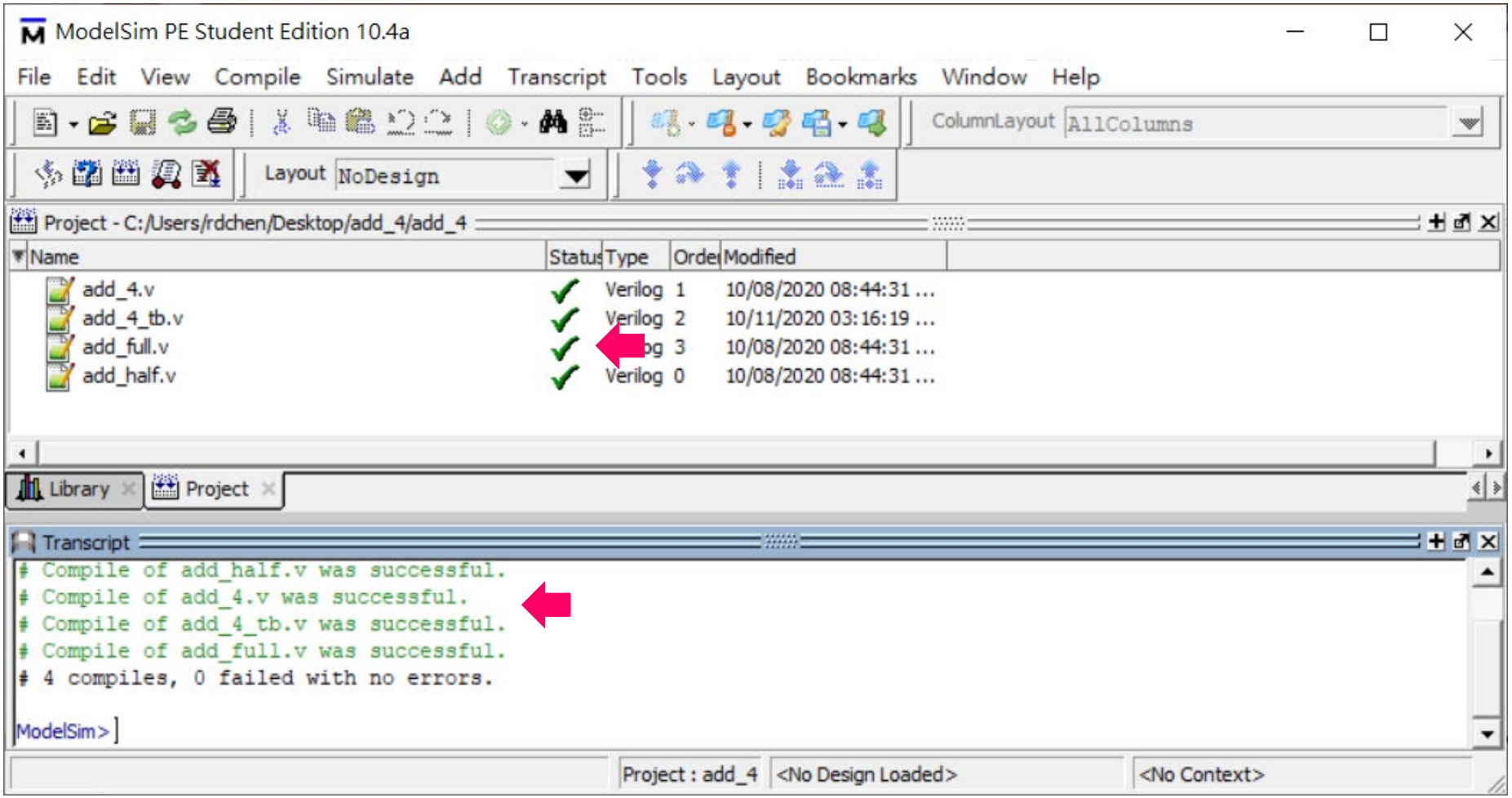
Add Existing File



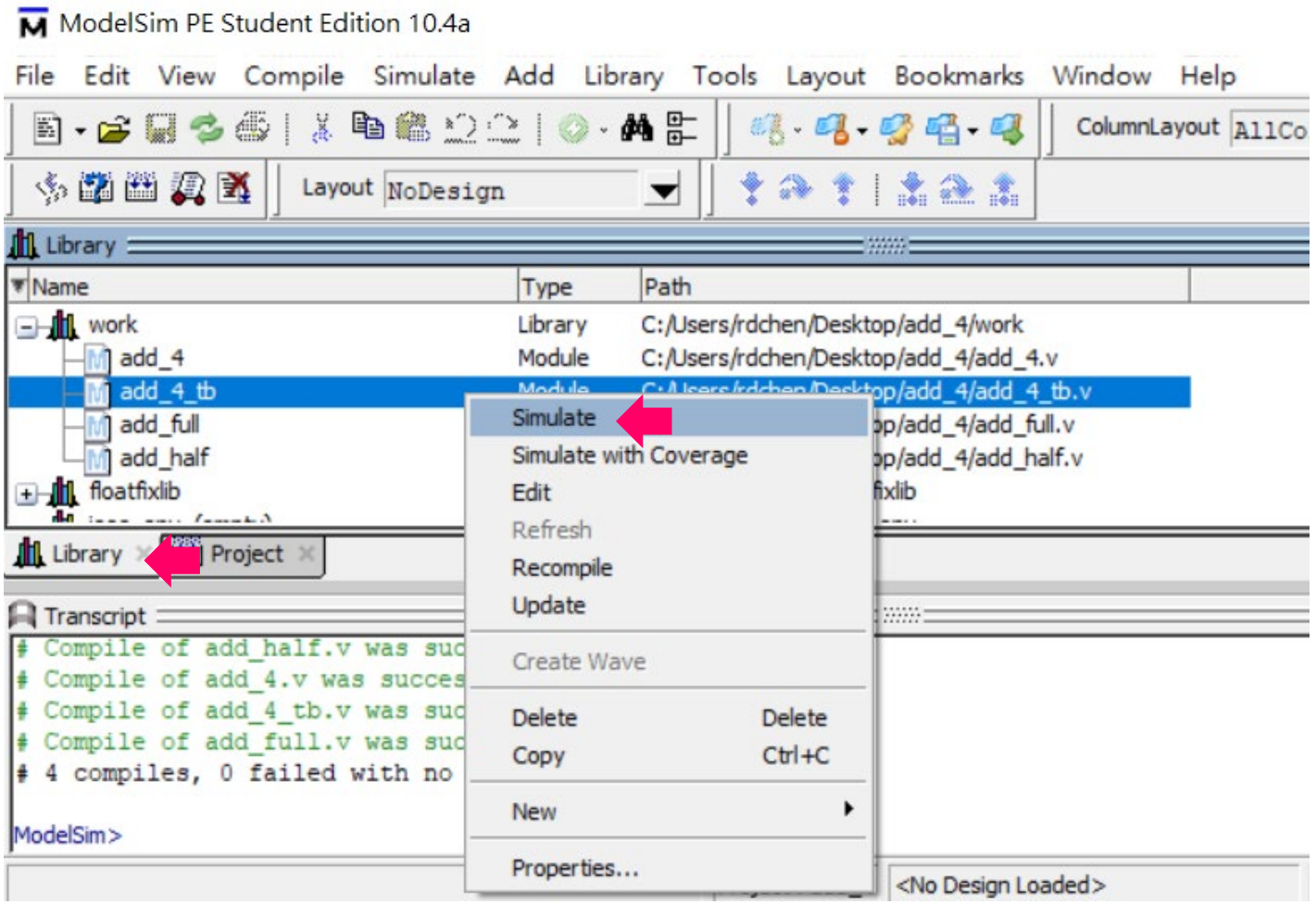
Compile All Files (1/2)



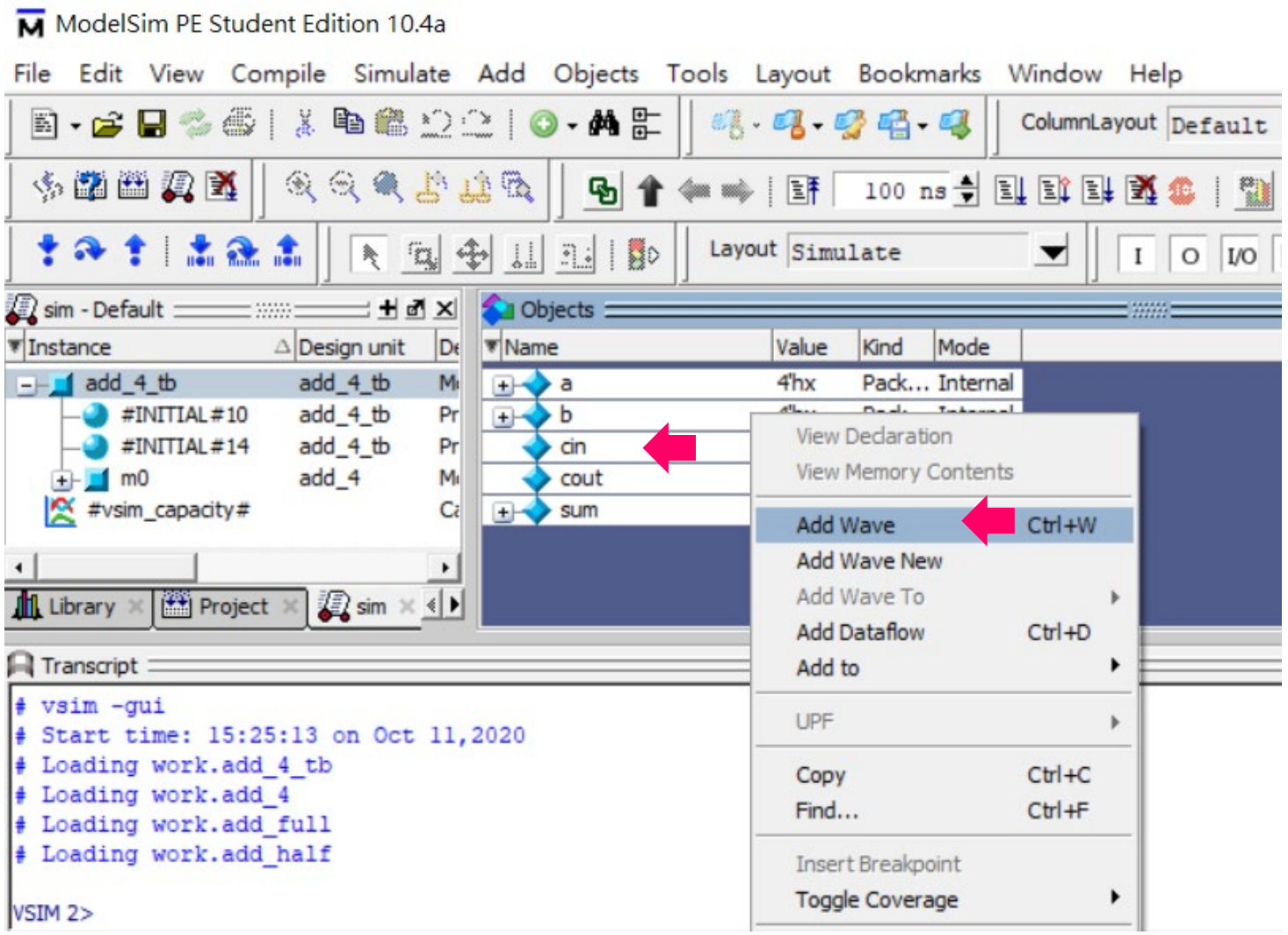
Compile All Files (2/2)



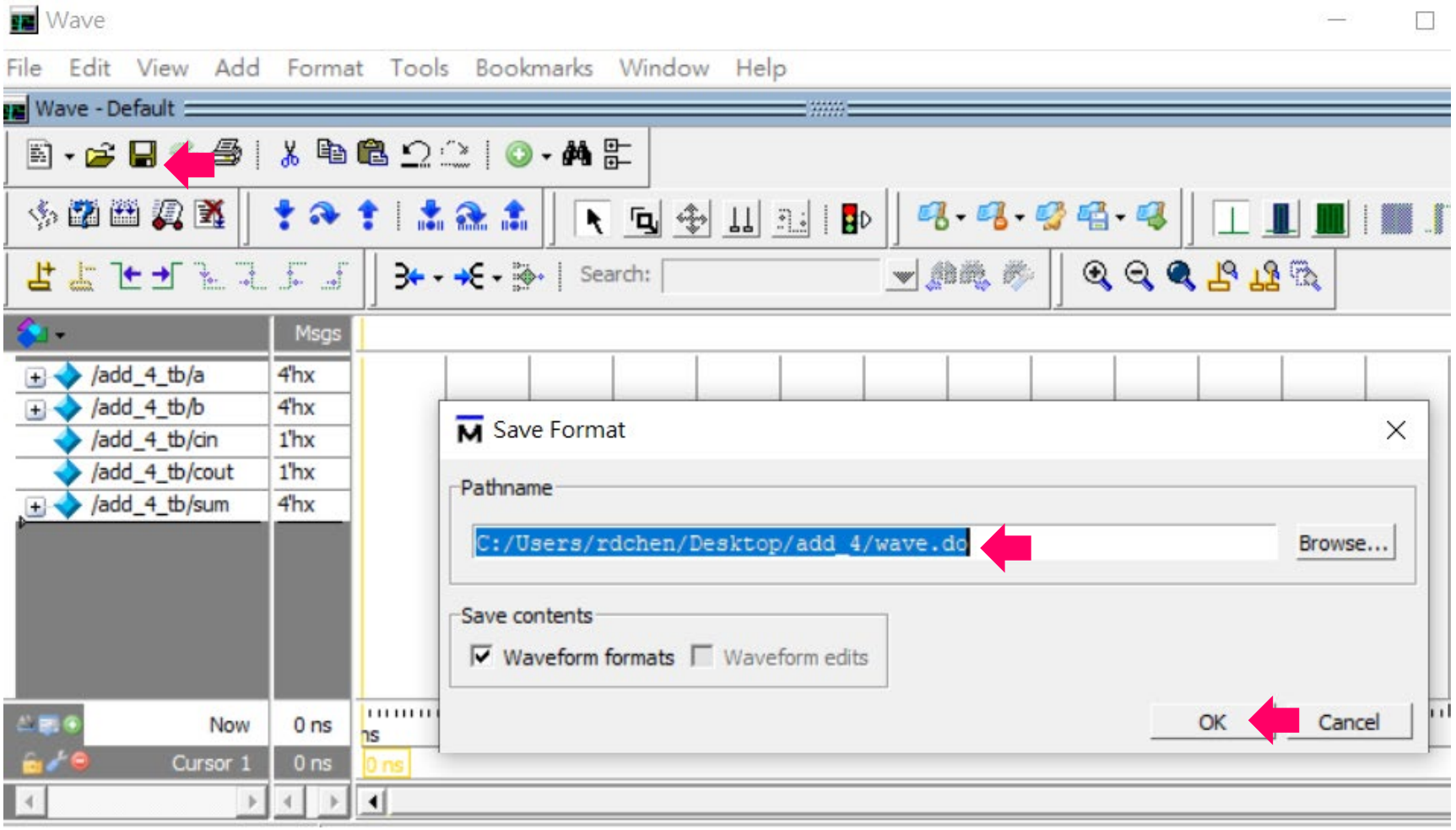
Start Simulation



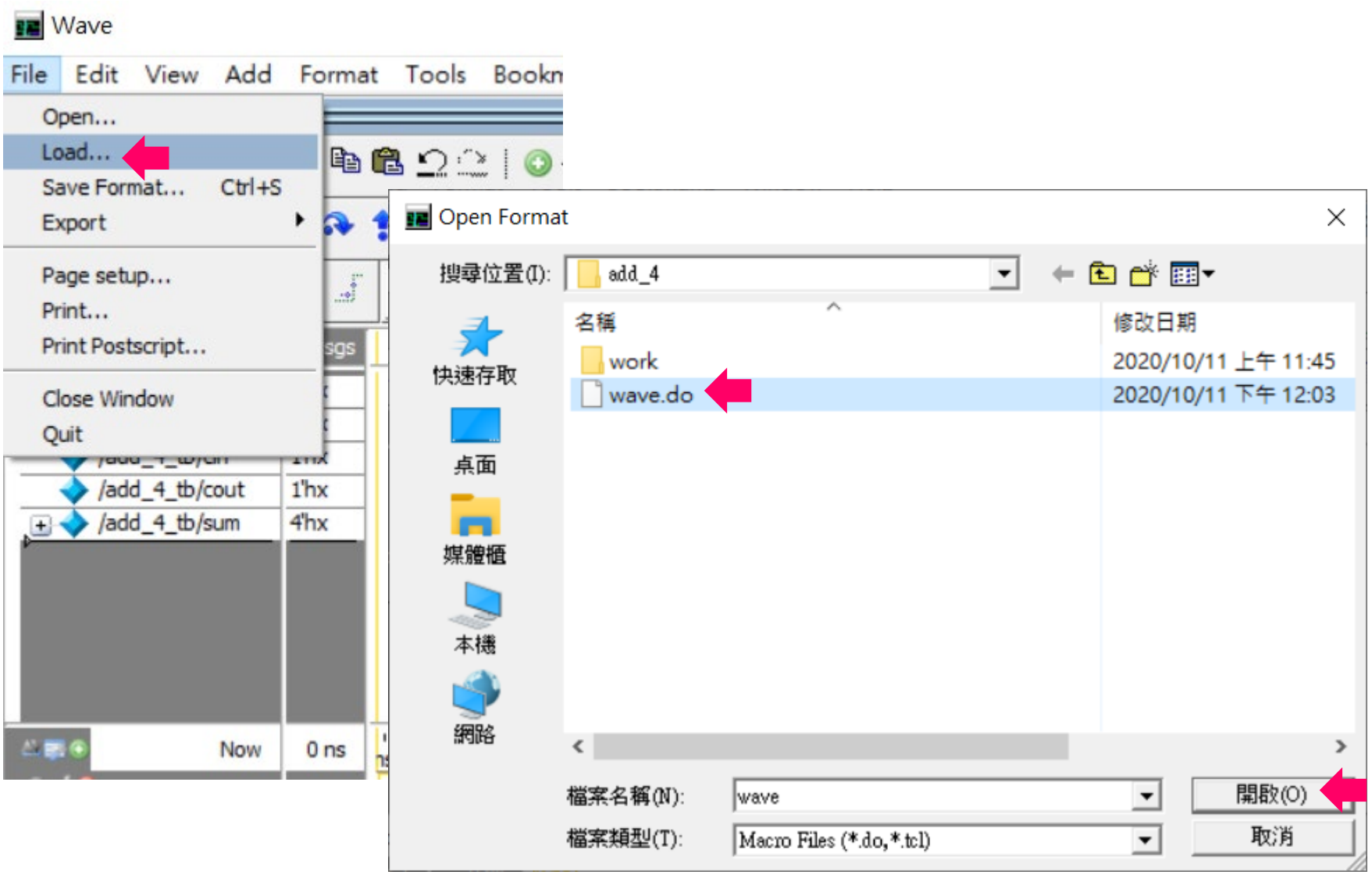
Add Wave


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help
ColumnLayout Default
100 ns
Layout Simulate
I O I/O
sim - Default
Instance Design unit
add_4_tb add_4_tb
#INITIAL#10 add_4_tb
#INITIAL#14 add_4_tb
m0 add_4
#vsim_capacity#
Objects
Name Value Kind Mode
a 4'hx Pack... Internal
b
cin
cout
sum
View Declaration
View Memory Contents
Add Wave Ctrl+W
Add Wave New
Add Wave To
Add Dataflow Ctrl+D
Add to
UPF
Copy Ctrl+C
Find... Ctrl+F
Insert Breakpoint
Toggle Coverage
Library
Project
sim
Transcript
vsim -gui
Start time: 15:25:13 on Oct 11,2020
Loading work.add_4_tb
Loading work.add_4
Loading work.add_full
Loading work.add_half
VSIM 2>

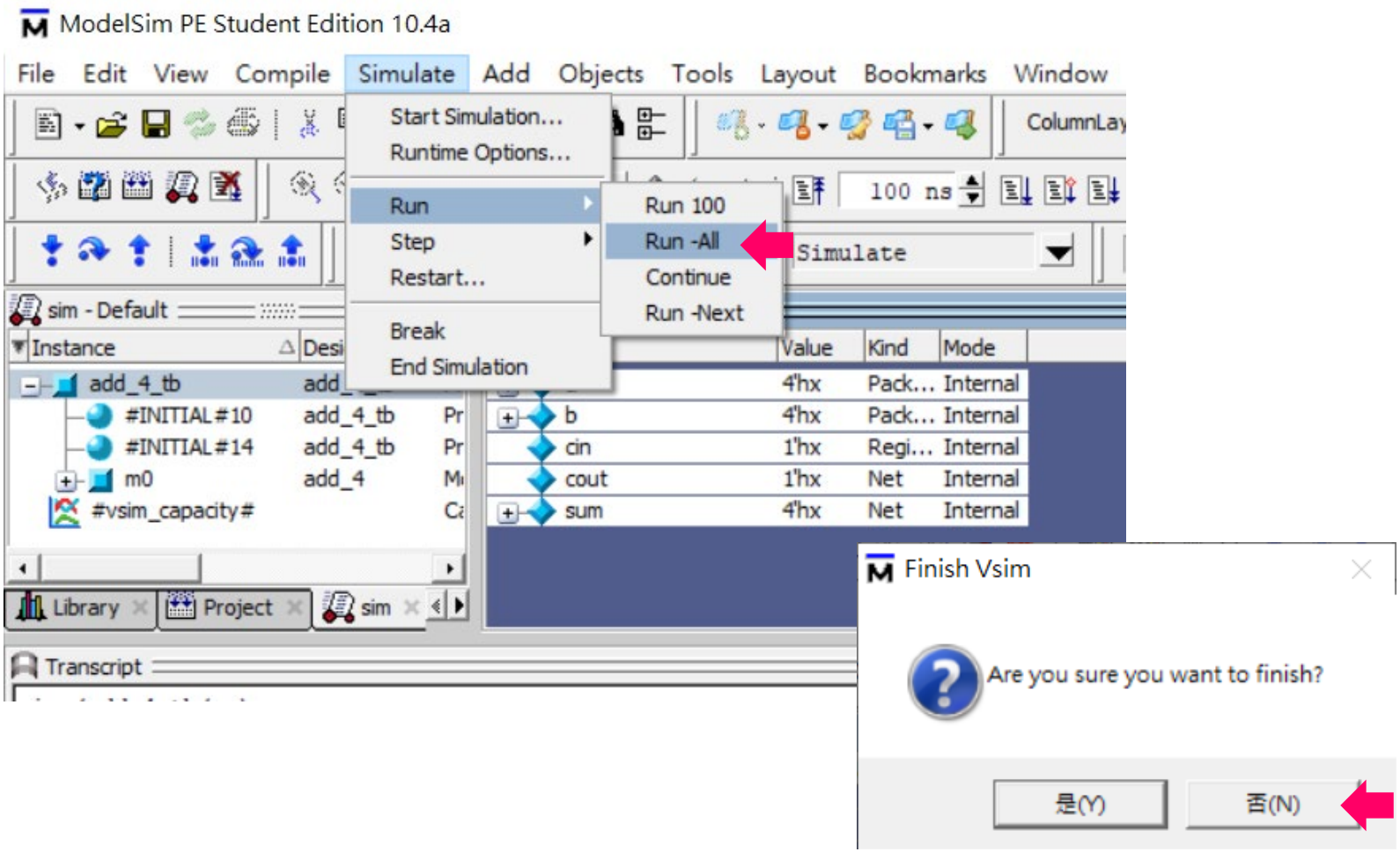
Save Waveform Format



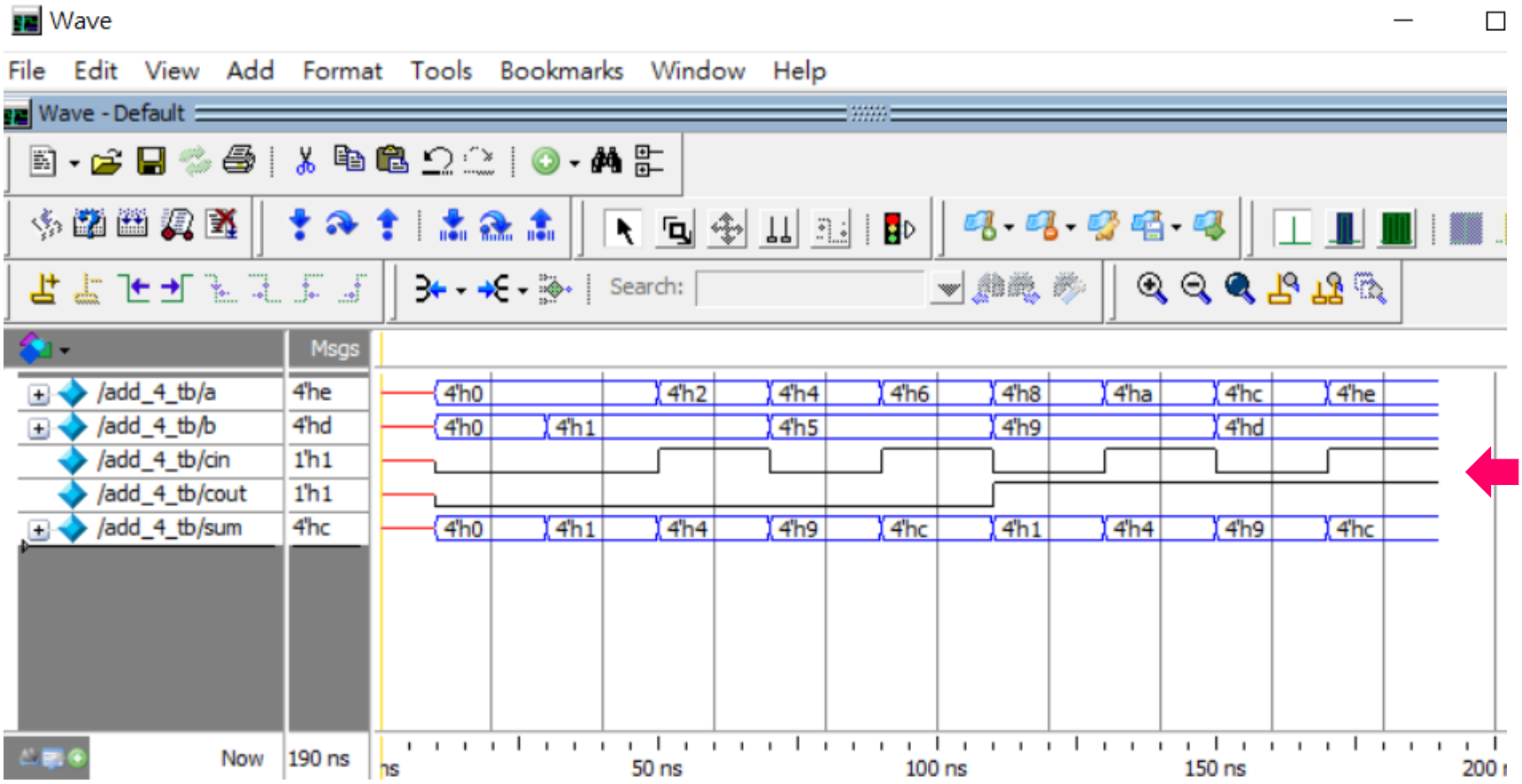
Load Waveform Format (Optional)



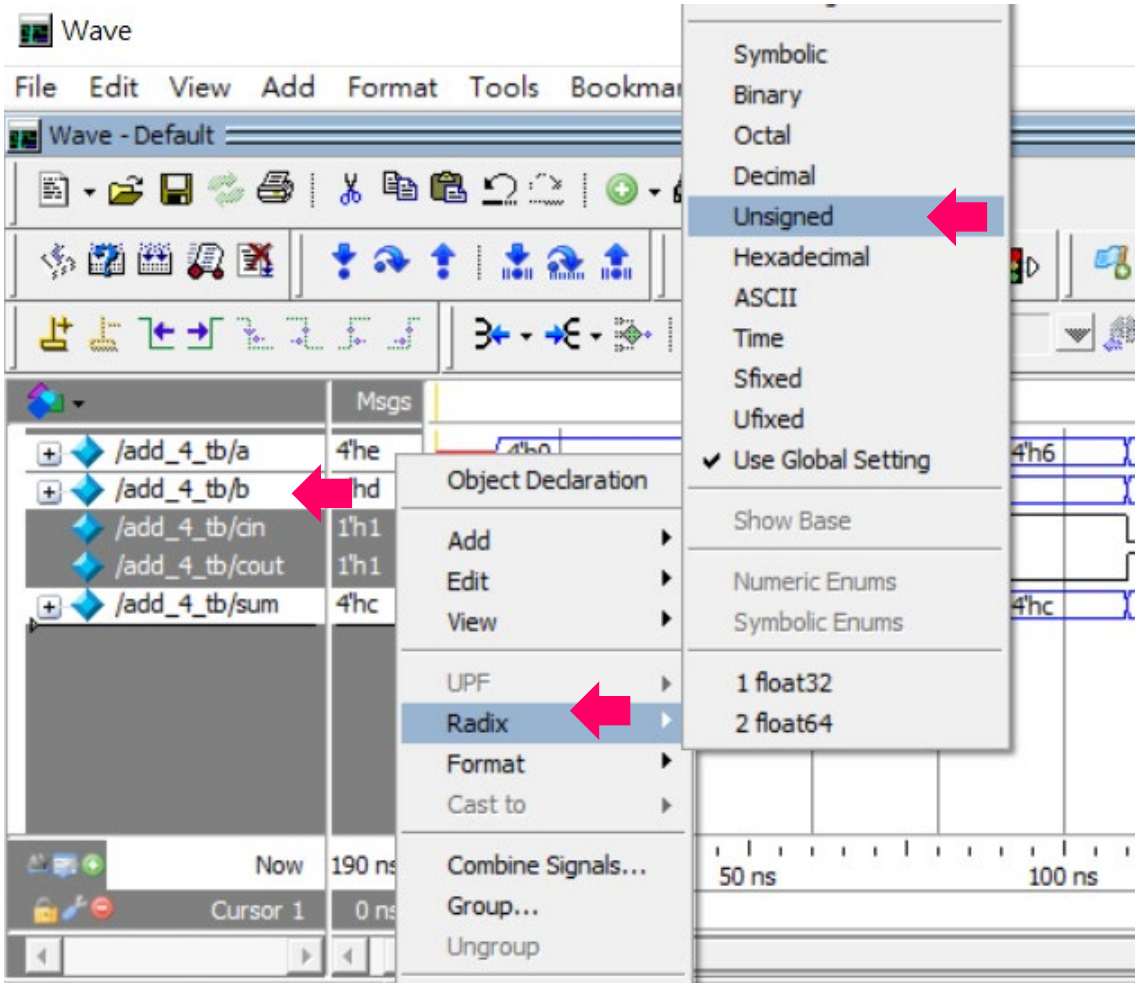
Run Simulation



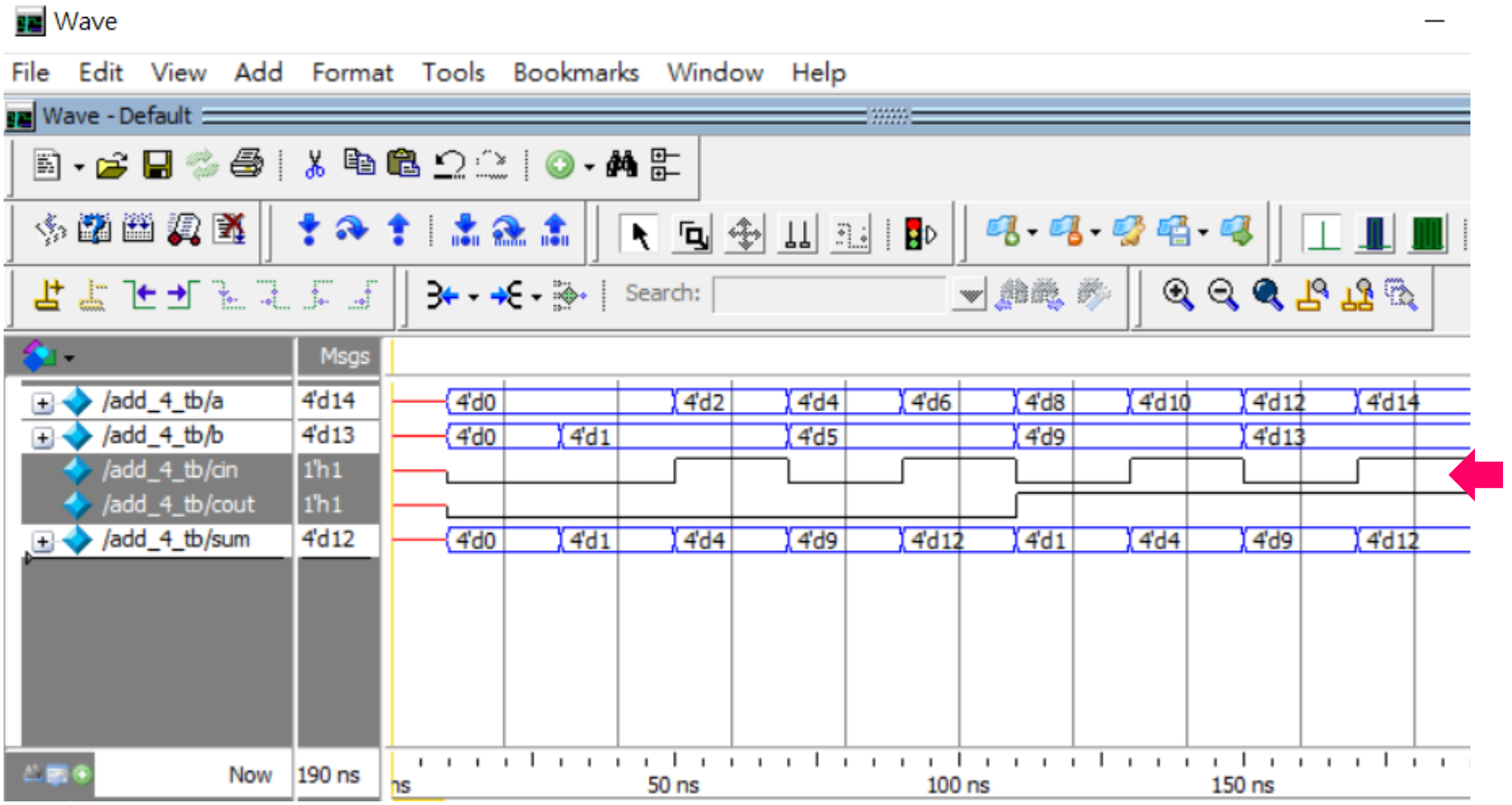
Simulation Result – Waveform 1



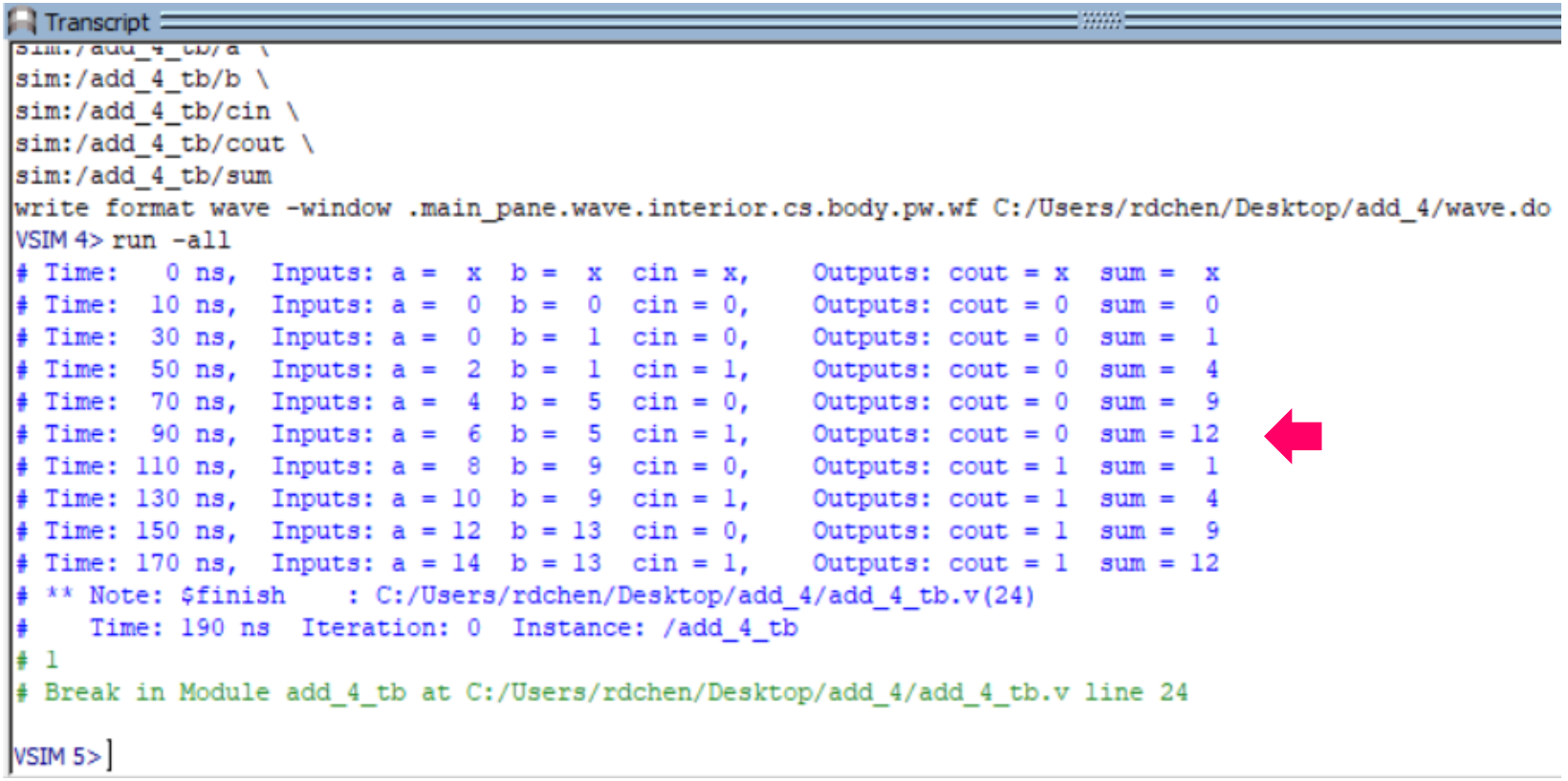
Change Radix



Simulation Result – Waveform 2



Simulation Result – Text Message



End Simulation