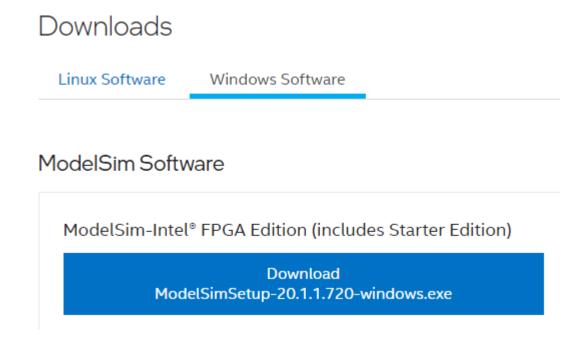


ModelSim

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ModelSim Download

https://www.intel.com/content/www/us/en/software-kit/750666/modelsim-intel-fpgas-standard-edition-software-version-20-1-1.html

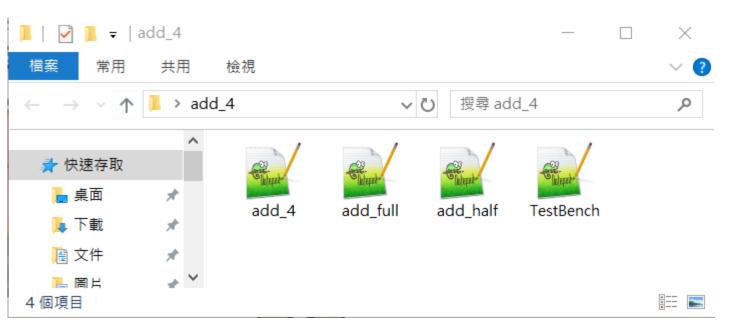


Design Example: 4-Bit Adder

- Half Adder (add_half.v)
- Full Adder (add_full.v)
- 4-Bit Adder (add_4.v)
- Testbench File (add_4_tb.v)

测量式





Half Adder (add_half.v)

module add_half (a, b, cout, sum);

input a, b;

output cout, sum;

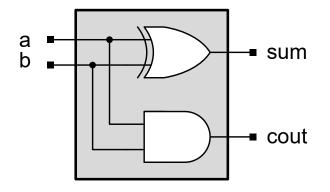
assign cout = a & b;

assign sum = $a \wedge b$;

endmodule



a∖b	0	1	a\b	0	1
0	0	1	0	0	0
1	1	0	1	0	1



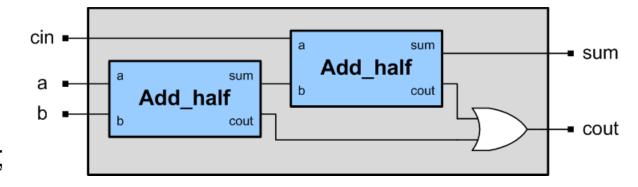
Full Adder (add_full.v)

module add_full (a, b, cin, cout, sum);

input a, b, cin;

output cout, sum;

wire w0, w1, w2;



```
add_half inst0 (a, b, w2, w0);
```

add_half inst1 (cin, w0, w1, sum);

assign cout = w1 | w2;

endmodule

4-Bit Adder (add_4.v)

module add_4 (a, b, cin, cout, sum);

```
input [3:0]
                      a, b;
                                             a[3]
                                                   b[3]
                                                              a[2]
                                                                    b[2]
                                                                               a[1]
                                                                                     b[1]
                                                                                                a[0]
                                                                                                      b[0]
input
                       cin;
                                                        w2
                                                                                          w0
                                  cout -
                                          cout Add full
                                                                                                              cin
                                                                                             cout Add full
                                                           cout Add full
                                                                            cout Add full
output
                      cout;
                                          inst3
                                                           inst2
                                                                            inst1
                                                                                             inst0
output [3:0]
                       sum;
                                               sum[3]
                                                                sum[2]
                                                                                 sum[1]
                                                                                                  sum[0]
                      w0. w1. w2:
wire
```

```
add_full inst0 (a[0], b[0], cin, w0, sum[0]);
add_full inst1 (a[1], b[1], w0, w1, sum[1]);
add_full inst2 (a[2], b[2], w1, w2, sum[2]);
add_full inst3 (a[3], b[3], w2, cout, sum[3]);
```

endmodule

Testbench File (add_4_tb.v) (1/2)

```
module add 4_tb;
reg [3:0] a, b;
reg cin; Inputs
wire cout;
wire [3:0] sum; Outputs

add 4 m0 (a, b, cin, cout, sum); Top module

initial

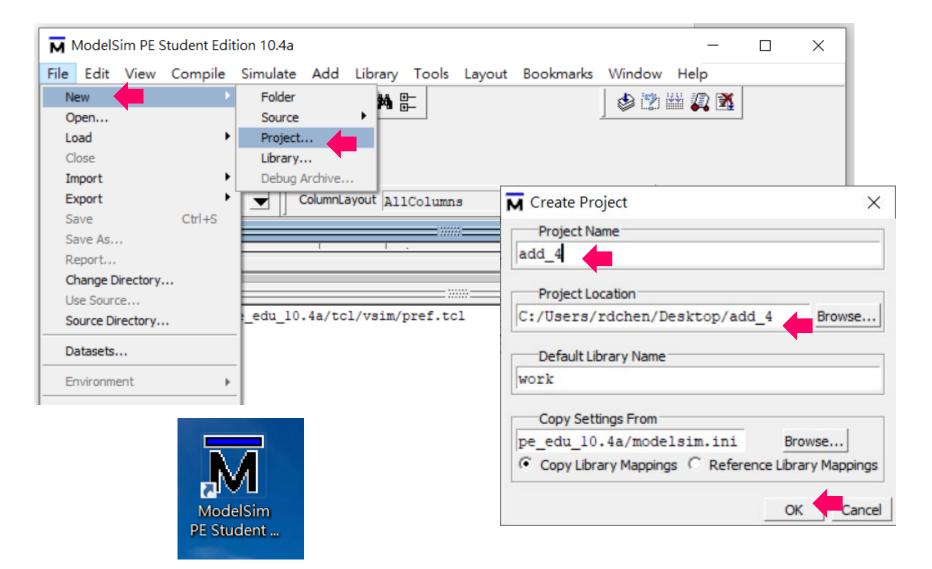
Print > $monitor("Time: %3t ns, Inputs: a = %2d b = %2d cin = %b, \
Outputs: cout = %b sum = %2d", $time, a, b, cin, cout, sum);
Text message
```

Testbench File (add_4_tb.v) (2/2)

```
initial begin

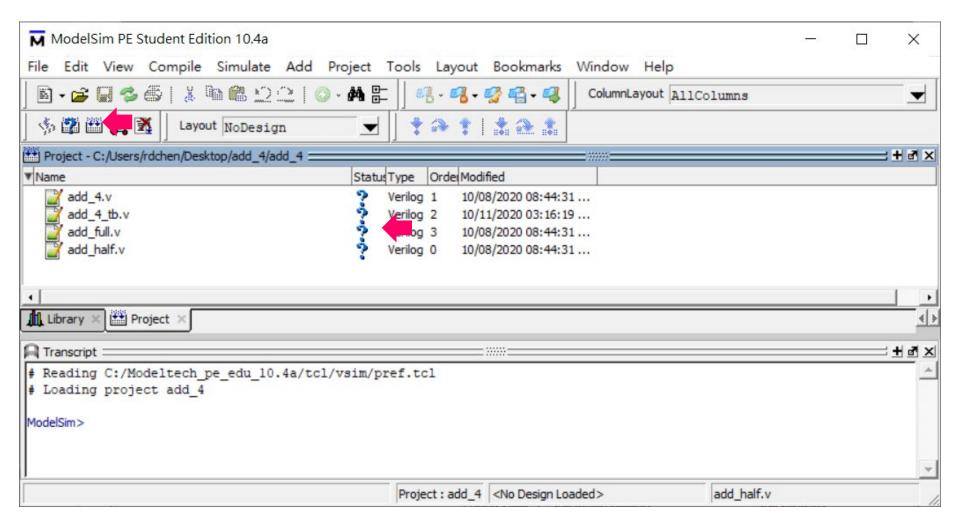
#10 a = 4'd0; b = 4'd0; cin = 1'b0;
#20 a = 4'd0; b = 4'd1; cin = 1'b0;
#20 a = 4'd2; b = 4'd1; cin = 1'b1;
#20 a = 4'd4; b = 4'd5; cin = 1'b0;
#20 a = 4'd6; b = 4'd5; cin = 1'b1;
#20 a = 4'd8; b = 4'd9; cin = 1'b0;
#20 a = 4'd10; b = 4'd9; cin = 1'b1;
#20 a = 4'd12; b = 4'd13; cin = 1'b1;
#20 a = 4'd14; b = 4'd13; cin = 1'b1;
#20 $finish;
end
endmodule
```

Create New Project

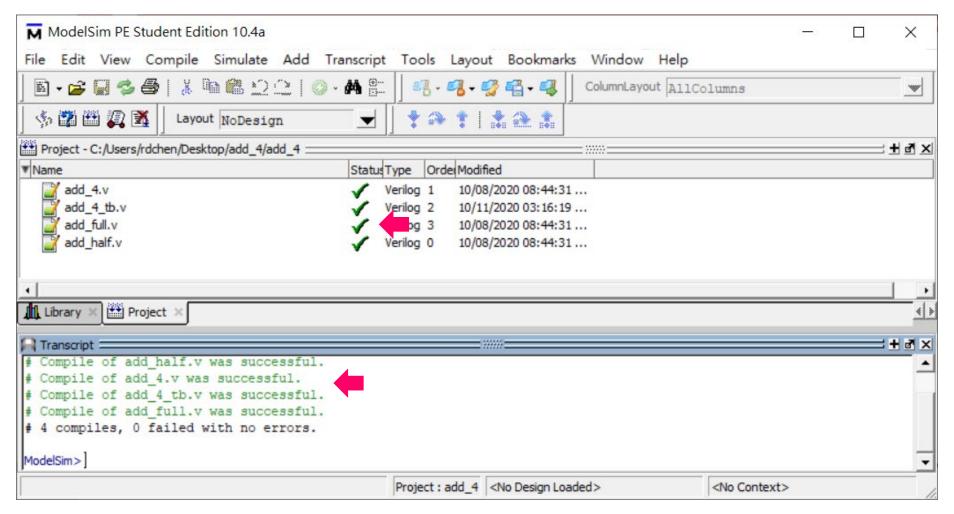


M Add items to the Project × Click on the icon to add items of that type: Add Existing File Add Existing File Create New File Add file to Project Х File Name ate New Folder Browse. Close M Select files to add to project 搜尋位置(I): add_4 to project directory 名稱 修改日期 Cancel 2020/10/11 下午 03:18 work 快速存取 add 4 2020/10/8 上午 08:44 Add file to Project add_4_tb add_full 点面 File Name add_half C:/Users/rdchen/Desktop/add 4/add half.v C:/U Browse... Add file as type Folder Top Level default Reference from current location Copy to project directory "add_half.∨" "add_4.∨" "add_4_tb.∨" "add_full ▼ 開啟(O) 檔案名稱(N): 檔案類型(T): 取消 HDL Files (*.v, *.vl, *.vhd, *.vhdl, *.vho, *.hdl, *.

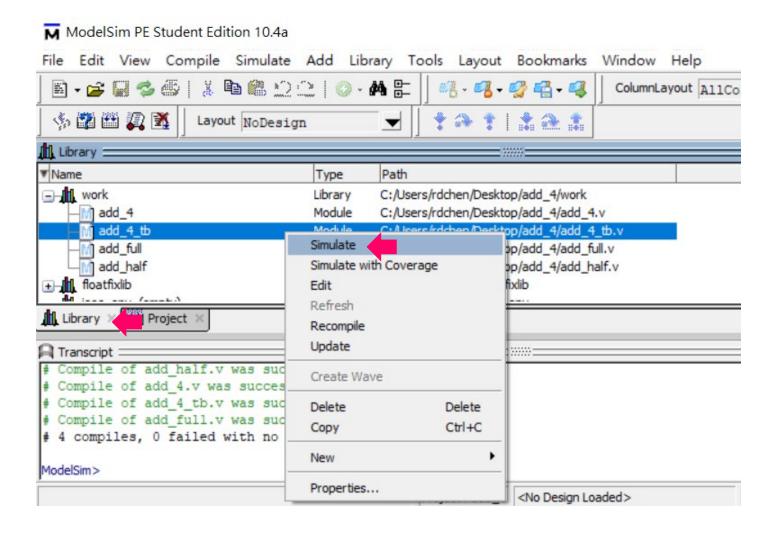
Compile All Files (1/2)



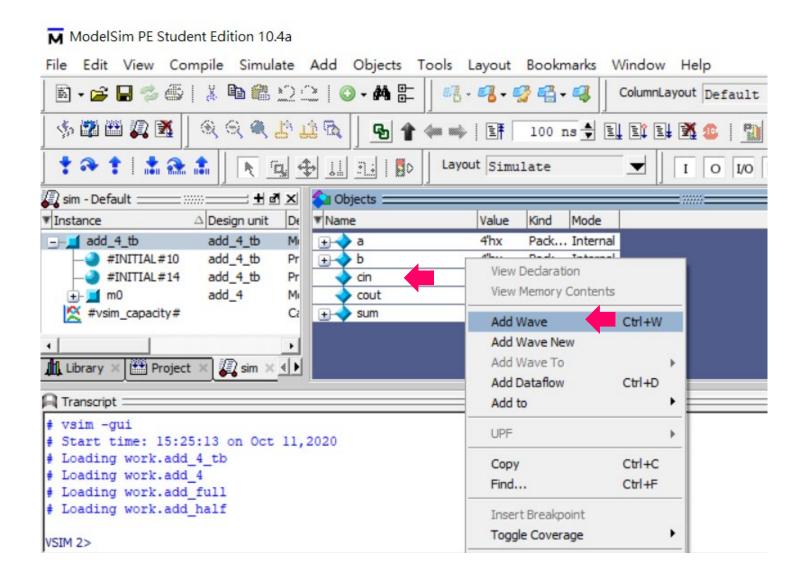
Compile All Files (2/2)



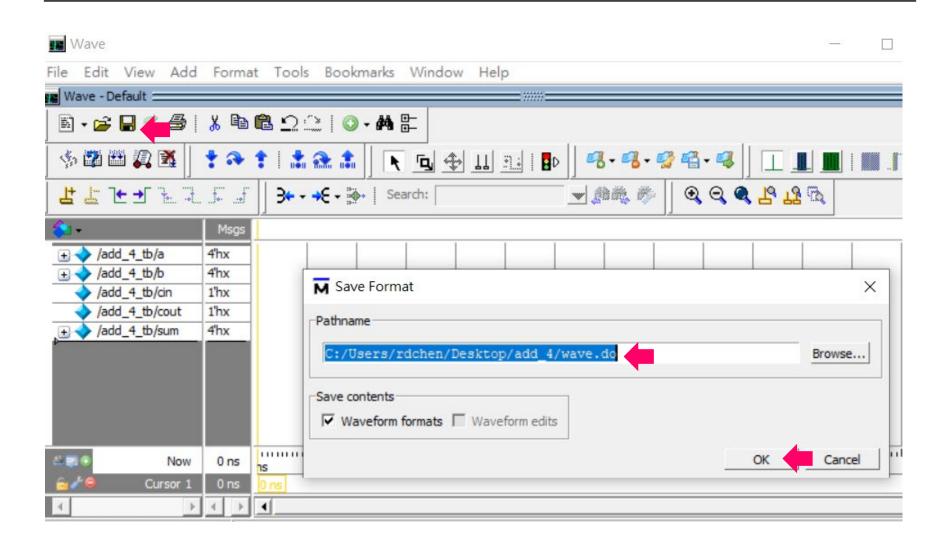
Start Simulation



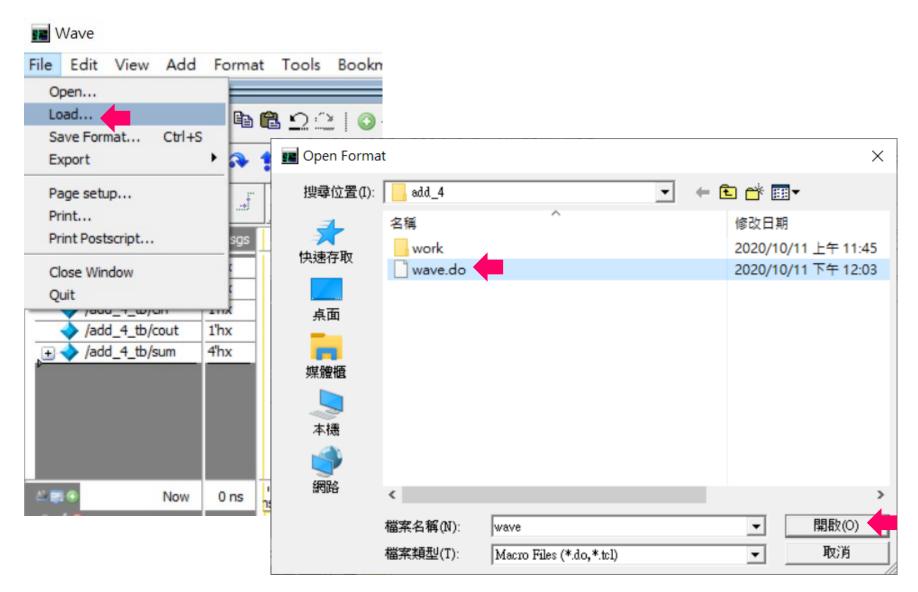
Add Wave



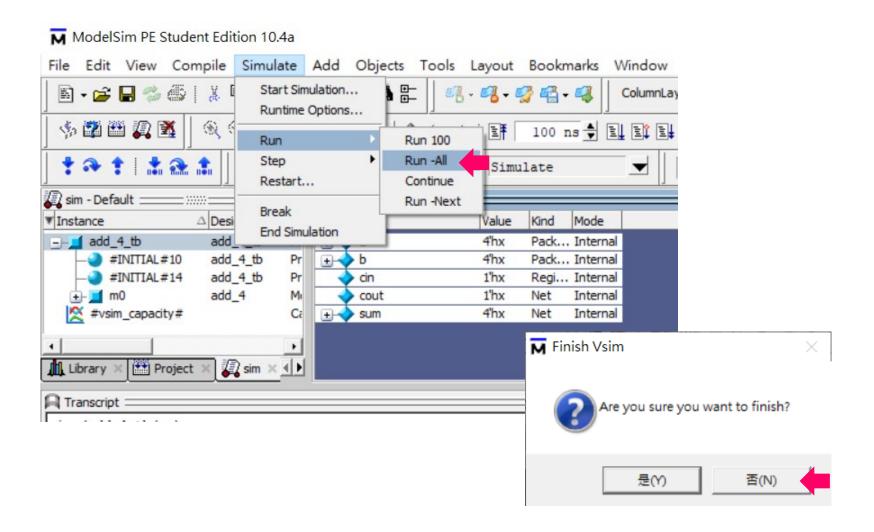
Save Waveform Format



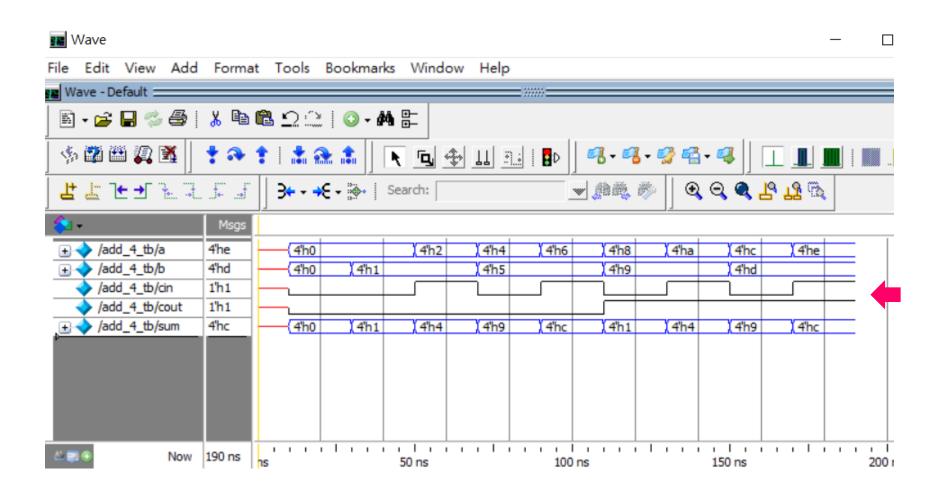
Load Waveform Format (Optional)



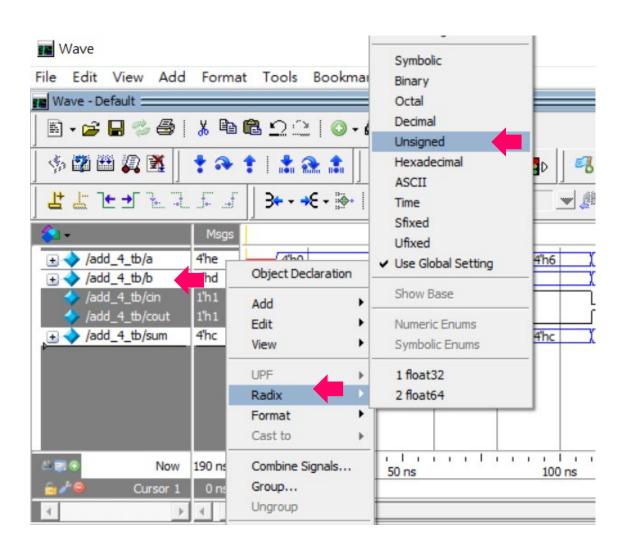
Run Simulation



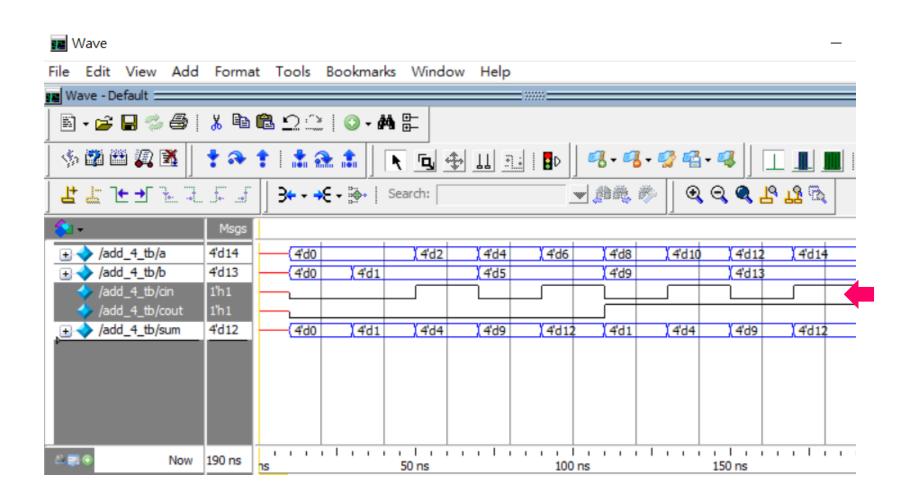
Simulation Result – Waveform 1



Change Radix



Simulation Result – Waveform 2



Simulation Result – Text Message

```
Transcript :
SIM./ auu 4 LD/a
sim:/add 4 tb/b \
sim:/add 4 tb/cin \
sim:/add 4 tb/cout \
sim:/add 4 tb/sum
write format wave -window .main pane.wave.interior.cs.body.pw.wf C:/Users/rdchen/Desktop/add 4/wave.do
VSIM 4> run -all
                                                Outputs: cout = x
# Time:
         0 ns, Inputs: a = x
                                   x cin = x.
# Time: 10 ns, Inputs: a = 0 b = 0 cin = 0, Outputs: cout = 0
# Time: 30 ns, Inputs: a = 0 b = 1 cin = 0, Outputs: cout = 0 sum = 1
# Time: 50 ns, Inputs: a = 2 b = 1 cin = 1, Outputs: cout = 0 sum = 4
# Time: 70 ns, Inputs: a = 4 b = 5 cin = 0,
                                               Outputs: cout = 0 sum = 9
# Time: 90 ns, Inputs: a = 6 b = 5 cin = 1, Outputs: cout = 0 sum = 12
# Time: 110 ns, Inputs: a = 8 b = 9 cin = 0, Outputs: cout = 1 sum = 1
# Time: 130 ns, Inputs: a = 10 b = 9 cin = 1, Outputs: cout = 1 sum = 4
# Time: 150 ns, Inputs: a = 12 b = 13 cin = 0, Outputs: cout = 1 sum = 9
# Time: 170 ns, Inputs: a = 14 b = 13 cin = 1, Outputs: cout = 1 sum = 12
# ** Note: $finish : C:/Users/rdchen/Desktop/add 4/add 4 tb.v(24)
    Time: 190 ns Iteration: 0 Instance: /add 4 tb
# Break in Module add 4 tb at C:/Users/rdchen/Desktop/add 4/add 4 tb.v line 24
VSIM 5>
```

End Simulation

