數位系統技術

Lab 02
Full Adder 設計

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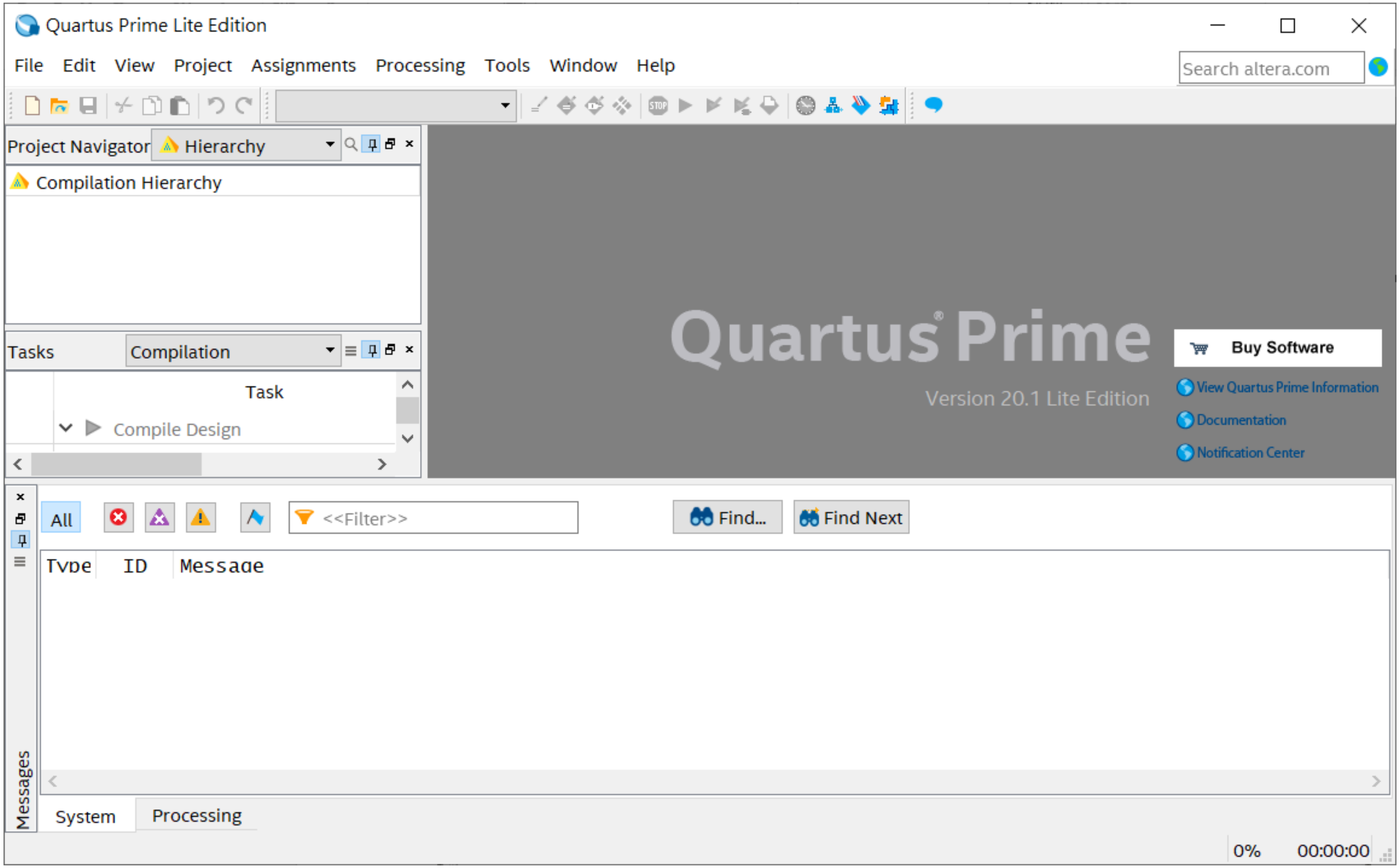
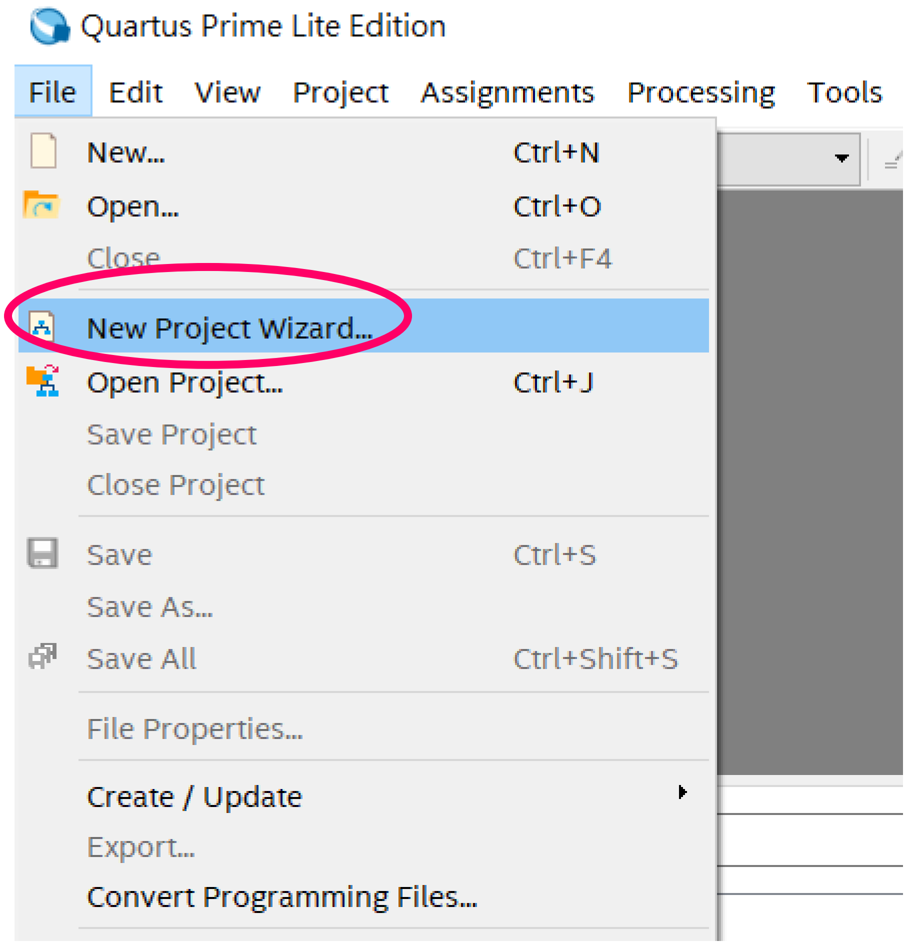
實驗目的

- 熟悉 Quartus 軟體之操作
- 學習如何以schematic方式設計half adder及full adder
- 學習如何對所設計之電路進行functional及timing simulation
- 學習如何將所設計之電路燒錄至FPGA晶片中，並利用實驗板週邊進行電路功能驗證

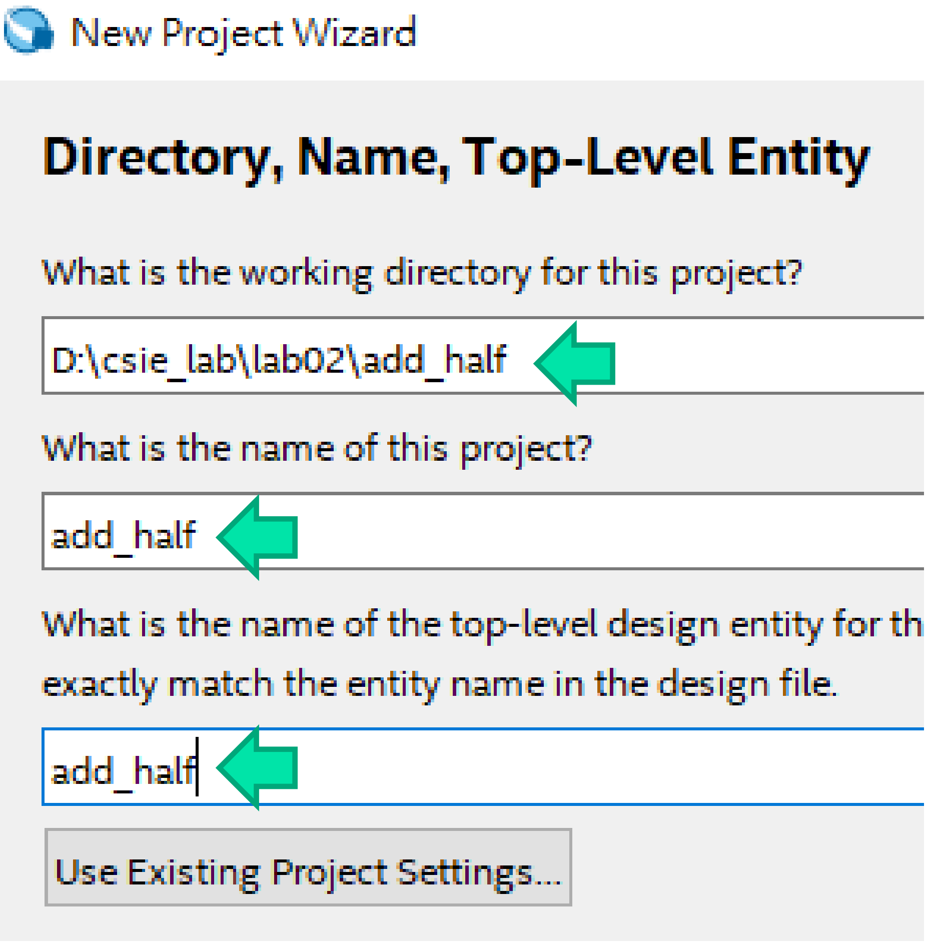
Get Started


Quartus Prime Lite Edition
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
Search altera.com
Project Navigator
Hierarchy
Compilation Hierarchy
Tasks
Compilation
Task
Compile Design
Quartus® Prime
Version 20.1 Lite Edition
Buy Software
View Quartus Prime Information
Documentation
Notification Center
All
<<Filter>>
Find...
Find Next
Type
ID
Message
Messages
System
Processing
0%
00:00:00

Create a New Project



Create a New Project - add_half



New Project Wizard

Directory, Name, Top-Level Entity

What is the working directory for this project?

D:\csie_lab\lab02\add_half

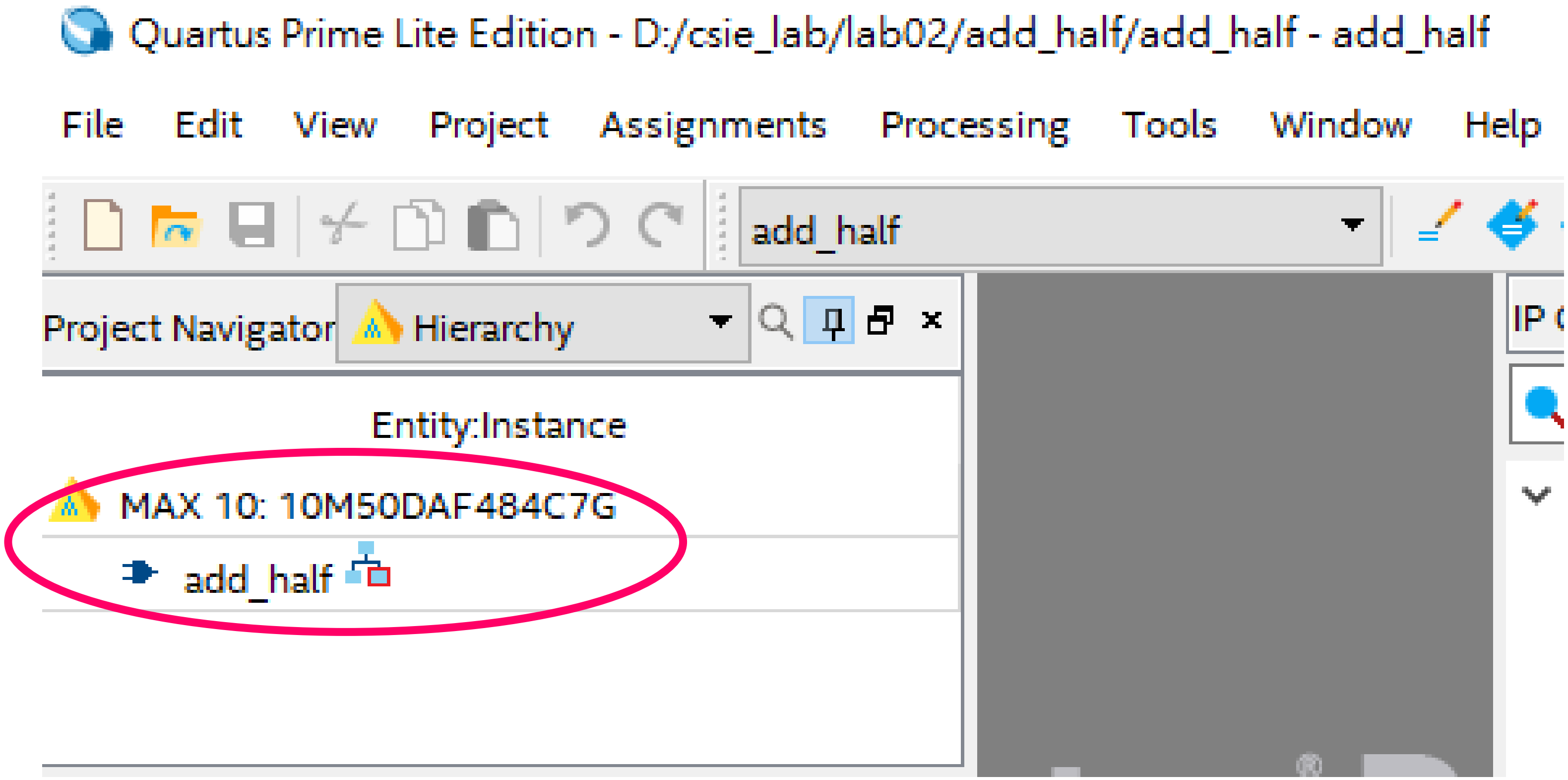
What is the name of this project?

add_half

What is the name of the top-level design entity for th
exactly match the entity name in the design file.

add_half

Select a Device



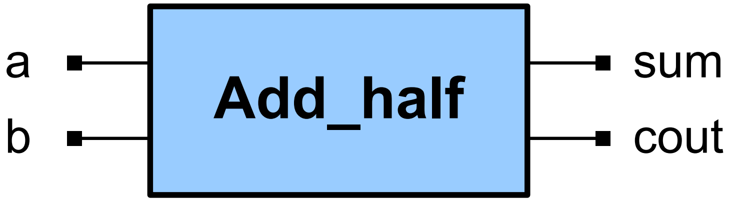
Quartus Prime Lite Edition - D:/csie_lab/lab02/add_half/add_half - add_half

Entity:Instance

MAX 10: 10M50DAF484C7G

add_half

Design Example: Half Adder

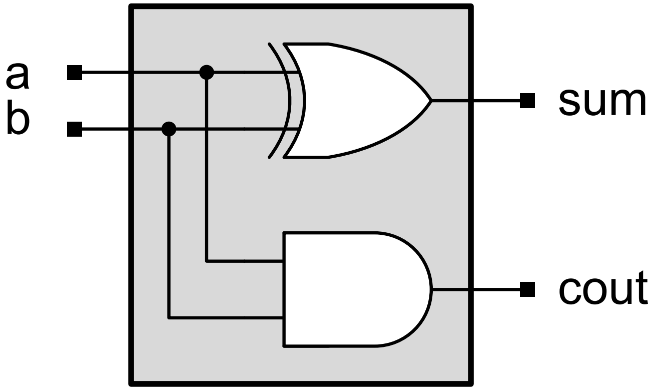


a\b	0	1
0	0	1
1	1	0

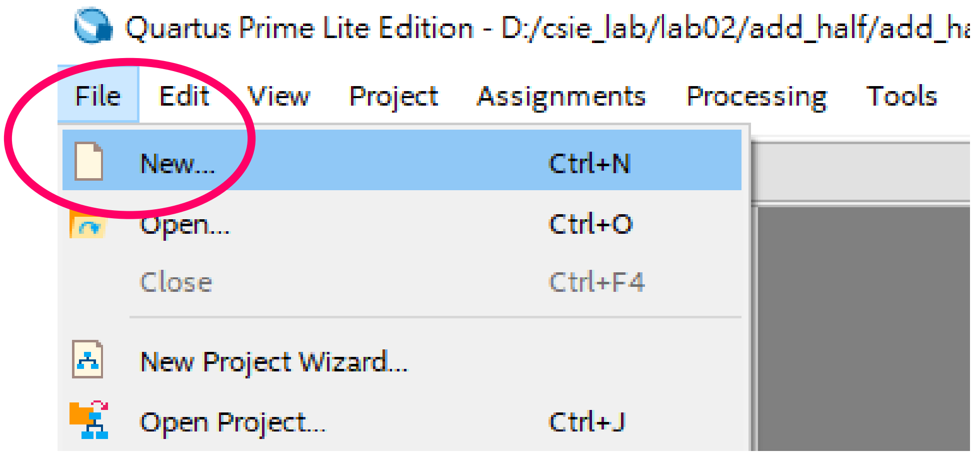
a\b	0	1
0	0	0
1	0	1

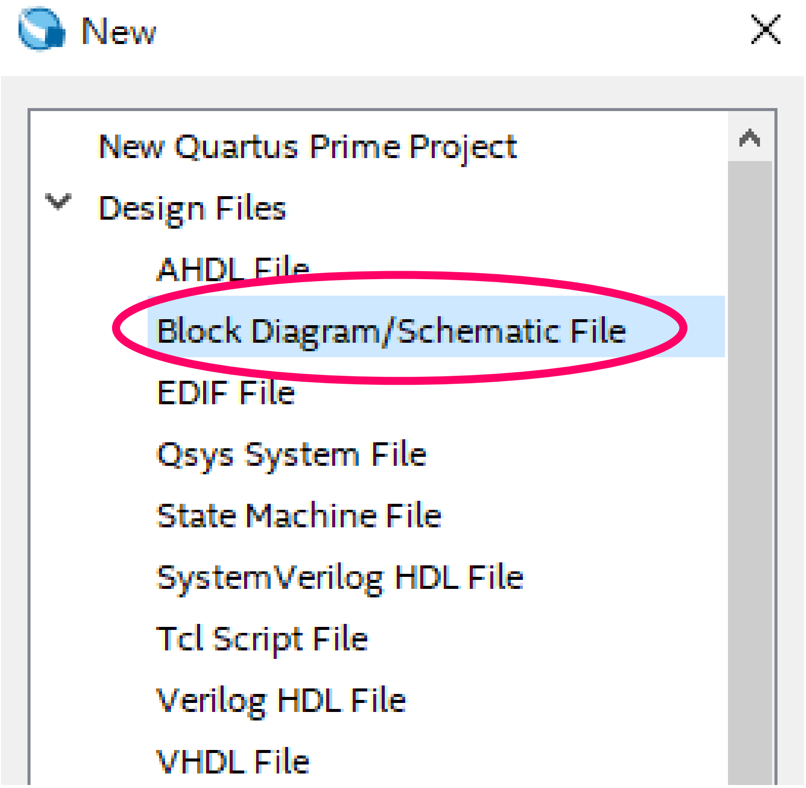
$sum = a \oplus b$

$cout = a \cdot b$

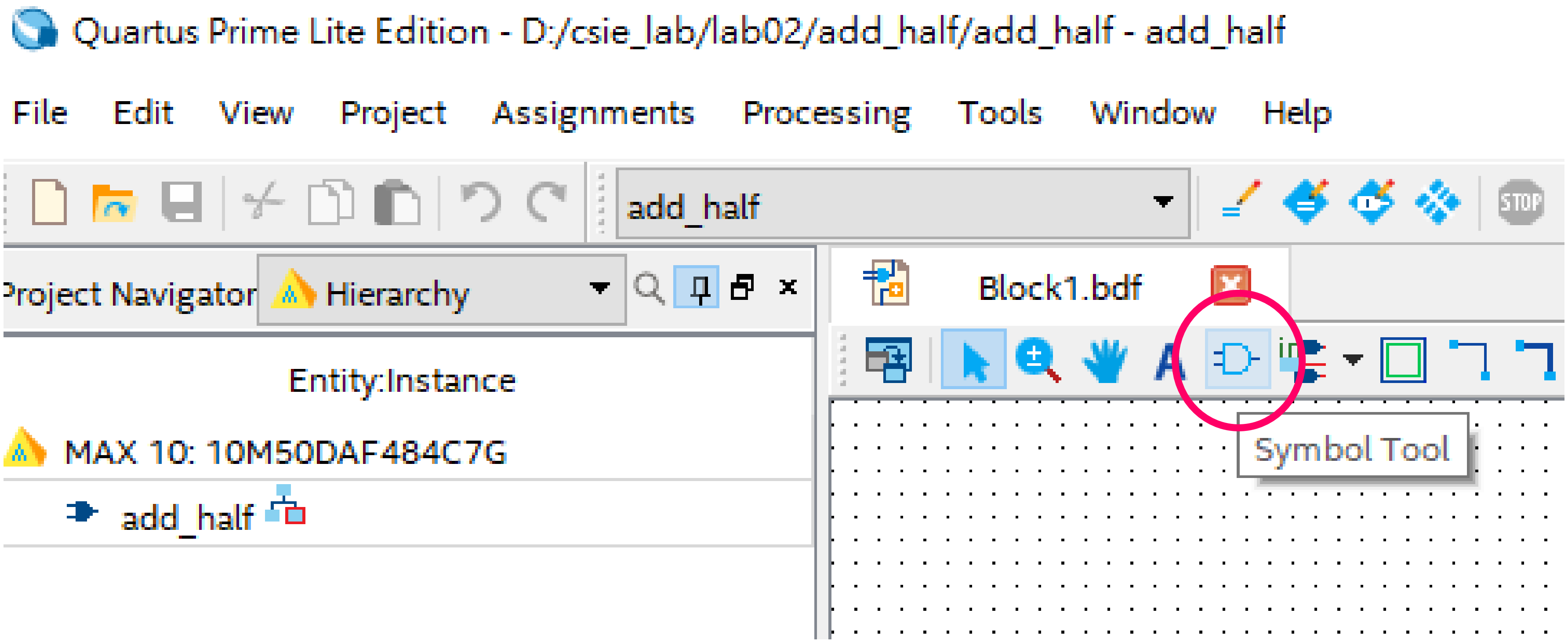


Use Block Editor for Schematic Design

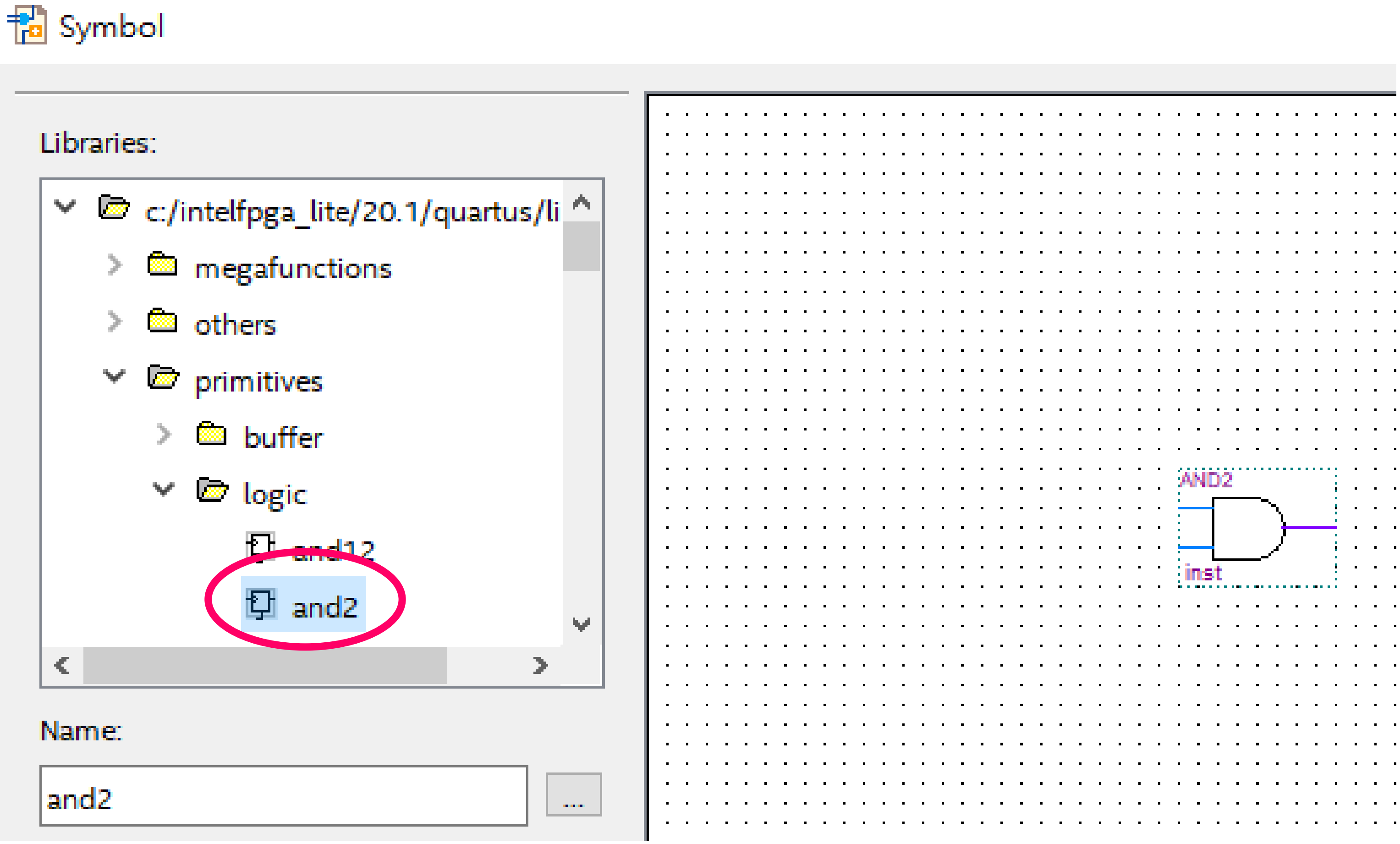




Import Logic Gates

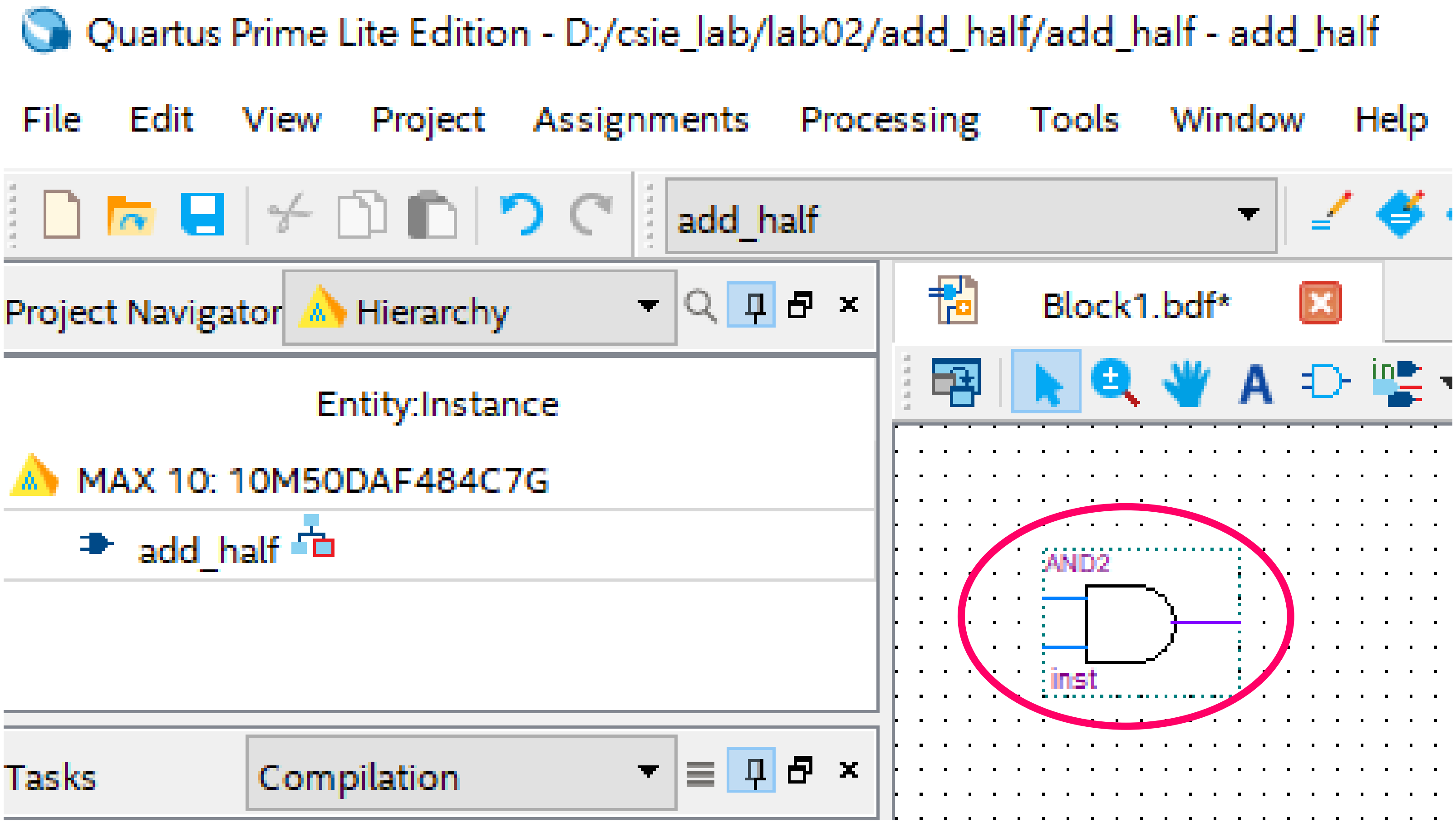


Select and Import an AND2 Gate

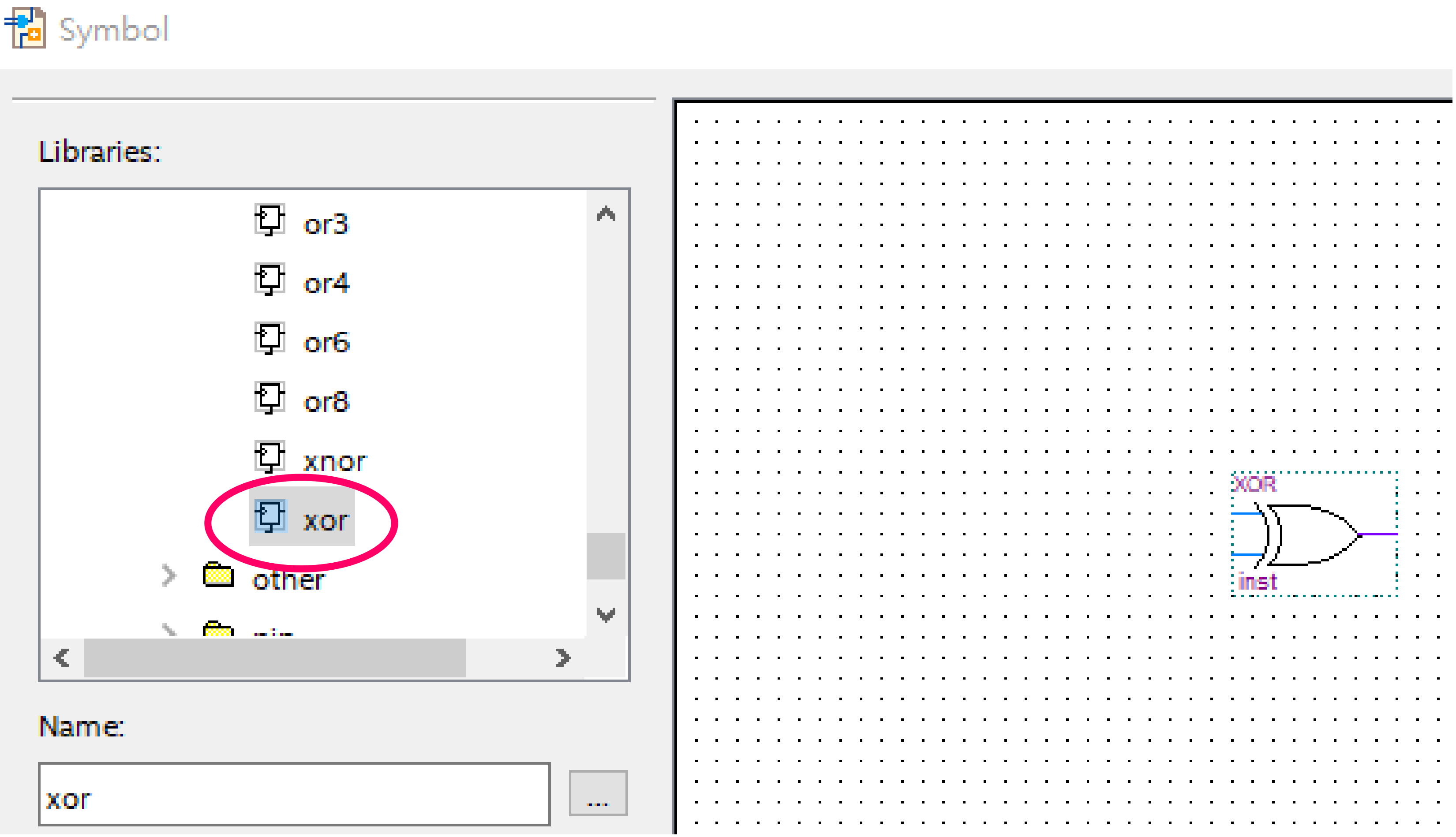


Name: and2

An AND2 Gate is Imported

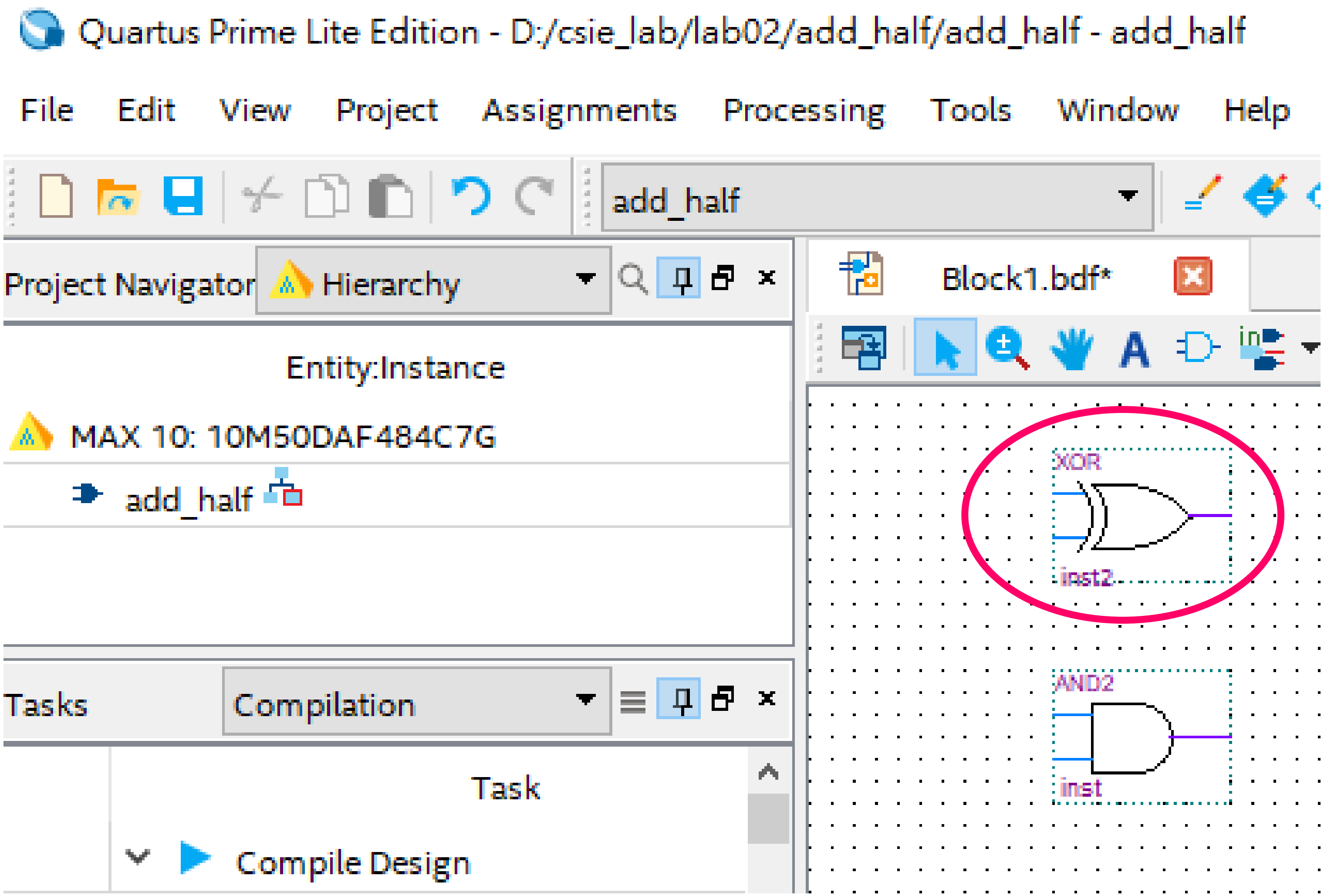


Select and Import an XOR Gate

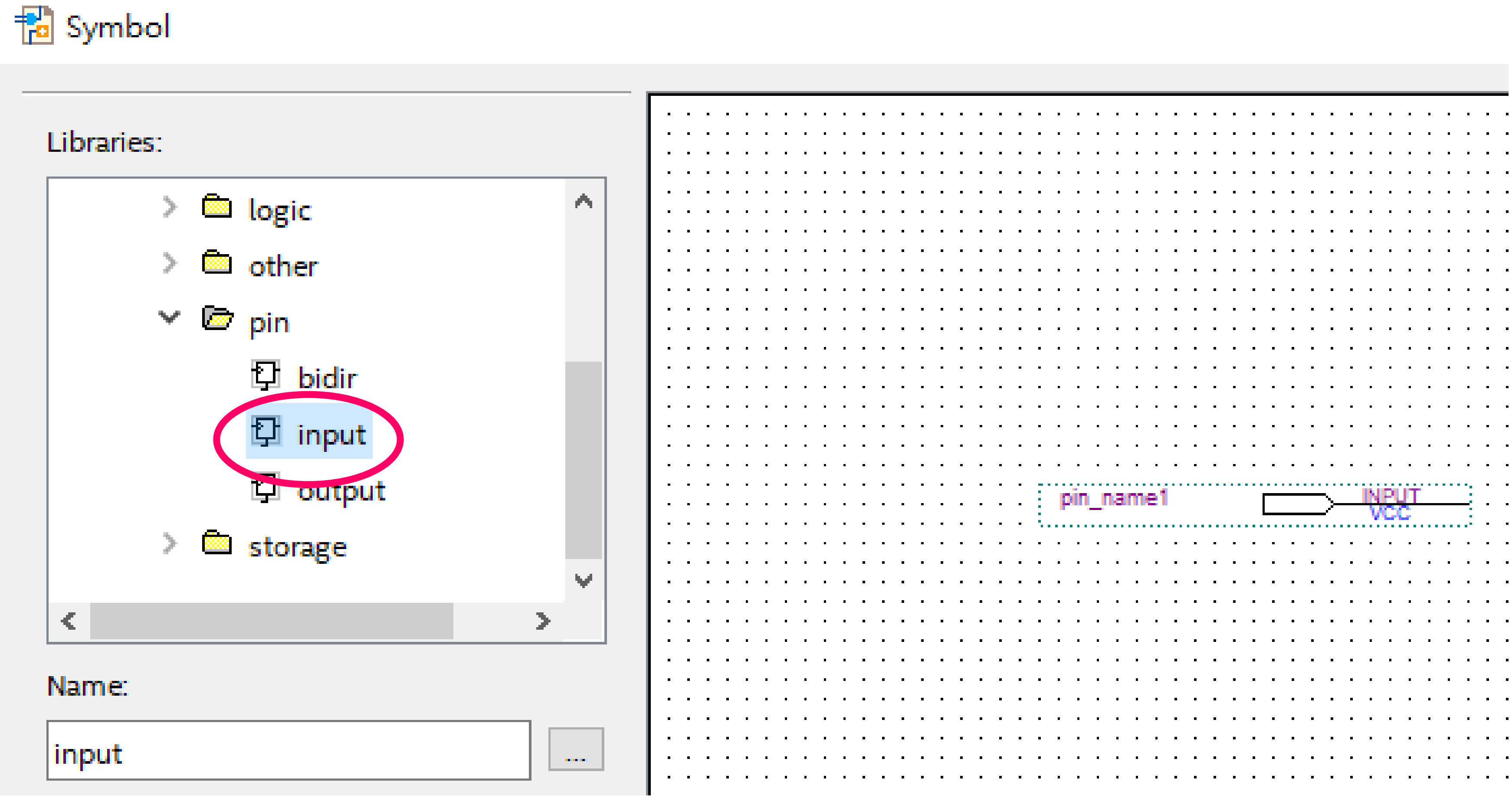


Name: xor

An XOR Gate is Imported



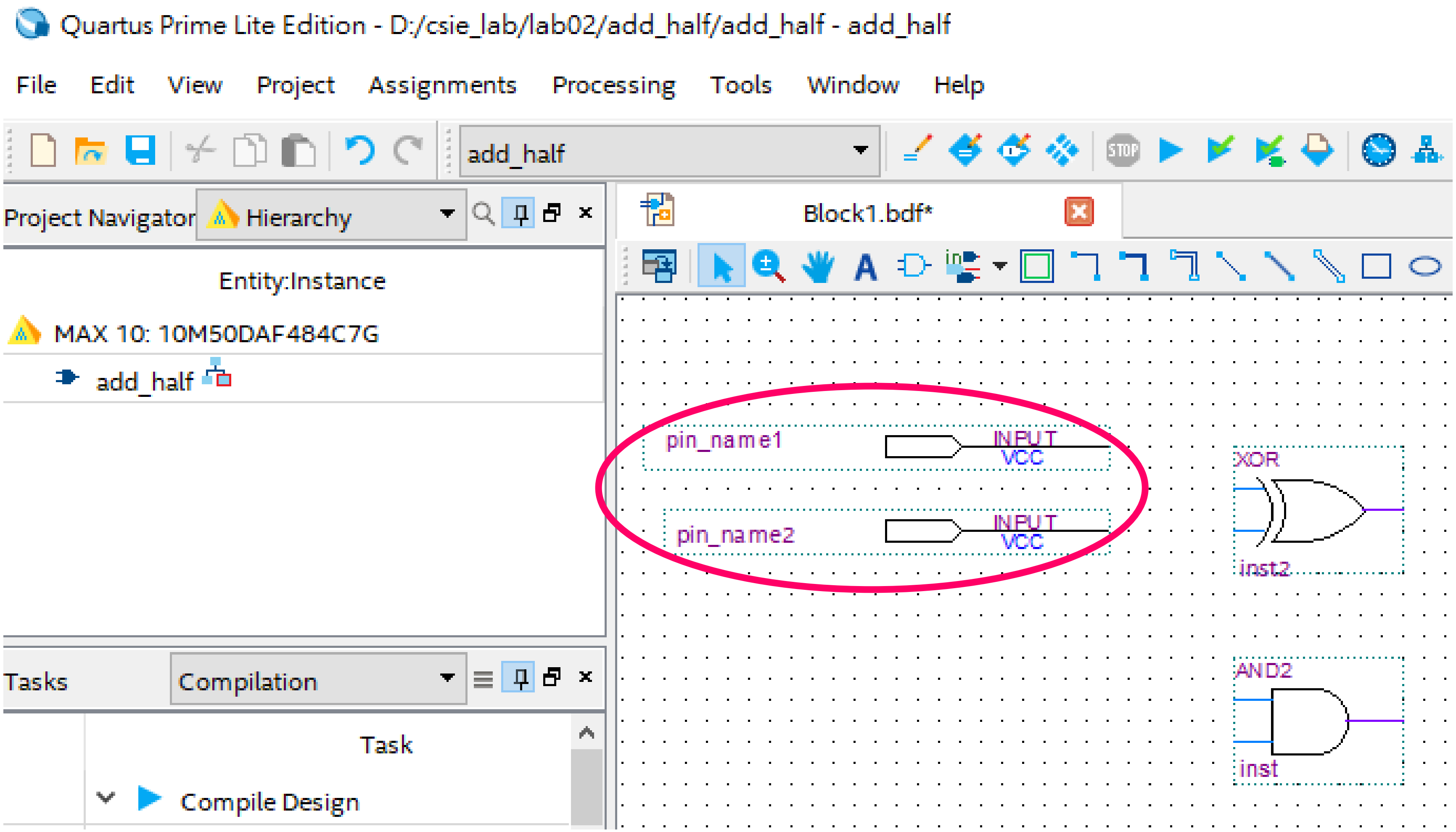
Select and Import an Input Pin



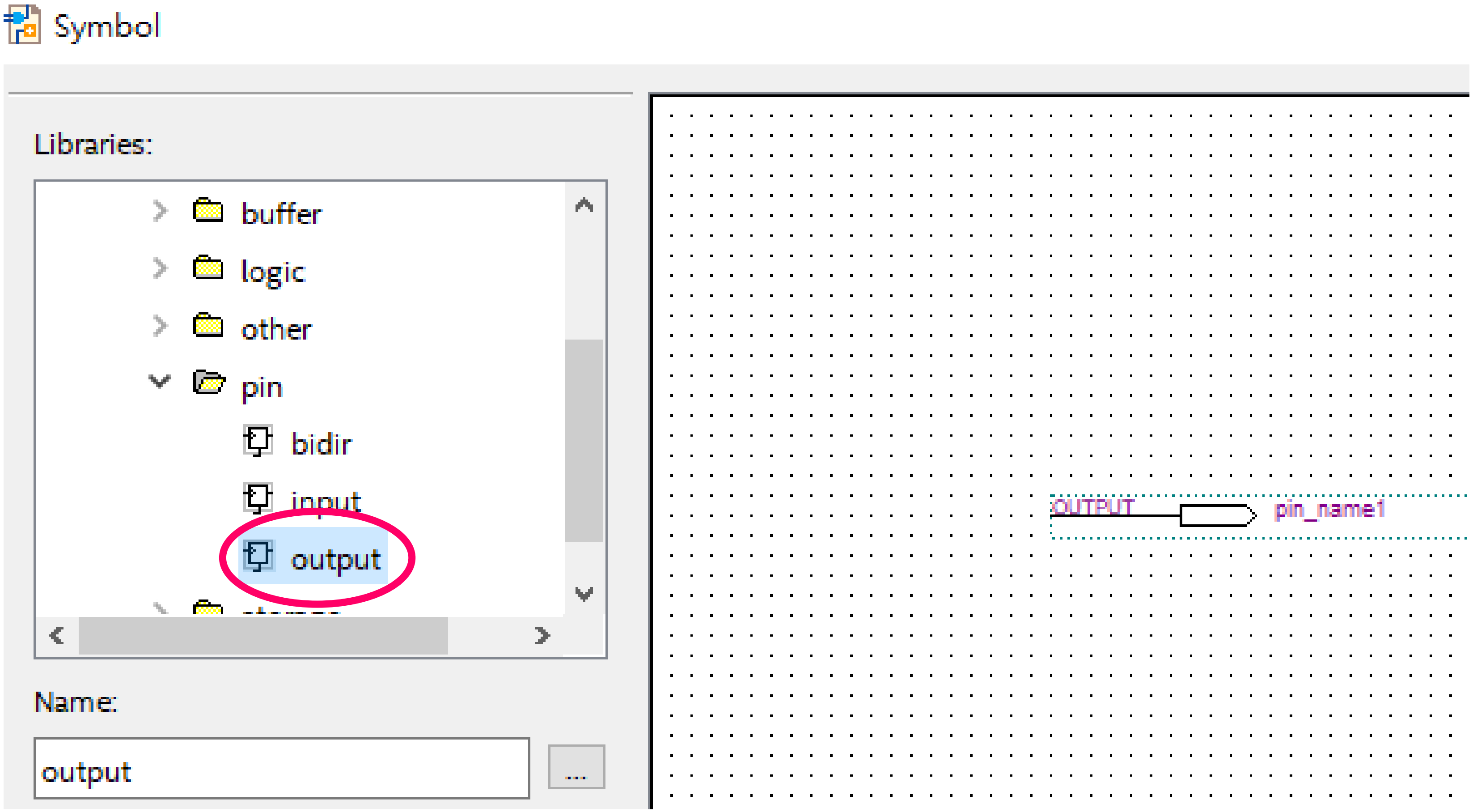
Symbol

Name: input

Two Input Pins are Imported

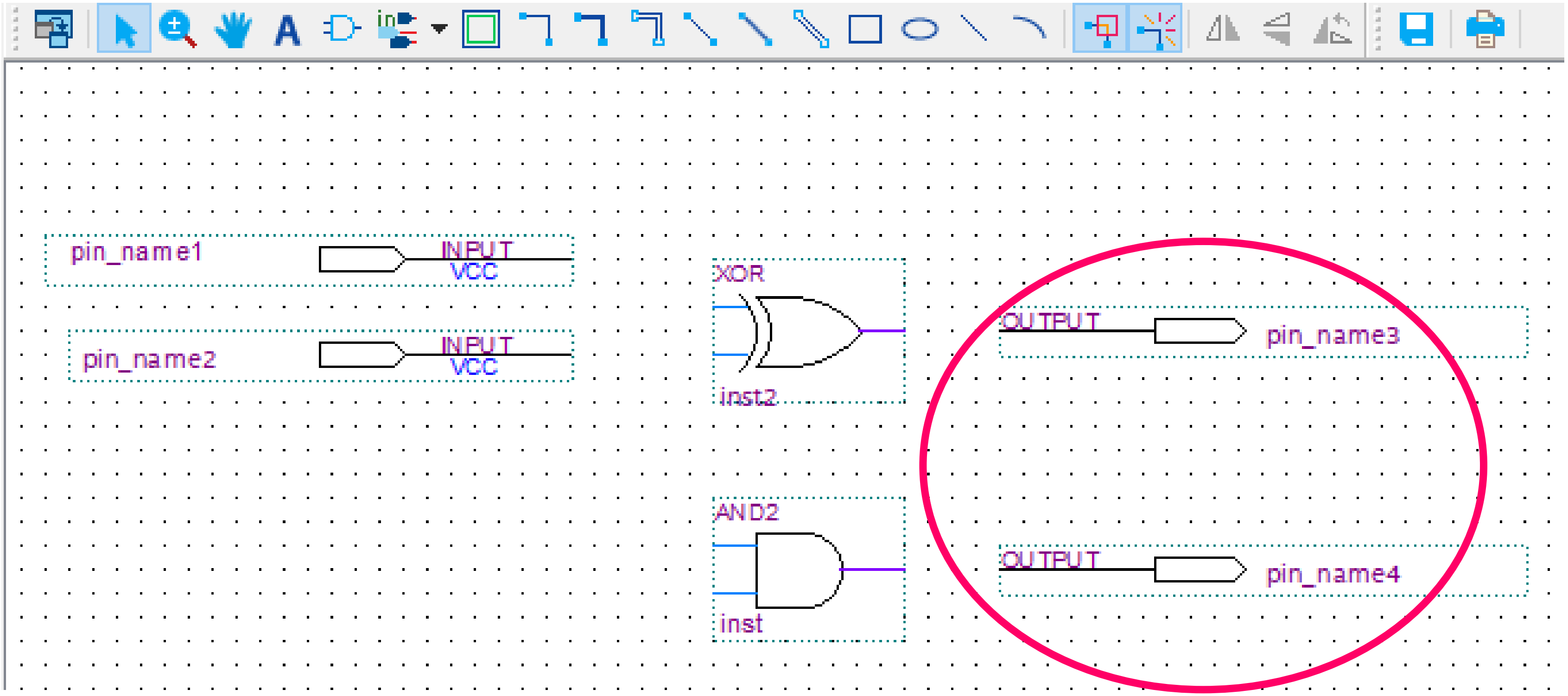


Select and Import an Output Pin

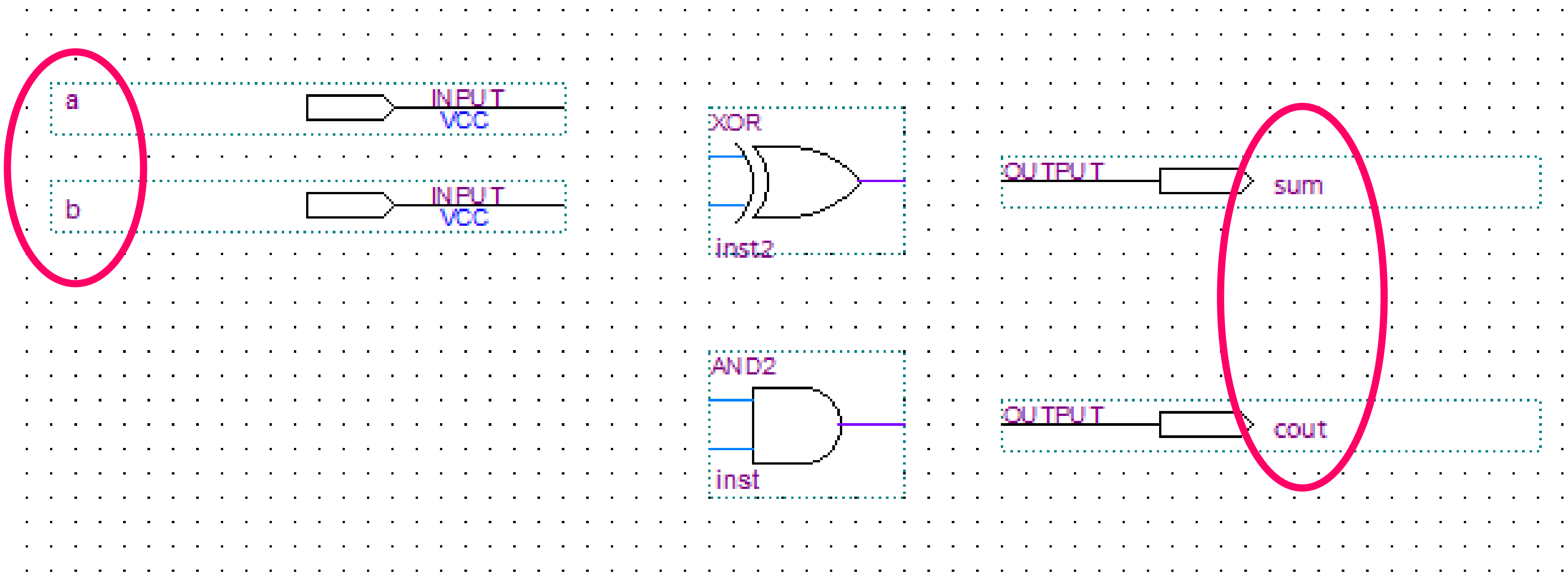


Name: output

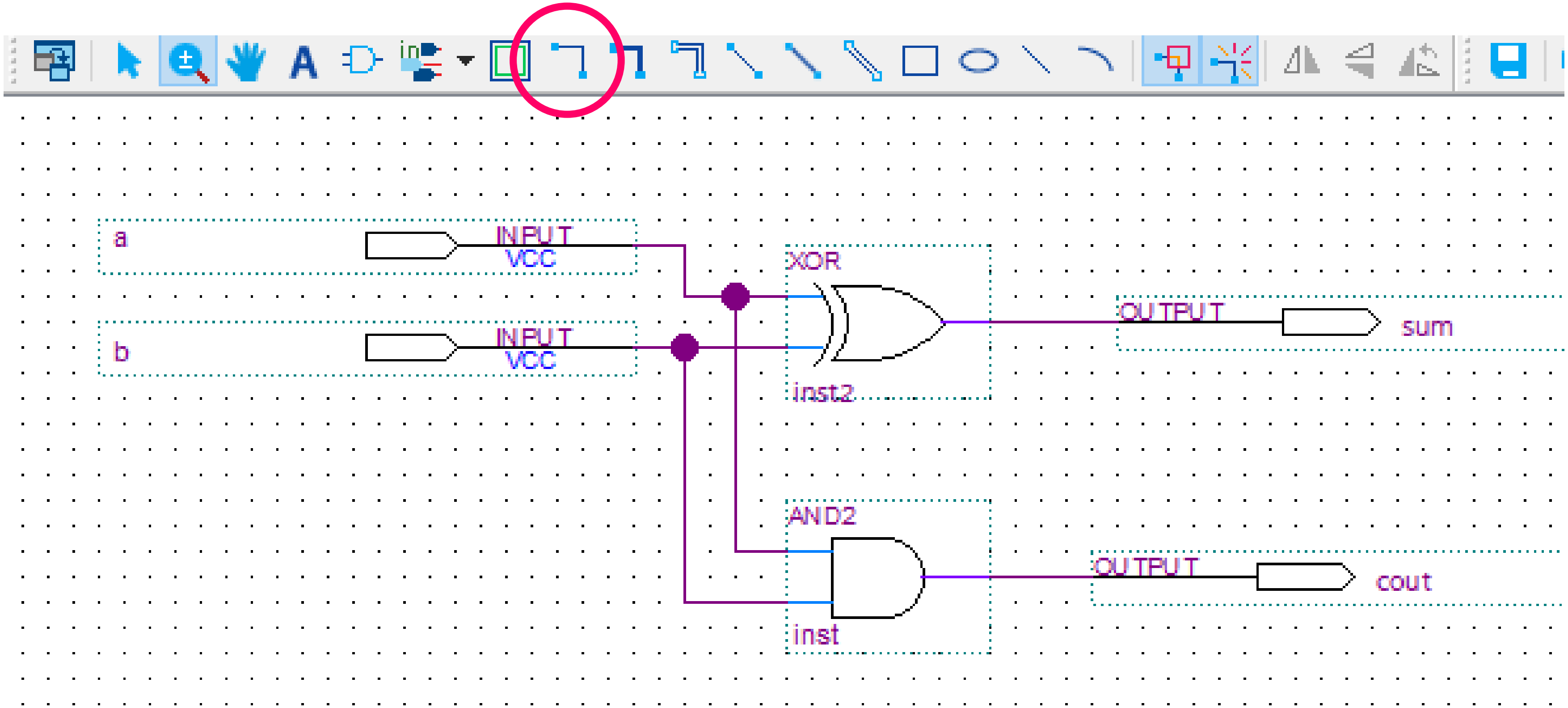
Two Output Pins are Imported



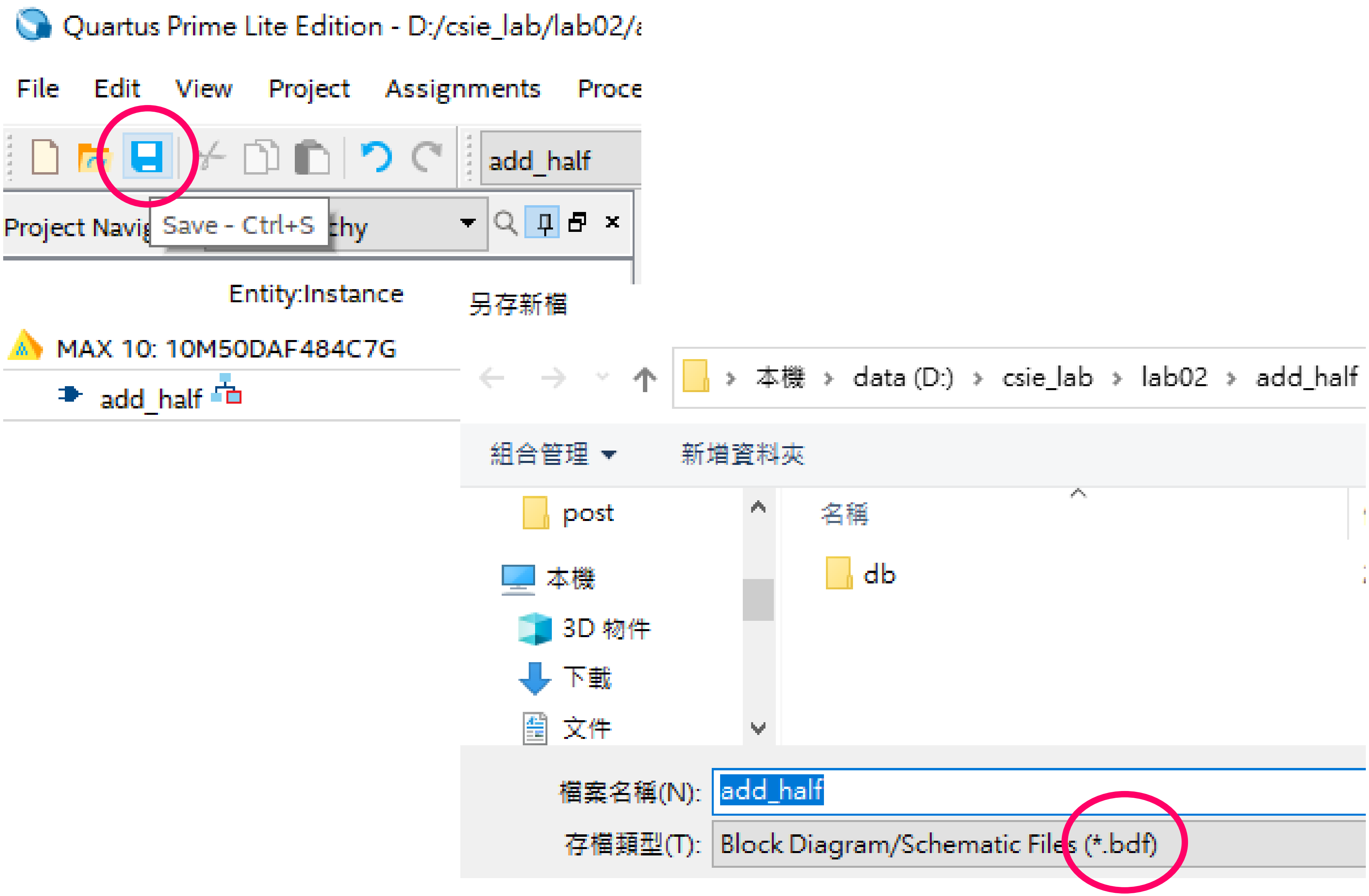
Assign Names to I/O Pins



Connect Nodes with Wires



Save the Schematic File



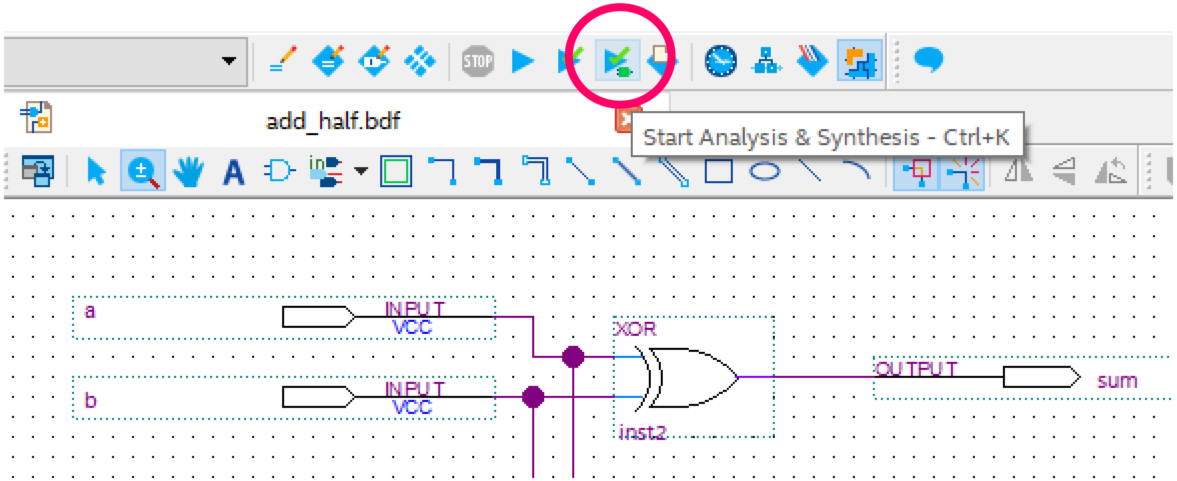
檔案名稱(N): add_half

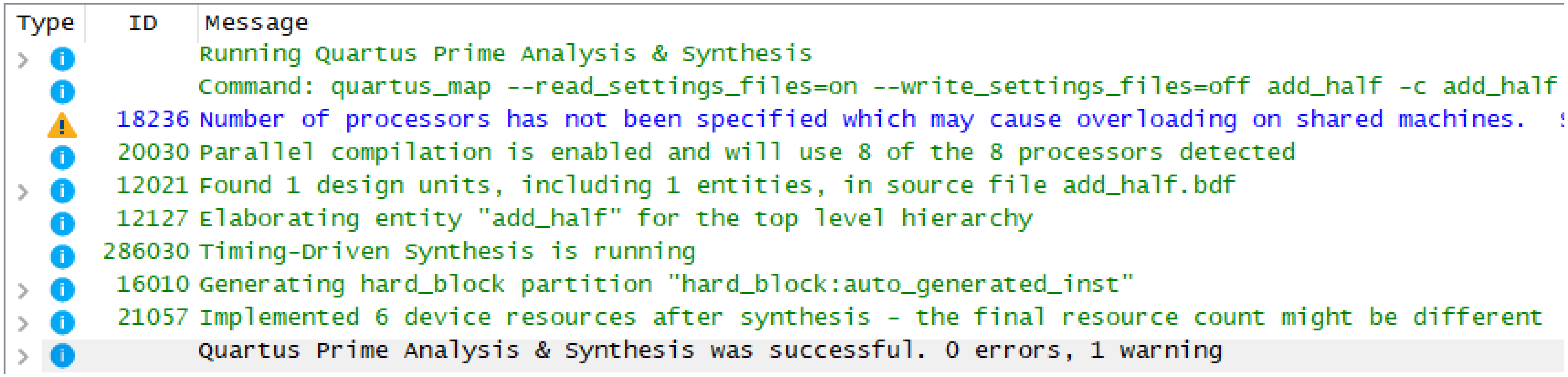
存檔類型(T): Block Diagram/Schematic Files (*.bdf)

Synthesize the Schematic Circuit

- The synthesis tool translates the schematic into logic expressions.
- Then the technology mapping step determines how each logic expression should be implemented in the logic elements (LEs) available in the target chip.
- The ***Analysis & Synthesis*** function performs the synthesis step.
- It produces a circuit of logic elements, where each element can be directly implemented in the target chip.

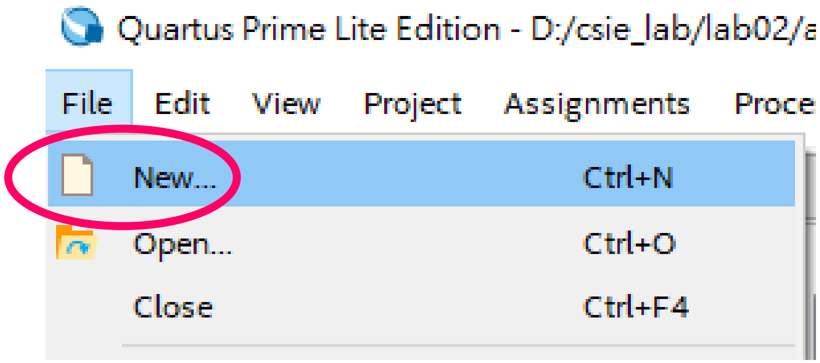
Run “Analysis & Synthesis” for Functional Simulation

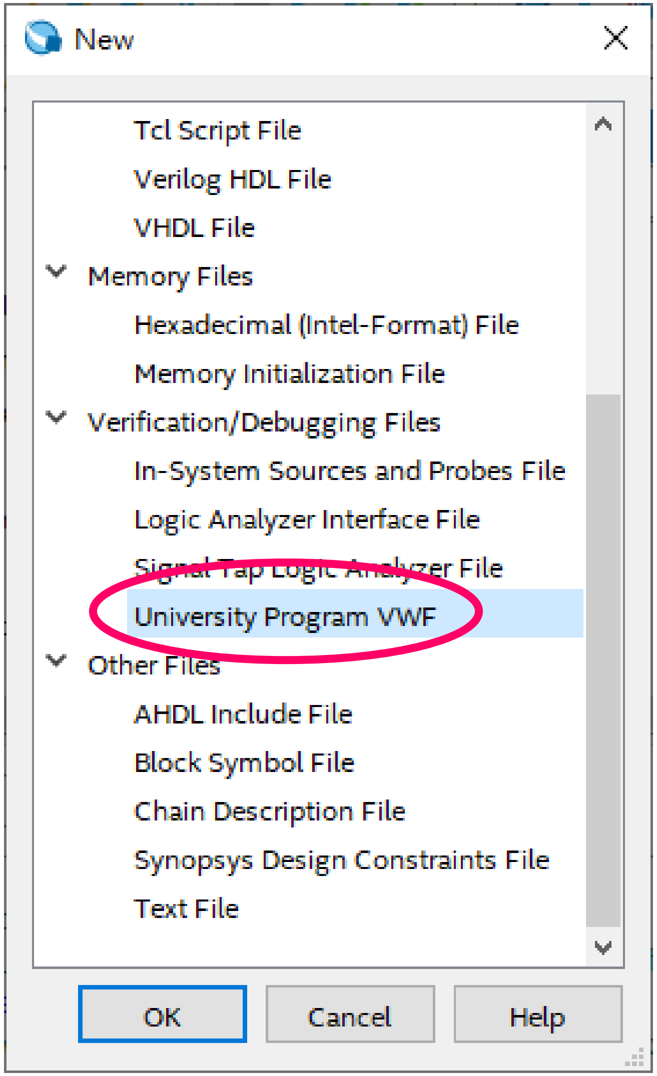




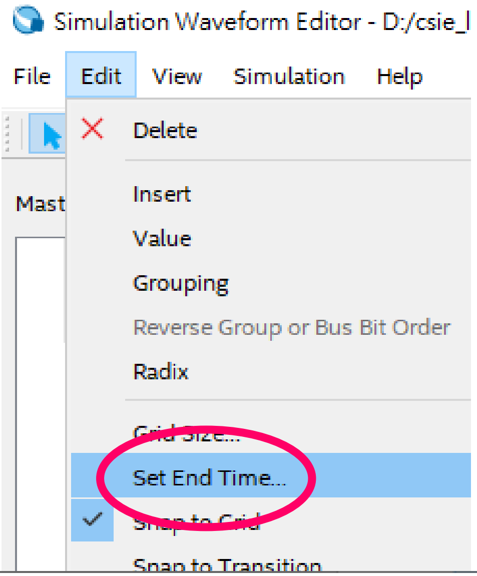
```
Type   ID     Message
            Running Quartus Prime Analysis & Synthesis
            Command: quartus_map --read_settings_files=on --write_settings_files=off add_half -c add_half
      18236 Number of processors has not been specified which may cause overloading on shared machines.
      20030 Parallel compilation is enabled and will use 8 of the 8 processors detected
      12021 Found 1 design units, including 1 entities, in source file add_half.bdf
      12127 Elaborating entity "add_half" for the top level hierarchy
     286030 Timing-Driven Synthesis is running
      16010 Generating hard_block partition "hard_block:auto_generated_inst"
      21057 Implemented 6 device resources after synthesis - the final resource count might be different
            Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning
```

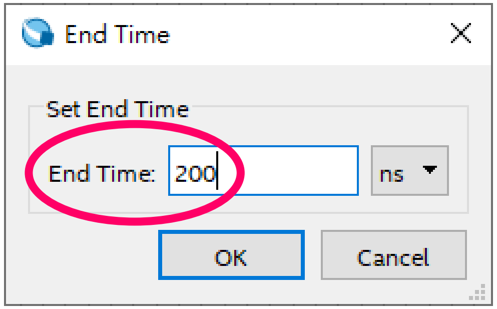
Create a Waveform File




New
Tcl Script File
Verilog HDL File
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes File
Logic Analyzer Interface File
Signal Tap Logic Analyzer File
University Program VWF
Other Files
AHDL Include File
Block Symbol File
Chain Description File
Synopsys Design Constraints File
Text File
OK
Cancel
Help

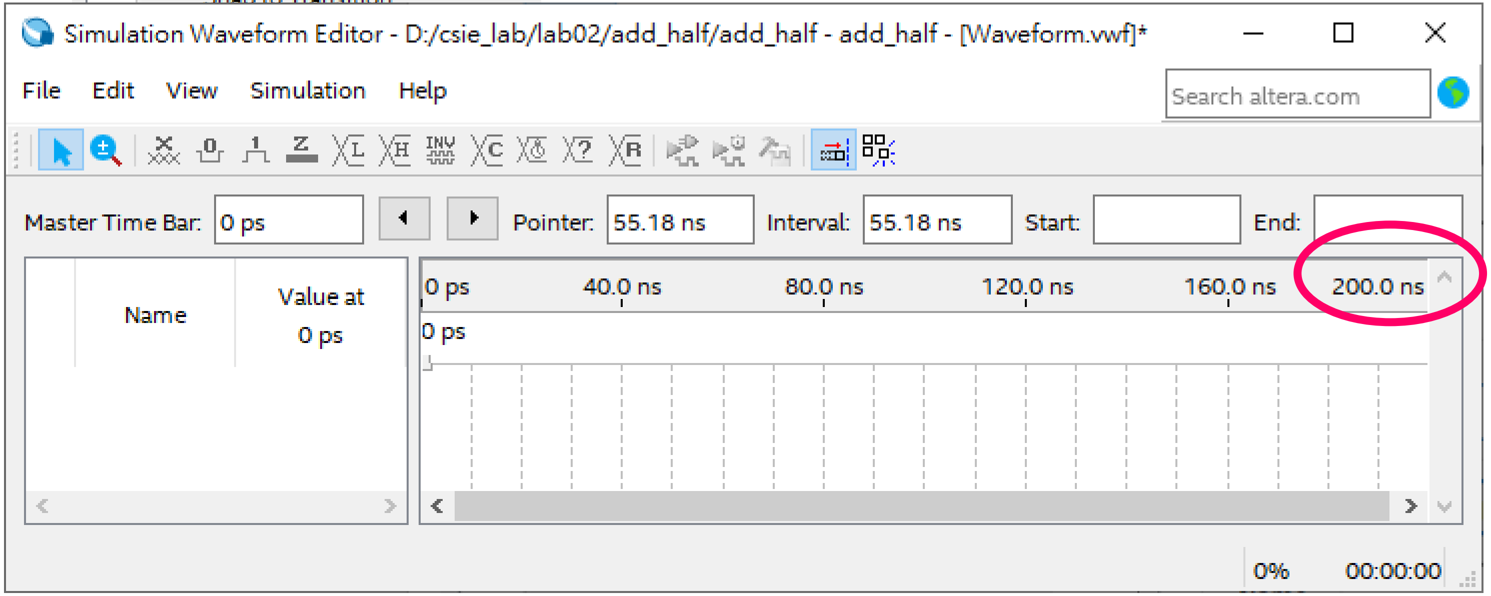
Set End Time for Simulation




End Time

Set End Time

End Time: 200 ns


Simulation Waveform Editor - D:/csie_lab/lab02/add_half/add_half - add_half - [Waveform.vwf]*

Master Time Bar: 0 ps

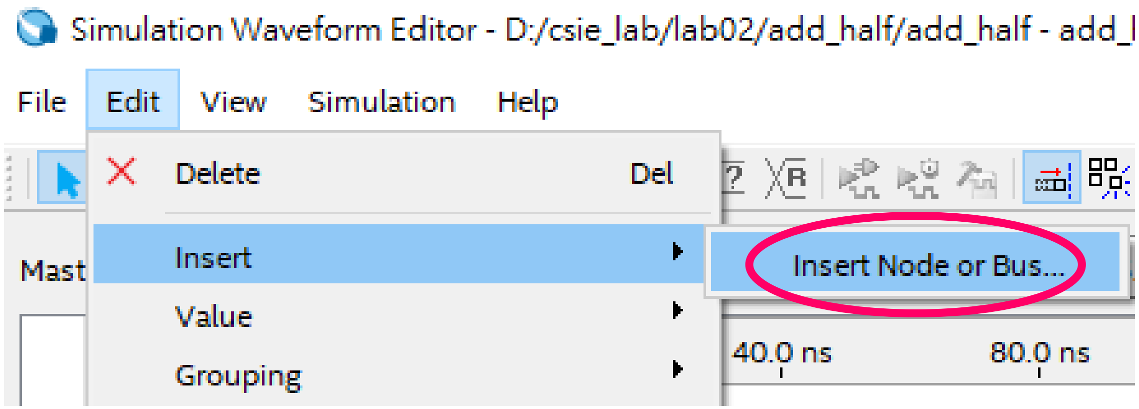
Pointer: 55.18 ns

Interval: 55.18 ns

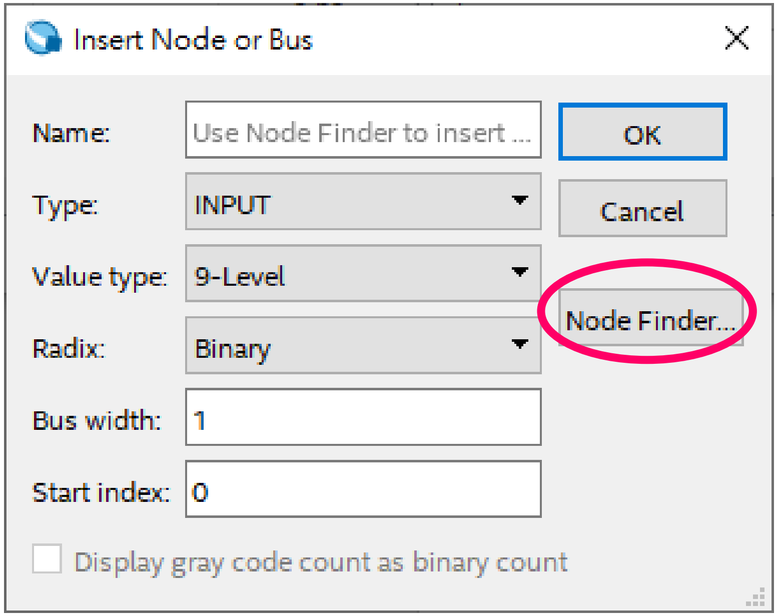
Start:

End:

Insert Node for I/O Signals (1/3)



Simulation Waveform Editor - D:/csie_lab/lab02/add_half/add_half - add_l



Insert Node or Bus

Name: Use Node Finder to insert ...

Type: INPUT

Value type: 9-Level

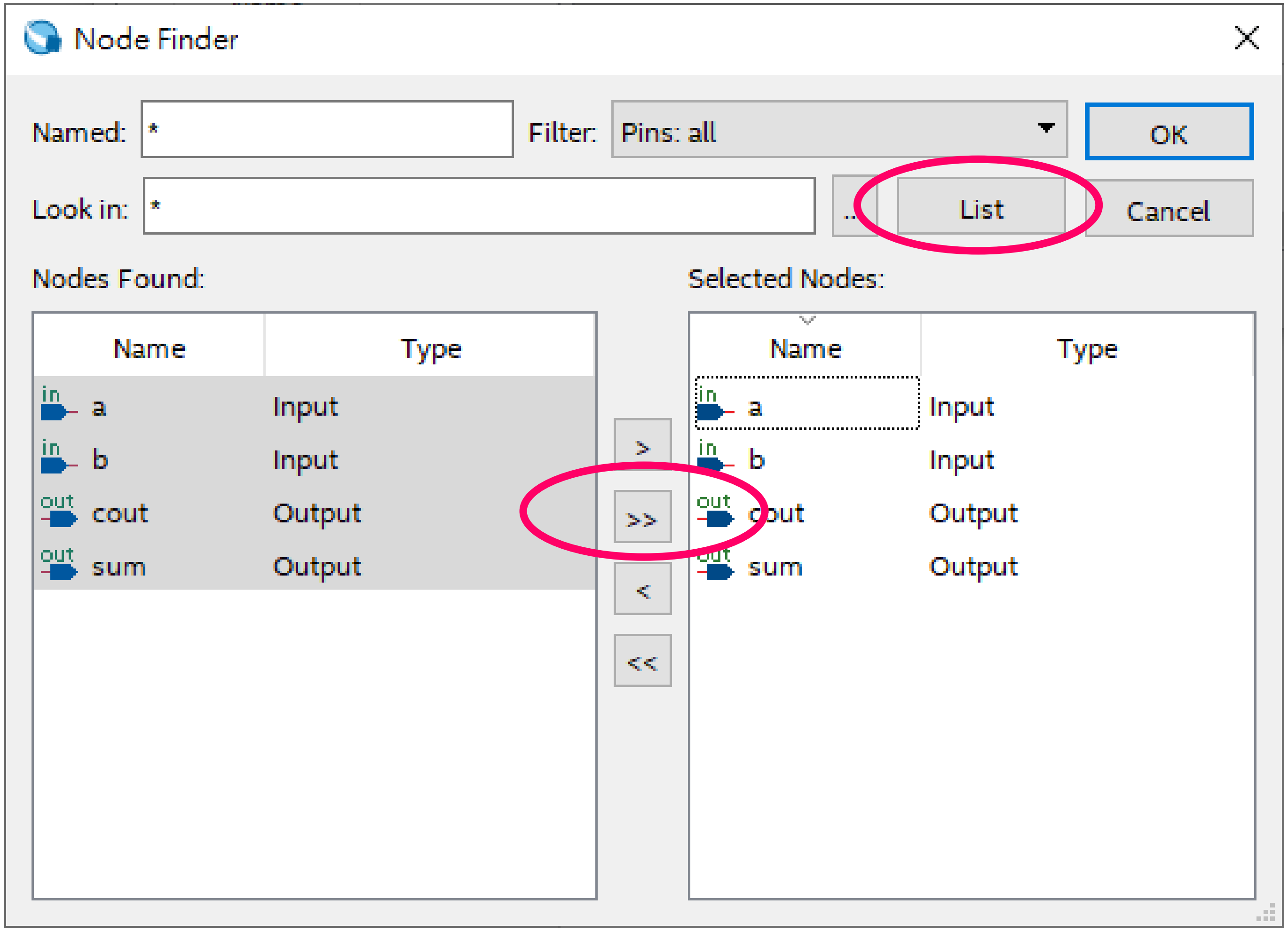
Radix: Binary

Bus width: 1

Start index: 0

□ Display gray code count as binary count

Insert Node for I/O Signals (2/3)



Node Finder

Named: *

Filter: Pins: all

Look in: *

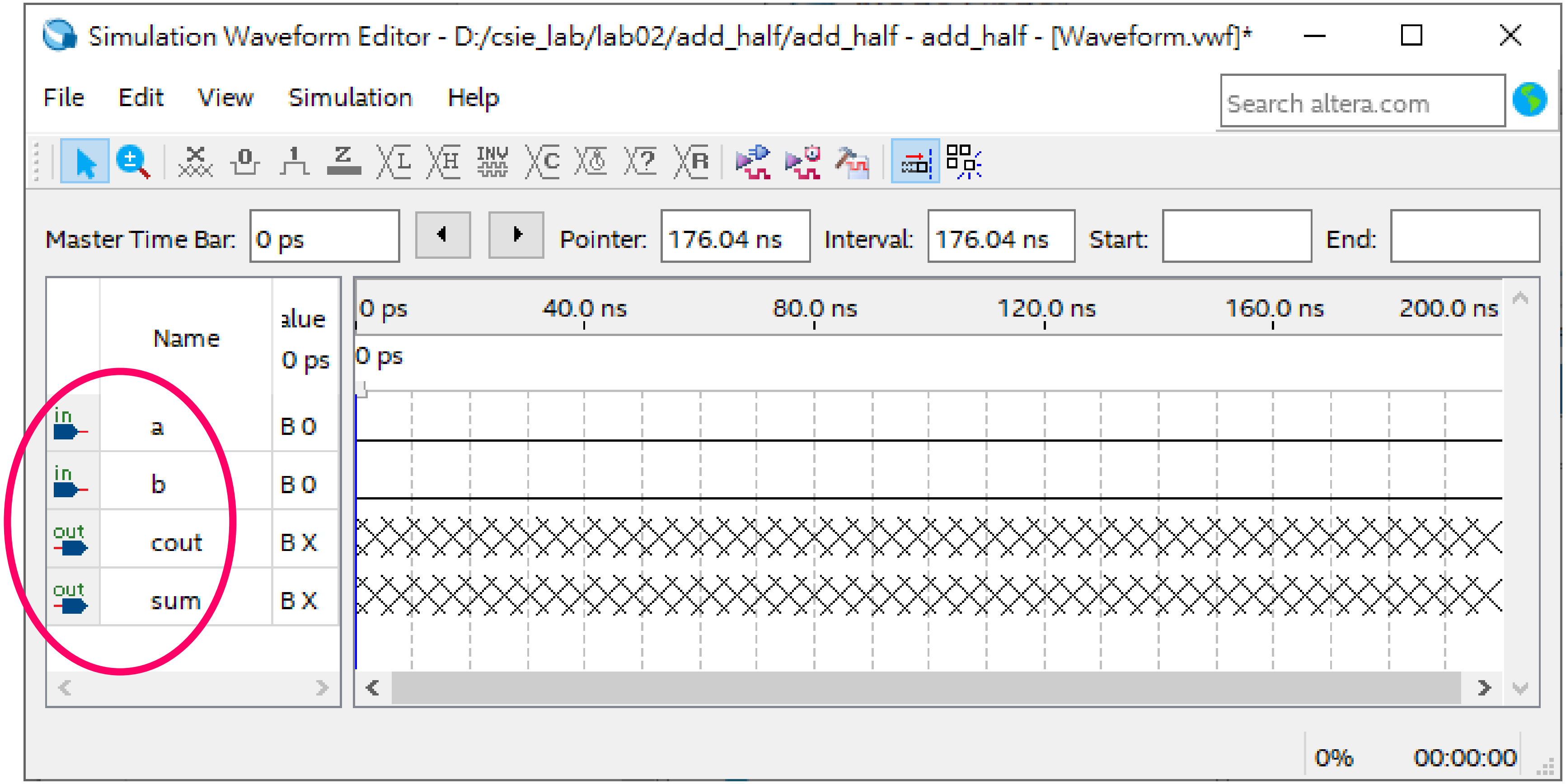
Nodes Found:

Name	Type
a	Input
b	Input
cout	Output
sum	Output

Selected Nodes:

Name	Type
a	Input
b	Input
cout	Output
sum	Output

Insert Node for I/O Signals (3/3)



Simulation Waveform Editor - D:/csie_lab/lab02/add_half/add_half - add_half - [Waveform.vwf]*

Master Time Bar: 0 ps

Pointer: 176.04 ns

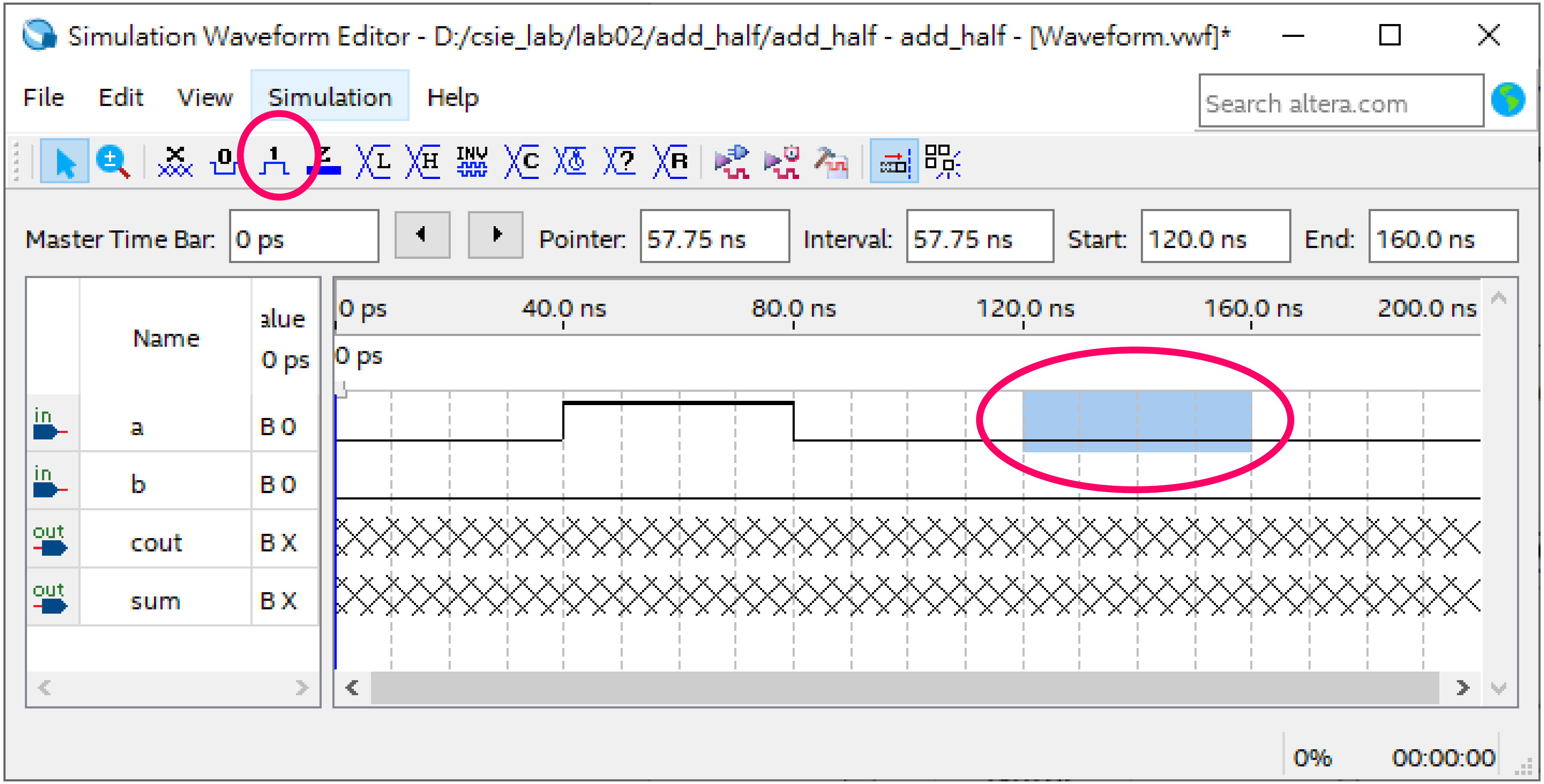
Interval: 176.04 ns

Start:

End:

Name	alue 0 ps
in a	B 0
in b	B 0
out cout	B X
out sum	B X

Set Values for Input Signals (1/2)



Simulation Waveform Editor - D:/csie_lab/lab02/add_half/add_half - add_half - [Waveform.vwf]*

Master Time Bar: 0 ps

Pointer: 57.75 ns

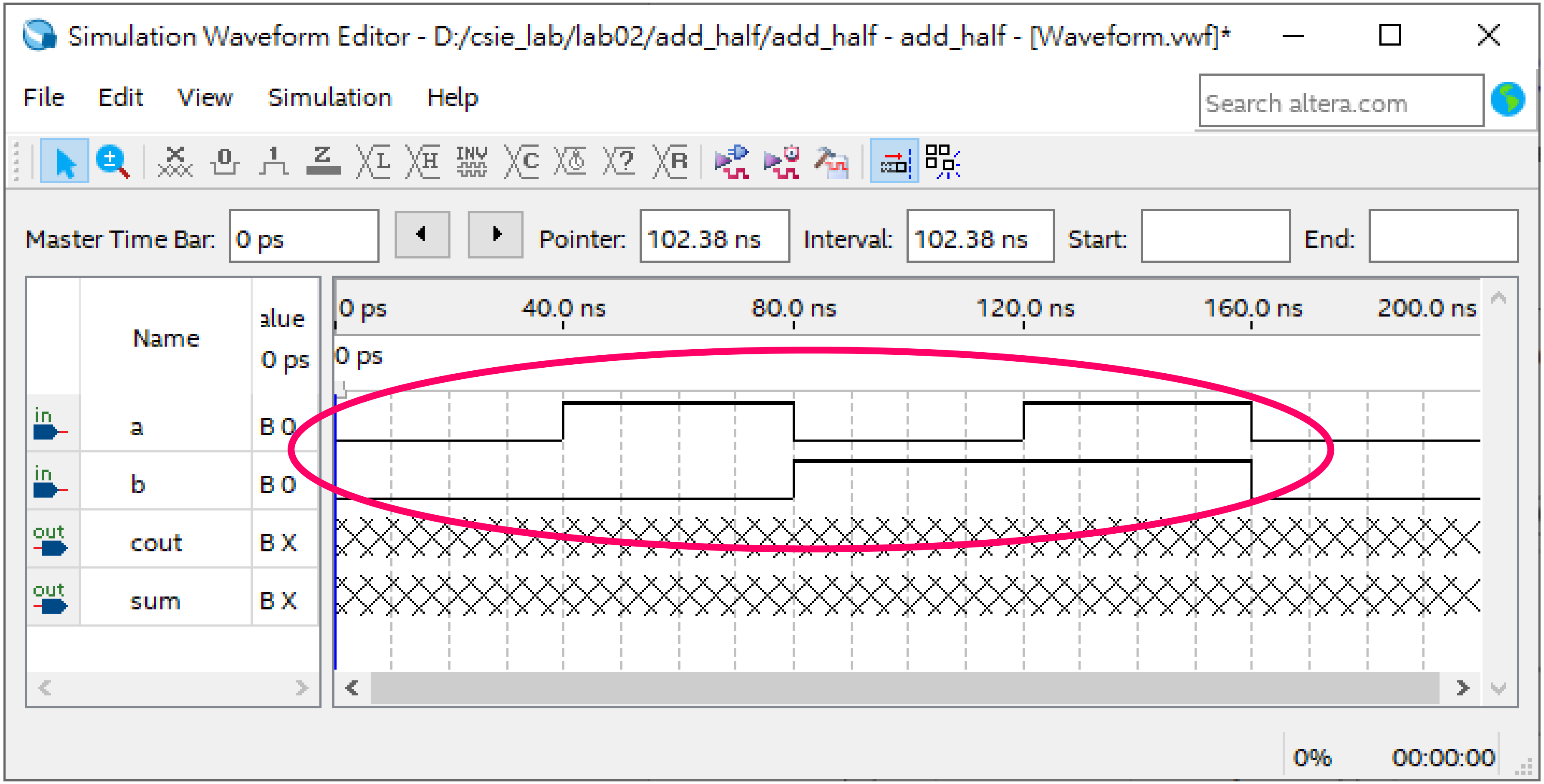
Interval: 57.75 ns

Start: 120.0 ns

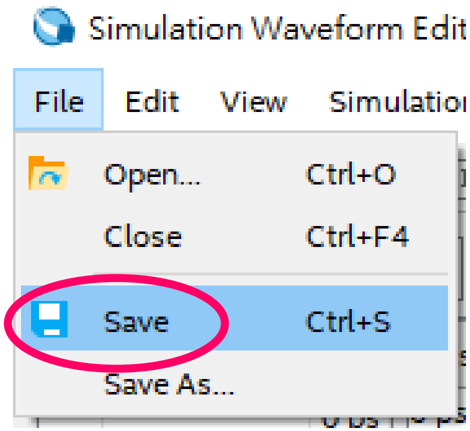
End: 160.0 ns

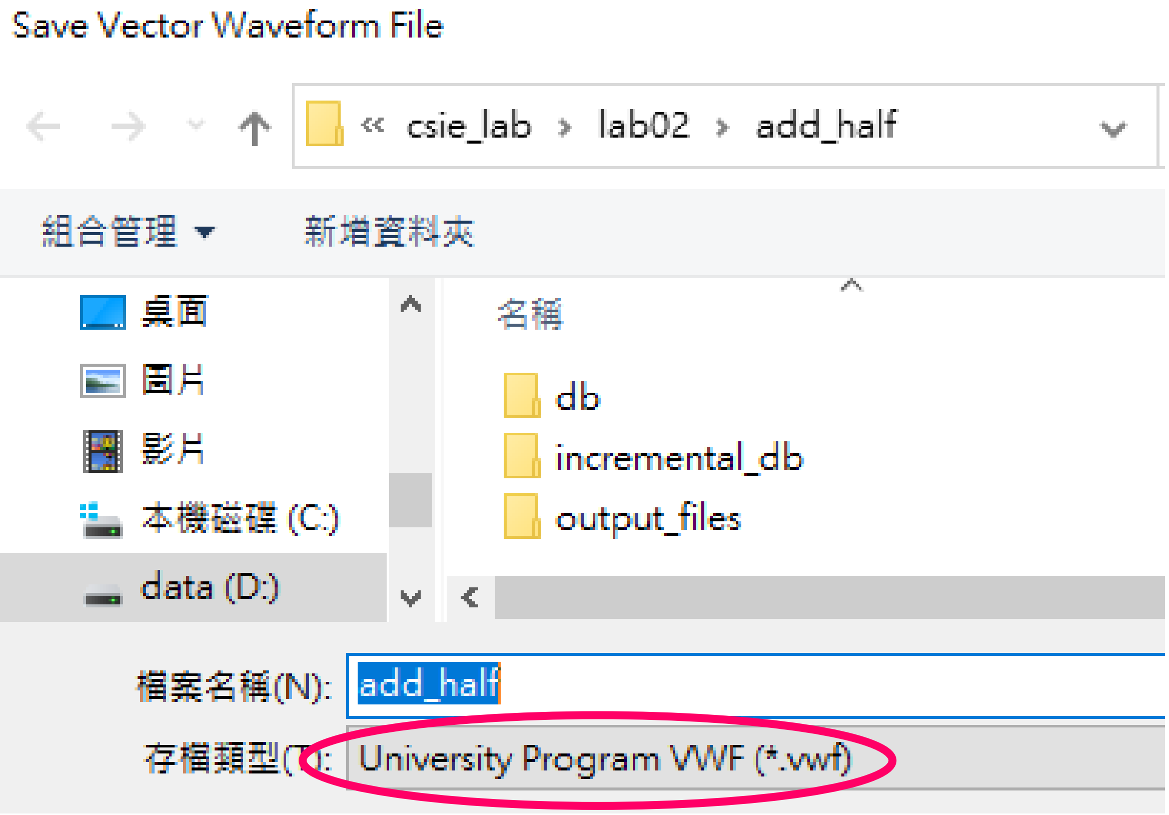
Name	Value 0 ps
a	B 0
b	B 0
cout	B X
sum	B X

Set Values for Input Signals (2/2)



Save the Waveform File





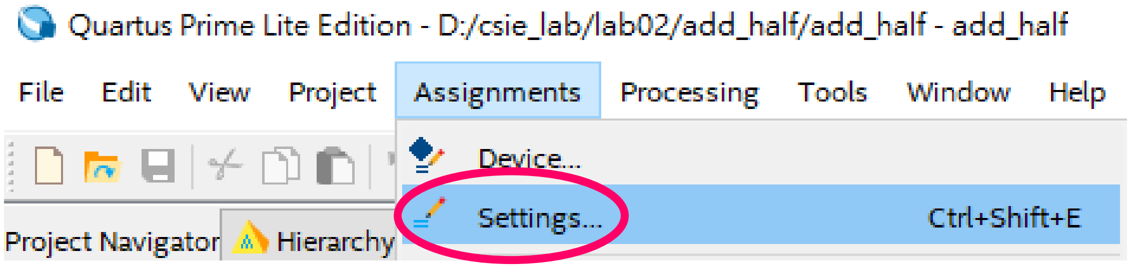
檔案名稱(N): add_half

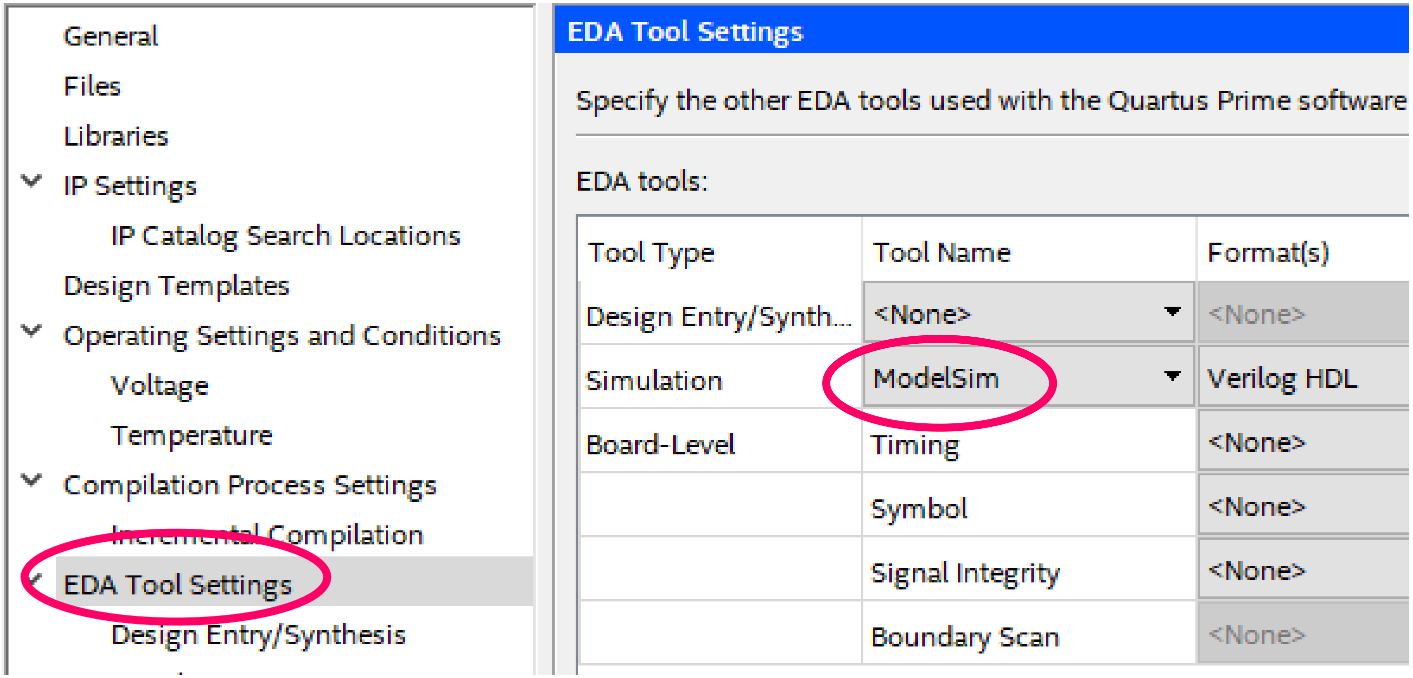
存檔類型(T): University Program VWF (*.vwf)

Simulation

- Functional simulation
  - Logic elements and interconnection wires are perfect, causing no delay in propagation of signals through the circuit.
  - Used to verify the functional correctness of a circuit.
  - Takes much less time.
- Timing simulation
  - Takes all propagation delays into account.

Set Simulation Tool - ModelSim


Quartus Prime Lite Edition - D:/csie_lab/lab02/add_half/add_half - add_half



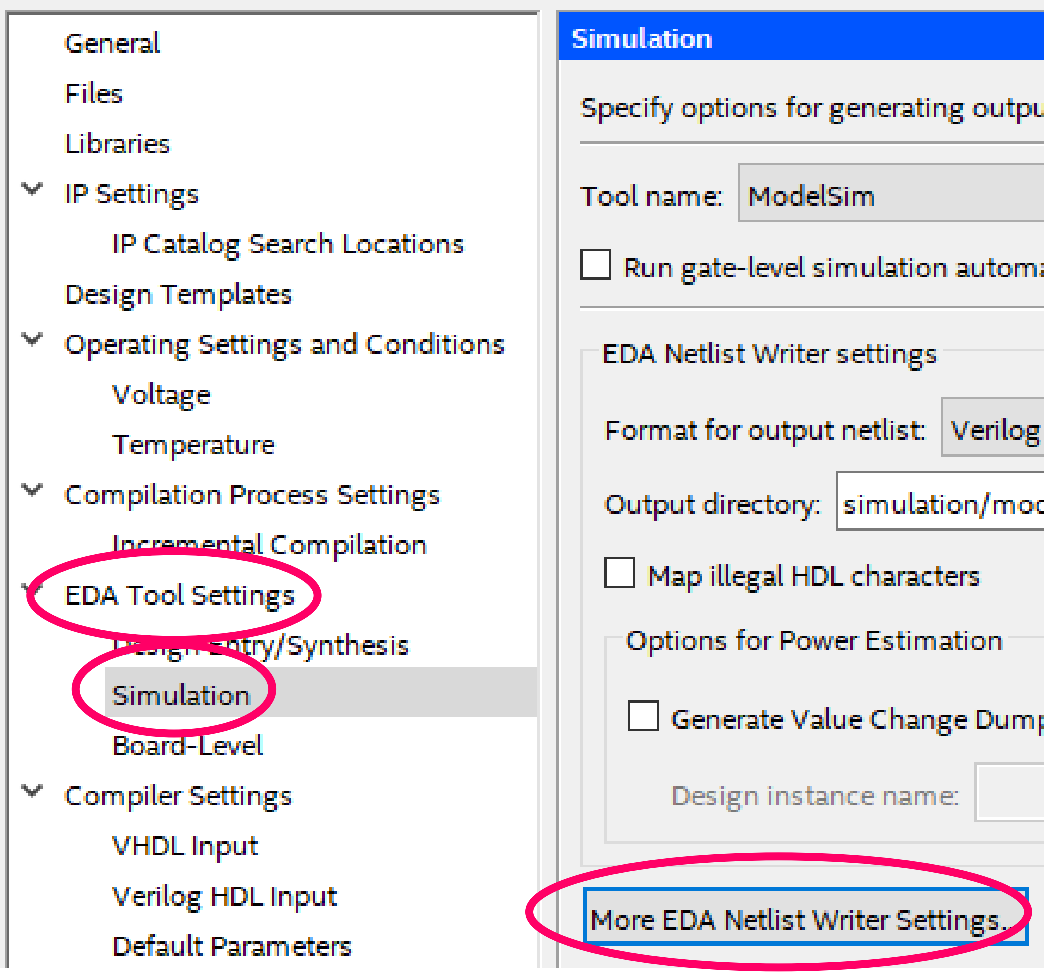
EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software

EDA tools:

Tool Type	Tool Name	Format(s)
Design Entry/Synth...	<None>	<None>
Simulation	ModelSim	Verilog HDL
Board-Level	Timing	<None>
	Symbol	<None>
	Signal Integrity	<None>
	Boundary Scan	<None>

Check Functional Simulation Netlist (1/2)



Specify options for generating outpu

Tool name: ModelSim

☐ Run gate-level simulation automa

EDA Netlist Writer settings

Format for output netlist: Verilog

Output directory: simulation/moc

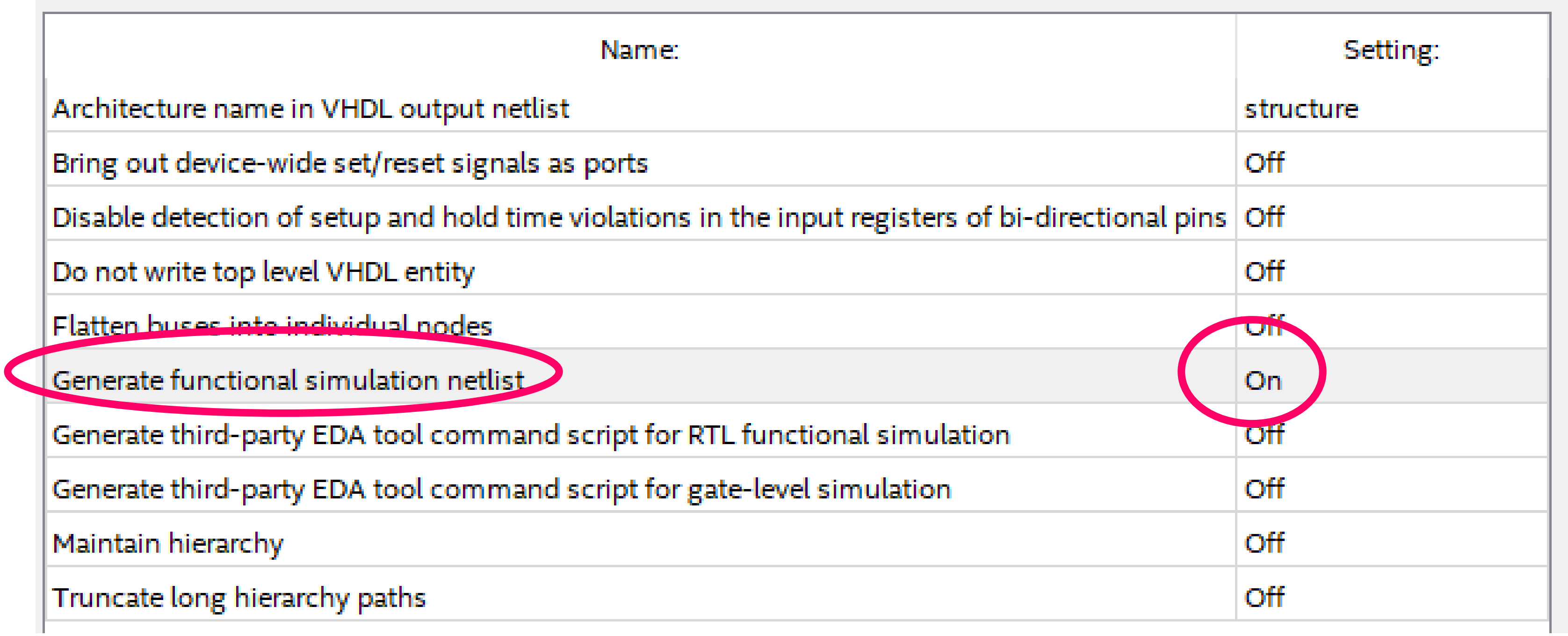
☐ Map illegal HDL characters

Options for Power Estimation

☐ Generate Value Change Dump

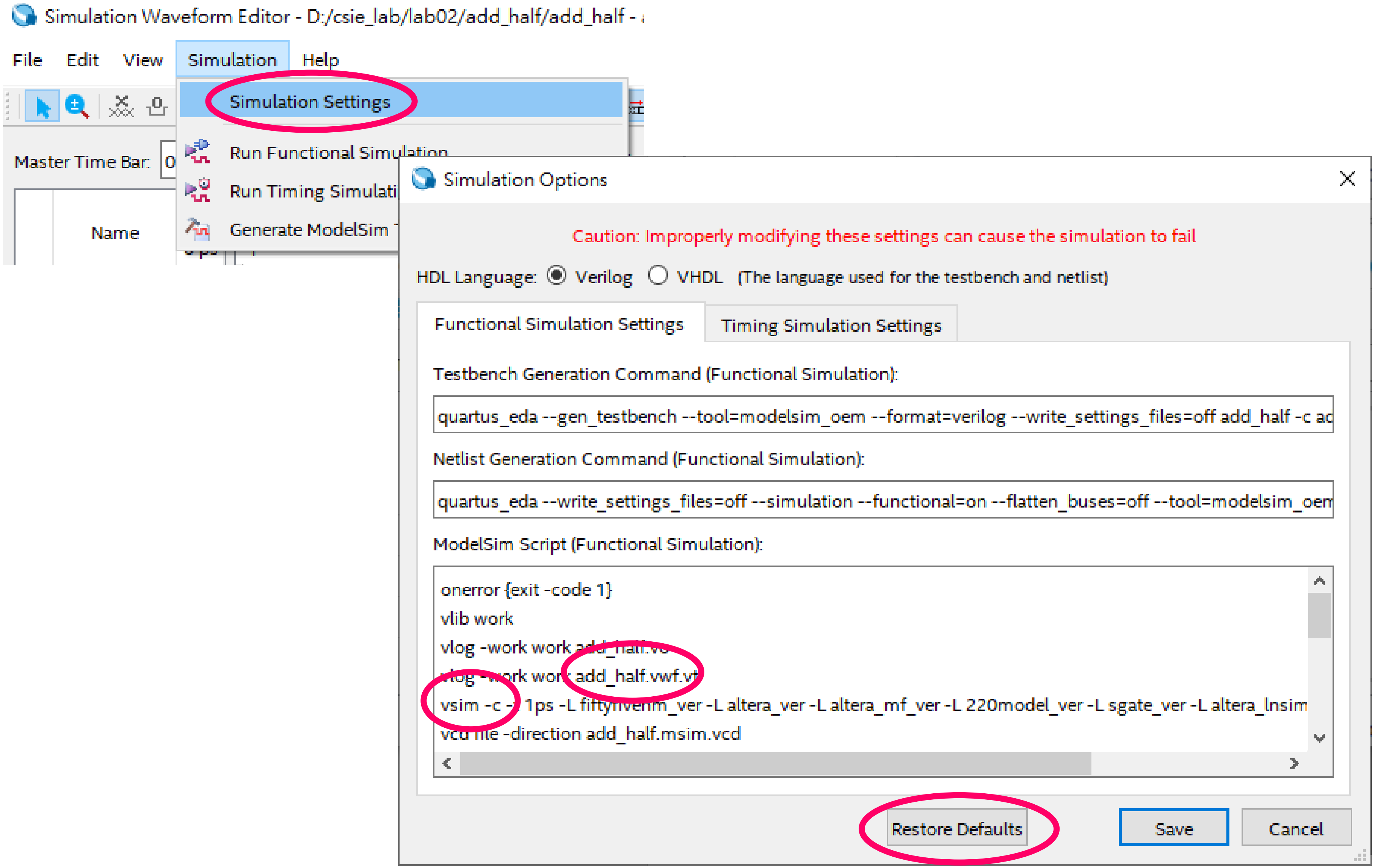
Design instance name:

Check Functional Simulation Netlist (2/2)



Name:	Setting:
Architecture name in VHDL output netlist	structure
Bring out device-wide set/reset signals as ports	Off
Disable detection of setup and hold time violations in the input registers of bi-directional pins	Off
Do not write top level VHDL entity	Off
Flatten buses into individual nodes	Off
Generate functional simulation netlist	On
Generate third-party EDA tool command script for RTL functional simulation	Off
Generate third-party EDA tool command script for gate-level simulation	Off
Maintain hierarchy	Off
Truncate long hierarchy paths	Off

Modify ModelSim Script



Simulation Waveform Editor - D:/csie_lab/lab02/add_half/add_half -
File
Edit
View
Simulation
Help
Simulation Settings
Run Functional Simulation
Run Timing Simulati
Generate ModelSim T
Master Time Bar:
Name
Simulation Options
Functional Simulation Settings
Timing Simulation Settings
Restore Defaults
Save
Cancel

Caution: Improperly modifying these settings can cause the simulation to fail

HDL Language: ● Verilog ○ VHDL (The language used for the testbench and netlist)

Testbench Generation Command (Functional Simulation):

```
quartus_eda --gen_testbench --tool=modelsim_oem --format=verilog --write_settings_files=off add_half -c ad
```

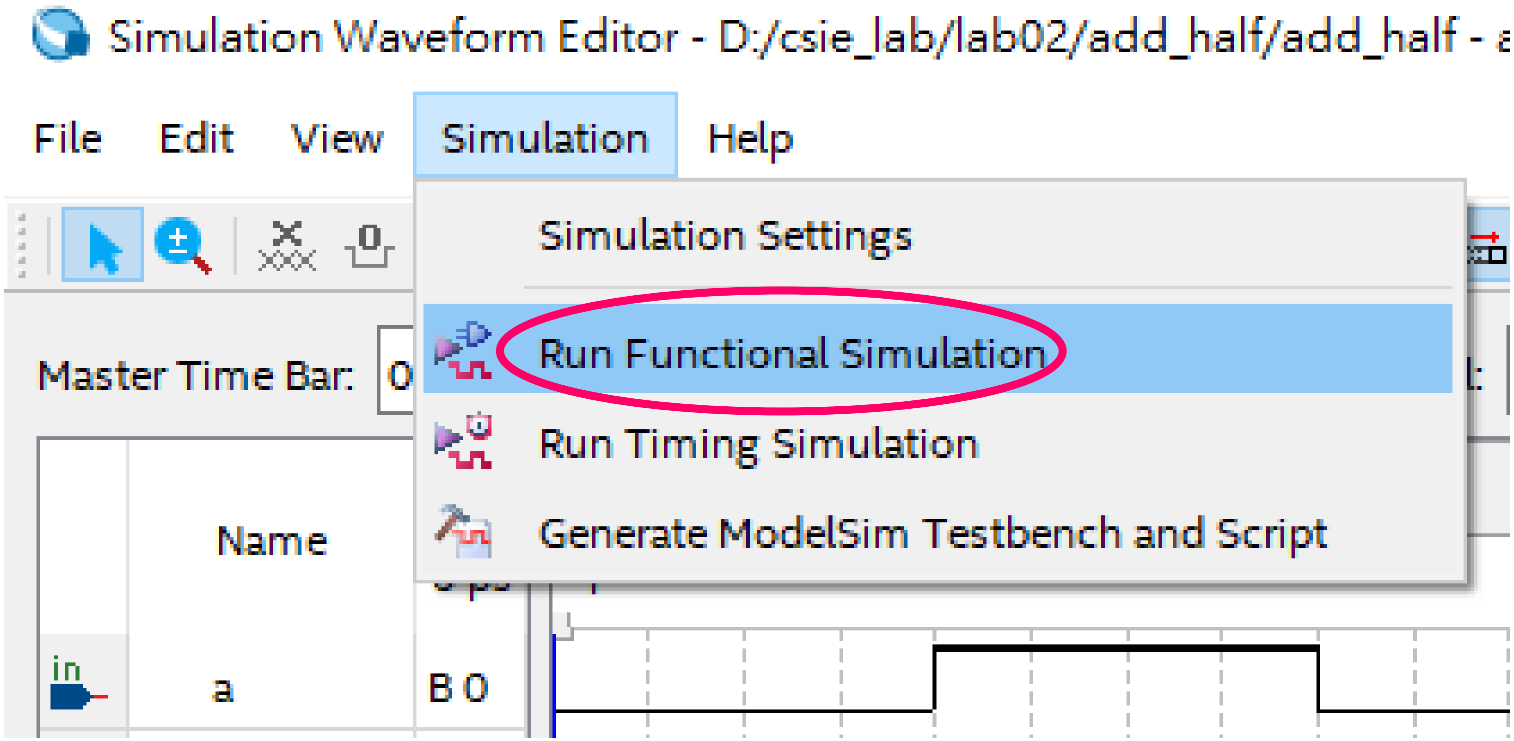
Netlist Generation Command (Functional Simulation):

```
quartus_eda --write_settings_files=off --simulation --functional=on --flatten_buses=off --tool=modelsim_oem
```

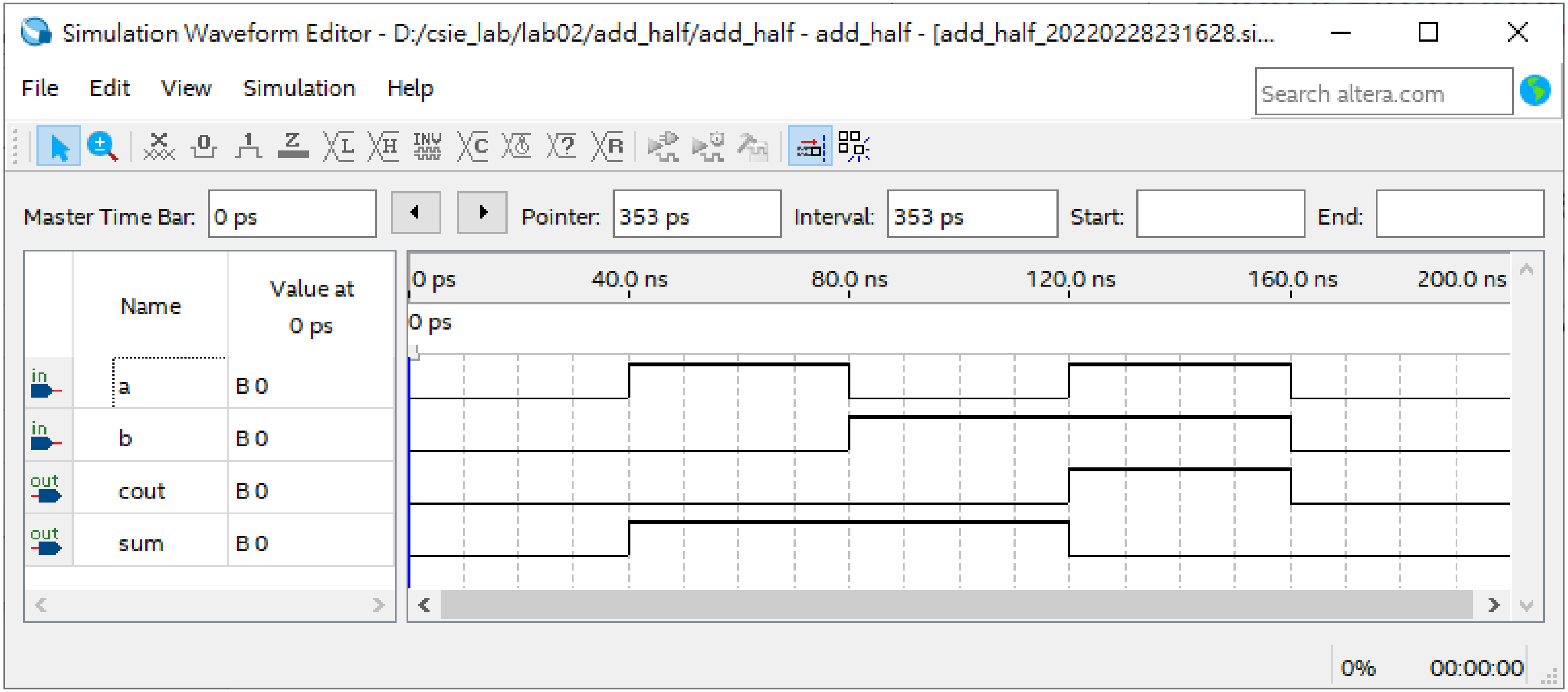
ModelSim Script (Functional Simulation):

```
onerror {exit -code 1}
vlib work
vlog -work work add_half.vo
vlog -work work add_half.vwf.vt
vsim -c -t 1ps -L fiftyfivenm_ver -L altera_ver -L altera_mf_ver -L 220model_ver -L sgate_ver -L altera_lnsim
vcd file -direction add_half.msim.vcd
```

Run Functional Simulation


Simulation Waveform Editor - D:/csie_lab/lab02/add_half/add_half - a
File
Edit
View
Simulation
Help
Simulation Settings
Run Functional Simulation
Run Timing Simulation
Generate ModelSim Testbench and Script
Master Time Bar:
0
Name
in
a
B 0

Functional Simulation Result



Simulation Waveform Editor - D:/csie_lab/lab02/add_half/add_half - add_half - [add_half_20220228231628.si...

Master Time Bar: 0 ps

Pointer: 353 ps

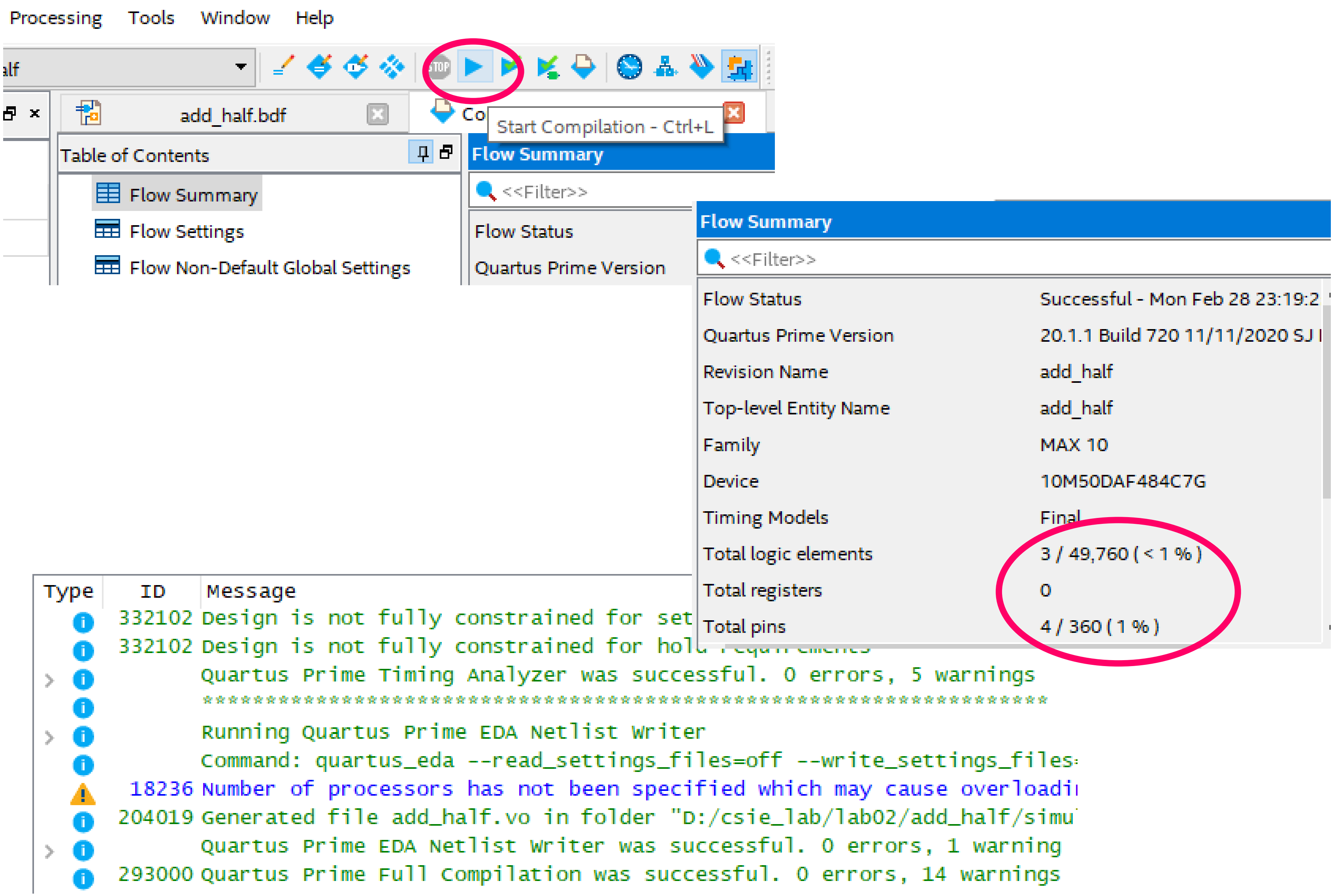
Interval: 353 ps

Start:

End:

Name	Value at 0 ps
a	B 0
b	B 0
cout	B 0
sum	B 0

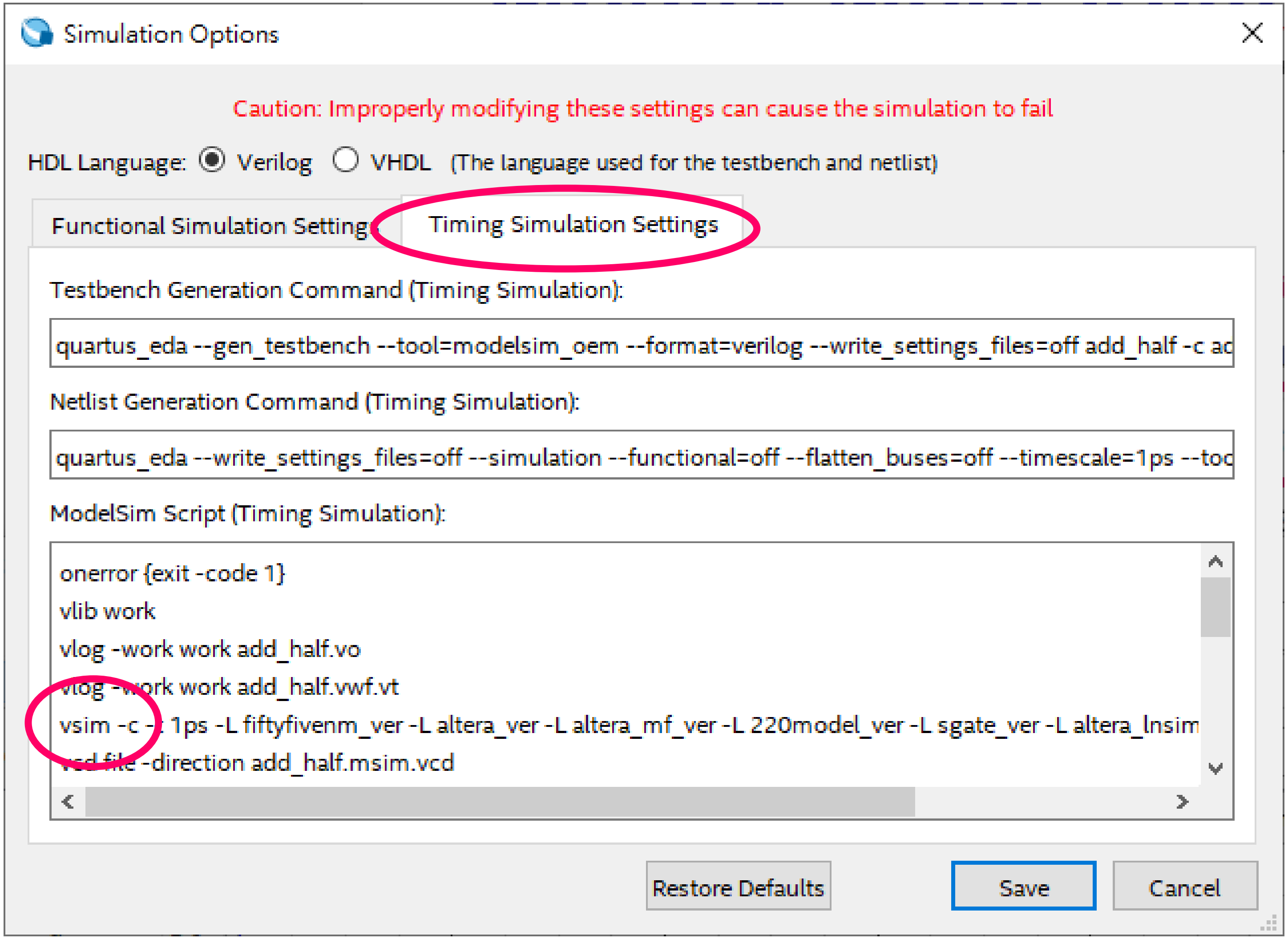
Perform Advanced Compilation for Timing Simulation



Flow Status	Successful - Mon Feb 28 23:19:2
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ I
Revision Name	add_half
Top-level Entity Name	add_half
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	3 / 49,760 (< 1 %)
Total registers	0
Total pins	4 / 360 (1 %)

```
Type  ID     Message
      332102 Design is not fully constrained for set
      332102 Design is not fully constrained for hold requirements
             Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
             ********************************************************************
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=
       18236 Number of processors has not been specified which may cause overloadi
      204019 Generated file add_half.vo in folder "D:/csie_lab/lab02/add_half/simu
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
      293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
```

Modify ModelSim Script



Caution: Improperly modifying these settings can cause the simulation to fail

HDL Language: ● Verilog ○ VHDL (The language used for the testbench and netlist)

Testbench Generation Command (Timing Simulation):

```
quartus_eda --gen_testbench --tool=modelsim_oem --format=verilog --write_settings_files=off add_half -c ac
```

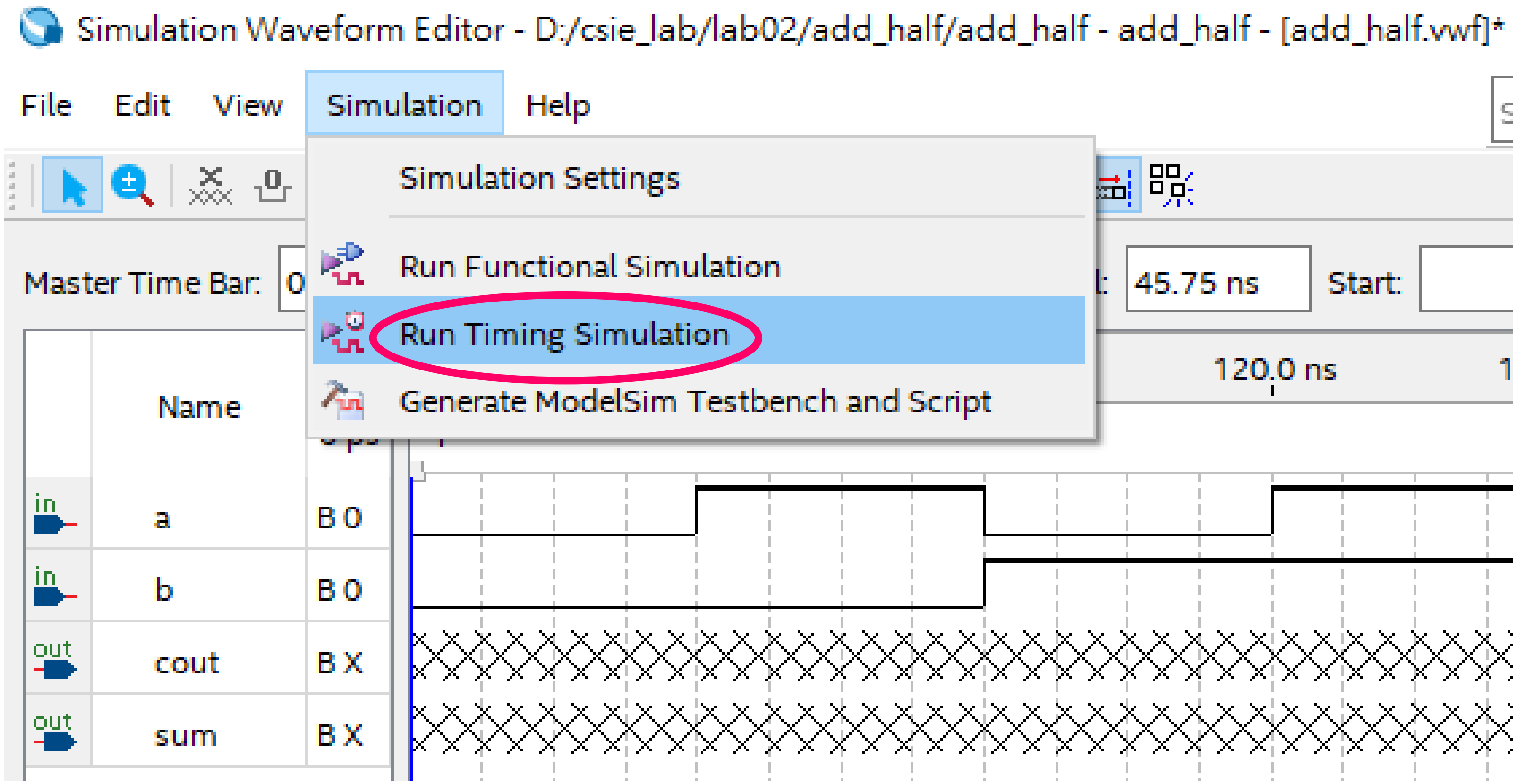
Netlist Generation Command (Timing Simulation):

```
quartus_eda --write_settings_files=off --simulation --functional=off --flatten_buses=off --timescale=1ps --toc
```

ModelSim Script (Timing Simulation):

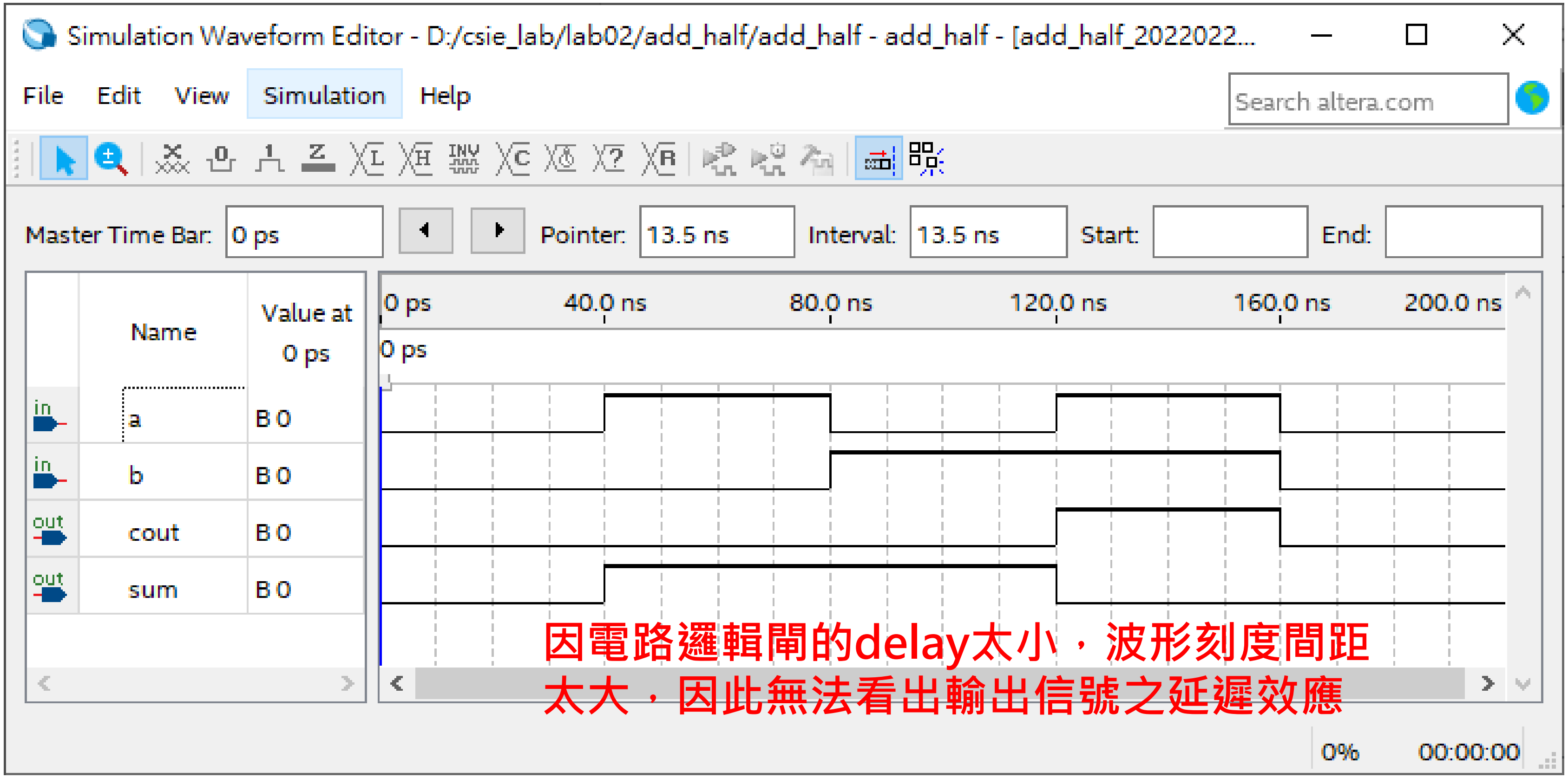
```
onerror {exit -code 1}
vlib work
vlog -work work add_half.vo
vlog -work work add_half.vwf.vt
vsim -c -t 1ps -L fiftyfivenm_ver -L altera_ver -L altera_mf_ver -L 220model_ver -L sgate_ver -L altera_lnsim
vcd file -direction add_half.msim.vcd
```

Run Timing Simulation



Simulation Waveform Editor - D:/csie_lab/lab02/add_half/add_half - add_half - [add_half.vwf]*

Timing Simulation Result



Simulation Waveform Editor - D:/csie_lab/lab02/add_half/add_half - add_half - [add_half_2022022...

Master Time Bar: 0 ps

Pointer: 13.5 ns

Interval: 13.5 ns

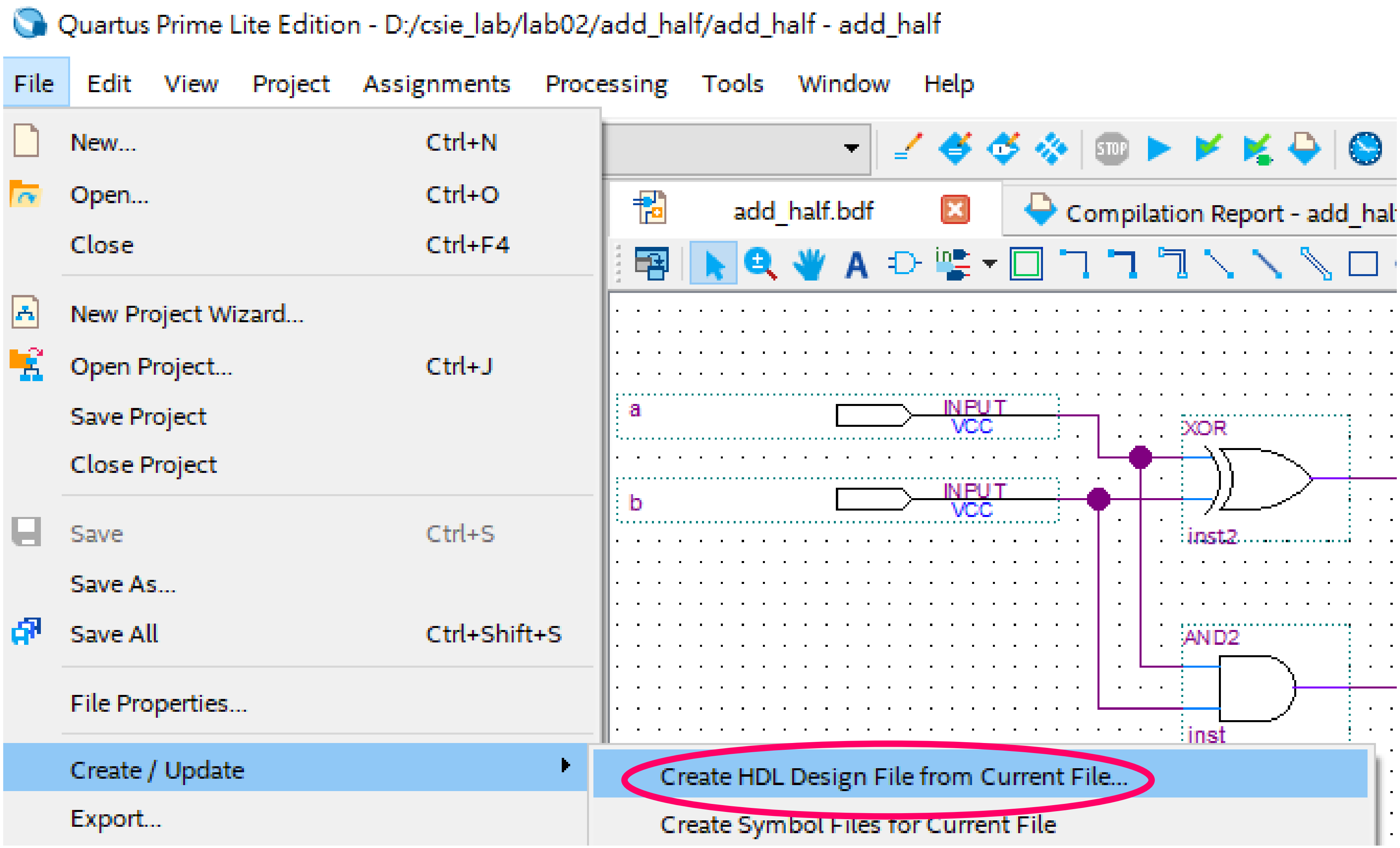
Start:

End:

	Name	Value at 0 ps
in	a	B 0
in	b	B 0
out	cout	B 0
out	sum	B 0

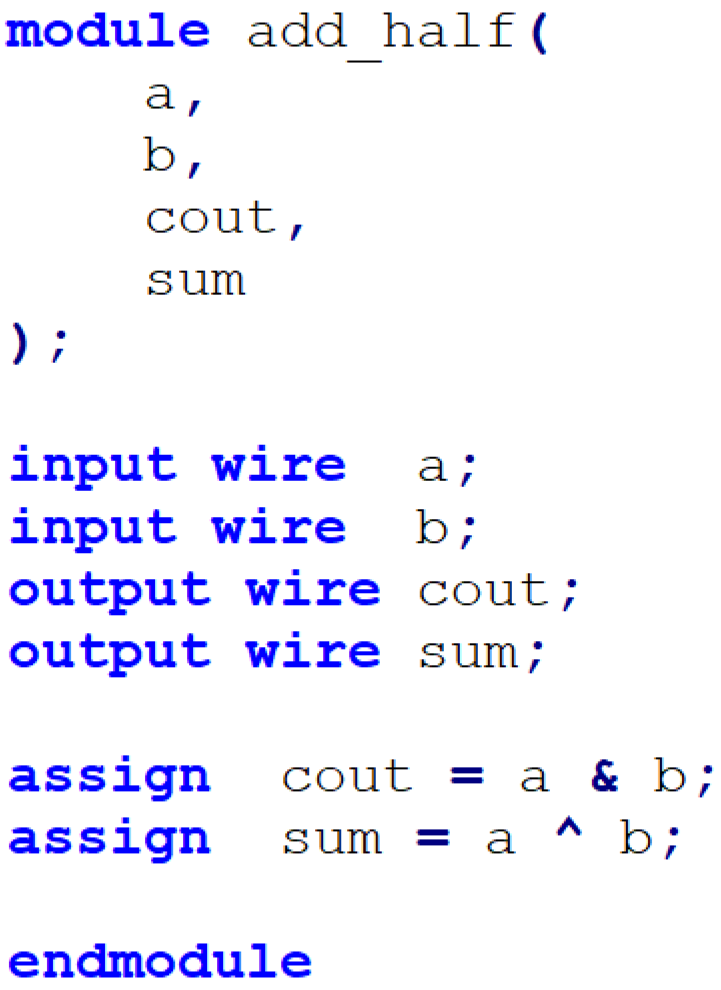
因電路邏輯閘的delay太小，波形刻度間距太大，因此無法看出輸出信號之延遲效應

Create the HDL (Verilog) File



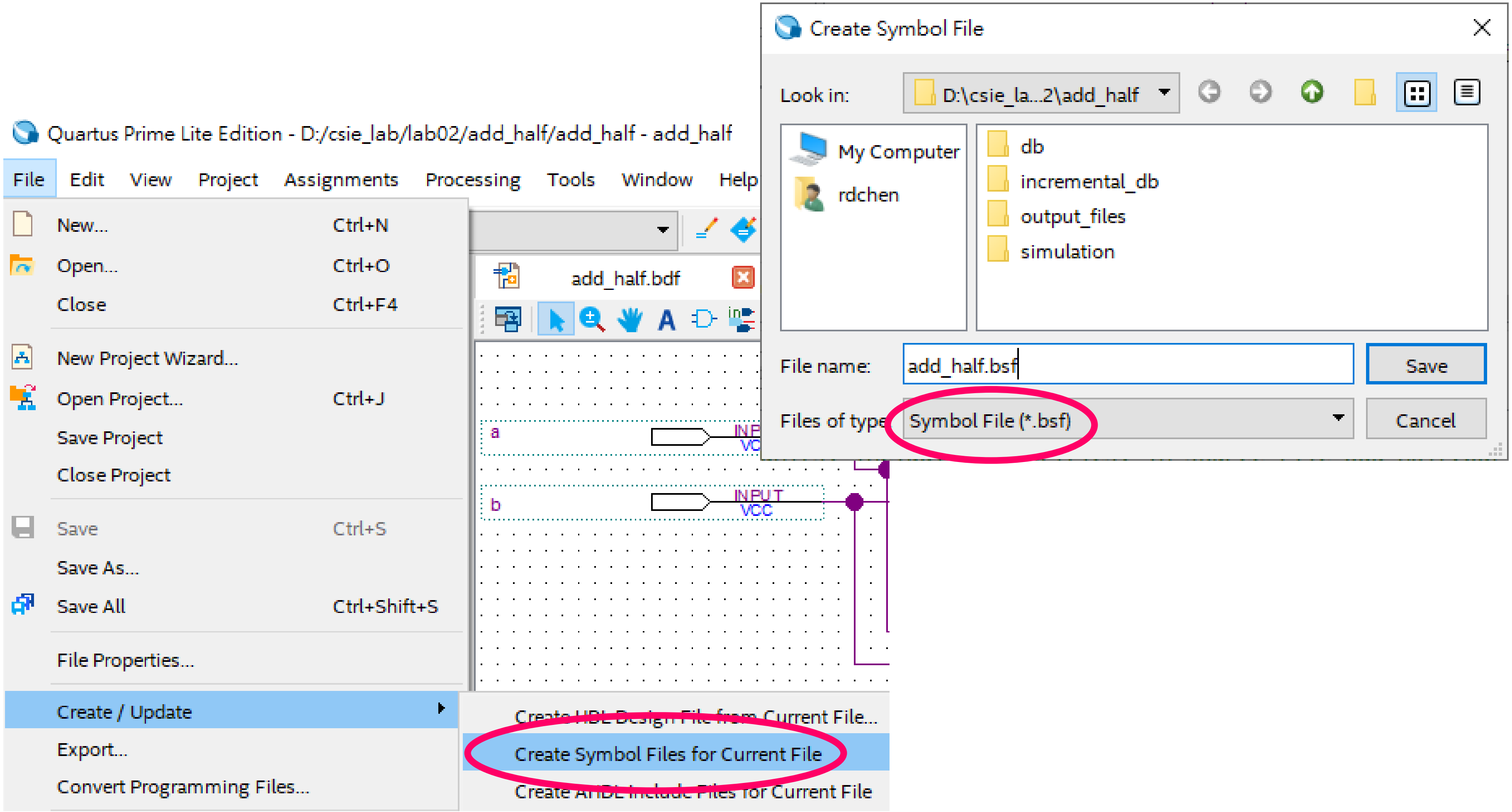
Quartus Prime Lite Edition - D:/csie_lab/lab02/add_half/add_half - add_half

Content in add_half.v (Generated by Tool)

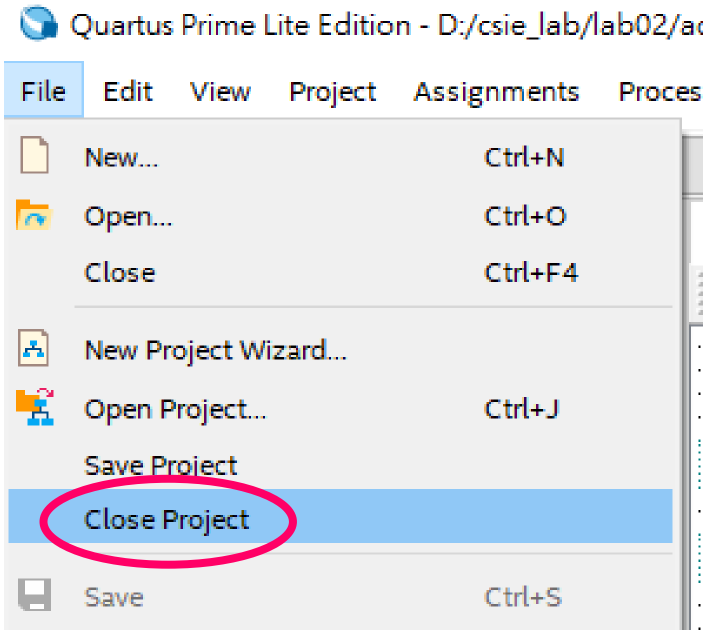


```
module add_half(
    a,
    b,
    cout,
    sum
);

input wire  a;
input wire  b;
output wire cout;
output wire sum;

assign  cout = a & b;
assign  sum = a ^ b;

endmodule
```

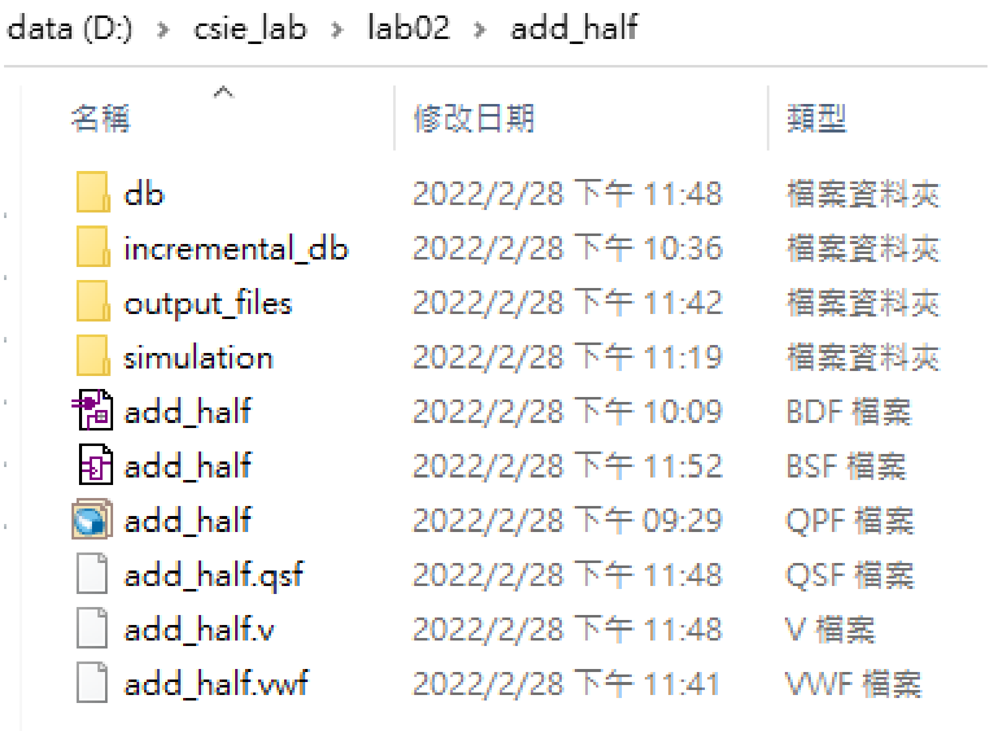
Create the Symbol File



Close the Current Project

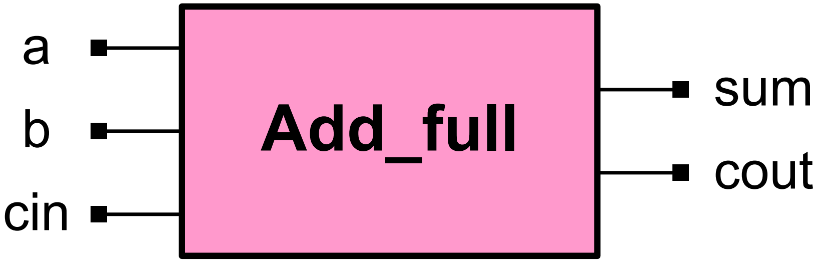


All add_half files


data (D:) › csie_lab › lab02 › add_half

名稱	修改日期	類型
db	2022/2/28 下午 11:48	檔案資料夾
incremental_db	2022/2/28 下午 10:36	檔案資料夾
output_files	2022/2/28 下午 11:42	檔案資料夾
simulation	2022/2/28 下午 11:19	檔案資料夾
add_half	2022/2/28 下午 10:09	BDF 檔案
add_half	2022/2/28 下午 11:52	BSF 檔案
add_half	2022/2/28 下午 09:29	QPF 檔案
add_half.qsf	2022/2/28 下午 11:48	QSF 檔案
add_half.v	2022/2/28 下午 11:48	V 檔案
add_half.vwf	2022/2/28 下午 11:41	VWF 檔案

Design Example: Full Adder (1/2)



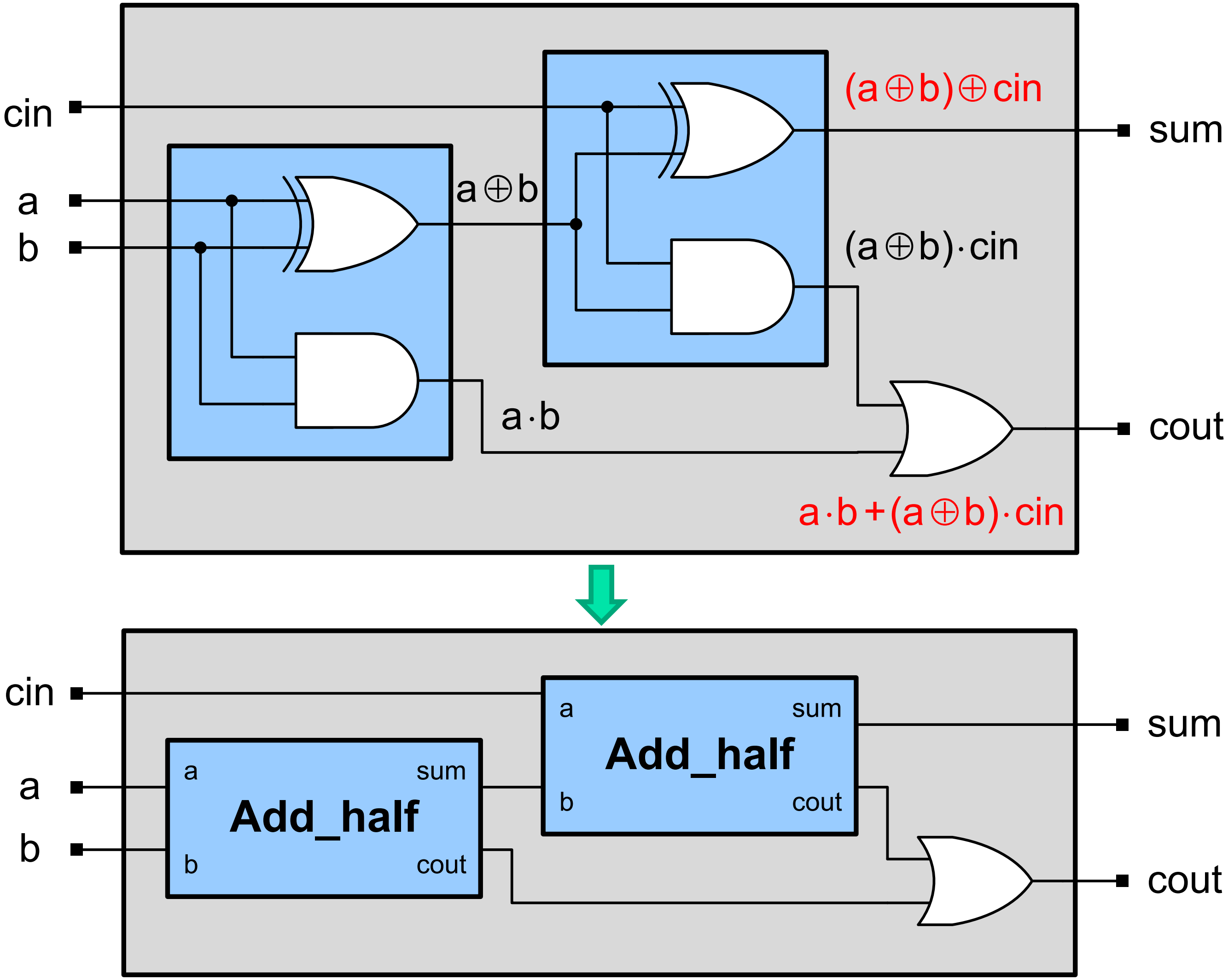
ab\cin	0	1
00	0	1
01	1	0
11	0	1
10	1	0

ab\cin	0	1
00	0	0
01	0	1
11	1	1
10	0	1

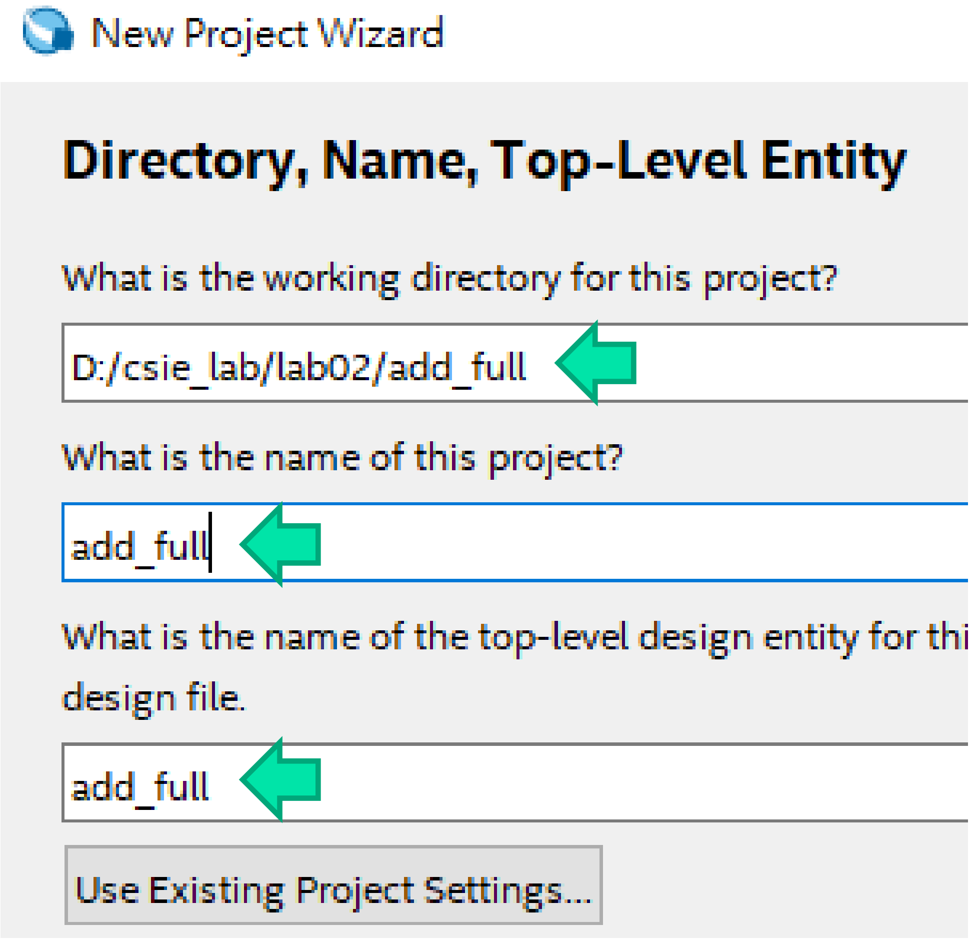
$sum=(a\oplus b)\oplus cin$

$cout=a\cdot b+(a\oplus b)\cdot cin$

Design Example: Full Adder (2/2)



Create a New Project - add_full



New Project Wizard

Directory, Name, Top-Level Entity

What is the working directory for this project?

D:/csie_lab/lab02/add_full

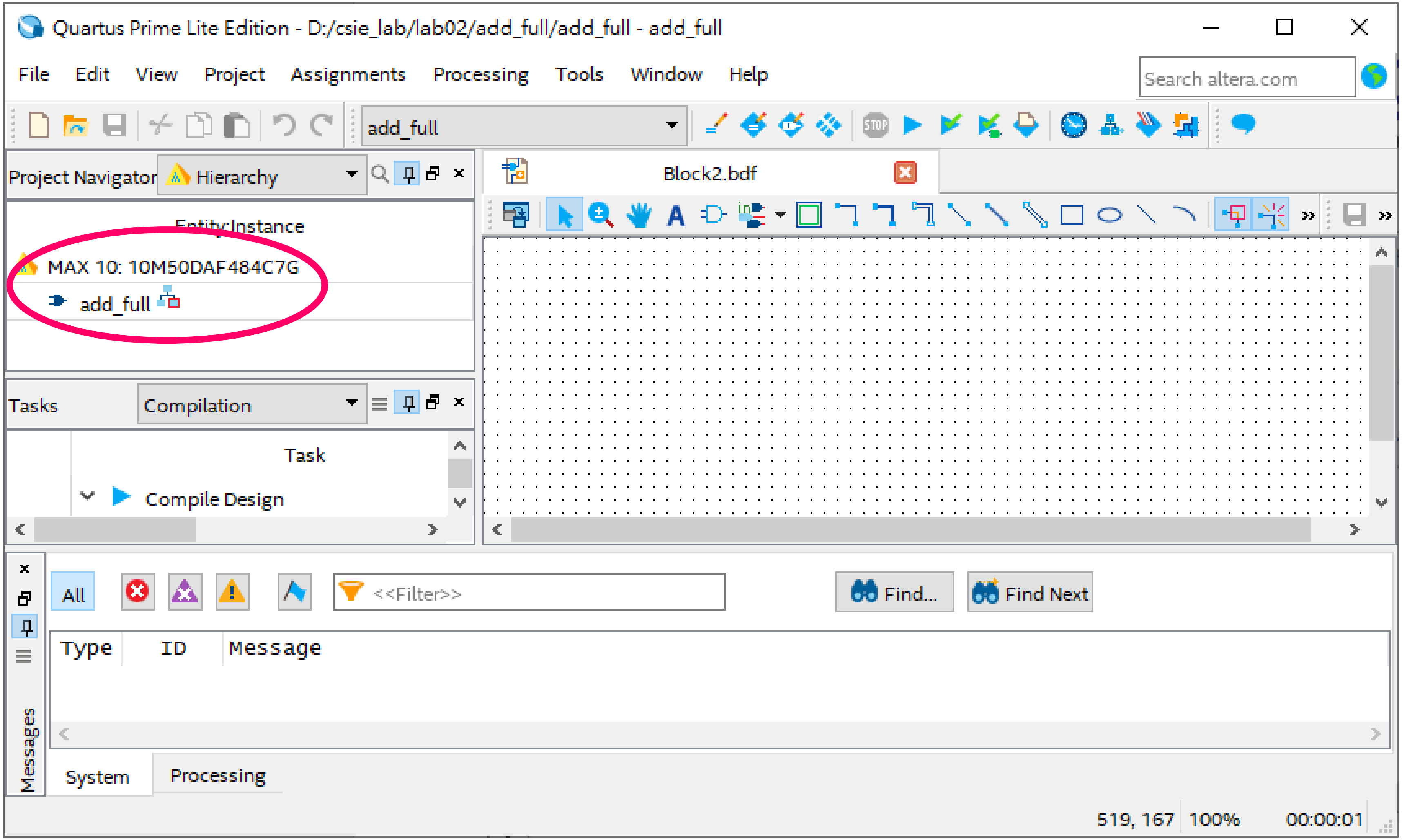
What is the name of this project?

add_full

What is the name of the top-level design entity for thi
design file.

add_full

Create a Schematic Design for add_full



Quartus Prime Lite Edition - D:/csie_lab/lab02/add_full/add_full - add_full

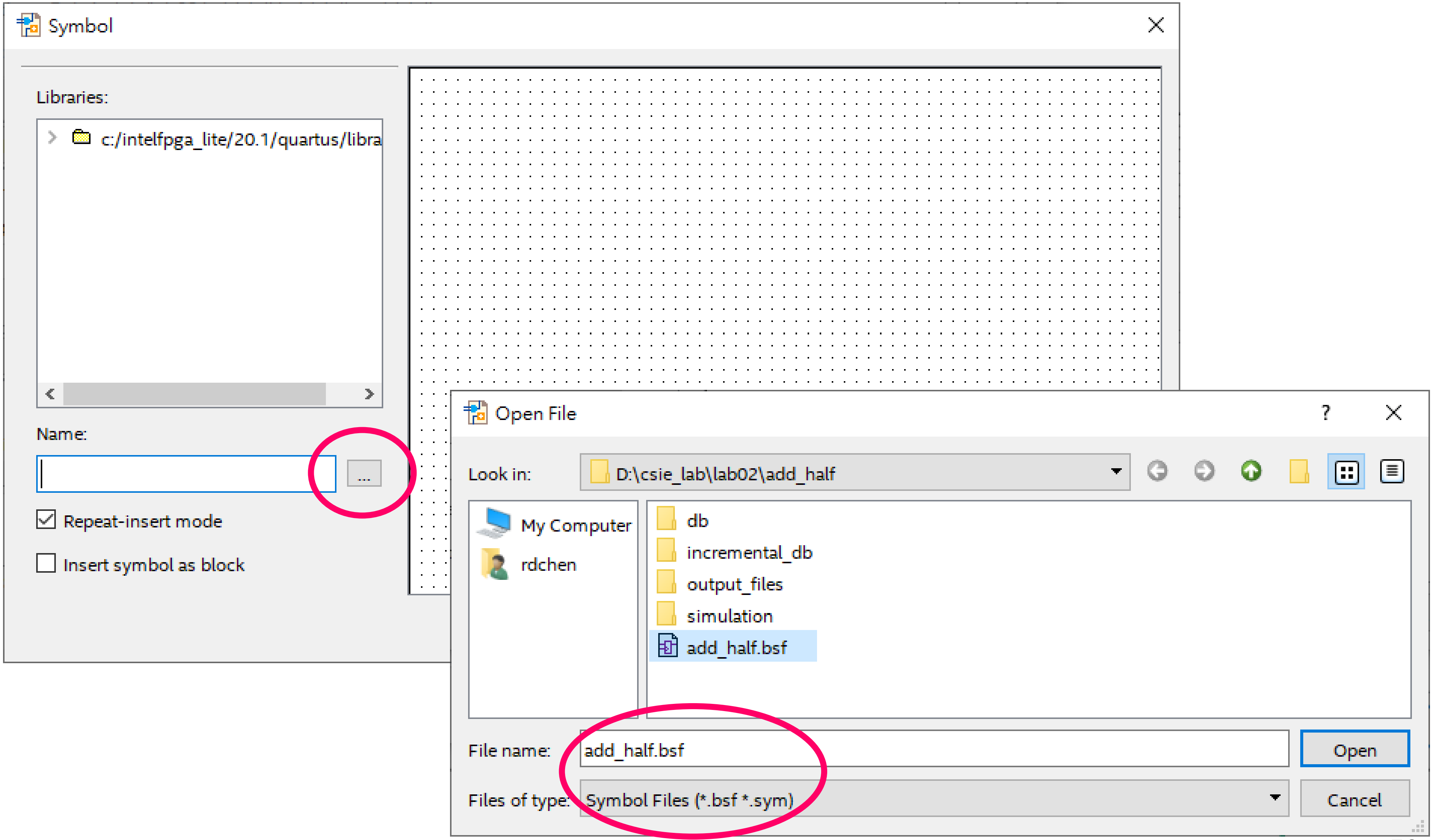
Entity:Instance

MAX 10: 10M50DAF484C7G

add_full

519, 167 100% 00:00:01

Select and Import a Half Adder



Symbol

Libraries:

c:/intelfpga_lite/20.1/quartus/libra

Name:

☑ Repeat-insert mode

□ Insert symbol as block

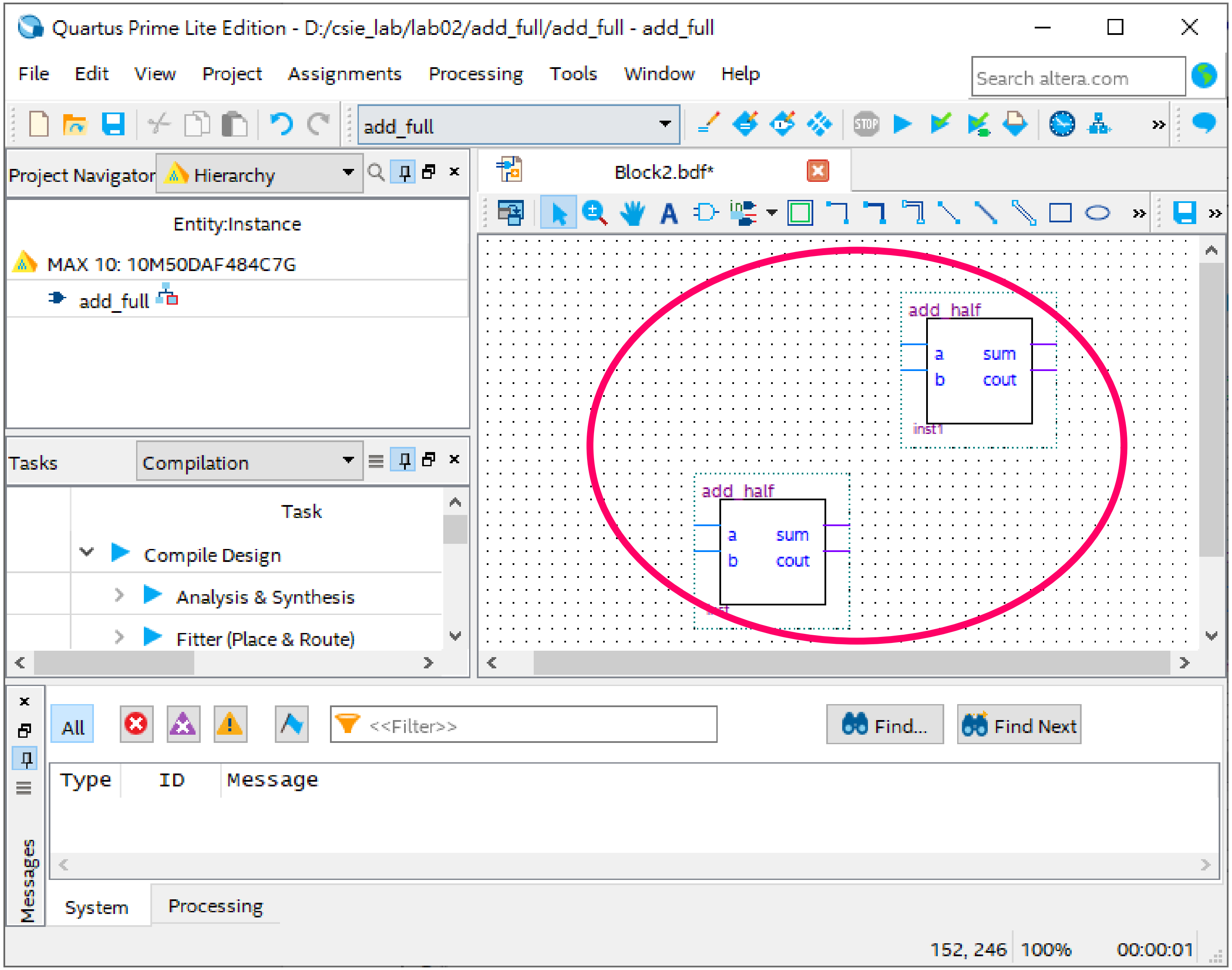
Open File

Look in: D:\csie_lab\lab02\add_half

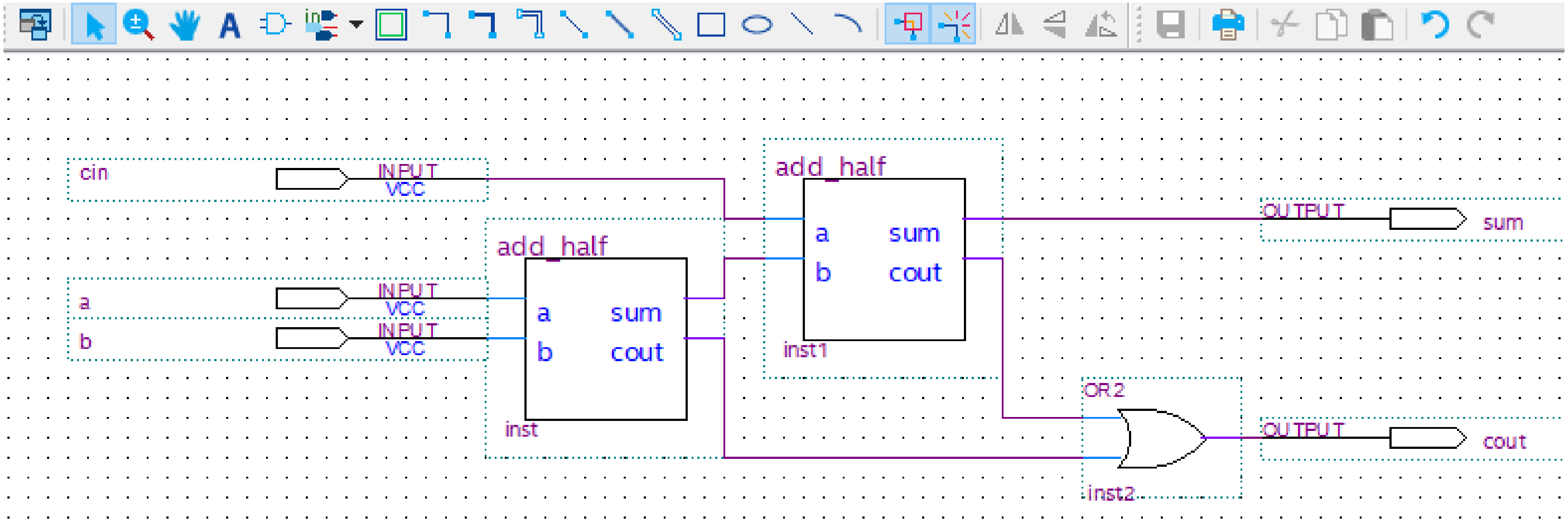
File name: add_half.bsf

Files of type: Symbol Files (*.bsf *.sym)

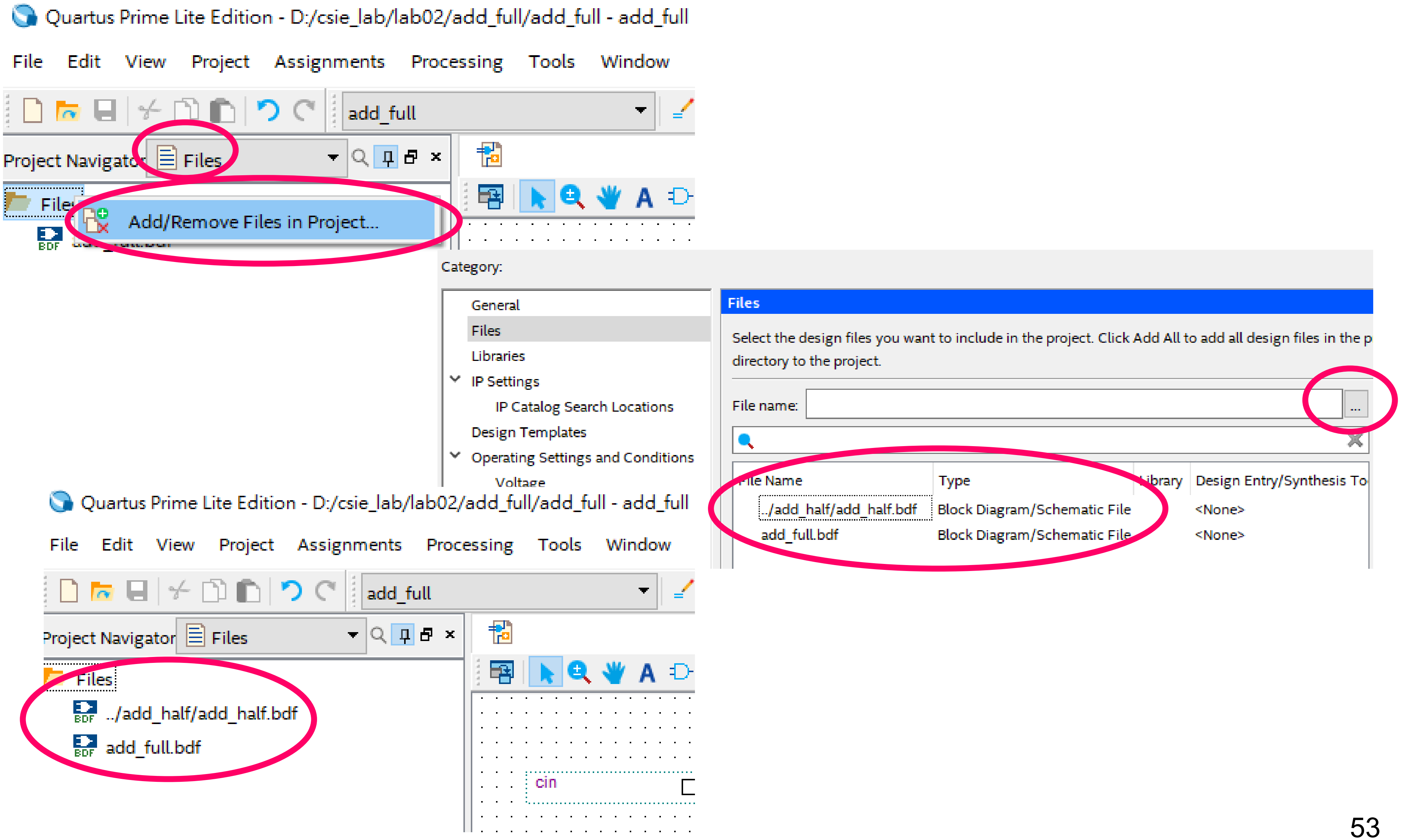
Two Half Adders are Imported



Import OR2 Gate and I/O Pins



Add the add_half Schematic File



Quartus Prime Lite Edition - D:/csie_lab/lab02/add_full/add_full - add_full
File
Edit
View
Project
Assignments
Processing
Tools
Window
add_full
Project Navigator
Files
Add/Remove Files in Project...
Category:
General
Files
Libraries
IP Settings
IP Catalog Search Locations
Design Templates
Operating Settings and Conditions
Voltage
File name:
...
cin

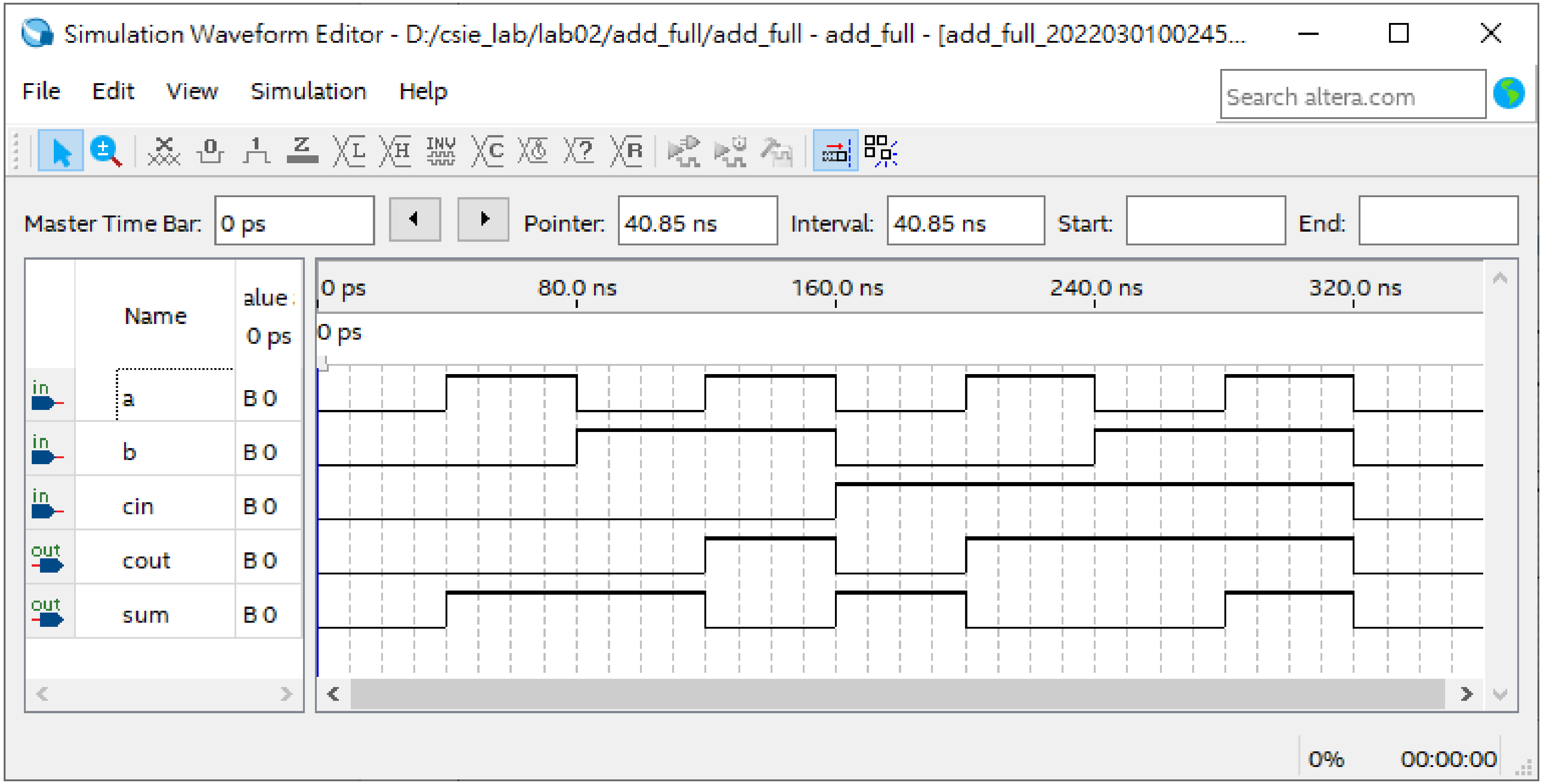
Files

Select the design files you want to include in the project. Click Add All to add all design files in the p
directory to the project.

File Name	Type	Library	Design Entry/Synthesis To
../add_half/add_half.bdf	Block Diagram/Schematic File		<None>
add_full.bdf	Block Diagram/Schematic File		<None>

Files
- ../add_half/add_half.bdf
- add_full.bdf

Functional Simulation Result



Simulation Waveform Editor - D:/csie_lab/lab02/add_full/add_full - add_full - [add_full_2022030100245...

Master Time Bar: 0 ps

Pointer: 40.85 ns

Interval: 40.85 ns

Start:

End:

	Name	alue 0 ps
in	a	B 0
in	b	B 0
in	cin	B 0
out	cout	B 0
out	sum	B 0

Content in add_full.v (Generated by Tool)

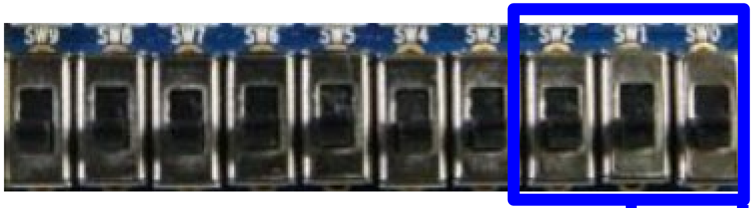
```
module add_full(
    a,
    b,
    cin,
    cout,
    sum
);

input wire  a;
input wire  b;
input wire  cin;
output wire cout;
output wire sum;

wire    SYNTHESIZED_WIRE_0;
wire    SYNTHESIZED_WIRE_1;
wire    SYNTHESIZED_WIRE_2;
```

```
add_half    b2v_inst(
    .a(a),
    .b(b),
    .cout(SYNTHESIZED_WIRE_2),
    .sum(SYNTHESIZED_WIRE_0));


add_half    b2v_inst1(
    .a(SYNTHESIZED_WIRE_0),
    .b(cin),
    .cout(SYNTHESIZED_WIRE_1),
    .sum(sum));

assign  cout = SYNTHESIZED_WIRE_1 | SYNTHESIZED_WIRE_2;


endmodule
```

Pin Assignments

Inputs

SW2 SW1 SW0

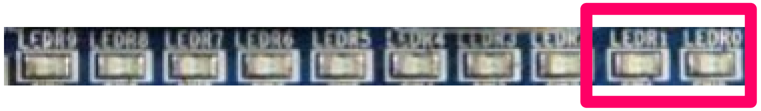


1
0

a b cin

Outputs

LED1 LED0

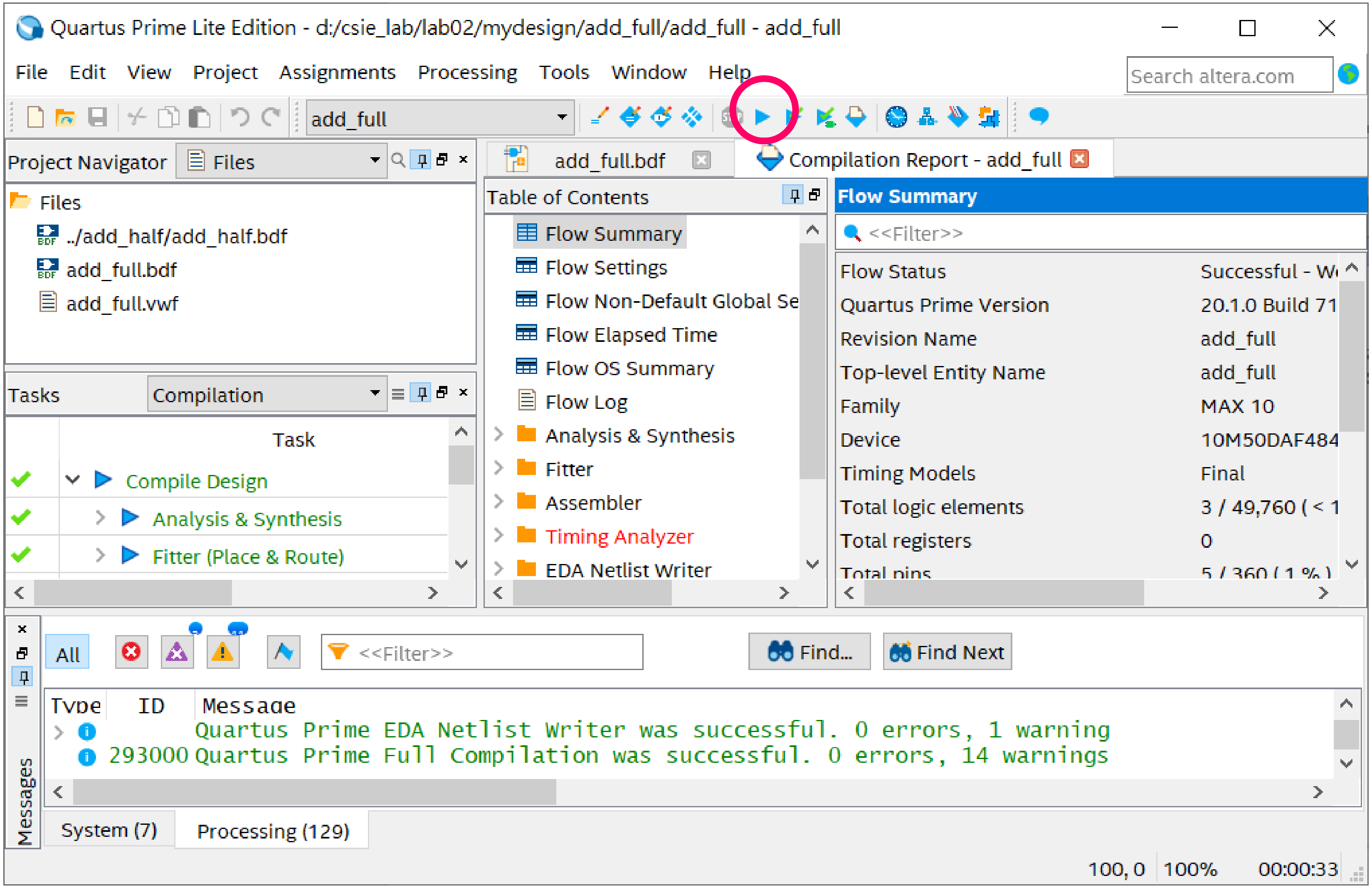


1: LED on
0: LED off

cout sum

{cout, sum} = a + b + cin

Start Compilation



Files
- ../add_half/add_half.bdf
- add_full.bdf
- add_full.vwf

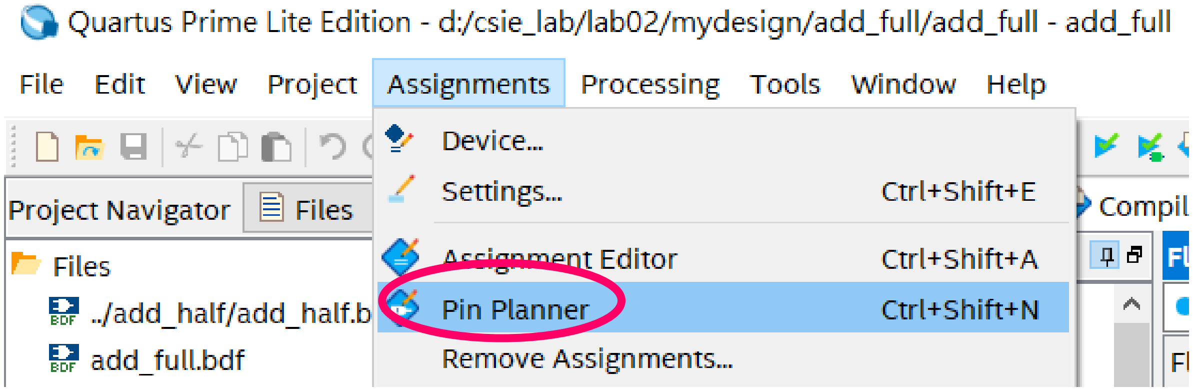
Tasks:
- ✓ Compile Design
- ✓ Analysis & Synthesis
- ✓ Fitter (Place & Route)

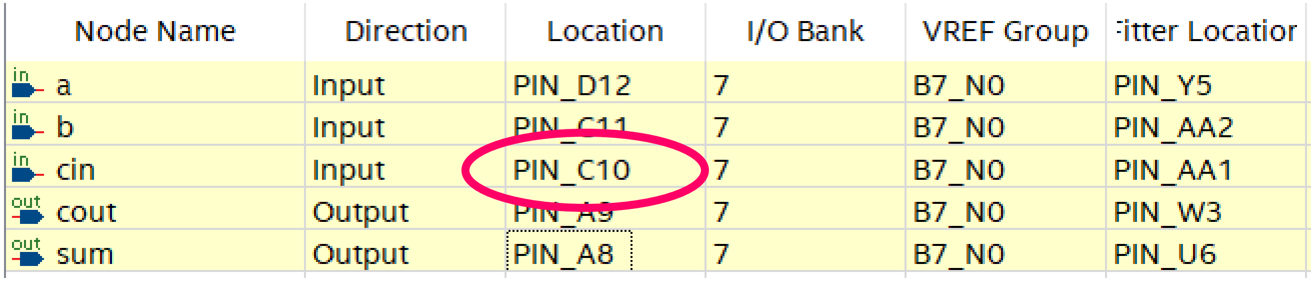
Table of Contents:
- Flow Summary
- Flow Settings
- Flow Non-Default Global Se
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- Timing Analyzer
- EDA Netlist Writer

Flow Summary	
Flow Status	Successful - W
Quartus Prime Version	20.1.0 Build 71
Revision Name	add_full
Top-level Entity Name	add_full
Family	MAX 10
Device	10M50DAF484
Timing Models	Final
Total logic elements	3 / 49,760 (< 1
Total registers	0
Total pins	5 / 360 (1 %)

```
Type  ID     Message
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
      293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
```

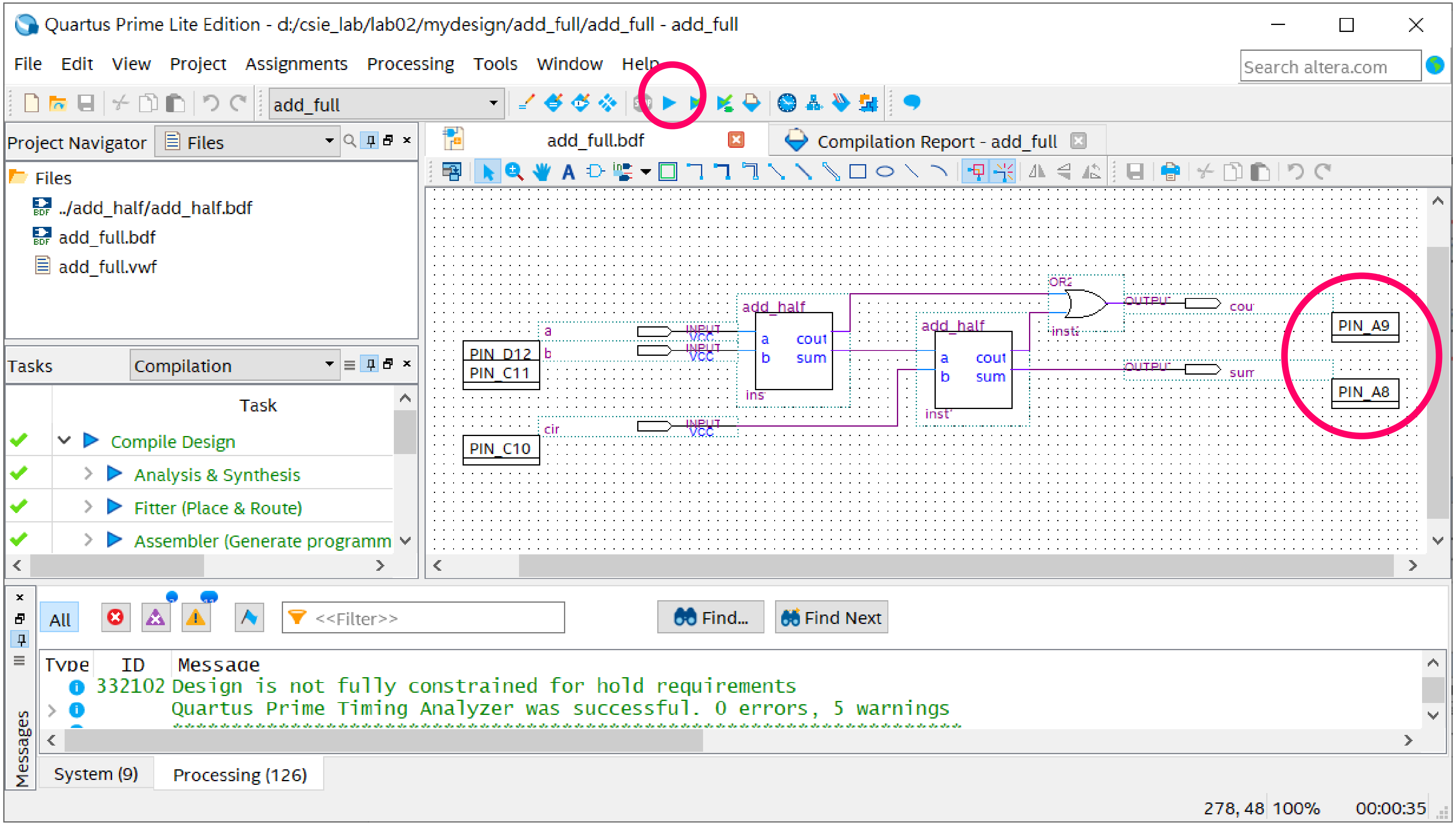
Make Pin Assignments





Node Name	Direction	Location	I/O Bank	VREF Group	itter Locatior
a	Input	PIN_D12	7	B7_N0	PIN_Y5
b	Input	PIN_C11	7	B7_N0	PIN_AA2
cin	Input	PIN_C10	7	B7_N0	PIN_AA1
cout	Output	PIN_A9	7	B7_N0	PIN_W3
sum	Output	PIN_A8	7	B7_N0	PIN_U6

Start Compilation



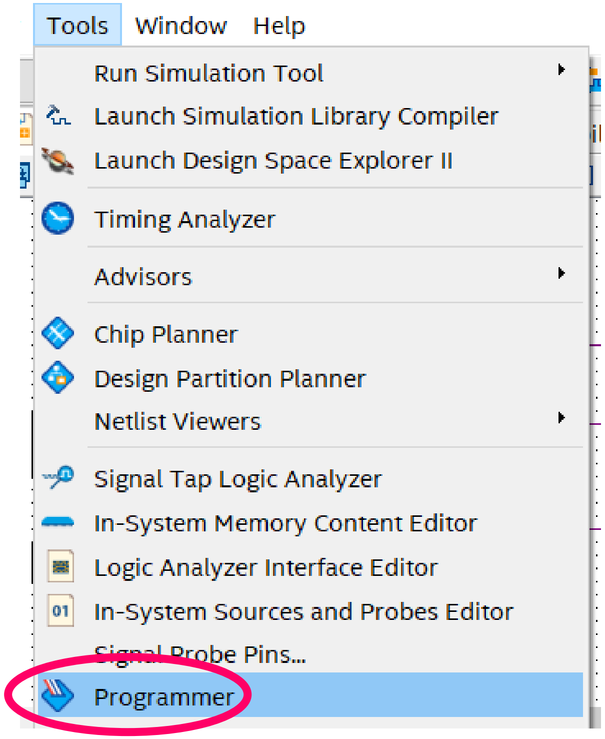
Files
- ../add_half/add_half.bdf
- add_full.bdf
- add_full.vwf

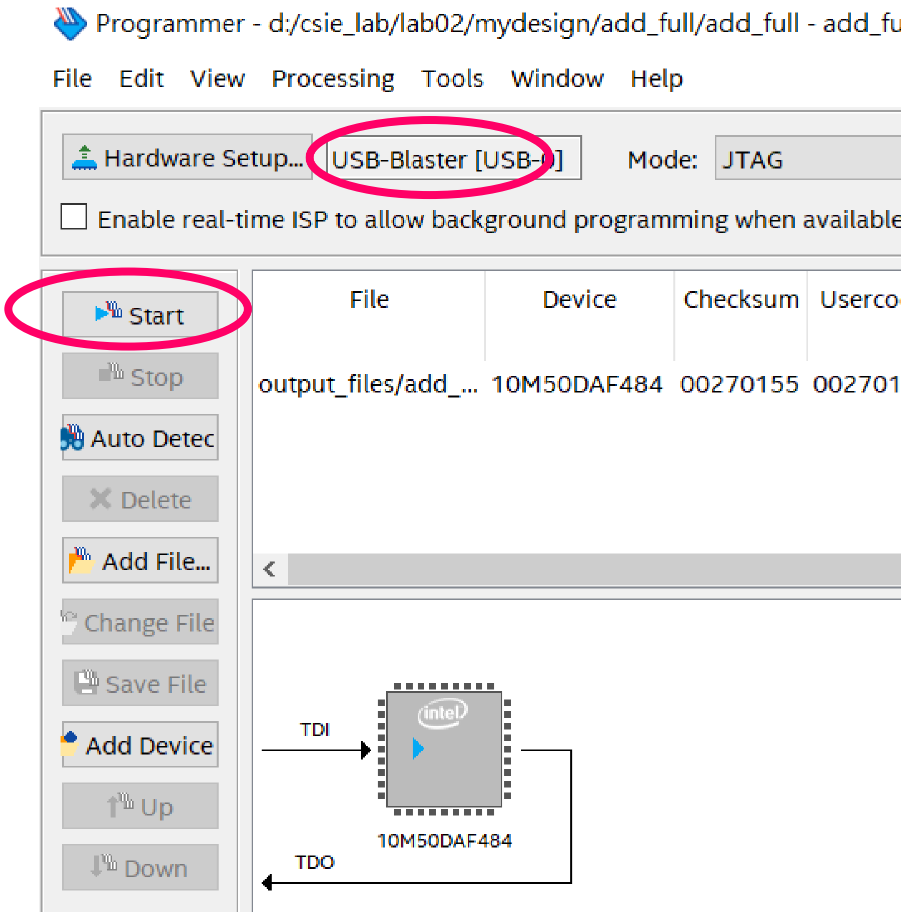
Tasks: Compilation

	Task
✓	Compile Design
✓	Analysis & Synthesis
✓	Fitter (Place & Route)
✓	Assembler (Generate programm

```
Type  ID     Message
  ⓘ   332102 Design is not fully constrained for hold requirements
> ⓘ          Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
```

Program into Device


Tools
Window
Help
Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer II
Timing Analyzer
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
Signal Tap Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
Signal Probe Pins...
Programmer


Programmer - d:/csie_lab/lab02/mydesign/add_full/add_full - add_fu

USB-Blaster [USB-0]

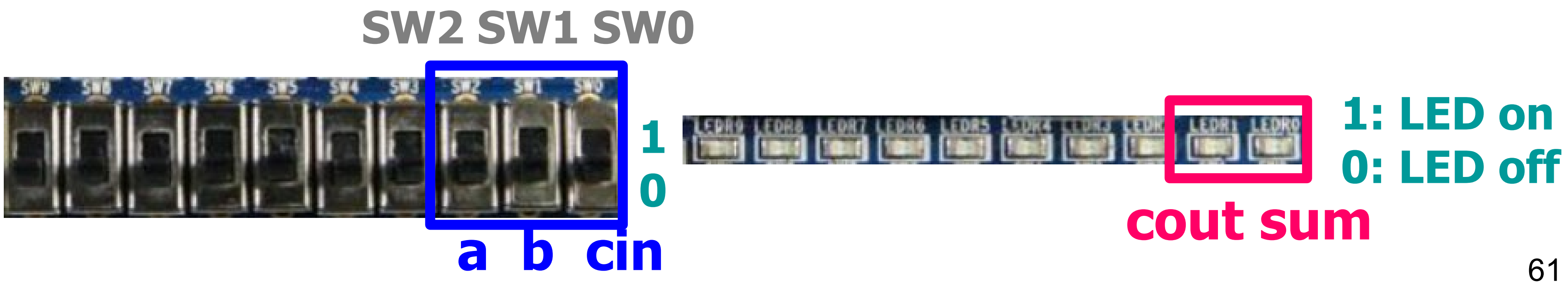
Mode: JTAG

□ Enable real-time ISP to allow background programming when available

File	Device	Checksum	Userco
output_files/add_...	10M50DAF484	00270155	002701

Verify Your Design

- sw2/sw1/sw0 : dn/dn/dn (0/0/0) => L1/L0: off/off (0/0)
- sw2/sw1/sw0 : dn/dn/**up** (0/0/1) => L1/L0: off/**on** (0/1)
- sw2/sw1/sw0 : dn/up/dn (0/1/0) => L1/L0: off/on (0/1)
- sw2/sw1/sw0 : dn/**up/up** (0/1/1) => L1/L0: **on**/off (1/0)
- sw2/sw1/sw0 : up/dn/dn (1/0/0) => L1/L0: off/on (0/1)
- sw2/sw1/sw0 : up/dn/up (1/0/1) => L1/L0: on/off (1/0)
- sw2/sw1/sw0 : up/up/dn (1/1/0) => L1/L0: on/off (1/0)
- sw2/sw1/sw0 : **up/up/up** (1/1/1) => L1/L0: **on/on** (1/1)



實驗報告

- 請老師or助教驗證**add_full**電路之模擬波形及實驗板之行為是否正確