Comparing the Performance of 4-bits Adders Topologies on Sub 32nm Bulk CMOS Technologies

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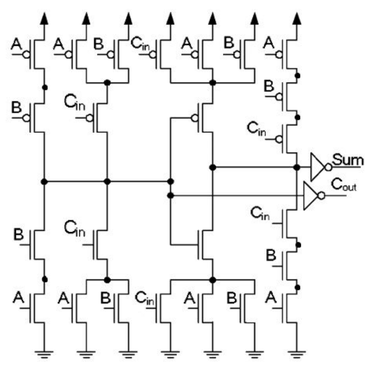
Introduction

Adders are very important circuits within combinational logic, serving as the basis for the implementation of several arithmetic functions. This work presents a comparative study on some models present in the literature on *n-bits* adders, from electrical simulations.

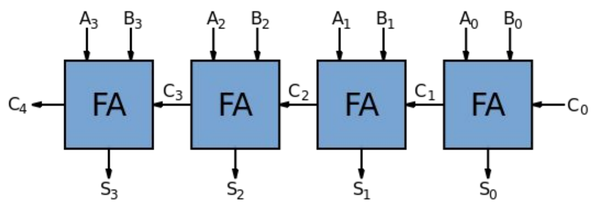
Methodology

- 4 architectures: Ripple-Carry, Carry-Lookahead, Carry-Select and Kogge-Stone Adder:
  - 4 bits;
  - Mirror CMOS FA.
- **16 and 32 nm CMOS technology (PTM)**;
- Electrical Simulation (Ngspice);
- Models will be verified and compared in delay and power consumption.

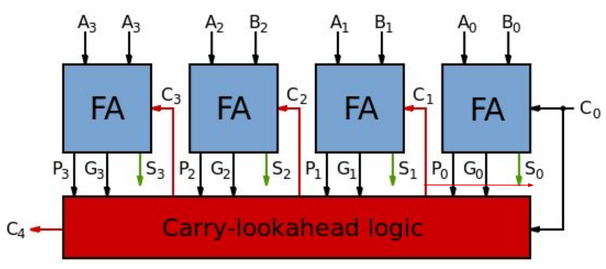
Mirror CMOS Full Adder



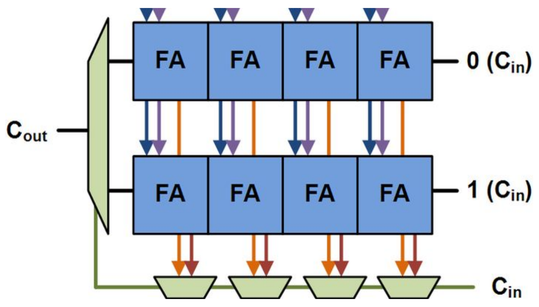
Ripple-Carry



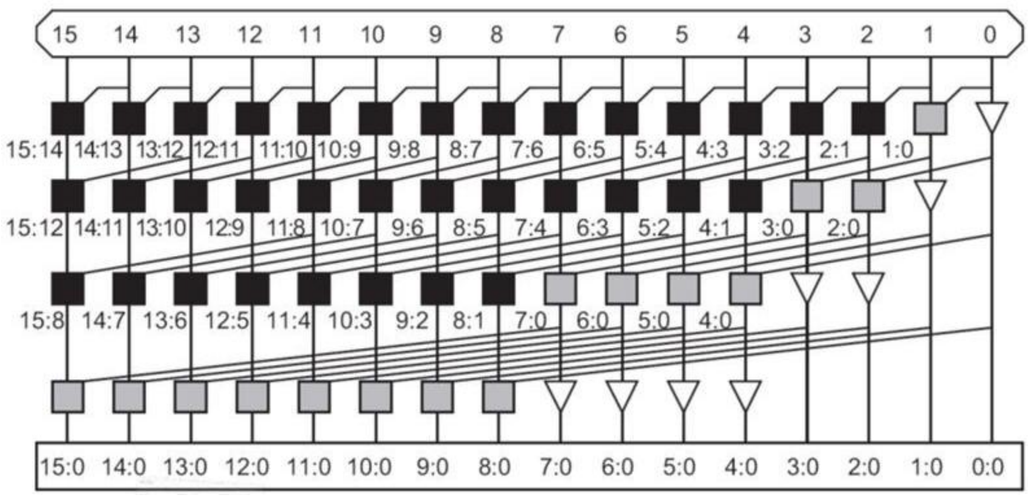
Carry-Lookahead



Carry-Select

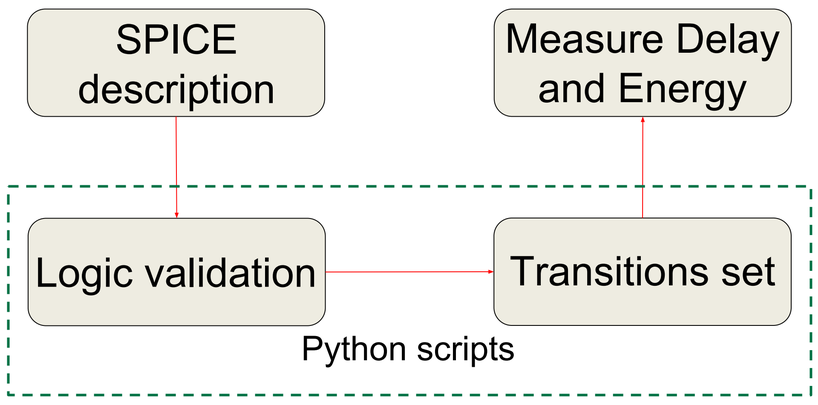


Kogge-Stone Adder



Calculate Gi:j = Gi:k + Pi:k · Gk-1:j
Calculate Gi:j = Gi:k + Pi:k · Gk-1:j and Pi:j=Pi:k · Pk-1:j

Evaluation Flow



Results

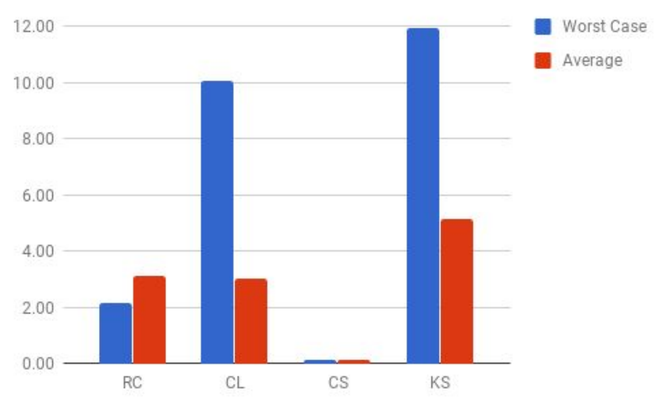
Signal Propagation Times

	Longer delay times (ns)		Average (ns)	
Model	**32nm**	**16nm**	**32nm**	**16nm**
Ripple-Carry	0.932	0.806	0.297	0.249
Carry-Lookahead	0.613	3.565	0.387	0.637
Carry-Select	0.543	0.404	0.360	0.337
Kogge-Stone Tree	0.549	1.393	0.469	0.497

Energy Consumption

	Higher energy costs (fJ)		Average (fJ)	
Model	**32nm**	**16nm**	**32nm**	**16nm**
Ripple-Carry	5.588	3.587	1.90	1.81
Carry-Lookahead	3.888	1.733	1.61	0.76
Carry-Select	6.916	0.353	4.14	0.15
Kogge-Stone Tree	7.515	9.107	4.15	5.19

Normalized PDP



Ripple-Carry adder presented a good power consumption coupled with the penalty of the longest path to carry-out generation. Carry-Lookahead model was more efficient than the first in terms of signal propagation time and the lowest average energy consumption for 32nm.

Conclusions

The models presented expected characteristics regarding the observed variables. Finally, the Kogge-Stone Tree adder had a good delay time but a high power consumption for their 4-bit simulation. These architecture of n-bit adders probably reaches better results for 16 bits adders or more.

Thus, the next steps are to perform the simulations for 8, 16, 32 and 64 bits with the same analysis of propagation delay and power consumption.

References

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