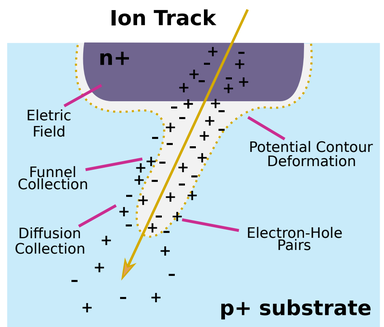
CHIP in Sampa
SForum 2019

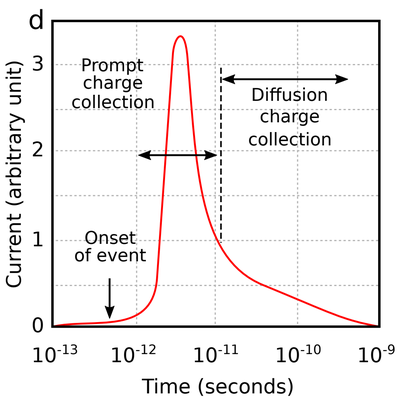
Radiation Robustness Evaluation on XOR Logic Gates at 16nm CMOS and FinFET Technology

Rafael Neves de Mello Oliveira, Cristina Meinhardt, Federal University of Santa Catarina - Brazil
rafael.nmo@grad.ufsc.br, cristina.meinhardt@ufsc.br

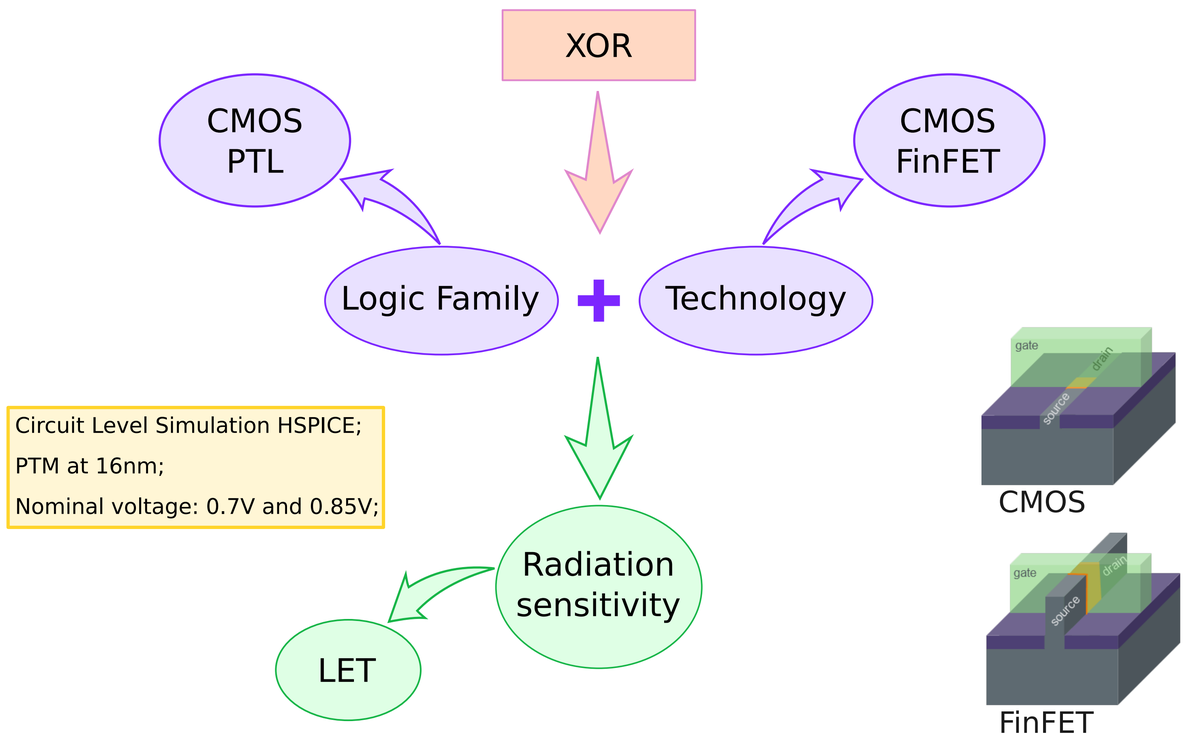
1. Introduction

- Circuits are becoming more susceptible to noise effects due to technology scaling (R. C. Baumann, IEEE T-DMR 2005).
- Particles with low energy are able to interfere within the operation of the circuits (J. Leray, RADECS 2001).
- The experiments consist of extracting minimum current that causes a fault on the device, i.e., the Linear Energy Transfer (LET) based on an analytic solution (G. C. Messenger, IEEE T NUCL SCI 1982).





2. Method



2. Topologies

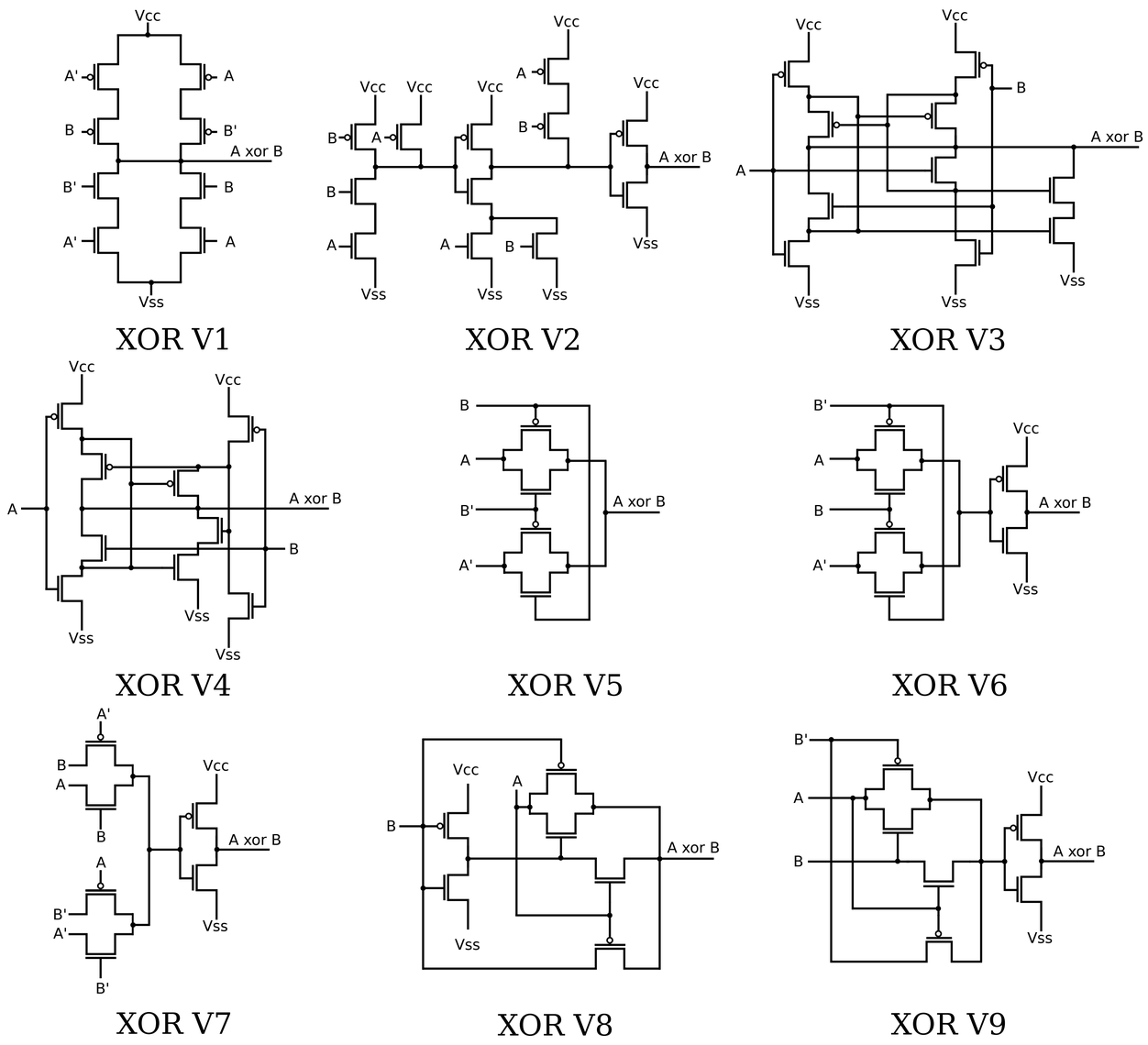
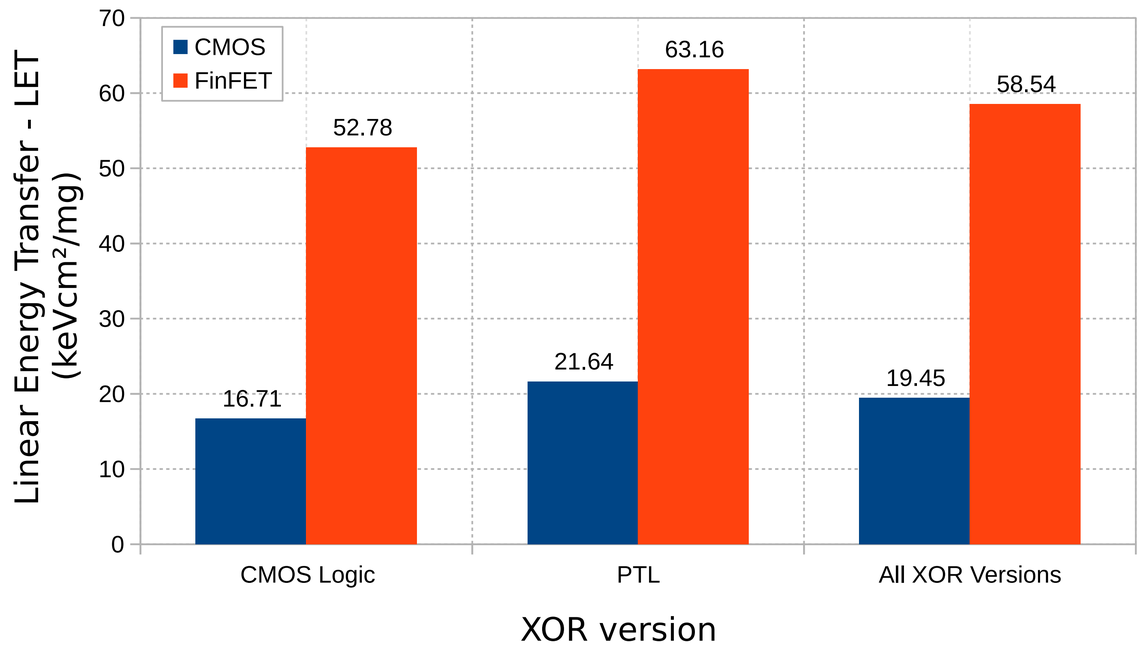


Fig. 1 XOR topologies explored in this work

4. Results

- PTL topologies had an increase in robustness up to 30% for CMOS devices and up to 20% for FinFET when compared with CMOS logic versions.
- FinFET devices improve the average robustness 2x for both logic families.



CMOS vs PTL

↑2,1x ↑1,9x

CMOS FinFET

Linear Energy Transfer - LET

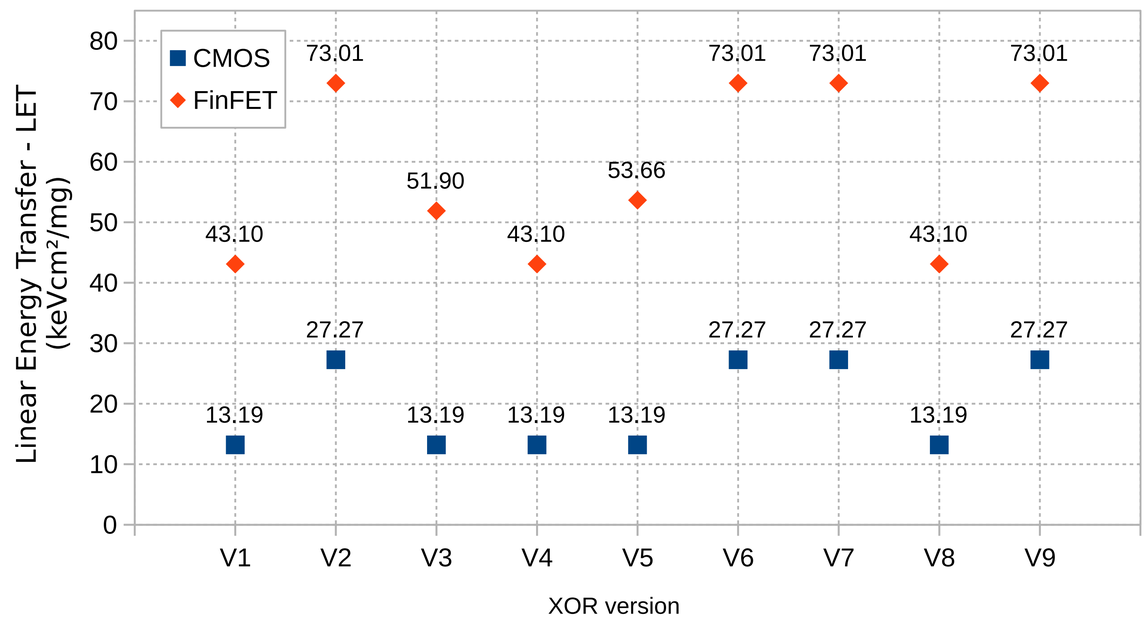
CMOS vs FinFET

↑2x

FinFET

Average LET

- For both technologies, XOR V2, V6, V7, and V9 have shown to be the least sensitive to radiation effects.
- XOR V1, one of the most common topologies found in standard cells, proved to be one of the most sensitive.
- XOR V5 implemented with FinFET technology had the greatest improvement with more than 3x when compared with its equivalent in CMOS devices.



5. Conclusion and Future Work

- This work evaluates the radiation sensitivity on 9 XOR logic gates at 16nm. PTL topologies have shown to be less sensitive against faults for both technologies analyzed. FinFET devices improve robustness up to 2x.
- As future work:
  - ➔ Investigate new methodologies to fault insertion;
  - ➔ Modeling in a new tool;
  - ➔ Transistor sizing;
  - ➔ Evaluation of different XOR topologies;

CNPq Conselho Nacional de Desenvolvimento Científico e Tecnológico

August 26-30, 2019 São Paulo, SP

EEL UFSC