Investigating Algorithms for Identifying Transition Arcs in Logic Circuits

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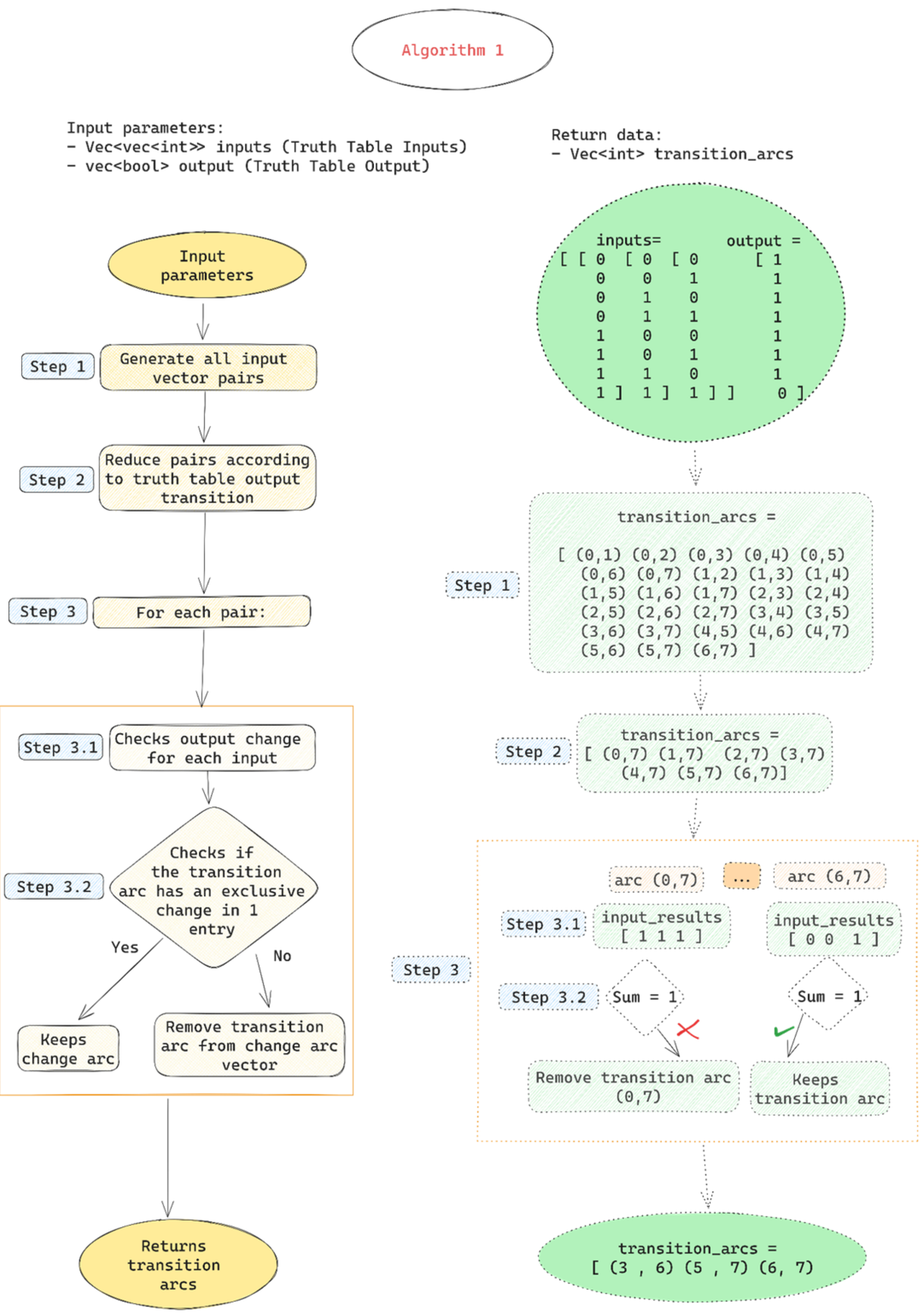
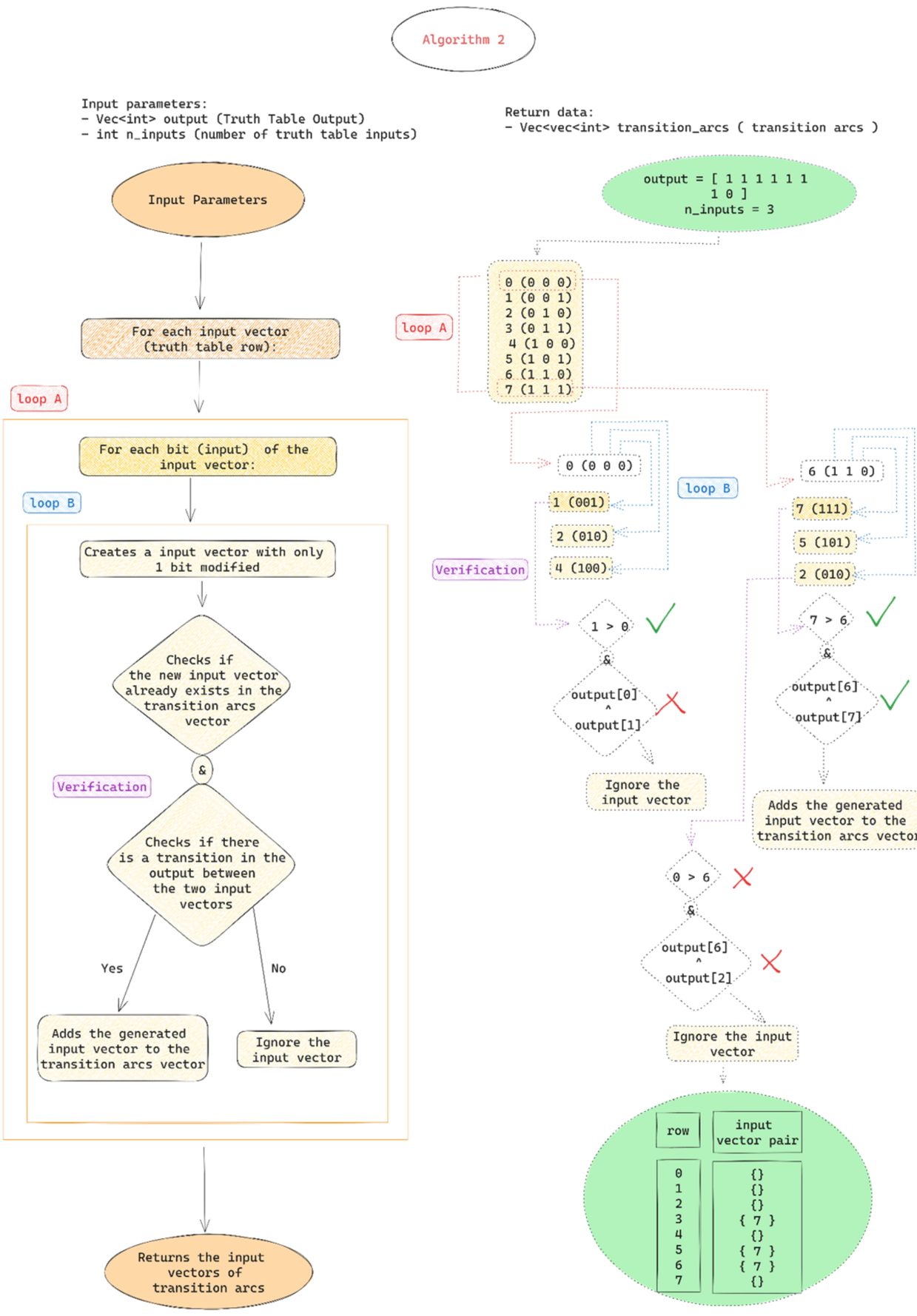
Introduction

The identification of transition arcs of Boolean functions is an important step in the simulation and analysis of logic circuit design. This identification allows the measurement of delay times in output state transitions given a change in a specific input.

The main objective of this work is to provide a fast and memory efficient flow to delay characterization of combinational circuits.

This work starts exploring 2 algorithmic alternatives for recognizing these arcs.





Conclusions

The next stage of the ongoing study is to obtain metrics regarding the efficiency of the developed algorithms and compare the results in different truth table situations. The following metrics will be evaluated:

- Execution time
- Memory usage
- Algorithmic complexity

For this, the algorithms will be implemented using the Rust programming language.

Also, as future work, we will provide a related work review about similar algorithms and characterization flows.

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