Evaluation of Approximate Static CMOS Magnitude Comparators

Omitted to allow double blind review

***Abstract*—This work consists of an assessment of 8-bit digital magnitude comparators designed with requirements for energy efficiency. Nine circuits were selected from the relevant literature, distinguished in 3 categories: full-custom (STC), gate-based (EDC and AxDC1, AxDC2) and two-bit comparator-based designs (ETBC, T22, T14, T43 and T34). The topologies were described in 7 nm FinFET and simulated under nominal voltage to extract delay, power and the power-delay-product (PDP), as well as considering the error distance of the approximate topologies. Our results spotlight the STC circuit, which obtained relevant advantages in the examined metrics, compared to the others. Among the approximate gate-level designs, the results highlight AxDC1 as a promising alternative for low-power and small-input applications. The AxDC1 demonstrated low penalty of 0.59% error rate with to achieve a 37% reduction in PDP compared to the original EDC comparator.**

***Index Terms*—approximate computing, digital arithmetic, magnitude comparators**

I. Introduction

Designing efficient Digital Magnitude Comparators (DMC) is highly relevant for many general purpose [1] and dedicated hardware architectures, with impact on a varied of application as image and signal processing systems [2], [3], modern wireless communication [4], [5], and tree-based learning accelerators [6], [7]. In general, it is desirable that these circuits compute all three possible results of a comparison between two operands, $A > B$, $A = B$ and $A < B$. In energy-constrained application, exploring single-output alternatives becomes interesting for minimizing computation and circuit area. This involves selectively removing specific comparison branches, like either $A < B$ or $A > B$. Moreover, in error-tolerant scenarios such as learning models and image processing, where energy efficiency is paramount, motivates the consideration of design techniques exploiting relaxed accuracy, namely approximate computing (AxC) [8].

Some approaches for approximation in DMCs leverage the knowledge of the distribution of the input values from target application to design circuits that provide improved energy efficiency while avoiding part of the degradation in accuracy. For instance, in [6], the authors propose a methodology for approximating bespoke tree-based classifiers, so that each comparator circuit is optimized for the threshold constants used in each attribute test. Nonetheless, there are situations where application-agnostic topologies are better suited, e.g. when it is desirable to maximize hardware reuse, or when the end-user requires future reconfiguration of the system, making bespoke architectures unfitting. In these cases, designers interested in employing an approximate DMC must fully understand the error dispersion of the approximation and opt for topologies that meet the accuracy and electrical requirements, avoiding alternatives that cause many pointless errors and compromise the quality of the output [9].

To this end, the main contribution of this work is the systematization of electrical and error characteristics of a set of exact and approximate comparators from the available literature, viewed under the same technology node and simulation conditions. The goal is to provide a general panorama about the trade-offs of their potential use, highlighting the energy-efficiency and error dispersion of each examined circuit.

The rest of this text is organized as follows: Section II gives an overview of related work on energy-efficient digital comparator design, detailing the topologies selected for this evaluation. In Section III, we describe the evaluation environment for electrical and error characterization. Finally, the electrical results and error characteristics are presented and analyzed in Section IV, and we conclude in Section V.

II. On the design of energy-efficient and approximate comparators

Due to the importance of this magnitude comparators, numerous research works have focused on improving the design of this circuit, with different techniques focused on energy efficiency or timing performance. Conventionally, high performance DMCs are designed using components from high-speed adders, for instance [12], [13]. An alternative architecture is proposed in [14], using a static CMOS parallel-prefix tree structure that is up to $2.7\times$ faster and $3.3\times$ more energy-efficient than the previous state-of-the-art designs. Recently, [15] proposed a parallel-prefix single clock cycle comparator using dynamic domino logic and dual-mode operation to reduce power dissipation from internal node switching, while in [16], a tree-structured dynamic logic in domino CMOS comparator is described using a reduced number of transistors in comparison with established implementations.

On the other hand, energy efficient designs generally use static CMOS logic, which has lower switching activity and thus less dynamic power dissipation. In [10], a full-custom tree structured magnitude comparator is presented and confronted with [14], demonstrating lower area overhead, delay and Power-Delay Product (PDP) for small inputs.

When focusing on approximation techniques for comparator design particularly, we find most of research works employ standard cell-based designs, and a few centering on adder-based comparators. [17], explores an approximate sub-carry generator circuits in a 16-bit inexact comparator that has an

TABLE I: Details for selected 8-bit comparators

Topology	Transistor count	Techonology	Platform	Notes	Target
STC [10]	142	UMC 90nm CMOS	Cadence Virtuoso, Spectre simulation, pre-layout	full custom static CMOS, tree-based comparator, single branch computation	N/A
EDC [11]	158	ASAP7 7nm FinFET	PrimeSim HSPICE simulation, pre-layout	gate-level, limited precision, single branch computation, conventional design based on Bit-Competition Logic (BCL)	Decision tree models
AxDC1 [11]	106			truncation approximation of EDC - 2 LSBs ignored	
AxDC2 [11]	70			truncation approximation of EDC- 2 LSBs ignored, bits B2 and B3 propagated directly	
ETBC [9]	240†	Nangate 45nm Open Cell LIbrary	Synopsys Design Compiler	gate-level, sub-magnitude comparison ($A > B$ and $A < B$), BCL-based Two-Bit Comparator (TBC) design	Image median filtering
T22, T14, T43, T34 [9]	104, 176, 136, 136†			gate-level, sub-magnitude comparator, approximate TBC logic	

†Includes 56 transistors used for resolving the bit competition logic and common to all variants.

Error Rate (ER) $< 0.1\%$ and is up to $18\times$ more efficient in the Energy-Delay Product (EDP), when compared to Ripple-Carry Comparators (RCC) and Carry-Lookahead Comparators (CLC). [18] then extends this work by replacing the sub-carry generator for equality and greater-or-equal logic in a portion of the LSBs, achieving ER as little as 0.04% and up to $1.5\times$ lower EDP than the previous design [17].

Targeting tree-based learning accelerators, [11] proposes two dedicated approximate magnitude comparators employing bit competition logic in the standard cascading architecture [19], where the inexactness is introduced by truncation of the 25% of the Least Significant Bits (LSB) from each input. In the best case, these comparators showed 11% savings in energy and 24% reduction in critical delay, with an ER of only 0.56%, suitable for error-tolerant applications.

Finally, dealing with image median filtering applications, [9] propose a set of Two-Bit Comparators (TBC) designed using "don't care" logic, which can then be used to build larger comparators with adjustable error characteristics. The novel circuits reduce up to 46% in power consumption and up to 50% in area. In the follow-up [2], three more approximate TBCs were developed with guarantees that the inserted errors would not interfere with the targeted median filters, i.e. there is no compromise between approximation and quality of the application. In [3], two more TBC approximations are given using functional simplification for use in compare-and-swap blocks. No information is given on the error and electrical metrics of the comparator circuits, but the complete median filters are shown to achieve 41.9% reduction in PDP compared to the exact implementation.

In this work, we are specially interested in circuits well-suited for small operands, rejecting, for instance, carry-lookahead type comparators which have more benefits for larger inputs, as was the case with [18]. From the discussed approximate designs, we selected those which had the best potential to be used in a application-agnostic manner, excluding those from [2], for example. The selected comparators included the following: (1) the full-custom Static CMOS Tree-structured Comparator (hereafter labeled as STC) [16]; (2) the gate-based exact and approximate dedicated comparators (EDC and AxDC1, AxDC2) [11]; and (3) TBC-based comparators with 75% LSB approximation (ETBC, T22, T14, T43 and T34) [9]. Details from each circuit are summarised in Table I. Since the architectures presented in [10] and [11] actually compute $\overline{A > B}$, i.e. $A \leq B$, to make the analysis fairer, only the less-or-equal branch of computation will be considered from the TBC-based DMC discussed in [9], representing a reduction of 30 transistors in the bit comparison resolution logic from the lower and equal computation branches. Circuit and gate-level schematics are provided at the transistor or gate-level in Figure **??**.

III. Methods

In this study, we focus on two fronts: (1) the electrical characterization of all selected comparators in the same technology and evaluated under equal conditions; and (2) the error assessment of the approximate adders.

Regarding the first front, the electrical characteristics chosen to establish a comparison between the circuits under analysis were the average power dissipation and critical delay. For this purpose, 8-bit extensions of each comparator were described adopting the 7nm FinFET ASAP7 PDK [20] using the RVT device models and simulated in PrimeSim™ HSPICE®. All devices are sized with 3 fins, the minimum recommended by the PDK specification. The electrical simulations were performed with nominal supply voltage of 0.7 V. To emulate a realistic scenario, the input stimulus sources are fed through a buffer made of 2 minimum sized inverters, and the Device Under Test (DUT) output was connected to a 1fF capacitor to simulate load, enough to cover a FO4-equivalent load. Aside from the full-custom design, the gate-level architectures are implemented using static CMOS circuits of up to 4 inputs, and any larger gates are broken down into smaller cells to avoid issues arising with charge mobility when connecting many devices in series.

To find the critical delay of each comparator topology, the strategy adopted was to exhaustively stimulate the relevant transition arcs to measure propagation delay, ensuring they are

as close to reality as feasible pre-layout. Due to the functional approximation, each comparator topology has a different truth table, making it necessary to compute separate transition arcs for the inexact circuits. Since delays for the DUTs were in the order of picoseconds, the transition arcs were simulated with 1Ghz frequency, sufficient for all waveforms to stabilize. From the simulation results, we calculate the average power dissipation considering all transition arcs, and select the largest delay as the one representing the critical path. The PDP is also provided as a trade-off metric.

For the error analysis, we consider the error rates for each comparator, calculated from their respective truth tables. Error Dispersion Maps (EDM) are included to ease the understanding of the error distribution as a function of the inputs.

IV. Results and discussion

From the simulation results and error analysis, the obtained results are summarized in Table II. Starting with an evaluation of the three exact comparators investigated, it is clear that the full-custom STC design outperforms the EDC and ETBC in all measurements observed. The average power dissipation is 24.1% lower than the EDC and 62.1% lower than the ETCB designs, while reducing the delay by $\approx 55\%$ compared to either gate-based comparator. The difference in power dissipation could be offset by employing a full custom design for the logic in EDC and ETBC, for instance using complex gates instead of standard 2-input implementations of the basic operations. It is also important to note that the STC design is particularly well suited to exploit parallelism, while providing good extensibility to n-bit comparators, contrasting with the EDC, which becomes quite complex to implement for larger values of n, e.g. $n > 16$, due to the required n-input logic gates in the critical path,

Only two exact comparators discussed have approximate counterparts, namely the Exact Dedicated Comparator (EDC) and Exact Two-Bit Comparator (ETBC). While both comparators employ a form of bit-competition logic, the strategy used to resolve the comparison is quite different: the EDC uses a cascading greater-than comparison resolving the output at each stage, while the ETBC compares bits two-by-two which allows for a parallel evaluation of parts of the input, then resolving the output by combining the initial 2-bit tests. The results shown in Table II indicate similar propagation delays for both architectures, though the average power dissipation of the ETBC is nearly $1.6\times$ that of the EDC, which is at least partly explained by the more complex logic of bit competition used, requiring the evaluation of lesser-than and equal-to branches in the 2-bit pre-encoding to the resolution logic. We note that the architecture implemented with TBCs is significantly easier to extend to single or double precision if required, compared to the cascading logic in EDC, which would provide an extensive critical path, with no parallel partial comparations. Nonetheless, for the 8-bit precision circuits, the EDC stands out considering standard cell implementations, with the STC maintaining the best results if full custom design is feasible.

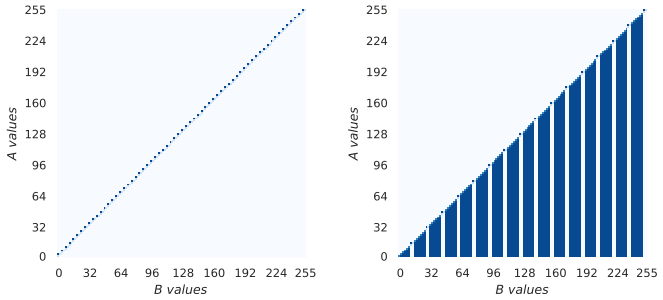
TABLE II: Electrical and error characterization for selected comparators

Topology	Delay (ps)	P_{avg} (nW)	PDP (aJ)	ER (%)
STC [10]	33.88	357.86	12.12	N/A
EDC [11]	75.35	471.14	35.50	N/A
AxDC1 [11]	57.11	453.85	25.92	0.59%
AxDC2 [11]	39.03	296.21	11.56	37.21%
ETBC [9]	73.36	746.41	54.76	N/A
T22 [9]	74.03	730.13	54.05	16.60%
T34 [9]	74.03	691.86	51.22	11.66%
T43 [9]	73.71	706.70	52.09	11.66%
T14 [9]	73.36	692.31	50.79	11.03%

Concentrating on the approximate designs, similar patterns appear in Table II. The EDC-derived designs AxDC1 and AxDC2 both follow a similar design methodology, truncating 25% of the LSB, and AxDC2 further bypassing logic for the next 25% LSBs by copying the B operand as a partial result. This effectively reduces the number of transistors needed by a third in the AxDC1 and by more than half in the AxDC2, as seen in Table I. Since these approximations are somewhat independent of implementation, we could, for instance, design a truncated ETBC similarly to the AxDC1 by removing the least significant TBC, or yet a truncated STC leveraging both the efficient and scalable design in [10] as well as the approximation benefits found in [11]. The $ER < 0.6\%$ of AxDC1 is also particularly attractive, as it signals to little degradation of application output quality, with promising reduction of Power-Delay Product (PDP) of up to 37% in comparison to the EDC. On the other hand, while AxDC2 provides a three-fold reduction in PDP, it has quite a high error rate, close to 40%, which makes it unsuitable for most applications.

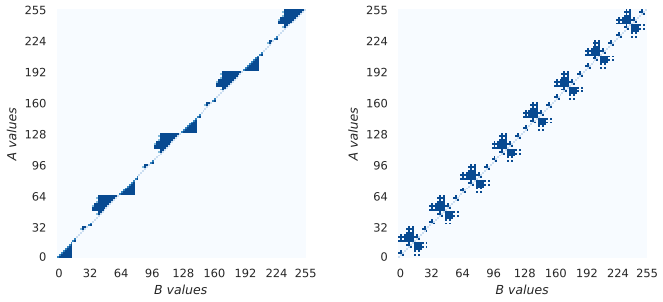
The TBC-based designs show no reduction in the critical delay, an interesting result considering the removal of at least one logic gate from the critical path of all TBCs. This behavior may be an effect of the delay arcs stimulating the exact TBC used in the two most significant bits to control error which could lead to the similar delay results observed. Regarding power dissipation, the effect was more significant, with the best case T14 providing a reduction of up to 7.8% in both average power and PDP, and along with T34 and T43 providing similar error rates of $\approx 11\%$. Interestingly, the least significant gains were observed in T22, the comparator with highest error, with an ER of 16.6% and only 1.3% reduction in PDP.

Despite modest gains in PDP reduction, the main benefits of the approximate TBC-based comparators compared to the EDC-inspired versions are their configurability and scalability. The modular design of TBC-based DMCs allows them to be extended to n-bits by simply chaining TBC and Equality Checking (EC) blocks. Accordingly, the designer may choose the configuration of one or more approximate TBCs that match the required accuracy and electrical characteristics, as well as how many TBC blocks will be approximated [9]. We note that the truncation strategy presented in [11] may also be explored here by simply using a smaller comparator and ignoring the



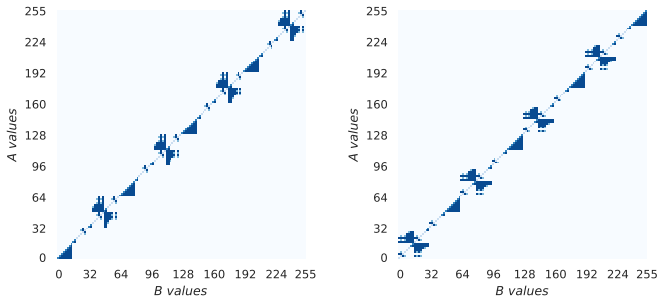
(a) AxDC1

(b) AxDC2



(c) T14

(d) T22



(e) T34

(f) T43

Fig. 1: Error Dispersion Maps (EDM) for each approximate comparator. Comparators T14, T22, T34 and T43 use 75% LSB approximation [9].

m LSBs of both inputs.

While the electrical characteristics are important factors in deciding which comparator, or combination of such, should be used in a given application, when handling approximate circuits, the designer should also strive to incorporate knowledge from the target application to enhance accuracy results. To this end, we analyze the Error Dispersion Maps (EDM) in Figure 1. The most notable effect we see is that for all comparators, except AxDC2, the majority of errors are concentrated on the diagonal representing similar inputs. Since all approaches investigated employ a form of LSB approximation, this is expected, as closer inputs should lead to the comparison resolution being reached in the LSBs, i.e. the error-prone region. Once again, the AxDC1 stands out in Figure 1a, as the error region is highly concentrated on this diagonal, with a large number of error non-inducing inputs also being close. On the other hand, the AxDC2 has a weak use-case when lesser-or-equal checking is somewhat guaranteed, that is, most A inputs are expected to be less than or equal to B values, as seen in Figure 1b(b). The high error rates makes this a very unattractive alternative for most applications. As for the approximate TBC versions, the errors are concentrated on a 5-bit error margin around the equality main diagonal, reflecting the fact that each 8-bit DMC used 3 approximate two-bit comparators. The 6-bit approximation also explain the repeating pattern we see in Figure 1c, 1d, 1e and 1f.

V. Conclusion

This work consisted of an evaluation of eight alternatives for energy efficient and approximate Digital Magnitude Comparators. From these designs, three DMCs were exact: the STC, a full custom tree-structured; the EDC, a gate-level cascading bit competition logic architecture; and the ETBC, also a gate-based TBC bit competition topology. Considering the approximate designs, we investigated two truncation-based approximations for the EDC, and four "don't care" inexact variants of the ETBC. All designs were evaluated under the same technology node and simulation conditions, enabling a fair assessment of their electrical characteristics.

The full custom design, STC, provided the best overall results in all metrics, with the smallest critical delay of 33.88ps, less than half that of the exact comparators and any of the TBC-based approximations. In power consumption, only the aggressive truncation in AxDC2 achieved lower, or even similar, results, although its error rates are a significant limitation to their real-world applicability.

Focusing on the approximate gate-level designs, the truncation-based approximation showed the most promise in the AxDC1, demonstrating that this simple strategy causes $ER < 1$ while achieving 37% reduction in PDP, compared to its original comparator EDC. As such, it comes as the best alternative for a low-power and small-input application, especially in cases where the full custom STC is unfeasible.

In summary, truncation-based techniques are particularly simple to implement in a multitude of comparator architectures, and provide well controlled error when limited to the LSBs with good results in the electrical characterization. For instance, the functional approximation in AxDC1 could easily be replicated in STC by removing one black node from the tree, and in the TBC-based comparators, removing the TBC for the two LSBs. At the moment, these explorations are left as future work.

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