Energy-Efficient Design of Approximated Full Adders

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***Abstract*—This work analyses a set of approximate full adder circuits in 7nm FinFET device technology in order to identify how energy-efficient these designs are for different voltage operation points. The behavior in a specific environment with voltage scaling is compared to conventional exact adders. The results allow designers access to the pros and cons of each design in error-tolerant applications. Considering the impact on delay and power consumption, approximate XNOR and PTL based FAs showed increase in PDP for all voltages applied. However, Mirror Adder inspired approximate designs showed a reduction in PDP at 0.4V. The PDP for buffer approximated FAs remained constant throughout voltage scaling.**

***Index Terms*—approximate computing, full adder, low-power**

I. Introduction

Approximate Computing (AC) is an emerging research area capable of providing excellent results on energy savings [1], which exploits the fact that many applications do not have exactness as the central requirement. In the last years, AC has been explored in hardware and software development for different contexts, including video and sound processing, Internet of Things (IoT) devices, fault-tolerant environments, computer vision, machine learning and sensor networks [2].

There are many error-free computations where exploring AC enlarges the design space with the addition of quality metrics [3]. Some of the opportunities for Approximate Computing are applications that [3] [4]:

1) process noisy real-world data, such as those coming from sensors, or IoT uses;
2) have final results which will be perceived by human senses, as many problems in Inference and Vision; and
3) are based on inherently imprecise algorithms, in which the concept of a correct result is replaced by a range of acceptable results, for example, recognition, data analysis, and machine learning.

The primary motivation for the development of AC solutions is the increased demand for low-power designs [5]. Nowadays, in deep nanotechnology designs, battery life is a significant factor to be considered. Many applications involve a large number of arithmetic operations that explore in-depth the adding modules. The add operation is, as such, the main arithmetic function in computer systems and the base of the most commonly used arithmetic blocks. Thus, a digital system has the 1-bit full adder (FA) as one of the most critical basic blocks of an arithmetic unit.

The performance of a FA cell is a vital point to be improved to achieve low-power, fast operations on arithmetic blocks [6]. The literature shows that many works explore AC on arithmetic blocks at architectural or Register-Transfer Level (RTL) [3] [5] [7] [8]. However, few works investigate AC techniques applied to the transistor level of full adders. There is a lack of electrical level evaluation of approximated techniques, and voltage scaling approaches applied together in the same circuit, furthermore considering a multigate technology nanometer node.

This work provides a comparison of a set of FA circuits at a FinFET nanometer technology. The main goal is to identify how these designs behave in a specific environment compared to conventional exact adders, when combining AC techniques and voltage scaling [9], analyzing performance, power consumption, and Power-Delay Product (PDP). This set of information contributes to designers better understanding of the AC full adder alternatives and choosing the most appropriate adder for a specific application.

II. Approximate Full Adders

The FA is the base of most arithmetic operations, such as subtraction, multiplication and division, and, as such, is the main cell of the Arithmetic Logic Unit (ALU) of computing systems. While the functioning of an adding cell is not very complicated, taking into account the frequency of its use, the electrical behavior of FAs becomes critical for the performance of the system. These circuits consist of three inputs, the two bits from the operands (A and B) and a carry-in (Cin), and two outputs. The sum (S) output is given in the Equation 1, and the carry out (Cout) is described in the Equation 2. Various transistor arrangements implement 1-bit adders. Each design has advantages and disadvantages regarding the area, delay, and power consumption.

In this work, eight different full adder topologies were chosen and analyzed. Two of them are exact full adders, namely the Exact Mirror Adder (EMA) and Exact XNOR Adder (EXA) [10], respectively Figs. 1 and 2. The other topologies are three approximations based on the EMA, presented in Figs. 3(a), 3(b) and 3(c), and two simplifications of the EXA [11], whose circuit is shown in Figs. 4(a) and 4(b). Finally, a simple buffer approximate FA (BXFA) is the also evaluated where the Sum output is defined by propagating the A input, and the Carry-out output follow the B input. To decouple the output from the input, in the BXFA insert two inverters in cascade from the selected input to the output.

$$S = A \oplus B \oplus Cin \tag{1}$$

$$Cout = (A \cdot B) + (A \oplus B) \cdot Cin \tag{2}$$

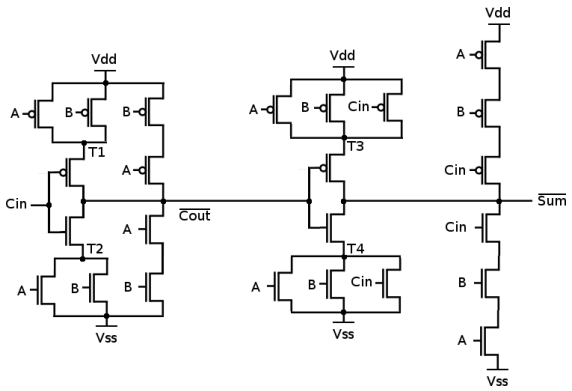


Fig. 1: Exact Mirror Adder (EMA).

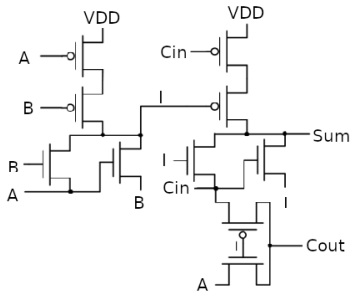


Fig. 2: Exact XNOR Adder (EXA).

The most traditional architecture is the Mirror CMOS EMA, chosen as a base for comparison between the studied topologies. It is composed of 24 transistors structured in logically complimentary pull-up and pull-down networks. The advantages of this circuit are good conductibility and robustness when working with small technologies and lower tension. However, the EMA shows high input capacitance, and the impact of the pull-up network makes the circuit's operation slower [12]. On the other hand, the EXA uses Pass Transistor Logic (PTL) to reduce the number of transistors, having ten devices in total. This circuit was chosen as an example of low-power and area-efficient design in FAs [10] [11].

The approximations exploit the relaxation of numerical accuracy and were designed with diminished logical complexity to reduce the number of transistors and power consumption. Therefore, they present differences in their truth tables, as shown in Table I, along with the error distance (ED) as a figure of merit to compare the AC FAs. The input vectors that generate failure when compared to the exact full adder implementations are summarized in Table II. Notably, the BFXA is the topology that produces the largest number of errors while the AXA3 is the topology with least error-inducing input vectors with only an ED of two. SMA also fails for the same two input vectors that AXA3, but it provokes only three output errors as the ED in total. The most critical inputs are 010 (except the AXA2 topology) and 100 (except the AMA1 and BXFA topology).

TABLE I: Truth tables for an exact adder and the evaluated approximations.

INPUT			**EXA**		**SMA**		**AMA1**		**AMA2**		**AXA2**		**AXA3**		**BXFA**	
A	B	Cin	S	Cout	S	Cout	S	Cout	S	Cout	S	Cout	S	Cout	S	Cout
0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0
0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0
0	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1
0	1	1	0	1	0	1	0	1	1	0	0	1	0	1	0	1
1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0
1	1	0	0	1	0	1	0	1	0	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
ED			-	-	2	1	3	1	3	2	4	0	2	0	4	2

TABLE II: Transistor and error count for each approximate topology

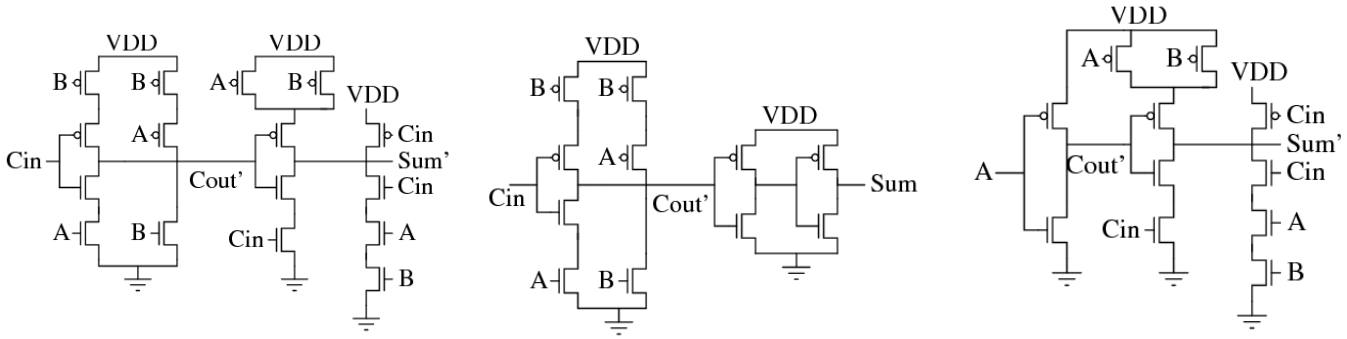
Topology	**Transistor count**	**Failure inputs**	**Fail count**
SMA	16	010, 100	2
AMA1	11	000, 010, 111	3
AMA2	11	010, 011, 100	3
AXA2	6	000, 001, 100, 110	4
AXA3	8	010, 100	2
BXFA	8	001, 010, 101, 110	4

III. Methodology

The goal of this work is to show the energy-efficiency of AC FAs design. For this, the reduction in power consumption provided by the use of approximate FA cells is evaluated for different voltage points, while observing the impact on delay. In particular, the effects of AC combined with the savings known to be provided by voltage scaling techniques [9] are explored, in order to find the overall most efficient low-power adder cells within acceptable accuracy restraints.

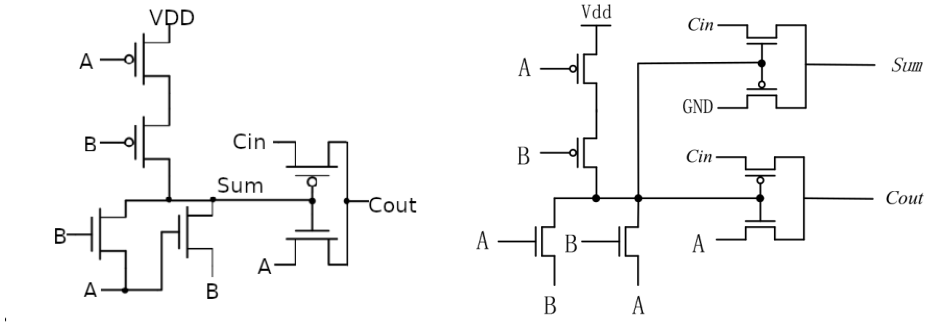
The topologies are described under the model provided by the 7nm FinFET ASAP7 PDK [13], and simulated in HSPICE. All designs adopt three fins, as recommend by the design rules provided by the ASAP7. The nominal supply voltage for these devices are 0.7V [13]. The voltage was reduced in steps of 0.1V until the noise levels were too great to provide correct functioning, or the delay was too large to be used in operation. The threshold voltage is approximately 0.3V, thus, we define as near-threshold operation the results obtained for voltages between 0.4V and 0.2V. In order to emulate a more realistic scenario, two inverters were used as a load in each input and both Cout and Sum outputs of the FAs circuits are connected to a FO4 inverter.

The experiment considers the exhaustive evaluation of all transition arches of each FA Truth Table. Thus, complementary to the error-distance and the critical delay, the power consumption is determined by the average power result for all the transition arcs. This work also considers a figure of merit the product of power consumption and critical delay Power-Delay



(a) Simplified Mirror Adder (SMA). (b) Approximate Mirror Adder 1 (AMA1) (c) Approximate Mirror Adder 2 (AMA2)

Fig. 3: Approximate FAs inspired by the EMA.



(a) Approximate XNOR Adder 2 (AXA2). (b) Approximate XNOR Adder 3 (AXA3)

Fig. 4: Approximated FAs based on the EXA

Product (PDP) for the eight adders under nominal and later with reducing voltages.

IV. Effects of Voltage Scaling Technique

When applying voltage scaling in conjunction with full adders developed in an Approximate Computing design space, the evaluated topologies showed some advantages and disadvantages, as present the Table III, the Table IV, and the Fig. 5. There was evident improvement in power consumption, the main focus of the voltage reduction technique, shown in Table III. All designs appear to be good candidates to voltage scaling, with an average reduction in power dissipation of 34% for each topology when stepping from 0.7V to 0.6V. In near-threshold operation of 0.3V, the power consumption reduced on average by 86.69%, being lowest in the AXA3 design (8.89nW, in absolute value). Although BXFA does not stand out in terms of power reduction, it shows the best result for delay at near-threshold voltages. Thus, voltage scaling successfully obtained results in energy saving when using these AC adder cells.

The most significant drawback of voltage scaling is the increased critical delay in all FA architectures. The XNOR-based adders are by design optimized for low-power operation and have the disadvantage of more considerable delay when compared to the Mirror Adder versions. XNOR topologies were also the worst-performing when considering timing analysis, as shown in Table IV. Overall, the adders analyzed are, on average, 9.32× slower in near-threshold operation (0.3V), with the worst-case found in the AXA2, which has a delay of 13.37× that found in nominal voltage operation.

TABLE III: Effects of Voltage Scaling on Power (nW)

Topology	0.7 V	0.6 V	0.5 V	0.4 V	0.3 V
EMA	772.15	509.54	334.19	197.54	105.58
SMA	539.93	357.10	231.50	136.73	71.85
AMA1	659.75	435.60	271.08	159.93	84.95
AMA2	418.31	263.40	171.83	102.30	52.95
EXA	271.92	175.02	109.23	61.29	31.66
AXA2	128.18	85.90	57.25	33.36	17.98
AXA3	60.90	40.32	27.45	16.40	8.89
BXFA	279.53	176.25	114.50	66.67	35.20

TABLE IV: Effects of Voltage Scaling on Delay (ps)

Topology	0.7 V	0.6 V	0.5 V	0.4 V	0.3 V
EMA	12.28	13.80	24.01	42.51	122.80
SMA	13.07	14.34	19.46	35.28	117.30
AMA1	9.45	11.74	16.27	29.69	98.76
AMA2	8.72	9.52	13.22	25.64	81.62
EXA	52.60	104.80	220.50	495.20	714.20
AXA2	57.40	116.30	248.50	546.20	828.40
AXA3	40.49	84.25	188.30	412.10	418.00
BXFA	6.42	8.14	10.72	23.04	63.25

Since voltage scaling presents such advantages and drawbacks, Power-Delay Product (PDP) will be used as a metric to trace a relation between the gains in power and the increase on the delay. All circuits showed rise in PDP when comparing operation in near-threshold and nominal voltages. Notably, the XNOR-based FAs showed continuous increase up until 0.4V, as seen in Fig. 5.

The best alternative considering both power and delay is the BXFA, that reaches the best results for all evaluated cases. This topology keeps the PDP practically constant independently of the voltage applies, as the reduction in power consumption was proportional to the increase in delay, especially when compared to the variations in PDP seen in the other adders. Therefore, despite the ED, the BXFA is an interesting approach for applications that require a good trade-off between power and delay.

The second best option observing PDP is the AMA2 operating in 0.5V, that is, 2.27aJ. However, for applications considering the error-distance, the power reduction and the PDP, a good solution could be exploring the AXA3 circuit at nominal or at 0.4V (lowest power, but high delay).

In general, PDP shows that the operation at near-threshold voltages (under 0.5V) can introduce high degradation due to the significant increases in the delay for these FAs. The worst results amongst the approximate adders was found in the near-threshold operation (0.4V) of the AXA2 architecture, which had a PDP of 18.22aJ.

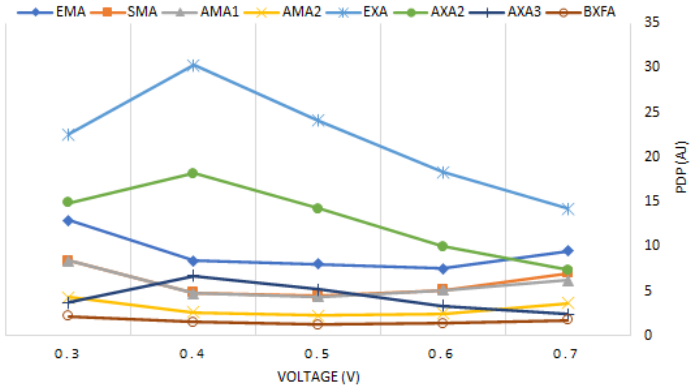


Fig. 5: Effects of voltage scaling on PDP (aJ).

V. Conclusion

Full adders are critical circuits in many applications that are error-tolerant, which allows the use of approximations. As such, it is essential to understand the behavior of different topologies for FAs, mainly when operating in conjunction with other low-power design techniques, as voltage scaling.

In this analysis, significant improvement was found in all EMA-based architectures for voltages from 0.6V to 0.4V, with reductions of up to 38% in PDP. Thus, the SMA, AMA1, and AMA2 are topologically well adapted to voltage scaling, which provides even better energy savings compared to exact adders or approximate adders in nominal voltage. The BXFA was well adapted for operation in all voltages applied, and is also a good option when considering PDP.

Some approximate circuits studied will not provide better power efficiency when reducing the operation voltage, especially when considering the increase in critical delay. In near-threshold operation (0.3V), none of the circuits, except the BXFA, showed improvement in Power-Delay Product, having a 37% increase on average. Notably, the XNOR adders are not well suited to voltage reduction, as there was no reduction in PDP whatsoever for none of the voltages applied. As future work, this project will investigate the impact of adopting these approximated full adders on n-bit adders and error-free applications, such as Machine Learning and video applications.

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