Ritarka Samanta

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Education

Georgia Institute of Technology Jun 2021 – Dec 2023
Bachelor of Science in Computer Engineering, Major GPA 4.0/4.0 *Atlanta, GA*

Relevant coursework: Adv. Computer Architecture, Processor Design, VLSI & Adv. Digital Design, Programming for HW/SW Systems, Compilers & Interpreters, Embedded Systems, Adv. Operating Systems, Adv. Data Structures & Algorithms, Adv. Prog. Techniques

Skills

Programming: C/C++, Java, Python, Assembly, Tcl, Shell Scripting, CUDA, XML, Open MPI, React, HTML5
Software: Unix/Linux, Docker, GDB, Git/Perforce, PyTorch, Jenkins, Qemu**,** Vivado, Quartus, Networking
Hardware: Verilog, System Verilog, VHDL, Vitis HLS, FPGAs, Logic Analyzers, DMMs, PCBs, Microcontrollers
Activities: Reading, Chess, Hiking, Travelling, Puzzles, Tutoring

Work Experience

Cadence Design Systems May 2023 – Aug 2023
Software Engineering Intern *San Jose, CA*
- Automated finding differences in hardware models using Python. Reduced analysis time by a factor of 6
- Engineered Java application to support quick edits to the memory map of complex systems
- Expanded debugger to enable collaboration between companies while retaining their individual proprietary information (codebase of over 400 million lines)
- Updated C/C++ code (over 1000 lines) and removed dependencies on boost library. Developed and tested custom data-structures and string libraries as part of project

Northrop Grumman Jun 2022 – Aug 2022
Hardware Engineering Intern *Baltimore, MD*
- Developed JTAG code to reduce multi-day debugging process into one hour
- Enabled fully automated testing of hardware network board. Resolved 2 documentation errors in the process
- Modified C++ application to bypass lengthy setup times of large codebase, speeding up testing by 5 times

Research

HPArch Lab May 2023 – Present
Researcher *Atlanta, GA*
- Accelerated ability to select dataset-effective pretrained object-detection ML models by 4 times
- Upgraded object-detection framework with newer models, decreasing inference time by 15%
- Designed dynamic model selectors to obtain balance between mean average precision (mAP) and latency

Sharc Lab Aug 2022 – May 2023
Researcher *Atlanta, GA*
- Developed a web-based tool to enable source-level Vitis HLS debugging, improving debugger load times by 8 times
- Extracted new information from HLS output files, set-up back-end API, and created new visualizations
- Composed architecture and coordinated 3 cross-functional teams to manage product development

Leadership & Extracurricular

Deep Learning Accelerator January 2023 – Present
Director *Atlanta, GA*
- Organized and trained a group of 6 people to accelerate machine learning algorithm using FPGAs
- Splitting neural network in half to create a multi-FPGA accelerator
- Optimizing model in Vitis-HLS, with goal of obtaining over 30 fps across datasets

Operating System Design January 2023 – May 2023
- Designed Virtual Memory, Threading, File System, Bootloader, etc. for Linux-like monolithic OS
- Programmed primarily in C and Assembly, debugged slow applications, and optimized them

Volatility Viewer October 2022
Georgia Tech Hackathon, a winner of BlackRock Challenge
- Created a data analytics platform to educate investors about market volatility with insights on portfolio management
- Analyzed and plotted economic indicators against a volatility index using Python libraries such as Pandas and NumPy