- Awarded **Undergraduate Research Award** for Study of Phase Noise Sources in Ring Oscillator *2019*
- Awarded **Institute Technical Color** for exceptional contribution to technical activities in the institute *2019*
- Received the **Kishore Vaigyanik Protsahan Yojana (KVPY)** fellowship, with **AIR 171** *2014*

## Publications

**O. Kolhe** and C. Jain, '*Microcontroller based, satellite borne Transmitter for broadcasting images using SSTV - A prototype design*', Satellite Technology Day, **ISRO Satellite Centre**, Bengaluru, April 2018

## Internships

- **Sony Semiconductor Solutions Corporation, Japan** || *Analog LSI Bussiness Division* May '18 - July '18
  - Investigated and benchmarked Automotive TV LSI solutions of competitor, against DTG and NorDig test set
  - Developed an new **Software Defined Radio** (SDR) technology feature on Automotive TV LSI products by designing and testing of **USB streaming** application on Raspberry Pi platform after an extensive study of existing RTL-SDR
  - Designed and successfully tested a digital down converter logic board for down sampling and interleaving IQ samples as a proof of concept demonstrator system by decoding FM signal using a programmable RF tuner IC

## Research and Technical Projects

- **VCO for 5G and NB-IoT Receivers** || *Masters' Thesis* May '19 - Present
  *Guide : Prof. Maryam Shojaei Baghini, Electrical Engineering, IIT Bombay*
  - Studied **phase noise models** in Ring Oscillators and effect of bond wire and power supply noise on phase noise
  - Studying **Injection Locking** of a 4-Stage Ring oscillator with a LC Oscillator for generation of accurate **8 phase** clock for N-Path Filtering for 5G receivers and the effect of injection locking on ring oscillator's phase noise
  - Modelling **wire bonds** in **HFSS** to estimate its inductance, to utilize it as an inductor in LC tank of the LC oscillator
- **Receiver for IRNSS** || *Research Project* May '17 - May '18
  *Indian Regional Navigation Satellite System (IRNSS also named as **NavIC**) is navigation satellite constellation consisting of 7 satellites, completed in April 2016 for navigation in the Indian subcontinent - **ISRO***
  - **RF Amplfier and Filter design for the Receiver** *May '17 - Jul '17*
    *Guide: Prof. Shalabh Gupta & Prof. Sibi Raj Pillai* *Research Project*
    - One of the **first** student project to conceptualize and fabricate a receiver for IRNSS and first step towards implementing NavIC for **civil** and **military** applications as an **indigenous** alternative to GPS
    - Designed and successfully tested a PCB for signal conditioning and out-of-band noise rejection consisting of a Low Noise Amplifier (LNA), a SAW Filter and 2 stage RF amplifier
  - **Antenna and RF Front-end for the Receiver** Jan '18 - May '18
    *Guide: Prof. Shalabh Gupta* *Electronic Design Lab Project*
    - Designed, fabricated and successfully tested a S-band (2.492048 GHz) right hand circularly polarized (**RHCP**) dual feed patch antenna with a branch line coupler with 16 MHz bandwidth
    - Designed and fabricated a **4-layer** PCB for **amplifying** and **downconverting** the received RF signal in **S-band** to baseband (0 Hz) using I/Q Demodulator with baseband amplifiers, Frequency Synthesizer and microcontroller
    - Successfully received **navigation bits** from all satellites using our setup thereby validating the prototype
  - **Signal Processing for the Receiver** Jan '18 - May '18
    *Guide: Prof. Rajesh Zele* *Supervised Research Exposition*
    - Studied the signal processing block in a IRNSS receiver implemented in MATLAB to get navigation bits
    - Implemented FFT based acquisition methods- code phase domain & doppler frequency domain thus decreasing the acquisition time compared to the common Serial Search technique in MATLAB
    - Implemented the serial search acquisition block, digital Phase Locked Loop and Delay Locked Loop for tracking using ping-pong buffers on TM320C5515 DSP board to get navigation bits
- **Disbond Detection** || *Research Project* Oct '18 - May '19
  *Aimed at detection of disbonds in carbon fibre honeycomb structure used in launch vehicle - Funded by **ISRO***
  *Guide : Prof. Siddharth Tallur*
  - **Prototype I** : Single Channel Sampling System *Course Project : Sensors in Instrumentation*
    - Designed an embedded system to sample Lamb waves on carbon fibre sheet using PWT sensors at 512 kHz by implementing a **ping-pong** buffer for real time signal processing on TM4C1294XL board using internal ADC
    - Implemented real time 512 point FFT and 1-D Continuous Wavelet Transform (**CWT**) using Morlet wavelet

- **Prototype II** : 8-Channel Simultaneous Sampling System *Research Project*
  - Designed a modular 8 channel data acquisition system with each channel capable of sampling at 4 GHz using a FPGA as buffer, which will then send the sampled data serially to a DSP board for signal processing
  - Implemented the system using ADC121S101 sampling at 1GHz, **FPGA** and **Nios II** processor as a proof of concept
  - Implemented 1-D Continuous Wavelet Transform using Morlet wavelet on TI's DSP C6678 multicore processor

- **Communication Subsystem** || *Advitiy, Student Satellite Team* May '17 - Present

*Advitiy is the 2nd student satellite of IITB, technically advanced and efficient version of the 1st, Pratham*

- Devised the operational modes for the system, defined switching conditions and conceptualized the framework for the flight code designed to coordinate between 3 microcontrollers and onboard peripherals
- Designed and implemented end to end link of image transmission and reception in SSTV (Slow Scan Television) protocol in software as well as hardware, establishing it as a proof of concept of Advitiy's payload
- Ideated the functioning of Beacon to minimize load on the communication microcontroller by using scheduled interrupts so as to enable the satellite to perform other computations simultaneously
- Designed and tested PCBs for uplink, power amplifier & pre-flight board to access the satellite electronics after integration

## Academic Projects

- **VCO Design and Layout** || *VCO Design and Layout* Mar '19 - May '19
  - Awarded prize for **unique design** in Layout Design Competition judged by **industry experts** from Qualcomm
  - Implemented an LC based PMOS cross-coupled VCO with tail noise filtering with a tuning range of 4.5 to 5.5 GHz
  - Used capacitor banks and varactor for frequency tuning and achieved a low Phase Noise of -118 dBc/Hz at 1MHz Offset
- **Folding Flash A/D Converter Design** || *Mixed Signal VLSI Design* Mar '18 - Apr '18
  - Designed 4-Bit 1GS/s Folding Flash ADC using double tail latch with offset cancellation with reference subtraction
  - Designed a differential T/H circuit with dummy switches for clock feedthrough and charge-injection compensation
- **LNA Design and Layout** || *Radio Frequency Microelectronics Chip Design* Mar '19 - May '19
  - Designed a two stage noise cancelling Common Source LNA with inductive source degeneration at 2.49 GHz
  - Achieved Noise Figure of 3.2dB, DC gain of 24.9dB, Bandwidth of 100MHz, IIP3 of -10dBm and P1dB of -21.8dBm
- **16-bit Rational Arithmetic Unit (RAU)** || *VLSI Design Lab* Mar '19 - May '19
  - Designed a 16-bit RAU capable of addition, subtraction, multiplication and division of 16-bit signed numbers
  - Implemented a modified **Dadda reduction** technique for addition of partial products from **signed multiplication** of 2 or 4 numbers on Cyclone IV E FPGA thus increasing computational speed and reducing the resources required
- **Card Shuffling Optimization** || *Probability and Random Processes* Sep '17 - Nov '17
  - Developed a simulation based model to suggest best shuffling strategy to randomize a deck of 52 cards
  - Implemented GSR model of riffle shuffle to find probability distribution of each possible sequence in deck
  - Incorporated rising sequence and simulated for different combinations of shuffles such as riffle, overhand and cut

## Positions Of Responsibility

- **Subsystem Head, Communication Subsystem** || *Advitiy, Student Satellite Team* Jan '18 - Present
  - Spearheaded a team of **8** members to developed a **quality assured** communication system for the satellite
  - Organized Groundstation Workshops in 2019, 2018 and 2017 with over **80 students** and **faculty members** across India sharing knowledge on satellite communication and how to setup a groundstation as part of the social goal of the project
  - Contributed to Satellite 101 wiki, a compilation of basic knowledge of satellite project with **26k** pageviews and **10k** users
  - Executed a **three-step recruitment** process to select 16 students for the subsystem, from 70+ applicants evaluating their technical ability, practical approach and teamwork for recruitment in 2018 and 2019.
- **Teaching Assistant** || *Electronic Devices Lab* July '19 - Present
  - Part of a team of teaching assistants responsible for conducting weekly core course lab sessions for **60+ students**
  - **Aiding** and **evaluating** students for in-lab work involving ngSpice and characterization of electronic devices and circuits
- **Technical Secretary** || *Hostel 5, IIT Bombay* April '16 - April '17
  - Awarded Hostel **Tech Colour** and **Organizational Special Mention** for display of ardent dedication
  - Managed all the technical resources and inventories of the hostel with a budget of more than **80,000 INR**

## Relevant Courses Undertaken

| | |
|---|---|
| **Analog VLSI** | CMOS Analog VLSI Design, Mixed Signal VLSI Design, **RF Microelectronics Chip Design** |
| **Digital VLSI** | VLSI Design, Foundations of VLSI CAD, VLSI Design Lab |
| **Instrumentation** | **Integrated Circuit Design for Sensor Systems**, Sensors in Instrumentation |
| **Devices** | VLSI Technology,Solid State Microwaves Devices, Microelectronics Simulation Lab |
| **Miscellaneous** | Design and Evaluation of Photovoltaic Power Plants |

## Skills and Interests

| | |
|---|---|
| **Design Tools** | Cadence Virtuoso, Intel Quartus, HFSS, ADS, IE3D, TI CCS, System Advisor Model, PVlib |
| **HDLs & Programming** | C++, C, Python, MATLAB, VHDL, Verilog, Assembly, JAVA |
| **Interests** | Circuit Simulation, RF and Mixed Signal Design, Sensor System Design and PV systems |

## Extra Curricular Activities

- Actively **volunteered** in Green Campus, **National Service Scheme** for conservation of plant species in the institute *2015*
- Successfully qualified level 1 and 2 **Tabla** exams conducted by Akhil Bharatiya Gandharva Mahavidyalaya Mandal *2012*