Solid State Microwave Devices and Applications

Course Project

Power Amplifier Design

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Design Steps

➢ Cascade the 2 stages and run S parameter simulation.

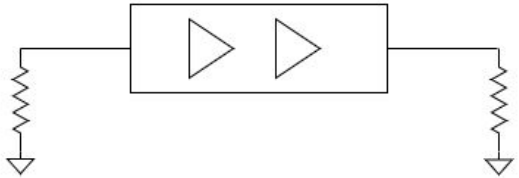
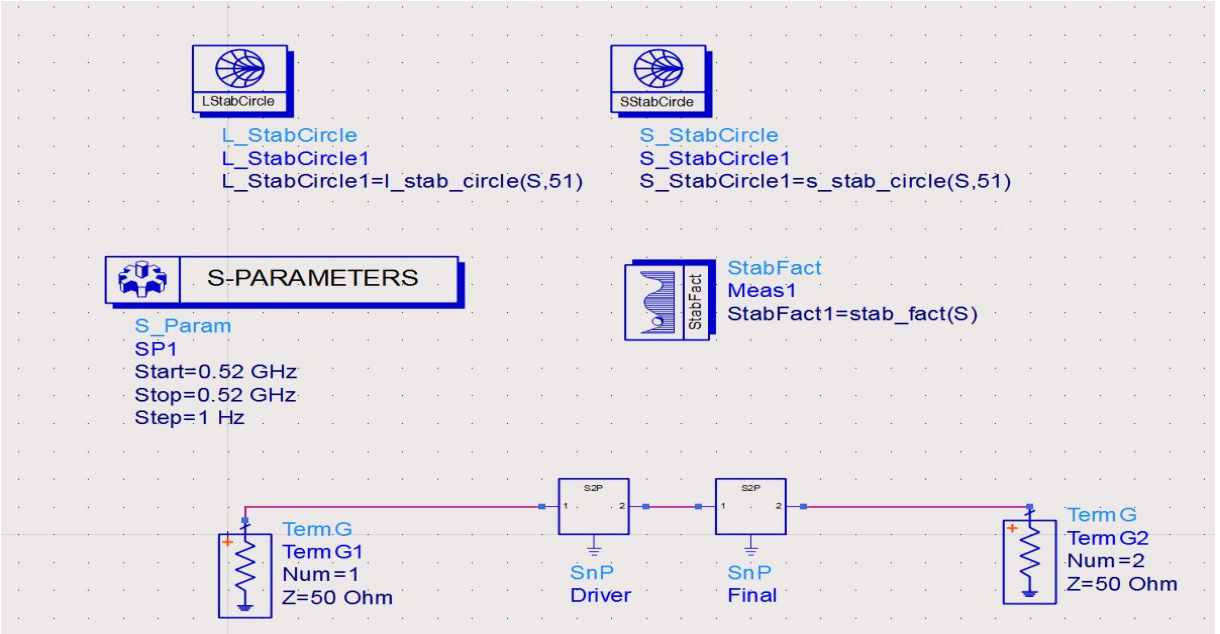


Fig: 2 stage amplifier

AIM :

- Get the combined S parameters.
- Check for stability.



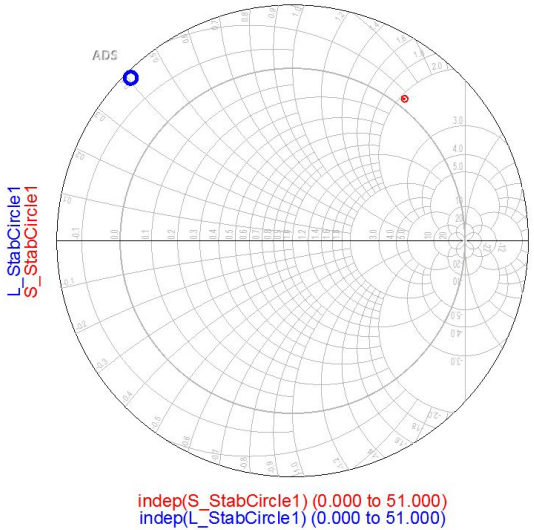
S Parameter Simulation results :

freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
520.0 MHz	0.954 / -51.934	1.788E-4 / 12.589	10.175 / -175.692	0.734 / -135.415

Stability Factor :

freq	StabFact1
520.0 MHz	10.833

Stability Circles:



Observation:

- K>1, |Δ|<1 means unconditional stability.
- Both source and load stability circles are outside the Smith chart

Conclusion : We are safe

Design Steps

Unilateral or Bilateral Design?

- S_{12} is not 0.
- Check unilateral figure of merit.

freq	U	Error_min_dB	Error_max_dB
520.0 MHz	0.031	-0.261	0.269

Observation: 0.27dB error is tolerable

Conclusion : We will do unilateral design

Design Steps

- Since we don't have stability issues, we can go with any possible gain.
- $G_{TU}(dB) = G_S(dB) + G_O(dB) + G_L(dB)$

AIM :

- Find maximum possible gain.
- Find the corresponding Γ_S and Γ_L

Equations :

```
Eqn Gs_max = 1/(1-(mag(S(1,1)))**2)
Eqn Gs_max_db = 10*log(Gs_max)
```

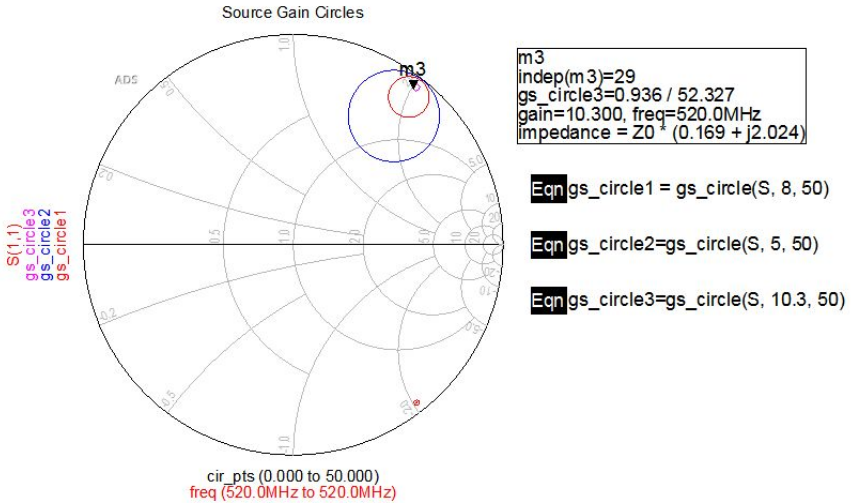
```
Eqn G_o=(mag(S(2,1)))**2
Eqn Go_db=10*log(G_o)
```

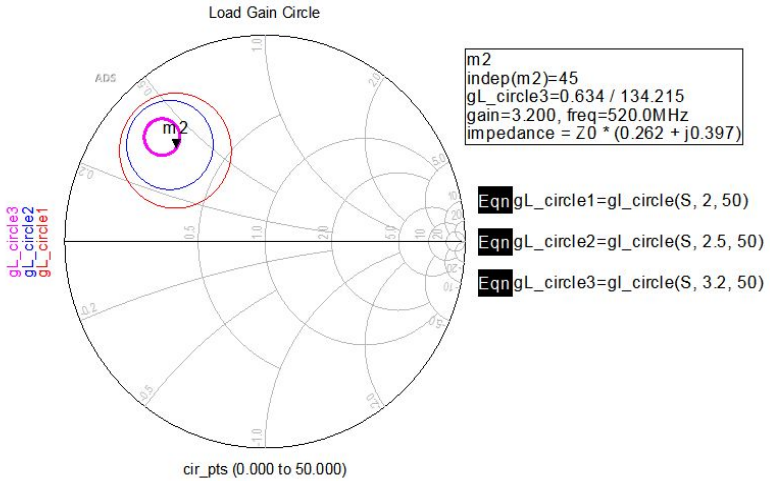
```
Eqn GL_max=1/(1-(mag(S(2,2)))**2)
Eqn GL_max_db=10*log(GL_max)
```

freq	Gs_max	G_o	GL_max
520.0 MHz	11.057	103.524	2.167

freq	Gs_max_db	Go_dB	GL_max_db
520.0 MHz	10.436	20.150	3.358

Design Step :Choosing Source and Load Gain



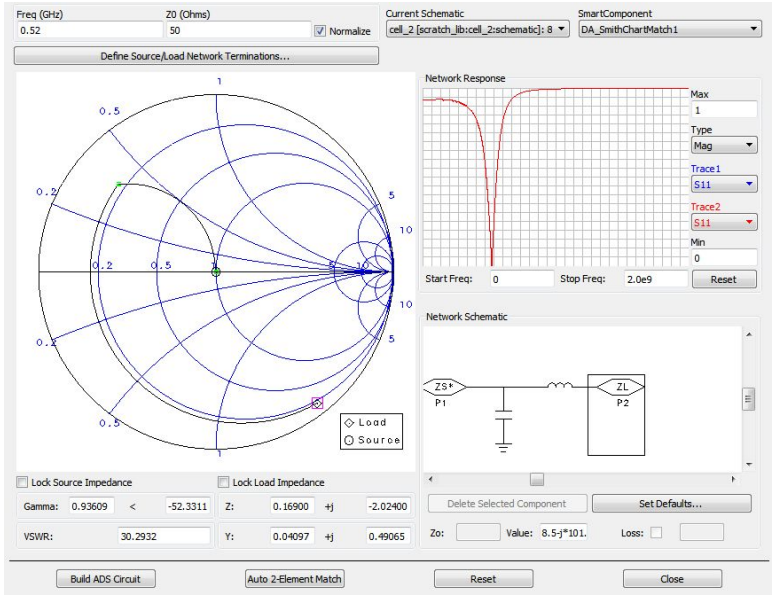


Result :

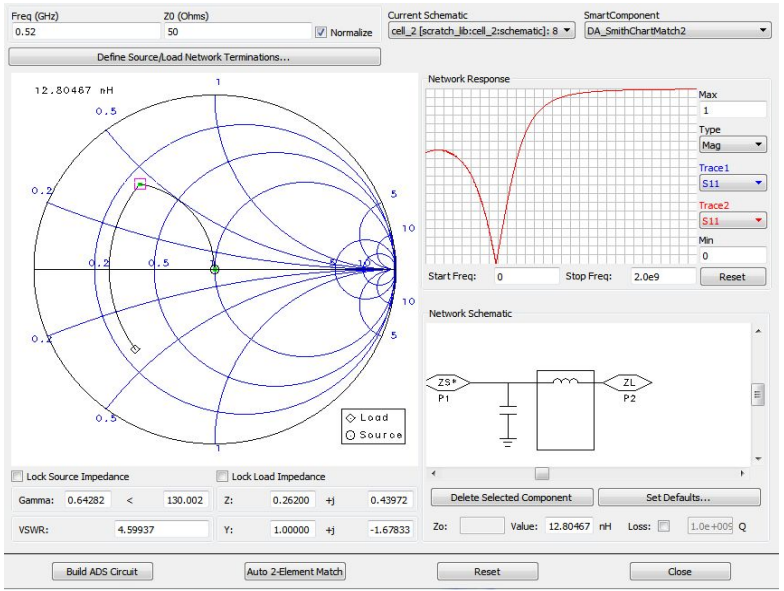
- Source gain circle selected for Gain = 10.3dB
- Γ_S chosen for Z_S = 50 * (0.169 + j2.024)
- Load gain circle selected for Gain = 3.2 dB
- Γ_L chosen for Z_L = 50 * (0.262 + j0.397)

Design Step : Design matching network

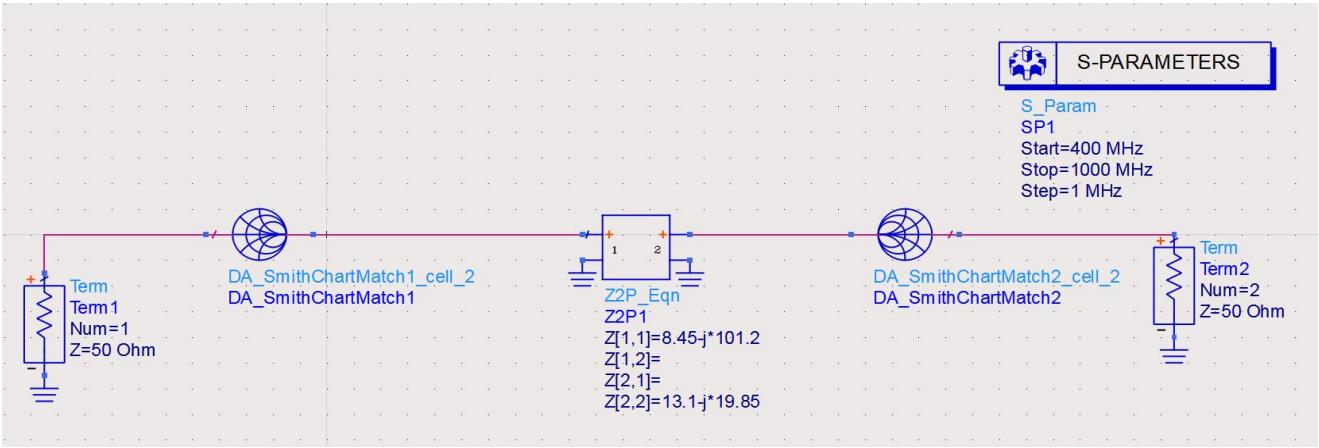
Using **Smith Chart Utility tool** to match
source impedance : 50 * (0.169 + j2.024)



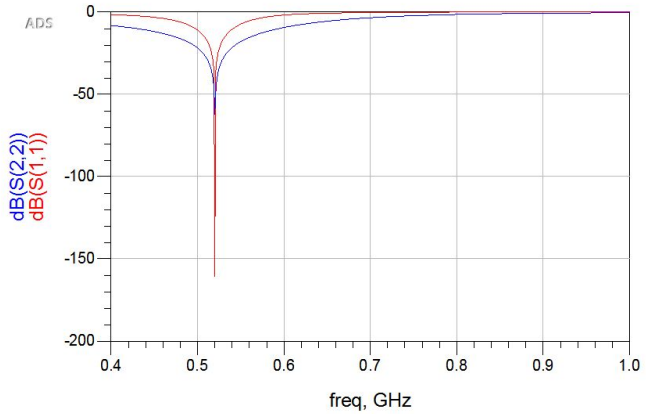
Load impedance : 50 * (0.262 + j0.397)

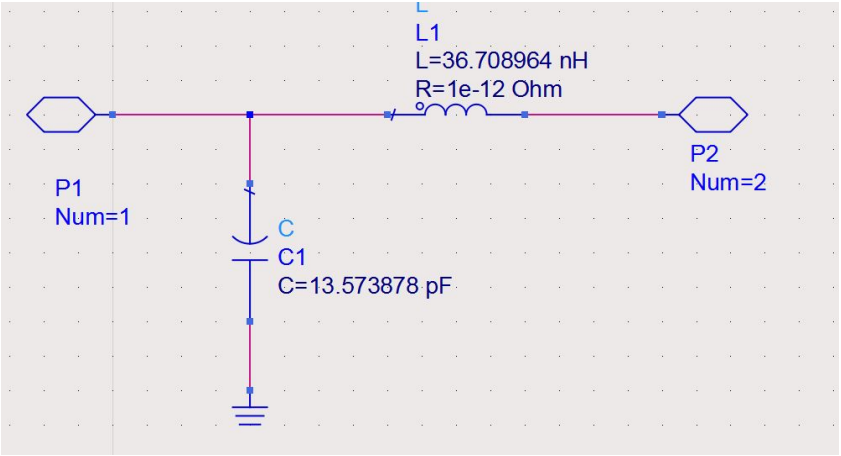


Matching simulation Setup (without the s param file):

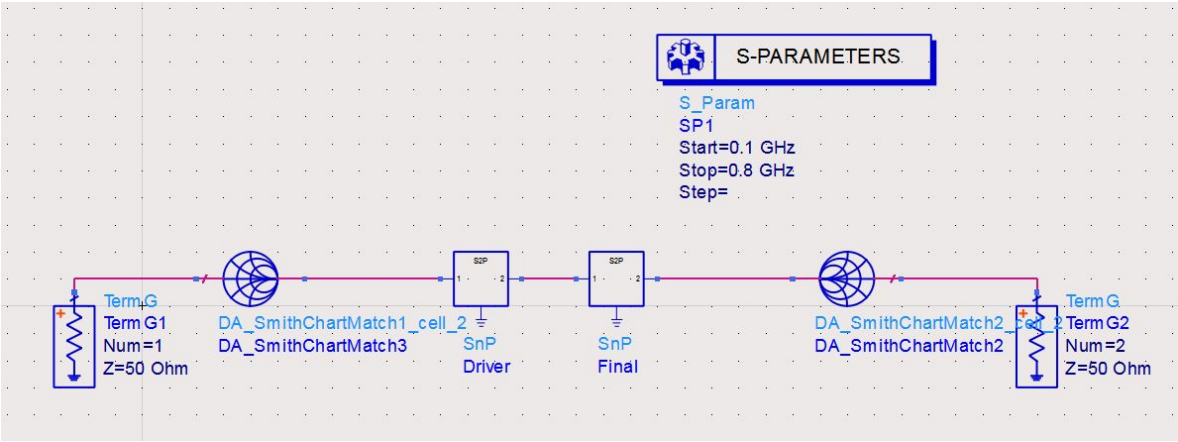


Matching result :

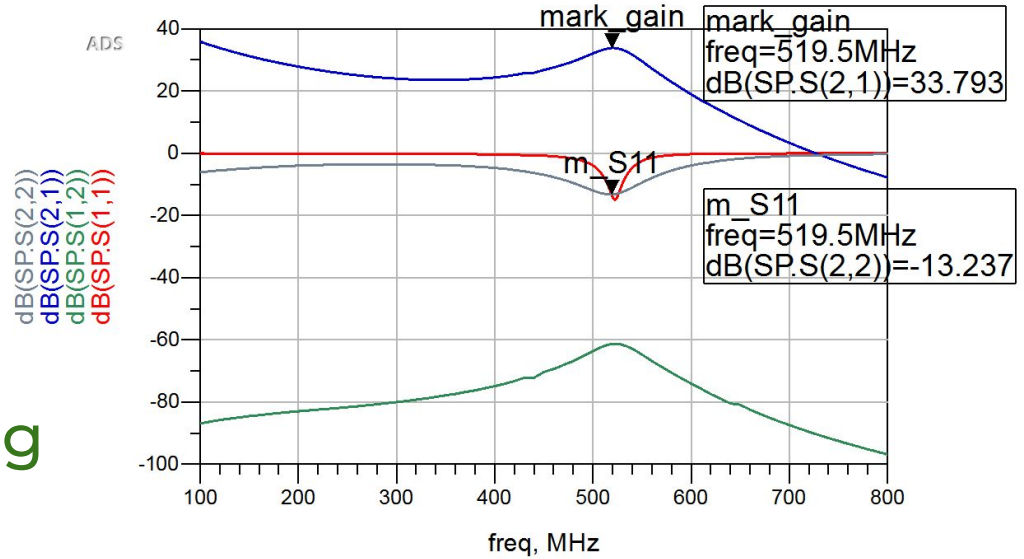




Setup for simulation with S param file :



S param plot :



Conclusion : Working

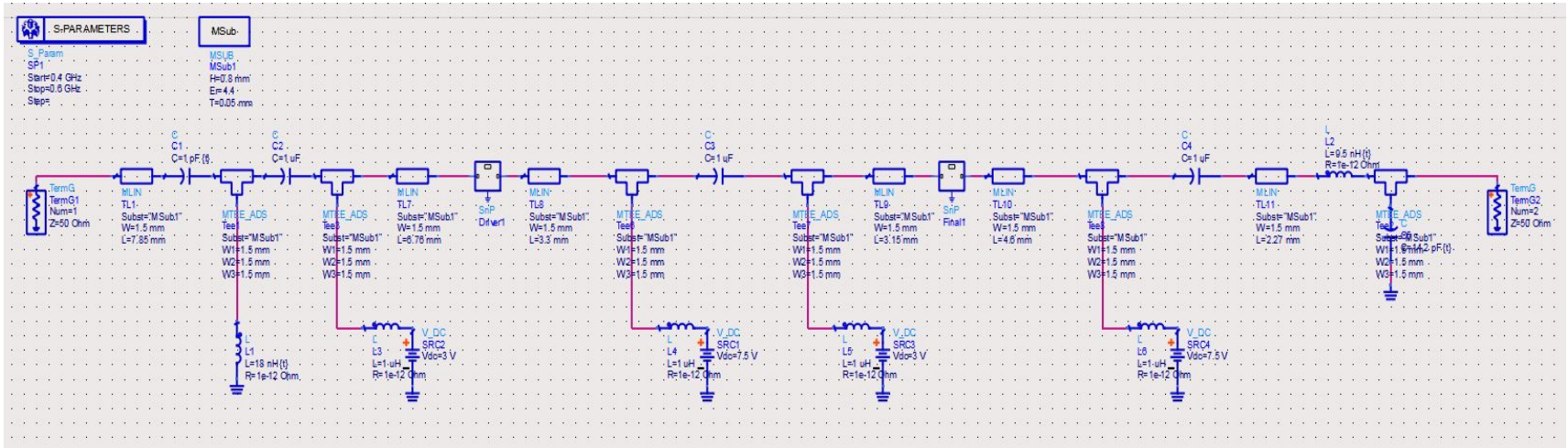
Design Step : Bias T design and simulation

AIM :

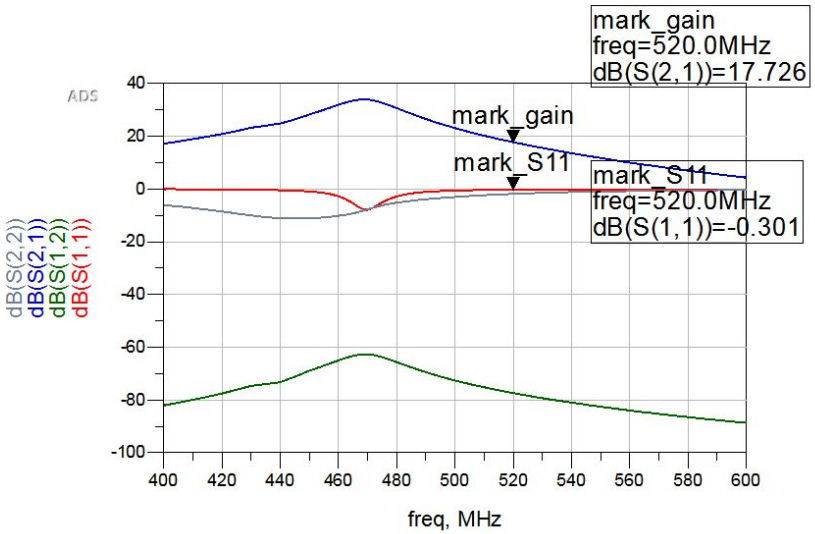
- DC bias the transistor for proper working
- Separate DC and RF signals with proper blocking

Used capacitors for DC blocking and inductors for AC short

Simulation with transmission lines



Simulation result :

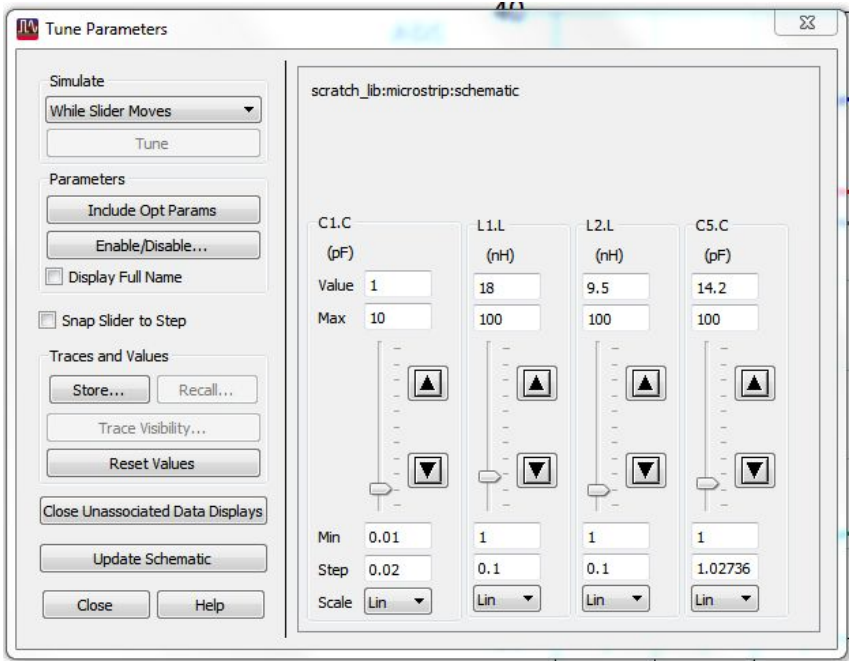


Observation:
Shift in peak frequency

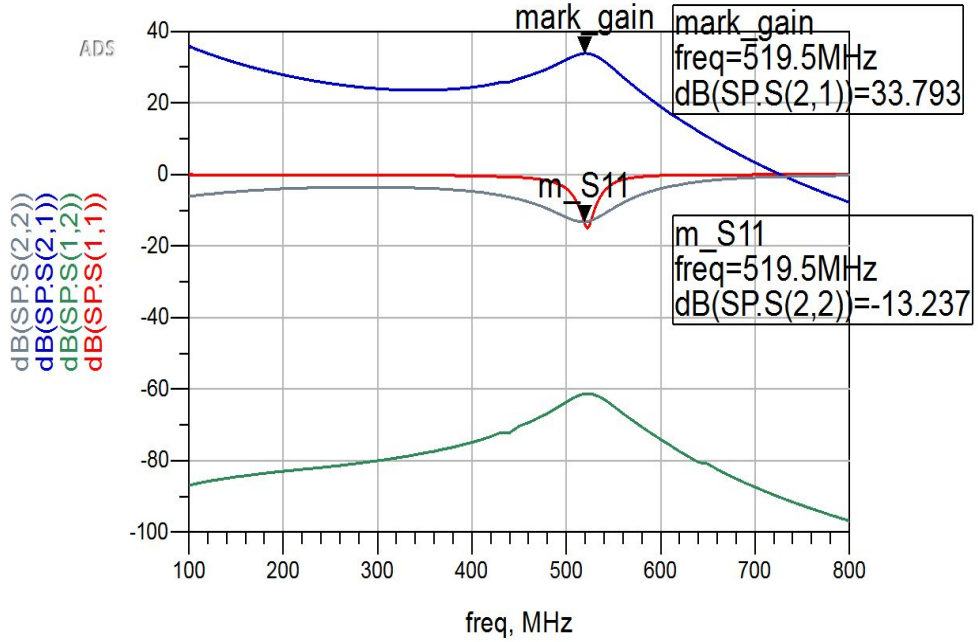
Need to tune matching network elements to get the peaks at 520 MHz

Use tuner to tune L and C values of matching circuits

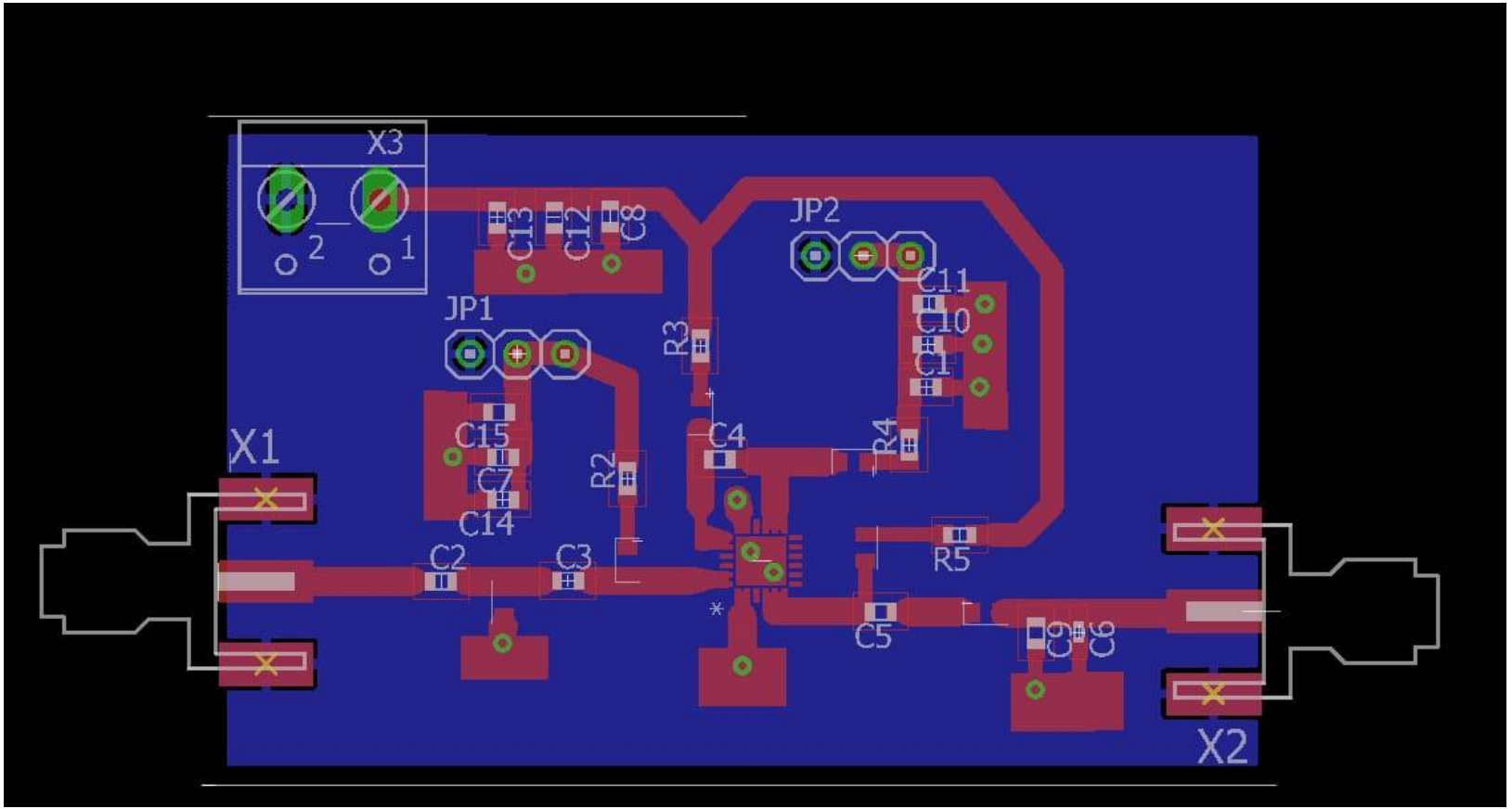
Tuner in ADS :



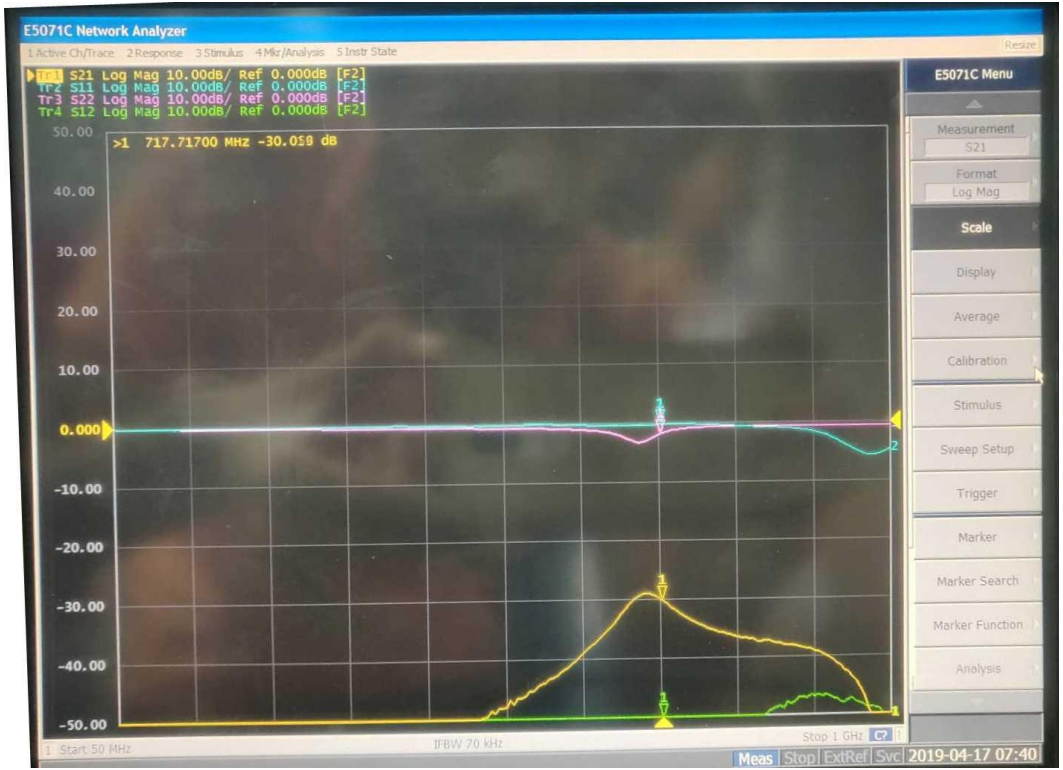
Final result after tuning :



Layout (in EAGLE):



RESULT :



Observations:

- The DC part of circuit is functioning properly.
- At Vgs= 3.3 V and Vds = 5.4V the circuit is drawing 105 mA current.
- S_{21} observed -30DB

Improvements done during testing:

- Replaced 1uH inductor with 10uH (had better SRF) to avoid RF leaking into DC.
- Added 50 Ω resistors in the drain paths.