Barrier Thickness Optimization for Silicon compatible Resonant tunnelling diode (RTD)

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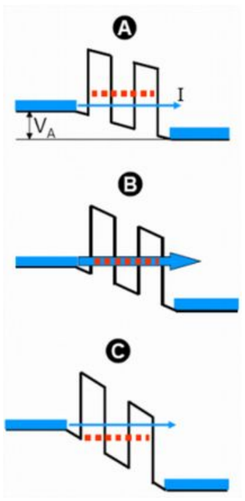
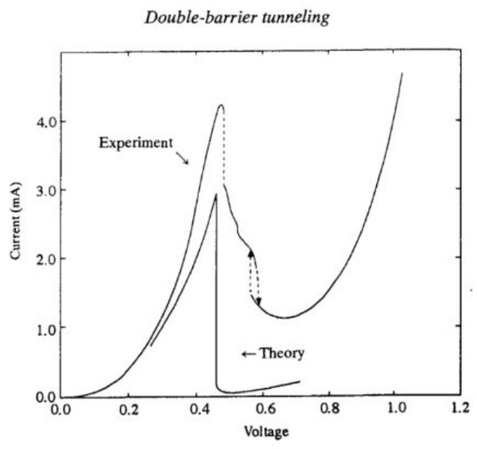
Introduction

Resonant tunneling phenomena arises from the wave nature of electrons which gives rise to energy quantization in confined structures.
Resonant tunneling effect in double barrier structure is one of the most important, since the resonant spectrum gives insight into quantized levels of electrons.
Resonant Tunneling Diode (RTD) structure is comprised of one quantum well sandwiched between two high band-gap material barriers. Due to confined well, energy band splitting occurs and conduction will happen only for the bias for which the bands are aligned. The negative differential resistance of the RTD makes the device interesting. Non-linear I-V can be used for multiple applications such as amplifiers, switches, logic gates, oscillators, detection & generation of EM waves at a very high frequency.The conduction mechanism of RTD for increasing bias is shown in the figure below, next to it is the negative differential resistance.





Background & Motivation

The most general resonant tunnelling diodes that are fabricated till date are using III-V group materials such as GaAs/AlGaAs, GaAs/AlAs etc.
Group III-V and other materials are Si incompatible. Therefore, Si or Ge based RTD will be of great interest. III-V group or any other material than group-IV based RTD have high peak current and acceptable PVR yet incompatibility with CMOS process kill their popularity. SiO2/Si/SiO2 based RTD are CMOS compatible yet have difficult fabrication process and the relative outcomes are unsatisfactory. Amorphous Si/SiO2 based RTD can also be used however, the layer thickness precision is an issue, also hydrogen passivation is required to reduce the defects. RTD behavior will be seen only at low-temperature IV measurement.

The motivation is designing a good RTD chosing group IV elements for the device rather than going for III-V elements, as they are silicon compatible and can be integrated with CMOS technology. The fabrication process should also be not so difficult and deposited layers should be crystalline, so that the interface is smooth. Moreover, we need to find a combination that works well under room temperature.

Methods

For a high performance RTD, we want it to have a high peak-to-valley ratio and steep NDR slope. For designing such an RTD, following are the requirements:

- The quantum well thickness should be optimally low (Should be at the boundary of quantum confinement) to operate it at low voltage and avoid thermionic emission
- Low band gap material must be used for quantum well to operate it at low voltage
- The tunnel barriers thicknesses should be as low as possible to increase FWHM of T*T peak and to facilitate high tunneling current
- Layer roughness should be as low as possible to avoid scattering
- Sufficient enough conduction band offset to avoid over the barrier current and therefore reduce thermionic emission current
- Transmission effective mass of electron should be as low as possible to make tunnel barrier transparent for electrons.
- All the interfaces must be H-passivated to reduce interface traps

So, by optimising all the above criterions, the most satisfactory RTD stack was $Al/Gd_2O_3/Ge/Gd_2O_3/Si/Al$. We can make smooth interface stack with uniform layer thickness in sputter. Also, the band gap of Ge is 0.67eV, so, Ge quantum well can be used. The transmission effective mass is also favourable and Gd_2O_3/Ge have sufficient band offset and therefore high barrier height so as to reduce over the barrier tunneling current and enhance the resonant tunneling current. Now we need to optimize the barrier(Gd_2O_3) thickness, which we will do by doing I-V characterization of barriers with different barrier width.

Results

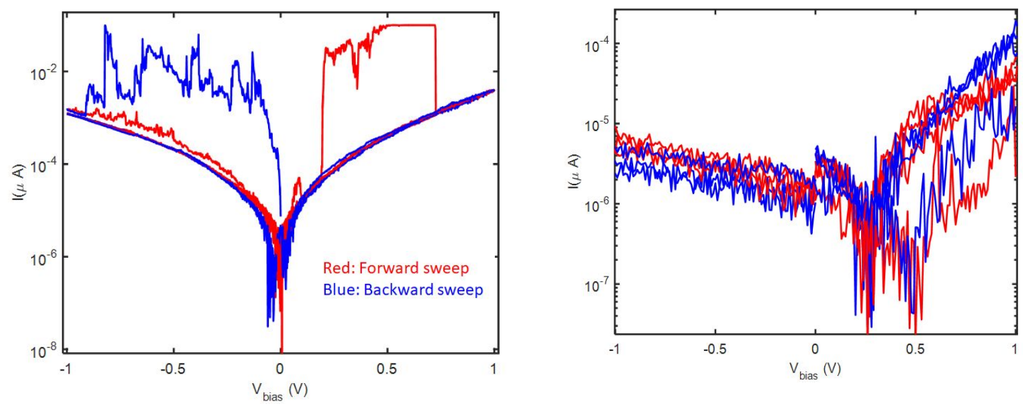


Fig.: 1. Three sweeps for 1nm Gd_2O_3 moscap.(In third sweep behaviour becomes unpredictable.)
2. Three sweeps for 2nm Gd_2O_3 moscap. (Very noisy and unpredictable I-V sweeps)

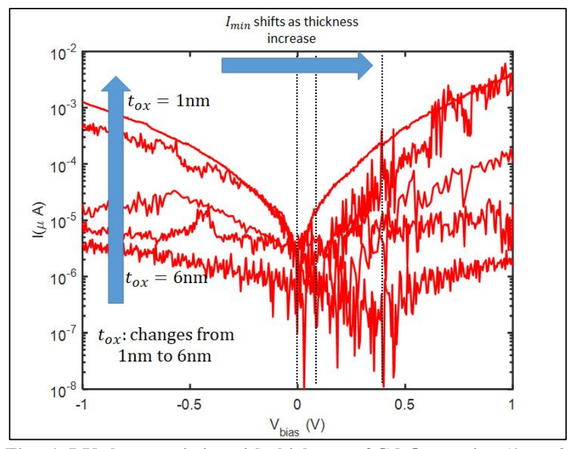


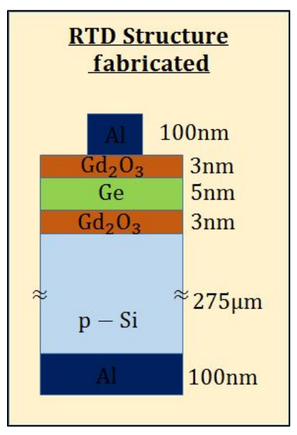
Fig.: 1. I-V characteristics with thickness of Gd_2O_3 varying (1nm-6nm)

We varied the oxide thickness from 1nm to 6nm and performed I-V characterization experiment on each of the devices.
Following are the results we get after I-V characterization of Gd_2O_3 based MOS capacitor:

- 1nm moscap had no certain consistent characteristic with the voltage sweeps, it showed random behavior in almost every new cycle.
- 2nm moscap had too much noise comparable to the measurement noise with it.
- 3nm and above had very consistent characteristics.
- As we increased the thickness, current went down as expected.
- We also observed that min. current is not at 0 bias voltage, there is a shift in I_{min} for thickness >3nm which might be due to the charge trapped in the oxide.

Conclusions

Fabrication of $Gd_2O_3/Ge/Gd_2O_3$ stack based RTD will be most suitable and is very favourable as it is silicon compatible and therefore, can be integrated with CMOS technology. The RTD shows negative differential resistance at room temperature too.
Now, we can see from the above I-V characteristics of the Gd_2O_3(Oxide insulator) that thickness below 3nm don't have consistent I-V curves probably because of the rough and uneven deposition on the surface. Therefore, even the best choice was to go for the minimum thickness oxide, we need to choose oxide greater than 2nm thickness.
For oxides greater than 3nm, we see that the current is getting very low and comparable to the noise floor. Therefore, we chose 3nm Gd_2O_3 oxide as our barrier insulator for RTD



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