

WORK EXPERIENCE AND SURVEY

Edelweiss Securities Limited, Mumbai

[May '18 - July '18]

Institutional Equities - Trading Technology Team

- Designed UX and UI for easy access to Transaction Cost Analysis(TCA) report to help traders get actionable insights to enhance and synchronize trading related execution quality, compliance and management
- Implemented login authorization, dynamic forms to query single day and multiple day TCA reports based on date, account ID, portfolio and instrument with download link to summary file on Django framework
- Created infrastructure for logging errors, warnings and regular django server information
- Reviewed and reengineered the code base for plotting transaction execution graphs using python
- Introduced features like embedding the volume traded, hover for more details and colour schemes for different algorithms to help traders compare their performance with the market more efficiently

PV Module Field survey, Leh

[June '19]

NCPRE, IIT Mumbai

- Collaborated with 2 others in PV module survey to inspect plant installations and performance degradation
- Surveyed 88 modules at 3 sites and carried out module and string level I-V characterization, IR thermography to detect hotspots and visual imaging to capture cracks on the cells
- Calculated average performance degradation rate per year to be 1.42%, 3.32% and 3.97% using MATLAB

PV Module Field survey, Leh

[June '19]

Instructor: Prof. Narendra Shiradkar, EE dept. IIT Mumbai

- Developed an online portal for 40+ students to access personalized random failure data of devices and predict the nature of failure
- Generated artificial random data for normal, weibull, lognormal and exponential distributions with varying parameters

Research and Technical Projects

VCO for 5G and NB-IoT Receivers

[May '19 - Present]

Guide : Prof. Maryam Shojaei Baghini, Electrical Engineering, IIT Bombay

Masters' Thesis

- Collaborated with 2 others in PV module survey to inspect plant installation and diagnose performance decline
- Surveyed 88 modules at 3 sites and carried out module and string level I-V characterization, IR thermography to detect hotspots and visual imaging to capture cracks on the cells
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Receiver for IRNSS

[May '17 - May '18]

*Indian Regional Navigation Satellite System (IRNSS also named as **NavIC**) is navigation satellite constellation consisting of 7 satellites, completed in April 2016 - ISRO*

RF Amplifier and Filter design for the Receiver

[May '17 - Jul '17]

Guide: Prof. Shalabh Gupta & Prof. Sibi Pillai

Research Project

- One of the **first** student project to conceptualize and fabricate a receiver for IRNSS and first step towards implementing NavIC for **civil** and **military** applications as an **indigenous** alternative to GPS
- Designed and successfully tested a PCB for signal conditioning and out-of-band noise rejection consisting of a Low Noise Amplifier (LNA), a SAW Filter and 2 stage RF amplifier

Antenna and RF Front-end for the Receiver

[Jan '18 - May '18]

Guide: Prof. Shalabh Gupta

Electronic Design Lab Project

- Designed, fabricated and successfully tested a S-band (2.492048 GHz) right hand circularly polarized (**RHCP**) dual feed patch antenna with a branch line coupler with 16 MHz bandwidth
- Designed and fabricated a **4-layer** PCB for **amplifying** and **downconverting** the received RF signal in **S-band** (2.492028 GHz) to baseband (0 Hz) using I/Q Demodulator, PLL and microcontroller
- Successfully received **navigation bits** from all satellites using our setup thereby validating the prototype

Signal Processing for the Receiver

[Jan '18 - May '18]

Guide: Prof. Rajesh Zele

Supervised Research Exposition

- Studied the signal processing block in a IRNSS receiver implemented in MATLAB to get navigation bits
- Implemented FFT based acquisition methods- code phase domain & doppler frequency domain thus decreasing the acquisition time compared to the common Serial Search technique in MATLAB
- Implemented the serial search acquisition block, digital Phase Locked Loop and Delay Locked Loop for tracking using ping-pong buffers on TM320C5515 DSP board to get navigation bits

Disbond Detection

[Oct '19 - May '19]

Guide: Prof. Siddharth Tallur

Aimed at detection of disbonds in carbon fibre honeycomb structure used in launch vehicle - Funded by **ISRO**

Prototype I

Course Project : Sensors in Instrumentation

- Designed an embedded system to sample Lamb waves on carbon fibre sheet using PWT sensors at 512 kHz by implementing a **ping-pong** buffer for real time signal processing on TM4C1294XL board using internal ADC
- Implemented real time 512 point FFT and 1-D Continuous Wavelet Transform (**CWT**) using Morlet wavelet

Prototype II

Research Project

- Designed a modular 8 channel data acquisition system with each channel capable of sampling at 4 GHz using a FPGA as buffer, which will then send the sampled data serially to a DSP board for signal processing
- Implemented the above system using A/D converter ADC121S101 sampling at 1 GHz, Cyclone IV E **FPGA** and **Nios II** processor in Platform Designer as a proof of concept
- Implemented 1-D Continuous Wavelet Transform using Morlet wavelet on TI's DSP C6678 multicore processor

Communication Subsystem, Advitiy

[May '17 - Present]

Advitiy is the 2nd student satellite of IITB, technically advanced and efficient version of the 1st, Pratham

- Converted **2-bit Frequency Shift Keying (FSK)** to **4-bit FSK** on Downlink board thereby doubling the data rates for satellite communication using transceiver **CC1101** and power amplifier
- Analyzed **data budget** and **communication protocols** to minimize redundancy and unnecessary delays thereby **improving data rate** from 1200 bits per second (bps) to 9600 bps
- Generated the **requirements** on and by the communication subsystem on other subsystems and the system for 5 payloads keeping in mind the guidelines prescribed by **ISRO**
- Programmed **On-Board Computer** to enable linear reading and writing of **EEPROM**, overcoming their inherent hardware barrier (memory arranged in different blocks)

Course Projects

VCO Design and Layout | Radio Frequency Microelectronics Chip Design

[Mar '19 - May '19]

- Awarded prize for **unique design** in Layout Design Competition judged by **industry experts** from Qualcomm
- Implemented an LC based VCO with tail noise filtering with a tuning range of 4.5 to 5.5 GHz
- Used capacitor banks and varactor for frequency tuning and achieved a low Phase Noise of -118 dBc/Hz at 1MHz Offset

Folding Flash A/D Converter Design | Mixed Signal VLSI Design

[Mar '19 - Apr '19]

- Designed 4-Bit 1GS/s Folding Flash ADC using double tail latch with offset cancellation with reference subtraction
- Designed a differential T/H circuit with dummy switches for clock feedthrough and charge-injection compensation

LNA Design and Layout | Radio Frequency Microelectronics Chip Design

[Mar '19 - May '19]

- Designed a two stage noise cancelling Common Source LNA with inductive source degeneration at 2.49 GHz

- Achieved Noise Figure of 3.2dB, DC gain of 24.9dB, Bandwidth of 100MHz, IIP3 of -10dBm and P1dB of -21.8dBm

16-bit Rational Arithmetic Unit (RAU) | VLSI Design Lab

[Mar '19 - May '19]

- Designed a 16-bit RAU capable of addition, subtraction, multiplication and division of 16-bit signed numbers
- Implemented a modified **Dadda reduction** technique for addition of partial products from **signed multiplication** of 2 or 4 numbers on Cyclone IV E FPGA thus increasing computational speed and reducing the resources required

Positions of Responsibility

Technical Secretary

Hostel 5, IIT Bombay

[May '16 - March '17]

- Awarded Hostel **Tech Colour** and **Organizational Special Mention** for display of ardent dedication
- Worked in a team of 3 and in-charge of the **maintenance** of hostel Tech Room and **management** of the inventory for the same from a budget of IRN **80,000**
- Organized hostel teams' participation in **Tech General Championships** conducted by Student Technical Activities Body (STAB) throughout the year

Technical Skills

Programming Languages	C++, Java, Python
Simulation & CAD Softwares	EAGLE, Mentor Graphics PADS, NGspice, LTSpice, Quartus, MATLAB
Libraries	OpenCV, NumPy and SciPy
Software Packages	Adobe Premiere Pro, MS-Office, Solidworks and L ^A T _E X

Relevant Courses Undertaken

Extra-Curricular Activities

- Presented different **amplifiers** in Satellites in **Ground Station Workshop** conducted by **Advitiy** for 50+ students from 15+ colleges across India towards achieving the social goal of the Project [2017]
- Won the **Best Design** Award for bluetooth controlled obstacle avoiding bot in **XLR8 2015** [2015]
- Actively **volunteered** in Green Campus, **National Service Scheme**, IIT Bombay for conservation of plant species in the institute [2015]
- **Directed** and **edited** music videos for **Inter-Hostel Competition** [2015]
- Led the school **Cricket** team and represented school in **Table Tennis** inter-school tournaments. [2013]