# Schematic Design Review Checklist

| Style | Status (Checked/Not Checked) | Remarks |
|---|---|---|
| Do you have used the correct schematics template? | | |
| Title block for all the pages? | | |
| Are all schematic sheets the same size? | | |
| Do nets have a net name for understanding? | | |
| Are nets consistently net-named? | | |
| Are power ports properly named? | | |
| Does the schematic design compile and pass design rules without errors? | | |
| Is there a change list or revision list, that is mentioned in the correct page design change list section? | | |
| Are all components aligned to the grid, and are all the net wires correctly connected to each pin? | | |
| Can groups of off-sheet connections be grouped into a bus? | | |
| The net named signals only used in the page? | | |
| Do all components have the correct designators? (i.e.: You annotated the schematic)? If it is a revision board old designators are maintained? | | |
| **General** | **Status** | **Remarks** |
| CAD ERC was 100% clean. If some warning/errors are accecptable, each warning/errors must be inspected and signed off as invalid. | | |
| Verify PINs of all connector's with respect to the EICD (if not yet board proven). | | |
| The schematic symbol matches the chosen component package(if not yet board-proven). | | |
| Thermal pads are connected to the correct Power rail/Ground (may not always be ground) | | |
| Debug interfaces should be 'ON' always. | | |
| Verify the PIN of all cables to other boards in the system (straight vs mirror).ICD must be verified and signed off. | | |
| **Passive Components** | **Status** | **Remarks** |
| Power/voltage/tolerance ratings specified or displayed as required | | |
| Derating values are in the limit. | | |
| Polarized components polarity check. | | |
| **Usability/Testing** | **Status** | **Remarks** |
| Is there an LED for each power rail? At least for the input? | | |
| Are there test points for each power rail? | | |
| Are there test points for critical signals/signals of interest? | | |
| **Production** | **Status** | **Remarks** |
| Can any component values be merged to reduce BOM line items? Is BOM optimization done? | | |
| Is only one part number specified for each passive component value with a specific size? If the used component is critical,mentiond the alternate for that. | | |
| Check that each symbol has a manufacturer and part number assigned. | | |
| Are all components active production, and not end-of-life/discontinued/not recommended for new designs at the time of the schematic review? | | |
| Are all the selected components industrial/automotive/Mil-grade? | | |
| Does each component have sufficient stock in the supply chain? | | |
| **Connectors** | **Status** | **Remarks** |
| Check that I/O pins have a pull-up or down to define their default state when disconnected. | | |
| Connector pin pitch and the position in footprint is checked? | | |
| Ensure there is a decoupling capacitor for each power pin on the connector.Smaller,medium and bulk capacitors are there. | | |
| Do cables need to be rugged? | | |

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| Do long cables need to be isolated for EMC? | | |
| **Components** | **Status** | **Remarks** |
| Check all symbol pinouts against the datasheet, even if you have used the IC before or trust the symbol source. | | |
| The Capacitor's voltage rating is at least twice the maximum expected voltage. | | |
| Have you checked the current passing through each resistor for power dissipation? | | |
| Is each resistor’s voltage rating sufficient for the maximum voltage applied (mostly relevant to 0402 and smaller sizes)? | | |
| Have all the current limiting resistors been correctly calculated for each LED's forward voltage? | | |
| Have all the current limiting resistors been correctly calculated for each optoisolator forward voltage? | | |
| Do reset/enable pins need external pull-up or pull-down resistors? | | |
| Are any potentially floating pins pulled up or down with external resistors? | | |
| Are any pins with a state that is critical at power up externally pulled up or down? | | |
| Are the JTAG programmer header's pitch and onboard header's pitch are same? | | |
| Programming header is there for all the programmable devices? | | |
| Is each operational amplifier and comparator connected with the correct polarity? correct voltage is applied? | | |
| Check for the correct polarity of each diode or LED. | | |
| **Power** | **Status** | **Remarks** |
| Every power pin of every IC should have a decoupling capacitor. | | |
| Has each switched mode voltage regulator been simulated to ensure it is stable across all load conditions? | | |
| Power analysis has been done? | | |
| Do multiple voltage rails need sequencing? | | |
| All power inputs fed by correct voltage value? | | |
| Do you need a reset supervisor IC on any devices if a regulator has a soft start? | | |
| Has Power Tree been prepared for the board? | | |
| Digital and analog ground separated with ferrite bead. | | |
| Check and add an inrush limiter(Soft start capacitor) if needed. | | |
| Board ground and earth ground are separated with an isolation circuit. | | |
| Any isolation is required in the power input section? Isolated regulator to be used? | | |
| Core voltage for on board main IC is generated from the same board? | | |
| Does each voltage regulator’s output meet the requirements for the ICs connected to it? | | |
| Is the total capacitance connected to each regulator within its ability to supply? | | |
| Is there sufficient input capacitance on each regulator to prevent reverse supply under changing loads? | | |
| Are any input voltages to regulators able to drop below the regulator’s minimum operating voltage? | | |
| Option to isolate the voltage from the board ICs? | | |
| Are any input voltages to regulators able to exceed the regulator's maximum voltage? | | |
| Sink and Source regulator is used for DDR memories? | | |
| Decoupling meets/exceeds vendor recommendations if specified | | |
| Bulk decoupling present at PSU | | |
| Voltage regulator's load current,ouput voltage, switching frequency is mentioned? | | |
| Is there a LDO between any devices that need extremely clean power (e.g.: operational amplifiers )? | | |
| **Signal** | **Status** | **Remarks** |
| Have amplifier circuits been simulated to ensure they are stable? | | |
| Have all voltage dividers been re-calculated to ensure the output voltage is correct? | | |
| Is there capacitance and/or a Zener diode on the output of each operational amplifier? | | |
| Signals are correct logic level for input pin | | |
| DC analysis for the board performed? Signed as valid from senior. | | |

| | | |
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| Pullups on all open-drain outputs? | | |
| Pulldowns on all PECL outputs? | | |
| Termination of all high-speed signals | | |
| AC coupling caps on gigabit transceivers | | |
| TX/RX paired correctly for UART, SPI, MGT, etc.. | | |
| Are differential pairs correctly connected with respect to the IC's datasheet pin function? | | |
| Are differential pairs correctly identified with _P and _N signals? | | |
| Active high/low enables signal polarity to correct | | |
| I/O banking rules met on FPGAs etc | | |
| RC time constant for attenuators same given ADC sampling frequency | | |
| Verify the frequency response of RF components across the entire operating range. Don't assume a "1-100 MHz" amplifier has the same gain across the whole range. | | |
| Verify the polarity of op-amp feedback | | |
| When using auto-sensing level shifters, ensure the intended receiver doesn't have a pullup/down | | |
| Are all signals feeding into logic devices within the maximum voltage rating? | | |
| **EMI/EMC/Protection** | **Status** | **Remarks** |
| Does every externally accessible connection/exposed piece of metal have adequate ESD protection?<br>Connector pins<br>Connector housings<br>Metal shields on buttons<br>Pins of buttons<br>Displays<br>Potentiometers/dials<br>Card socket pins<br>Metal card housings | | |
| Does the input power require a fuse to protect upstream devices? | | |
| If EMI/EMC Compliance mentioned in the requirements of the product should have the EMI Filter. | | |
| Is the input power protected against reverse polarity? | | |
| Is there overvoltage protection on the power input? | | |
| Is there overcurrent protection on the power input? | | |
| Are there current limiting resistors on nets from external devices to sensitive devices (e.g.: microcontroller pins) | | |
| Do all optoisolators have parallel resistors/capacitors with their diode for noise immunity? | | |
| Is there input under-voltage protection? | | |
| Is there short circuit protection on each voltage rail that has an external connection/output? | | |
| Does every switching regulator have a sufficient input filter to prevent conducted EMI from escaping on its input? | | |
| Pullup/pulldowns on all signals that need a defined state at boot | | |
| Strap pins connected to the correct rail for the desired state | | |
| JTAG/ICSP connector provided for all programmable devices | | |
| Config/boot flash provided for all FPGAs or MPUs without internal flash | | |
| Reference resistor's correct value and reference rail | | |
| Power outputs (USB etc) are current limited | | |
| ESD protection on data lines going off-board | | |
| Are MOSFETs protected against voltage transients with external diodes? | | |
| **Clocks** | **Status** | **Remarks** |
| All oscillators meet the required jitter/frequency tolerance. Be extra cautious with MEMS oscillators as these tend to have higher jitter. | | |
| Correct load caps provided for discrete crystals | | |
| Crystals are only used if the IC has an integrated crystal driver | | |
| Banking/clock capable input rules met for clocks going to FPGAs | | |

| Regulators | Status | Remarks |
|---|---|---|
| Under/overvoltage protection configured correctly if used | | |
| Verify estimated power usage per rail against regulator rating | | |
| Current-sense resistors on power rails after regulator output caps, not in the switching loop | | |
| Remote sense used on low voltage or high current rails | | |
| The regulator's input and output capacitors, diode, and ferrite bead power rating/voltage/size are mentioned. | | |
| The power sequencing tree is provided and explained. | | |
| Power tree for the system is provided? | | |
| Linear regulators and voltage reference ICs are stable with selected output cap ESR | | |
| Source and destination voltage names are correct? There is no spelling mistake. | | |
| Confirm power rail sequencing against device datasheets | | |
| **ERRATA** | **Status** | **Remarks** |
| Read errata sheets (if available) for all major and newly developing devices | | |
| Newly developed design section verified with the manufacturer? | | |
| **Debugging /Rework ability** | **Status** | **Remarks** |
| Use 0-ohm resistors vs direct hard-wiring for strap pins when possible | | |
| Provide multiple ground clips/points for scope probes | | |
| Dedicated ground close to analog test points | | |
| Test points on all power rails | | |
| Test points on interesting signals that may need probing for bring up/debug | | |
| **Thermal** | **Status** | **Remarks** |
| Power estimates for all large/high-power ICs | | |
| Thermal calculations for all large/high-power ICs | | |
| Specify heatsinks as needed | | |