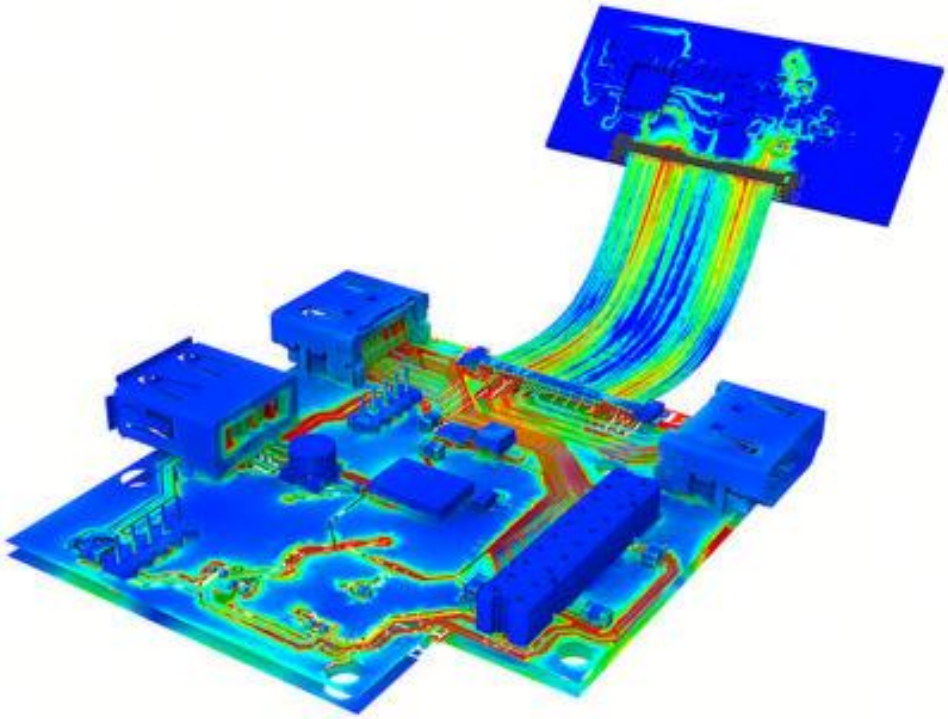
EMC GUIDELINES FOR PCB



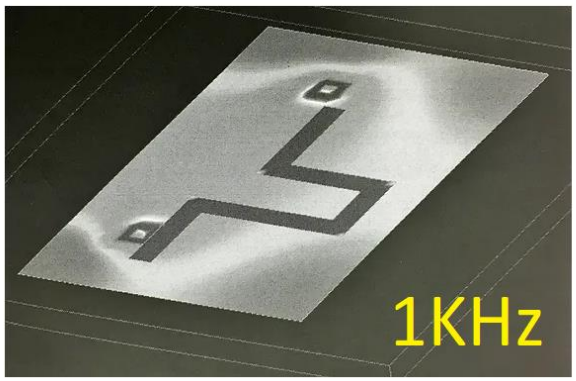
Source- Ansys

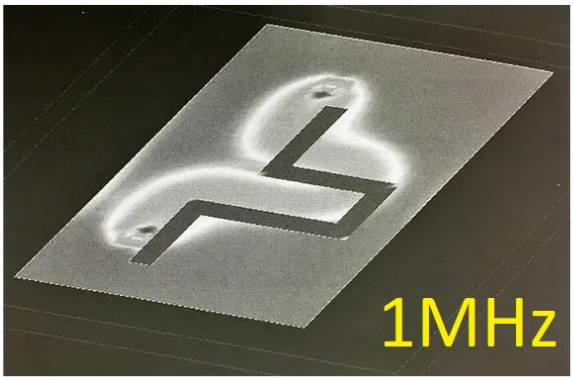
Introduction

We try to avoid the terms ground plane and GND plane in our guidelines. Whenever appropriate, we use the terms signal return plane or return signal reference plane or simply: reference plane. Why is this?

Currents flow in loops. A current does always return to its source. And a common issue is that engineers tend to forget about this when they design PCBs and electronics systems, especially when they design digital systems where you can only see the signal traces from chip to chip and the return current flows through the "GND symbols" in the schematic. The majority of EMC problems (e.g. radiated emission, ESD) involve high-frequency signals (several megahertz - MHz). It is important to understand that a return current of a signal above about 50kHz prefers to flow close to the forward current, e.g. directly under the forward current in an adjusted power supply or ground plane - the so called return signal reference plane.

The following two impressive images compare the return currents through a reference plane of a low-frequency signal vs. a high-frequency signal (source: EMI Troubleshooting Cookbook for Product Designers). In the left picture, the signal has a frequency of 1kHz and in the right 1MHz. The difference is obvious and eye-opening! So lets get started with the guidelines and learn more about EMC compliant design.



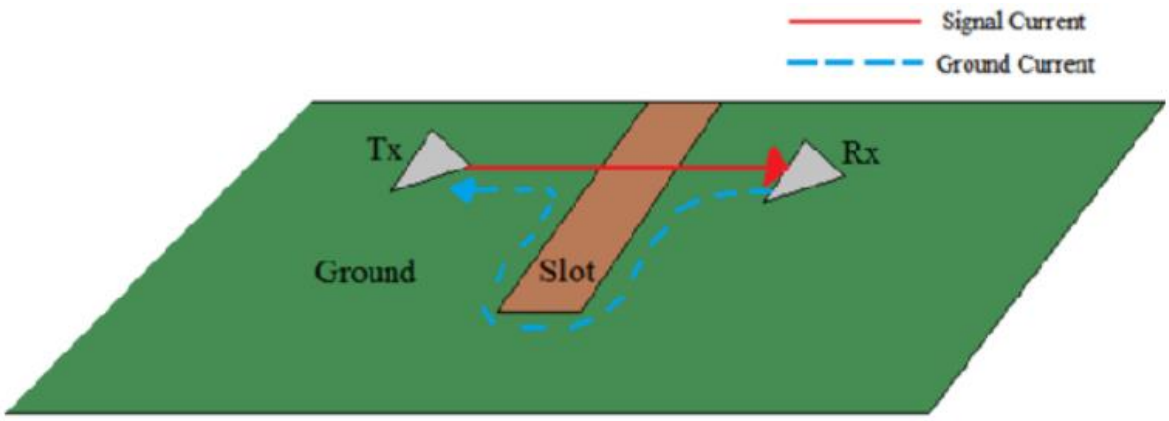


EMC Design Guidelines

EMC Guideline # 1 – Never route signals over split reference planes!

Reduce Radiated Emission

Do not route signals over split return signal reference planes (GND, power planes)! Never! This leads to unnecessary large current loops (as the current return cannot flow directly under/beside the forward current) and large current loops in general lead to high radiated emission values.



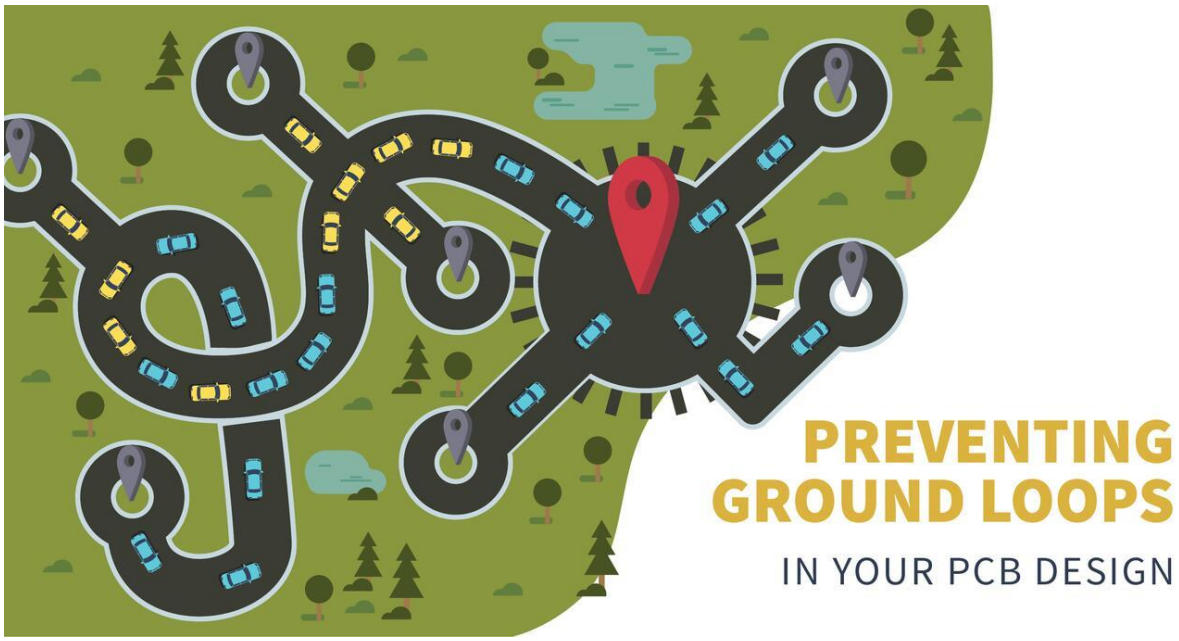
Rule Of Thumb #1: Whenever in doubt, do not split return current reference planes (GND, power planes), go with a solid filled reference plane instead. There must be a good reason for splitting planes! There should always be at least one solid reference plane closely adjusted to signals.

EMC Guideline #2 – Keep current loops as small as possible.

Reduce Radiated Emission

Always consider the return current! Always! And with the return current in mind: minimize the loop you have between forward and return current. This is especially true for high-frequency signals (several MHz),

This is a very generic guideline and should always be kept in mind. Out of this guideline, many others will follow here in a more specific way.

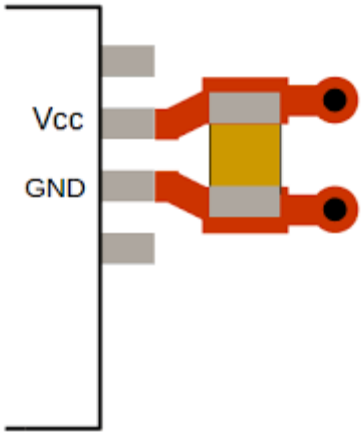


Hint #1: We assume that you have a high-frequency signal (s1, >1MHz) trace on layer 1 and a reference plane (e.g. GND or power plane) on the neighbour layer 2, the return current of the high-frequency signal (s1) on the reference plane prefers to flow directly under the trace of s1.

EMC Guideline #3 – Decoupling: use low-inductance capacitors / traces AND planes.

Reduce Radiated Emission, Reduce Impedance Coupling

Decoupling is important! Always consider decoupling! Place ceramic capacitors close to EVERY power supply pin of EVERY chip on your PCB design.



Hint #2:

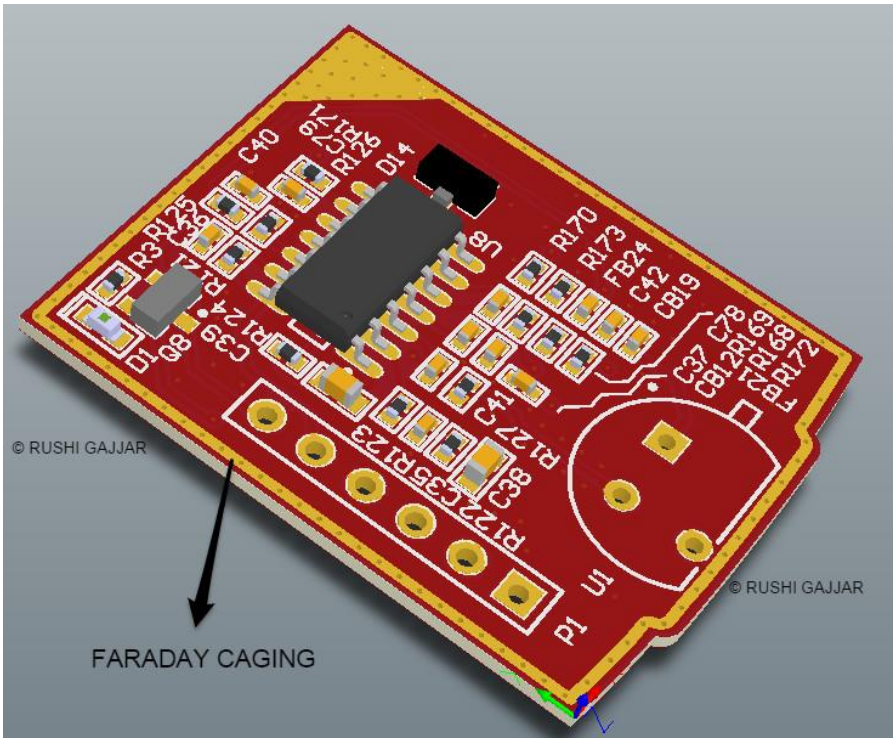
Decoupling depending on PCB stackups:

- Multilayer PCB: Design a PCB stackup with power supply plane and GND plane close together (<0.1 mm or 2...3 mils). This leads to an especially good decoupling at high frequencies (>1MHz).
- Double/single layer PCB: Keep traces of decoupling capacitors to power-supply-pin and ground-pin as short as possible (to keep inductance as low as possible).

EMC Guideline #4 – Use ground planes on PCB for shielding.

Reduce on-board Interferences.

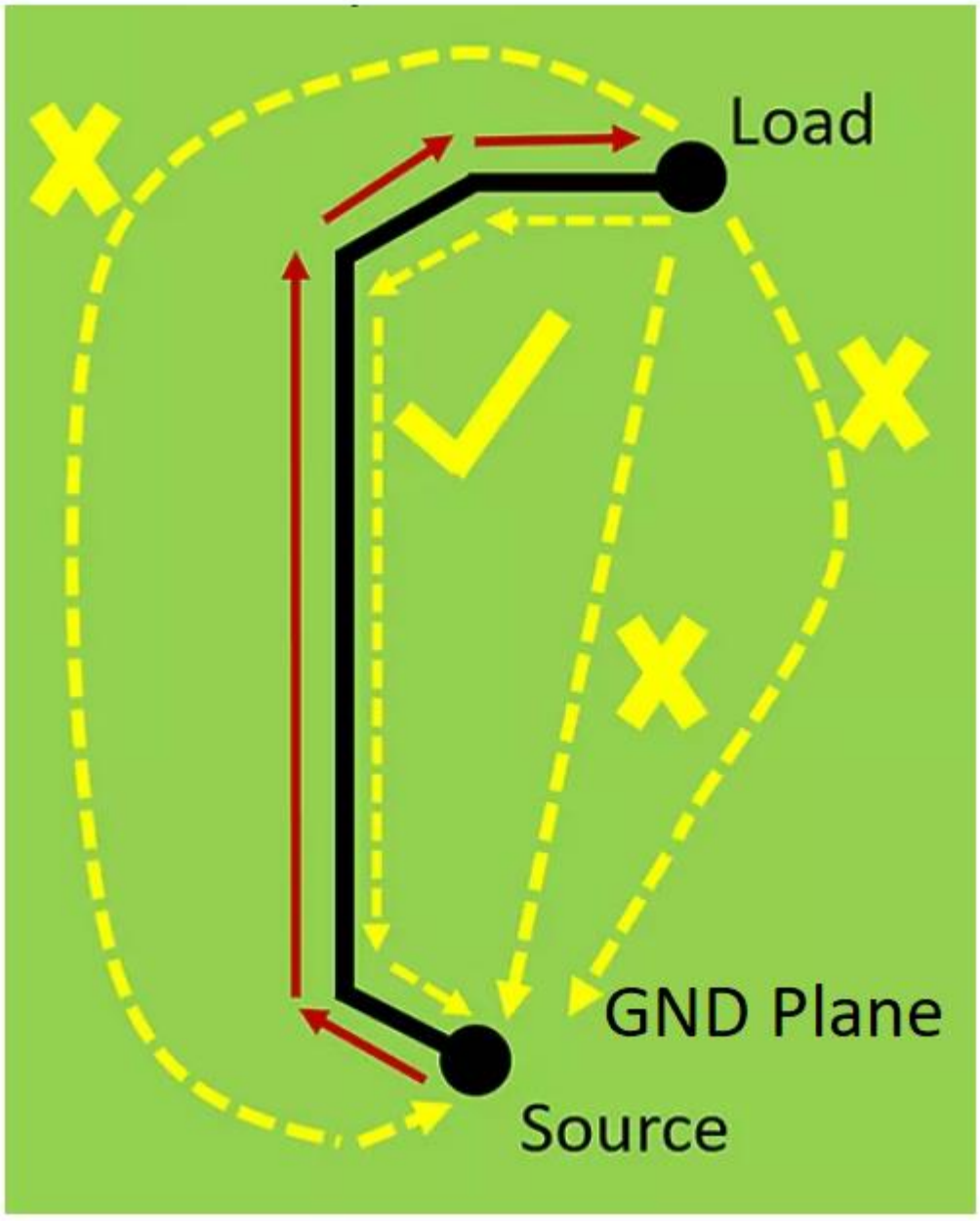
Use solid filled reference planes (e.g. GND or power supply planes) on a PCB to separate noisy signals (e.g. motor signals) from sensitive signals (e.g. sensor signals). The reference plane will act as a shield and will lower Electromagnetic Interference (EMI). Be aware, that the shielding of such a copper plane will primarily be effective for E-fields and not H-field, because copper has a low µr and does not shield against (low-frequency) magnetic fields.



EMC Guideline #5 – Route high-frequency signals adjusted to a plane.

Reduce Radiated Emission

This guideline follows out of EMC Guideline #1 and EMC Guideline #2: route high-frequency signals (>50kHz) ALWAYS closely to an adjusted reference plane (GND or power supply plane, which acts in this case as a high-frequency ground). For single layer designs: use guard traces close to the high-frequency signal where the return current can flow.



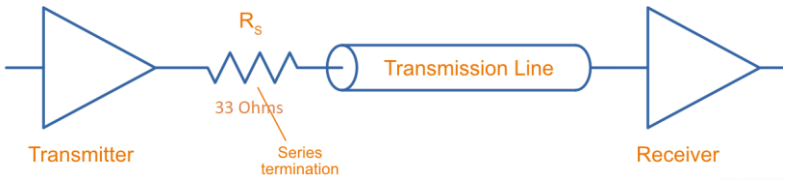
Hint #3: Generally, core laminate is more reproducible than prepreg regarding thickness and dielectric constant. This means that controlled impedance layers should ideally be routed along the core material, rather than prepreg.

EMC Guideline #6 – Control rise and fall time.

Reduce Radiated Emission

Increase rise- and fall time of any digital signal (especially clock signals) as far as possible.

Rule Of Thumb #2: Add a series resistor (typically 33 Ohm, close to the driver's output) to all digital signal traces with signal length [inch] higher than rise-/fall-time [nsec].



Rule Of Thumb #3: The approximately highest frequency content in a digital signal depends NOT on the first harmonic (fundamental frequency), it depends on the rise/fall-time:

$$f_{knee} = \frac{0.35}{t_{10\%-90\%}}$$

Where t10%-90% is the rising- or fall-time from 10% to 90% of the slope of a digital signal in [sec] and fknee is the maximum frequency content in [Hz].

Example: Given a digital clock with rise/fall-time of t10%-90%=1nsec which runs over a PCB microstrip trace which has a length of 250mm (10inch). The highest frequency content in this digital signal is approximately fmax=fknee≈350MHz and has a wavelength of λ≈v/fknee=500mm, where v is the propagation velocity of the electromagnetic wave inside the signal PCB media and air (typical dielectric constant εr=4.5 for FR-4 and an effective dielectric constant of εreff≈3.0 for the assumed microstrip line):

$$\lambda = \frac{v}{f} = \frac{c}{f} \cdot \frac{1}{\sqrt{\varepsilon_r \cdot \mu_r}} = \frac{c}{f} \cdot \mathrm{VF}$$

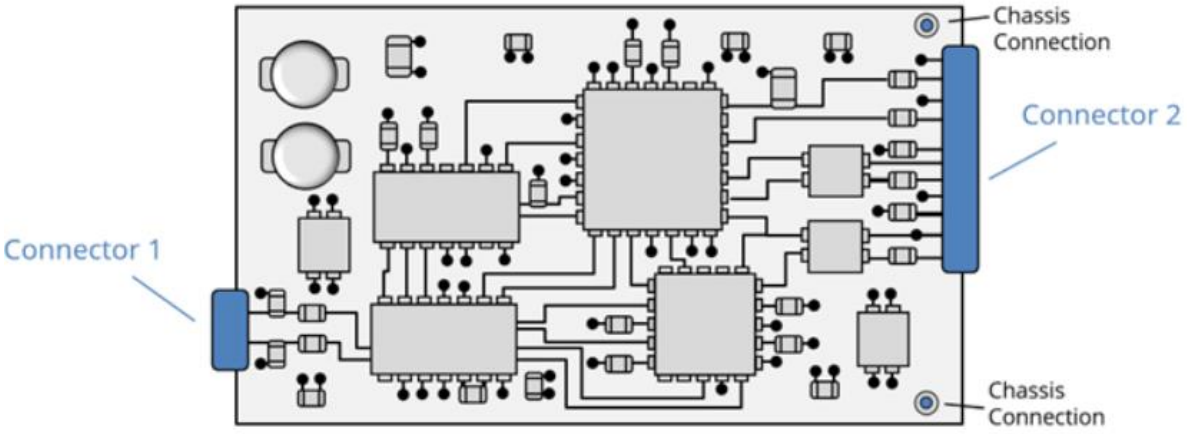
The digital clock signal with a rise/fall-time of 1nsec running through a trace on a PCB with FR-4 material results in λ/2=250mm and λ/10=50mm for fmax. Given all these facts, the PCB trace of length 250mm will tend to radiate at high levels (because a trace length or cable of length λ/2 makes a good antenna). To prevent this: add a series resistor close to the drivers output which will lower the rise/fall-time.

Rule Of Thumb #4: Every PCB trace of length longer than λ/10 should be considered as a transmission line and no longer as a simple interconnection. This means that such a trace should be laid out with controlled impedance. In other words: there should not be any impedance changes / discontinuities along the PCB trace, as these impedance changes / discontinuities lead to e.g. reflections. Reflections affect the signal integrity.

EMC Guideline #7 – Add ceramic capacitors close to every pin of a connector.

ESD, Reduce Radiated Emission, Increase Radiated Immunity

Filtering of signals directly at the connector is very important! This helps to add Electrostatic Discharge (ESD) immunity to your PCB, lower radiated emission and increase immunity to coupled burst signals on IO cables.



Every signal or power supply line which enters or leaves your PCB needs a ceramic capacitor. One side of the capacitor close to the connector pin, the other pin tied to the ground plane. Some rules of thumb:

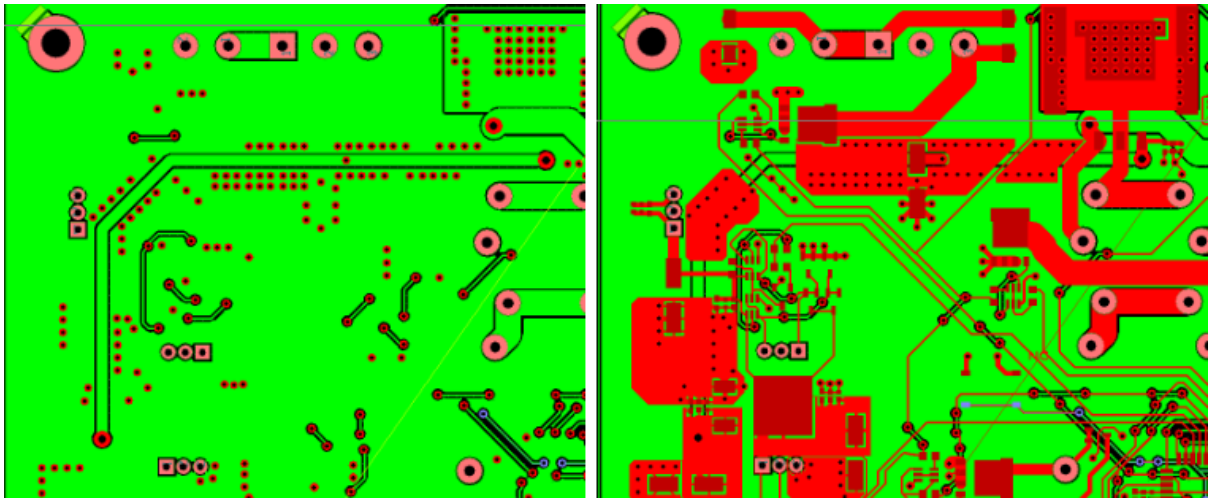
Rule-of-thumb for EMC, EMI, ESD capacitors as IO-filters	Maximum signal bandwidth (not fundamental frequency, bandwidth!)
≥ 100 nF	DC (power supplies)
1 nF	< 0,1 MHz
100 pF	< 0,1...1 MHz
10 pF	< 1...10 MHz
Transient voltage suppressor diode (TVS)	> 10 MHz

Hint #4: Signals which go outside your device (e.g. a connector which people can touch with their hands), will be tested with an ESD gun (±2kV, ±4kV, ±6kV, ±8kV). In this case, use capacitors with high voltage rating (e.g. >250V, depending on capacitance and ESD test voltage and other components involved, e.g. like ferrite beads between connector pin and capacitor).

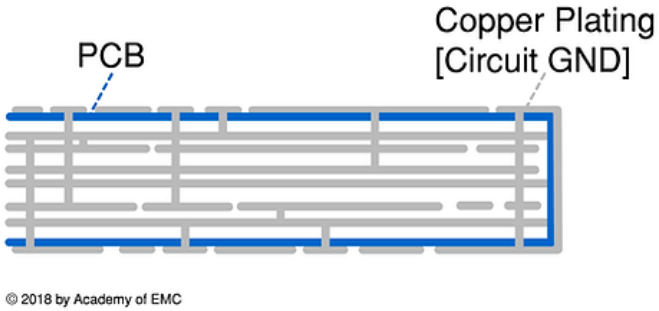
EMC Guideline #8 – Fill top and bottom layers with circuit GND and metalize the PCB edges.

Reduce Radiated Emission

Fill top and bottom layers of a PCB with a solid ground plane around the signals (copper area) and metalize the PCB edges. This helps to minimize radiated emission, because the filled GND areas at top and bottom help to shield inner-layer signals from radiation. Moreover, the filled copper areas help to maintain a low impedance return current path and therefore short current loops. However, do not forget to place a grid of ground stitch vias throughout the whole PCB (otherwise some small copper islands may radiate)! This is very important! Read about the distances between the vias below in Rule Of Thumb #5.



Plated PCB outside edges (which are connected to circuit GND) help to prevent the inner PCB layers from radiating. Moreover, the plated PCB edges help to increase cooling efficiency of a PCB, because there is an additional copper surface where heat exchange can take place. The additional costs for metalized PCB edges are low.



Rule Of Thumb #5: It is best practice to add a grid of ground stitch vias over the whole PCB (when filling top and bottom layers with a ground plane). Otherwise, some small GND copper areas would tend to radiate! The distance between these vias within that grid depends on the highest frequency fmax on the PCB. Given a signal with wavelength λ, it is a rule of thumb that a stub or trace of the length of λ/10 starts to become a problem (regarding radiation) and a trace of length λ/20 won't be a problem (in between λ/10 and

λ/20 is a gray area). Therefore, the distance between the vias should be shorter than λ/10 of fmax. The wavelength λ of a sinusoidal signal running through a PCB signal trace is.

$$\lambda = \frac{c}{f \cdot \sqrt{\varepsilon_r}}$$

Where λ = wavelength [m], c = speed of light [3E8 m/sec], f = frequency [Hz] and εr = permeability [1] of the PCB material (e.g. typical εr=4.5 for FR-4 and e.g. εr=2...11 for special high frequency (f > 2GHz) PCB materials, where an isotropic and stable dielectric constant is needed over a wide frequency-range, temperature-range and every PCB-lot).

But how to determine fknee = fmax or λ/10, respectively? Usually, the highest frequencies occur in digital signals with small rise/fall-time, especially clock signals. A good estimation gives our Rule Of Thumb #3 with:

$$f_{knee} = \text{bandwidth} = \frac{0.35}{t_{10\%-90\%}}$$

The following table shows some example values of high frequency digital signals rise/fall-time and its corresponding highest frequency content and λ/10 values (the recommended distance between vias of the grid of vias is <λ/10).

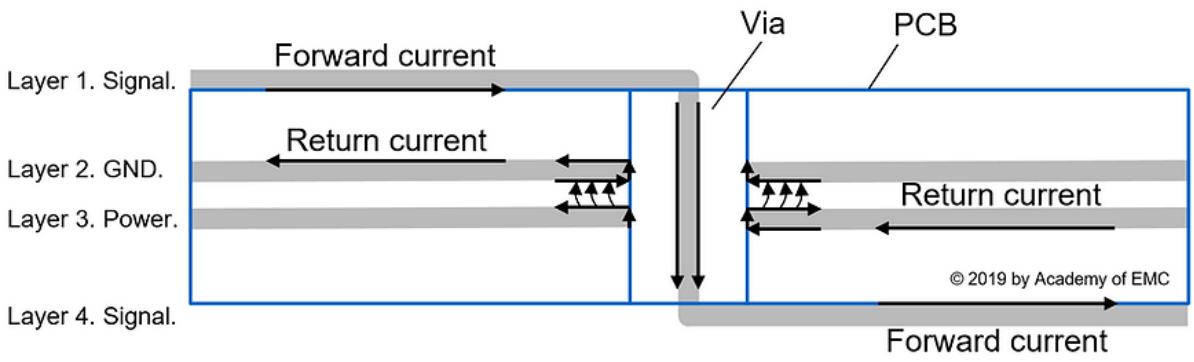
Smallest rise/fall-time on the PCB [nsec]	Highest frequency f_{max} on the PCB	$\lambda/10$ for ε_r=3,5 (**ceramic+PTFE**) [mm]	$\lambda/10$ for ε_r=4,5 (**FR-4**) [mm]	$\lambda/10$ for ε_r=6 (**HF-laminate**) [mm]	$\lambda/10$ for ε_r=11 (**HF-laminate**) [mm]
500	0.7 MHz	22908	20203	17496	12922
200	1.75 MHz	9163	8081	6999	5169
100	3.5 MHz	4582	4041	3499	2584
50.0	7 MHz	2291	2020	1750	1292
20.0	17.5 MHz	916	808	700	517
10.0	35 MHz	458	404	350	258
5.00	70 MHz	229	202	175	129
2.00	175 MHz	92	81	70	52
1.00	350 MHz	46	40	35	26
0.50	700 MHz	23	20	17	13
0.20	1.75 GHz	9.2	8.1	7.0	5.2
0.10	3.5 GHz	4.6	4.0	3.5	2.6
0.05	7 GHz	2.3	2.0	1.7	1.3
0.02	17.5 GHz	0.9	0.8	0.7	0.5
0.01	35 GHz	0.5	0.4	0.3	0.3

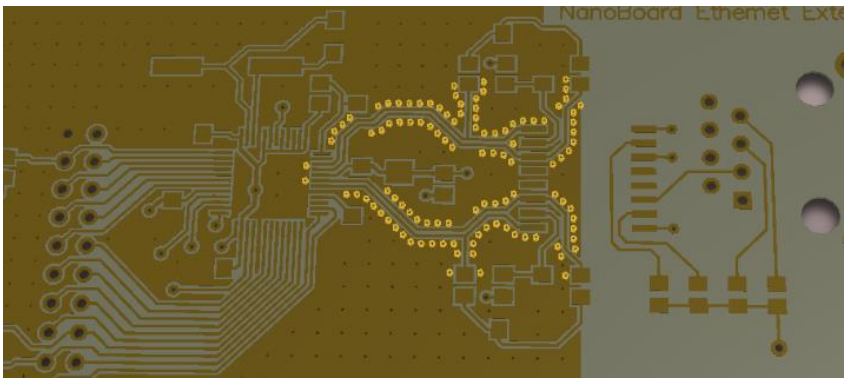
EMC Guideline #9 – Add stitching vias around high-speed signal vias.

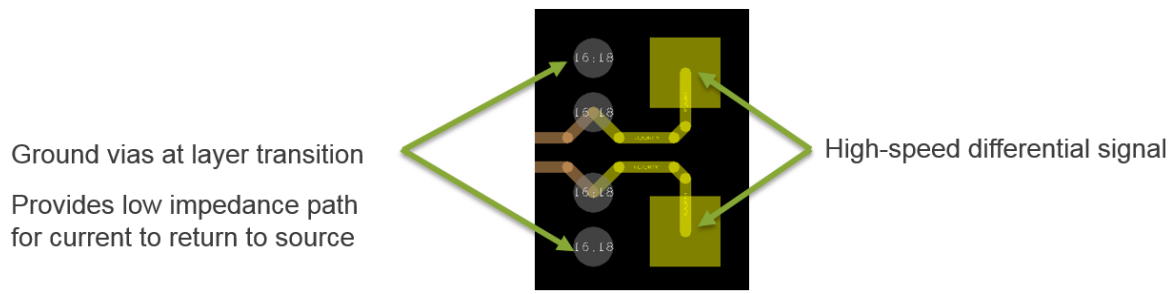
Reduce Radiated Emission

This guideline follows directly out of EMC Guideline #2. Imagine the following scenario: a high-speed signal switches planes on a PCB. In order to minimize ground bounce, you have to minimize the return current path. There are these two options, depending on the return current path:

- **Identical return current reference nets**. In case the two planes have the same reference net with the identical electrical potential (e.g. GND), add two or three stitching vias (between the reference planes) close to high-speed signal via. These stitching vias help to keep current loops as small as possible.
- **Different return current reference reference nets.** In case the two reference planes are DC isolated, make sure that the two reference planes are coupled with the lowest impedance possible. This can be achieved with the thinnest possible dielectric layer between them (see the picture below)



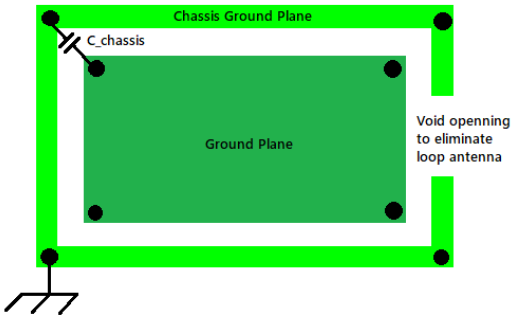




EMC Guideline #10 – Connect circuit GND to chassis at IO area.

Reduce Radiated Emission, Conducted Immunity, ESD

Do not think this guideline is not important, just because it isn't listed at first place! This guideline is essential! Bound your circuit GND to chassis at the area where your cable leaves/enters the chassis. Connect it with VERY LOW impedance!



It is important that GND and chassis have the same potential at the IO area:

- This prevents radiation, as the GND shows a minimum voltage difference to the chassis (earth).
- This helps your IO-signal-filters on your PCB (see EMC Guideline #7) being most effective and keeps ESD pulses away from your circuit. Why? Because incoming noise (burst, ESD) from the cable can directly flow back over chassis to earth.

References

www.academyofemc.com
www.ti.com
www.altium.com

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