

## SPI

1. Who designed SPI?  
⇒ SPI was designed by Motorola.
2. What is the full form of SPI?  
⇒ Serial Peripheral Interface.
3. How many wires are used in SPI communication?  
⇒ SPI is a 4-wired communication protocol.
  - a) Master out, Slave in (MOSI)
  - b) Master in, Slave out (MISO)
  - c) Serial clock (SCLK)
  - d) Chip select / Slave select (CS/SS).
4. Is SPI Half duplex (or) Full duplex?  
⇒ Full duplex.
5. Is SPI Synchronous (or) asynchronous communication?  
⇒ Synchronous communication.
6. What is the standard speed of SPI?  
⇒ Upto 10 Mbps.
7. What is the main feature of SPI communication?  
⇒ SPI is Multi-Slave Communication protocol.
8. What is the byte order in SPI?  
⇒ LSB First (or) MSB first. It depends on SPI device connected to master.
9. How many slaves can be connected in SPI?  
⇒ Maximum number of slaves are limited by the hardware. It is not restricted in the protocol.
10. Name some SPI devices?  
⇒
  - 1) Micro SD Card
  - 2) Digital pressure sensor
  - 3) Digital Accelerometer.
11. What is the role of shift registers in SPI communication?  
⇒ In SPI, shift are used to transfer the data to slave using the MOSI bus and at the same time receiving the dummy data from MISO bus and vice versa.
12. What is the clock polarity and clock phase in SPI?  
⇒ Clock polarity represents base value of the clock.  
Clock phase represents on which edge data to be sampled.
13. What are the advantages of SPI?  
⇒
  - 1) Full duplex communication
  - 2) Simple hardware interfacing
  - 3) Not limited to 8 bits word in case of bit transferring
  - 4) No arbitration
  - 5) No start and stop bit, so that data can be transferred without any disturbance.



14. What are the Dis-advantages of SPI?

- ⇒
- 1) No form of Error Checking.
  - 2) Uses four wire.
  - 3) No Acknowledgement.
  - 4) It allows only for a single master.

15. What are the application of SPI?

- ⇒
- 1) SPI bus is commonly used for flash memory, sensor, Real time Clock.
  - 2) This bus is commonly used to send data between microcontroller to small peripherals like LCD Display, ADC.
  - 3) Secure digital card.

### UART

1. What is the full form of UART?

- ⇒ Universal Asynchronous Receiver Transmitter.

2. How many wires are used in UART communication?

- ⇒ UART is two wired protocol

1) TxD (Transmit Data)

2) RxD (Receive Data)

3. Is UART Half Duplex (or) Full Duplex?

- ⇒ Full Duplex.

4. What is UART?

- ⇒ UART is an on-chip peripheral of Microcontroller which can be used for synchronous and asynchronous serial communication in which data format and transmission speeds are configurable.

5. What is the byte order in UART?

- ⇒ LSB to MSB.

6. Name some UART devices?

- ⇒
- 1) GSM

2) GPS

3) RFID

7. What is the standard speed of UART?

- ⇒ The standard speed of UART is up to 1 Mbps.

8. What are the advantages of UART?

- ⇒
- 1) Hardware complexity is low.
  - 2) Requires only two wires for full duplex data transmission.
  - 3) Parity bit for error checking.

9. What are the dis-advantages of UART?

- ⇒
- 1) Size of data in the frame is limited.
  - 2) Is it suitable for communication between two devices.

10. What is a serial terminal?

- ⇒ In computing, a serial port is a serial communication interface through which information transfer in (or) out sequentially one bit at a time.



11. What is Hyper Terminal?

⇒ Hyper Terminal is a communications software (or) Hyper Terminal is a program that you can use to connect to other computers. With Hyper Terminal, the user can transfer files between the two computers.

### Introduction to UART

• UART stands for universal asynchronous receiver transmitter.

• Speed of UART comm. is called Baud rate.

1) What is UART?

⇒ UART is hardware as well as protocol.

Protocol :- Protocol means a set of standard rules.

• UART is parallel-in, serial-out and serial-in, parallel out device.

• UART follows some set of standard rules for transmitting and receiving the data. That's why it is a protocol also.

Note :- while transmitting data using UART, it will act as a parallel-in and serial-out, and while receiving the data UART will act as a serial-in and parallel-out devices.



2. Why UART is used/ designed?

⇒ UART is mainly designed for asynchronous serial communication.

Note :- UART can do asynchronous as well as synchronous serial comm.

3. Serial Comm vs Parallel comm.?

⇒ Serial Comm

1) Serial comm is a process of sending 1 bit at a time (ex:- 1 bit in 1 millisecond).

2) Slower than parallel comm.

3) In serial long distance, comm is possible.

4) Hardware complexity is less (less no. of pins required to connect two or more ICs).

Ex:- USB (Universal serial bus) pen drive.

Parallel Comm

1) Parallel comm is a process of sending 1 byte at a time (ex:- 1 byte in 1 millisecond).

2) Faster than serial comm.

3) In parallel long distance, comm is not possible.

4) Hardware complexity is more (more no. of pins required to connect two or more ICs).

Ex:- alphanumeric LCD.



## Synchronous Serial Comm.

1. One data line and a common clock line is used b/w transmitter and receiver. Clock line is used to synchronize data. Data line use to exchange data.

2. In the case of synchronous speed of tx device and Rx device can be different. Because a common clock line manages synchronization.

Ex :- EEPROM (Electrically), RTC, Thermometers

Ex of sync protocol : I2C, SPI etc

## Asynchronous Serial Comm.

1. There is no common clock line used between transmitter and receiver.

2. In the case of asynchronous Tx speed and Rx device speed must be the same.

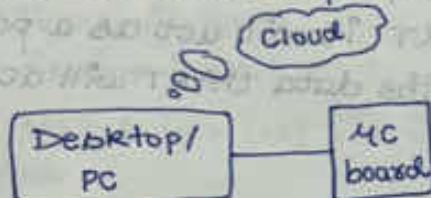
Ex :- GPS, GSM, wifi, Bluetooth, RFID

Automatic sync happens when the speed is the same.

Ex :- UART, USB

### \* Use of UART protocol in real time

- Communication between pc to the microcontroller board



- Remote logic with board single computer (sbc)
- Communication with external uart devices (gsm, gps, bluetooth, RFID readers)
- Communication between microcontroller board.

### \* Features of UART protocol :-

1. UART is designed for long and short - distance communication.
2. It is a two-wired communication protocol

TXD (Transmit data)

RXD (Receiver data)

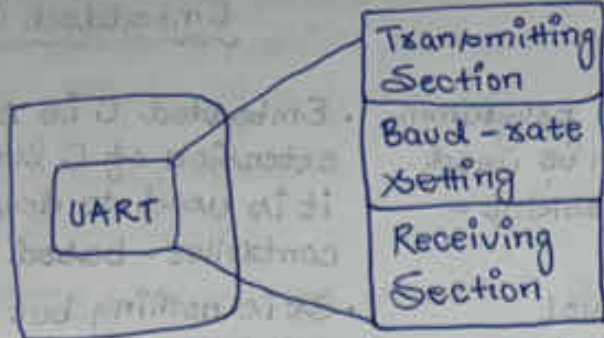
3. Max speed of UART is upto 1Mbps.
4. UART is designed for peer-to-peer communication (we cannot use multiple devices at a time to communicate).
5. Parity checking is the error detection mechanism used in UART.
6. Data transfer direction is from LSB to MSB always.
7. UART can send only 1 byte of data at the same time.

### \* List of UART devices :-

- GSM modem
- GPS modem
- BT modem
- Wifi modem

# \* Working of UART :-

- While sending a data UART will acts as parallel-in, serial-out & while receiving a data UART will acts as serial-in, parallel-out.



- UART consists three different sections for receiving, transmitting and setting baud rate.
- Both transmitting and receiving section contains 1BUF registers (1-byte) to store data (TxBUF) and (RxBUF)
- To transmit and receive data and Txintx and Rxintx Flag.

Popular compilers to execute an C language program are:

- 1) gcc (GNU Compiler Collection)
- 2) Turbo C
- 3) Intel C++

Compiler is a hardware independent language. C compilers are OS dependent.

C language has a free format of program coding. It is specifically used for desktop applications.

Optimization is needed. It is very easy to read and write code at your own risk.

Compiler

↑

Applications and Libraries



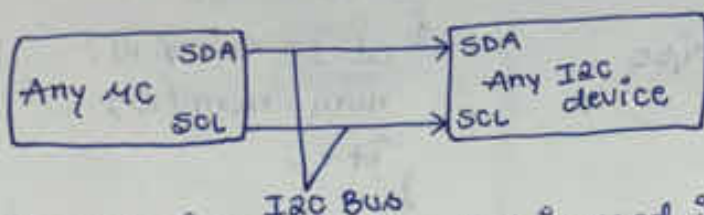
## I2C Protocols

### \* Inter - Integrated Circuit Protocol

- I2C Protocol was designed by Phillips (now NXP Semiconductors) for on board IC communication or short distance communication.
- I2C can communicate off board also but distance not more than 2 meters.
- This protocol is first designed to reduce wiring complexity.
- This protocol is not designed for long distance communication (10 feet or 5m).

### \* Features :-

- It is a two wired communication protocol
  - 1) Serial data line (SDA)
  - 2) Serial clock line (SCL)



- In I2C the any microcontroller that is used is called as master and the device that is used is called as slave.

Note :- In master and slave communication only master can generate clock pulses.

- Role of SCL line is synchronize and SDA line is to exchange data b/w master and slave.
- I2C is half-duplex & synchronous serial communication protocol.
- I2C is multi-slave and multi-master protocol.

Note :- Only one master or one slave can send data at a time in multi master and multi slave communication.

When two or more than two masters are sending a data at the same time on the bus, it will clash the data & data gets corrupted. To avoid this data corruption the mechanism used in the multi-master communication protocol is called as Arbitration.

- Every slave of I2C comes with inbuilt slave address & size of address is (7 bits or 10 bits).
- I2C is acknowledgement based protocol, slave ack to master for every received bytes.

### \* Speed of I2C :-

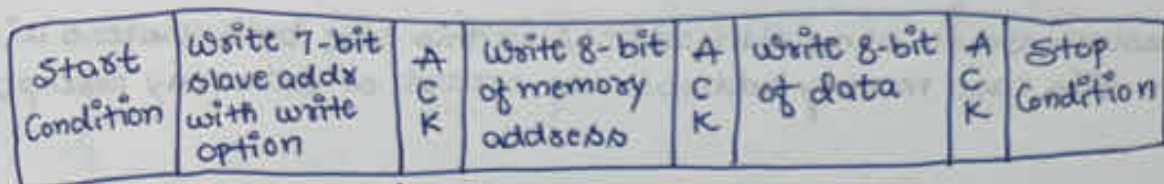
- Standard speed of I2C is 100 Kbps & the max speed is 5 Mbps (Speed setting can only done in master not slave).
- The max num of slaves that are connected on the I2C bus are restricted by the slave addresses (or devices address).  
If 7 bit  $2^7 = 128$ , if 10-bit  $2^{10} = 1024$ .



- In the I2C protocol, master will get acknowledgement after every 8 bits written into slave.
- Data transfer direction is from MSB to LSB.

### \* I2C Data Frames :-

- 1) I2C Byte write frame
- 2) I2C Byte read frame



MSB  $\xrightarrow{\text{00000001}}$  LSB

1 - master read option  
0 - master write option

- Inside the slave one address pointer is available suppose master wants to write data at memory location 0x2, then this pointer will have address 0x2.
- when data is written at memory location 0x2 addr-pt'r will automatically increment.

### \* I2C Starts Condition :-

A high to low transition on the SDA line, while SCL is high, defines a start condition.



### \* I2C Arbitration :-

Note :- This arbitration concept comes to the picture only in the case of multi-master communication.

Bit 0 :- dominant bit (high priority bit)

Bit 1 :- recessive bit (low priority bit)

- The master who will write first dominant bit becomes a winner in the arbitration process, and winner data will be transmitted first.
- The master who lost arbitration will wait till the bus free (generate stop condition) or till completion of winner data transmission.
- The master who lost arbitration will check the bus continuously whether the stop condition is generated or not.

Note :- I2C bus is wired AND logic.

- When M1 will send 1 and M2 will send 0 on the bus so  $1 \& 0 = 0$ , M2 wins from this process onwards only M2 will send bits (slave address bit) on bus.



- After sending address bits, master will wait for acknowledgement. The both slave will first compares address send by master with inbuilt slave address who's address matches will send ack and start communication.
- The moment stop condition generated  $M_1$  will start its transmission from beginning.
- After sending data if  $M_1$  &  $M_2$  again start transmitting data then again  $M_2$  will win, so after transmit data we have to write small delay so that  $M_1$  can also transmit.
- If both masters sends same slave address in this case both masters will win but in this case memory address may corrupt or data may corrupt.

\* Because the IDE bit is dominant (0) for standard frames and recessive (1) for extended frames, standard frames are always higher priority than extended frames.

Standard frame :- Car, Passenger vehicles.

Extended frame :- Heavy Vehicles like Buses and Trucks.

Voltage or Power Supply at home :- 220 - 240 V

50 Hz frequency (1 sec it will on and off by 50 times i.e., high and low).

### BJT

- 1) Bipolar Junction Transistor.
- 2) Current Controlled device.
- 3) NPN transistor and PNP transistor.
- 4) Emitter, Base, Collector
- 5) Current flow is due to both majority and minority charge carriers. Thus, it is a bipolar.
- 6) The input ckt is forward biased. Thus, the BJT has low input impedance.  
Switch - in saturation and cut-off  
amplifier - in active region

### FET

- 1) Field Effect Transistor
- 2) Voltage controlled device
- 3) N-Channel FET and P-Channel FET
- 4) Gate, Drain, Source
- 5) Current flow only due to majority charge carriers. Thus, it is unipolar.
- 6) FET has high input impedance due to reverse bias of input circuit.  
Switch - Ohmic and cut-off  
amplifier - in saturation region