

# DIGITAL ELECTRONICS

-- Interview Topics

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# Number System

1. Number System types (Radix, Symbols) – Binary, Octal, Decimal, Hexadecimal, radix-n
2. Number System Conversions
3. Representations of Binary Number System: (Ranges & Symbols)
  - Signed & Unsigned
  - 1's complement ((n-1)'s complement)
  - 2's complement (n's complement)
4. Arithmetic Operations on Number Systems:
  - Addition
  - Subtraction using n's comp & (n-1)'s comp
  - Multiplication & Division
5. Floating point Numbers representation and Operations on them.
6. Different types of Codes:
  - BCD Code
  - Gray Code
  - Parity Code
  - Hamming Code
  - Excess – 3 code
  - Weighted code & Non – Weighted code
  - One – hot coding
7. Code Conversions

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# Boolean Algebra

1. Concepts of Boolean algebra:
  - Basic Boolean Properties
  - Boolean laws:
    - Commutative Law
    - Distributive Law
    - Associative Law
    - Identity Law
    - Null Elements
    - Complement Law
    - Idempotent Law (Duality Principle)
    - Involution Law
    - De Morgan's Law
    - Absorption Law
    - Shannon's Expansion
  - Boolean Theorems: (with proofs using laws)
    - Consensus Theorem
    - Transposition Theorem
  - Simplification of Boolean expressions using Boolean laws & theorems
2. M – Notations (Min & Max terms)
3. Switch Boolean functions ( $SOP \rightarrow POS$ ,  $POS \rightarrow SOP$ )
4. Standard and Canonical forms



# Logic Gates

1. Concepts of Logic gates:
  - All basic logic gates: (Algebraic form, Graphical symbols, Truth tables, Physical circuit with switches)
    - Buffer, NOT, AND, OR, NAND, NOR, XOR, XNOR
2. Alternate gate representations ( AND  $\approx$  OR)
3. Implementation of NOT gate using all basic gates
4. Enabling signal and disabling signals of logic gates
5. NAND – NAND realisations
6. NOR – NOR realisations
7. Implementation of expressions using minimum number of gates
8. Implementation of gates using universal gates
9. Conversion of gates



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# Minimization of Switching Functions

1. Terminology needed for minimization:
  - Prime Implicants / Prime False Implicants
  - Essential Prime Implicants / Essential False Prime Implicants
  - Redundant Prime Implicants / Redundant False Prime Implicants
  - Selective Prime Implicants / Selective False Prime Implicants
2. Karnaugh Map (K – Map):
  - K – Map for SOP expression ( $\sum m = f()$ )
  - K – Map for POS expression ( $\pi M = F()$ )
  - K – Map for SOP & POS expressions with don't cares
  - K – Map Advantages & Disadvantages
3. Tabular Form:
  - Tabular Form for SOP expression ( $\sum m = f()$ )
  - Tabular Form POS expression ( $\pi M = F()$ )
  - Tabular Form SOP & POS expressions with don't cares
  - Tabular Form Advantages & Disadvantages



# Combinational Circuits

1. Concepts of Combinational circuits:
  - Definition, Design Steps, Advantages, Disadvantages & Applications
2. Half Adder
3. Full Adder
4. Implementation of Full Adder using Half Adders
5. Parallel Adder / Ripple Carry Adder
6. Half Subtractor
7. Full Subtractor
8. Implementation of Full Subtractor using Half Subtractors
9. Parallel Subtractor / Ripple Carry Subtractor
10. Ripple Carry Adder & Subtractor
11. Carry Look Ahead Adder
12. Carry Save Adder
13. Carry Increment Adder
14. Carry Select Adder
15. Carry Skip Adder
16. Carry Bypass Adder
17. Decoder
  - Logical Expressions, Functionality, Internal circuitry for decoder with and without enable signal
  - Realisation of higher decoder using lower decoders
  - Realisation of Boolean expressions using decoders

# Combinational Circuits

## 18. Encoder

- Logical Expressions, Functionality, Internal circuitry for encoder with and without enable signal
- Realisation of higher encoder using lower encoders

## 19. Multiplexer

- Logical Expressions, Functionality, Internal circuitry for Multiplexer with and without enable signal
- Realisation of higher Multiplexer using lower Multiplexers
- Realisation of logic gates using multiplexer
- Realisation of Boolean expressions using different size Multiplexers

Example: if no of variables = 3, expression can be realised using  $8 \times 1$ ,  $4 \times 1$  &  $2 \times 1$

## 20. Demultiplexer

- Logical Expressions, Functionality, Internal circuitry for Demux with and without enable signal
- Realisation of higher Demultiplexer using lower Demultiplexer

## 21. Priority Encoder

## 22. Mux using Decoder

## 23. Comparator

## 24. Code Converters (Binary $\leftrightarrow$ Gray, BCD $\leftrightarrow$ Excess 3, Gray $\leftrightarrow$ Excess 3)

## 25. Parity Generator & Checkers (Even & Odd)



# Sequential Circuits

1. Concepts of Sequential circuits:
  - Definition, classification & Clock Parameters
2. Differences between Sequential circuits & Combinational Circuits
3. Latches: (Logic Diagrams, Truth tables & Excitation Tables)
  - SR Latch, D Latch, JK Latch & T Latch
5. Race Around condition
6. Differences between Level Triggering and Edge Triggering
7. Master – Slave configuration
8. Flip Flops: (Logic Diagrams, Truth tables & Excitation Tables)
  - SR F/F, D F/F, JK F/F & T F/F
8. Setup and Hold time (Definitions & Violations)
9. Flip Flops Conversions
10. Counters: (State Diagram, State table, Logic Diagram, Timing Diagram)
  - Asynchronous up, down, up/down counter
  - Synchronous up, down, up/down counter
  - Mod – n counters (Synchronous & Asynchronous)
  - Ring Counter
  - Twisted Ring Counter / Johnson Counter



# Sequential Circuits

## 10. Registers:

- Shift register
- Serial In – Serial Out register
- Serial In – Parallel Out register
- Parallel In – Serial Out register
- Parallel In – Parallel Out register
- Universal Shift register

## 11. Finite State Machines (FSM): (State Diagram, State table with output, Logic Diagram, Timing Diagram)

- Sequence Detectors
  - Non – Overlapping : Mealy & Moore
  - Overlapping: Mealy & Moore
- Multi – Sequence Detectors
  - Non – Overlapping: Mealy & Moore
  - Overlapping: Mealy & Moore
- Styles of state assignments (Binary, Gray & One – hot)
- Differences between Mealy & Moore



# PLDs

## Programmable Logic Devices

1. Operation & Circuit level implementation of:
  - Programmable Read Only Memory (PROM)
  - Programmable Logic Array (PLA)
  - Programmable Array Logic (PAL)
2. Combinational Logic Implementation using PROM, PLA & PAL

# IC Logic Families

1. Implementation of basic gates using:
  - Transistor Logic
  - CMOS Logic
  - Bipolar Logic
  - TTL

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