Review Questions/Answers

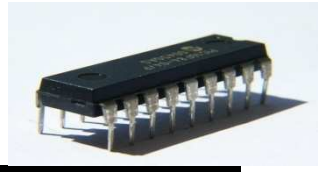
Low Power Circuits and Systems

Ajit Pal

Professor

Department of Computer Science and Engineering
Indian Institute of Technology Kharagpur
INDIA-721302

Review Questions of Lec-1



Q1. Why low power has become an important issue in the present day VLSI circuit realization?

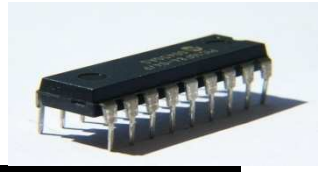
Q2. How reliability of a VLSI circuit is related to its power dissipation?

Q3. How environment is affected by the power dissipation of VLSI circuits?

Q4. Why leakage power dissipation has become an important issue in deep submicron technology?

Q5. Distinguish between energy and power dissipation of VLSI circuits. Which one is more important for portable systems?

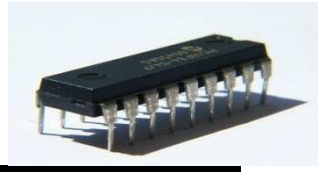
Answer to Questions of Lec-1



Q1. Why low power has become an important issue in the present day VLSI circuit realization?

- **Ans: In deep submicron technology the power has become as one of the most important issue because of:**
  - **Increasing transistor count; the number of transistors is getting doubled in every 18 months based on Moore,s Law**
  - **Higher speed of operation; the power dissipation is proportional to the clock frequency**
  - **Greater device leakage currents; In nanometer technology the leakage component becomes a significant percentage of the total power and the leakage current increases at a faster rate than dynamic power in technology generations**

Answer to Questions of Lec-1



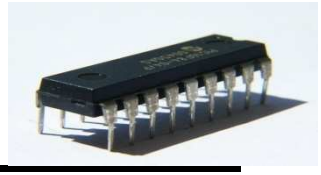
Q2. How reliability of a VLSI circuit is related to its power dissipation?

Ans: It has been observed that every 10ºC rise in temperature roughly doubles the failure rate because various failure mechanism such as silicon interconnect fatigue, electromigration diffusion, junction diffusion and thermal runaway starts occurring as temperature increases.

Q3. How environment is affected by the power dissipation of VLSI circuits?

- **Ans: According to an estimate of the U.S. Environmental Protection Agency (EPA), 80% of the power consumption by office equipment are due to computing equipment and a large part from unused equipment. Moreover, the power is dissipated mostly in the form of heat. The cooling techniques, such as AC transfers the heat to the environment.**

Answer to Questions of Lec-1



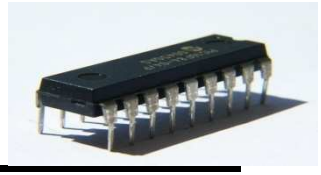
Q4. Why leakage power dissipation has become an important issue in deep submicron technology?

Ans: In deep submicron technology the leakage component becomes a significant percentage of the total power and the leakage current increases at a faster rate than dynamic power in new technology generations. That is why the leakage power has become an important issue.

Q5. Distinguish between energy and power dissipation of VLSI circuits. Which one is more important for portable systems?

Ans: Power (P) is the power dissipation in Watts at different instances of time. On the other has energy (E) refers to the energy consumed in Joule over a period of time (E = P*t).

Review Questions of Lec-2



Q1. What are the commonly used conducting layers used in IC fabrication?

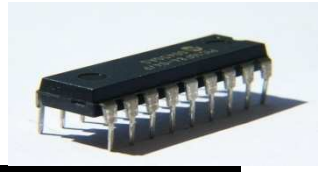
Q2. Show the basic structure of a MOS transistor.

Q3. What is the latch up problem that arises in bulk CMOS technology? How is it overcome?

Q3. Distinguish between the bulk CMOS technology with the SoI technology fabrications.

Q4. What are the benefits of SOI technology relative to conventional bulk CMOS technology?

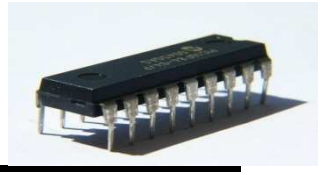
Answer to Questions of Lec-2



Q1. What are the commonly used conducting layers used in IC fabrication?

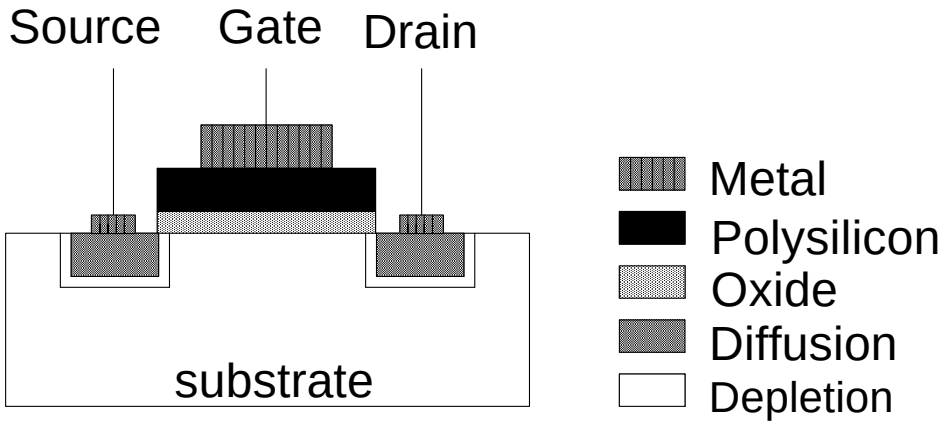
Ans: Fabrication involves fabrication of patterned layers of the three conducting materials: *metal*, *poly-silicon* and *diffusion by using* a series of photolithographic techniques and chemical processes involving oxidation of silicon, diffusion of impurities into the silicon and deposition and etching of aluminum or polysilicon on the silicon to provide interconnection.

Answer to Questions of Lec-2

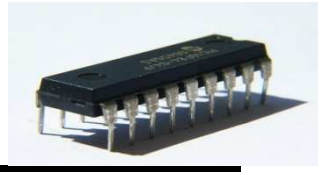


Q2. Show the basic structure of a MOS transistor.

➢**Ans: The basic structure of a MOS transistor is given below. On a lightly doped substrate of silicon two islands of diffusion regions called as *source* and *drain*, of opposite polarity of that of the substrate, are created. Between these two regions, a thin insulating layer of silicon dioxide is formed and on top of this a conducting material made of poly-silicon or metal called *gate* is deposited.**



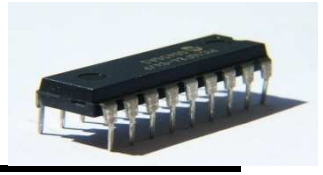
Answer to Questions of Lec-2



Q3. What is the latch up problem that arises in bulk CMOS technology?

Ans: The latch-up is an inherent problem in both n-well as well as p-well based CMOS circuits. The phenomenon is caused by the parasitic bipolar transistors formed in the bulk of silicon as shown in the figure for the n-well process. *Latch-up* can be defined as the formation of a low-impedance path between the power supply and ground rails through the parasitic npn and pnp bipolar transistors. As shown the BJTs are cross-coupled to form the structure of a silicon-controlled-rectifier (SCR) providing a short-circuit path between the power rail and ground. Leakage current through the parasitic resistors can cause one transistor to turn on, which in turn turns on the other transistor due to positive feedback and leading to heavy current flow and consequent device failure.

Answer to Questions of Lec-2

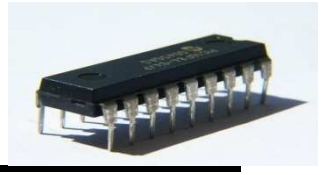


Q4. How the latch up problem can be overcome?

Ans: There are several approaches to reduce the tendency of Latch-up. Some of the important techniques are mentioned below:

- **Use guard ring around p- and/or n-well with frequent contacts to the rings**
- **To reduce the gain product B1XB2**
- **Moving the n-well and the n+ source/drain further apart**
- **Buried n+ layer in well to reduce gain of Q1**
- **Higher substrate doping level to reduce R-sub**
- **Reduce R-well by making low resistance contact to GND**

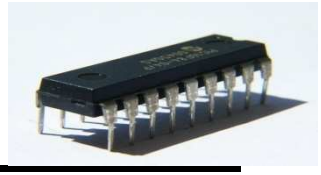
Answer to Questions of Lec-2



Q5. Distinguish between the bulk CMOS technology with the SoI technology fabrications.

Ans: In bulk CMOS technology, a lightly doped p-type or n-type substrate is used to fabricate MOS transistors. On the other hand, an insulator can be used as a substrate to fabricate MOS transistors

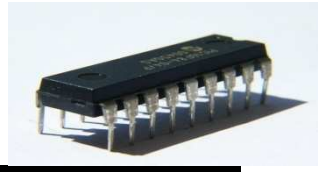
Answer to Questions of Lec-2



Q6. What are the benefits of SOI technology relative to conventional bulk CMOS technology?

- **Ans: Benefits of SOI technology relative to conventional silicon (bulk CMOS):**
  - **Lowers parasitic capacitance due to isolation from the bulk silicon, which improves power consumption and thus high speed performance.**
  - **Reduced short channel effects**
  - **Better sub-threshold slope.**
  - **No Latch up due to BOX (buried oxide).**
  - **Lower Threshold voltage.**
  - **Reduction in junction depth leads to low leakage current.**
  - **Higher Device density.**

Review Questions of Lec-3



Q1. What are the basic assumptions of the fluid model?

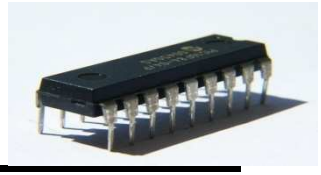
Q2. Explain the function of a MOS transistor in the saturation mode using fluid model.

Q3. Explain the function of a MOS transistor in the nonsaturation mode using the fluid model.

Q4. Explain the three modes of operation of a MOS transistors.

Q5. Explain the linear region of the I-V characteristic of an nMOS transistor using the fluid model.

Answer to the Questions of Lec-3



Q1. What are the basic assumptions of the fluid model?

Ans: There are two basic assumptions as follows:

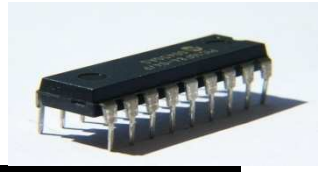
(a) Electrical charge is considered as fluid, which can move from one place to another depending on the difference in their level, of one from the other, just like a fluid.

(b) Electrical potentials can be mapped into the geometry of a container, in which the fluid can move around.

Q2. Explain the function of a MOS transistor in the nonsaturation mode using the fluid model.

Ans: Gate voltage higher than the threshold voltage and the drain voltage is slightly higher than source voltage. In such a situation, as the drain voltage is increased the slope of the fluid flowing out increases indicating linear increase in the flow of current.

Answer to the Questions of Lec-3



Q3. Explain the function of a MOS transistor in the saturation mode using fluid model.

Ans: The saturation mode corresponds to the drain voltage is much higher than source voltage. In such a situation the slope of the fluid cannot increase representing constant flow of fluid.

Q4. Explain the three modes of operation of a MOS transistors.

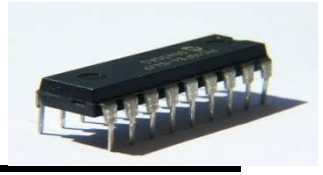
Ans: The three modes are:

(a) Accumulation mode when Vgs is much less than Vt

(b) Depletion mode when Vgs is equal to Vt

(c) Inversion mode when Vgs is greater than Vt

Answer to the Questions of Lec-3



Q5. What are the three regions of operation of a MOS transistor?

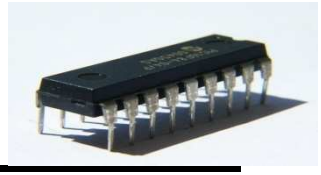
Ans: The three regions are:

***Cut-off region*: This is essentially the accumulation mode, where there is no effective flow of current between the source and drain.**

***Non-saturated region:* This is the *active, linear* or *week inversion* region, where the drain current is dependent on both the gate and drain voltages.**

***Saturated region:* This is the *strong inversion* region, where the drain current is independent of the drain-to-source voltage but depends on the gate voltage.**

Review Questions of Lec-4



Q1. What is the threshold voltage of a MOS transistor? How it varies with the body bias?

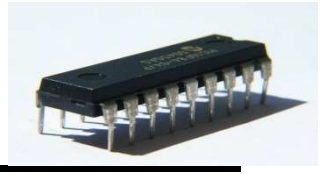
Q2. The following parameters are given for an nMOS process: t_{ox} 500Å, $N_A = 1x10^{16}cm^{-3}$, $N_D = 1x10^{20}cm^{-3}$, $N_{OX} = 2x10^{10}cm^{-1}$. (i) Calculate Vt for an unimplanted transistor, (ii) what type and what concentration must be implanted to achieve Vt = +1.5V and Vt = -2.0V?

Q3. What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?

Q4. What is body effect? How does it influences the threshold voltage of a MOS transistor?

Q5. What is transconductance of a MOS transistor? Explain its role in the operation of the transistor.

Answer to the Questions of Lec-4

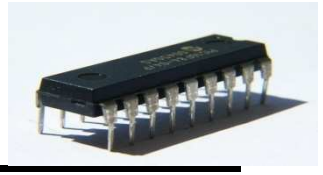


Q1. What is the threshold voltage of a MOS transistor? How it varies with the body bias?

Ans: One of the parameters that characterizes the switching behavior of a MOS transistor is its threshold voltage V_t. This can be defined as the gate voltage at which a MOS transistor begins to conduct.

Q2. The following parameters are given for an nMOS process: t_{ox} 500Å, $N_A = 1x10^{16}cm^{-3}$, $N_D = 1x10^{20}cm^{-3}$, $N_{OX} = 2x10^{10}cm^{-1}$. (i) Calculate Vt for an unimplanted transistor, (ii) what type and what concentration must be implanted to achieve Vt = +1.5V and Vt = -2.0V?

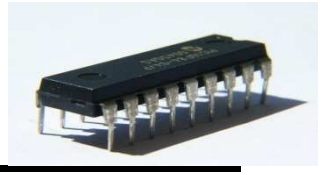
Answer to the Questions of Lec-4



Q3. What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?

Ans: It is assumed that channel length remains constant as the drain voltage is increased appreciably beyond the on set of saturation. As a consequence, the drain current remains constant in the saturation region. In practice, however the channel length shortens as the drain voltage is increased. For long channel lengths, say more than 5 μm, this variation of length is relatively very small compared to the total length and is of little consequence. However, as the device sizes are scaled down, the variation of length becomes more and more predominant and should be taken into consideration. As a consequence, the drain current increases with the increase in drain voltage even in the saturation region.

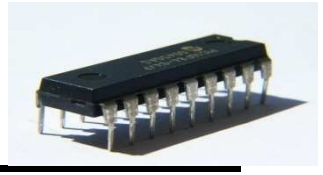
Answer to the Questions of Lec-4



Q4. What is body effect? How does it influences the threshold voltage of a MOS transistor?

Ans: All MOS transistors are usually fabricated on a common substrate and substrate (body) voltage of all devices is normally constant. However, as we shall see in subsequent chapters, when circuits are realized using a number of MOS devices, several devices are connected in series. This results in different source potentials for different devices. It may be noted that the threshold voltage V_t is not constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This is known as the substrate-bias effect or *body effect*. Increasing the V_{sb} causes the channel to be depleted of charge carries and this leads to increase in the threshold voltage.

Answer to the Questions of Lec-4

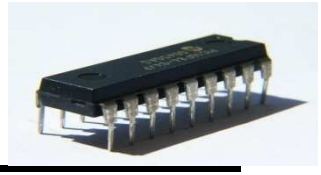


Q5. What is transconductance of a MOS transistor? Explain its role in the operation of the transistor.

Ans: Trans-conductance is represented by the change in drain current for change in gate voltage for constant value of drain voltage. This parameter is somewhat similar to β, the current gain of bipolar junction transistors. The following equation shows the dependence of on various parameters. As MOS transistors are voltage controlled devices, this parameter plays an important role in identifying the efficiency of the MOS transistor.

$$g_m = \frac{\mu_n \varepsilon_{ox} \varepsilon_0}{D} \frac{W}{L} (V_{GS} - V_t)$$

Review Questions of Lec-5



Q1. Explain the behaviour of a nMOS transistor as a switch.

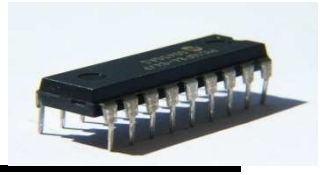
Q2. Explain the behaviour of a pMOS transistor as a switch.

Q3. How one nMOS and one pMOS transistor are combined to behave like an ideal switch.

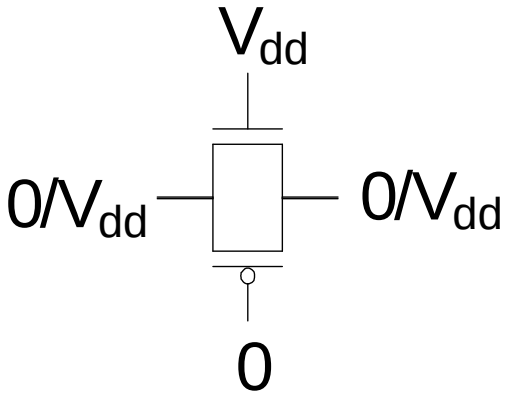
Q4. The input of a lightly loaded transmission gate is slowly changes from HIGH level to LOW level. How the currents through the two transistors vary?

Q5. How its ON-resistance of a transmission gate changes as the input varies from 0 V to Vdd, when the output has a light capacitive load.

Answer to the Questions of Lec-5

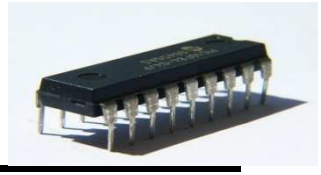


Q3. How one nMOS and one pMOS transistor are combined to behave like an ideal switch.



Ans: To overcome the limitation of either of the transistors, one pMOS and one nMOS transistor can be connected in parallel with complementary inputs at their gates. In this case we can get both LOW and HIGH levels of good quality at the output. The low level passes through the nMOS switch and HIGH level passes through the pMOS switch without any degradation as shown in the figure.

Answer to the Questions of Lec-5



Q4. The input of a lightly loaded transmission gate is slowly changes from HIGH level to LOW level. How the currents through the two transistors vary?

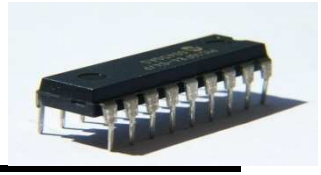
Ans: Another situation is the operation of the transmission gate when the output is lightly loaded (smaller load capacitance). In this case, the output closely follows the input. In this case the transistors operate in three regions depending on the input voltage as follows:

Region I: nMOS non-saturated, pMOS cut-OFF

Region II: nMOS non-saturated, pMOS non-saturated

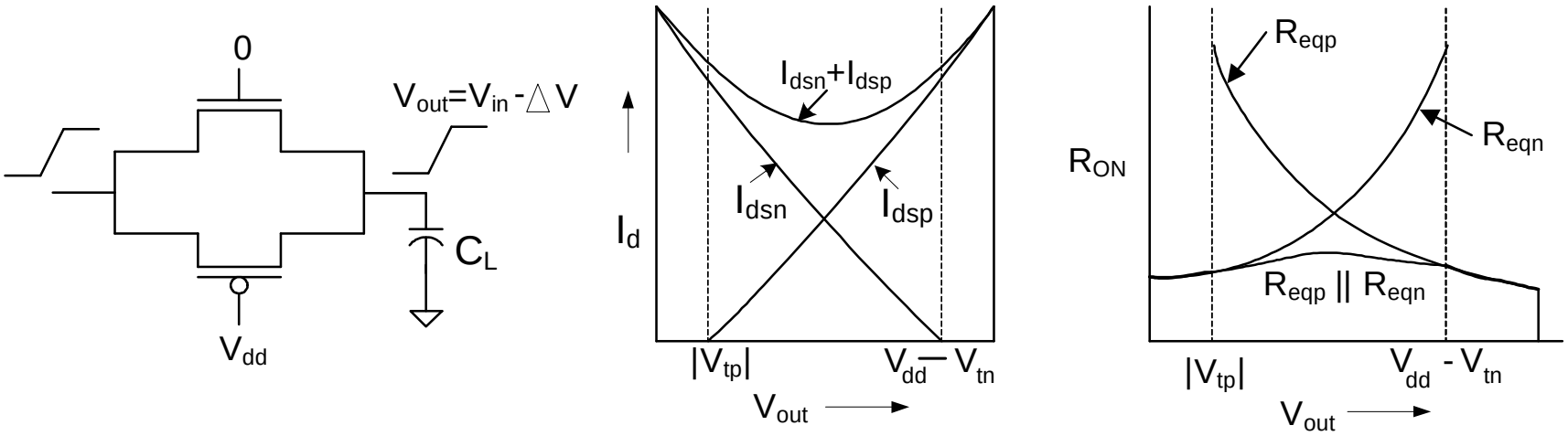
Region III: nMOS cut off, pMOS non-saturated

Answer to the Questions of Lec-5

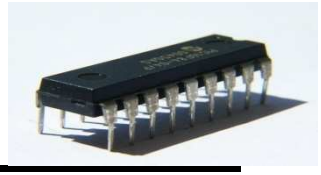


Q5. How its ON-resistance of a transmission gate changes as the input varies from 0 V to Vdd, when the output has a light capacitive load.

Ans: The variation of ON resistance is shown in the figure. The parallel resistance remains more or less constant.



Review Questions of Lec-6

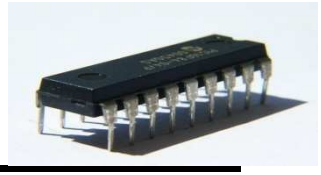


Q1. Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics.

Q2. What is noise margin? Find out the noise margin from the actual characteristics of the inverter.

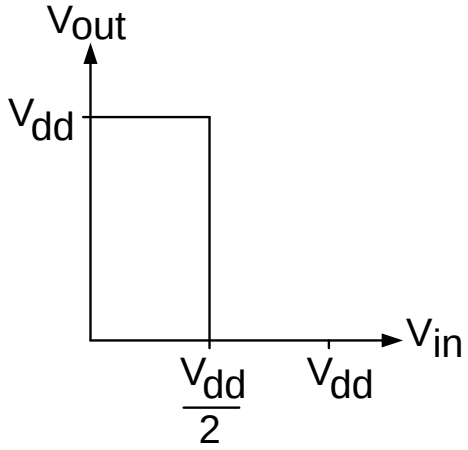
Q3. Compare the characteristics of the different types of MOS inverters in terms of noise margin and power dissipation.

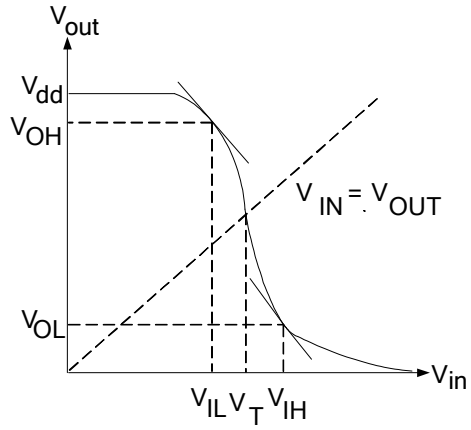
Answer to the Questions of Lec-6



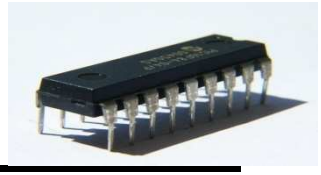
Q1. Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics.

Ans: The ideal and actual characteristics are given below. In the ideal characteristics, the output voltage is Vdd for input voltage from o to Vdd/2 and 0 for input voltage from Vdd/2 to Vdd. This is not true in case of the actual characteristics as shown below.





Answer to the Questions of Lec-6



Q2. What is noise margin? Find out the noise margin from the actual characteristics of the inverter.

Ans: An important parameter called *noise margin* is associated with the input-output voltage characteristics of a gate. It is defined as the allowable noise voltage on the input of a gate so that the output is not affected. The deviations in logic levels from the ideal values, which are restored as the signal propagates to the output, can be obtained from the DC characteristic curves. The logic levels at the input and output are given by

$$\text{logic 0 input}: \quad 0 \le V_{in} \le V_{IL}$$

$$\text{logic 1 input}: \quad V_{IH} \le V_{in} \le V_{DD}$$

$$\text{logic 0 output}: \quad 0 \le V_{o} \le V_{OL}$$

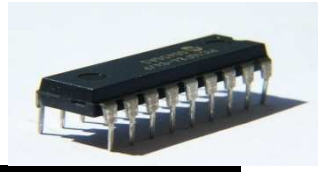
$$\text{logic 1 output}: \quad V_{OH} \le V_{o} \le V_{DD}$$

The noise margins are:

$$NM_L = |V_{IL} - V_{OL}|$$

$$NM_H = |V_{OH} - V_{IH}|$$

Answer to the Questions of Lec-6

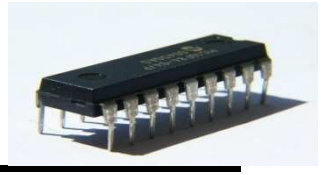


Q3. Compare the characteristics of the different types of MOS inverters in terms of noise margin and power dissipation.

Ans: Various characteristic parameters are compared in the following table:

Inverters	V_{LO}	V_{HI}	*Noise-margin*	*Power*
Resistor	Weak	Strong	Poor for Low	High
nMOS depletion	Weak	Strong	Poor for Low	High
nMOS enhancement	Weak	Weak	Poor for both Low and High	High
Psuedo-nMOS	Weak	Strong	Poor for Low	High

Review Questions of Lec-7



Q1. What is the inversion voltage of an inverter? Find out the inversion voltage of a CMOS inverter.

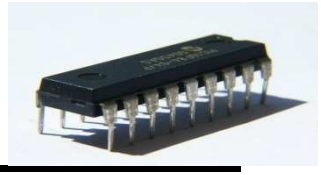
Q2. How the inversion voltage is affected by the relative sizes of the nMOS and pMOS transistors of the CMOS inverter?

Q3. Find out the noise margin of a CMOS inverter.

Q4. How the noise margin is affected by voltage scaling?

Q5. What is the lower limit of supply voltage of a CMOS inverter. What happens if the supply voltage is further reduced?

Answer to Questions of Lec-7



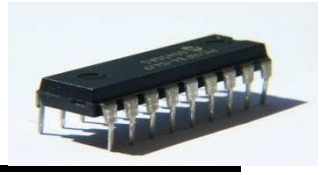
Q1. What is the inversion voltage of an inverter? Find out the inversion voltage of a CMOS inverter.

Ans: The inversion voltage Vinv is defined as the voltage at which the output voltage Vo is equal to the input voltage Vin. For a CMOS inverter it can be expressed in terms of the threshold voltages of the MOS transistors and other parameters.

$$V_{inv} = \frac{V_{dd} + V_{tp} + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

For $\beta_n = \beta_p$ and $V_{tn} = -V_{tp}$, we get $V_{inv} = V_{dd}$ 2

Answer to Questions of Lec-7



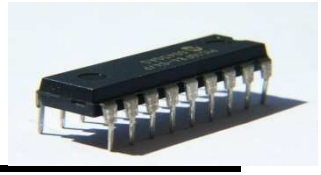
Q2. How the inversion voltage is affected by the relative sizes of the nMOS and pMOS transistors of the CMOS inverter?

Ans: In a CMOS process $\frac{K_n}{K_p} = \frac{\mu_n}{\mu_p} \approx 2.5$

To make one may choose $\left(\frac{W}{L}\right)_p = 2.5\left(\frac{W}{L}\right)_n$.

to get Vinv = Vdd/2

Answer to Questions of Lec-7



Q3. Find out the noise margin of a CMOS inverter.

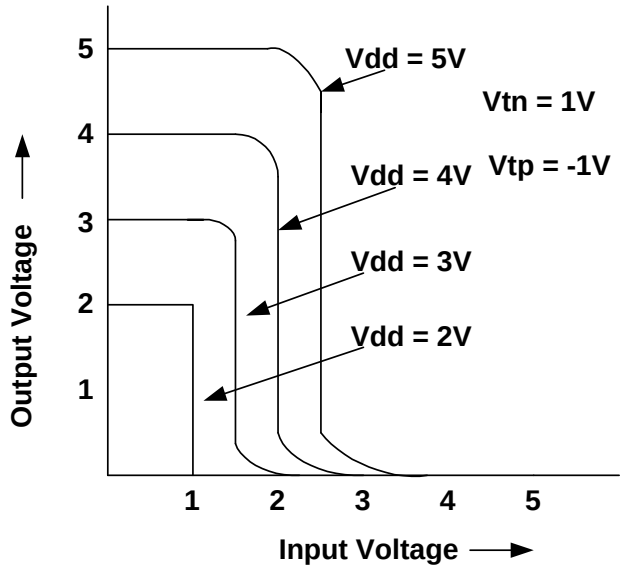
Ans: For a symmetric inverter $V_{IH} + V_{IL} = V_{dd}$

Noise Margin $NM_L = V_{IL} - V_{OL} = V_{IL}$

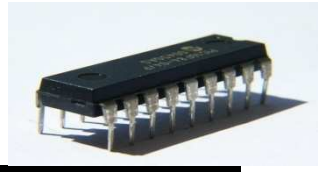
and $NM_H = V_{OH} - V_{IH} = V_{dd} - V_{IH} = V_{IL}$

Q4. How the noise margin is affected by voltage scaling?

Ans: As the supply voltage is reduced, the margin also decreases as shown in the figure.



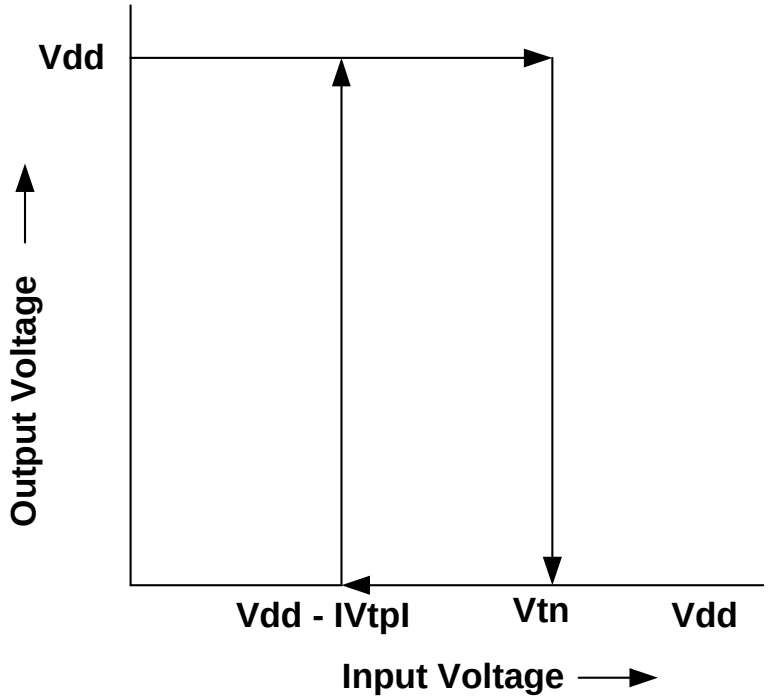
Answer to Questions of Lec-7



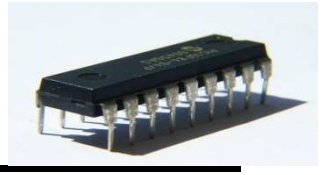
Q5. What is the lower limit of supply voltage of a CMOS inverter. What happens if the supply voltage is further reduced?

Ans: The lower limit of the supply voltage depends on the sum of the threshold voltages of the nMOS and the pMOS transistors.

Vdd = Vtn +|Vtp|. As the supply voltage is reduced further, it leads to hysteresis in the transfer characteristics.



Review Questions of Lec-8



Q1. What is sheet resistance? Find out the expression of the resistance of rectangular sheet in terms of sheet resistance.

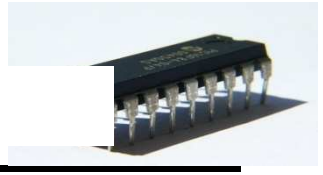
Q2. Find out the capacitance of a MOS capacitor.

Q3. Find out the expression of delay time of a CMOS inverter.

Q4. What are the various ways to reduce the delay time of a CMOS inverter?

Q5. Explain the commonly used technique to estimate the delay time of a CMOS inverter.

Answer to the Questions of Lec-8



- **Q1. What is sheet resistance? Find out the expression of the resistance of rectangular sheet in terms of sheet resistance.**

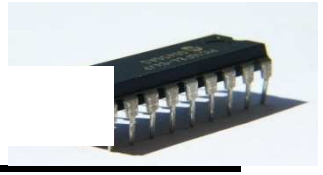
Ans: The sheet resistance is defined as the resistance per unit area of a sheet of material. Consider a rectangular sheet of material with Resistivity = ρ, Width = W, Thickness = t and Length = L.

Then, the resistance between the two ends is

$$R_{AB} = \frac{\rho L}{t.W} = \frac{\rho L}{A} ohm$$ **For L = W** $$R_S = \frac{\rho}{t} = R\, ohm$$

Where, R_S is defined as the sheet resistance

Answer to the Questions of Lec-8



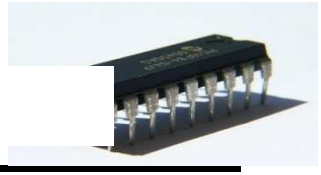
Q2. Find out the capacitance of a MOS capacitor.

Ans: The capacitance of a parallel plate capacitor is given by

$$Co = \frac{\varepsilon_0 \varepsilon_{ins} A}{D} \text{ Farads}$$

Where A is the area of the plates and D is the thickness of the insulator between the plates.

Answer to the Questions of Lec-8



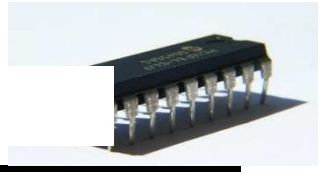
Q3. Find out the expression of delay time of a CMOS inverter.

Ans: The delay time td is given by the expression

$$t_d = \left[\frac{L_n}{K_n W_n} + \frac{L_p}{K_p W_p} \right] \frac{C_L}{V_{dd} \left(1 - \frac{V_t}{V_{dd}} \right)^2}$$

Where C is the load capacitance, Vdd is the supply voltage and Vt is the threshold voltages of the MOS transistors.

Answer to the Questions of Lec-8



Q4. What are the various ways to reduce the delay time of a CMOS inverter?

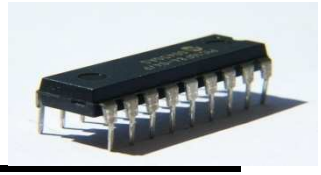
Ans: Various ways for reducing the delay time are given below:

(a) The width of the MOS transistors can be increased to reduce the delay. This is known as gate sizing, which will be discussed later in more details.

(b) The load capacitance can be reduced to reduce delay. This is achieved by using transistors of smaller and smaller dimensions as provided by future generation technologies.

(c) Delay can also be reduced by increasing the supply voltage Vdd and/or reducing the threshold voltage Vt of the MOS transistors.

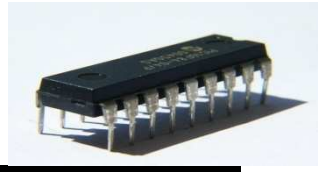
Answer to the Questions of Lec-8



Q5. Explain the commonly used technique to estimate the delay time of a CMOS inverter.

Ans: As the delay time of an inverter is very small, it cannot be measured accurately using conventional method with the help of an oscilloscope. Delay is usually measured by realizing a ring oscillator using a large number of inverters, say 101. Then the frequency of oscillation is measured using the expression $f = \frac{1}{2nt_d}$ **where n is the number of inverters and td is the delay time.**

Review Questions of Lec-9



Q1. Justify the reason for not recommending more than 4 pass transistors to use in series in realizing logic circuits.

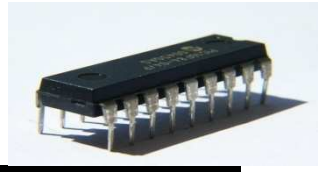
Q2. Draw the schematic diagram of an inverting super-buffer and explain its operation.

Q3. Give the schematic diagram of a Bi-CMOS inverter. Explain its operation. . Compare the switching characteristics of a BiCMOS inverter with respect to that for static CMOS for different fan out conditions.

Q4. Prove that the delay of a series of pass transistors can be reduced from quardratic dependence to linear dependence on the number of transistors in series by inserting buffers at suitable intervals.

Q5. Design a scaled chain of inverters such that the delay time between the logic gate (C_g = 100 fF) and a load capacitance 2 pF in minimized. Find out the number of stages and stage ratio.

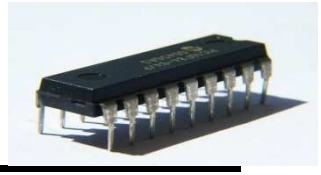
Answer to Questions of Lec-9



Q1. Explain the basic concept of super buffer.

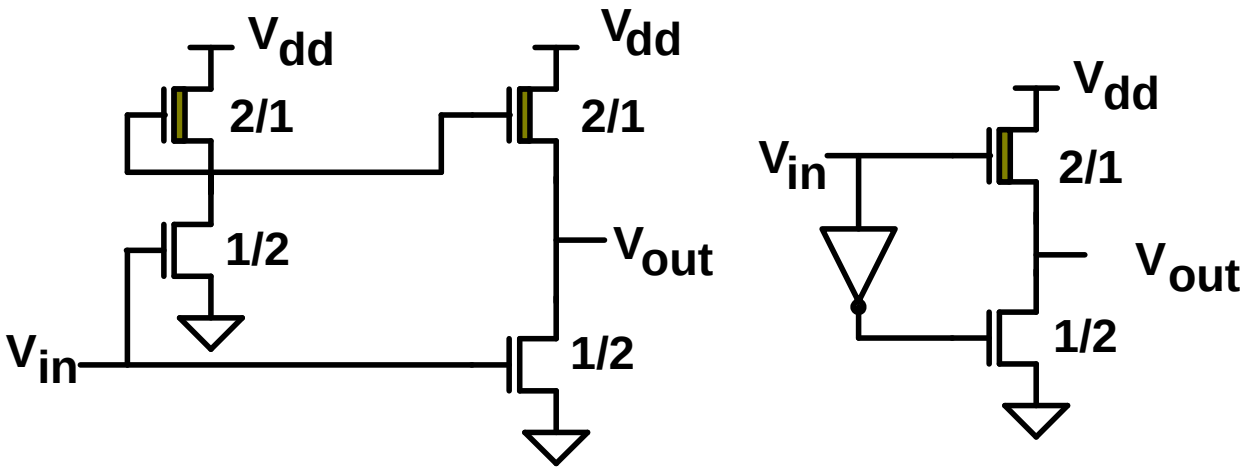
Ans: There are situations when a large load capacitance such as, long buffers, off-chip capacitive load, or I/O buffer are to be driven by a gate. In such cases, the delay can be very high if driven by a standard gate. Limitations of driving by a simple nMOS inverter is the asymmetric drive capability of pull-up and pull-down devices (ratioed logic). Moreover, when the pull-down transistor is ON, the pull-up transistor also remains ON. So, the pull-down transistor should also sink the current of the pull-up device. Although this limitation is overcome in CMOS circuits, there is asymmetry in drive capability of pull-up and pull-down devices having the same minimum size.

Answer to Questions of Lec-9

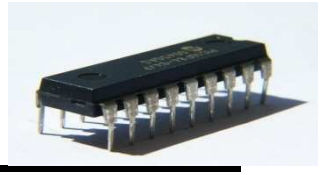


Q2. Draw the schematic diagram of an inverting and non-inverting super-buffers and explain its operation.

Ans: The schematic diagrams of the super buffers are given below. The average of the saturation currents for Vds = 5V and linear current for Vds = 2.5V is approximately 4.4 βpu for the standard inverter. On the other hand the, for the super-buffer, the average current is 19.06 βpu, which is 4 times that of standard inverter. Thus, the pull-up device is capable of sourcing about four times the current of the standard nMOS inverter.

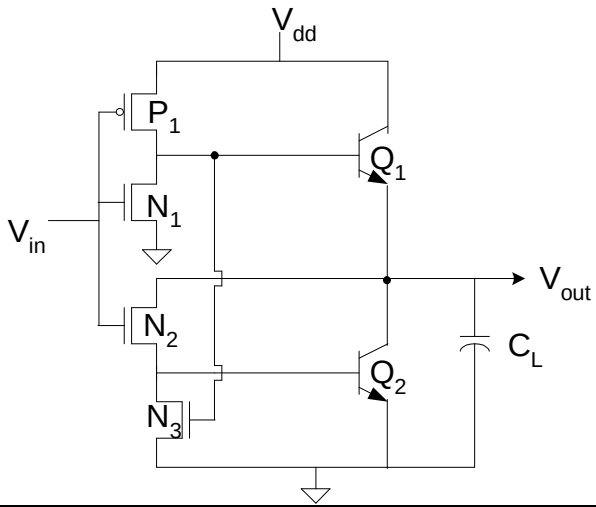


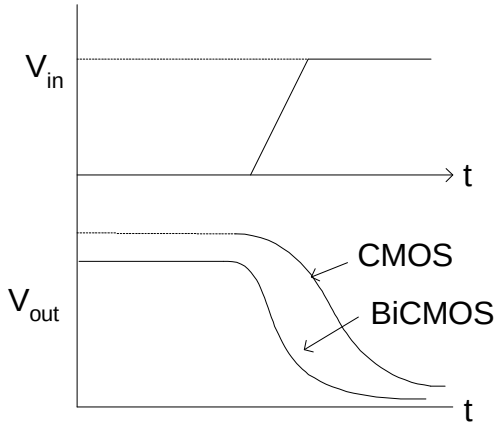
Answer to Questions of Lec-9



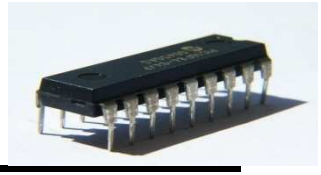
Q3. Give the schematic diagram of a Bi-CMOS inverter. Explain its operation. . Compare the switching characteristics of a BiCMOS inverter with respect to that for static CMOS for different fan out conditions.

Ans: The schematic diagram of a BiCMOS inverter is given below. Higher current drive capability of bipolar NPN transistors is used in realizing bi-CMOS inverters. The delays of CMOS and BiCMOS inverters are compared for different fan-outs. It may be noted that for fan-out of 1 or 2, CMOS provides smaller delay compared to BiCMOS. However, as fan-out increases further, BiCMOS performs better and better.





Answer to Questions of Lec-9



Q4. Design a scaled chain of inverters such that the delay time between the logic gate (C_g = 100 fF) and a load capacitance 2 pF in minimized. Find out the number of stages and stage ratio.

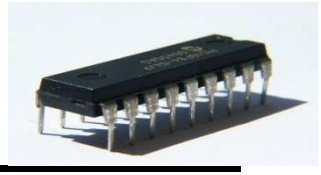
Ans: It may be noted that a MOS transistor of unit length (2λ) has gate capacitance proportional to its width (W), which may be multiple of λ. With the increase of the width, the current driving capability is increased. But, this in turn, also increases the gate capacitance. As a consequence the delay in driving a load capacitance C_L by a transistor of gate capacitance Cg is given by the relationship $\tau.C_L$ / Cg . So, delay in driving by a single stage is 2000/100 τ = 200 τ. With n stages, where n dependent on the stage ratio, the delay is

$$t_{\min} = nf\tau = e\tau \ln\left[\frac{c_L}{c_g}\right]$$

$$\text{or} \quad \ln y = \text{n} \ln f$$

$$\text{or} \quad \text{n} = \frac{\ln y}{\ln f}$$

Review Questions of Lec-10



Q1. How the transfer characteristic of a CMOS NAND gate is affected with increase in fan-in?

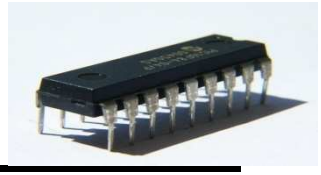
Q2. How the transfer characteristic of a CMOS NOR gate is affected with increase in fan-in?

Q3 How switching characteristic of a CMOS NAND gate is affected with increase in fan-in?

Q4. How switching characteristic of a CMOS NOR gate is affected with increase in fan-in?

Q5. How noise margin of a CMOS NAND/NOR gate is affected with increase in fan-in?

Answer to Questions of Lec-10



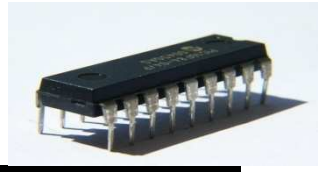
Q1. How the transfer characteristic of a CMOS NAND gate is affected with increase in fan-in?

Ans: Transfer characteristic does not remain symmetric with increase in fan-in of the NAND gate. The inversion voltage moves towards right with the increase in fan-in.

Q2. How the transfer characteristic of a CMOS NOR gate is affected with increase in fan-in?

Ans: In case of NOR gate the transfer characteristic also does not remain symmetric and the inversion voltage moves towards left with the increase in fan-in.

Answer to Questions of Lec-10



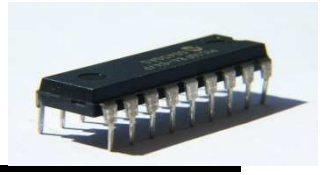
Q3 How switching characteristic of a CMOS NAND gate is affected with increase in fan-in?

Ans: When the load capacitance is relatively large, the fall time increases linearly with the increase in fan-in and the rise time is not affected much.

Q4. How switching characteristic of a CMOS NOR gate is affected with increase in fan-in?

Ans: When the load capacitance is relatively large, the rise time increases linearly with the increase in fan-in and the fall time is not affected much. For the same area, NAND gates are superior to NOR gates in switching characteristics because of higher mobility of electrons compared holes. For the same delay, NAND gates require smaller area than NOR gates

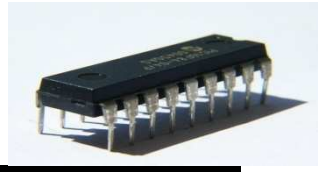
Answer to Questions of Lec-10



Q5. How noise margin of a CMOS NAND/NOR gate is affected with increase in fan-in?

Ans: Because of the change in the inversion voltage, the noise margin is affected with the increase in fan-in. For equal fan-in, noise margin is better for NAND gates compared to NOR gates. We may conclude that for equal area design NAND gates are faster and better alternative to NOR gates

Review Questions of Lec-11



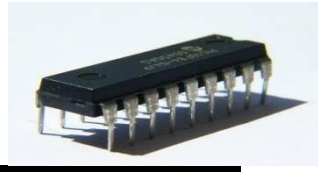
Q1. For a complex/compound CMOS logic gate, how do you realize the pull-up and the pull-down networks?

Q2. Give the two possible topologies AND-OR-INVERT AND-OR-INVERT (AOI) and OR-AND-INVERT (OAI) to realize CMOS logic gate. Explain with an example.

Q3. Give the AOI and OAI realizations for the sum and carry functions of a full adder.

Q4. How do you realize pseudo nMOS logic circuits. Compare its advantage and disadvantages with respect to standard static CMOS circuits.

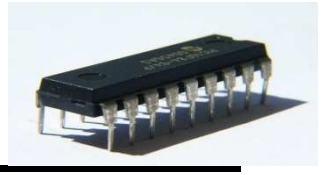
Answer to Questions of Lec-11



Q1. For a complex/compound CMOS logic gate, how do you realize the pull-up and the pull-down networks?

- **Ans: A CMOS logic gate consists of a nMOS pull-down network and a pMOS pull-up network. The nMOS network is connected between the output and the ground, whereas the pull-up network is connected between the output and the power supply. The nMOS network corresponds to the complement of the function either in sum-of-product or product-of-sum forms and the pMOS network is dual of the nMOS network .**

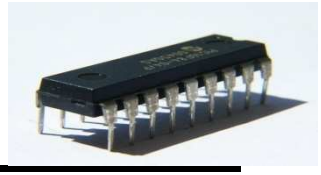
Answer to Questions of Lec-11



Q2. Give the two possible topologies AND-OR-INVERT AND-OR-INVERT (AOI) and OR-AND-INVERT (OAI) to realize CMOS logic gate. Explain with an example.

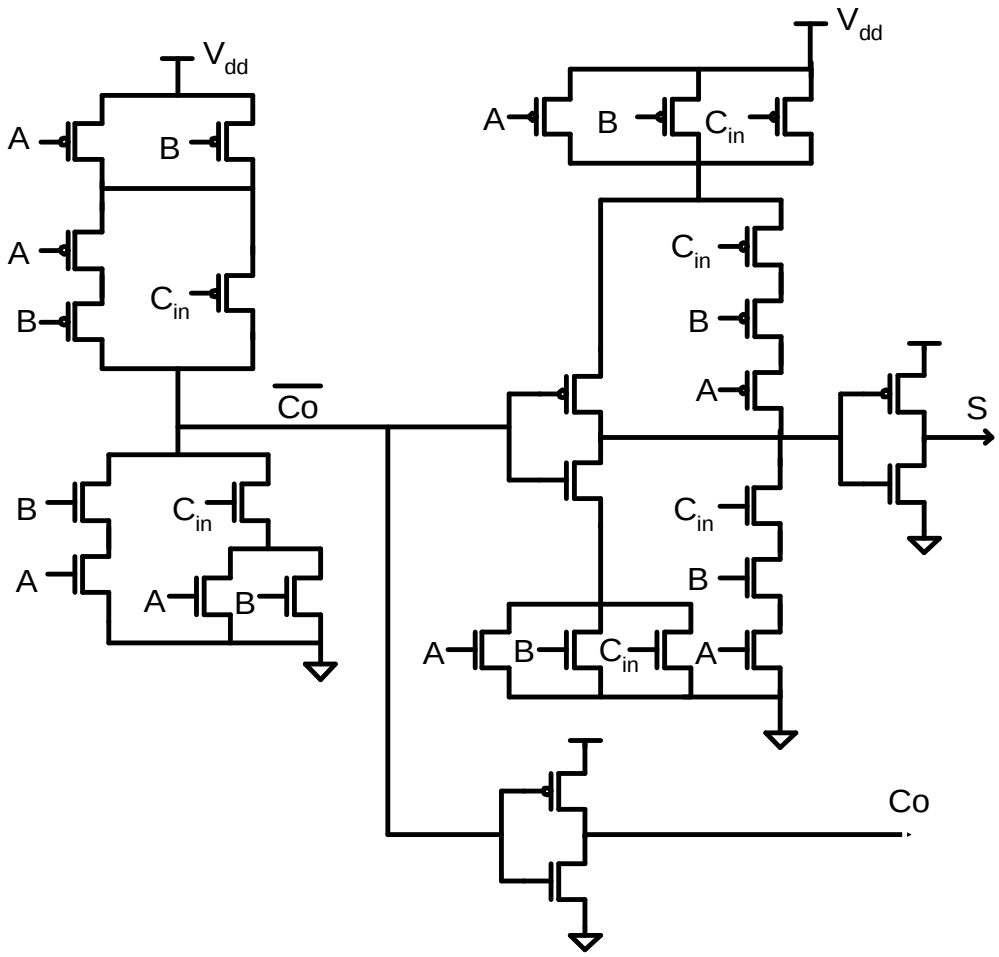
Ans: The AND-OR-INVERT network corresponds to the realization of the nMOS network in sum-of-product form. Where as the OR-AND-INVERT network corresponds to the realization of the nMOS network in product-of-sum form. In both the cases, the pMOS network is dual of the nMOS network .

Answer to Questions of Lec-11

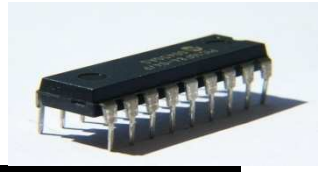


Q3. Give the AOI and OAI realizations for the sum and carry functions of a full adder.

Ans: AOI form of realization is shown in the figure.



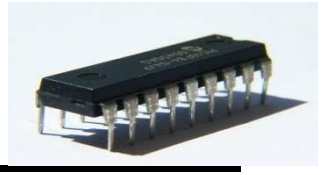
Answer to Questions of Lec-11



Q4. How do you realize pseudo nMOS logic circuits. Compare its advantage and disadvantages with respect to standard static CMOS circuits.

Ans: In the pseudo-nMOS realization, the pMOS network of the static CMOS realization is replaced by a single pMOS transistor with its gate connected to GND. An n-input pseudo nMOS requires n+1 transistors compared to 2n transistors of the corresponding static CMOS gates. This leads to substantial reduction in area and delay in pseudo nMOS realization. As the pMOS transistor is always ON, it leads to static power dissipation when the output is LOW.

Review Questions of Lec-12



Q1. In what way relay logic circuits differ from pass transistor logic circuits? Why the output of a pass transistor circuit is not used as a control signal for the next stage?

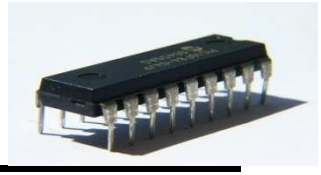
Q2. What are the advantages and limitations of pass transistor logic circuits? How the limitations are overcome?

Q3. Why is it necessary to insert a buffer after not more than four pass transistors in cascade?

Q4. Why is it necessary to have swing restoration logic in pass transistor logic circuits? Explain its operation.

Q5. What is the 'sneak path' problem of pass transistor logic circuits? How sneak path is avoided in Universal Logic Module (ULM) based realization of pass transistor network. Illustrate with an example.

Answer to Questions of Lec-12



Q1. In what way relay logic circuits differ from pass transistor logic circuits? Why the output of a pass transistor circuit is not used as a control signal for the next stage?

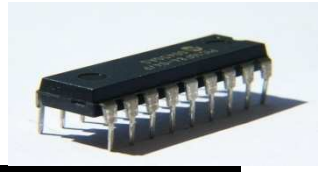
Ans: Logic functions can be realized using pass transistors in a manner similar to relay contact networks. However, there are some basic differences as mentioned below:

(a) In relay logic, output is considered to be '1' when there is some voltage passing through the relay logic. Absence of voltage is considered to be '0'. On the other hand, is case of pass transistor logic it is essential to provide both charging and discharging path for the output load capacitance.

(b) There is no voltage drop in the relay logic, but there is some voltage drop across the pass transistor network.

(c) Pass transistor logic is faster than relay logic.

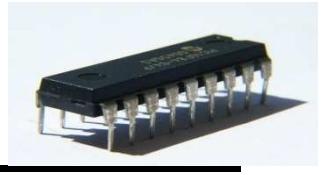
Answer to Questions of Lec-12



Q2. What are the advantages and limitations of pass transistor logic circuits? How the limitations are overcome?

Ans: Pass transistor realization is ratioless, i.e. there is no need to have L:W ration in the realization. All the transistors can be of minimum dimension. Lower area due to smaller number of transistors in pass transistor realization compared to static CMOS realization. Pass transistor realization also has lesser power dissipation because there is no static power and short-circuit power dissipation in pass transistor circuits. The limitations are (a) Higher delay in long chain of pass transistors (b) Multi-threshold Voltage drop (Vout = Vdd – Vtn) (c) Complementary control signals and (d) Possibility of sneak path because of the presence of path to Vdd and GND.

Answer to Questions of Lec-12



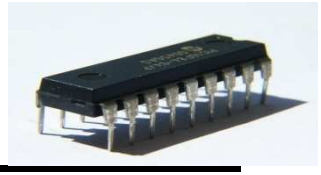
Q3. Why is it necessary to insert a buffer after not more than four pass transistors in cascade?

Ans: When a signal is steered through several stages of pass transistors, the delay can be considerable. For n stages of pass transistors, the delay is given by the relationship

$$\tau = CR_{eq}\frac{n(n+1)}{2}$$

To overcome the problem of long delay, buffers should be inserted after every three or four pass transistor stages.

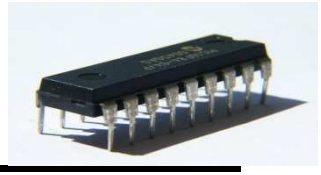
Answer to Questions of Lec-12



Q4. Why is it necessary to have swing restoration logic in pass transistor logic circuits? Explain its operation.

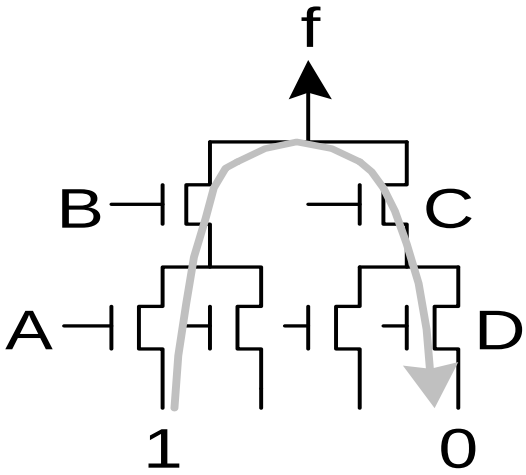
Ans: In order to avoid the voltage drop at the output (Vout = Vdd – Vtn) , it is necessary to use additional hardware known swing restoration logic at the gate output. At the output of the swing restoration logic there is rail to rail voltage swing. The swing restoration can be done using a pMOS transistor with its gate connected to GND.

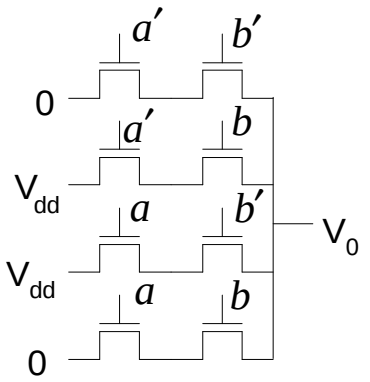
Answer to Questions of Lec-12



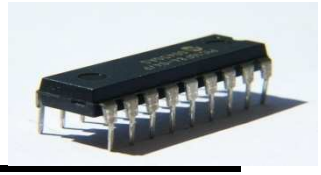
Q5. What is the 'sneak path' problem of pass transistor logic circuits? How sneak path is avoided in Universal Logic Module (ULM) based realization of pass transistor network. Illustrate with an example.

Ans: As shown in the figure, the output is connected to both '1' (Vdd) and '0' (GND). The output attains some intermediate Value between Vdd and GND. The MUX based realization allows connection of the output to only one input, which can be either 0 or 1. Multiplexer realization of $f = a'b + ab'$ **Is shown in the figure.**





Review Questions Lec-13

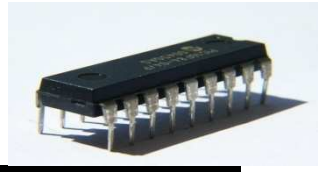


Q1. What is Shanon's Expansion Theorem? How can be used realize pass transistor circuit for a given Boolean function?

Q2. Obtain an ROBDD for the Boolean function F = ∑(3, 7, 9, 11, 12, 13, 14,15). Realize the function using a CPL circuit.

Q3. Compare the area, in terms of the number of transistors, for the three different implementations of a full adder using (i) static CMOS, (ii) domino CMOS, and (iii) complementary pass transistor logic (CPL).

Answer to Questions of Lec-13

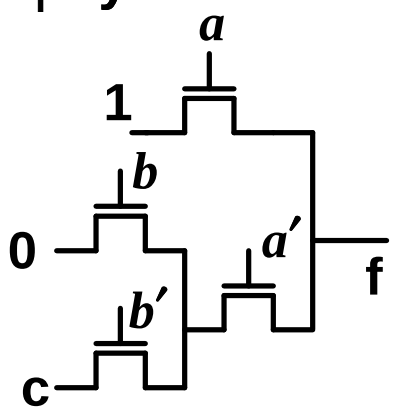


Q1. What is Shanon's Expansion Theorem? How can be used realize pass transistor circuit for a given Boolean function?

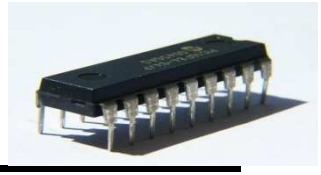
Ans: According to Shanon's expansion theorem, a Boolean function can be expanded around a variable x_i to represent the function as $f = x_i f_{xi} + x_i' f_{xi'}$, where f_{xi} and $f_{xi'}$ are the positive and negative cofactors of f, respectively. A positive Shannon cofactor of function f with respect to variable x_i is defined as that function with all instances of x_i replaced by 1. A negative Shannon cofactor is the same, but replaces all instances of x_i by 0.

This is illustrated by the following example:

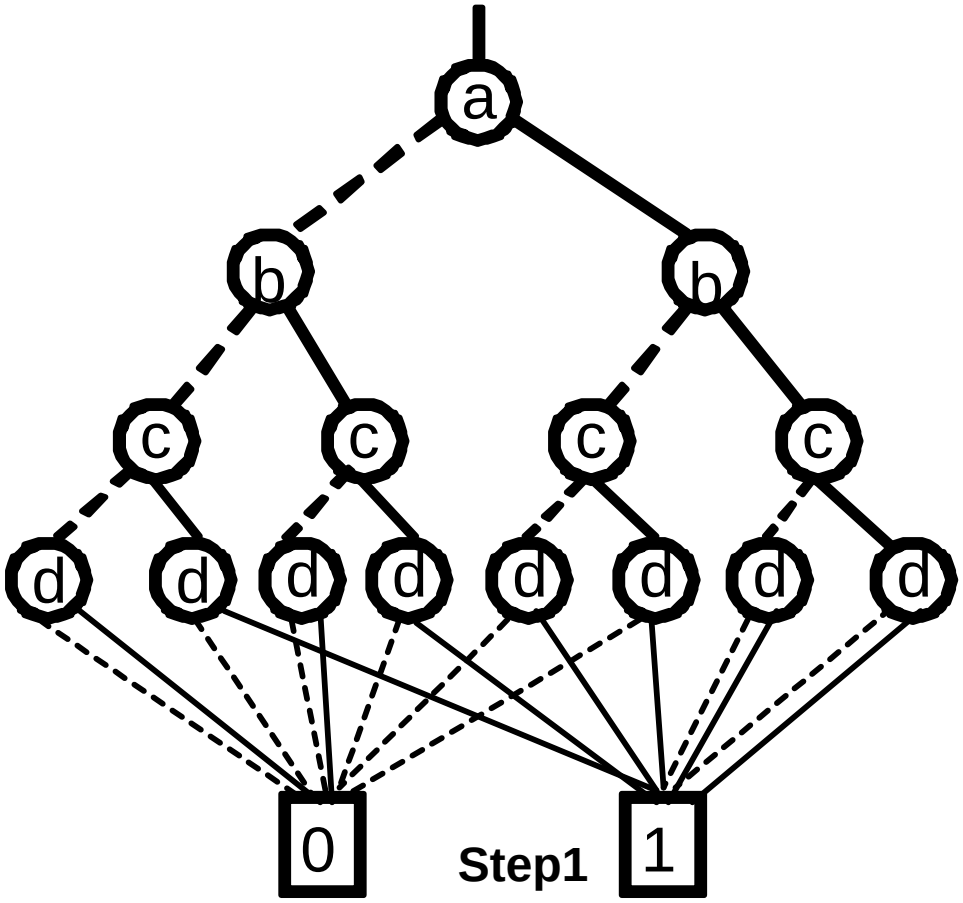
$$f = a.1 + a'(b.0 + b'.c)$$

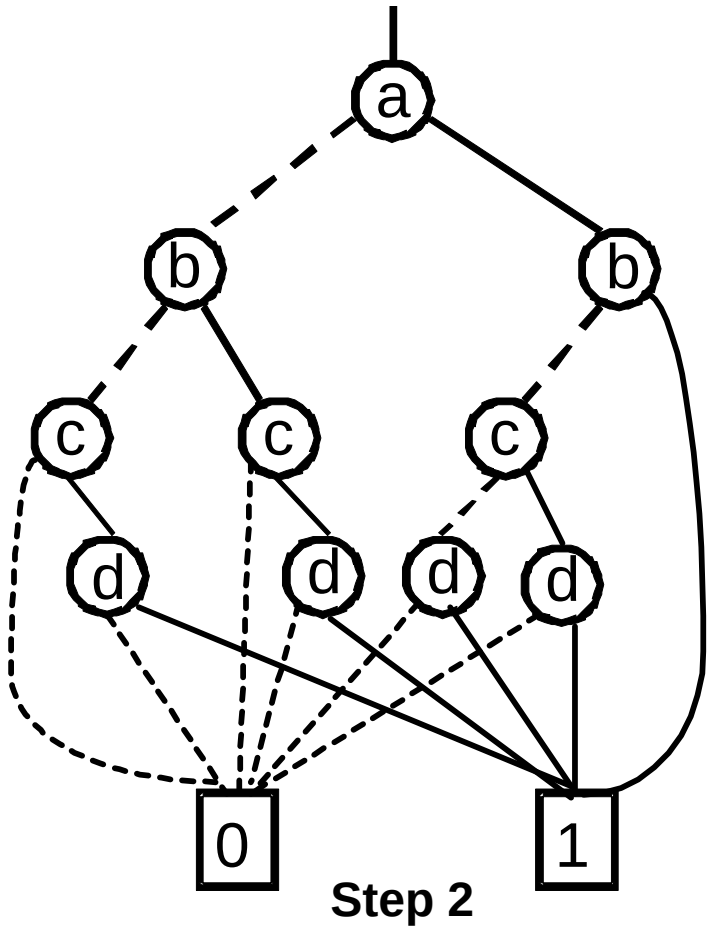


Answer to Questions of Lec-13

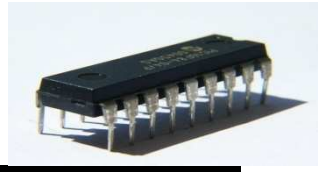


Q2. Obtain an ROBDD for the Boolean function F = ∑(3, 7, 9, 11, 12, 13, 14,15). Realize the function using a CPL circuit.

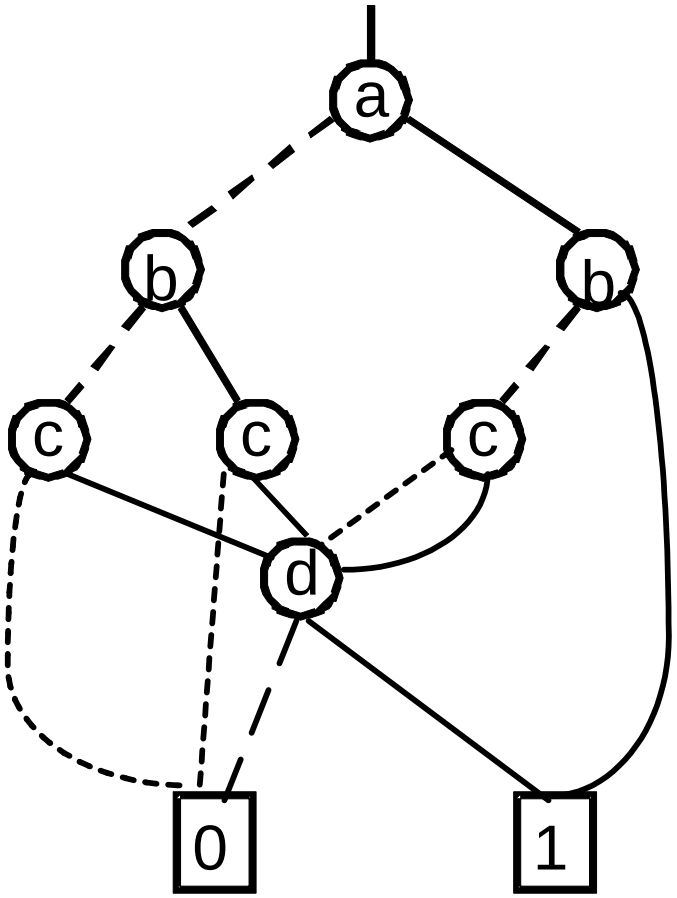




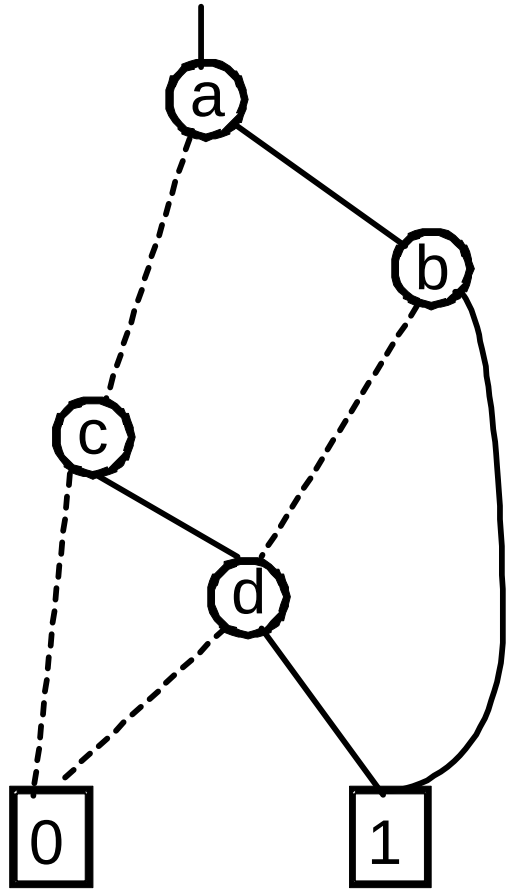
Answer to Questions of Lec-13



Ans 2:

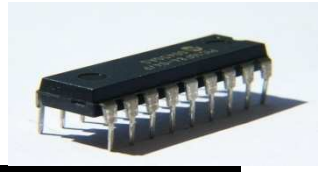


Step 3

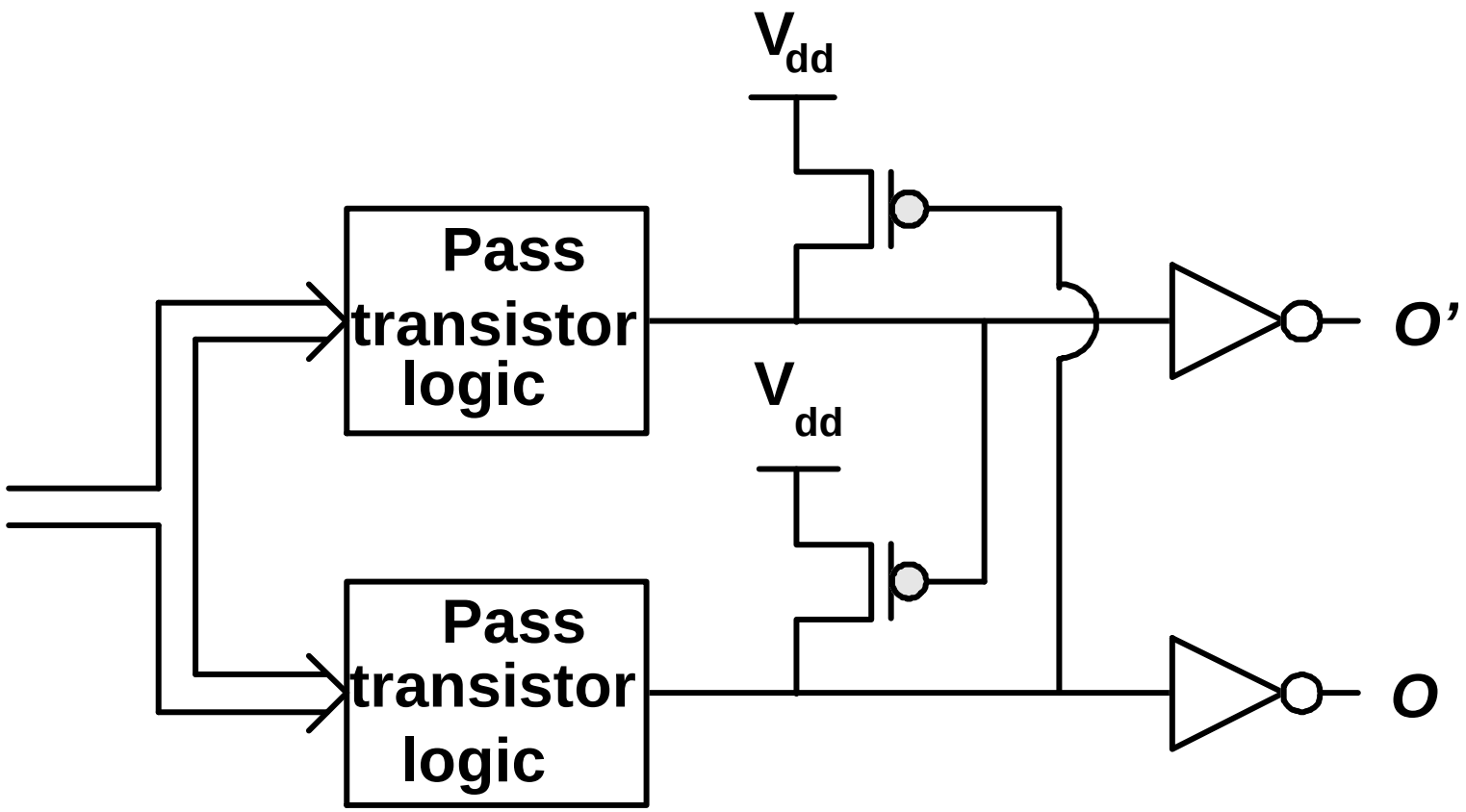


Step 4

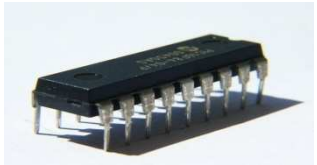
Answer to Questions of Lec-13



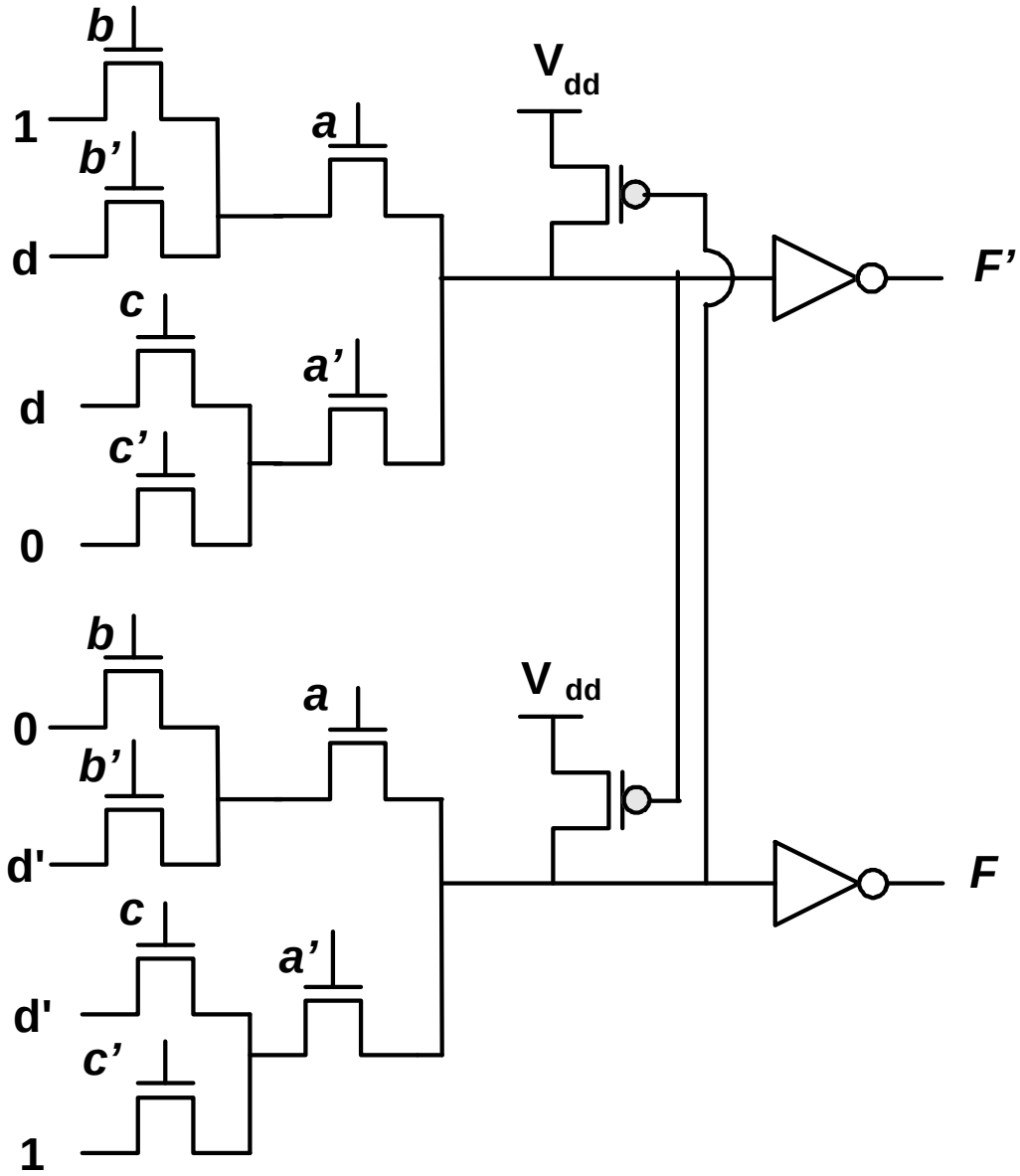
Ans 2:



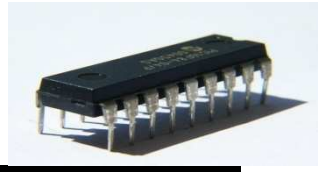
Answer to Questions of Lec-13



Ans 2:

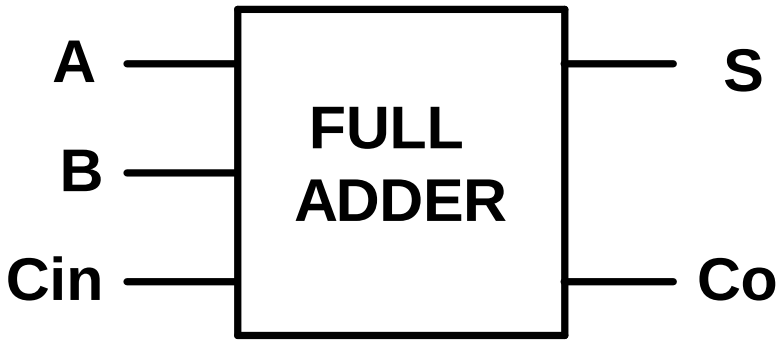


Answer to Questions of Lec-13

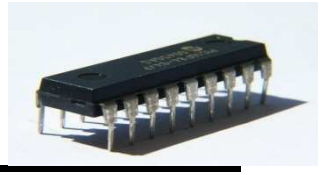


Q3. Compare the area, in terms of the number of transistors, for the three different implementations of a full adder using (i) static CMOS, (ii) domino CMOS, and (iii) complementary pass transistor logic (CPL).

Ans: The full adder block diagram is given below:



Answer to Questions of Lec-13

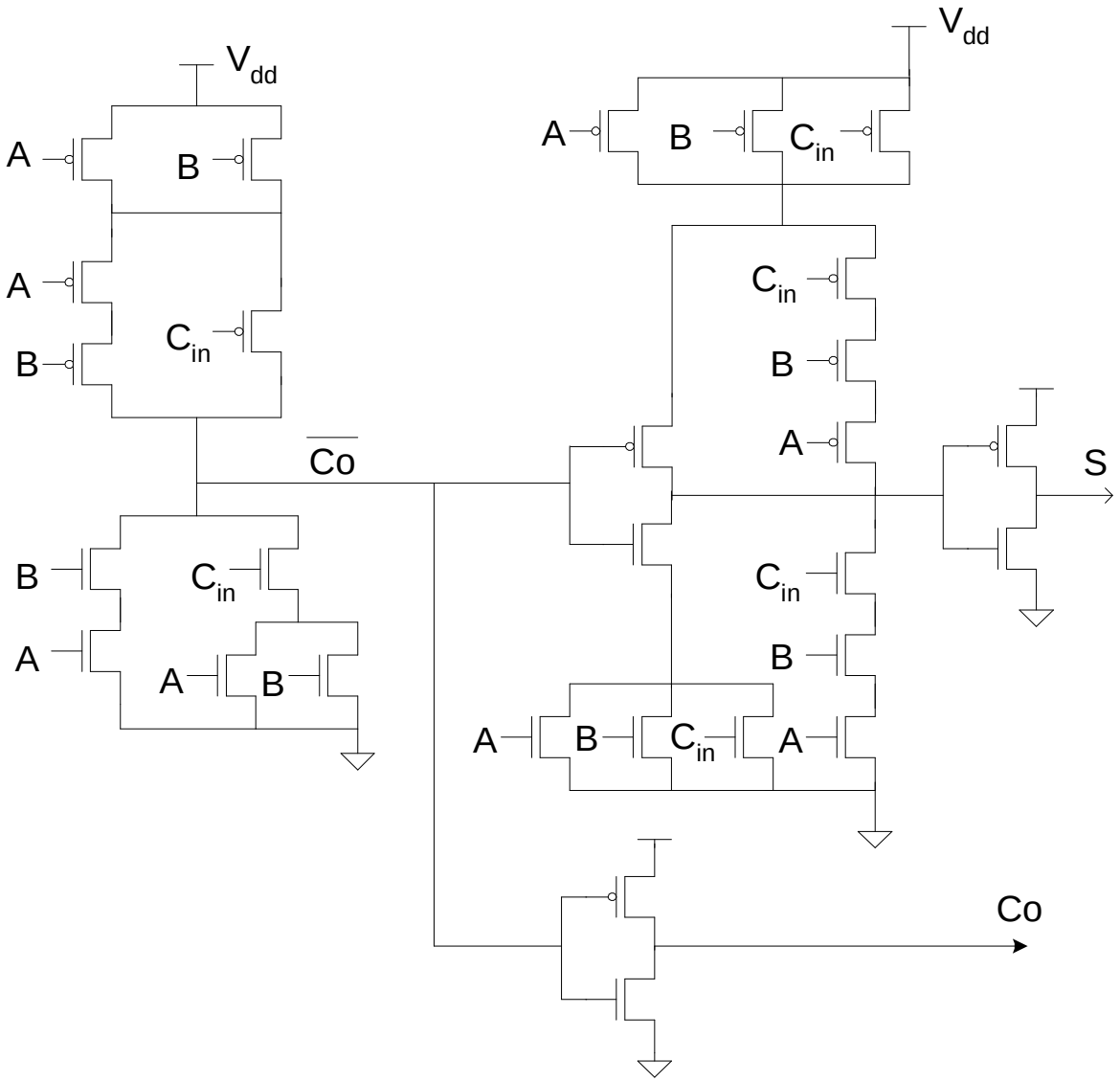


The full adder

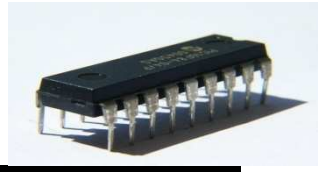
Realization using

Static CMOS is given here.

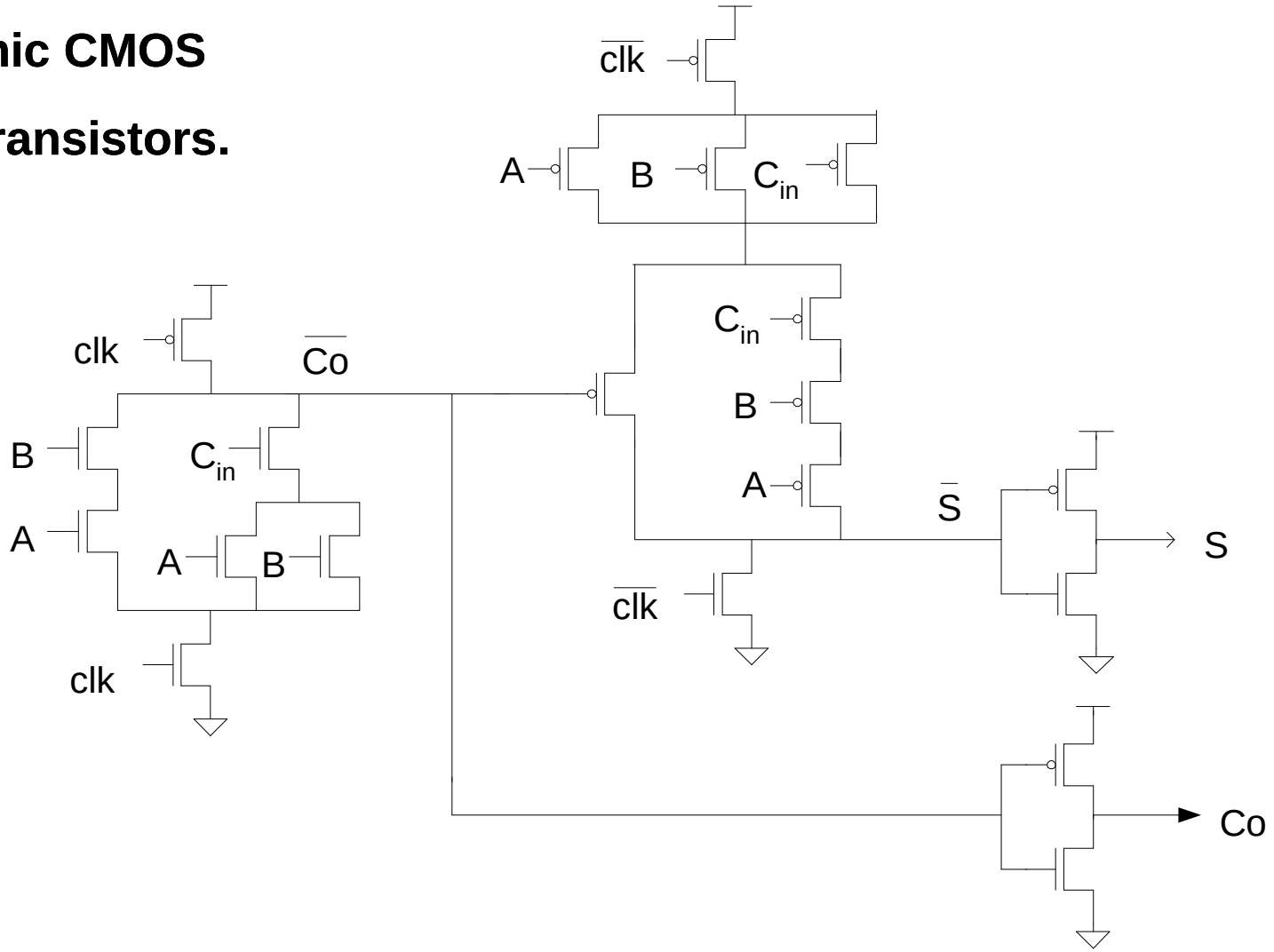
It requires 28 transistors.



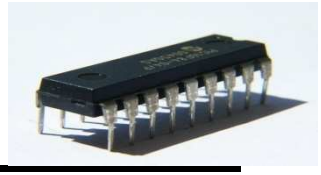
Answer to Questions of Lec-13



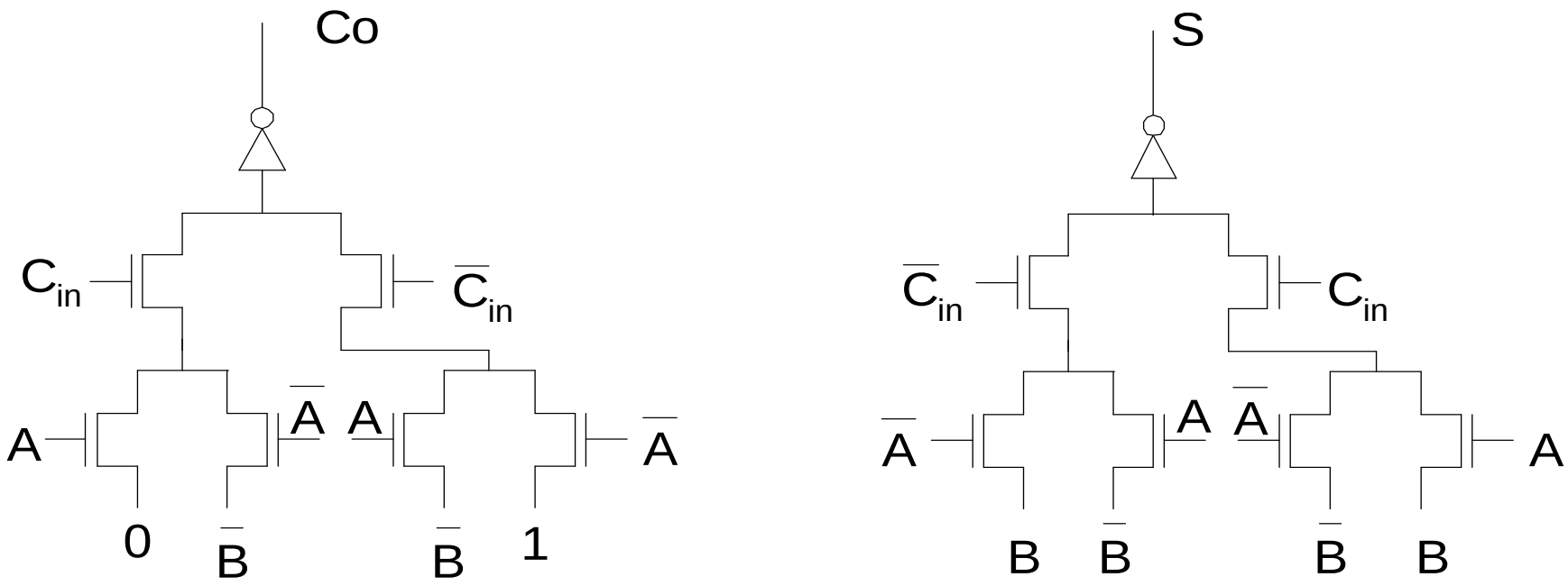
The realization using NORA dynamic CMOS requires 20 transistors.



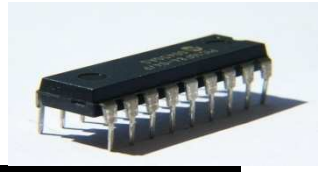
Answer to Questions of Lec-13



The pass transistor realization of the full adder is given below. It requires 16 (8+8) transistors.



Review Questions of Lec-14



Q1. What are the key characteristics of MOS dynamic circuits?

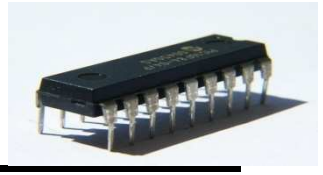
Q2. Explain the basic operation of a 2-phase dynamic circuit?

Q3. How 2-phase clocks can be generated using inverters?

Q4. What makes dynamic CMOS circuits faster than static CMOS circuits?

Q5. Compare the sources of power dissipation between static CMOS and dynamic CMOS circuits?

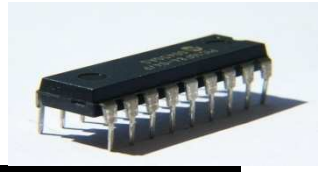
Answer to Questions of Lec-14



Q1. What are the key characteristics of MOS dynamic circuits?

Ans: The advantage of low power of static CMOS circuits and smaller chip area of nMOS circuits are combined in dynamic circuits leading to circuits of smaller area and lower power dissipation. Smaller area due to lesser number of transistors (n+2) compared to static CMOS realization requiring 2n transistors to realize a n-variable function. Dynamic CMOS circuits have Lower static power dissipation because of smaller capacitance. There is no short circuit power dissipation and no glitching power dissipation. Dynamic CMOS circuits are also faster because the capacitance is about half that of the static CMOS circuits.

Answer to Questions of Lec-14

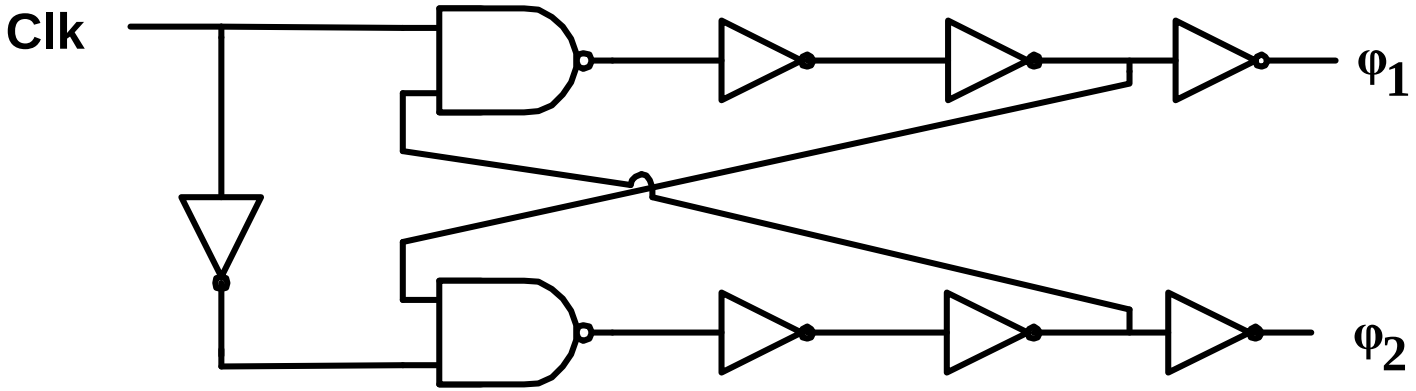


Q2. Explain the basic operation of a 2-phase dynamic circuit?

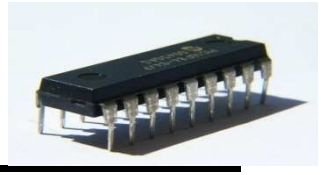
Ans: The operation of the circuit can be explained using precharge logic in which the output is precharged to HIGH level during $\phi 2$ clock and the output is evaluated during $\phi 1$ clock.

Q3. How 2-phase clocks can be generated using inverters?

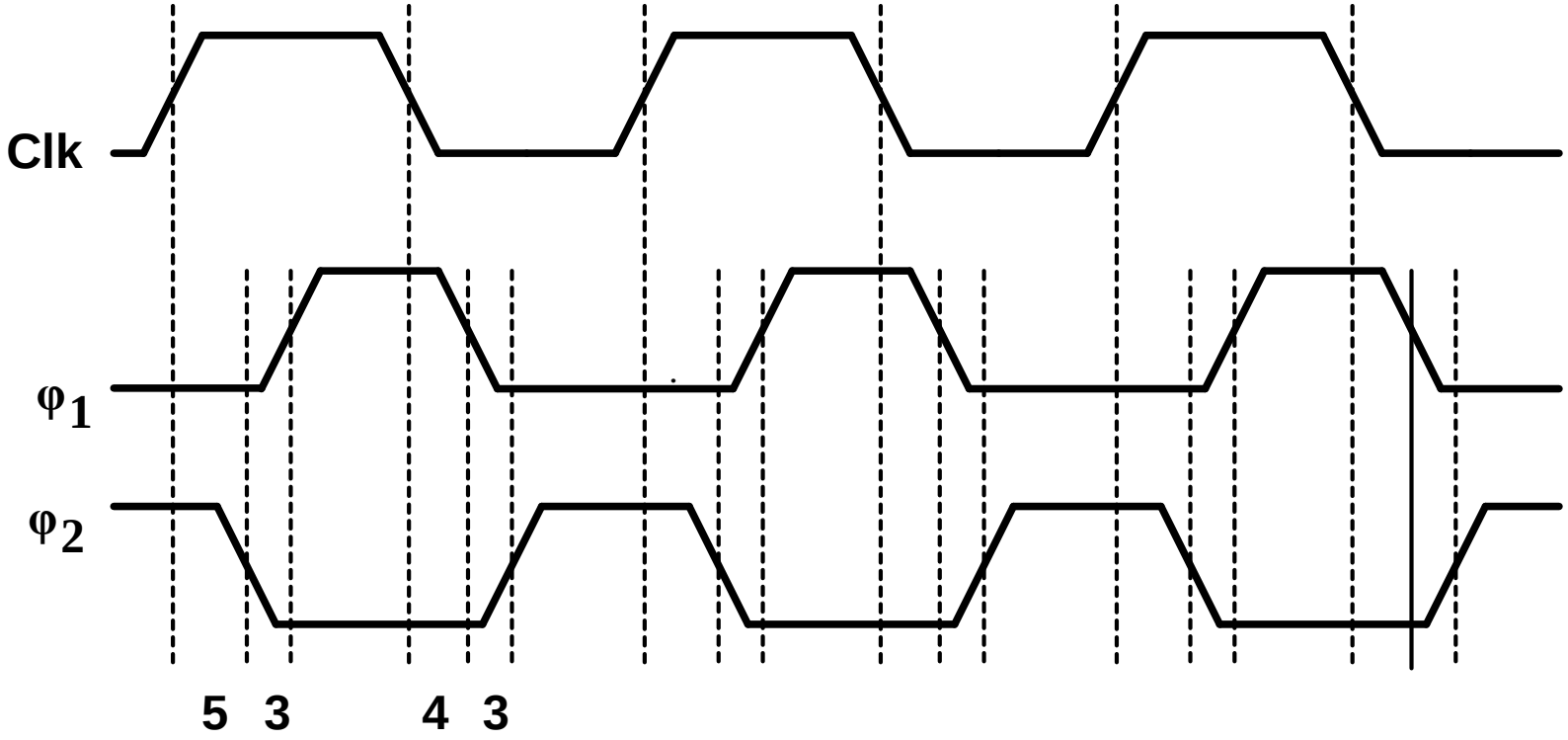
Ans: As shown below, two phase clock can generated using inverters. The timing diagram is given in the next slide.



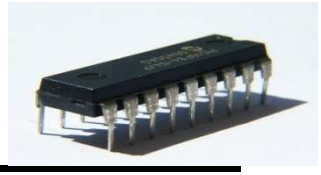
Answer to Questions of Lec-14



Timing diagram of the two-phase clock generated from a single-phase clock.



Answer to Questions of Lec-14



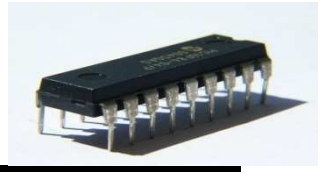
Q4. What makes dynamic CMOS circuits faster than static CMOS circuits?

Ans: As MOS dynamic circuits require lesser number of transistors and lesser capacitance is to be driven by it. This makes MOS dynamic circuits faster.

Q5. Compare the sources of power dissipation between static CMOS and dynamic CMOS circuits?

Ans: In both the cases there is switching power and leakage power dissipations. However, the short circuit and glitching power dissipations, which are present in static CMOS circuits, are not present in dynamic CMOS circuits.

Review Questions of Lec-15



Q1. What is charge leakage problem of dynamic CMOS circuits? How is it overcome?

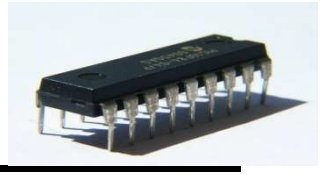
Q2. What is charge sharing problem? How can it be overcome?

Q3. Explain the clock skew problem of dynamic CMOS circuits?

Q4. How clock skew problem is overcome in in domino CMOS circuits?

Q5. How clock skew problem is overcome in in NORA CMOS circuits?

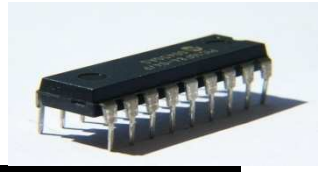
Answer to Questions of Lec-15



Q1. What is charge leakage problem of dynamic CMOS circuits? How is it overcome?

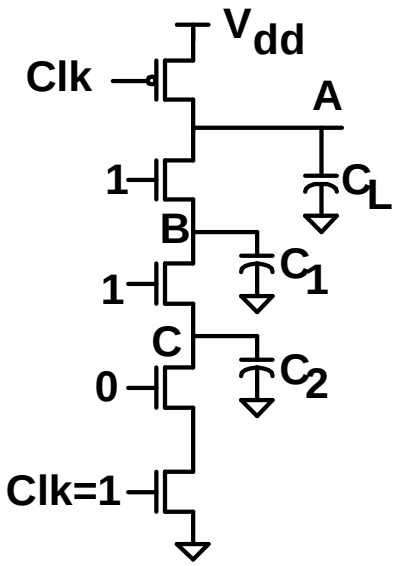
Ans: The source-drain diffusions form parasitic diodes with the substrate. There is reverse bias leakage current .The current is in the range 0.1nA to 0.5nA per device at room temperature and the current doubles for every 10°C increase in temperature . This leads to slow but steady discharge of the charge on the capacitor, which represent information. This needs to be compensated by refreshing the charge at regular interval.

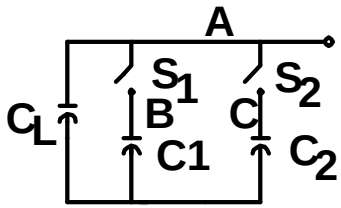
Answer to Questions of Lec-15



Q2. What is charge sharing problem of dynamic CMOS circuits?

Ans: The charge sharing problem is illustrated in the following diagram





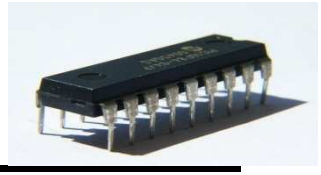
Before the switches are closed, the charge on C_L is given by $QA = V_{dd}\ C_L$ and charges at node B and C are $Q_B = 0$ and $Q_C = 0$

After the switches are closed, there will be redistribution of charges based of charge conservation principle, and the voltage V_A at node A is given by VA, which is less than Vdd.

$$C_L V_{dd} = (C_L + C_1 + C_2) V_{A.}$$

$$V_A = \frac{C_L}{(C_L + C_1 + C_2)} V_{dd}$$

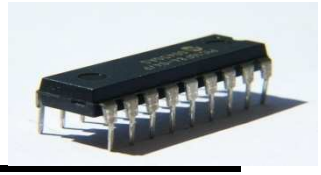
Answer to Questions of Lec-15



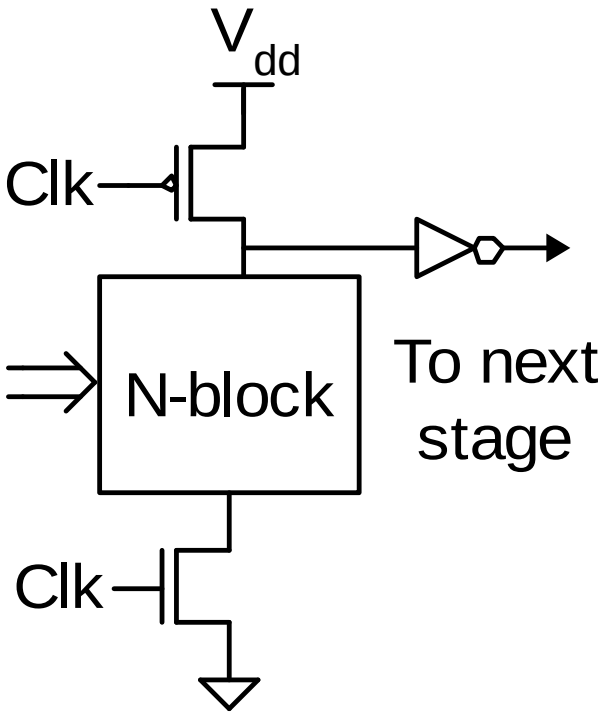
Q3. Explain the clock skew problem of dynamic CMOS circuits?

Ans: Clock skew problem arises because of delay due to resistance and parasitic capacitances associated with the wire that carry the clock pulse and this delay is approximately proportional to the square of the length of the wire. When the clock signal reaches a later stage before its preceding stage, the precharge phase of the preceding stage overlaps with the evaluation phase of the later stage, which may lead to premature discharge of the load capacitor and incorrect output during evaluation phase.

Answer to Questions of Lec-15

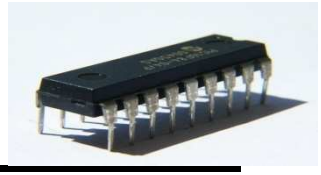


Q4. How clock skew problem is overcome in in domino CMOS circuits?



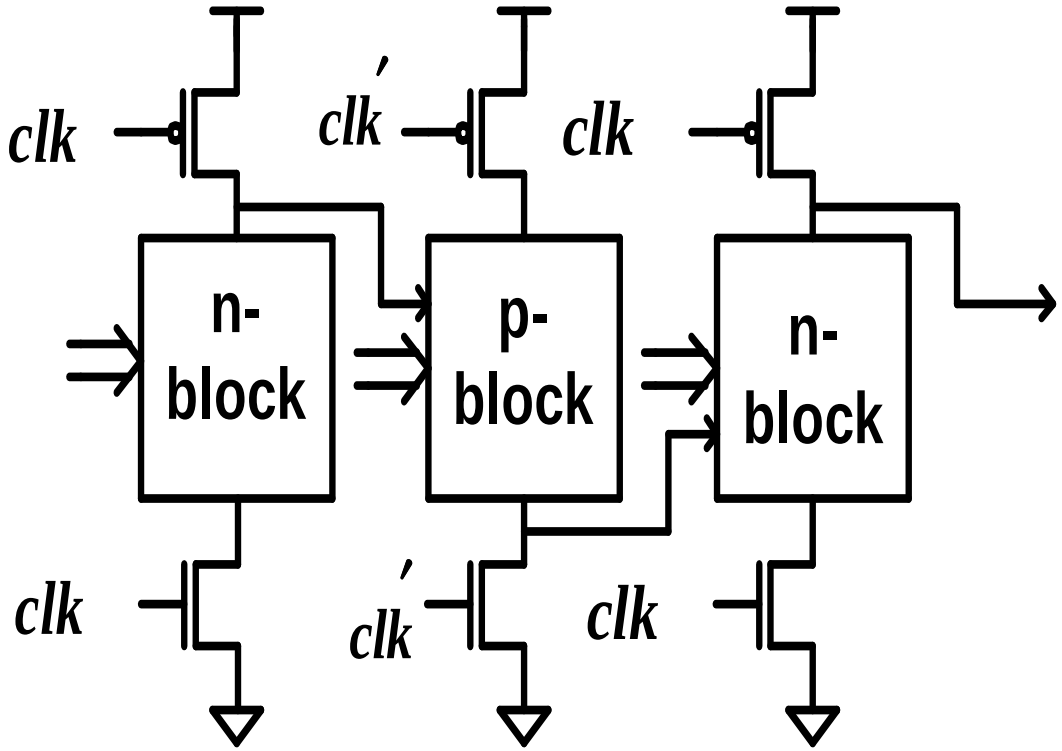
Ans: In domino CMOS circuits the problem is overcome by adding an inverter as shown in the diagram. It consists of two distinct components: The first component is a conventional dynamic CMOS gate and the second component is a static inverting CMOS buffer . During precharge phase, the output of the dynamic gate is high, but the output of the inverter is LOW. As a consequence it cannot drive an nMOS transistor ON. So, the clock skew problem is overcome.

Answer to Questions of Lec-15

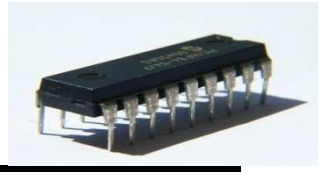


Q5. How clock skew problem is overcome in in NORA CMOS circuits?

Ans: The problem can be overcome using NORA logic, nMOS and pMOS transistor networks are alternatively used. The output of an nMOS block is HIGH during precharge, which cannot turn a pMOS transistor ON. Similarly, the output of an pMOS block is LOW during precharge, which cannot turn a nMOS transistor ON.



Review Questions of Lec-16



Q1. Distinguish between Mealy and Moore machines.

Q2. A sequence detector produces a '1' for each occurrence of the input sequence '1001' at its input.

(a) Draw the state-transition diagram of the FSM realizing the sequence detector.

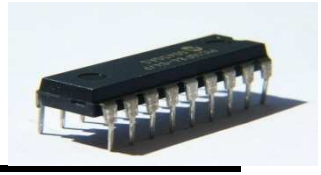
(b) Obtain state table from the state transition diagram.

(c) Realize the FSM using D FFs and a PLA.

Q3. How can you realize a set of Boolean functions using a ROM.

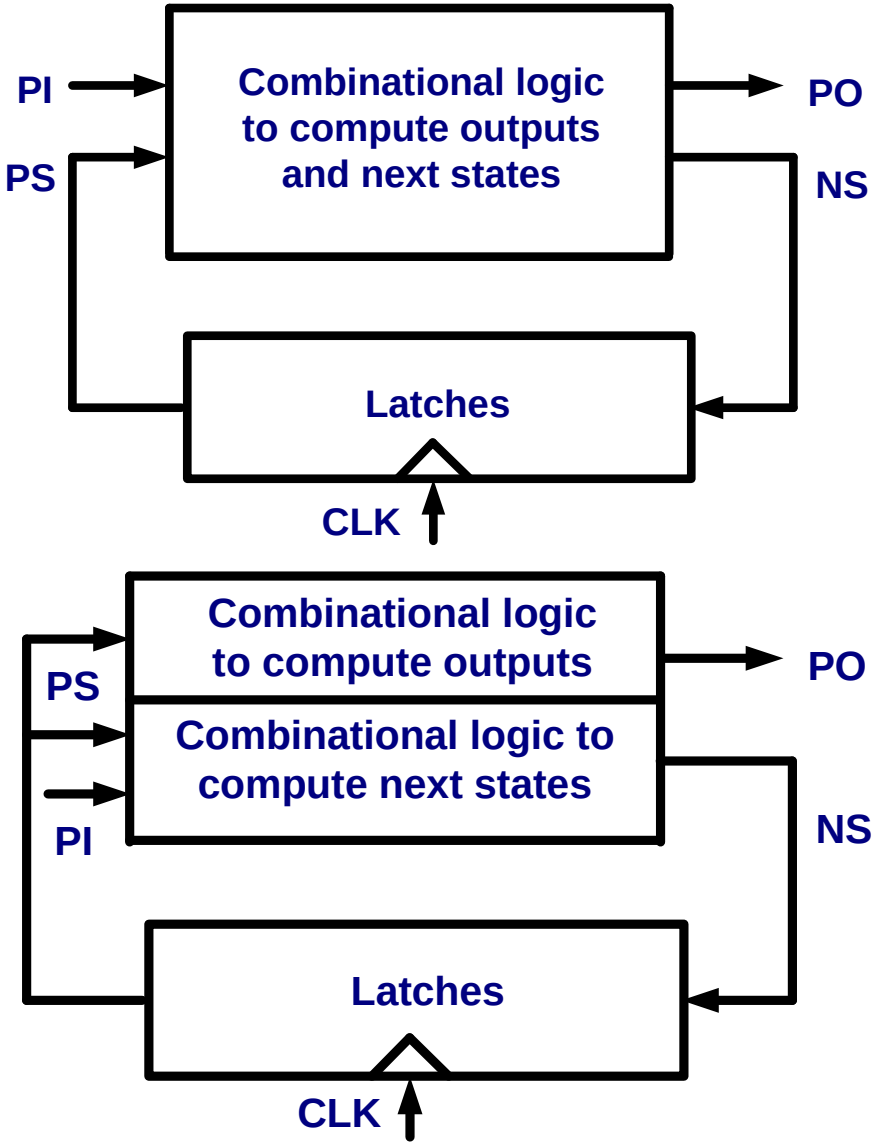
Q4. How the limitations of a ROM-based realization is overcome in a PLA-based realization.

Answer to Questions of Lec-16

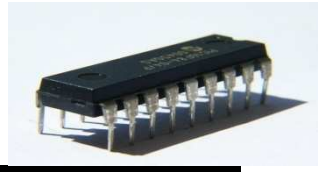


Q1. Distinguish between Mealy and Moore machines.

Ans: In a Mealy machine the outputs are dependent on the inputs and present state. The Output transition function is represented by $Z = \lambda(S,X)$. Where as in a Moore machine the outputs are dependent only on present state. The output transition function is represented by $Z = \lambda(S)$



Answer to Questions of Lec-16



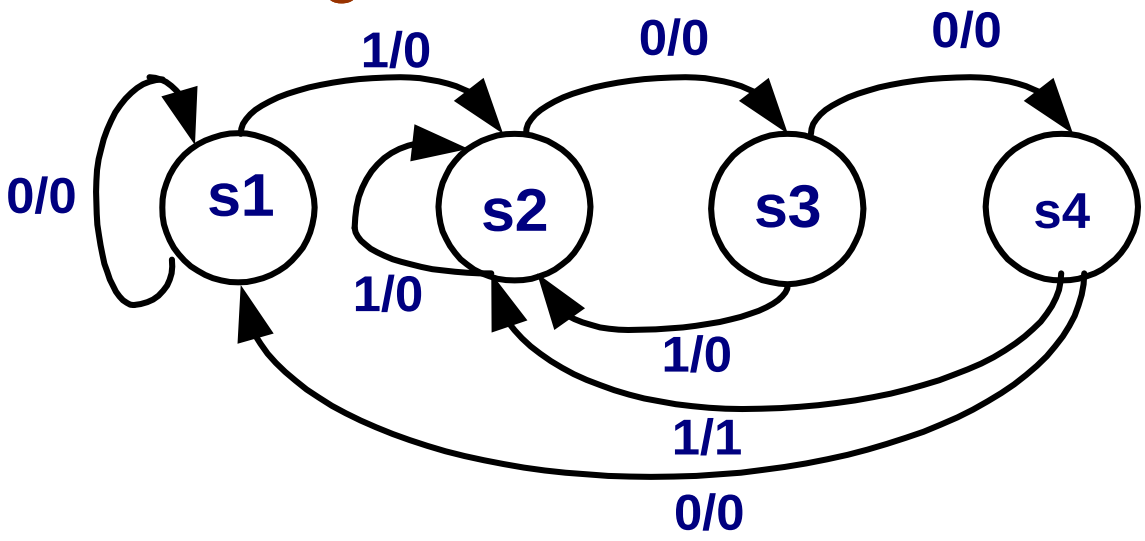
Q2. A sequence detector produces a ’1’ for each occurrence of the input sequence ‘1001’ at its input.

(a) Draw the state-transition diagram of the FSM realizing the sequence detector.

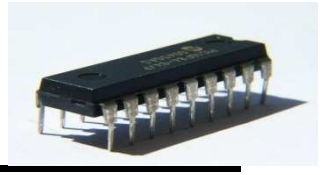
(b) Obtain state table from the state transition diagram.

(c) Realize the FSM using D FFs and a PLA.

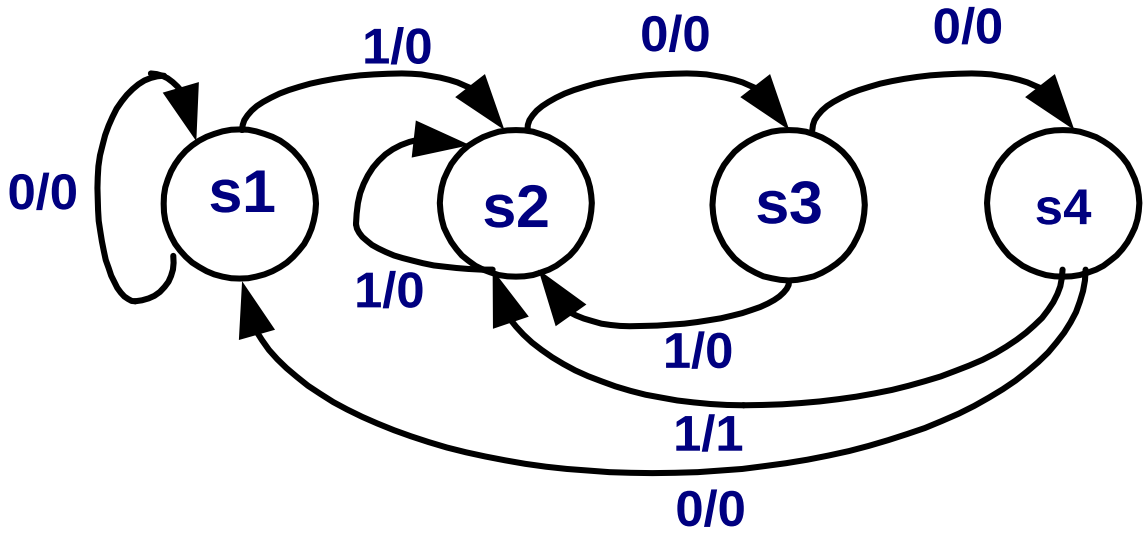
Ans: 2(a)



Answer to Questions of Lec-16

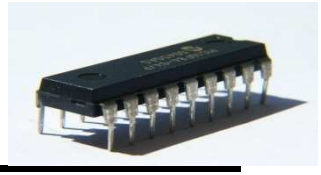


Ans: 2(b) The state table from the state transition diagram is given below:



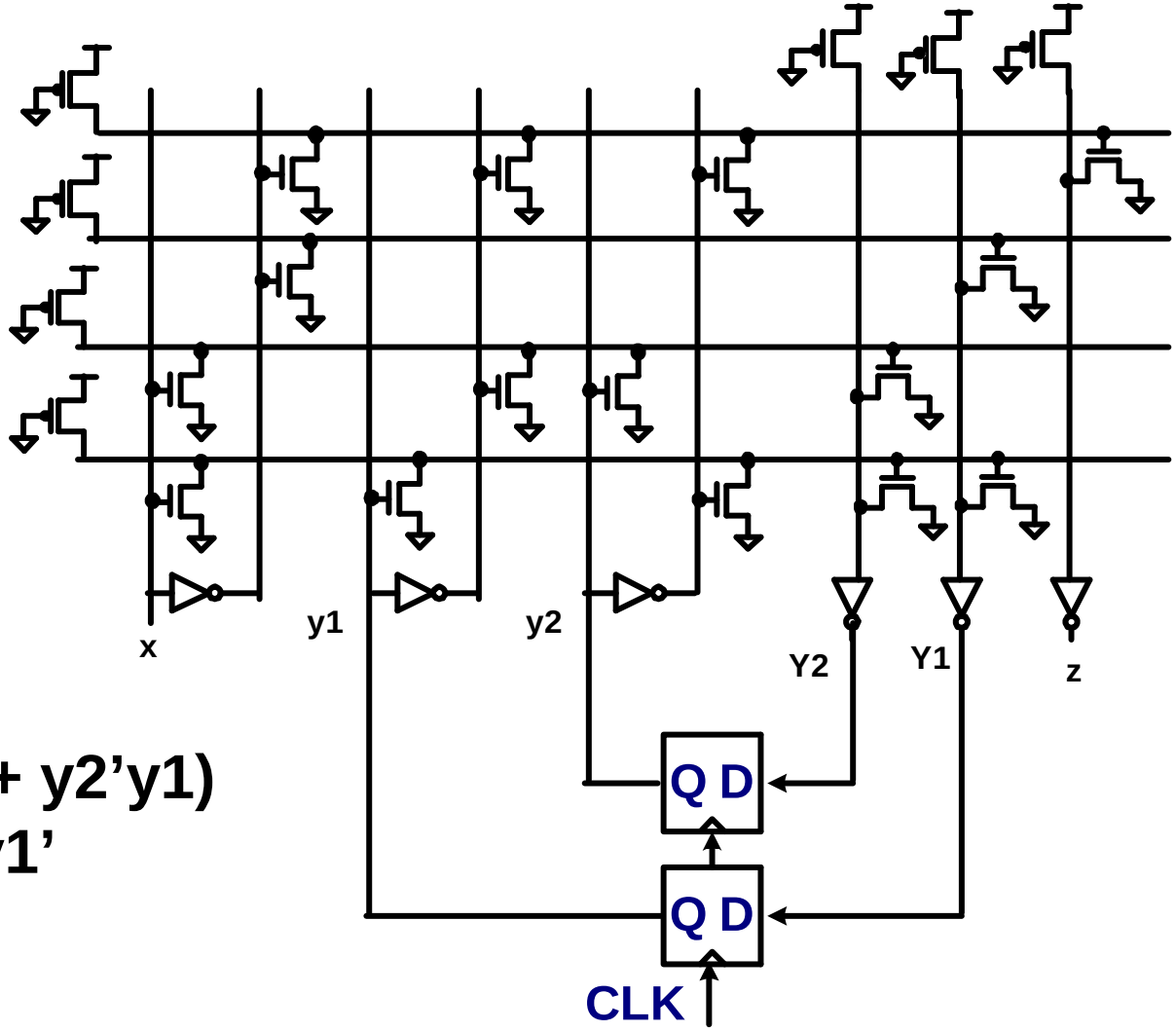
		Y2Y1, z	
PS	y2y1	x =0	X = 1
S1	0 0	00,0	01,0
S2	01	10,0	01,0
S3	1 0	11,0	01,0
S4	1 1	00,0	01,1

Answer to Questions of Lec-16



Ans: 2(c)

Realization of the FSM using D FFs and a PLA is shown in the diagram.

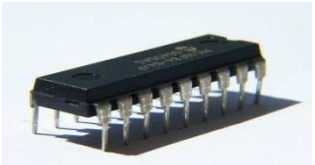


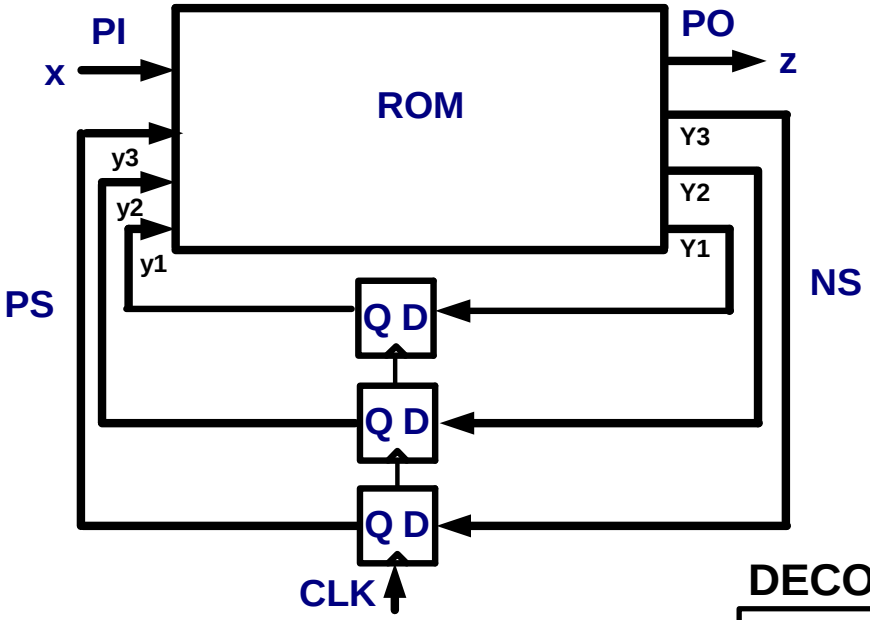
$Y2 = x'(y2y1' + y2'y1)$

$Y1 = x + x'y2y1'$

$z = xy2y1$

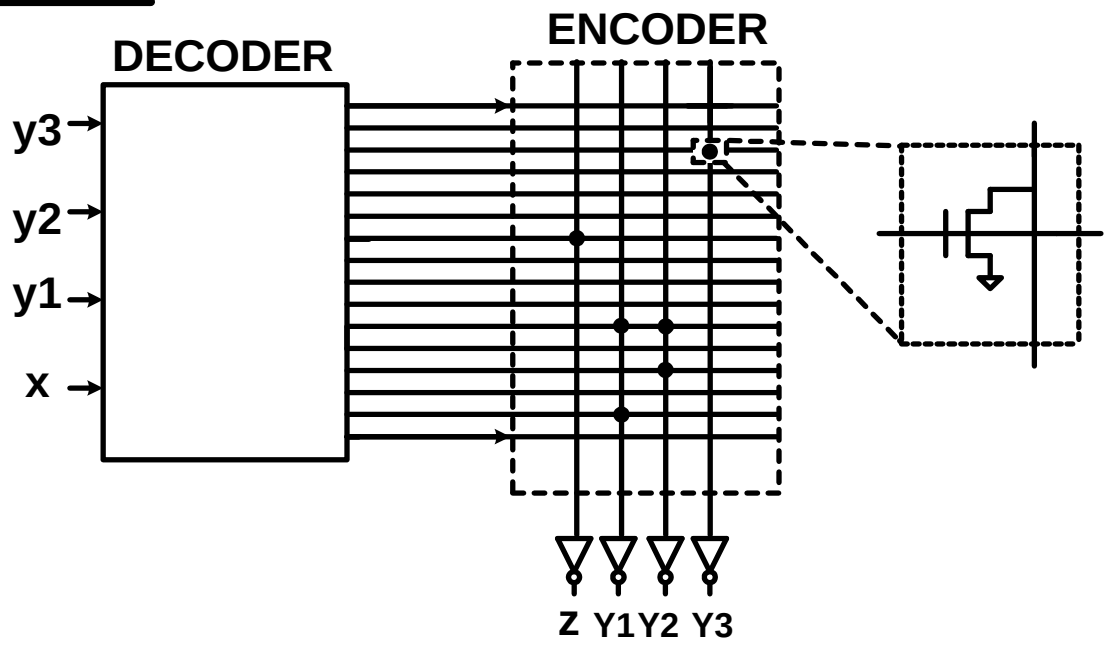
Answer to Questions of Lec-16



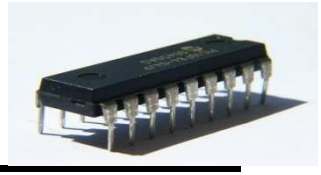


Q3. How can you realize a set of Boolean functions using a ROM?

Ans: ROMs can be used to realize a set of Boolean functions as show In the diagram. Encoder part of the ROM is realized according to the functions.



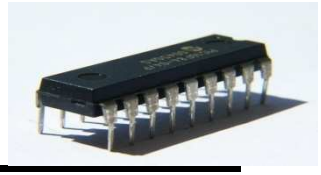
Answer to Questions of Lec-16



Q4. How the limitations of a ROM-based realization is overcome in a PLA-based realization.

Ans: In a ROM, the encoder part is only programmable and use of ROMs to realize Boolean functions is wasteful in many situations because there is no cross-connect for a significant part . This wastage can be overcome by using Programmable Logic array (PLA), which requires much lesser chip area.

Review Questions of Lec-17



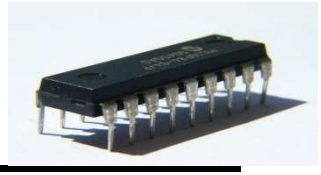
Q1. Sketch the schematic diagram of a SRAM memory cell along with sense amplifier and data write circuitry.

Q2. Explain how read and write operations are performed in a SRAM.

Q3. In what way the DRAMs differ from SRAMs?

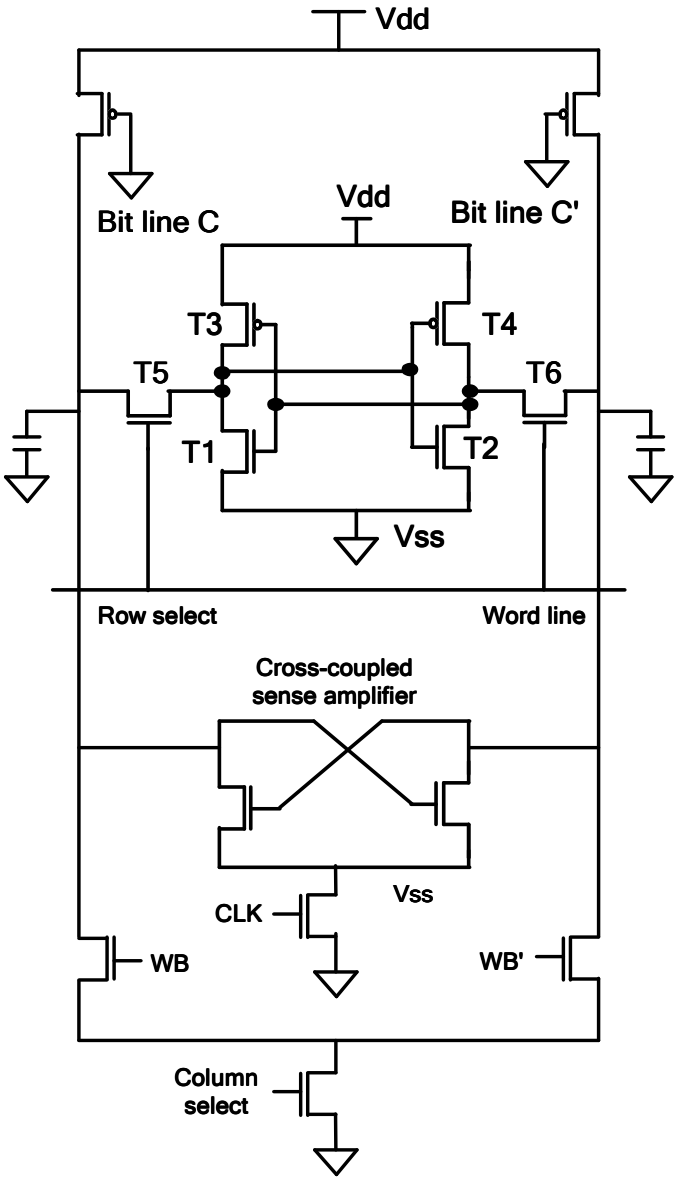
Q4. Explain the read and write operations for a one-transistor DRAM cell.

Answer to Questions of Lec-17

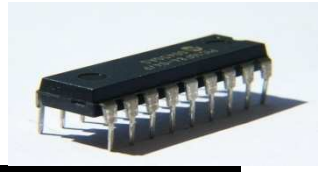


Q1. Sketch the schematic diagram of a SRAM memory cell along with sense amplifier and data write circuitry.

Ans: The schematic diagram of a SRAM memory along with the sense amplifier and data write circuitry



Answer to Questions of Lec-17



Q2. Explain how read and write operations are performed.

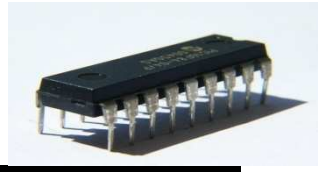
Ans: Steps of READ operation:

1. **Precharge and equalization circuit is activated to precharge the bus lines to Vdd/2**
2. **The word line is activated connecting the cell to B and B' lines. As a consequence, a voltage is developed between B and B'.**
3. **Once adequate voltage is developed between B and B', the sense amplifier amplifies the signals to rail to rail using regenerative action. The output is then directed to the chip I/O pin by the column decoder.**

Steps of write operation:

1. The data available on the chip I/O pin re directed to the B and B' lines. By activating the word line signal, the data is transferred to the memory cell

Answer to Questions of Lec-17



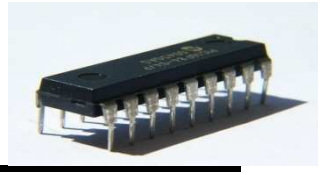
Q3. In what way the DRAMs differ from SRAMs?

Ans: Both SRAMS and DRAMs are volatile in nature, i.e. information is lost if power line is removed. However, SRAMs provide high switching speed, good noise margin but require larger chip area than DRAMs.

Q4. Explain the read and write operations for a one-transistor DRAM cell.

Ans: A significant improvement in the DRAM evolution was to realize 1-T DRAM cell. One additional capacitor is explicitly fabricated for storage purpose. To store '1', it is charged to Vdd-Vt and to store '0' it is discharged to 0V. Read operation is destructive. Sense amplifier is needed for reading. Read operation is followed by restoration operation.

Review Questions of Lec-18



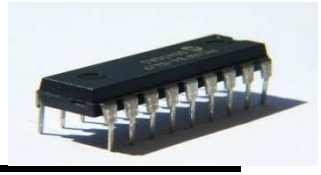
Q1. How charge sharing leads to power dissipation?

Q2. What is short circuit power dissipation? On what parameters does it depend?

Q3. Justify the statement; “there is no short circuit power dissipation in a static CMOS circuit if Vdd < (Vtn + !Vtp!)”

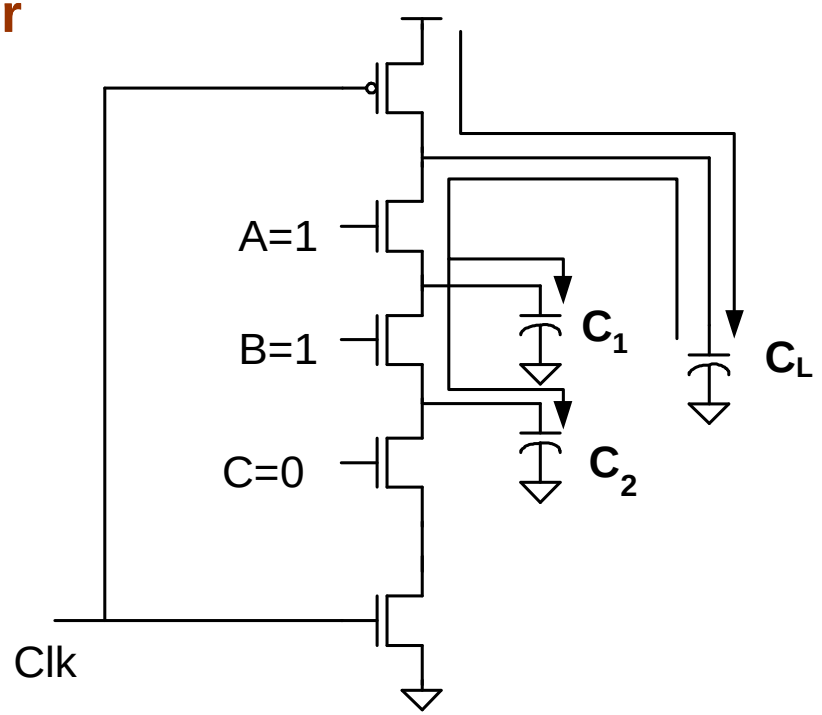
Q4. What is glitching power dissipation? How can it be minimized?

Answer to Questions of Lec-18

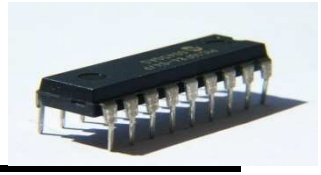


Q1. How charge sharing leads to power dissipation?

Ans: In case of dynamic gates, power dissipation takes place due to the phenomenon of charge sharing even when the output is not 0 at the time evaluation. At the time of precharge, the output is charged to Vdd, but at the time of evaluation, the output decreases because of the of the sharing of charge by the two capacitors C1 and C2. In the next precharge phase a power dissipation equal to P takes place.



Answer to Questions of Lec-18



After charge sharing, the new voltage level is Vnew. Because of the conservation of charge, we get

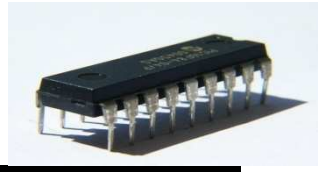
$$(C_1 + C_2 + C_L).V_{new} = V_{dd} C_L$$

$$V_{new} = \frac{C_L V_{dd}}{C_1 + C_2 + C_3}$$

$$\Delta V = V_{dd} - \frac{C_L}{C_1 + C_2 + C_L}.V_{dd} \qquad \frac{C_1 + C_2}{C_1 + C_2 + C_L}.V_{dd}$$

$$P = C_L.V_{dd}.\Delta V = \frac{C_L.(C_1 + C_2)}{(C_1 + C_2 + C_L)} V_{dd}^2$$

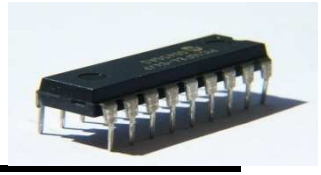
Answer to Questions of Lec-18



Q2. What is short circuit power dissipation? On what parameters does it depend?

Ans: As input changes slowly, power dissipation takes place even when there is no load or parasitic capacitor. When the input is greater than Vtn and less than (Vdd – Vtp), both the nMOS and pMOS transistors are ON. The supply voltage is now shorted to GND through the two transistors. This leads to the short circuit power dissipation.

Answer to Questions of Lec-18



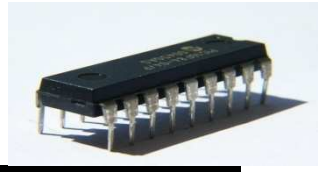
Q3. Justify the statement; "there is no short circuit power dissipation in a static CMOS circuit if Vdd < (Vtn + !Vtp!)".

Ans: When Vdd < (Vtn + !Vtp!), only one thansistor can turn on at a time. Since bothe transistors cannot turn on simultaneously, there is no short circuit power dissipation.

Q4. What is glitching power dissipation? How can it be minimized?

Ans: Because of finite delay of the gates used to realize Boolean functions, different signals cannot reach the inputs of a gate simultaneously. This leads to spurious transitions at the output before it settles down to its final value. The spurious transitions leads to charging and discharging of the outputs causing glitching power dissipation. It can be minimized by having balanced realization having same delay at the inputs.

Review Questions of Lec-19



Q1. List various sources of leakage currents.

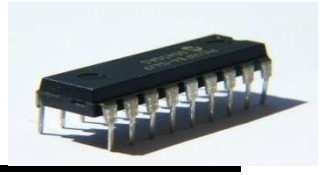
Q2. Why leakage power is an important issue in deep submicron technology?

Q3. What is band-to-band tunneling current?

Q4. What is body effect?

Q5. What is subthreshold leakage current? Briefly discuss various mechanisms responsible for this leakage current?

Answer to Questions of Lec-19

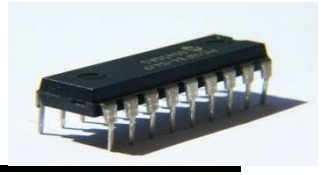


Q1. List various sources of leakage currents.

Ans: Various sources of leakage currents are listed below:

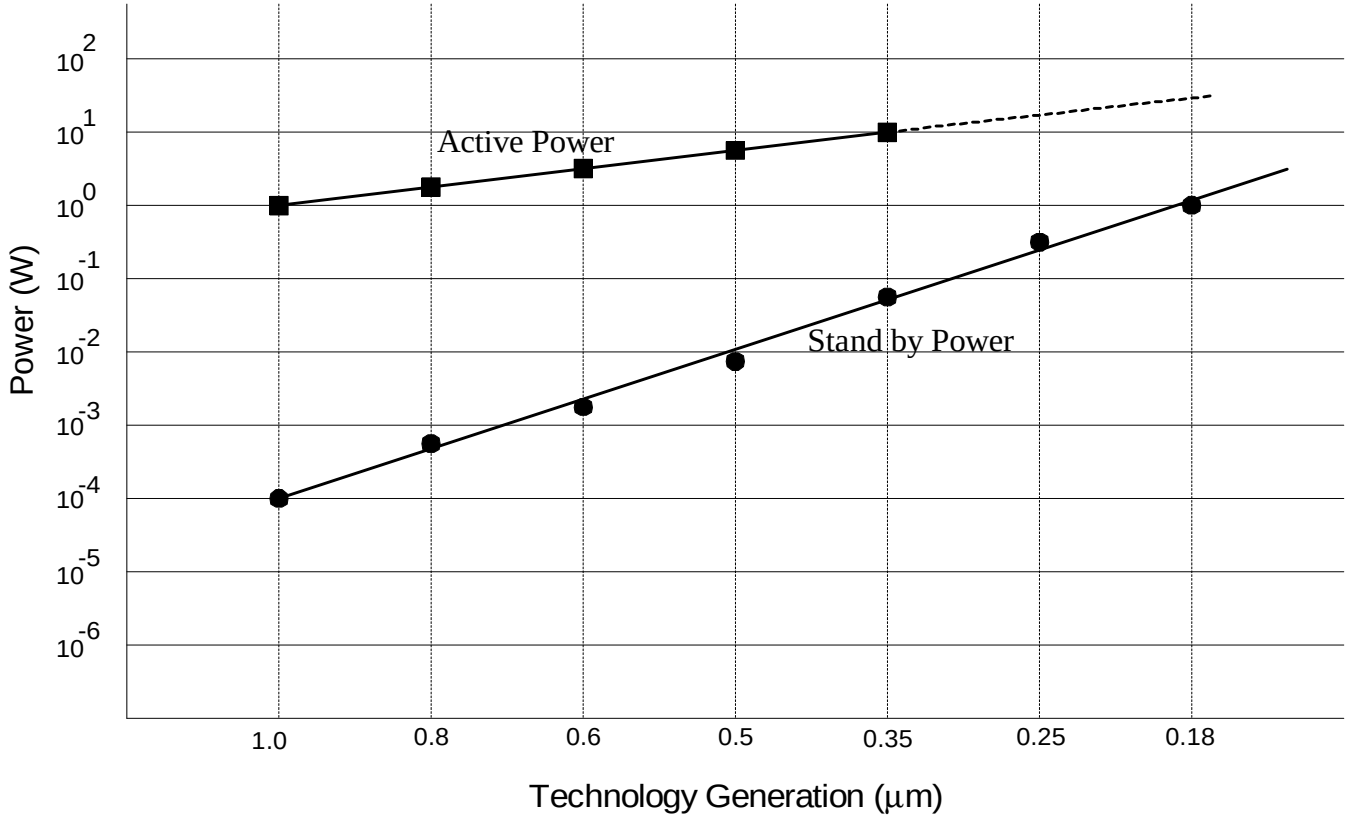
- **I_1= Reverse-bias p-n junction diode leakage current**
- **I_2 = Band-to-band tunneling current**
- **I_3 = Subthreshold leakage current**
- **I_4 = Gate Oxide tunneling current**
- **I_5 = Gate current due to hot-carrier injection**
- **I_6 = Channel punch-through**
- **I_7 = Gate induced drain-leakage current**

Answer to Questions of Lec-19

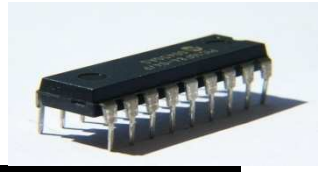


Q2. Why leakage power is an important issue in deep submicron technology?

Ans: In deep submicron technology, the leakage component is a significant % of total power as shown in the diagram. Moreover, the leakage current is increasing at a faster rate than dynamic power. As a consequence, it has become an important issue in DSM.



Answer to Questions of Lec-19



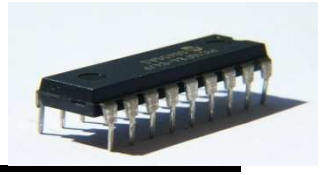
Q3. What is band-to-band tunneling current?

Ans: When both n regions and p regions are heavily doped, a high electric field across a reverse biased p-n junction causes significant current to flow through the junction due to tunneling of electrons from the valence bond of the p-region to the conduction band of n-region. This is known as band-to-band tunneling.

Q4. What is body effect?

Ans: As a negative voltage is applied to the substrate with respect to the source, the well-to-source junction the device is reverse biased and bulk depletion region is widened. This leads to increase the threshold voltage. This effect is known as body effect.

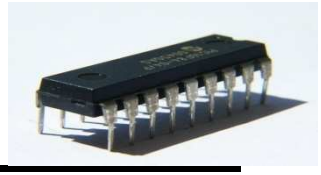
Answer to Questions of Lec-19



Q5. What is subthreshold leakage current? Briefly discuss various mechanisms responsible for this leakage current?

Ans: The subthreshold leakage current in CMOS circuits is due to carrier diffusion between the source and the drain regions of the transistor in weak inversion, when the gate voltage is below V_t. The behavior of an MOS transistor in the subthreshold operating region is similar to a bipolar device, and the subthreshold current exhibits an exponential dependence on the gate voltage. The amount of the subthreshold current may become significant when the gate-to-source voltage is smaller than, but very close to the threshold voltage of the device.

Answer to Questions of Lec-20



Q1. Explain the basic concepts of supply voltage scaling.

Q2. As you move to a new process technology with a scaling factor S = 1.4, how the drain current, power density, delay and energy requirement changes for the constant field scaling?

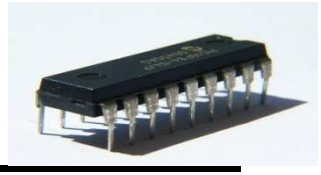
Q3. Distinguish between constant field and constant voltage feature size scaling? Compare their advantages and disadvantages.

Q4. Compare the constant field and constant voltage scaling approaches in terms of area, delay, energy and power density parameters.

Q5. Explain how *parallelism* can be used to achieve low power instead of high performance in realizing digital circuits.

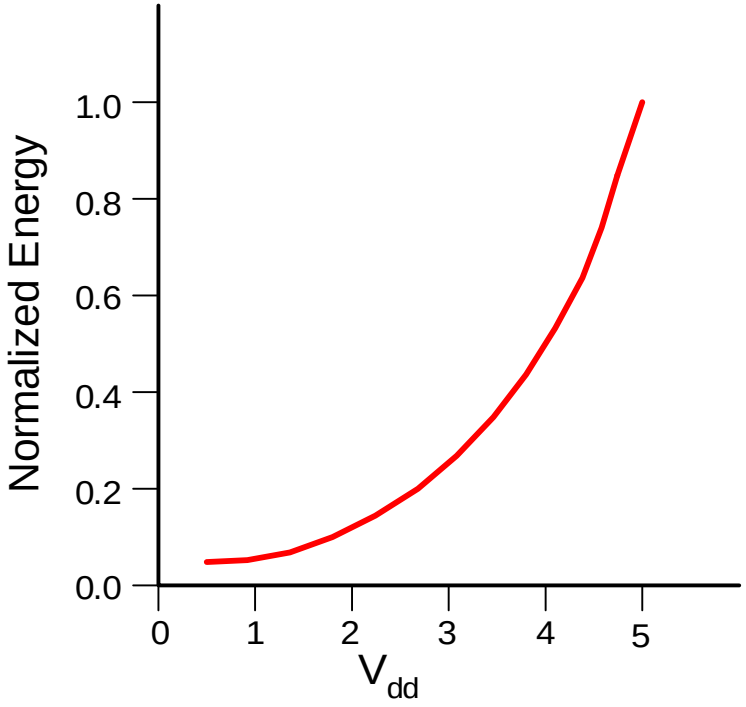
Q6.Explain how multicore architecture provides low power compared to the single core architecture of the same performance.

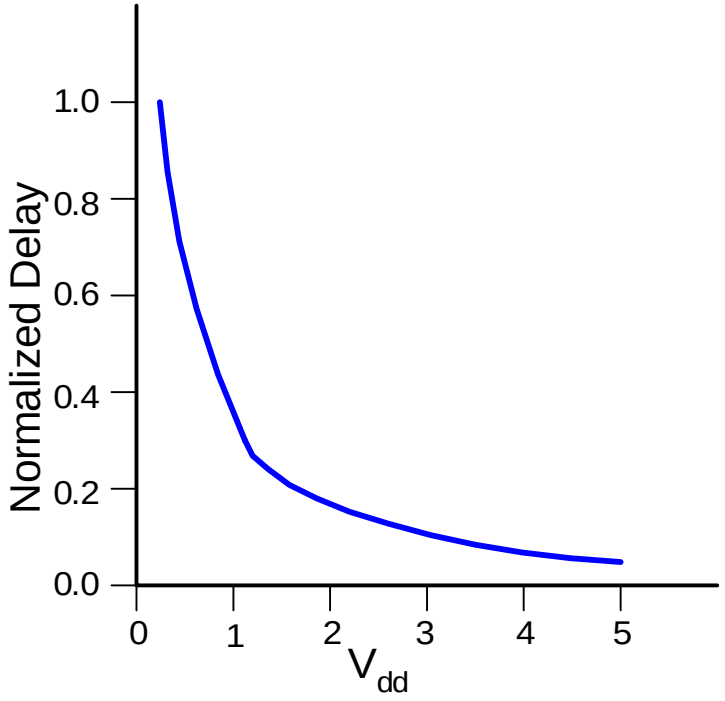
Answer to Questions of Lec-20



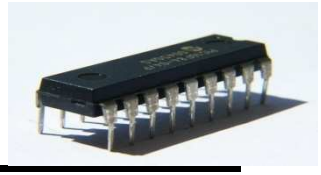
Q1. Explain the basic concepts of supply voltage scaling.

Ans: Power dissipation is proportional the square of the supply voltage. So, a factor of two reduction in supply voltage yields a factor of four decrease in energy. But, as the supply voltage is reduced, delay increases as shown in the diagram. So, the challenge is to scale down the supply voltage without compromise in performance.





Answer to Questions of Lec-20

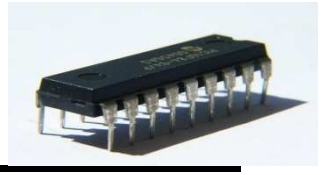


Q2. As you move to a new process technology with a scaling factor S = 1.4, how the drain current, power dissipation, power density, delay and energy requirement changes for the constant field scaling?

Ans: Drain current reduces by a factor of S. Although power dissipation decreases by a factor of S^2 , the power density remains the same. The delay decreases by a factor of S and the energy decreases by a factor of S^3 .

Quality	Before Scaling	After Scaling
Gate Capacitance	C_g	$C_g' = C_g / S$
Drain Current	I_D	$I_D' = I_D / S$
Power Dissipation	P	$P' = P / S^2$
Power Density	P/ Area	$P' / Area' = (P / Area)$
Delay	t_d	$t_d' = t_d / S$
Energy	$E = P.t_d$	$E' = \frac{P}{S^2} \times \frac{t_d}{S} = \frac{P.t_d}{S^3} = \frac{1}{S^3} E$

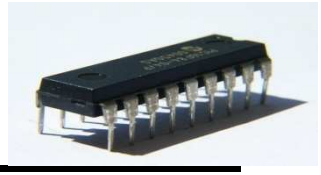
Answer to Questions of Lec-20



Q3. Distinguish between constant field and constant voltage feature size scaling? Compare their advantages and disadvantages.

Ans: In this approach the magnitude of all the internal electric fields within the device are preserved, while the dimensions are scaled down by a factor of S. This requires that all potentials must be scaled down by the same factor. Accordingly, supply as well as threshold voltages are scaled down proportionately. But, in constant-voltage scaling, all the device dimensions are scaled down by a factor of S just like constant-voltage scaling, supply voltage and threshold voltages are not scaled.

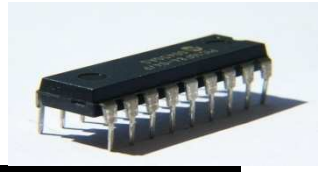
Answer to Questions of Lec-20



Q4. Compare the constant field and constant voltage scaling approaches in terms of area, delay, energy and power density parameters.

Quality	Cons field Scaling	Constant Voltage Scaling
Gate Capacitance	$C_g' = C_g / S$	$C_g' = C_g / S$
Drain Current	$I_D' = I_D / S$	$I_D' = I_D.S$
Power Dissipation	$P' = P / S^2$	$P' = P.S$
Power Density	$P' / Area' = (P / Area)$	$P' / Area' = S^3 P / Area$
Delay	$t_d^{'} = t_d / S$	$t_d^{'} = t_d / S^2$
Energy	$E' = \frac{P}{S^2} \times \frac{t_d}{S} = \frac{P.t_d}{S^3} = \frac{1}{S^3} E$	$E' = E / S$

Answer to Questions of Lec-20



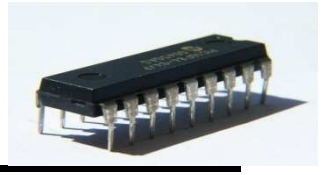
Q5. Explain how *parallelism* can be used to achieve low power instead of high performance in realizing digital circuits.

Ans: Traditionally, parallelism is used to improve performance at the expense of larger power dissipation. But, instead of trying to improve performance, the power dissipation can be reduced by scaling down the supply voltage such that the performance remains unaltered.

Q6.Explain how multicore architecture provides low power compared to the single core architecture of the same performance.

Ans: The idea behind the parallelism for low-power can be extended to multi-core architecture. The clock frequency can be reduced with commensurate scaling of the supply voltage as the number of cores is increased from one to more than one while maintaining the same throughput.

Review Questions of Lec-21



Q1. In what situation pipelining can be implemented?

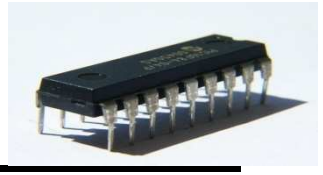
Q2. Explain how pipelining can be used to achieve low power instead of high performance in realizing digital circuits.

Q3. How clock frequency, speed up, throughput and power dissipation changes for a pipelined implementation with k stages with respect to non-pipelined implementation?

Q4. How can you combine sizing and supply voltage scaling to realize low power circuits?

Q5. Explain with an example how pipelining and parallelism can be combined to realize low power circuits?

Answer to Questions of Lec-21



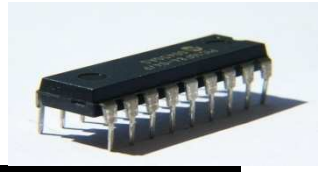
Q1. In what situation pipelining can be implemented?

Ans: A task can be pipelined when it can be divided into more than one independent subtasks, which can be executed in a overlapped manner.

Q2. Explain how pipelining can be used to achieve low power instead of high performance in realizing digital circuits.

Ans: In a conventional pipelined implementation, the subtasks are executed in a overlapped manner at a faster rate. Instead of that, the subtasks can be executed at the same rate as the original task but with reduced supply voltage. This is how the pipelined the implementation will require lower power.

Answer to Questions of Lec-21



Q3. How clock frequency, speed up, throughput and power dissipation changes for a pipelined implementation with k stages with respect to non-pipelined implementation?

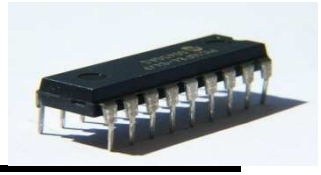
Ans: Clock frequency = kf, speedup = $S_k = \frac{n.k}{k+(n-1)}$

where n is the number of tasks executed using k-stage pipeline, and power dissipation = $1/k^2$.

Q4. How can you combine sizing and supply voltage scaling to realize low power circuits?

Ans: It can be done in three steps (a) Upsize gates on the critical path to reduce delay of the circuit (b) Scale down the supply voltage to equalize with the original delay (c) Upsize gates on non-critical paths selectively without exceeding the critical path delay.

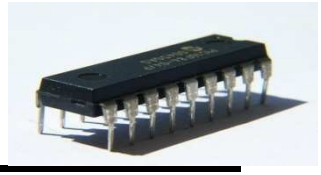
Answer to Questions of Lec-21



Q5. Explain with an example how pipelining and parallelism can be combined to realize low power circuits?

Ans: Here, more than one parallel structure is used and each structure is pipelined. Both power supply and frequency of operation are reduced to achieve substantial overall reduction in power dissipation.

Review Questions of Lec-22



Q1. Explain the basic concept of multi level voltage scaling.

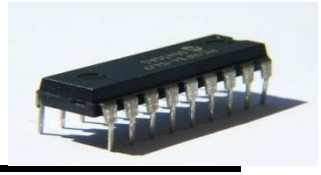
Q2. What is the impact of multiple supply voltages on the distribution of path delays of a circuit with respect to that for single supply voltage?

Q3. List and explain three important issues in the context of multiple supply voltage scaling?

Q4. What problem arises when a signal passes from low voltage domain to high voltage domain? How this problem is overcome?

Q5. Explain the design decision for the placement of converters in the voltage scaling interfaces.

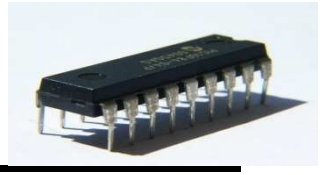
Answer to Questions of Lec-22



Q1. Explain the basic concept of multi level voltage scaling.

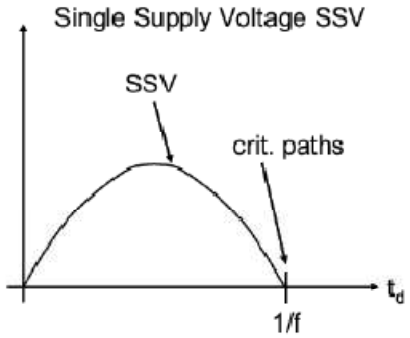
Ans: This is an extension of SVS where two or few fixed voltage domains are used in different parts of a circuit,. As we know, high Vdd gates have less delay, but higher dynamic and static power dissipation and low Vdd gates have larger delay but lesser power dissipation. Voltage islands can be generated at different levels of granularity, such as macro level and standard cell level. The slack of the off-critical path can be utilized for allocation of macro modules of low-Vdd to off-critical-path macro modules. Total power dissipation can be reduced without degrading the overall circuit performance.

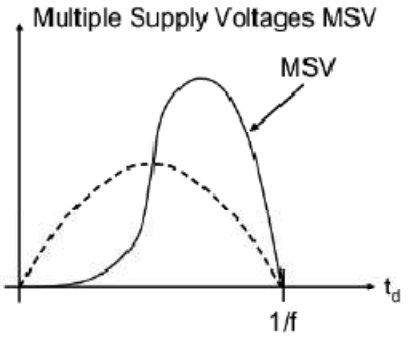
Answer to Questions of Lec-22



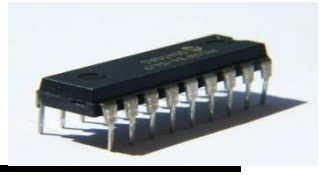
Q2. What is the impact of multiple supply voltages on the distribution of path delays of a circuit with respect to that for single supply voltage?

Ans: Path delay for different paths in a circuit for single supply voltage is shown. The graph of a Gaussian is a characteristic symmetric "bell curve" shape that quickly falls off towards plus/minus infinity plus/minus infinity. However, when multiple supply voltages are used, the path delay distribution is not Gaussian because modules having smaller delays are assigned with smaller supply voltage and their delay increases.





Answer to Questions of Lec-22

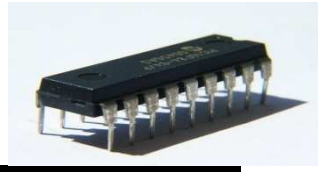


Q3. List and explain the important issues in the context of multiple supply voltage scaling?

Ans: Important issues in the context of MVS are listed below:

(a) Voltage Scaling Interfaces
(b) Converter Placement
(c) Floor planning, Routing and Placement
(d) Multiple Supply Voltages
(e) Static Timing Analysis
(f) Power up and Power down Sequencing
(g) Clock distribution

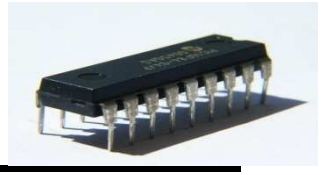
Answer to Questions of Lec-22



Q4. What problem arises when a signal passes from low voltage domain to high voltage domain? How this problem is overcome?

Ans: A high-level output from the low-Vdd domain has output VddL, which may turn on both nMOS and pMOS transistors of the high-Vdd domain inverter resulting in short circuit between VddH to GND. A level converter needs to be inserted to avoid this static power consumption

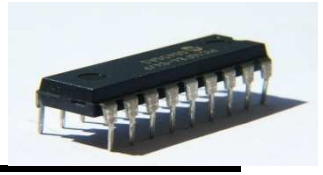
Answer to Questions of Lec-22



Q5. Explain the design decision for the placement of converters in the voltage scaling interfaces.

Ans: One important design decision in the voltage scaling interfaces is the placement of converters . As the high-to-low level converters use low-Vdd voltage rail, it is a appropriate to place them in the receiving or destination domain. It is also recommended to place the low-to-high level converters in the receiving domain. As the low-to-high level converters require both low and high-Vdd supply rails, at least one of the supply rails needs to be routed from one domain to the other.

Review Questions of Lec-23



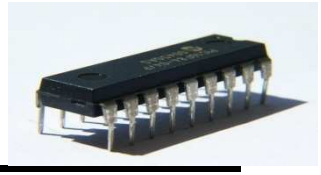
Q1. For a workload of 50%, explain how reduction in power dissipation takes place for DVS and DVFS?

Q2. With the help of a schematic diagram, explain how the dynamic voltage and frequency scaling technique is used to achieve low power dissipation of a processor.

Q3. In what way adaptive voltage scaling differs from dynamic voltage scaling?

Q4. Show various building blocks required for the implementation of adaptive voltage scaling system.

Answer to Questions of Lec-23



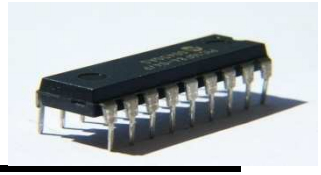
Q1. For a workload of 50%, explain how reduction in power dissipation takes place for DVS and DVFS?

Q2. With the help of a schematic diagram, explain how the dynamic voltage and frequency scaling technique is used to achieve low power dissipation of a processor.

Q3. In what way adaptive voltage scaling differs from dynamic voltage scaling?

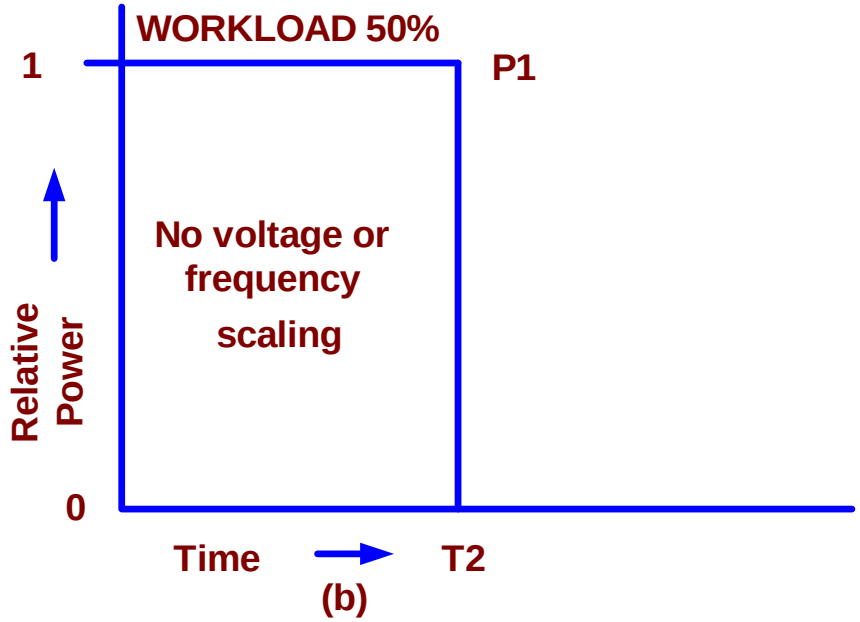
Q4. Show various building blocks required for the implementation of adaptive voltage scaling system.

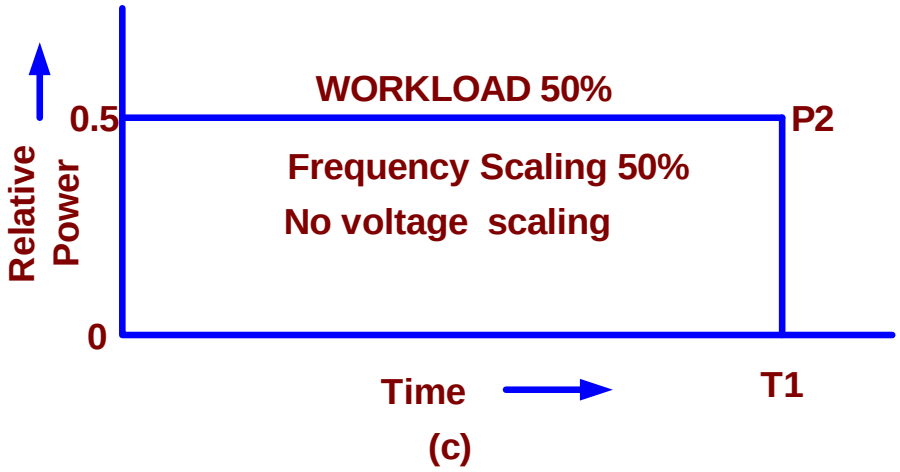
Answer to Questions of Lec-23

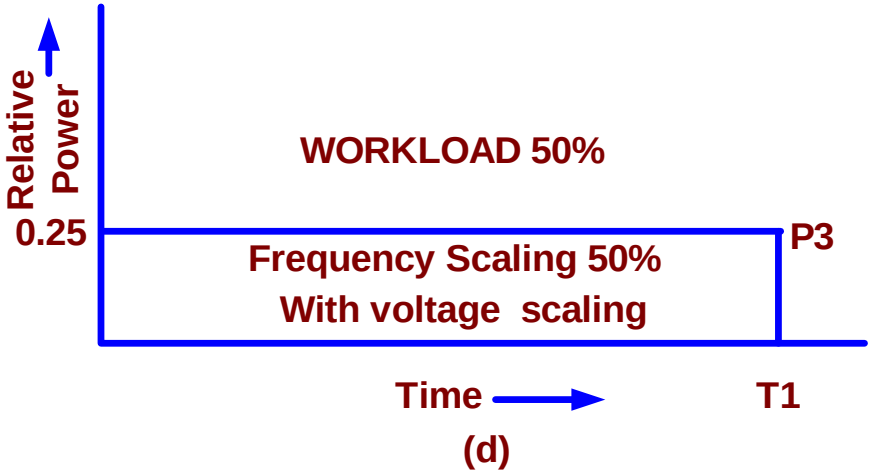


Q1. For a workload of 50%, explain how reduction in power dissipation takes place for DFS and DVFS?

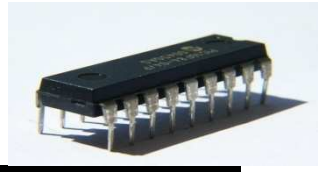
Ans: The adjacent diagrams show how reduction in power dissipation take in the two situations.





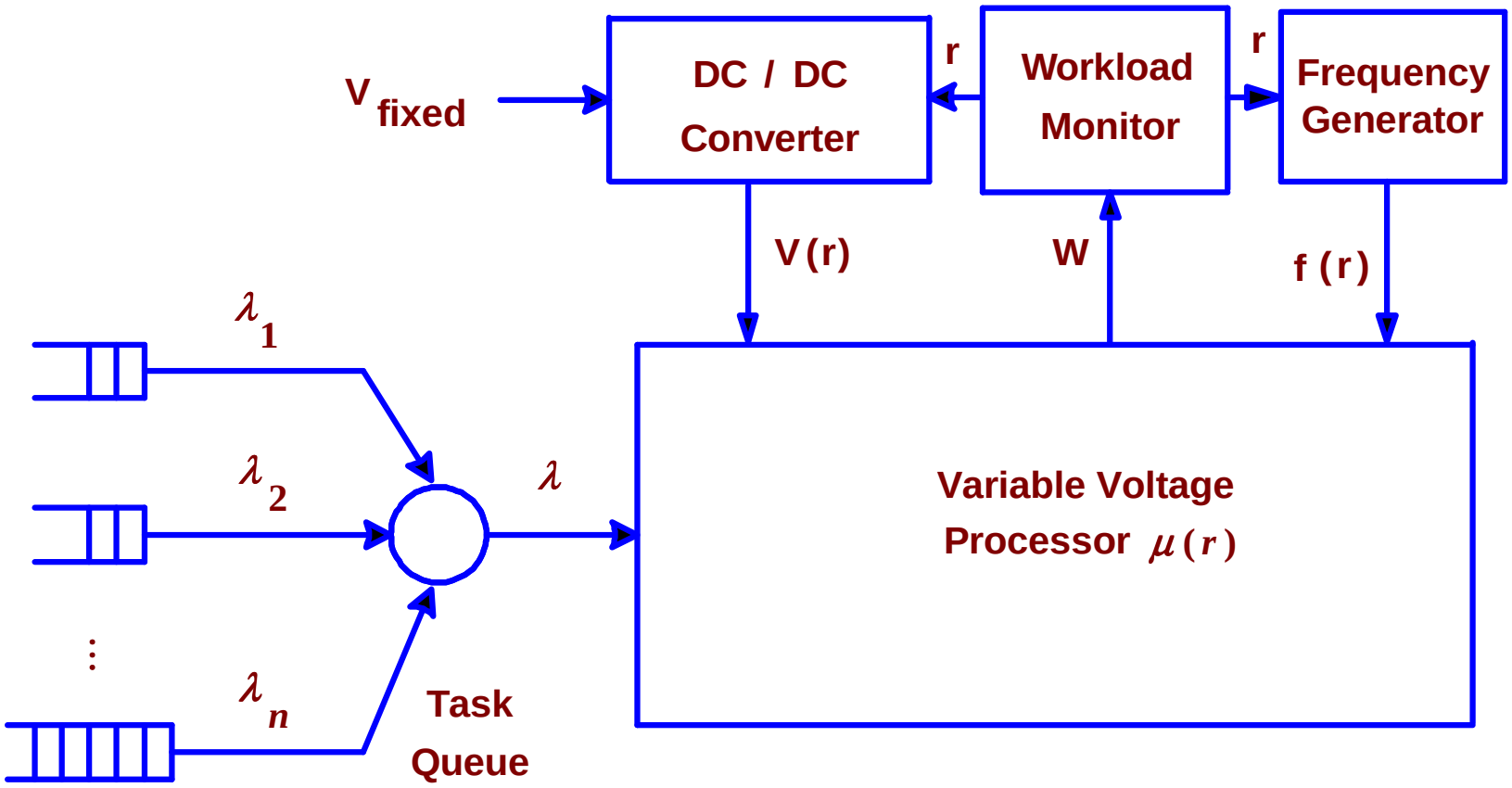


Answer to Questions of Lec-23

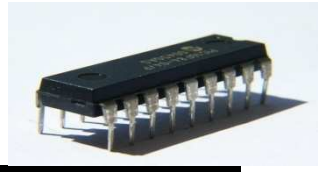


Q2. With the help of a schematic diagram, explain how the dynamic voltage and frequency scaling technique is used to achieve low power dissipation of a processor.

Ans: The diagram shows how both voltage and frequency are controlled for different predicted workload.



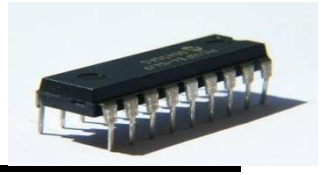
Answer to Questions of Lec-23



Q3. In what way adaptive voltage scaling differs from dynamic voltage scaling?

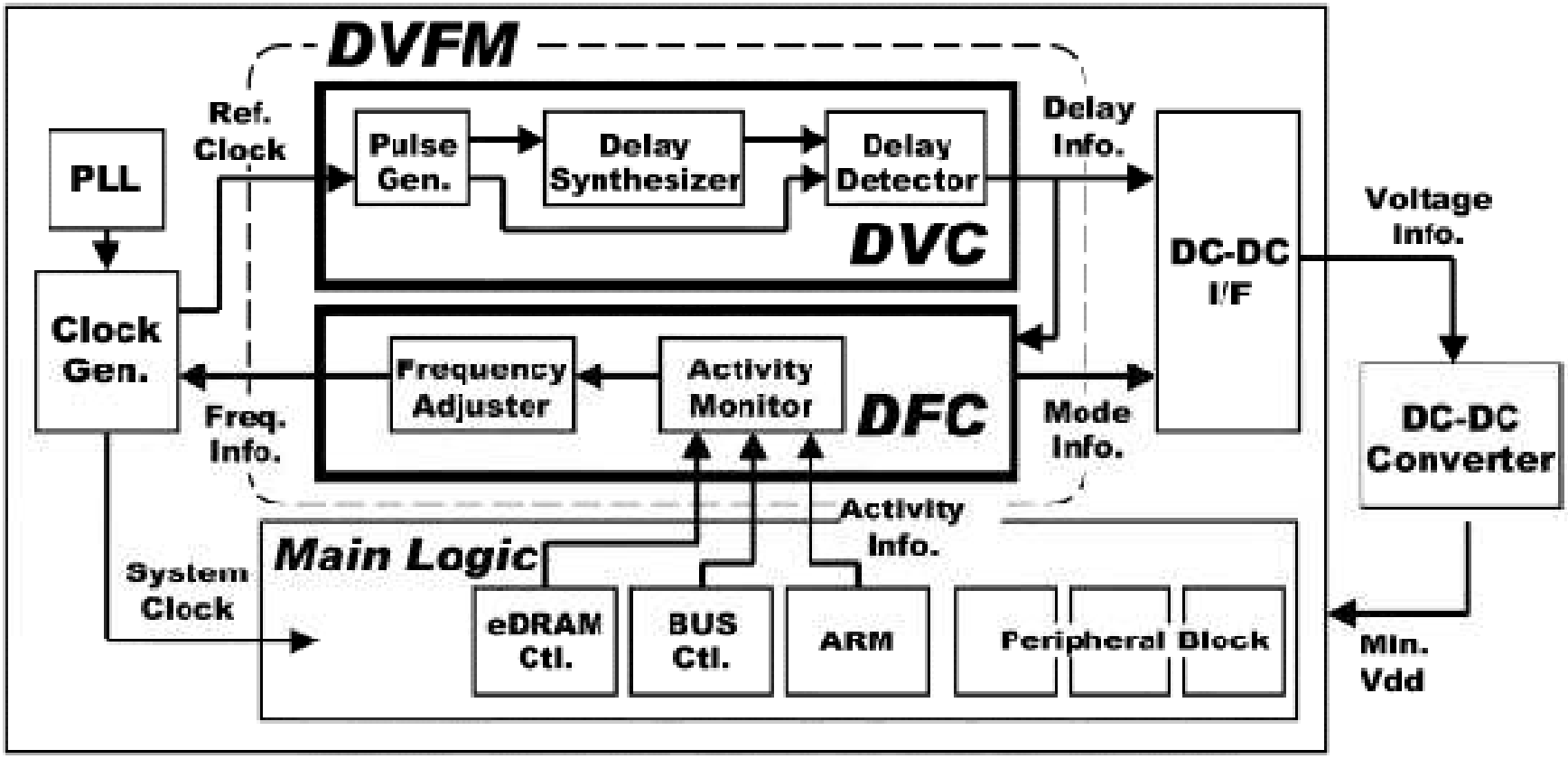
Ans: The DVFS approach is open-loop in nature. Voltage-frequency pairs are determined at design time keeping sufficient margin for guaranteed operation across the entire range of best and worst case process, voltage and temperature (PVT) conditions. As the design needs to be very conservative for successful operation, the actual benefit obtained is lesser than actually possible. A better alternative that can overcome this limitation is the Adaptive Voltage Scaling (AVS) where a close-loop feedback system is implemented between the voltage scaling power supply and delay sensing performance monitor at execution time.

Answer to Questions of Lec-23

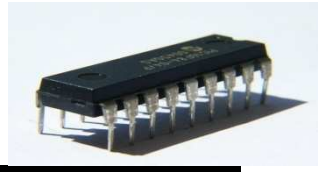


Q4. Show various building blocks required for the implementation of adaptive voltage scaling system.

Ans: The schematic diagram is given below. The operation of different building blocks are as follows:

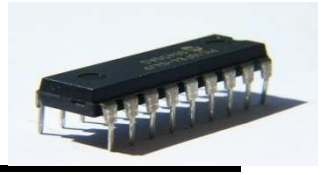


Answer to Questions of Lec-23



The on-chip monitor not only checks the actual voltage developed, but also detects whether the silicon is slow, typical or fast and the effect of temperature on the surrounding silicon. The DVC emulates the critical path characteristic of the system by using a delay synthesizer and controls the dynamic supply voltage (0.9 to 1.6V at 5mV step in real time). The DFC adjusts the clock frequency at the required minimum value by monitoring the system activity (20MHz to 120MHz). The voltage and frequency are predicted according to the performance monitoring of the system. The DVFM system can track the required performance with a high level of accuracy over the full range of temperature and process deviations.

Review Questions of Lec-24



Q1. Explain the basic concept of hardware-software tradeoff with an example for low power .

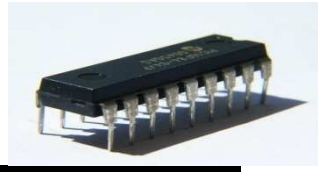
Q2. Distinguish between superscalar and VLIW architecture

Q3. Discuss why VLIW architecture allows lower power dissipation compared to Superscalar architecture.

Q4. In the context of Transmeta's Crusoe processor explain the role of Code Morphing Software.

Q5. How caching can be used to achieve lower power dissipation in VLIW architecture?

Answer to Questions of Lec-24



Q1. Explain the basic concept of hardware-software tradeoff with an example for low power .

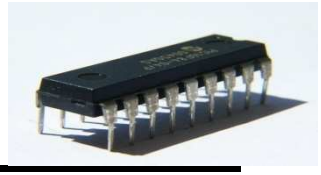
Ans: It is well known that the same functionality can be either realized by hardware or by software or by a combination of both. The hardware-based approach has the following characteristic:

- **Faster**
- **Costlier**
- **Consumes more power**

On the other hand the software-based approachhas the following characteristics:

- **Cheaper**
- **Slower**
- **Consumes lesser power**

Answer to Questions of Lec-24

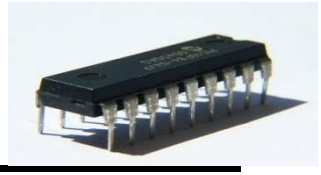


Q2. Distinguish between superscalar and VLIW architecture.

Ans: Both superscalar and VLIW architectures implement a form of parallelism called instruction-level parallelism within a single processor. A superscalar processor executes more than one instructions during a clock cycle by simultaneously dispatching multiple instructions to more than one functional units on the processor. In a superscalar CPU the dispatcher reads instructions from memory and decides which ones can be run in parallel, dispatching them to two or more functional units contained inside a single CPU. So, in this case ILP is implemented by hardware.

On the other hand, a compiler identifies that can be executed in parallel and generates long instructions having multiple operations meant for different functional units. Therefore, in this case ILP is implemented by software.

Answer to Questions of Lec-24



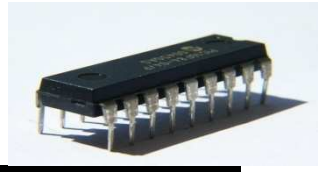
Q3. Discuss why VLIW architecture allows lower power dissipation compared to Superscalar architecture.

Ans: As parallelism is identified by software at compile time, the VLIW incurs lower power dissipation.

Q4. In the context of Transmeta's Crusoe processor explain the role of Code Morphing Software.

Ans: The Code Morphing software mediates between x86 software and the VLIW engine. It is fundamentally a dynamic translation system. A program that translates instructions from one instruction set architecture to another instruction set architecture. Here, x86 code is compiled into VLIW code of the Cruosoe processor. Code Morphing software insulates x86 programs from the hardware engine's native instruction set. The code morphing software is the only program that is written directly for the VLIW processor.

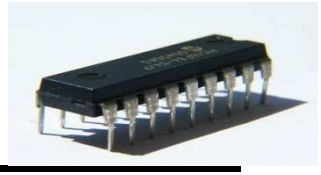
Answer to Questions of Lec-24



Q5. How caching can be used to achieve lower power dissipation in VLIW architecture?

Ans: In real-life applications it is very common to execute a block of code many times over and over after it has been translated once. A separate memory space is used to store the translation cache and the code morphing software. It allows reuse the translated code by making use of locality of reference property. Caching translations provide excellent opportunity of reuse in many real-life applications.

Review Questions of Lec-25



Q1. Explain the basic concept of bus encoding to reduce switched capacitance.

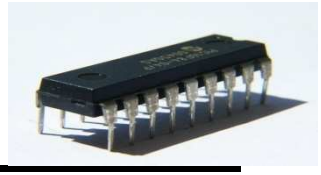
Q2. Find out the switching activity of a modulo-7 counter using binary and Gray codes for state encoding

Q3. How gray coding helps to reduce power dissipation for fetching instructions from main memory?

Q4. How reduction in power dissipation is achieved by dividing a 64-bit bus into eight 8-bit buses.

Q5. How T0 encoding achieves almost zero transition on a bus.

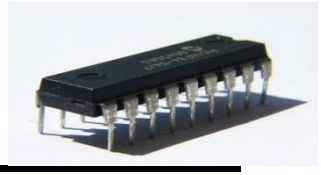
Answer to Questions of Lec-25



Q1. Explain the basic concept of bus encoding to reduce switched capacitance.

Ans: Switching activity can be reduced by coding the address bit before sending over the bus. This is done introducing sample to sample correlation such that total number of bit transitions is reduced. Similarly, communicating data bits in an appropriately coded form can reduce the switching activity.

Answer to Questions of Lec-25

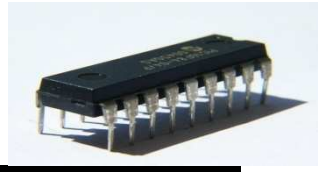


Q2. Find out the switching activity of a modulo-7 counter using binary and Gray codes for state encoding.

Ans: The reduction in the number of bit transitions for the two types of coding is given below:

Binary code	Transitions	Gray code	Transitions
000		000	
001	1	001	1
010	2	011	1
011	1	010	1
100	3	110	1
101	1	111	1
110	2	101	1
	2		2
Total	12		8

Answer to Questions of Lec-25

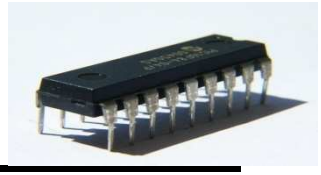


Q3. How gray coding helps to reduce power dissipation for fetching instructions from main memory?

Ans: A gray code sequence is a set of numbers in which adjacent numbers have only one bit difference. On the other hand, the number of transitions vary from 1 to n (n/2 on the average) as shown in the adjacent table. The power dissipations of the bus driver decreases because of the reduction of switching activity.

Decimal Value	Binary Code	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

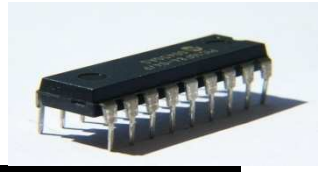
Answer to Questions of Lec-25



Q4. How T0 encoding achieves almost zero transition on a bus.

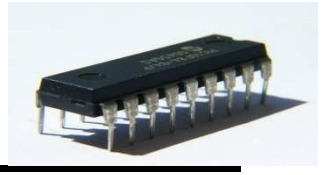
Ans: In T0 encoding, after sending the first address, the same address is sent for infinite streams of consecutive addresses. The receiver side is informed about it by sending an additional bit known as increment (INC) bit. However, if the address is not consecutive, then the actual address is sent. The T0 code provides, zero transition property for infinite streams of consecutive addresses.

Review Questions of Lec-26



1. Explain the basic concept of clock gating to reduce power dissipation in a digital circuit.
2. What are the three levels of clock gating granularity? Compare their pros and cons.
3. Explain the important issues related to clock gating in the clock tree.
4. Explain with an example, how power dissipation in a combinational circuit can be reduced by using operand isolation.

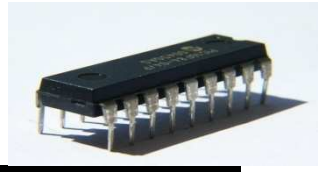
Answer to Questions of Lec-26



1. **Explain the basic concept of clock gating to reduce power dissipation in a digital circuit.**

Ans: It has been observed that a major component of processor power is the clock power (50% of the total power). So, there is scope for large reduction of power dissipation by using suitable technique to remove a large number of unnecessary transitions. Such transitions can be suppressed without affecting functionality. One of the most successful and commonly used low power technique is clock gating.

Answer to Questions of Lec-26

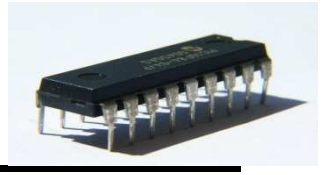


2. What are the three levels of clock gating granularity? Compare their pros and cons.

Ans: There are three levels of granularity:

- **Module-level clock gating: Large reduction in power but there is limited opportunity.**
- **Register-level clock gating: There is more opportunity compared to module level clock gating, but lesser reduction of power.**
- **Cell-level clock gating: Provides many more opportunities and it lends itself to automated insertion and can result in massively clock gated designs.**

Answer to Questions of Lec-26

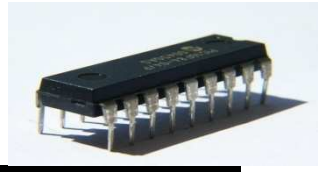


3. Explain the important issues related to clock gating in the clock tree.

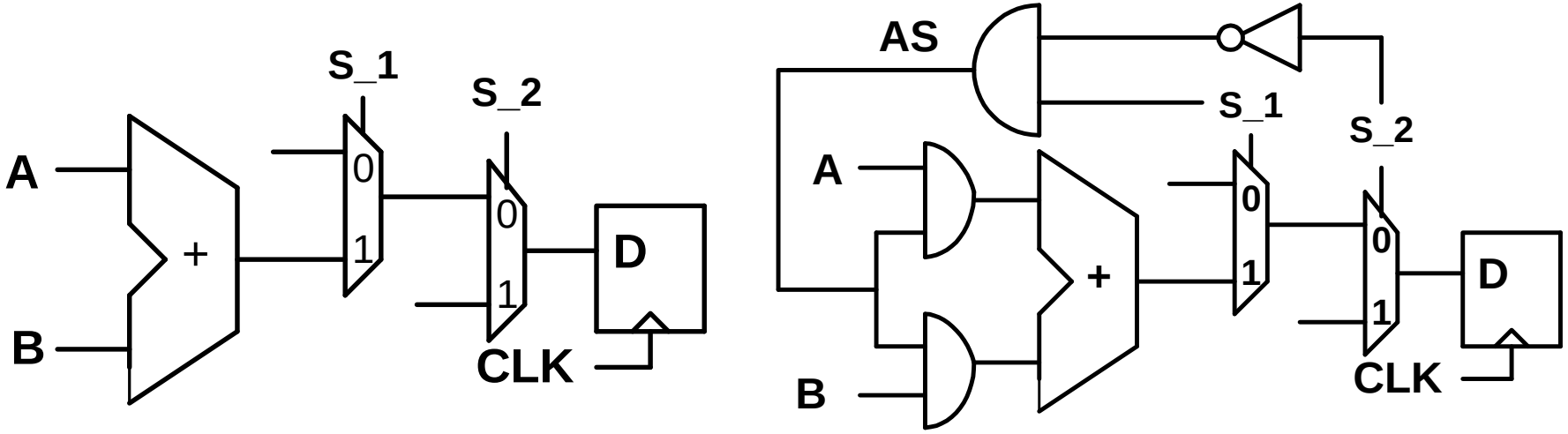
Ans: Clock tree amounts to a significant portion of the total dynamic power consumption. It leads to a tradeoff between the physical capacitance that is prevented from switching and the number of unnecessary transitions. Disabling at higher up in the tree prevents larger capacitance from switching, but the gating condition is satisfied fewer times. Having multiple gating points along a path may be beneficial.

4. Explain with an example, how power dissipation in a combinational circuit can be reduced by using operand isolation.

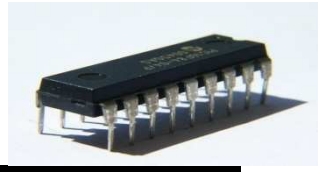
Answer to Questions of Lec-26



Ans: Operand isolation is a technique for power reduction in the combinational part of the circuit. Here the basic concept is to 'shut-off' logic blocks when they do not perform any useful computation. Shutting-off is done by not allowing the inputs to toggle in clock cycles when the output of the block is not used. In the following example, the output of the adder is loaded into the latch only when S_1 is 1 and S_2 is 0. So, input lines of the adder may be gated based on this condition, as shown in the diagram.



Review Questions of Lec-27



Q1. What is the basic concept of clock gated FSM.

Q2. How state encoding can be used to reduce power dissipation in an FSM? Explain with an example.

Q3. How power dissipation is reduced by partitioning an FSM> Explain with an example.

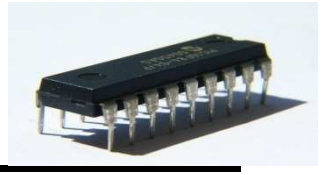
Q4. A sequence detector produces a '1' for each occurrence of the input sequence '1001' at its input.

(a) Draw the state-transition diagram of the FSM realizing the sequence detector.

(b) Obtain state table from the state transition diagram.

(c) Realize the FSM using D FFs and a PLA.

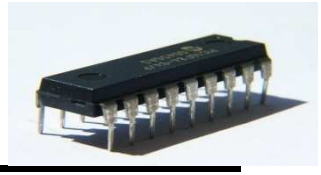
Answer to Questions of Lec-27



Q1. What is the basic concept of clock gated FSM.

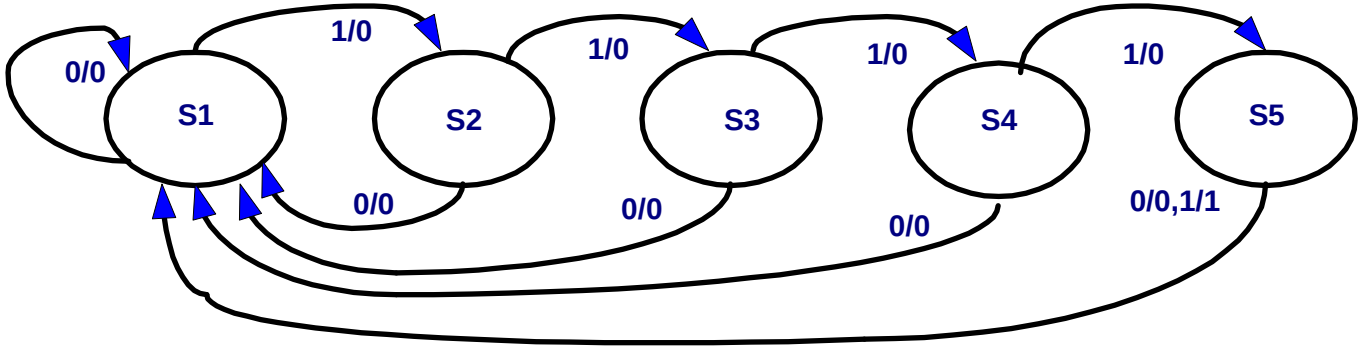
Ans: There are conditions when the next state and output values do not change (idle condition). Clocking the circuit during this idle condition leads to unnecessary wastage of power. The clock can be stopped, if the idle conditions can be detected. This saves power both in the combinational circuit as well as the registers/latches.

Answer to Questions of Lec-27

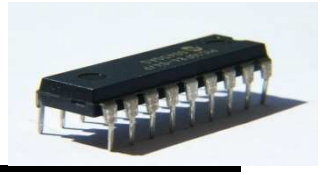


Q2. How state encoding can be used to reduce power dissipation in an FSM? Explain with an example.

Ans: In the state assignment phase of an FSM, each state is given a unique code. It has been observed that states assignment strongly influences the complexity of its combinational logic part used to realize the FSM. Traditionally state assignment has been used to optimize the area and delay of the circuit. It can also be used to reduce switching activity for the reduction of the dynamic power. This is illustrated with the help of the following example:

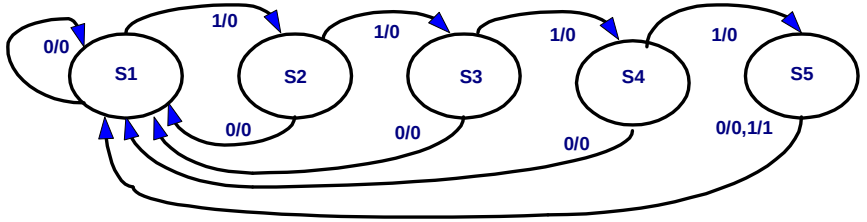


Answer to Questions of Lec-27



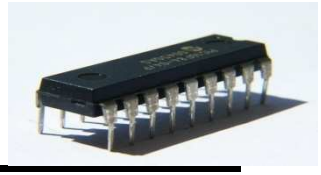
State	Encoding
S1	000
S2	111
S3	001
S4	110
S5	101

State	Encoding
S1	000
S2	001
S3	011
S4	010
S5	100



Transitions	Assignment-1	Assignment-2
S1→S1	0.0	0.0
S1→S2	1.5	0.5
S2→S1	1.5	0.5
S2→S3	1.0	0.5
S3→S1	0.5	1.0
S3→S4	1.5	0.5
S4→S1	1.0	0.5
S4→S5	1.0	1.0
S5→S1	2.0	1.0
Total	10.0	5.5

Answer to Questions of Lec-27



Q3. How power dissipation is reduced by partitioning an FSM. Explain with an example.

Ans: The idea is to decompose a large FSM into a several smaller FSMs with smaller number of state registers and combinational blocks. Out of all the FSMs, only the active FSMs receive clock and switching inputs, and the others are idle and consume no dynamic power. This is the basic concept of reducing dynamic power by partitioning an FSM.

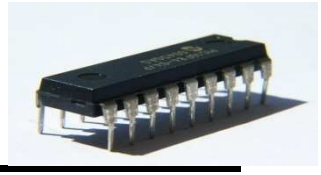
Q4. A sequence detector produces a '1' for each occurrence of the input sequence '1001' at its input.

(a) Draw the state-transition diagram of the FSM realizing the sequence detector.

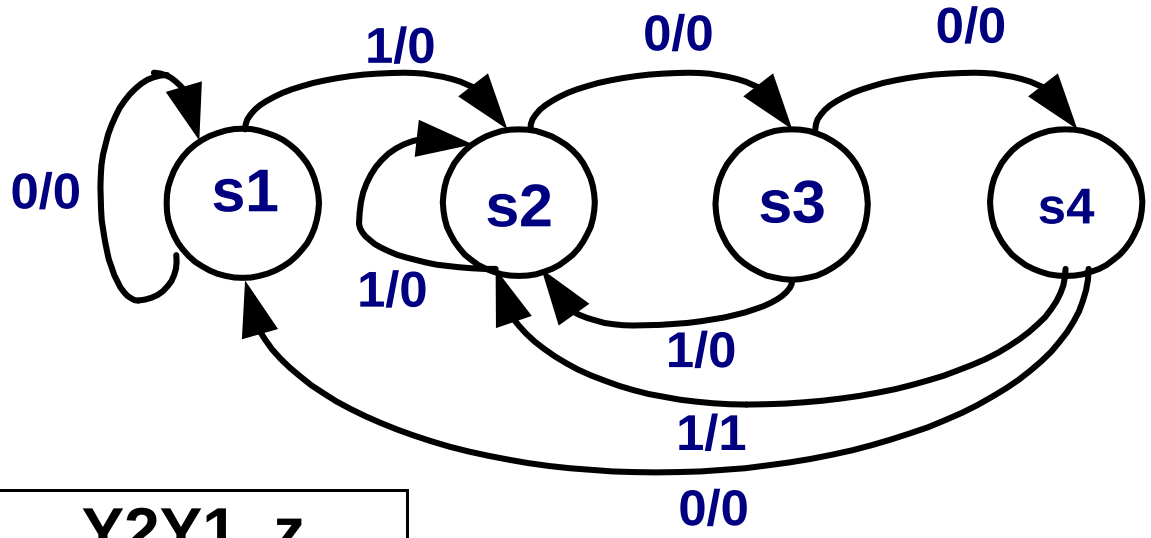
(b) Obtain state table from the state transition diagram.

(c) Realize the FSM using D FFs and a PLA.

Answer to Questions of Lec-27



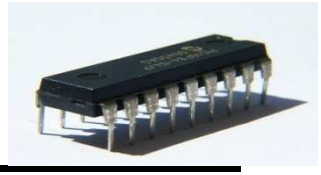
Ans: 4(a) The state transition diagram is given below:



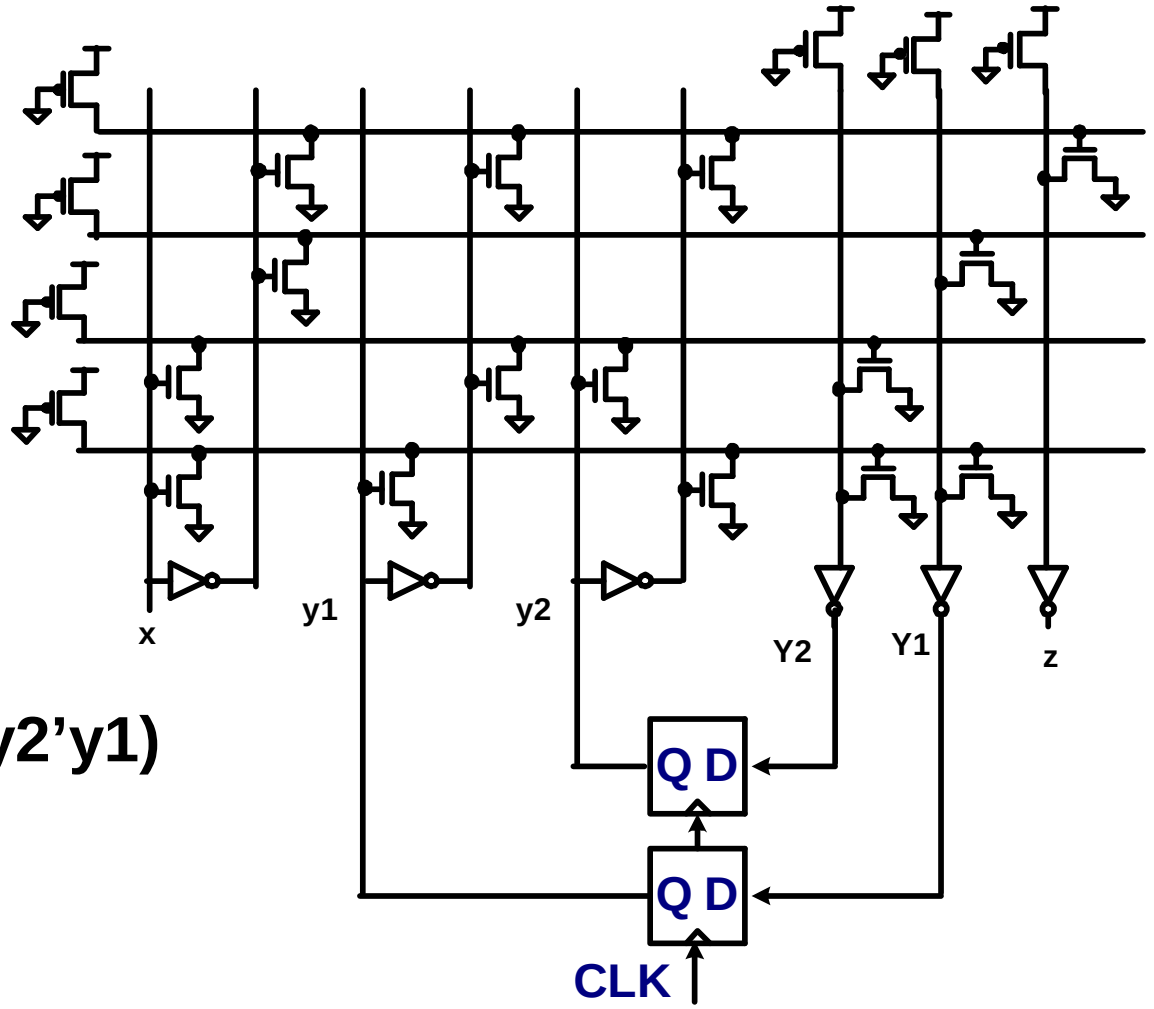
		Y2Y1, z	
PS	y2y1	x =0	X = 1
S1	0 0	00,0	01,0
S2	01	10,0	01,0
S3	1 0	11,0	01,0
S4	1 1	00,0	01,1

Ans: 4(b) The state table is given in the adjacent diagram

Answer to Questions of Lec-27



Ans: 4(c) The FSM using D FFs and a PLA to realize the combinational circuit is given below:.

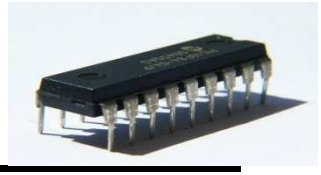


$Y2 = x'(y2y1' + y2'y1)$

$Y1 = x + x'y2y1'$

$z = xy2y1$

Review Questions of Lec-28



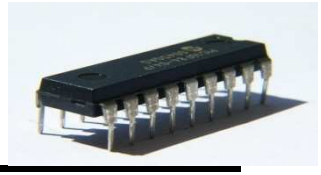
Q1. In what situation the use of sign-magnitude form of number representation instead of 2's complement form is beneficial in terms of power dissipation? Illustrate with an example.

Q2. Explain how the ordering of input signal does affect the dynamic power dissipation on a bus? Illustrate with an example.

Q3. What is glitching power dissipation? How can it be minimized?

Q4. How is it possible to reduce power dissipation by duplicating a resource rather than using it twice?

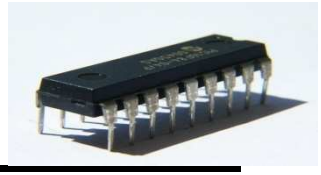
Answer to Questions of Lec-28



Q1. In what situation the use of sign-magnitude form of number representation instead of 2's complement form is beneficial in terms of power dissipation?

Ans: In most of the signal processing applications, 2's complement is typically chosen to represent numbers. Sign extension causes MSB sign-bits to switch when a signal transitions from +ve to –ve or vice versa. 2's complement can result in significant switching activity when the signals being processed switch frequently around zero. Switching in MSBs can be minimized by using sign-magnitude (S-M) representation.

Answer to Questions of Lec-28



Q2. Explain how the ordering of input signal does affect the dynamic power dissipation on a bus? Illustrate with an example.

Ans: Let us consider two alternative topologies to implement the required 2 additions

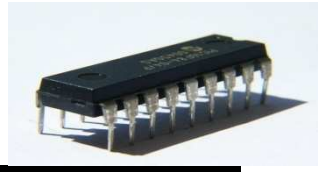
Topology #1

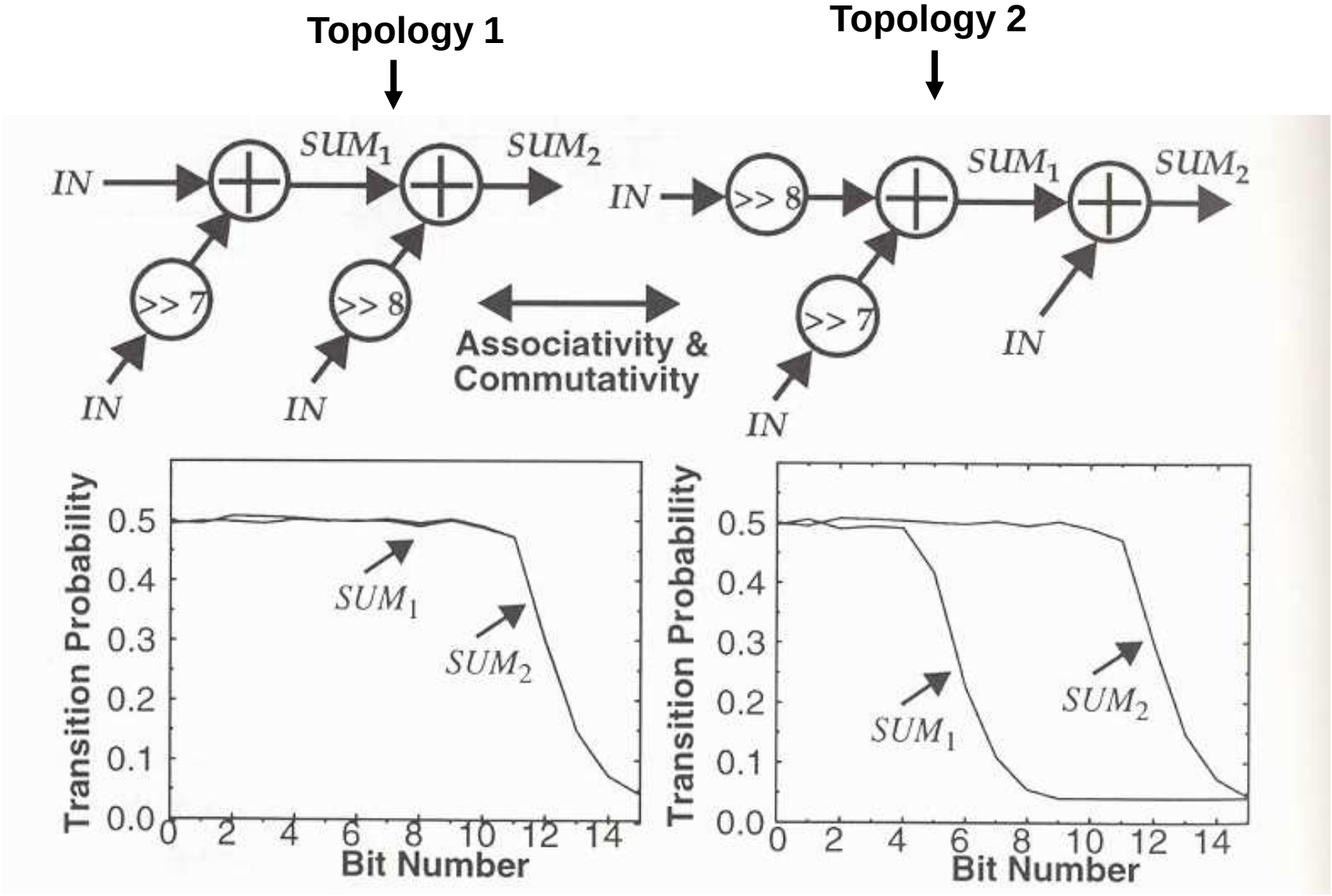
- **SUM1 = IN + (IN>>7)**
- **SUM2 = SUM1 + (IN>>8)**

Topology #2

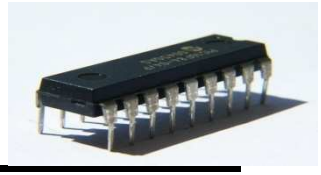
- **SUM1 = (IN>>7) + (IN>>8)**
- **SUM2 = SUM1 + IN**

Answer to Questions of Lec-28

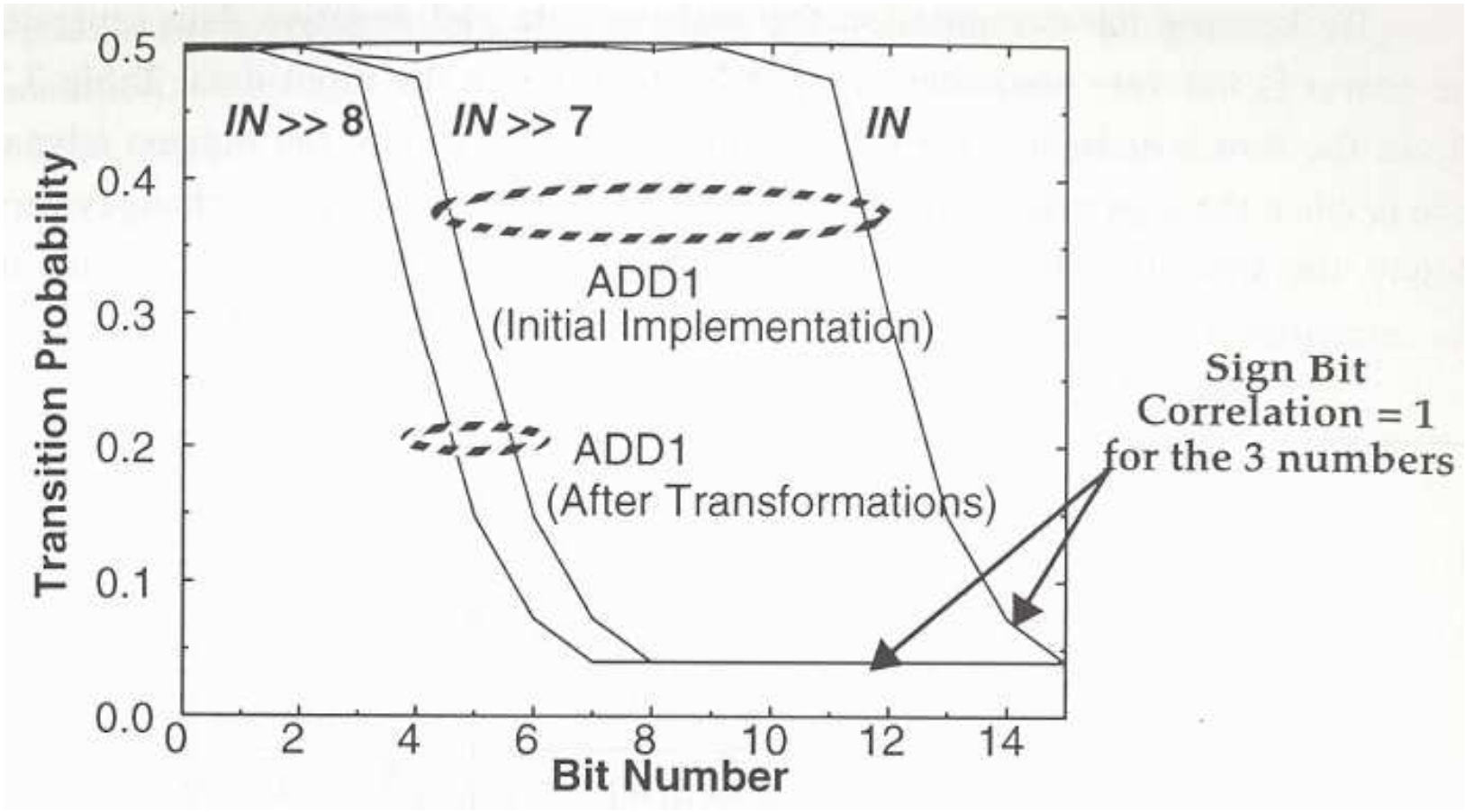




Answer to Questions of Lec-28

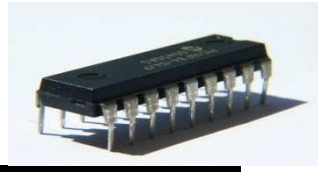


Shift operation represent a scaling operation, which has the effect of reducing the dynamic range of the signal



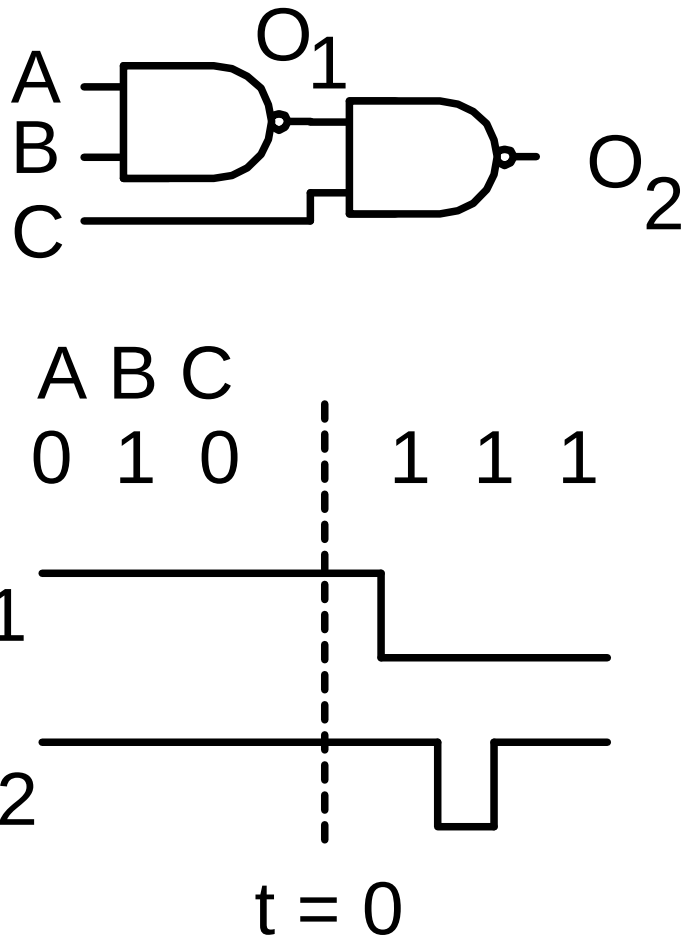
- **Transition Probability for 3 signals – IN, IN>>7, IN>>8**

Answer to Questions of Lec-28

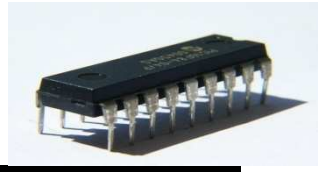


Q3. What is glitching power dissipation? How can it be minimized?

Ans: In digital circuits glitch is an undesired transition that occurs before the signal settles to its intended value. In other words, glitch is an electrical pulse of short duration that is usually the result of a fault or design error. As shown in the adjacent diagram, there is some delay at the output O_1, which results in a glitch at output O_2. As there is some capacitance associated with the output O_2, it leads to switching power dissipation. This switching power dissipation arising out of a glitch is known as glitching power dissipation.

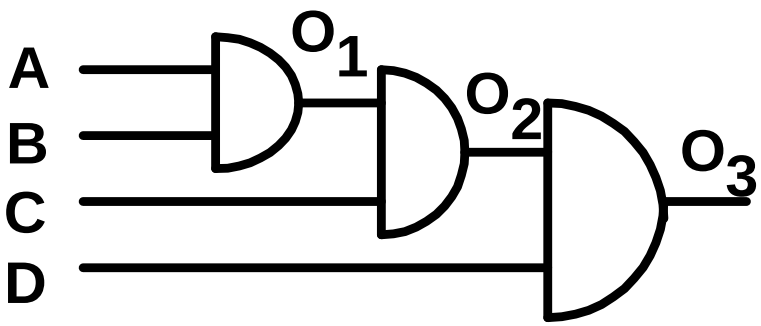


Answer to Questions of Lec-28

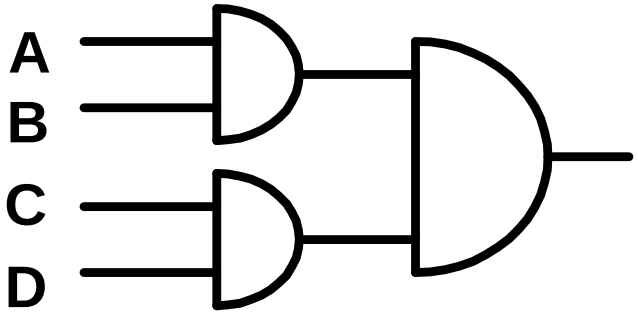


These “Extra” transitions can be minimized by

- Balancing all signal paths
- Reducing logic depth

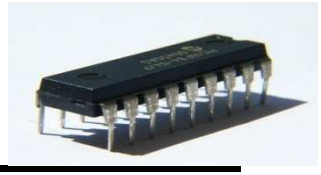


Realization of A.B.C.D in cascaded form where there is possibility of glitch.



Balanced realization of the same function with lesser possibility of glitch

Answer to Questions of Lec-28



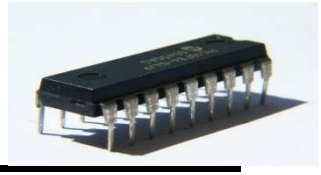
Q4. What are the potential logic styles for the realization of low power high performance CMOS circuits?

Ans: Potential Logic Styles are:

- **Static CMOS Logic**
- **Dynamic CMOS Logic**
- **Pass-Transistor Logic (PTL)**

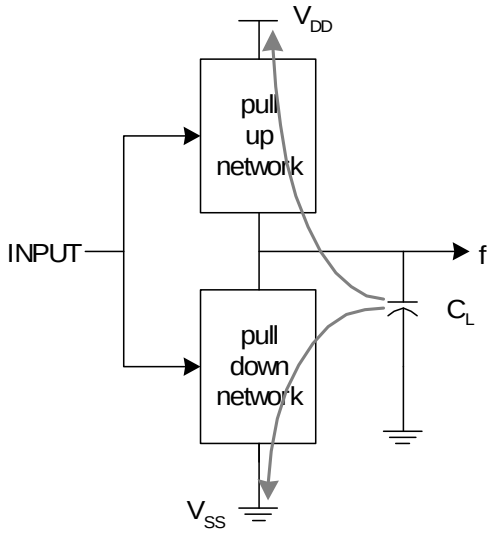
Ref: **D. Samanta, Ajit Pal, *Logic Styles for High Performance and Low Power*, Proceedings of the 12th International Workshop on Logic and Synthesis, 2003 (IWLS-2003), pp. 355-362, May 2003**

Answer to Questions of Lec-28



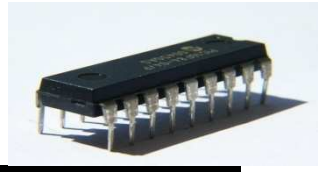
Static CMOS Logic

- Advantages
  - Ease of fabrication
  - Good noise margin
  - Robust
  - Lower switching activity
  - Good input/output decoupling
  - No charge sharing problem
  - Availability of matured logic synthesis tools and techniques

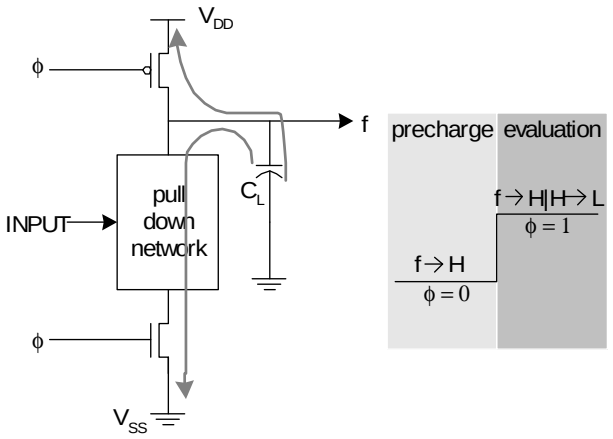


- Disadvantages
  - Larger number of transistors (larger chip area and delay)
  - Spurious transitions (glitch) due to finite propagation delays leading to extra power dissipation and incorrect operation
  - Short circuit power dissipation
  - Weak output driving capability
  - Large number of standard cells requiring substantial engineering effort for technology mapping

Answer to Questions of Lec-28



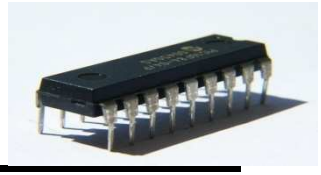
Dynamic CMOS Logic



- **Advantages**
- Combines the advantages of low power of static CMOS and low chip area of pseudo-nMOS
- Reduced number of transistors compared to static CMOS (n+2 versus 2n)
- Faster than static CMOS logic
- No short circuit power dissipation
- No spurious transition and glitching power dissipation

- **Disadvantages**
- Higher switching activity
- Not as robust as static CMOS logic
- Clock skew problem in cascaded realization
- Suffers from charge sharing problem
- Mature synthesis tool not available

Answer to Questions of Lec-28

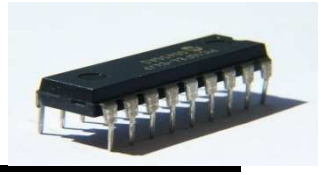


Pass-Transistor Logic

- Advantages
- Lower area due to smaller number of transistors and smaller input loads
- Ratio-less PTL allows minimum dimension transistors and hence makes area efficient circuit realization
- No short circuit current leading to lower power dissipation

- Disadvantages
- Increased delay due to long chain pf pass-transistors
- Multi-threshold voltage drop
- Dual-rail logic to provide all signals in complementary form
- There is possibility of sneak path

Review Questions of Lec-29



Q1. Why leakage power is an important in the deep sub micron technology?

Q2. What challenges we face in using threshold voltage scaling to minimize leakage power dissipation?

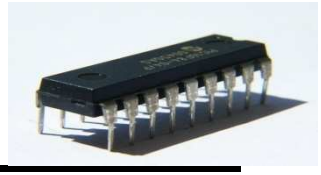
Q3. Explain how transistor staking can be used to reduce leakage power dissipation.

Q4. Distinguish between standby and runtime leakage power. Why runtime leakage power is becoming important in the present day context?

Q5. Compare between VTCMOS and MTCMOS for leakage power reduction.

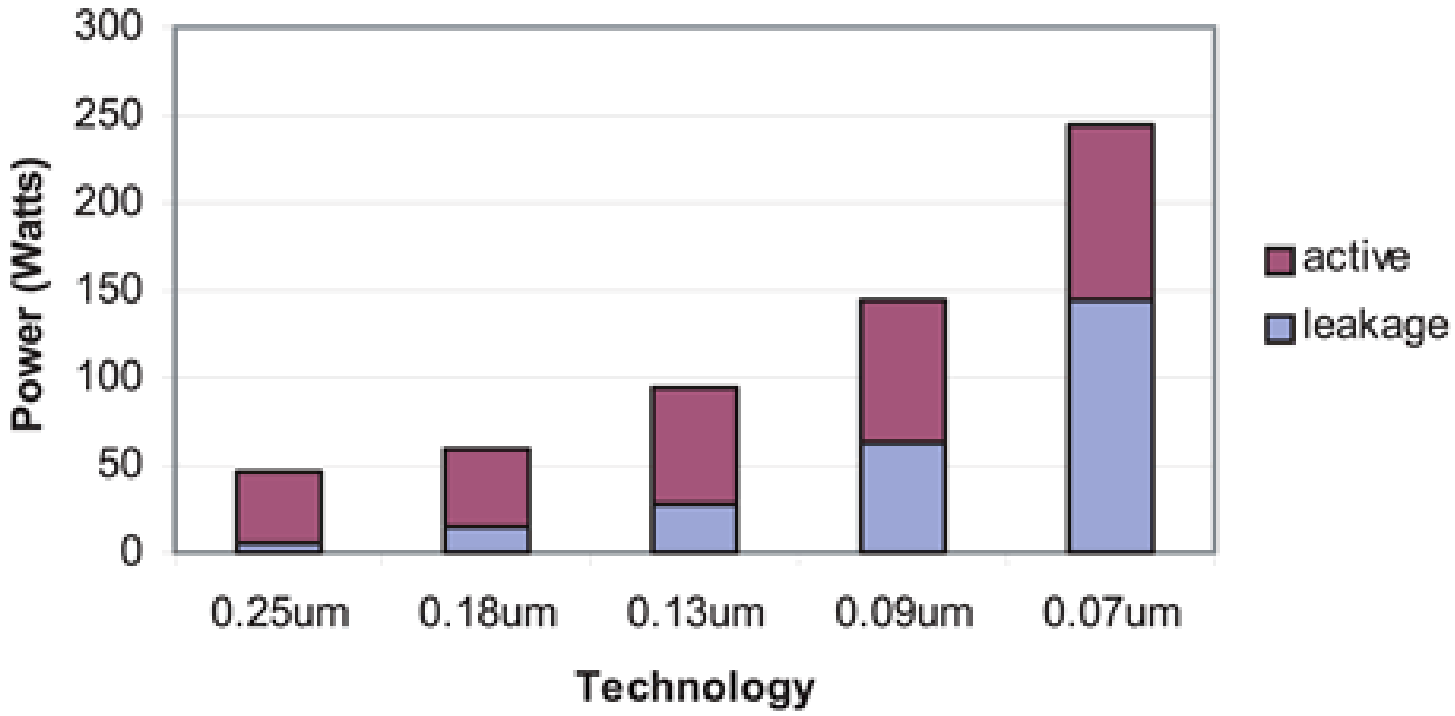
Q6. Give the advantages and limitations of MTCMOS approach.

Answer to Questions of Lec-29



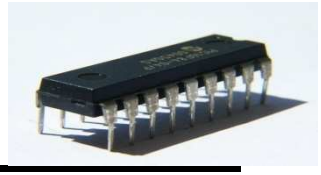
Q1. Why leakage power is an important in the deep sub micron technology?

Ans: As shown in the diagram, the leakage power component is increasing at a higher rate compared to dynamic power as we move towards deep sub micron technology. So, it has become an important issue.



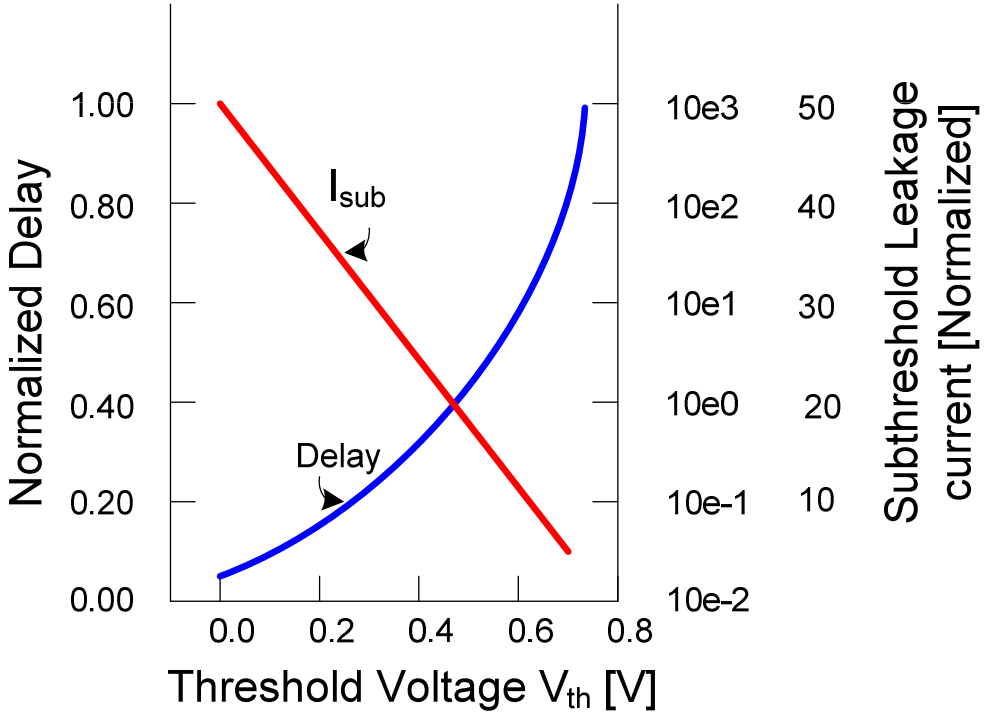
Source: Microprocessor power consumption, Intel

Answer to Questions of Lec-29

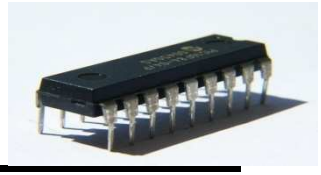


Q2. What challenges we face in using threshold voltage scaling to minimize leakage power dissipation?

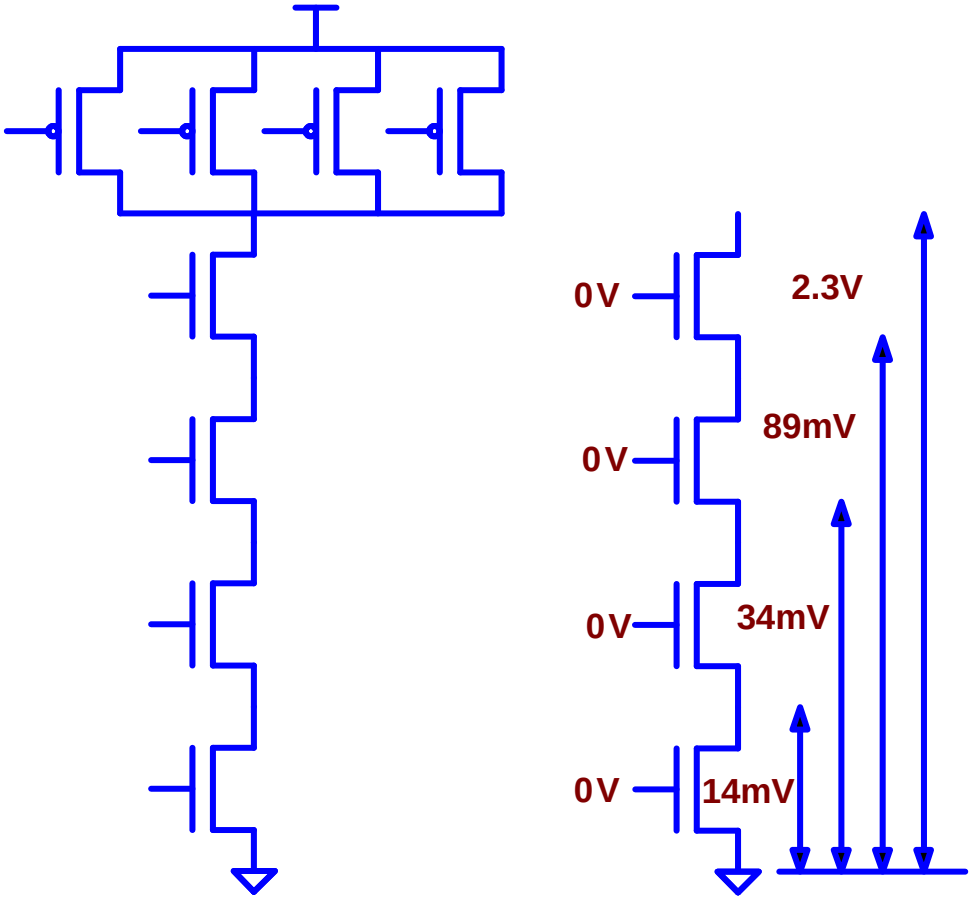
Ans: As supply voltage is scaled down to reduce power dissipation, the threshold voltage is also scaled down to maintain performance. As we do so, the subthreshold leakage current increases leading to high power dissipation. So, the challenge is to maintain performance with lower power dissipation.



Answer to Questions of Lec-29

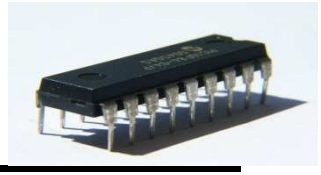


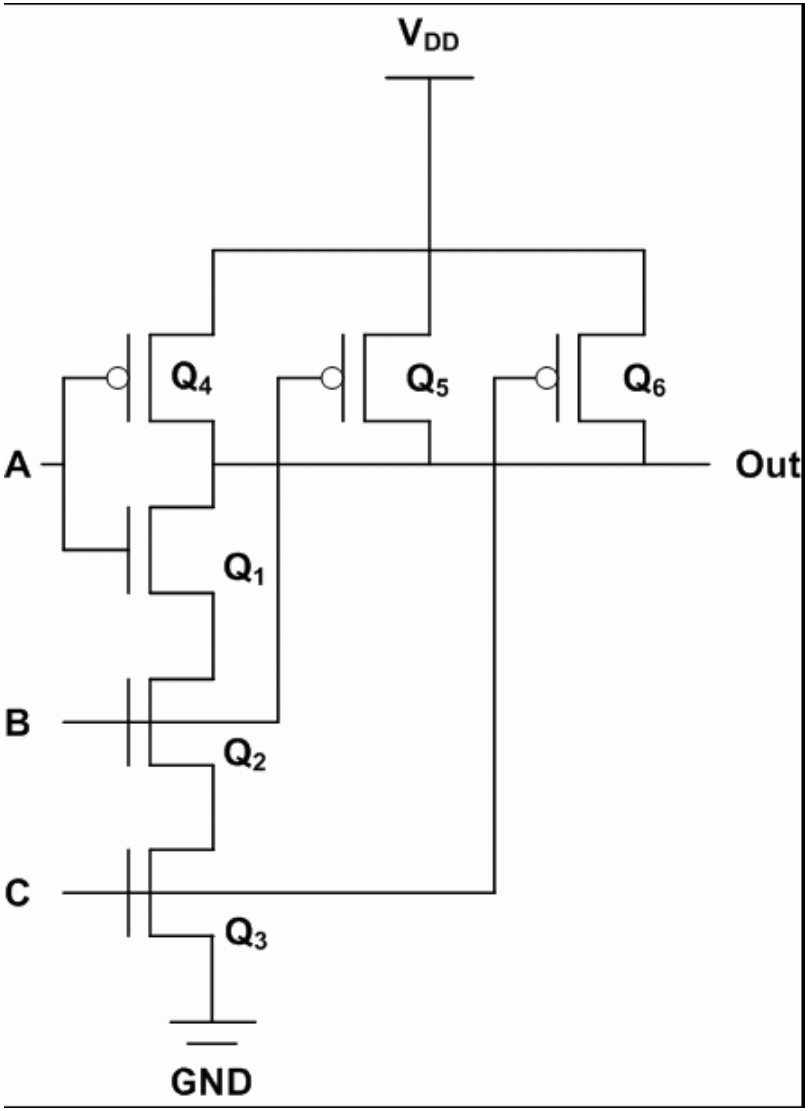
Q3. Explain how transistor staking can be used to reduce leakage power dissipation.



Ans: When more than one transistor is in series in a CMOS circuit, the leakage current has strong dependence on the number of turned off transistor. This is known as stacking effect. The highest leakage current is 99 times that of the lowest leakage current

Answer to Questions of Lec-29

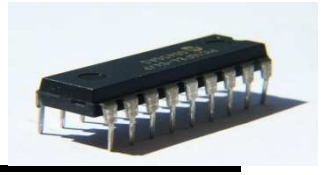




State (ABC)	Leakage Current (*nA*)	Leaking Transistors
000	0.095	*Q*1, *Q*2, *Q*3
001	0.195	*Q*1,*Q*2
010	0.195	*Q*1,*Q*3
011	1.874	*Q*1
100	0.184	*Q*2,*Q*3
101	1.220	*Q*2
110	1.140	*Q*3
111	9.410	*Q*4,*Q*5,*Q*6

A suitable input combination is used such that the reduction in leakage current due to stacking effect is maximized.

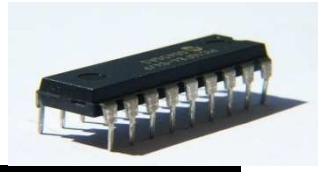
Answer to Questions of Lec-29



Q4. Distinguish between standby and runtime leakage power. Why runtime leakage power is becoming important in the present day context?

Ans: Standby leakage power dissipation takes place when the circuit is not in use, i.e. inputs do not change and clock is not applied. On the other hand, runtime leakage power dissipation takes place when the circuit is being used.

Answer to Questions of Lec-29

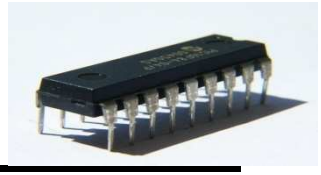


Q5. Compare between VTCMOS and MTCMOS for leakage power reduction.

Ans: In case of VTCMOS, basic principle is to adjust threshold voltage by changing substrate bias. Transistors initially have low V_{th} during normal operation and substrate bias is altered using substrate bias control circuit. The threshold is increased by using reverse body bias when the circuit is not in use. Effective in reducing leakage power dissipation in standby mode and it involved additional area and higher circuit complexity. So, it is a post-silicon approach.

On the other hand, in case of MTCMOS approach MOS transistors of multiple threshold voltages are fabricated in which a power gating transistor is inserted in the stack between the logic transistors and either power or ground, thus creating a virtual supply rail or a virtual ground rail, respectively. The logic block contains all low-Vth transistors for fastest switching speeds while the switch transistors, header and footer, are built using high-Vth transistors to minimize the leakage power dissipation. So, it is a pre-silicon approach.

Review Questions of Lec-30



Q1. Explain how standby power is reduced in MTCMOS technique. Discuss its advantage and disadvantages.

Q2. Explain how multiple threshold voltage transistors can be used to realize low voltage high performance circuits requiring low power (i) only in the standby mode, (ii) both in standby and active mode.

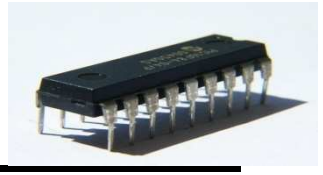
Q3. Compare the advantage and disadvantages of fine-grained and coarse-grained power gating approaches.

Q4. Distinguish between local and global power gating and compare their advantage and disadvantages.

Q5. Why is it necessary to isolate a signal as it goes from one voltage domain to another voltage domain? Explain how is it implemented?

Q6. Explain different approaches of state retention.

Answer to Questions of Lec-30



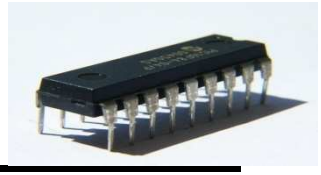
Q1. Compare and contrast clock gating versus power gating approaches.

Ans: Clock gating minimizes dynamic power by stopping unnecessary transitions, but power gating minimizes leakage power by inserting a high-Vt transistor in series with the low-vt logic blocks.

Q2. Compare the advantage and disadvantages of fine-grained and coarse-grained power gating approaches.

Ans: In case of fine-grained approach the switch is placed locally inside each standard cell and the switch must be designed to supply worst case current so that it does not impact performance. In this approach, the area overhead of each cell is significant (2X-4X). On the other hand, in case of coarse-grained approach, a block of gates has its power switched by a collection of switched cells. In this case the sizing is very difficult, but it has significantly less area overhead than that of fine grain approach. It is a preferred approach because of lesser area overhead.

Answer to Questions of Lec-30

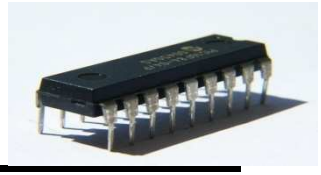


Q3. Distinguish between local and global power gating and compare their advantage and disadvantages.

Ans: Global power gating refers to a logical topology in which multiple switches are connected to one or more blocks of logic, and a single virtual ground is shared in common among all the power gated logic blocks. This topology is effective for large blocks (coarse-grained) in which all the logic is power gated, but is less effective for physical design reasons, when the logic blocks are small. It does not apply when there are many different power gated blocks, each controlled by different sleep enable signals.

On the other hand, local power gating refers to a logical topology in which each switch singularly gates its own virtual ground connected to its own group of logic. This arrangement results in multiple segmented virtual grounds for a single sleep domain.

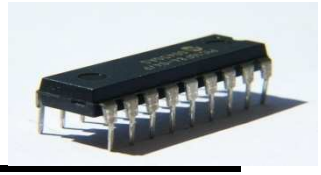
Answer to Questions of Lec-30



Q4. Why is it necessary to isolate a signal as it goes from one voltage domain to another voltage domain? Explain how is it implemented?

Ans: There is no guarantee that the power gated blocks will fully charge or discharge. As a consequence, the outputs of powered down blocks may result in crowbar currents in the powered up blocks. To overcome this problem, it is necessary to isolate a power gated block from a non power gated block.

Answer to Questions of Lec-30

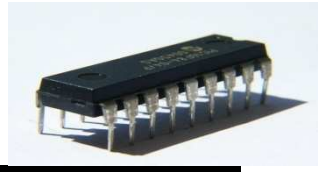


Q5. Explain different approaches of state retention.

Ans: Given a power switching fabric and an isolation strategy, it is possible to power gate a block of logic, but unless a retention strategy is employed, all state information is lost when the block is powered down. To resume its operation on power up, the block must either have its state restored from an external source or build up its state from the reset condition. In either case, the time and power required can be significant. The following three approached can be used

- **A software approach based on reading and writing registers**
- **A scan-based approach based on the re-use of scan chains to store state off chip**
- **A register-based approach that uses retention registers**

Review Questions of Lec-31



Q1. How supply voltage scaling leads to run time leakage power reduction?

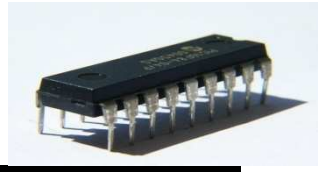
Q2. How can you combine power gating with dynamic voltage scaling to reduce power dissipation?

Q3. Explain the basic concept of dual Vt assignment for reduction of leakage power.

Q4. Distinguish between delay-constrained and energy-constrained dual Vt assignment approaches.

Q5. Explain how the threshold voltage can be dynamically adjusted to reduce leakage power dissipation.

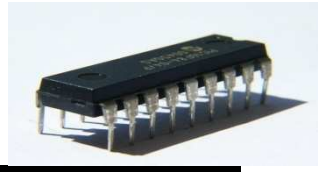
Answer to Questions of Lec-31



Q1. How supply voltage scaling leads to run time leakage power reduction.

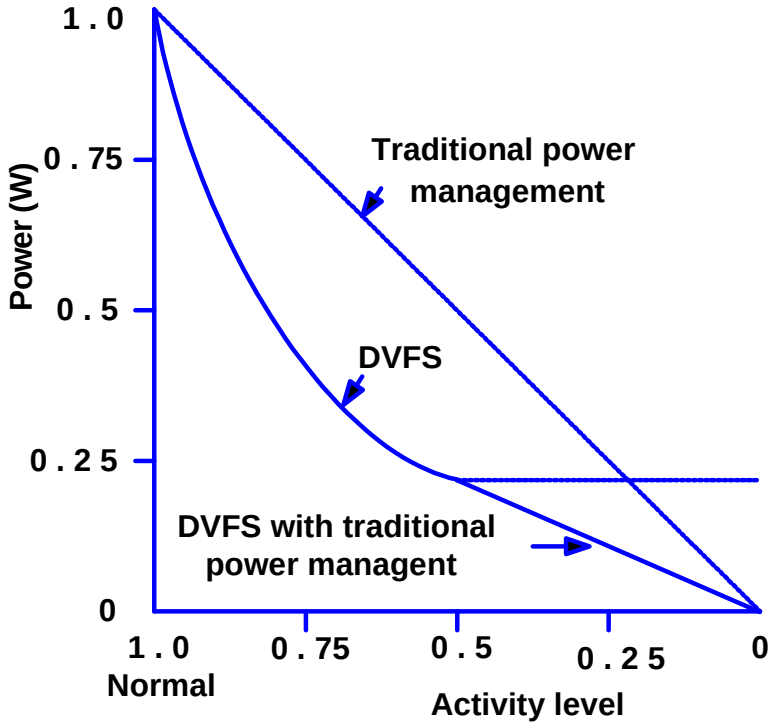
Ans: Supply voltage reduction not only leads to the reduction of dynamic power, it also leads to the reduction of leakage power. The subthreshold leakage due to GIDL and DIBL decreases as supply voltage is scaled down. It has also been demonstrated that the supply voltage scaling impacts in the orders of V^3 and V^4 on subthreshold leakage and gate leakage, respectively.

Answer to Questions of Lec-31

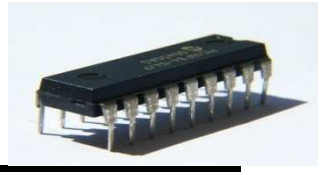


Q2. How can you combine power gating with dynamic voltage scaling to reduce power dissipation?

Ans: As the supply voltage along the frequency is lowered using the DVFS, the supply voltage hits the lower limit and the curve flattens out and the supply voltage cannot be further lowered. At this point it is more efficient to switch over to traditional power management, i.e. the supply voltage is turned on and off depending on the performance requirement. This is how one can combine the DVFS and traditional power management approach as shown in the diagram.



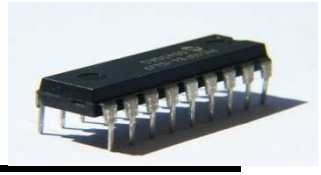
Answer to Questions of Lec-31



Q3. Explain the basic concept of dual Vt assignment for the reduction of leakage power.

Ans: This is based on the observation that all gates are not on the critical path when the circuit is represented with the help of a directed acyclic graph (DAG). So, gates on the critical path can be realized using Low-V_{th} transistors for high performance and the gates on the noncritical path are realized using high-V_{th} transistors to reduce leakage power. This is the basic concept of dualVt assignment.

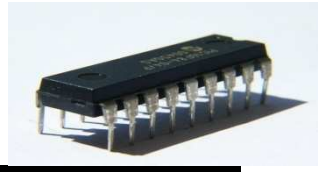
Answer to Questions of Lec-31



Q4. Distinguish between delay-constrained and energy-constrained dual Vt assignment approaches.

Ans: In delay-constrained approach, no compromise is made on performance. So, dual-Vt assignment is done such that there is no performance degradation. On the other hand, in energy constrained approach some compromise in performance is made, say 10% to 15%, to achieve larger reduction in the leakage power.

Answer to Questions of Lec-31

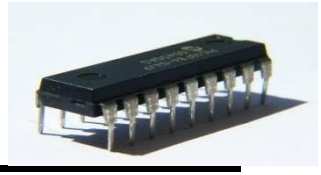


Q5. Explain how the threshold voltage can be dynamically adjusted to reduce leakage power dissipation.

Ans: Just like dynamic the Vdd scaling scheme, a dynamic Vth scheme (DVTS) can be used to reduce runtime leakage power in sub-100-nm generations, where leakage power is significant portion of the total power at runtime. When the workload is less than the maximum, the processor is operated at lower clock frequency. Instead of reducing the supply voltage, the DVTS hardware raises the threshold voltage using reverse body biasing to reduce runtime leakage power. Just enough throughput is delivered for the current workload by dynamically adjusting the Vth in an optimal manner to maximize leakage power reduction.

A simpler scheme is called Vth-hopping which dynamically switches between only two threshold voltages; Low-Vt and High-Vt as the frequency controller generates either FCLK or FCLK/2, respectively

Review Questions of Lec-32



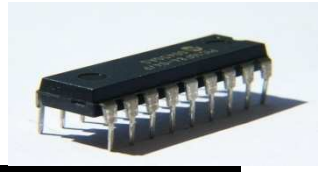
Q1. Distinguish between conventional charging (used in static CMOS circuits) and adiabatic charging of a load capacitance.

Q2. Explain how dynamic power dissipation is minimized using adiabatic switching?

Q3. Prove that the charging of a capacitor C in *n* steps to a voltage Vdd instead of a conventional single-step charging reduces the power dissipation by a factor of *n*.

Q4. Realize a 2-input OR/NOR gate using positive feedback adiabatic logic (PFAL) circuit. Explain its operation.

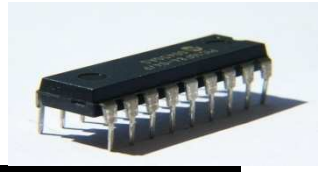
Answer to Questions of Lec-32



Q1. Distinguish between conventional charging (used in static CMOS circuits) and adiabatic charging of a load capacitance.

Ans: Switching power dissipation in static CMOS circuit with capacitive load C_L has a lower limit of $C_L V_{dd}^2/2$. On the other hand, charge moves efficiently from power supply to the load capacitance by using slow, constant-current charging. Reversing the current source will cause the energy to flow from the load capacitance back into the power supply. The power supply must be so designed to retrieve the energy fed back to it. Adiabatic-switching circuits require non-constant, non-standard power supply with time-varying voltage. This supply is called "Pulsed-power supplies".

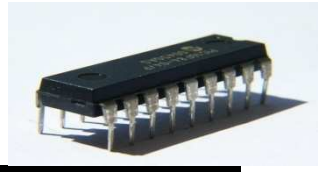
Answer to Questions of Lec-32



Q2. Explain how dynamic power dissipation is minimized using adiabatic switching?

Ans: In adiabatic switching, a time-dependent current source, I(t) is used to charge the capacitance C through a resistor R. For T>2RC, the dissipated energy is smaller than the conventional lower limit $C_L V_{dd}^2/2$. The dissipation can be made arbitrarily small by extending the charging time T. As the dissipated energy is proportional to R, a smaller R results in a lower dissipation unlike conventional case.

Answer to Questions of Lec-32

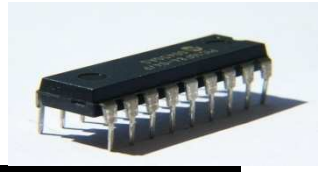


Q3. Prove that the charging of a capacitor C in *n* steps to a voltage Vdd instead of a conventional single-step charging reduces the power dissipation by a factor of *n*.

Ans: Energy dissipation for single step charging $E = C_L V^2 / 2$.

Energy dissipation in each of n step charging is equal to $E_{step} = C_L V^2 / 2n^2$ .The total energy dissipation in N step charging equal to $N.E_{step} = N. (C_L V^2 / 2n^2) = C_L V^2 / 2n$. Therefore, $E_{step} / E = 1/n$. Therefore, the power dissipation reduces by a factor of n.

Answer to Questions of Lec-32



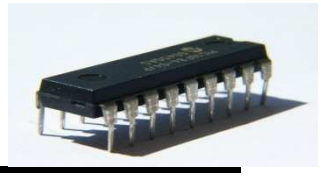
Q4. Realize a 2-input OR/NOR gate using positive feedback adiabatic logic (PFAL) circuit. Explain its operation.

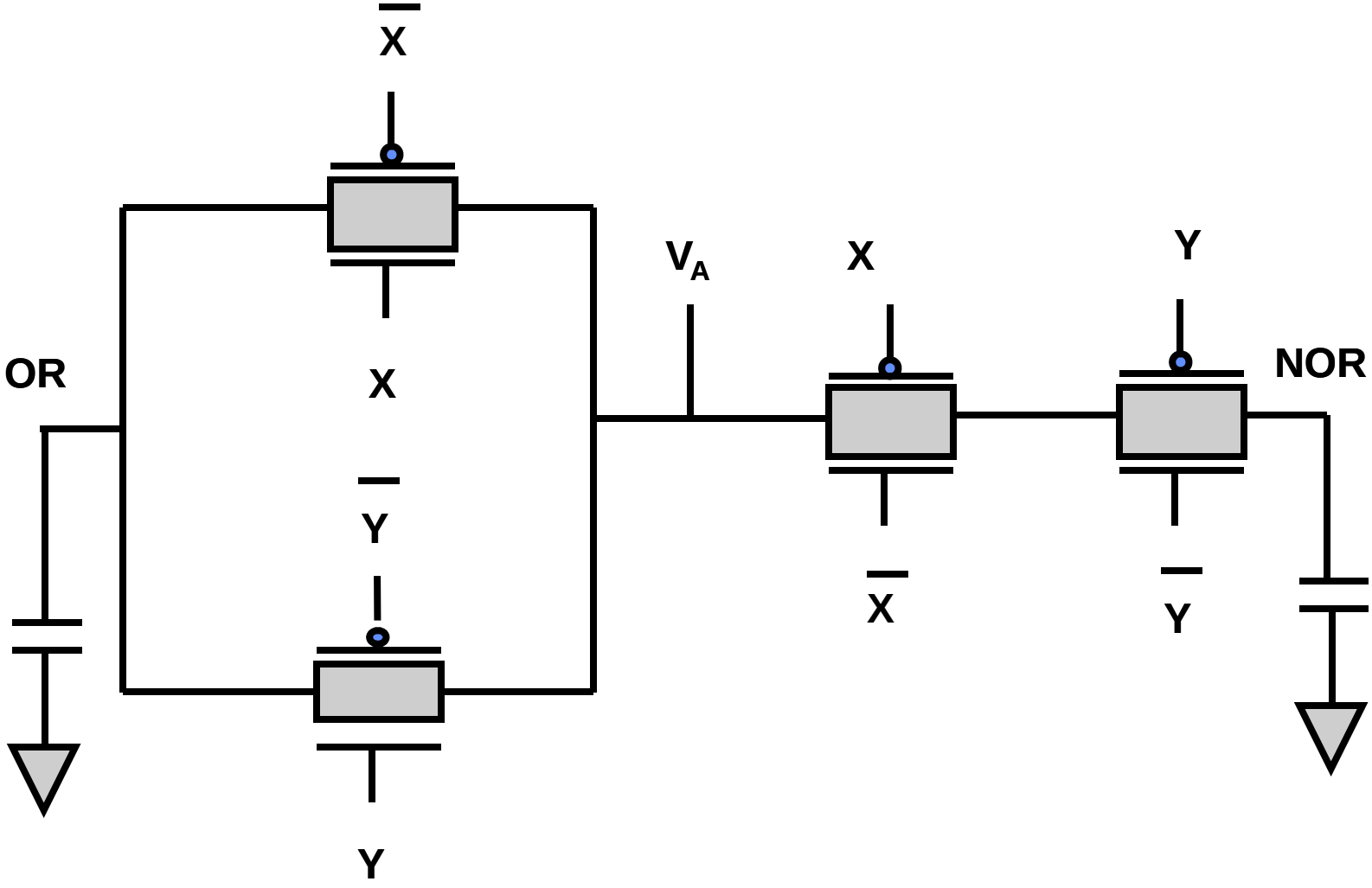
Ans: Perform the following steps:

1. **Replace each of the PMOS and NMOS devices in the pull-up and pull-down networks with T-gates.**
2. **Use expanded pull-up network to drive the true output. Use expanded pull-down network to drive the complementary output.**
3. **Both networks in the transformed circuit are used to charge and discharge the load capacitance.**
4. **Replace DC Vdd by a pulsed power supply with varying voltage to allow adiabatic operation.**

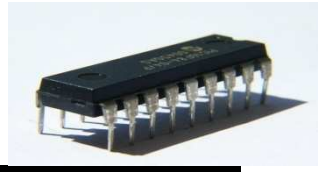
The realization is shown in the next slide

Answer to Questions of Lec-32





Review Questions of Lec-33



Q1. Write a short note on "Battery-driven system design".

Q2. Explain *rate capacity effect for* rechargeable batteries.

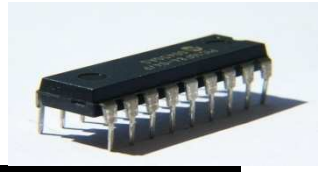
Q3 Explain *recovery effect for* rechargeable batteries.

Q3. What is the 'non-increasing profile effect' of a battery?

Q4. Explain the basic steps of battery aware task scheduling. How does it improves the lifetime of a Battery?

Q5. Why is the reverse body biasing important to extend the battery life in the present day context?

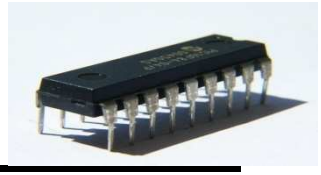
Answer to Questions of Lec-33



Q1. Write a short note on "Battery-driven system design".

Ans: In recent years there large proliferation of portable computing and communication equipment, such as laptops, palmtops, cell-phones, etc. and the growth rate of these portable equipment is very high. The complexity of these devices is also increasing with time, leading to larger energy consumption. As these devices are battery operated, battery life is of primary concern. Unfortunately, the battery technology has not kept up with the energy requirement of the portable equipment. Moreover, the commercial success of these products depend on weight, cost and battery life. Low power design methodology is very important to make these battery-operated devices commercially viable.

Answer to Questions of Lec-33



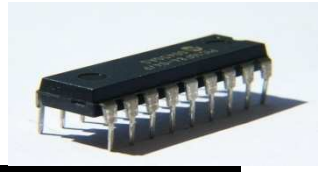
Q2. Explain *rate capacity effect for* rechargeable batteries.

Ans: Dependency between the actual capacity and the magnitude of the discharge current depends on the availability of active region. When discharge rate is high, surface of the cathode gets coated with insoluble compound. This prevents access to many active areas and consequent reduction of actual capacity of the battery. As a result, a higher rate of discharge leads to a lower available capacity. This is known as Rate Capacity effect.

Q3 Explain *recovery effect for* rechargeable batteries.

Ans: Availability of charge carriers D\depends of the concentration of positively charged ions near the cathode. When heavy current is drawn, rate at which positively charged ions consumed at the cathode is more than supplied. This improves as the battery is kept idle for some duration. As a consequence, the battery voltage recovers in idle periods.

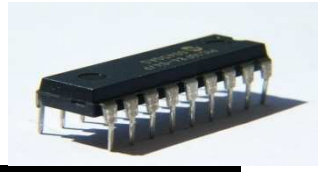
Answer to Questions of Lec-33



Q3. What is the 'non-increasing profile effect' of a battery?

Ans: It has been experimentally verified that if the tasks consuming higher power are scheduled first followed by tasks with decreasing power consumption, then energy available in the battery is larger compared to other schedules. This is known as non-increasing profile effect.

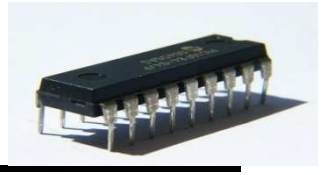
Answer to Questions of Lec-33



Q4. Explain the basic steps of battery aware task scheduling. How does it improves the lifetime of a Battery?

Ans: There are three steps. In the first step, an early deadline first (EDF) based schedule is made, provided the task dependencies are not violated. In the second step, the task schedule is modified by scheduling the tasks in the non increasing order of the current loads provided the deadlines and the task dependencies are not violated. In the third step, starting from the last task, the slack obtained at the end of the task is utilized to get the optimal pair of supply voltage and the body bias voltage. This procedure is followed until either there is no more slack, or further scaling down not possible.

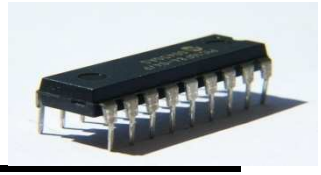
Answer to Questions of Lec-33



Q5. Why is the reverse body biasing important to extend the battery life in the present day context?

Ans: With the advancement of technology, as the process technology further gets lower, the energy due to static power becomes more significant, and the algorithm using RBB to reduce the leakage current provides larger saving in power dissipation.

Review Questions of Lec-34



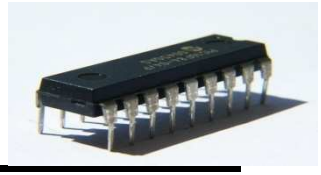
Q1. What is the limitation of contemporary CAD tools?

Q2. Give a summary of the benefits and impacts of the different low power techniques.

Q3. What is provided by UPF?

Q4. What are the key features of Eclypse, the low-power CAD tool of Synopsis?

Answer to Questions of Lec-34



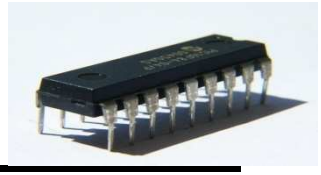
Q1. What is the limitation of contemporary CAD tools?

Ans: In RTL coding there is no provision to use Multi-Vt , Multi-Vdd, Body biasing and power gating in RTL synthesis. So, the static power reduction techniques cannot be used. As supply voltage and the operating frequency are also not handled at the RTL level, the dynamic power can be reduced primarily by reducing the switching activity α. Commonly used techniques in RTL synthesis to reduce α are:

- **Bus encoding**
- **Clock gating**
- **FSM state assignment**

Q2. Give a summary of the benefits and impacts of the different low power techniques.

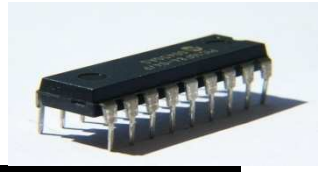
Answer to Questions of Lec-34



Ans: The benefits and impacts of different low power techniques is summarized in the following table. These techniques can significantly reduce power consumption in deep submicron chips. However, these techniques traditionally require ad-hoc, time-consuming, risk-prone, and manual verification and implementation approaches, unless automated using CAD tools.

Technique	Dynamic Power Benefit	Static Power Benefit	Design Impact	Verification Impact	Implementation Impact
Clock Gating	Large	Small	Small	Small	Small
Multi-Vdd	Large	Small	Little	Low	Medium
DVFS	Large	Small	Medium	Large	Medium
Multi-Vt	Small	Large	Medium	Small	Medium
Power Gating	Small	Very Large	Medium	Large	Medium

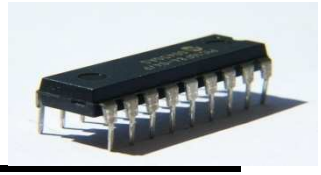
Answer to Questions of Lec-34



Q3. What is provided by UPF?

Ans: UPF provides the ability for electronic systems to be designed with power as a key consideration early in the process. It accomplishes this through the ability to allow the specification of implementation-relevant power information early in the design process — RTL (register transfer level) or earlier. UPF provides a consistent format to specify power-aware design information that cannot be specified in HDL code or when it is undesirable to directly specify within the HDL logic, as doing so would tie the logic specification directly to a constrained power implementation.

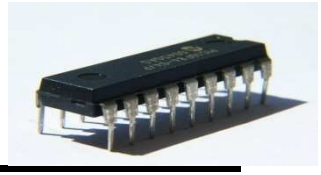
Answer to Questions of Lec-34



Q4. What are the key features of Eclypse, the low-power CAD tool of Synopsis?

Ans: Eclypse provides a comprehensive approach – power-aware tools at all levels of design hierarchy starting from early architectural and system-level analysis to verification, RTL synthesis, test, physical implementation and sign-off. This supports the Accellera Unified Power format – an open industry standard to specify power intent and it is backed by the popular "Low Power Methodology Manual" (LPMM).

Review Questions of Lec-35



Q1. How parameter variations impact on circuits and microarchitecture of present day VLSI circuits?

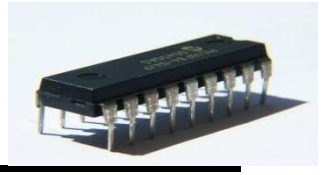
Q2. Why current or future technologies result in two-sided constraints?

Q3. What are the basic approaches for variation tolerant design?

Q4. Explain how you can achieve low power single-Vt circuits using judicious use of sizing?

Q5. Explain how you can use adaptive body biasing to improve yield.

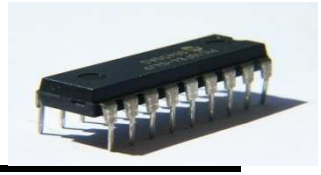
Answer to Questions of Lec-35



Q1. How parameter variations impact on yield of present day VLSI circuits?

- **Ans: Fluctuations are attributed to the manufacturing process (e.g., drifts in L_{eff}, T_{ox}, V_t, or N_{cheff}), which affect circuit yield. For example, with in die variation in L_{eff} can be as high as 50%. 30% delay variation and 20X leakage variation between fast and slow dies have been reported for 0.18µ CMOS process. Low leakage chips with too low frequency must be discarded and high frequency chips with too high leakage must also be discarded. This lwads to reduction in yield.**

Answer to Questions of Lec-35



Q2. Why current or future technologies result in two-sided constraints?

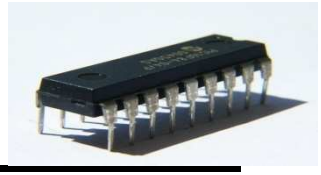
Ans: Lower channel length leads to smaller threshold voltage and larger power dissipation and higher channel length leads to higher threshold voltage and longer delay. This leads to two-sided constraints for current and future technologies.

Q3. What are the basic approaches for variation tolerant design?

Ans: Basic approaches are:

(a) To reduce the sources of variations, (b) Reduce the effects of variation at the time of design and (c) Reduce effects of variation after fabrication (post-silicon) such as reverse body biasing.

Answer to Questions of Lec-35



Q4. Explain how you can achieve low power single-Vt circuits using judicious use of sizing?

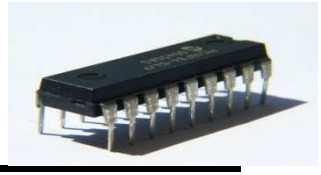
Ans: This can be done in three steps:

Step-I: Upsize gates on the critical path to reduce delay of the entire circuit.

Step II: Increase threshold voltage of the MOSFETs of the entire circuit to minimize leakage power

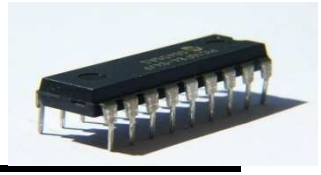
Step III: Downsize gates on the non critical path to reduce area and dynamic power

Answer to Questions of Lec-35



Q5. Explain how you can use adaptive body biasing to improve yield.

Ans: Starting with Vt lower than the target voltage, adaptive body biasing can be used to match the mean Vt of all the die samples. The die samples that require larger body bias to match its mean Vt to the target Vt end with higher within-die variation.



Thanks!