1. Difference between transition delay and path delay?
2. Define SDD?Ans:Software Design Description (IEEE 1016–2009), a standard that specifies the form of the document used to specify system architecture and application design in a software-related project. Software Design Document, a written outline of the development of a course or a description of a software product.
3. How do you propagate fault through AND gate?
4. Define the bridging fault?
5. How is At speed testing done?
6. Explain the entire flow of DFT.
7. **Interview:** Technical Questions: Timing Analysis, DRC Fix Methods, Understanding of Noise, Place and Route Principles

   Behavioral Questions: Stress management, workload management. Time management skills, What would you do if you had multiple deadlines on the same day.

   How do you prioritise your work.
8. Explain setup and hold time.

9. generate and print first N binary palindromes .
ex first 4 are as follow
1
11
101
111

10. Given an array of integers, rearrange the array in such a way that the first element is first maximum and second element is first minimum.
Input : {1, 2, 3, 4, 5, 6, 7}
Output : {7, 1, 6, 2, 5, 3, 4}

11. javascript data types?

12. Dynamic memory allocation-Constructors-Data Structure-Logical questions-Basic Linux c Commands

13. Cache coherence

14. RTL design

15. Design a divide by 3 counter

16.what is refresh rate of a Led matrix?

17. Asynchronous FIFO depth calculation, System verilog testbench overview

18. Logic Families, Mux, Demux, In CMOS circuits, which among tphl and tplh is longer? And why? Divide-by-3 counter, Round 2:- (after a wait of the futile 4 hours) Significance of 'reset' signal in digital circuits Given a step input to a low pass filter, high pass filter and band pass filter respectively, what do you expect the output to look like? Dissimilate a square wave into its harmonics (this question because I had mentioned signal processing projects in my resume) Now a days we have a large number of cells in logic blocks? What do you think is the approach to detect an error in such a case?

19. FIR & IIR Filter design, Polyphase structure, Heisenberg Uncertainty Principle(related to time frequency analysis), DCT, DFT, FFT, GPU and VPU difference

20. analog design basics such as amplifiers and opamps. knowledge of capacitors is a must

21. Low pass filter and high pass filter,their characteristics.

22. Step response of a few RC Circuits

23. ring oscillator

24. **What is glitch? What causes it (explain with waveform)? How to overcome it?**

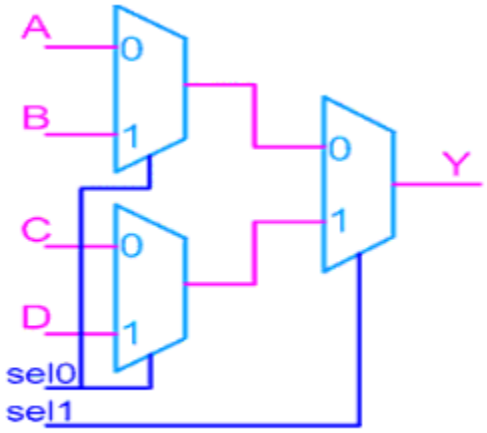
25. **Given only two xor gates one must function as buffer and another as inverter?**

Tie one of xor gates input to 1 it will act as inverter.
Tie one of xor gates input to 0 it will act as buffer.

26. **What is difference between latch and flipflop?**

The main difference between latch and FF is that latches are level sensitive while FF are edge sensitive. They both require the use of clock signal and are used in sequential logic. For a latch, the output tracks the input when the clock signal is high, so as long as the clock is logic 1, the output can change if the input also changes. FF on the other hand, will store the input only when there is a rising/falling edge of the clock.

27. **Build a 4:1 mux using only 2:1 mux?**



28. **Difference between mealy and moore state machine?**

A) Mealy and Moore models are the basic models of state machines. A state machine which uses only Entry Actions, so that its output depends on the state, is called a Moore model. A state machine which uses only Input Actions, so that the output depends on the state and also on inputs, is called a Mealy model. The models selected will influence a design but there are no general indications as to which model is better. Choice of a model depends on the application, execution means (for instance, hardware systems are usually best realized as Moore models) and personal preferences of a designer or programmer

B) Mealy machine has outputs that depend on the state and input (thus, the FSM has the output written on edges)

Moore machine has outputs that depend on state only (thus, the FSM has the output written in the state itself.

Adv and Disadv
In Mealy as the output variable is a function both input and state, changes of state of the state variables will be delayed with respect to changes of signal level in the input variables, there are possibilities of glitches appearing in the output variables. Moore overcomes glitches as output dependent on only states and not the input signal level.
All of the concepts can be applied to Moore-model state machines because any Moore state machine can be implemented as a Mealy state machine, although the converse is not true.
Moore machine: the outputs are properties of states themselves... which means that you get the output after the machine reaches a particular state, or to get some output your machine has to be taken to a state which provides you the output.The outputs are held until you go to some other state Mealy machine:
Mealy machines give you outputs instantly, that is immediately upon receiving input, but the output is not held after that clock cycle.

29. **Difference between onehot and binary encoding?**

30. **Implement an AND gate using mux?**

This is the basic question that many interviewers ask. for and gate, give one input as select line,incase if u r giving b as select line, connect one input to logic '0' and other input to a.

31. **Why is NAND gate preferred over NOR gate for fabrication**

NAND is a better gate for design than NOR because at the transistor level the mobility of electrons is normally three times that of holes compared to NOR and thus the NAND is a faster gate.
Additionally, the gate-leakage in NAND structures is much lower. If you consider t_phl and t_plh delays you will find that it is more symmetric in case of NAND (the delay profile), but for NOR, one delay is much higher than the

other(obviously t_plh is higher since the higher resistance p mos's are in series connection which again increases the resistance).

32. **What is Noise Margin? Explain the procedure to determine Noise Margin**

The minimum amount of noise that can be allowed on the input stage for which the output will not be effected.

33. Implementation of all basic gates using MUX
34. Implementation of all gates using universal gates (NAND, NOR)