M.Tech 2022 batch Mock test-1 on fundamentals

This test is only to make you understand how good you are in fundamentals, so that you can revise for all future recruitment processes.
Scores will be sent to the mail id you enter in this form.
For any preparation related queries, you can reach out to me.
My email ID: s_shivanathuni@blr.amrita.edu
Wish you all the best!!

Regards,
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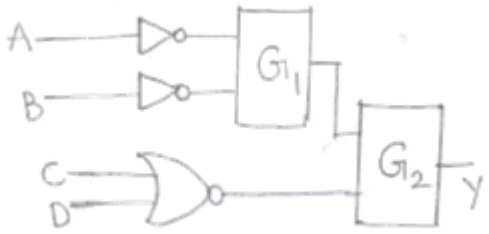
If the functions W, X, Y and Z are as follows W = R + PQ + RS ; X = PQR'S' + P'Q'R'S' + PQ'R'S' ; Y = RS + (PR+P'Q' + P'Q')' ; Z = R+S+(PQ + P'Q'R' + PQ'S')'. Then *

- (●) W = Z, X = Z'
- ( ) W = Z, X = Y
- ( ) W = Y
- ( ) W = Y= Z'

In the figure shown, the output Y is required to be y = AB + C'D'. The gates G1 and G2 must be *



- (●) NOR, OR
- ( ) OR, NAND
- ( ) NAND, OR
- ( ) AND, NAND

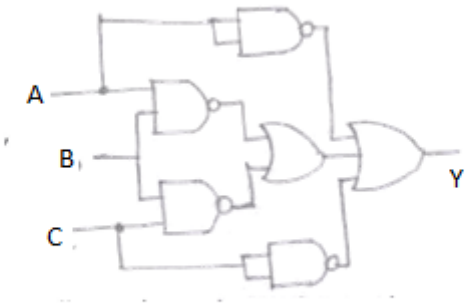
What are the minimum number of 2 - to -1 multiplexers required to generate a 2-input AND gate and a 2-input Ex-OR gate? *

- ( ) 1 and 2
- ( ) 1 and 3
- (●) 1 and 1
- ( ) 2 and 2

For realization of SR flip-flop from JK flip-flop, if S=1, R=0 & present state is 0 then the excitation input will be *

- ( ) . J =1, K =1
- ( ) J= 1, K = X
- ( ) J = X, K =1
- (●) J =0, K = X

For the circuit shown in figure, the output is equal to *

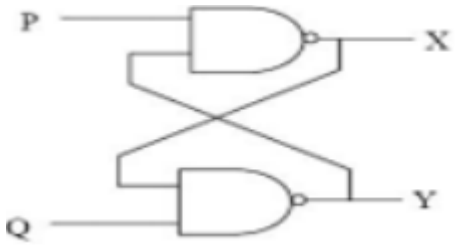


- (ABC)'
- A' + B' + C'
- (AB)' + (BC)' + A' + C'
- (AB)' + (BC)'

Calculate gm for a JFET having IDSS = 8mA, VP = -4V and is biased to operate VGS = -1.8V. *

- 2.2 mS
- 4.4mS
- 1.1mS
- 0

In the latch circuit shown, the NAND gates have nonzero, but unequal propagation delays. The present input condition is: P = Q = '0'. If the input condition is changed simultaneously to P = Q = '1', the outputs X and Y are *



- X = '1', Y = '1'
- either X = '1', Y = '0' or X = '0', Y = '1'
- either X = '1', Y = '1' or X = '0', Y = '0'
- X = '0', Y = '0'

The Boolean function Y = AB + CD is to be realized using only 2 - input NAND gates. The minimum number of gates required is *

- 2
- 3
- 4
- 5

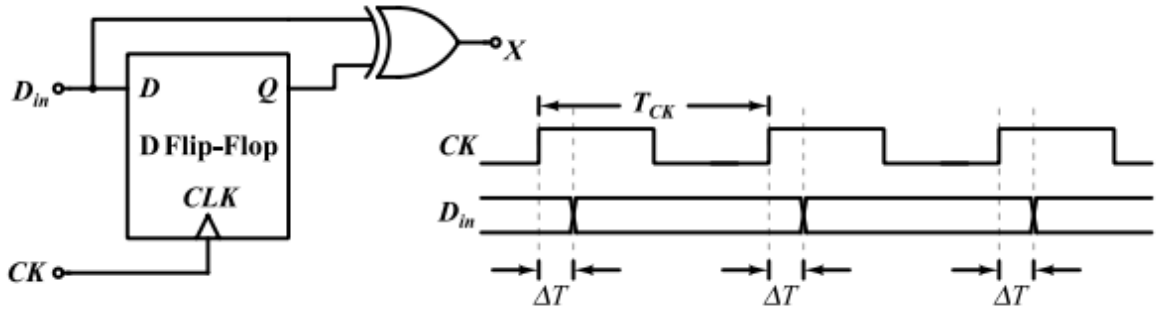
Which of the following is the Universal Flip-flop? *

- D Flip-Flop
- JK Flip-Flop
- SR Flip-Flop
- T Flip-Flop

Registration Number (Enter full reg. No. please) *

Your answer

In the circuit shown below, a positive edge-triggered D Flip-Flop is used for sampling input data Din using clock CK. The XOR gate outputs 3.3 volts for logic HIGH and 0 volts for logic LOW levels. The data bit and clock periods are equal and the value of $\Delta T/TCK$ = 0.15, where the parameters ΔT and TCK are shown in the figure. Assume that the Flip-Flop and the XOR gate are ideal. If the probability of input data bit (Din) transition in each clock period is 0.3, the average value (in volts, accurate to two decimal places) of the voltage at node X, is _____. *



Your answer

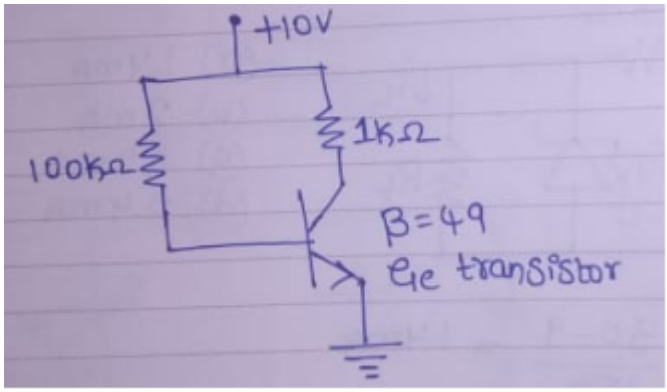
The source of FET is analogous to ..... of BJT *

- Collector
- Substrate
- Base
- Emitter

In the ohmic region, the FET can be used as *

- Voltage variable capacitor
- Voltage variable inductor
- Voltage variable resistor
- None of the above

Find the stability factor 'S' for the circuit shown *



- 49
- 50
- 51
- 150

What is the maximum transconductance of JFET having IDSS = 8 mA and VP= -4V *

- 2 mS
- 4 mS
- 1 mS
- 8 mS

A FET differs from a bipolar transistor as it has *

- Negative resistance
- Simpler fabrication
- High input impedance
- Any of the above

What is the maximum voltage gain obtained from FET having gm = 5 mS and rd = 20KOhm *

- 200
- 100
- 50
- 125

A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is *

- 40 ns
- 60 ns
- 12 ns
- 0 ns

In 8086 microprocessor, the address bus is ------ wide. *

- 8-bit
- 16-bit
- 20-bit
- 4-bit

Which of the following is valid for both P-N-P as well as N-P-N transistor *

- The emitter injects holes into the base region
- The electrons are the minority carriersin the base region
- The EB junction is forward biased for active operation
- All above are valid

The Boolean expression (X+Y)(X+Y')+(X'Y'+X')' simplifies to *

- X
- Y
- XY
- X + Y

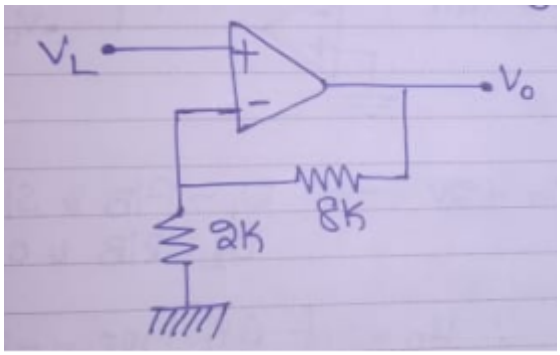
The 8051 microcontroller is of ___pin package as a _____ processor. *

- 30, 1byte
- 20, 1 byte
- 40, 8 bit
- 40, 8 byte

Name *

Your answer

The Op-amp given below has a very small open loop voltage gain of 45. But it is otherwise ideal. What is the closed loop voltage gain. *



- 45
- 4.5
- 450
- 0.45

The main disadvantage of the FET is its *

- Low input impedance
- Low thermal stability
- High noise
- Low gain-band width product

If one wants to design a binary counter, preferred type of flip-flop is *

- Latch
- D Flip-Flop
- . SR Flip-Flop
- JK Flip-Flop

11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number? *

- -7, -7 and -7 respectively
- 25, 9 and 57 respectively
- -25, -9 and -57 respectively
- -6, -6 and -6 respectively

In 8085 microprocessor system with memory mapped I/O, which of the following is true? *

- Devices have 8-bit address lines
- Devices are accessed using IN and OUT instructions
- There can be maximum of 256 input devices and 256 output devices
- Arithmetic and logic operations can be directly performed with the I/O data

A diode has a leakage current of 10 μA. Find its value if temperature is increased by 25 degree Centigrade *

- 28 μA
- 56.56 μA
- 34 μA
- 48 μA

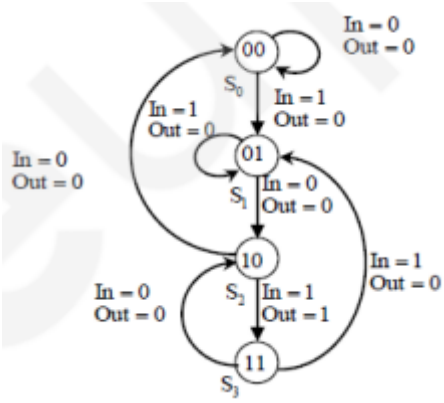
The minimized logical form of the logical expression (A'B'C' + A'BC' + A'BC + ABC') is *

- A'C' + BC' + A'B
- AC' + B'C + A'B
- A'C + B'C + A'B
- AC' + B'C + AB'

The datasheet of an op-amp gives a mid band voltage gain of 2,00,000 with a cut-off frequency of 10 Hz. What is the voltage gain at 1 MHz? *

- 2,000
- 200
- 2
- 2,00,000

. The state diagram of a finite state machine (FSM) designed to detect an overlapping sequence of three bits is shown in the figure. The FSM has an input „In" and an output 'Out'. The initial state of the FSM is S0. If the input sequence is 10101101001101, starting with the left-most bit, then the number times 'Out' will be 1 is _____. *

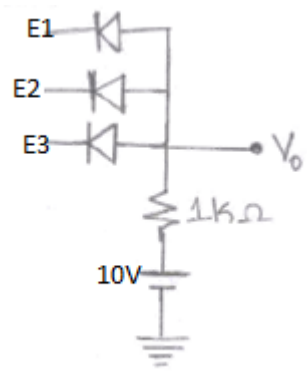


- 4
- 8
- 12
- 10

The main difference between a register and a counter is *

- A counter has no specific sequence of states.
- A register has capability of storing one bit of information where as counter has n-bit
- A register has no specific sequence of states
- None of the above

In the circuit shown diodes D1, D2 and D3 are ideal, and the inputs E1, E2 and E3 are '0V' for logic '0', and '10V' for logic '1'. What logic gate does the circuit represent? *



- 3 - input OR gate
- 3 - input NOR gate
- 3 - input AND gate
- 3 - input XOR gate

The Boolean expression for the truth table shown is *

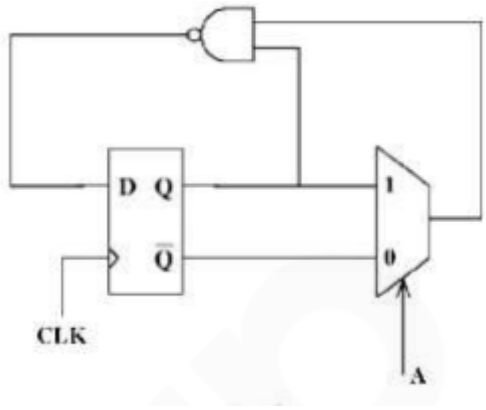
A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

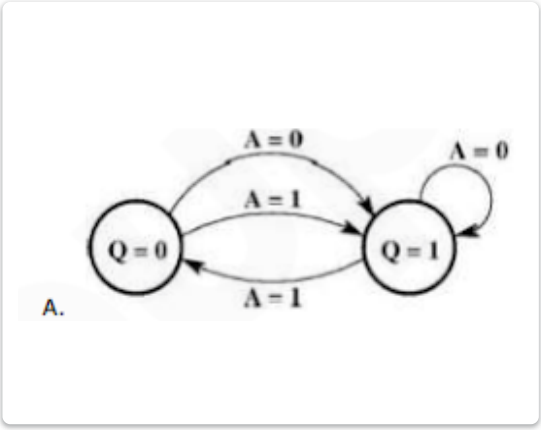
- B(A+C)(A'+C')
- B(A+C')(A'+C)
- B'(A+C')(A'+C)
- B'(A+C)(A'+C')

A FET is a.....controlled device whereas a bipolar transistor is a.....controlled device. *

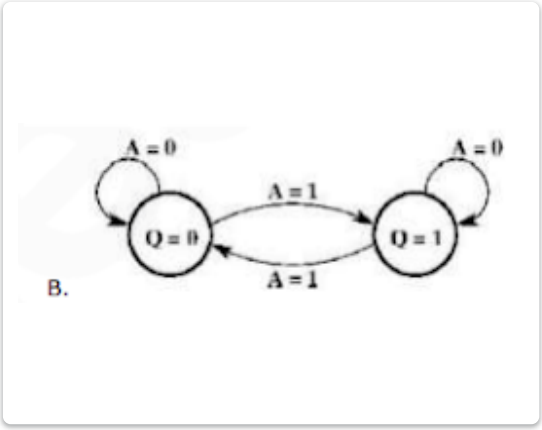
- Current, voltage
- Drain, gate
- Gate, drain
- Voltage, current

The state diagram for the circuit shown is *

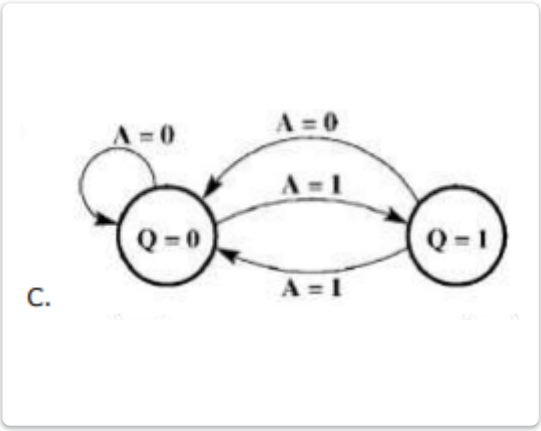




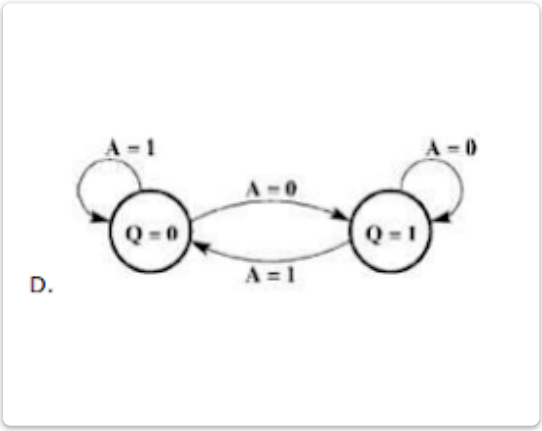
Option 1



Option 2



Option 3



Option 4

For D flip-flop to JK flip-flop, the characteristics equation is given by: *

- D = JQ+KQ'
- D = JQ'+KQ
- . D = JQ'+K'Q
- D = J'Q+KQ'

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