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# Colibri Computer Module

## Carrier Board Design Guide

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| **Issued by:** | Toradex | **Document Type:** | Carrier Board Design Guide |

| | |
|---|---|
| **Purpose:** | This document is a guideline for developing a carrier board that confirms to the specifications for the Colibri Computer Module |

| | |
|---|---|
| **Document Version:** | 1.0 |

| Revision History Date | Version | Remarks |
|---|---|---|
| 13 April 2015 | V1.0 | Initial Release: Preliminary Version |
| 28 Sept 2015 | V1.1 | Correct figure 3 and figure 4 in section 2.3.2 (positive and negative USB signals where swapped in schematics) |
| 22 October 2015 | V1.2 | Corrections in figure 4 in section 2.3.2 (pull up resistor of USB_OC# and pull down of USBH_EN where swapped)<br>Correction in typical pull up value for I2C in section 2.9 |

# 1 Introduction

## 1.1 Overview

This document guides the development of a customized carrier board for the Colibri computer module. It describes the different interfaces and contains reference schematics. This document reflects only the standardized primary function of the Colibri modules. The alternative functions are not guaranteed to be compatible between different Colibri modules. These interfaces are described in the datasheet of each computer module. Some Colibri modules do not feature the full set of standard interfaces. Therefore, it is strongly recommended to read the datasheets of the modules that are intended to be used with the carrier board.

Some of the Colibri computer module interfaces such as High-Speed USB, Ethernet, etc. require special layout considerations regarding trace impedance and length matching. Please carefully read the Toradex Layout Design Guide for additional information related to the routing of these interfaces.

## 1.2 Additional Documents

### 1.2.1 Layout Design Guide

This document contains layout requirement specifications for the high-speed signals and helps in avoiding problems related to the layout.

http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

### 1.2.2 Colibri Module Datasheets

There is a datasheet available for every Colibri module. Amongst other things, this document describes the type-specific interfaces and the alternative function of the pins. Before starting the development of a customized carrier board, please check this document to find out whether the required interfaces are really available on the selected modules.

https://www.toradex.com/products/apalis-arm-computer-modules

### 1.2.3 Toradex Developer Centre

You can find a lot of additional information at the Toradex Developer Centre, which is updated with the latest product support information on a regular basis.

Please note that the Developer Centre is common for all Toradex products. You should always check to ensure if the information is valid or relevant for the specific Colibri modules.

http://www.developer.toradex.com

### 1.2.4 Colibri Evaluation Board Schematics

We provide the complete schematics plus the Altium project file for the Colibri Evaluation Board for free. This is a great help when designing your own Carrier Board.

http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

### 1.2.5 Pinout Designer

This is an interactive and useful tool for configuring the pin muxing of the Colibri and Apalis modules. It can be really helpful in custom carrier board development on Toradex modules and for checking the compatibility of existing carrier boards with our modules.

http://developer.toradex.com/knowledge-base/pinout-designer

## 1.3 Abbreviations

| Abbreviation | Explanation |
|---|---|
| ADC | Analogue to Digital Converter |
| AGND | Analogue Ground - separate ground for analogue signals |
| Auto-MDIX | Automatically Medium Dependent Interface Crossing - a PHY with Auto-MDIX f is able to detect whether RX and TX need to be crossed (MDI or MDIX) |
| CAD | Computer-Aided Design - in this document is referred to PCB Layout tools |
| CAN | Controller Area Network - a bus that is manly used in automotive and industrial environment |
| CDMA | Code Division Multiplex Access - abbreviation often used for a mobile phone standard for data communication |
| CEC | Consumer Electronic Control - HDMI feature that allows to control CEC compatible devices |
| CPU | Central Processor Unit |
| CSI | Camera Serial Interface |
| DAC | Digital to Analogue Converter |
| DDC | Display Data Channel - interface for reading out the capability of a monitor, in this document DDC2B (based on $I^2C$) is always meant |
| DRC | Design Rule Check - a tool for checking whether all design rules are satisfied in a CAD tool |
| DSI | Display Serial Interface |
| DVI | Digital Visual Interface - digital signals are electrical compatible with HDMI |
| DVI-A | Digital Visual Interface Analogue only - signals are compatible with VGA |
| DVI-D | Digital Visual Interface Digital only - signals are electrical compatible with HDMI |
| DVI-I | Digital Visual Interface Integrated - combines digital and analogue video signals in one connector |
| EDA | Electronic Design Automation - software for schematic capture and PCB layout (CAD or ECAD) |
| EDID | Extended Display Identification Data - timing setting information provided by the display in a PROM |
| EMI | Electromagnetic Interference - high frequency disturbances |
| eMMC | Embedded Multi Media Card - flash memory combined with MMC interface controller in a BGA package, used as internal flash memory |
| ESD | Electrostatic Discharge - high voltage spike or spark that can damage electrostatic- sensitive devices |
| FPD-Link | Flat Panel Display Link - high-speed serial interface for liquid crystal displays. In this document also called LVDS interface. |
| GBE | Gigabit Ethernet - Ethernet interface with a maximum data rate of 1000Mbit/s |
| GND | Ground |
| GPIO | General Purpose Input/Output pin that can be configured to be either an input or output |
| GSM | Global System for Mobile Communications |
| HDA | High Definition Audio (HD Audio) - digital audio interface between CPU and audio codec |
| HDCP | High-Bandwidth Digital content Protection - copy protection system that is used by HDMI beside others |
| HDMI | High-Definition Multimedia Interface - combines audio and video signal for connecting monitors, TV sets or Projectors, electrical compatible with DVI-D |
| $I^2C$ | Inter-Integrated Circuit - two wire interface for connecting low speed peripherals |
| $I^2S$ | Integrated Interchip Sound - serial bus for connecting PCM audio data between two devices |
| IrDA | Infrared Data Association - infrared interface for connecting peripherals |
| JTAG | Joint Test Action Group - widely used debug interface |
| LCD | Liquid Crystal Display |
| LSB | Least Significant Bit |
| LVDS | Low-Voltage Differential Signaling - electrical interface standard that can transport very high-speed signals over twisted-pair cables. Many standard interfaces like PCIe or SATA use this interface standard. |

| Abbreviation | Explanation |
|---|---|
| | Since the first successful application was the Flat Panel Display Link, LVDS has become synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface. |
| MIPI | Mobile Industry Processor Interface Alliance |
| MDI | Medium Dependent Interface - physical interface between Ethernet PHY and cable connector |
| MDIX | Medium Dependent Interface Crossed - an MDI interface with crossed RX and TX interfaces |
| mini PCIe | PCI Express Mini Card - card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity |
| MMC | MultiMediaCard - flash memory card |
| MSB | Most Significant Bit |
| mSATA | Mini-SATA - a standardized form factor for small solid state drive, similar dimensions as mini PCIe |
| N/A | Not Available |
| N/C | Not Connected |
| OD | Open Drain |
| OTG | USB On-The-Go - a USB host interface that can also act as USB client when connected to another host interface |
| OWR | One Wire (1-Wire) - low speed interface which needs just one data wire plus ground |
| PCB | Printed Circuit Board |
| PCI | Peripheral Component Interconnect - parallel computer expansion bus for connecting peripherals |
| PCIe | PCI Express - high-speed serial computer expansion bus, replaces the PCI bus |
| PCM | Pulse-Code Modulation - digital representation of analogue signals and a standard interface for digital audio |
| PD | Pull Down Resistor |
| PHY | Physical Layer of the OSI model |
| PMIC | Power Management IC - integrated circuit that manages amongst others the power sequence of a system |
| PU | Pull-up Resistor |
| PWM | Pulse-Width Modulation |
| RGB | Red Green Blue - color channels in common display interfaces |
| RJ45 | Registered Jack - common name for the 8P8C modular connector that is used for Ethernet wiring |
| RS232 | Single ended serial port interface |
| RS422 | Differential signaling serial port interface - full duplex |
| RS485 | Differential signaling serial port interface - half duplex, multi drop configuration possible |
| R-UIM | Removable User Identity Module - identifications card for CDMA phones and networks, an extension of the GSM SIM card |
| S/PDIF | Sony/Philips Digital Interconnect Format - optical or coaxial interface for audio signals |
| SATA | Serial ATA, high-speed differential signaling interface for hard drives and SSD |
| SD | Secure Digital - flash memory card |
| SDIO | Secure Digital Input Output - an external bus for peripherals that uses the SD interface |
| SIM | Subscriber Identification Module - identification card for GSM phones |
| SMBus | System Management Bus (SMB) - two wire bus based on the $I^2C$ specifications, used specially in x86 design for system management. |
| SoC | System on a Chip - IC which integrates the main component of a computer on a single chip |
| SO-DIMM | Small Outline Dual Inline Memory Module - form factor for mobile RAM modules, the Colibri module uses the SO-DIMM (DDR, 2.5V variant) connector as main interface |
| SPI | Serial Peripheral Interface Bus - synchronous four wire full duplex bus for peripherals |
| TIM | Thermal Interface Material - thermal conductive material between CPU and heat spreader or heat sink |
| TMDS | Transition-Minimized Differential Signaling - serial high-speed transmitting technology that is used by DVI and HDMI |
| TVS Diode | Transient-Voltage-Suppression Diode - diode that is used to protect interfaces against voltage spikes |
| UART | Universal Asynchronous Receiver/Transmitter - serial interface, in combination with a transceiver a RS232, RS422, RS485, IrDA or similar interface can be achieved |
| USB | Universal Serial Bus - serial interface for internal and external peripherals |
| VCC | Positive supply voltage |
| VGA | Video Graphics Array - analogue video interface for monitors |

Table 1: Abbreviations

# 2 Interfaces

## 2.1 Architecture

### 2.1.1 Standard Interfaces

The standard interfaces on the Colibri module family intent to provide electrical and functional compatibility between module family members. The table below shows an overview of the standard interfaces that are provided by a Colibri module. The "GPIO Capable" column indicates whether the assigned pins are intent to be also used as GPIOs. "Yes" and "No" are self-Explanatory. "Optional" indicates that it may be possible for some modules, but not all.

The "Standard" column indicates the number of interfaces that the specification allows for in the standard pin-out. Customers should consult the datasheet for specific Colibri module variants to check which of the interfaces are available for that module.

| Description | Standard | Note | GPIO Capable |
|---|---|---|---|
| 4/5 Wire Resistive Touch | 1 | Touch wiper shared with analogue input 4 | No |
| Analogue Inputs | 4 | Minimum 8 bit resolution, 0-3.3V nominal range | No |
| Analogue Audio | 1 | Line in L&R, Microphone in, Headphone out L&R | No |
| Fast Ethernet | 1 | | No |
| HDMI (TDMS) | 1 | Located on dedicated FFC connector (availability depending on Module) | No |
| I2C | 1 | Additional dedicated DDC available on FFC connector | Yes |
| Parallel Camera | 1 | 8 bit BT.656 (other modes may available) | Yes |
| Parallel LCD | 1 | 18 bit resolution (additional bits may available) | Yes |
| Parallel Memory Bus | 1 | Supported bus width depends on Module | Optional |
| PWM | 4 | | Yes |
| SDIO | 1 | 4 bit | Yes |
| SPI | 1 | | Yes |
| UART | 3 | 1x Full Featured, 1x CTS/RTS, 1x RXD/TXD only | Yes |
| USB | 2 | 1x shared host/client, 1x host only | No |
| VGA | 1 | Located on dedicated FFC connector (availability depending on Module) | No |

Table 2: Standard Interfaces

### 2.1.2 Interfaces on Alternative Functions

Many SoC pins can be used for more than one function. This allows the modules provide many additional interfaces to the standard set. For example, in the Colibri standard there is only one SPI interface listed. Nevertheless, some modules can provide up to 6 SPI interfaces.

Please note that there are a few restrictions of using the interfaces that are provided as alternative functions of the pins. There is limited compatibility between their availability at different modules. For a design to be compatible with a wide range of Colibri modules, it is recommended to mainly use the standard interfaces. The various pins can be used for only one function each simultaneously.

The configuration of the alternative function interfaces can be quite complex. Toradex provides a powerful tool which helps the development engineer to resolve pin muxing conflicts. The tool is called Pinout Designer. It reduces the complexity of this important task. More information including its download link can be found here: http://developer.toradex.com/knowledge-base/pinout-designer.

The interfaces on the alternative functions are not described in this document since they differ between the modules. Information related to these functions can be found in the datasheets of the modules.

### 2.1.3 Pin Numbering

The diagrams in the figures below show the pin numbering schema on both sides of the module. The schema is equals to the JEDEC MO-224 DDR SO-DIMM standard. The even pin numbers are located on the top side of the module.

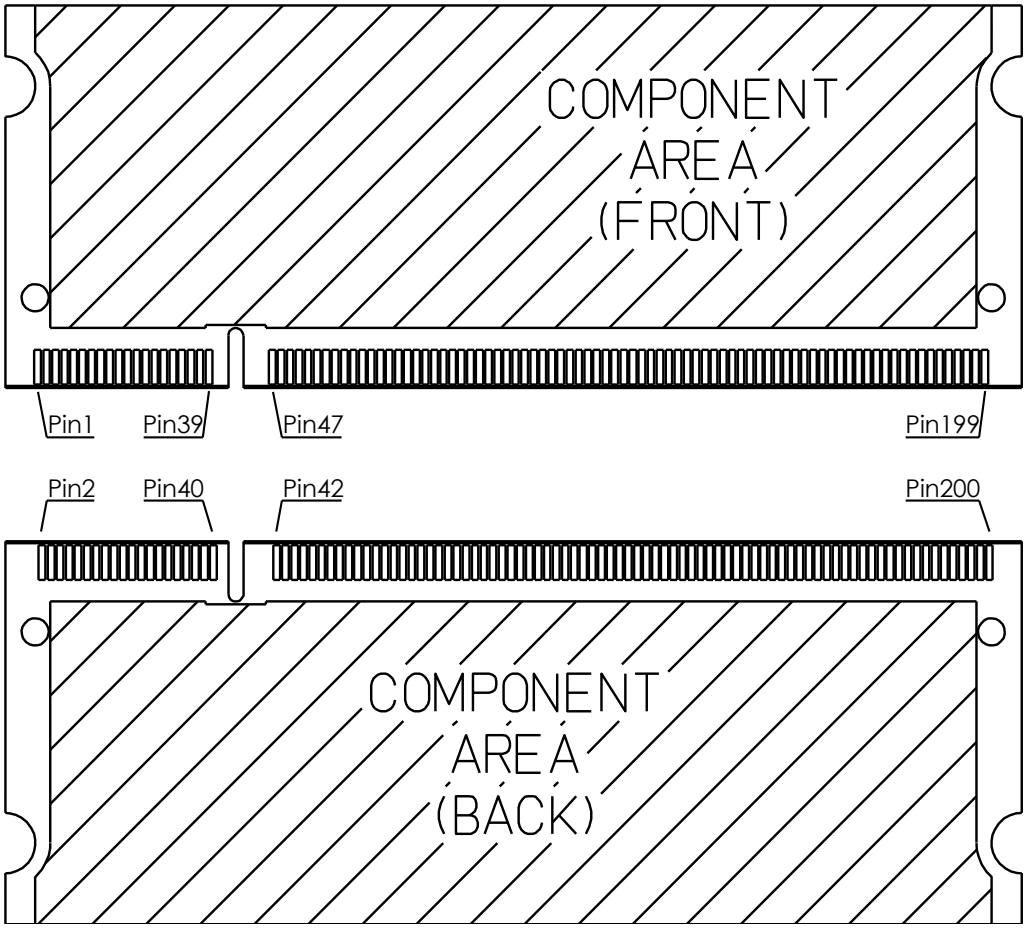


Figure 1: Colibri Module Pin Numbering Schema

## 2.2 Ethernet

The Colibri module standard features a fast 10/100Mbit Ethernet (10/100Base-TX) interface port. The required center tap circuit can differ between the modules. Different assembly options might be needed for supporting the complete Colibri module family. Some modules support Auto MDIX, which means they can swap the transmitting with the receiving lanes. Read the corresponding datasheet of the module for more information about the availability of the Auto MDIX function.

### 2.2.1 Ethernet Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 189 | ETH_1_TXO+ | I | Analogue | | 100BASE-TX: Transmit + (Auto MDIX: Receive +) |
| 187 | ETH_1_TXO- | I | Analogue | | 100BASE-TX: Transmit - (Auto MDIX: Receive -) |
| 195 | ETH_1_RXI+ | O | Analogue | | 100BASE-TX: Receive + (Auto MDIX: Transmit +) |
| 193 | ETH_1_RXI- | O | Analogue | | 100BASE-TX: Receive - (Auto MDIX: Transmit -) |
| 191 | AGND_LAN | | | | Ethernet ground, on some modules connected to common GND |
| 183 | ETH_1_LINK_AKT | O | CMOS | 3.3V | LED indication output for link activity on the Ethernet port |
| 185 | ETH_1_SPEED100 | O | CMOS | 3.3V | LED indication output for 100Mbit/s |

Table 3: Ethernet Signals

### 2.2.2 Reference Schematics

Ethernet connectors with integrated magnetics are preferable. If a design with external magnetics is chosen, additional care has to be taken to route the signals between the magnetics and Ethernet connector.

The LED output signals ETH_1_LINK_AKT and ETH_1_SPEED100 can be connected directly to the LED of the Ethernet jack with suitable serial resistors. There is no need for additional buffering if the current drawn does not exceeds 10mA.

The Fast Ethernet interface uses the ETH_1_TXO as transmitting lanes and the ETH_1_RXI as receiving lane. If the Ethernet PHY features Auto-MDIX, the signal lanes RX and TX could be swapped. We strongly recommend not swapping the RX and TX lanes in order to keep the compatibility with all Colibri modules.

The required center tap circuit depends on the supported modules. Currently, the Ethernet controller on the PXA270 module is the only one which requires a different center tap circuit since it does not support Auto-MDIX. All the other currently available modules feature a current control PHY which requires 3.3V supply at the center tap of the RX and TX lanes. Since all the Ethernet PHY manufacturer are tending to change from current mode to voltage mode which requires leaving the center tab pins of the magnetics unconnected, we recommend to add additional 0R resistors into the center tab lines. This ensures that the carrier board design is ready for any future Colibri module with voltage mode PHY.

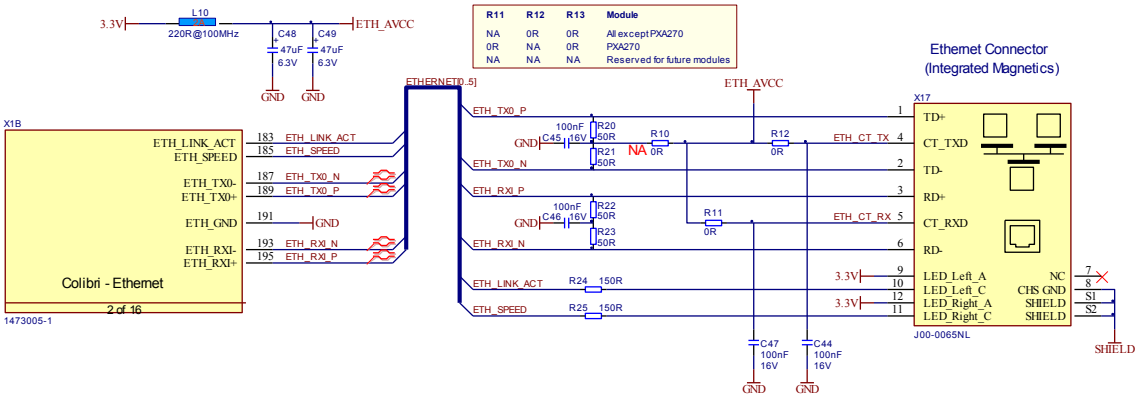


Figure 2: Fast Ethernet with Integrated Magnetics Reference Schematic

### 2.2.3 Unused Ethernet Signals Termination

All unused Ethernet signals can be left unconnected.

## 2.3 USB

The Colibri modules feature two USB interfaces. One of the two USB interfaces can be configured to be used as either the host or client. The other interface can only be used as host. Some of the Colibri modules use the USB client port for debugging and recovery purpose. Therefore, it is recommended to have the interface accessible even for carrier board designs which do not need any USB ports.

### 2.3.1 USB Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 139 | USB_H_DP | I/O | USB | 3.3V | Positive Differential Signal for USB Host port |
| 141 | USB_H_DM | I/O | USB | 3.3V | Negative Differential Signal for USB Host port |
| 143 | USB_C_DP | I/O | USB | 3.3V | Positive Differential Signal for the shared USB Host / Client port |
| 145 | USB_C_DM | I/O | USB | 3.3V | Negative Differential Signal for the shared USB Host / Client port |

Table 4: USB Data Signals

If you use the USB Host function you need to generate the 5V USB supply voltage on your carrier board. The Colibri modules provide two optional signals for USB power supply control (PWR_EN and OC). We recommend using the following pins to ensure the best possible compatibility. However, use of these signals is not mandatory and other GPIOs may be used instead.

In the USB client mode, an additional signal is required that detects whether the client is connected to a host interface (VBUS_DETECT). Please note that this pin is only 3.3V tolerant. Therefore, an additional logic level shifter (simplest solution is a voltage divider) is required.

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 129 | USB_H_PWR_EN | O | CMOS | 3.3V | This pin enables the external USB voltage supply |
| 131 | USB_H_OC | I | CMOS | 3.3V | USB overcurrent, this pin can signal an over current condition in the USB supply |
| 137 | USB_C_VBUS_DETECT | I | CMOS | 3.3V | Use this pin to detect if VBUS is present (5V USB supply). Please note that this pin is only 3.3V tolerant |

Table 5: USB Control Signals

### 2.3.2 Reference Schematics

#### 2.3.2.1 USB 2.0 Client Schematic Example

The differential USB data signals require a common mode choke to be placed. Make sure that the selected choke is certified for USB 2.0 High Speed. The same is also required for the TVS diodes. The VBUS_DETECT signal is only 3.3V tolerant on the Colibri module. The simplest solution is to use a voltage divider.

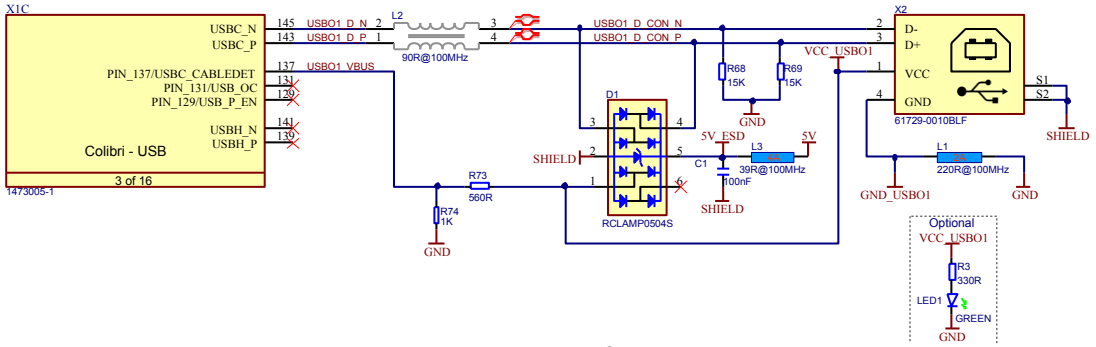


Figure 3: USB 2.0 Client Reference Schematic

#### 2.3.2.2 USB 2.0 Host Connector Schematic Example

The carrier board needs to provide 5V USB bus power on the USB host jacks. According to the USB 2.0 specifications, the maximum current drawn per port is limited by 500mA. The bus power needs to be in the range of 4.75V to 5.25V measured at the USB host jack for any load current from 0mA to 500mA. In order to ensure that an out of spec device or a defective device is not damaging the 5V power rail on the carrier board, it is recommended adding a current limiting IC. This device detects overcurrent situation and switches off the corresponding USB bus power. The overcurrent signal (USB_H_OC) is used to notify the host controller about the occurrence of an overcurrent shut down event.

The inrush current needs to be taken into account while designing the USB bus power. USB devices are allowed to have a maximum input capacitor at the bus power of 10µF. The maximum inrush charge is limited to 50µC. This means that the power rail at the USB host jack needs to be tolerant of this inrush current. A good approach is to place a large capacitor (e.g. 100µF) at the rail.

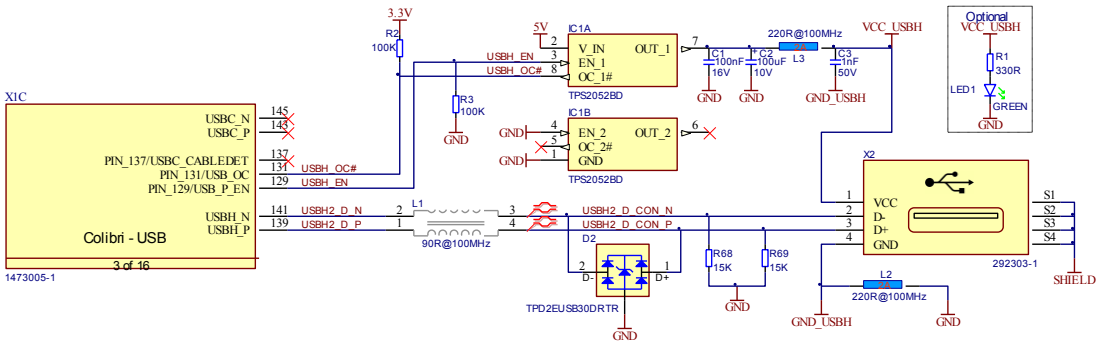


Figure 4: USB 2.0 Host Reference Schematic

### 2.3.3 Unused USB Signal Termination

| Colibri Pin | Colibri Signal Name | Recommended Termination |
|---|---|---|
| 139 | USB_H_DP | Leave NC if not used |
| 141 | USB_H_DM | Leave NC if not used |
| 143 | USB_C_DP | Leave NC if not used |
| 145 | USB_C_DM | Leave NC if not used |
| 129 | USB_H_PWR_EN | Leave NC if not used |
| 131 | USB_H_OC | Add pull-up resistor or disable the overcurrent function in software |
| 137 | USB_C_VBUS_DETECT | Leave NC if not used |

Table 6: Unused USB Signals Termination

## 2.4 Parallel RGB LCD Interface

The Colibri modules feature one parallel RGB LCD interface as main display interface. As standard, the Colibri modules feature the interface with 18-bit color depth. Some modules support color depth of 16-bit or 24-bit. Unfortunately, the color mapping of these modes can be different between the modules. Therefore, Toradex recommends using the interface in the 18-bit color mode for the best compatibility between all Colibri modules. Dithering can help reducing the visible color banding of gradients in lower color depth systems. Consider using 18-bit color mapping with enabled dithering instead of 24-bit mapping. Carefully check which modules support color dithering.

### 2.4.1 Parallel RGB LCD Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 52 | LCD_1_18bit_R0 | O | CMOS | 3.3V | Red LCD data signals (LSB: 0, MSB: 5) |
| 54 | LCD_1_18bit_R1 | O | CMOS | 3.3V | |
| 66 | LCD_1_18bit_R2 | O | CMOS | 3.3V | |
| 64 | LCD_1_18bit_R3 | O | CMOS | 3.3V | |
| 57 | LCD_1_18bit_R4 | O | CMOS | 3.3V | |
| 61 | LCD_1_18bit_R5 | O | CMOS | 3.3V | |
| 80 | LCD_1_18bit_G0 | O | CMOS | 3.3V | Green LCD data signals (LSB: 0, MSB: 5) |
| 46 | LCD_1_18bit_G1 | O | CMOS | 3.3V | |
| 62 | LCD_1_18bit_G2 | O | CMOS | 3.3V | |
| 48 | LCD_1_18bit_G3 | O | CMOS | 3.3V | |
| 74 | LCD_1_18bit_G4 | O | CMOS | 3.3V | |
| 50 | LCD_1_18bit_G5 | O | CMOS | 3.3V | |
| 76 | LCD_1_18bit_B0 | O | CMOS | 3.3V | Blue LCD data signals (LSB: 0, MSB: 5) |
| 70 | LCD_1_18bit_B1 | O | CMOS | 3.3V | |
| 60 | LCD_1_18bit_B2 | O | CMOS | 3.3V | |
| 58 | LCD_1_18bit_B3 | O | CMOS | 3.3V | |
| 78 | LCD_1_18bit_B4 | O | CMOS | 3.3V | |
| 72 | LCD_1_18bit_B5 | O | CMOS | 3.3V | |
| 44 | LCD_1_18bit_DE | O | CMOS | 3.3V | Data Enable (other names: Output Enable) |
| 56 | LCD_1_18bit_PCLK | O | CMOS | 3.3V | Pixel Clock (other names: Dot Clock, L_PCLK_WR) |
| 68 | LCD_1_18bit_HSYNC | O | CMOS | 3.3V | Horizontal Sync (other names: Line Clock, L_LCKL_A0) |
| 82 | LCD_1_18bit_VSYNC | O | CMOS | 3.3V | Vertical Sync (other names: Frame Clock, L_FCLK) |

Table 7: Parallel RGB LCD Signals

### 2.4.2 Reference Schematics

#### 2.4.2.1 18-bit Display Schematic Example

The parallel RGB interface can cause problems in passing the electromagnetic radiation tests when used with high pixel clocks frequency. Especially if a display is connected over long flat flex cables. The reduction of the radiation needs to be taken in account. Keep the flat flex cables as short as possible. Series resistors in the data lines reduce the slew rate of the signals which reduces the radiation problem but can introduce signal quality and timing problems. The serial resistor value is a trade-off between electromagnetic radiation reduction and signal quality. A good starting value is 22Ω.

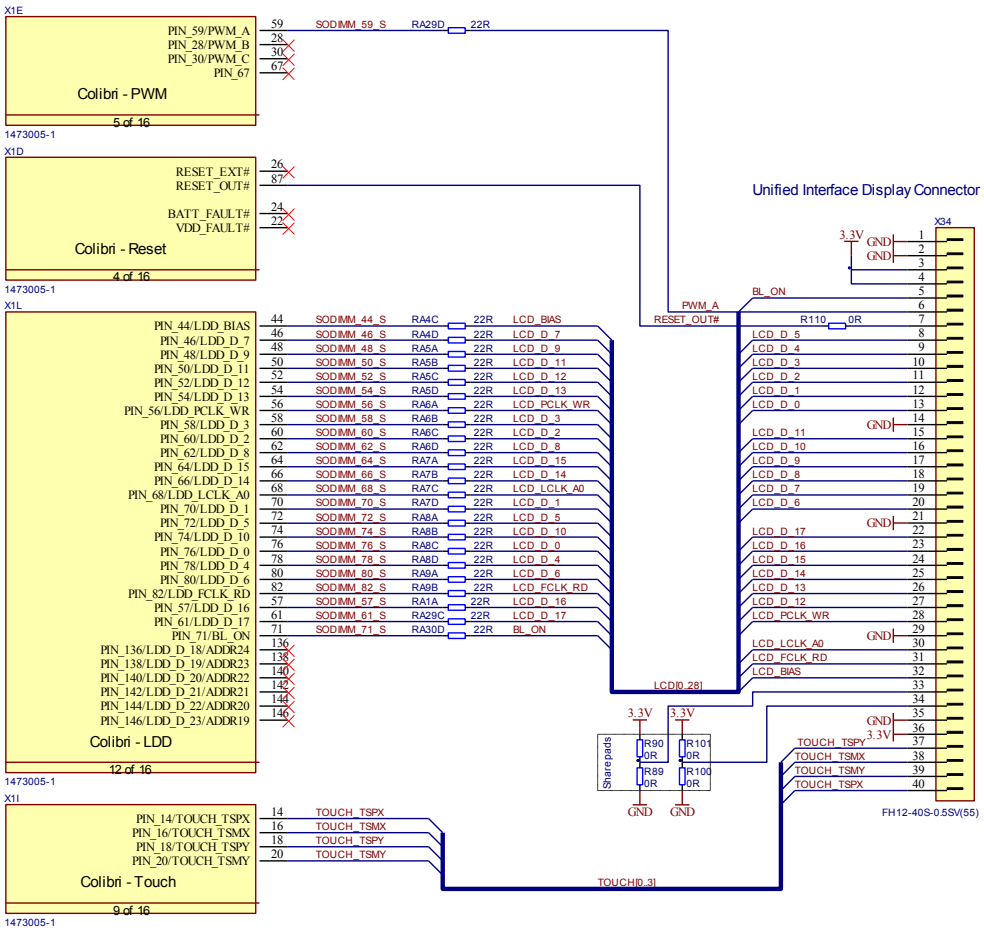


Figure 5: 18bit Parallel RGB Display Reference Schematic

#### 2.4.2.2 VGA DAC Schematic Example

A few Colibri modules feature a dedicated VGA interface on an FFC connector. Nevertheless, it is recommended adding a parallel RGB to VGA converter if a VGA interface is needed which is compatible with all modules. Since only the 18-bit color depth is compatible between the different modules, it is recommended to use this mode even if the DAC is capable of 24-bit.

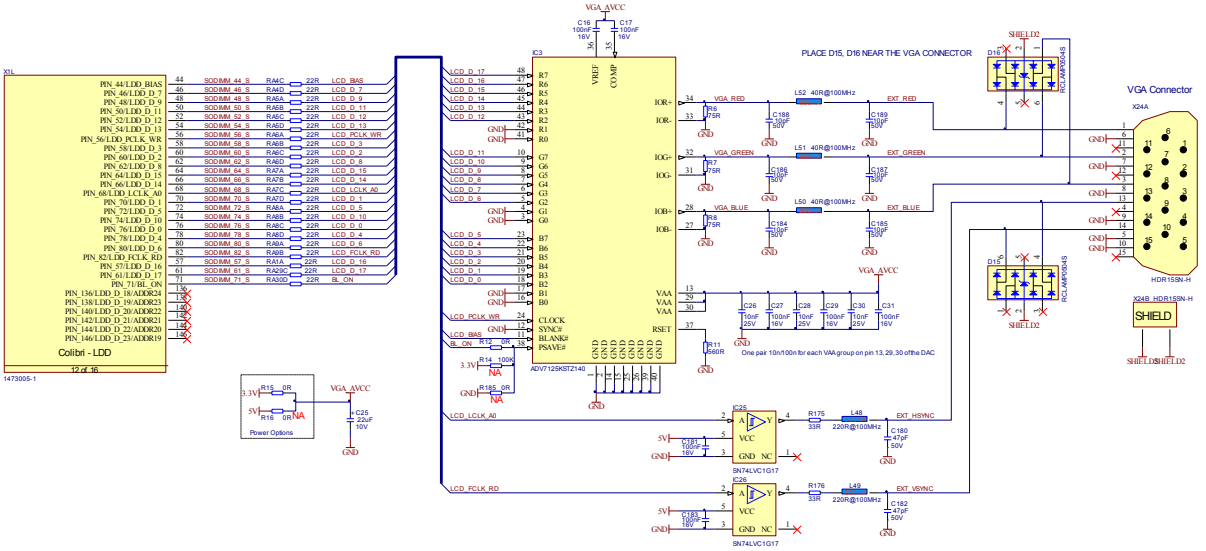

Figure 6: VGA DAC Reference Schematic

### 2.4.2.3 LVDS Transmitter Schematic Example

Since the electromagnetic radiation of the parallel RGB interface is not easy to handle, it is recommended to attach liquid crystal displays with high resolutions by using an LVDS interface. LVDS also reduces problems associated with long cables. The Colibri standard does not feature a dedicated LVDS LCD interface. Nevertheless, a parallel RGB to LVDS transmitter can be placed on the carrier board in order to get an LVDS interface.

Since there are different LVDS color mapping available, check with your display vendor how the RGB signals need to be connected to the transmitter in order to be compatible.

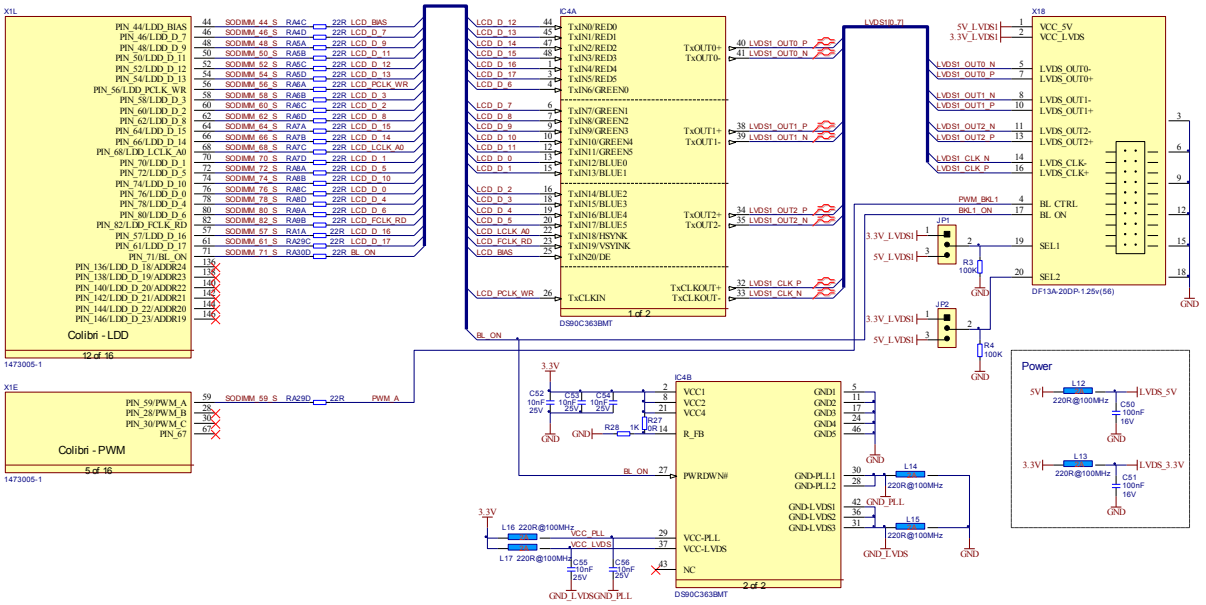

Figure 7: LVDS Transmitter Reference Schematic

### 18-bit Color Mapping

The color mapping for the 18-bit LVDS interface is standardized and is shown in the following picture:

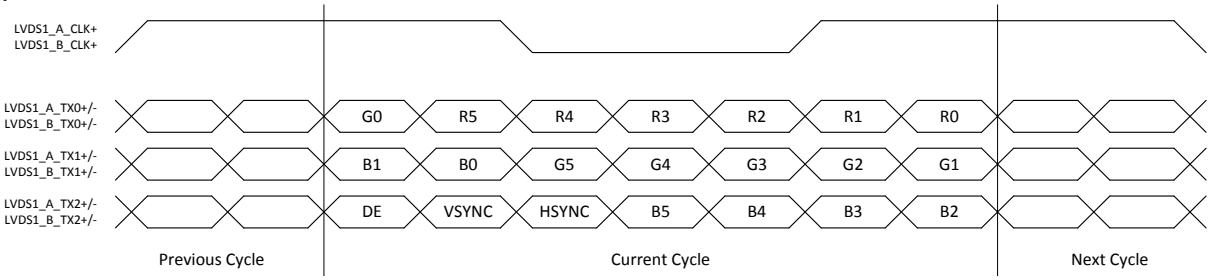


Figure 8: 18-bit LVDS Color Mapping

### 24-bit JEIDA Color Mapping

The JEIDA color mapping is compatible with the 18bit LVDS interface. Therefore, the mapping is sometimes also called "24bit / 18bit Compatible Color Mapping". The signal names of the color bits are renamed (e.g. the 18bit R5 is renamed to 24bit R7) but the position of the MSB is kept the same. The additional least significant bits R0, R1, G0, G1, B0 and B1 are located at the additional fourth LVDS data pair.

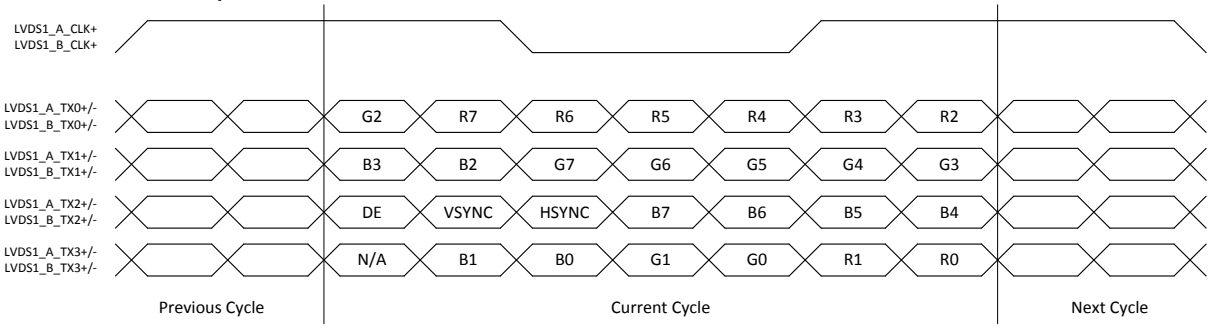


Figure 9: 24-bit JEIDA LVDS Color Mapping

### 24-bit VESA Color Mapping

Most of the 24bit LVDS displays follow the VESA Color mapping. The VESA color mapping does not rename the signal bits. This means that the position of the MSB is changed since they are available at the additional data pair. Therefore, the VESA color mapping is not compatible with the 18bit interface.

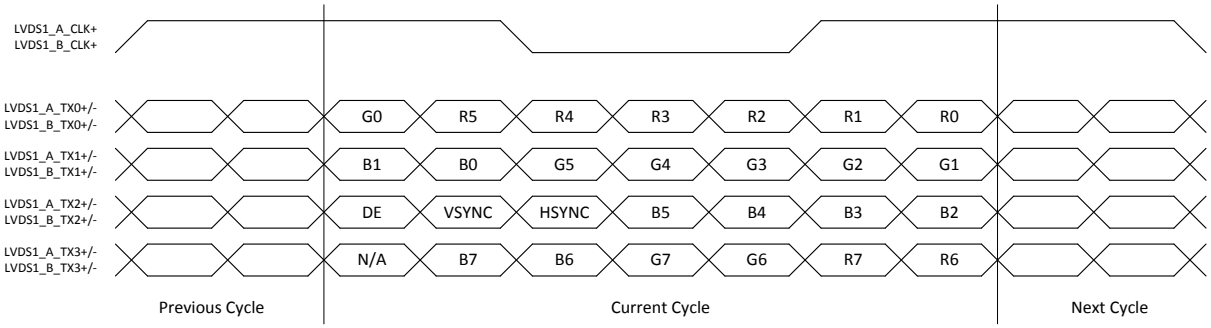


Figure 10: 24-bit VESA LVDS Color Mapping

## 2.4.3 Unused Parallel RGB Interface Signal Termination

All unused parallel RGB interface signals can be left unconnected.

## 2.5 HDMI/DVI

The HDMI and DVI interface uses a TMDS compatible physical link to transfer video and optional audio data. While electrically, HDMI and DVI are both similar, but there can be a few differences in their protocols. HDMI is the successor of DVI and specifies the additional transport for audio data and content protection (HDCP). As HDMI is backward compatible, HDMI devices (monitor, television set etc.) work with DVI signals. Forward compatibility is not guaranteed. Not all DVI displays accept the HDMI protocol or are HDCP compatible. Please read the datasheet of the Colibri modules for more information about the provided HDMI and DVI protocols.

The HDMI and DVI interface define different connectors. There are passive adapters available in both types. Please be advised that both HDMI and HDCP require to be licensed. The HDMI/DVI signals are available on a dedicated FFC connector. Check carefully to confirm which modules provide the interface.

### 2.5.1 HDMI/DVI Signals

| Colibri FFC Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 2 | HDMI_1_CLK_P | O | TDMS | | HDMI/DVI differential clock positive |
| 3 | HDMI_1_CLK_N | O | TDMS | | HDMI/DVI differential clock negative |
| 5 | HDMI_1_DATA0_P | O | TDMS | | HDMI/DVI differential data lane 0 positive |
| 6 | HDMI_1_DATA0_N | O | TDMS | | HDMI/DVI differential data lane 0 negative |
| 8 | HDMI_1_DATA1_P | O | TDMS | | HDMI/DVI differential data lane 1 positive |
| 9 | HDMI_1_DATA1_N | O | TDMS | | HDMI/DVI differential data lane 1 negative |
| 11 | HDMI_1_DATA2_P | O | TDMS | | HDMI/DVI differential data lane 2 positive |
| 12 | HDMI_1_DATA2_N | O | TDMS | | HDMI/DVI differential data lane 2 negative |
| 14 | HDMI_1_HPD | I | CMOS | 3.3V | Hot plug detect |
| 16 | HDMI_DDC_SDA | I/O | OD | 3.3V | $I^2C$ interface for reading the extended display identification data (EDID) over DDC. |
| 15 | HDMI_DDC_SCL | O | OD | 3.3V | |

Table 8: HDMI/DVI Signals

### 2.5.2 Reference Schematics

#### 2.5.2.1 DVI Schematic Example

There are different configurations of DVI connectors available. The DVI-D (digital) contains only the native DVI signals The DVI-A (analogue) provides no DVI signals. Only the analogue VGA signals are provided. The DVI-I (integrated) combines the digital DVI signals and the analogue VGA signals. For the DVI-A and DVI-I, there are passive adapters available for the D-SUB VGA connector. There is only one DDC channel available on the DVI-I interface. Therefore, the connector is not designed to use both links (DVI and VGA) contemporaneously. Nevertheless, there are Y-cables available which provides a DVI and VGA output contemporaneously. Such cables are not standardized and provide normally the DDC only on the DVI or VGA output. Please be aware of the DDC when using such a Y-cable.

The following schematic example shows a DVI-I implementation. It can also be used as an example for a DVI-D design, just remove the analogue VGA signals. The sync signals for the VGA signals need to be level shifted from 3.3V to 5V. The same is necessary for the DDC signals. The TDMS signals need to be ESD protected by using diodes. The schematic example shows a discrete solution for the level shifting and protection. There are also integrated solutions available.

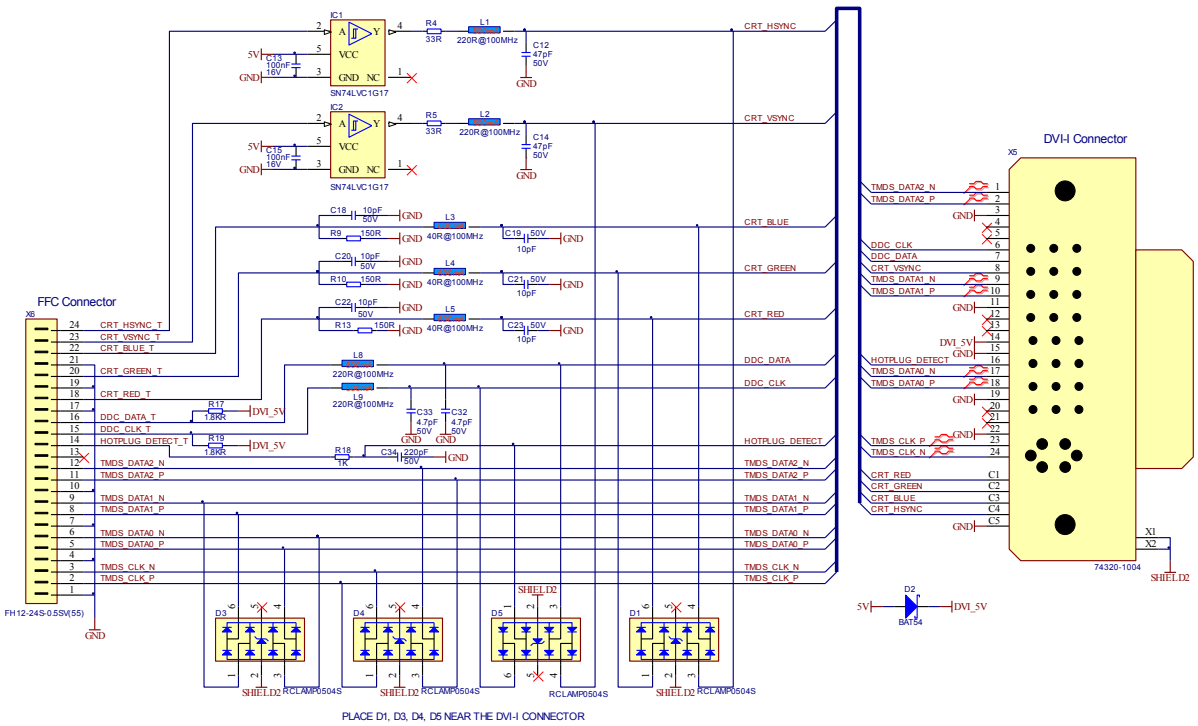


Figure 11: DVI-I Reference Schematic

### 2.5.2.2 HDMI Schematic Example

The HDMI connector does not feature an Analogue VGA interface, but there is an optional Consumer Electronics Control (CEC) interface available on the connector. The location of the CEC signal is not standardized on the Colibri modules. Check the datasheet of the modules for more information to the position of the signal. The CEC is a single- wire interface that is used to control consumer audio and video devices such as television set or AV receivers. There are many different trade names for CEC (VIERA Link, Anynet+, EasyLink, Aquos Link, BRAVIA Link, etc.). The CEC is a 3.3V interface. Nevertheless, it is recommended to add level shifter from the internal 3.3V logic level. This eliminates problems with displays that pull-up the signal to other voltage levels.

The $I^2C$ signals for the DDC and the hot plug detection (HPD) need to be shifted to/from the 5V logic level of the HDMI to the Colibri level of 3.3V. The HPD has a 100kΩ pull down resistor already on the baseboard

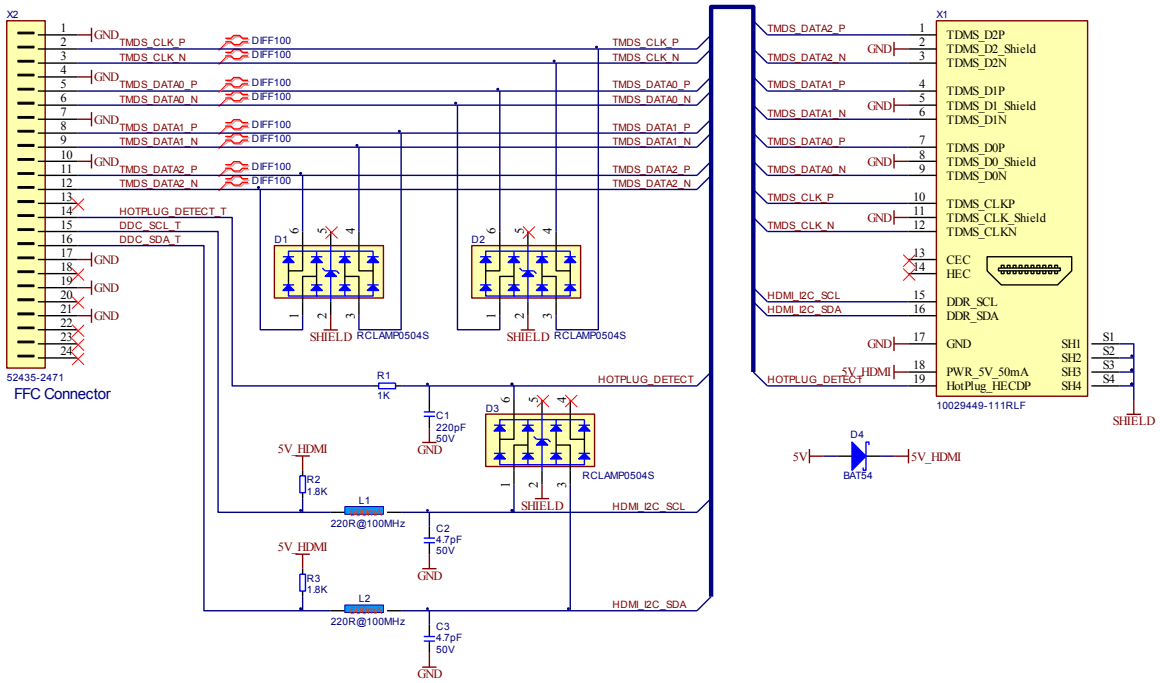


Figure 12: HDMI Reference Schematic

### 2.5.3 Unused HDMI/DVI Signal Termination

All unused HDMI/DVI signals can be left unconnected. The HPD has a 100kΩ pull down resistor on the module.

| Colibri Pin | Colibri Signal Name | Recommended Termination |
|---|---|---|
| 2 | HDMI_1_CLK_P | Leave NC if not used |
| 3 | HDMI_1_CLK_N | Leave NC if not used |
| 5 | HDMI_1_DATA0_P | Leave NC if not used |
| 6 | HDMI_1_DATA0_N | Leave NC if not used |
| 8 | HDMI_1_DATA1_P | Leave NC if not used |
| 9 | HDMI_1_DATA1_N | Leave NC if not used |
| 11 | HDMI_1_DATA2_P | Leave NC if not used |
| 12 | HDMI_1_DATA2_N | Leave NC if not used |
| 14 | HDMI_1_HPD | Leave NC if not used, 100kΩ resistor on Colibri module |
| 16 | HDMI_DDC_SDA | Add pull-up resistor or disable the $I^2C$ function in software |
| 15 | HDMI_DDC_SCL | Add pull-up resistor or disable the $I^2C$ function in software |

Table 9: Unused HDMI/DVI Signals Termination

## 2.6 Analogue VGA

Some Colibri modules feature a dedicated VGA interface on the HDMI FFC connector. For systems which need to be compatible with a wide range of Colibri modules, it is recommended to use a parallel RGB to VGA DAC instead of the dedicated VGA interface.

### 2.6.1 VGA Signals

| Colibri FFC Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 18 | VGA_1_R | O | Analogue | | Analogue red video (0 to 0.7V) |
| 20 | VGA_1_G | O | Analogue | | Analogue green video (0 to 0.7V) |
| 22 | VGA_1_B | O | Analogue | | Analogue blue video (0 to 0.7V) |
| 24 | VGA_1_HSYNC | O | CMOS | 3.3V | Horizontal sync |
| 23 | VGA_1_VSYNC | O | CMOS | 3.3V | Vertical sync |
| 16 | HDMI_DDC_SDA | I/O | OD | 3.3V/ 5V tolerant | $I^2C$ interface for reading the extended display identification data (EDID) over DDC. Signal shared with the HDMI interface |
| 15 | HDMI_DDC_SCL | O | OD | 3.3V/ 5V tolerant | |

Table 10: VGA Signals

### 2.6.2 Reference Schematics

The horizontal and vertical sync signals need to be level shifted on the baseboard. The DDC signals on the FFC connector do not require a level shifter since these signals are 5V tolerant. If a different $I^2C$ interface is used as DDC, the shifters are needed. In the VGA connector standard, the carrier board needs to provide 5V power supply for the EDID memory on the DDC. This allows the system to read out the EDID information of an attached display even if it is not powered. Unfortunately, some displays source the 5V internally and also provide internal pull-up resistors to the $I^2C$ lines. This can cause back feeding problems. Therefore we recommend connecting the display and pull-up resistor 5V supply over a diode to the module supply.

It is mandatory to place on every analogue RGB signal a 150Ω resistor to ground. Place this resistor as close to the VGA connector as possible. Before this resistor, the signal trace can be routed with 50Ω impedance. After the resistor, the signal should be routed with 75Ω impedance. Depending on the layer stack up, 75Ω traces cannot be reached since the trace with is getting too small. In this case, lower traces impedance (e.g. 50Ω) can be used but the trace length should be kept short.

All signals on the VGA D-SUB connector need to be ESD protected. TSR diodes can be used. It is recommended to add a PI-filter to the analogue RGB signals. The values for the capacitors and inductors depend on the maximum required display resolution. The PI-filter reduces EMI problems, but also limits the maximum bandwidth of the VGA signal.

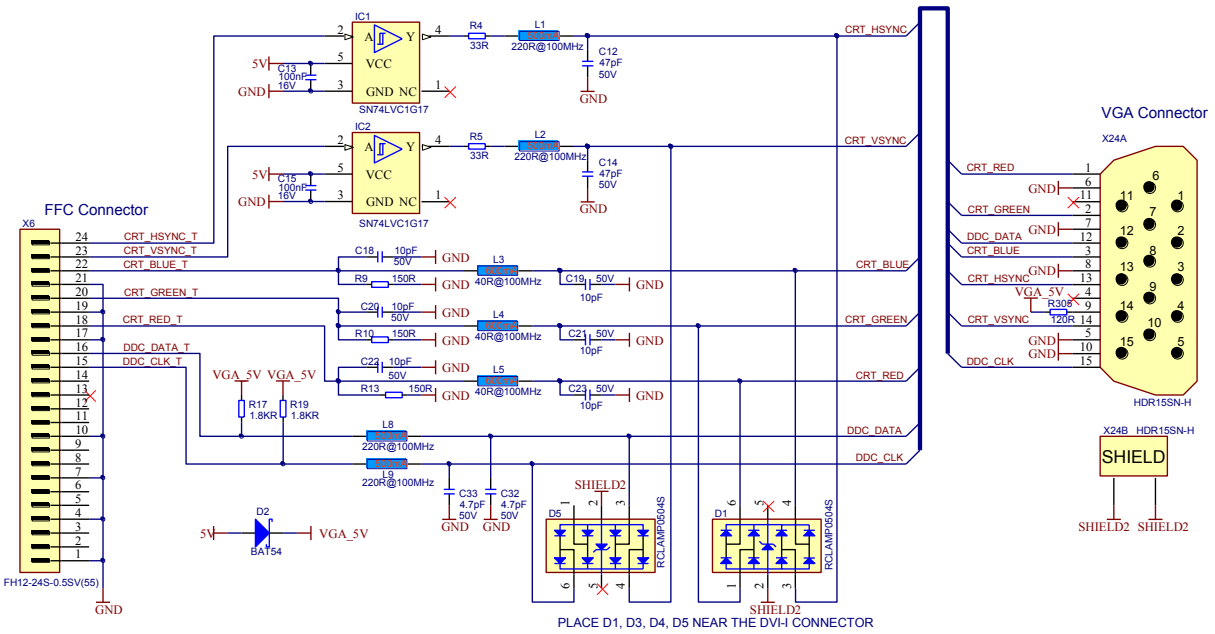


Figure 13: VGA Reference Schematic

### 2.6.3 Unused VGA Interface Signal Termination

All unused VGA interface signals can be left unconnected.

## 2.7 Parallel Camera Interface

The Colibri module form factor features an 8 bit parallel camera interface as a standard interface. Depending on the module, there are maybe additional bits available in the type specific area. Only the 8 bit YUV and ITU-R BT.656 format mode is intent to keep compatible between Colibri modules. Consult the Colibri datasheets in order to get more information about the additional available input modes (e. g. Bayer, RGB etc.)

### 2.7.1 Parallel Camera Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 101 | CAM_1_Y0/C0 | I | CMOS | 3.3V | Video input pixel data |
| 103 | CAM_1_Y1/C1 | I | CMOS | 3.3V | |
| 79 | CAM_1_Y2/C2 | I | CMOS | 3.3V | |
| 97 | CAM_1_Y3/C3 | I | CMOS | 3.3V | |
| 67 | CAM_1_Y4/C4 | I | CMOS | 3.3V | |
| 59 | CAM_1_Y5/C5 | I | CMOS | 3.3V | |
| 85 | CAM_1_Y6/C6 | I | CMOS | 3.3V | |
| 65 | CAM_1_Y7/C7 | I | CMOS | 3.3V | |
| 96 | CAM_1_PCLK | I | CMOS | 3.3V | Video input pixel clock |
| 81 | CAM_1_VSYNC | I | CMOS | 3.3V | Video input vertical sync |
| 94 | CAM_1_HSYNC | I | CMOS | 3.3V | Video input horizontal sync |
| 75 | CAM_1_MCLK | O | CMOS | 3.3V | Master clock output for the camera. Some Camera might do not need this clock since they use other clock sources |

Table 11: Parallel Camera Signals

### 2.7.2 Unused Parallel Camera Interface Signal Termination

All unused parallel camera input signals can be left unconnected if the interface is disabled in software. It depends on the module whether the signals can be used as GPIO when they are not used as camera interface.

## 2.8 SD/MMC/SDIO

The Colibri module form factor features one SD/MMC interfaces as standard interface. The interface provide up to 4 data bit which can be used for interfacing SD and MMC cards as well as SDIO interface peripherals. Depending on the module, there might be additional data signals in order to get an 8bit interface. This bit width is used by MMCplus cards and eMMC memory chips. The additional data bits are not intent to be compatible between different Colibri modules.

The SD cards know different bus speed modes. The required signal voltage depends on the bus speed mode. For example the SDR104 mode requires 1.8V signaling. In the Colibri module definition, all GPIO capable interfaces including the SD/MMC/SDIO are defined for 3.3V. Some Colibri modules might be capable to switch the voltages of the SD card interface pins to a 1.8V, but it is not mandatory. Read the according datasheet of the Colibri module.

Even if the bus speed mode requires the signaling voltage of 1.8V, the supply of the card itself is still 3.3V. Pay attention to the SD card signal pull-up resistors on the carrier board. If the 1.8V mode should be supported by the carrier board, the voltage for the pull-up resistors also needs to be switchable. Some Colibri modules might allow removing the pull-up resistors on the carrier board and using the internal ones only. In this case, this is the preferred solution. Even if the external pull-up resistors are not mandatory, we recommend adding not assembled pull-up resistors to the 3.3V rail in order to be compatible with future modules.

| Bus Speed Mode | Max. Clock Frequency | Max. Bus Speed | Signal Voltage |
|---|---|---|---|
| Default Speed | 25 MHz | 12.5 MByte/s | 3.3V |
| High Speed | 50 MHz | 25 MByte/s | 3.3V |
| SDR12 | 25 MHz | 12.5 MByte/s | 1.8V |
| SDR25 | 50 MHz | 25 MByte/s | 1.8V |
| DDR50 | 50 MHz | 50 MByte/s | 1.8V |
| SDR50 | 100 MHz | 50 MByte/s | 1.8V |
| SDR104 | 208 MHz | 104 MByte/s | 1.8V |

Table 12: SD Card Bus Speed Modes

### 2.8.1 SD/MMC/SDIO Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 192 | SD_1_DATA0 | I/O | CMOS | 3.3V | Data signals [3:0], used for SD, MMC and SDIO interfaces, add external pull-up resistors |
| 49 | SD_1_DATA1 | I/O | CMOS | 3.3V | |
| 51 | SD_1_DATA2 | I/O | CMOS | 3.3V | |
| 53 | SD_1_DATA3 | I/O | CMOS | 3.3V | |
| 190 | SD_1_CMD | I/O | CMOS | 3.3V | Command signal, add external pull-up resistor |
| 47 | SD_1_CLK | O | CMOS | 3.3V | Clock output |

Table 13: 4bit SD/MMC/SDIO Signals

### 2.8.2 Reference Schematics

Even if the selected module does not require pull-up resistors on the data and command lines, it is recommended to place such resistors in the customer design and just not assemble them. This makes sure that the module is compatible with other Colibri modules. There is no dedicated card detect signal available. Any free GPIO capable signal could be used, but we recommend using the signal on Pin 43 (CTRL_WAKE_0) whenever possible. There is also no dedicated write protection signal available on the standard Colibri pin-out. Any free GPIO capable signal can be used if the write protection function is required.

#### 2.8.2.1 SD Card Slot Reference Schematics

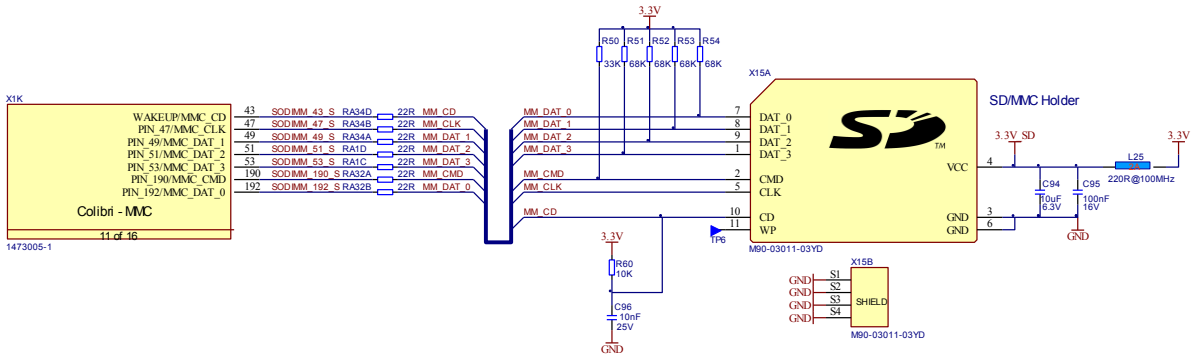


Figure 14: SD Card Slot Reference Schematic

### 2.8.3 Unused SD/MMC/SDIO Interface Signal Termination

All unused SD interface signals can be left unconnected.

## 2.9 I²C

The Colibri module form factor features one general purpose I²C interface. Additional, some Colibri modules feature a dedicated DDC interface on the HDMI FFC connector.

The I²C as well as the DDC interfaces do not feature any pull-up resistors on the module. It is required to add pull-up resistors to the data and clock lines on the carrier board. The pull-up resistor values are normally between 1kΩ and 10kΩ. A small pull-up resistor increases the power consumption while a large resistor could lead to problems in the signal quality. The optimum size of the resistor depends on the capacitive load on the I²C lines and the required bus speed. 4.7kΩ is a suitable value for many applications.

### 2.9.1 I²C Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 194 | I2C_1_SDA | I/O | OD | 3.3V | General purpose I²C data signal, pull-up resistor required on carrier board |
| 196 | I2C_1_SCL | O | OD | 3.3V | General purpose I²C clock signal, pull-up resistor required on carrier board |

Table 14: I²C Signals

### 2.9.2 Real-Team Clock (RTC) recommendation

The RTC on the module is not designed for ultra-low power consumption. Therefore, a standard lithium coin cell battery can drain faster than allowed for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the I²C interface of the module.

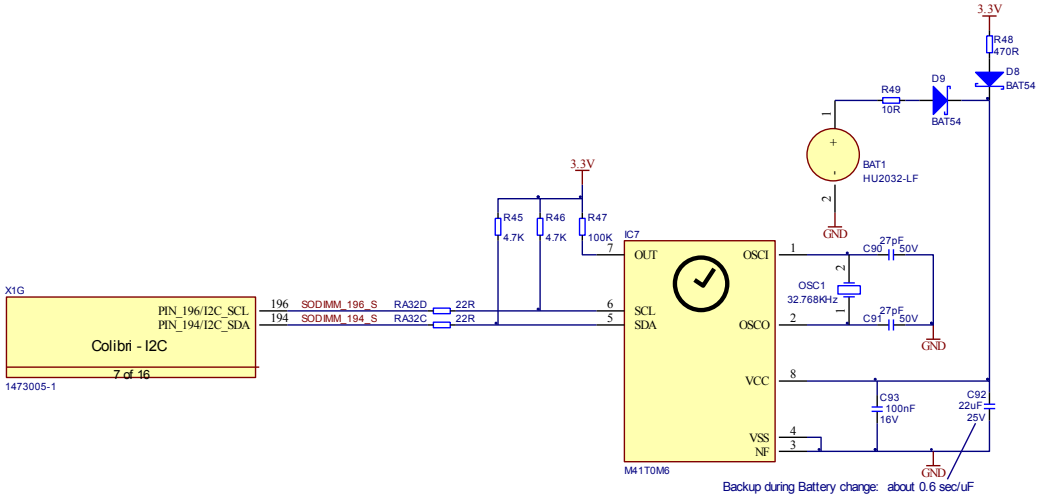


Figure 15: External RTC Reference Schematic

### 2.9.3 Unused I²C Signal Termination

All unused I²C can be left unconnected if the corresponding I²C port is switched off in software. Otherwise, it is recommended to keep the pull-up resistors available. Unused I²C signals can be configured to be GPIO.

## 2.10 UART

The Colibri module form factor features three UART interfaces. Even though the UART_A is specified as full featured UART, some modules might not provide all the control signals. Please read the corresponding datasheet of the module carefully. UART_A is the standard console output interface for the Linux and Windows Embedded Compact operating system. It is desirable to keep at least the RX and TX signals of this port accessible for system debugging.

UART_B features RTS and CTS signals for hardware flow control while UART_C do not feature any flow control signals. Some modules might provide the additional flow control signals on non-standard pins.

### 2.10.1 UART Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 33 | UART_A_RX | I | CMOS | 3.3V | Received Data |
| 35 | UART_A_TX | O | CMOS | 3.3V | Transmitted Data |
| 27 | UART_A_RTS | O | CMOS | 3.3V | Request to Send |
| 25 | UART_A_CTS | I | CMOS | 3.3V | Clear to Send |
| 23 | UART_A_DTR | O | CMOS | 3.3V | Data Terminal Ready |
| 29 | UART_A_DSR | I | CMOS | 3.3V | Data Set Ready |
| 37 | UART_A_RI | I | CMOS | 3.3V | Ring Indicator |
| 31 | UART_A_DCD | I | CMOS | 3.3V | Data Carrier Detect |
| 36 | UART_B_RX | I | CMOS | 3.3V | Received Data |
| 38 | UART_B_TX | O | CMOS | 3.3V | Transmitted Data |
| 34 | UART_B_RTS | O | CMOS | 3.3V | Request to Send |
| 32 | UART_B_CTS | I | CMOS | 3.3V | Clear to Send |
| 19 | UART_C_RX | I | CMOS | 3.3V | Received Data |
| 21 | UART_C_TX | O | CMOS | 3.3V | Transmitted Data |

Table 15: UART Signals

### 2.10.2 Reference Schematics

#### 2.10.2.1 Full Featured RS232 Reference Schematics

The RS232 interface can be classified as Data Terminal Equipment (DTE) or Data Communication Equipment (DCE). This classification is inherited from the usage of the interface for modems. The signal direction of these modes is different. Some Colibri modules might allow changing the mode, and therefore, also the data direction, but this is not a mandatory requirement. According to the Colibri specifications, the interface is intent to be used in the DTE configuration.

| Signal | Name | Usage | DTE Direction (Colibri standard) | DCE Direction |
|---|---|---|---|---|
| UART_A_RXD | Received Data | Data from DCE to DTE | Input | Output |
| UART_A_TXD | Transmitted Data | Data from DTE to DCE | Output | Input |
| UART_A_RTS | Request to Send | DTE request to DCE to be prepared to receive data | Output | Input |
| UART_A_CTS | Clear to Send | DCE indicates ready to accept data | Input | Output |
| UART_A_DTR | Data Terminal Ready | DTE indicates presence to DCE | Output | Input |
| UART_A_DSR | Data Set Ready | DCE is ready to receive commands or data | Input | Output |
| UART_A_RI | Ring Indicator | DCE announce to have detected an incoming ring signal on the telephone line | Input | Output |
| UART_A_DCD | Data Carrier Detect | DCE announce to be connected to the telephone line | Input | Output |

Table 16: RS232 Signal Modes

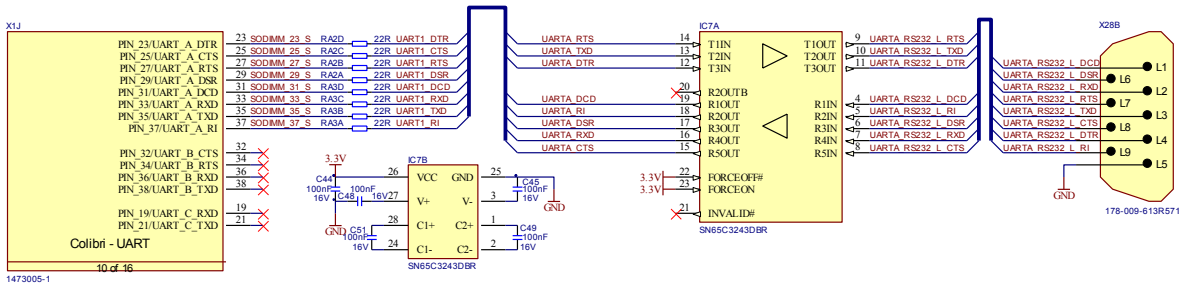


Figure 16: RS232 Reference Schematic

### 2.10.2.2 RS422 Reference Schematics

The RS422 is a full-duplex serial interface with differential pair signals. This allows higher data rates and longer distances as with the RS232. Since the RS422 has separate RX and TX signal pairs, no additional control signals are required for changing the signal direction. This means, the RS422 requires only the RX and TX signals of the UART interface. Therefore, it is possible to use any of the three standard UART interfaces of the Colibri standard.

The RS422 specification does not contain a connector. Therefore, there is no standard connector for this interface available. The reference schematic below uses the 9 pin D-sub connector (DE-9). Peripherals might have a different pin-out even if they use a DE-9 connector.

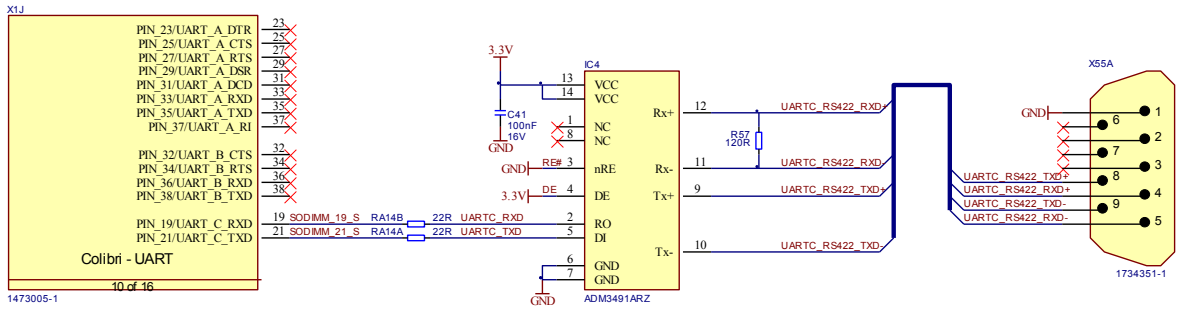


Figure 17: RS422 Reference Schematic

### 2.10.2.3 RS485 Reference Schematics

The RS485 interface is a half-duplex serial interface with differential pair signals. Instead of two differential pair wires (RS422), only one pair is used for transmitting and receiving the data. The bus allows multi point connections. Since the transceiver needs to be set either in the transmitting or receiving mode, an additional control signal is required. It is recommended to use the RTS signal of the corresponding UART interface. The RTS signal is only available on the UART_A and UART_B as Colibri standard interface. The schematic below inverts the RTS signal for the data enable input of the transceiver. Some modules allow inverting the signal in software, but it is recommended to use the inverter circuit shown below in order to maintain compatibility with different modules and drivers provided by Toradex. For some applications, it is desirable that the UART controller does not see the TX message on its RX pins (echo of the sent message). In this case, the receive enable pin (RE#) can be driven as well with the RTS signal. This turns off the RX output buffer while sending a message.

Like the RS422, the RS485 specification also does not describe a standard connector. The reference schematic below uses a DE-9 connector which may have a different pin-out as some peripheral devices.

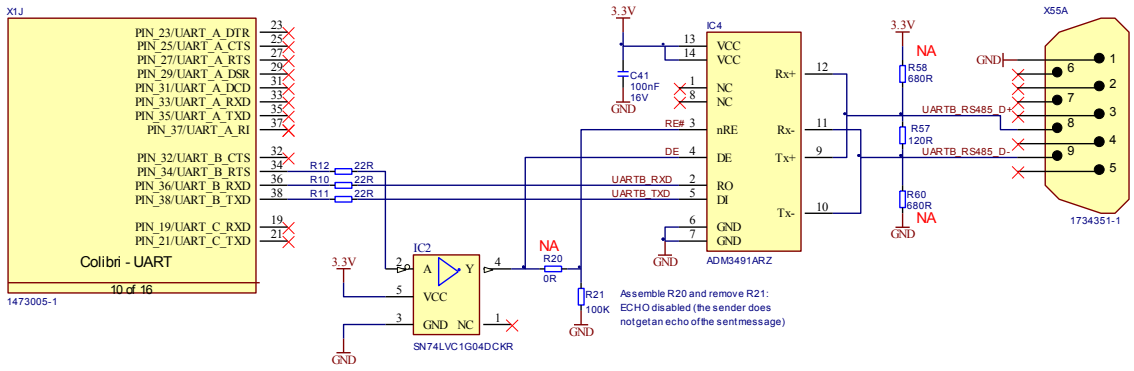


Figure 18: RS485 Reference Schematic

#### 2.10.2.4 IrDA Reference Schematics

IrDA is an optical wireless communication interface. There are different physical layer modulation schemes available. Make sure which modes are supported by the specific Colibri module and the peripheral devices. For compatibility reasons, it is recommended to use UART_C for the IrDA implementation. Some modules only feature the IrDA function on this UART instance.

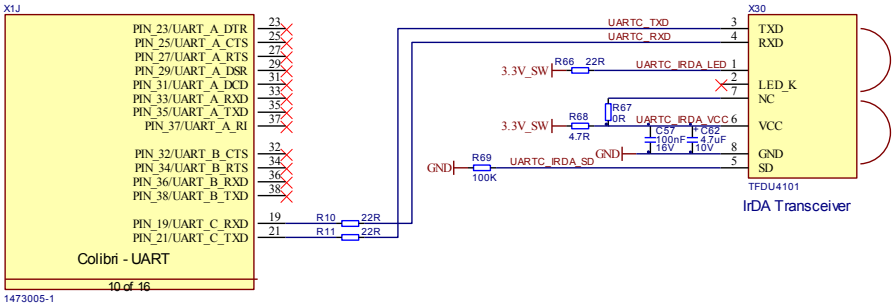


Figure 19: IrDA Reference Schematic

### 2.10.3 Unused UART Signal Termination

Unused UART interface signals can be left unconnected. For debugging purpose, it is recommended to have at least the UART1_RXD and UART1_TXD signals available.

## 2.11 SPI

The serial peripheral interface (SPI) bus is a synchronous, full duplex interface. The Colibri module form factor features one SPI interface. The interface has a chip select signal as compatible standard. Some module may feature additional chip select signal or additional SPI interfaces as secondary function of other pins.

The clock polarity and phase of the SPI bus is not standardized. Some peripherals are latching the data on the positive edge of the clock while others are latching it at the negative edge. The SPI modes describe these different behaviors. Make sure that the according Colibri module and the peripheral device can be set to the same SPI mode.

| SPI Mode | Clock Polarity | Clock Phase | Description |
|---|---|---|---|
| 0 | 0 | 0 | Clock is positive polarity and the data is latched on the positive edge of SCK |
| 1 | 0 | 1 | Clock is positive polarity and the data is latched on the negative edge of SCK |
| 2 | 1 | 0 | Clock is negative polarity and the data is latched on the positive edge of SCK |
| 4 | 1 | 1 | Clock is negative polarity and the data is latched on the negative edge of SCK |

Table 17: SPI Modes

### 2.11.1 SPI Signals

The SPI bus consists of one master and one or many slaves. In the Colibri standard, the module is the SPI master. Some modules might allow to be used also as SPI slaves. Some modules may provide this function on different, non-standard pins.

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 92 | SPI_1_MOSI | O | CMOS | 3.3V | Master Output, Slave Input |
| 90 | SPI_1_MISO | I | CMOS | 3.3V | Master Input, Slave Output |
| 86 | SPI_1_CS0 | O | CMOS | 3.3V | Slave Select |
| 88 | SPI_1_CLK | O | CMOS | 3.3V | Serial Clock |

Table 18: SPI Signals

### 2.11.2 Unused SPI Signal Termination

Unused SPI signals can be left unconnected.

## 2.12 CAN

The Colibri form factor does not provide a controller area network (CAN) bus as a standard interface. Some modules feature dedicated CAN interface signals. For the other modules, it is recommended to add an SPI to CAN controller on the carrier board for providing a CAN interface. This section describes how to add a CAN controller to the SPI interface. If you intent to use the dedicated CAN interface signals, please read the datasheet of the Colibri module.

### 2.12.1 Reference Schematics

Besides a controller, the CAN interface requires a transceiver on the carrier board. Normally, the CAN interface needs to be galvanically isolated from the Colibri computer module. There are transceivers with integrated signal isolation coupler and isolated DC/DC converters available (for example the Analog Devices ADM3053). The other solution is to use separate components for the transceiver, signal coupler and DC/DC converter. There are different type of connectors used for the CAN interface. The reference schematic below uses a DE-9 connector. Since this is not an official standard, some devices might have a different pin-out.

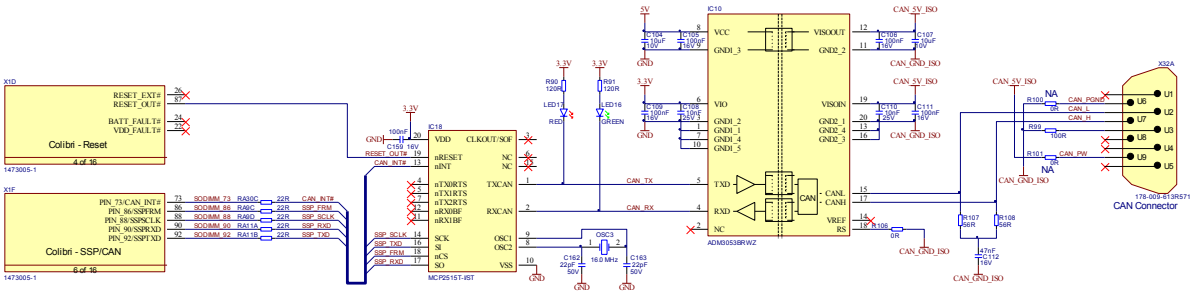


Figure 20: CAN Reference Schematic

## 2.13 PWM

The Colibri module form factor defines four general purpose pulse width modulator (PWM) outputs. Please note that two of the four PWM signals are located on pins that are also used for the standard parallel camera interface. These PWM outputs can only be used if the according camera pins are not in use. The maximum output frequency and the available duty cycle steps can also vary between the different Colibri modules.

### 2.13.1 PWM Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 59 | PWM_A | O | CMOS | 3.3V | General purpose PWM output, pin also used for camera interface |
| 28 | PWM_B | O | CMOS | 3.3V | General purpose PWM output |
| 30 | PWM_C | O | CMOS | 3.3V | General purpose PWM output |
| 67 | PWM_D | O | CMOS | 3.3V | General purpose PWM output, pin also used for camera interface |

Table 19: PWM Signals

### 2.13.2 Reference Schematics

The PWM output signals can be used for example to drive, motors, LEDs, robotic servos or fans. It is possible to get an analogue signal with a simple low-pass filter. A very common usage is driving of the backlight of liquid crystal displays.

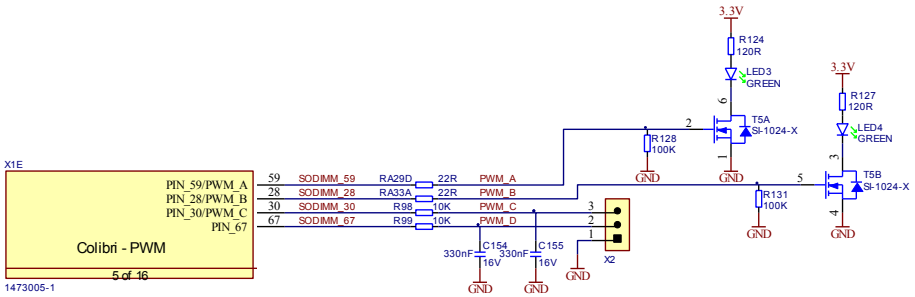


Figure 21: PWM Example Schematic

### 2.13.3 Unused PWM Signal Termination

Unused PWM signals can be left unconnected.

## 2.14 Analogue Audio

### 2.14.1 Analogue Audio Signals

If only single channel (mono) line input or headphone output is required, it is recommended to use the left channel.

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 1 | ANALOG_AUDIO_MIC_IN | I | Analogue | 3.3V | Microphone input |
| 3 | ANALOG_AUDIO_MIC_GND | | Analogue | | Microphone pseudo-ground |
| 5 | ANALOG_AUDIO_LINEIN_L | I | Analogue | 3.3V | Left line input |
| 7 | ANALOG_AUDIO_LINEIN_R | I | Analogue | 3.3V | Right line input |
| 15 | ANALOG_AUDIO_HEADPHONE_L | O | Analogue | 3.3V | Headphone left output (can also be used as line left output) |
| 17 | ANALOG_AUDIO_HEADPHONE_R | O | Analogue | 3.3V | Headphone right output (can also be used as line right output) |
| 13 | ANALOG_AUDIO_HEADPHONE_GND | | Analogue | | Headphone pseudo-ground (do not connect to ground!) |

Table 20: Analogue Audio Signals

### 2.14.2 Reference Schematics

Depending on the module, the headphone output signals can have a DC offset. A common solution is adding series capacitors to the headphone signal lines. If the headphone output signals are used only as line output signals, 1µF series capacitors are sufficient. If the signals are used for driving headphones, larger capacitors (47µF and more) are recommended. Some Colibri modules provide a virtual headphone ground that can be used instead of the series capacitors in order to reduce the BOM cost. Please note this solution only works if the attached device is isolated from the module ground. For example, this works perfectly for headphones, but does not work for an audio amplifier that uses the same ground as the module.

The line-in and microphone signals do not require serial capacitors since they are already placed on the module. Some microphones (e.g. the widely used electret microphones) require a phantom power. The reference schematic below shows a suitable solution for common electret microphone capsules. Please note that some microphones require providing the phantom power on the middle ring of the 3.5mm jack while others need to be powered over the tip of the 3.5mm jack which is also used for the audio signals. The Colibri modules features a special analog ground for the microphone. This is basically a switched ground. Using this ground instead of the regular analog ground allows switching off the phantom power when the microphone is not in use.

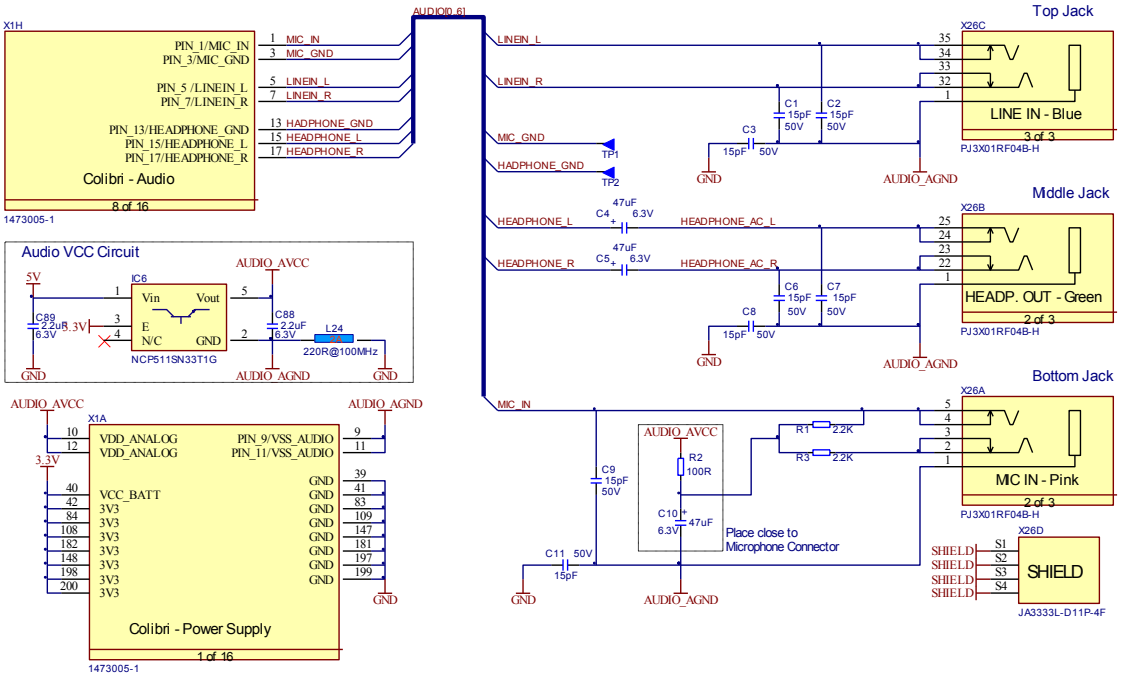


Figure 22: Analogue Audio Reference Schematic

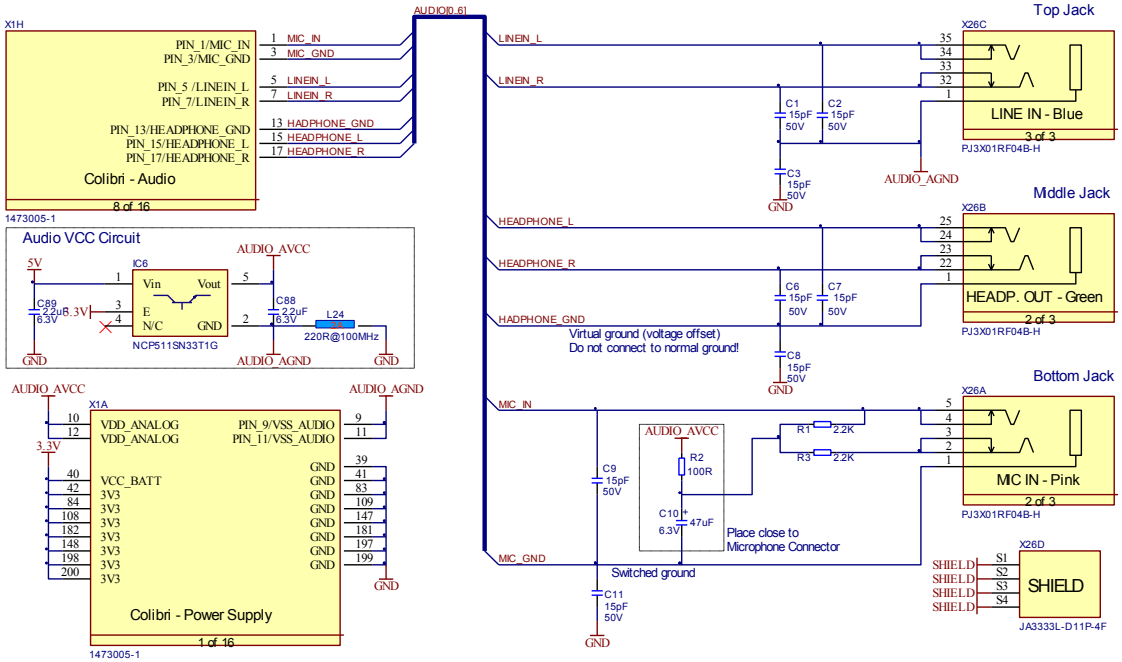


Figure 23: Analogue Audio Reference Schematic (using virtual and switched grounds)

### 2.14.3 Unused Analogue Audio Signal Termination

The unused analogue audio signals can be left unconnected. Please note, even if the analogue audio interface is not used at all, the analogue 3.3V power pins of the module (pin 10 and 12) still needs to be powered. Alternatively, the analogue power can be connected to the digital 3.3V power rail.

## 2.15 Touch Panel Interface

The Colibri module standard features a touch panel interface for resistive touch screens. This allows integrating touch screen solution with a minimum amount of components on the carrier board. This standard supports four-wire resistive touch screens. Some modules also support five-wire touch. Read the corresponding datasheet of the module for more information.

### 2.15.1 Resistive Touch Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 14 | TOUCH_4-wire_PX | I/O | Analogue | 3.3V | X+ (4-wire) |
| 16 | TOUCH_4-wire_MX | I/O | Analogue | 3.3V | X- (4-wire) |
| 18 | TOUCH_4-wire_PY | I/O | Analogue | 3.3V | Y+ (4-wire) |
| 20 | TOUCH_4-wire_MY | I/O | Analogue | 3.3V | Y- (4-wire) |

Table 21: Digital Audio Signals

### 2.15.2 Reference Schematics

In order to reduce the noise that is picked up by the display or long cables, it is recommended to add capacitor to the touch screen signals. 1nF to 10nF is a good choice. It is also recommended to add clamping diodes in order to protect the input of the touch screen controller against ESD.

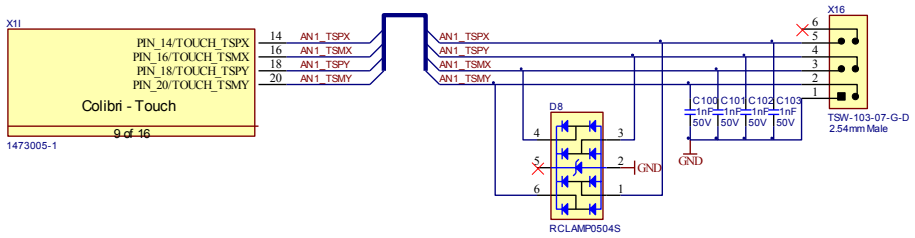


Figure 24: Touch Interface Reference Schematic

### 2.15.3 Unused Touch Panel Interface Signal Termination

Unused touch panel signals can be left unconnected. It is recommended to disable the corresponding drivers.

## 2.16 Analogue Inputs

The Colibri modules feature up to four analogue input channels. The supported sampling rates and resolution are dependent on the modules. The input voltage range is from 0V to 3.3V. The ADC reference is the analogue input voltage rail. The analogue input channels are not designed to be used for high precision measurement tasks. The interface can be used for battery voltage monitoring (additional circuit required), ambient light sensors, or simple analogue joystick input devices.

### 2.16.1 Analogue Input Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 14 | TOUCH_4-wire_PX | I | Analogue | 3.3V | ADC input (3.3V max) |
| 16 | TOUCH_4-wire_MX | I | Analogue | 3.3V | ADC input (3.3V max) |
| 18 | TOUCH_4-wire_PY | I | Analogue | 3.3V | ADC input (3.3V max) |
| 20 | TOUCH_4-wire_MY | I | Analogue | 3.3V | ADC input (3.3V max), some modules might use this input for the five wire resistive touch interface. |

Table 22: Analogue Input Signals

### 2.16.2 Unused Analogue Inputs Signal Termination

The unused analogue input signals can be left unconnected or tied to the ground. It is recommended to disable the corresponding inputs in the driver or disable the whole ADC block if not used.

## 2.17 Parallel Memory Bus (External Memory Bus)

The Colibri form factor reserves several module edge pins as parallel memory bus. This bus can be used for interfacing high-speed peripherals like FPGAs, DSPs, Ethernet controllers, CAN controllers, etc. The supported data and address width as well as some control signal are dependent on the module. Some modules do not even provide a compatible parallel bus on the dedicated signal pins. Carefully check the datasheets of the modules for more information about the supported modes. Additionally, the Pinout Designer tool can be a useful source of information. This tool allows comparing the different bus modes and data/address widths.

### 2.17.1 Memory Bus Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 111 | BUS_A00 | O | CMOS | 3.3V | Address signals. The actual available number of address signals varies from module. |
| 113 | BUS_A01 | O | CMOS | 3.3V | |
| 115 | BUS_A02 | O | CMOS | 3.3V | |
| 117 | BUS_A03 | O | CMOS | 3.3V | |
| 119 | BUS_A04 | O | CMOS | 3.3V | |
| 121 | BUS_A05 | O | CMOS | 3.3V | |
| 123 | BUS_A06 | O | CMOS | 3.3V | |
| 125 | BUS_A07 | O | CMOS | 3.3V | |
| 110 | BUS_A08 | O | CMOS | 3.3V | |
| 112 | BUS_A09 | O | CMOS | 3.3V | |
| 114 | BUS_A10 | O | CMOS | 3.3V | |
| 116 | BUS_A11 | O | CMOS | 3.3V | |
| 118 | BUS_A12 | O | CMOS | 3.3V | |
| 120 | BUS_A13 | O | CMOS | 3.3V | |
| 122 | BUS_A14 | O | CMOS | 3.3V | |
| 124 | BUS_A15 | O | CMOS | 3.3V | |
| 188 | BUS_A16 | O | CMOS | 3.3V | |
| 186 | BUS_A17 | O | CMOS | 3.3V | |
| 184 | BUS_A18 | O | CMOS | 3.3V | |
| 146 | BUS_A19 | O | CMOS | 3.3V | |
| 144 | BUS_A20 | O | CMOS | 3.3V | |
| 142 | BUS_A21 | O | CMOS | 3.3V | |
| 140 | BUS_A22 | O | CMOS | 3.3V | |
| 138 | BUS_A23 | O | CMOS | 3.3V | |
| 136 | BUS_A24 | O | CMOS | 3.3V | |
| 134 | BUS_A25 | O | CMOS | 3.3V | |
| 149 | BUS_D00 | I/O | CMOS | 3.3V | Data signals. The actual available data bits vary from modules. The major part of modules only supports 16 bit data. |
| 151 | BUS_D01 | I/O | CMOS | 3.3V | |
| 153 | BUS_D02 | I/O | CMOS | 3.3V | |
| 155 | BUS_D03 | I/O | CMOS | 3.3V | |
| 157 | BUS_D04 | I/O | CMOS | 3.3V | |
| 159 | BUS_D05 | I/O | CMOS | 3.3V | |
| 161 | BUS_D06 | I/O | CMOS | 3.3V | |
| 163 | BUS_D07 | I/O | CMOS | 3.3V | |
| 165 | BUS_D08 | I/O | CMOS | 3.3V | |
| 167 | BUS_D09 | I/O | CMOS | 3.3V | |
| 169 | BUS_D10 | I/O | CMOS | 3.3V | |
| 171 | BUS_D11 | I/O | CMOS | 3.3V | |

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 173 | BUS_D12 | I/O | CMOS | 3.3V | |
| 175 | BUS_D13 | I/O | CMOS | 3.3V | |
| 177 | BUS_D14 | I/O | CMOS | 3.3V | |
| 179 | BUS_D15 | I/O | CMOS | 3.3V | |
| 150 | BUS_D16 | I/O | CMOS | 3.3V | |
| 152 | BUS_D17 | I/O | CMOS | 3.3V | |
| 154 | BUS_D18 | I/O | CMOS | 3.3V | |
| 156 | BUS_D19 | I/O | CMOS | 3.3V | |
| 158 | BUS_D20 | I/O | CMOS | 3.3V | |
| 160 | BUS_D21 | I/O | CMOS | 3.3V | |
| 162 | BUS_D22 | I/O | CMOS | 3.3V | |
| 164 | BUS_D23 | I/O | CMOS | 3.3V | |
| 166 | BUS_D24 | I/O | CMOS | 3.3V | |
| 168 | BUS_D25 | I/O | CMOS | 3.3V | |
| 170 | BUS_D26 | I/O | CMOS | 3.3V | |
| 172 | BUS_D27 | I/O | CMOS | 3.3V | |
| 174 | BUS_D28 | I/O | CMOS | 3.3V | |
| 176 | BUS_D29 | I/O | CMOS | 3.3V | |
| 178 | BUS_D30 | I/O | CMOS | 3.3V | |
| 180 | BUS_D31 | I/O | CMOS | 3.3V | |
| 126 | BUS_DQM0 | O | CMOS | 3.3V | Byte Enable Mask, corresponds to D[7:0] |
| 128 | BUS_DQM1 | O | CMOS | 3.3V | Byte Enable Mask, corresponds to D[15:8] |
| 130 | BUS_DQM2 | O | CMOS | 3.3V | Byte Enable Mask, corresponds to D[23:16] |
| 132 | BUS_DQM3 | O | CMOS | 3.3V | Byte Enable Mask, corresponds to D[31:24] |
| 105 | BUS_nCS0 | O | CMOS | 3.3V | |
| 107 | BUS_nCS1 | O | CMOS | 3.3V | Chip select signals |
| 106 | BUS_nCS2 | O | CMOS | 3.3V | |
| 91 | BUS_nOE | O | CMOS | 3.3V | Output Enable |
| 99 | BUS_nPWE | O | CMOS | 3.3V | Buffered Write Enable |
| 89 | BUS_nWE | O | CMOS | 3.3V | Write Enable |
| 93 | BUS_RDnWR | O | CMOS | 3.3V | Buffered Write Enable |
| 95 | BUS_RDY | I | CMOS | 3.3V | Ready/Busy/Wait signal |

Table 23: Memory Bus Signals

### 2.17.2 Unused Memory Bus Signals Termination

All unused memory bus signals can be left unconnected. On the Colibri PXA270, the memory bus interface is also used on the module for connecting the RAM, flash and Ethernet controller. Therefore, the bus signal pins cannot be used for any other purpose on this module. On other modules, it might be possible to use the unused bus signals as GPIO or for other alternative functions.

## 2.18 GPIO

Many of the interface pins can also be used as general purpose input output pin (GPIO) for alternative function. Theoretically, any unused interface pin that serves GPIO function can be used. Since some interface pins do not provide GPIO functionality on certain Colibri modules, there is a list of preferred GPIO pins. For compatibility reason, we recommend using the first pin on this list. Please note that there might be additional restrictions in using the GPIO functions on certain modules. For example, two pins share the same GPIO instance and therefore cannot be used independently of each other on some modules. More information can be found in the datasheet of the module.

### 2.18.1 Preferred GPIO Signals

| Colibri Pin | I/O | Type | Power Rail | Description |
|---|---|---|---|---|
| 19, 21, 23, 25, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 78, 79, 80, 81, 82, 85, 86, 88, 90, 92, 95, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 127, 129, 131, 133, 135, 137, 190, 192, 194, 196 | I/O | CMOS | 3.3V | General purpose GPIO |

Table 24: Dedicated GPIO Signals

### 2.18.2 Unused GPIO Termination

The GPIO signals do not need to be terminated if they are not in use.

# 3 Power Management

## 3.1 Power Signals

### 3.1.1 Digital Supply Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 42, 84,108, 148,182,198, 200 | VCC | I | PWR | 3.3V | Main power supply input for the module |
| 39, 41, 83, 109,147, 181, 197, 199 | GND | I | PWR | | Common signal and power ground |
| 40 | VCC_BACKUP | I | PWR | 3.3V | RTC supply, connect this pin to 3.3V even if the internal RTC is not used |

Table 25: Digital Supply Signals

### 3.1.2 Analogue Supply Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 10, 12 | AVDD_AUDIO | I | PWR | 3.3V | Power supply for the analogue part of the module |
| 9, 11 | VSS_AUDIO | I | PWR | | Ground for the analogue part of the module |

Table 26: Analogue Supply Signals

The analogue power supply is used on the module for the analogue circuits. 3.3 Volt need to be provided to this input even if the analogue part is not used in a design. In this case, the pins can be connected to the main power input of the module. For a better audio quality, it is recommended to add separate filters to the analogue power supply rail. For the best quality, a separate power supply with linear voltage regulator is recommended.

### 3.1.3 Power Management Signals

| Colibri Pin | Colibri Signal Name | I/O | Type | Power Rail | Description |
|---|---|---|---|---|---|
| 26 | nRESET_EXT (CTRL_RESET_MICO) | I | CMOS | 3.3V | Active low reset input |
| 87 | nRESET_OUT (CTRL_RESET_MOCi) | O | CMOS | 3.3V | Active low reset output |
| 43 | CTRL_WAKE_0 | I | CMOS | 3.3V | Active low main module wake input signal, needs a pull-up resistor on the baseboard if wake function is used |

Table 27: Power Management Signals

In order to make the direction of the power management signals clear, the ending MICO or MOCI are added. MICO is the abbreviation for “Module Input, Carrier board Output” while MOCI stands for “Module Output, Carrier board Input”

## 3.2 Power Block Diagram

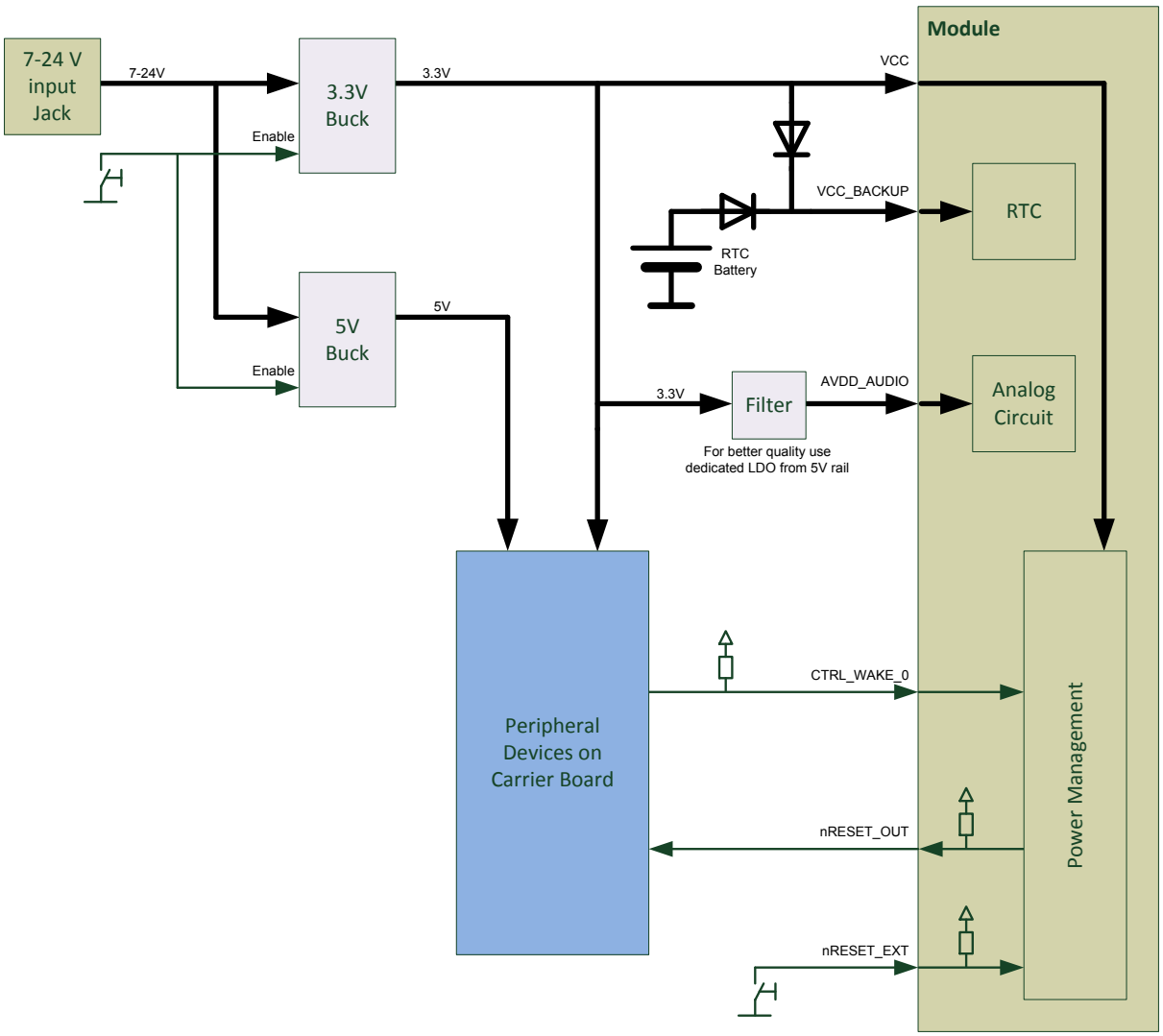


Figure 25: Power Block Diagram

If the internal RTC of the module is not used or the analog audio and resistive touch interface is not required, the carrier board power supply can be further simplified. It is important that even if RTC and/or the analog interfaces are not used, its corresponding supply rails need to be served by the carrier board.

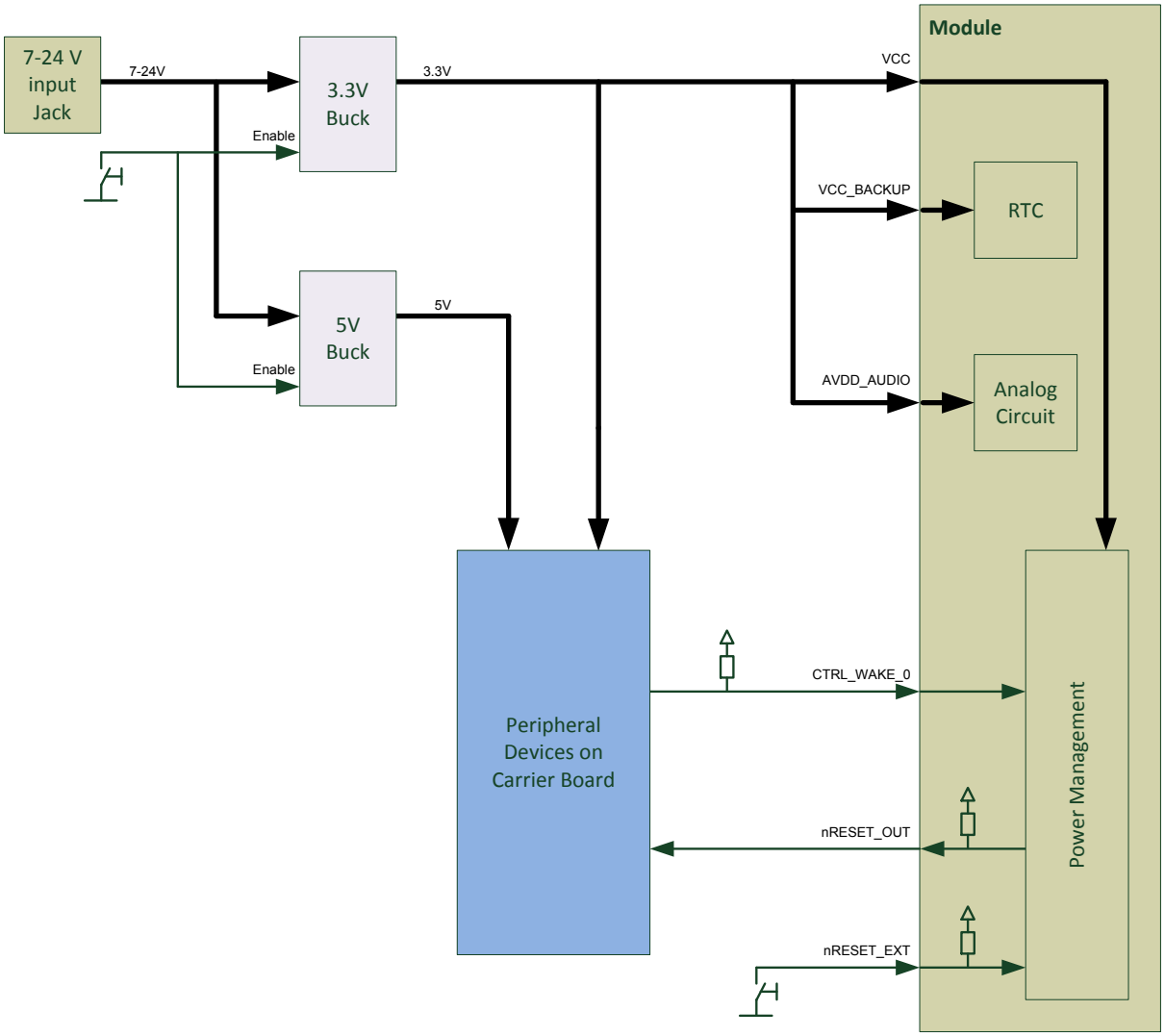


Figure 26: Power Block Diagram (without RTC an analog interfaces)

## 3.3 Power States

The Colibri module and carrier board has different power states. The table below describes the behavior during different states and which power rails and peripherals are active. These are just the standard power states. If additional power saving is necessary, it is possible to introduce other states in which some of the carrier board peripherals are switched off. In this case, free GPIO can be used to switch off unused peripheral power rails.

| Abbr. | Name | Description | Module | Carrier Board |
|---|---|---|---|---|
| UPG | Unplugged | No power is applied to the system, except the RTC battery might be available | No main VCC and AVDD_AUDIO applied, maybe VCC_BACKUP available | No power supply input, RTC battery maybe inserted |
| SUS | Suspend | System is suspended and waits for wakeup sources to trigger | CPU is suspended, wakeup capable peripherals are running while others might be switched off | Power rails are available on carrier board, peripherals might be stopped by software |
| RUN | Running | System is running | All power rails are available, CPU and peripherals are running | All power rails are available, peripherals are running |
| RST | Reset | System is put in reset state by holding nRESET low | All power rails are available, CPU and peripherals are in reset state | All power rails are available, peripherals are in reset state |

Table 28: Available Colibri Power States

The figure shown below shows a sequence diagram of the different power states. The module automatically goes into the running mode when the main power rail is applied to the module. In the running mode, the system can be set to be suspended by the software. There might be different wake up sources available. Read the datasheet of the corresponding module for more information about the available wakeup events. All Colibri modules have it in common that the CTRL_WAKE_0 wakes up the module if the signal level goes low. If compatibility between the modules is needed, use this pin as the general wake signal.

Unlike the Apalis module family, the Colibri modules do not provide a shutdown state in which the module can switch off the carrier board peripheral supplies. The Colibri module does not have a dedicated signal for turning off the peripheral supplies. Nevertheless, some modules can be shut down (depending on the used operating system). In the standard carrier board architecture, all power rails will remain on.

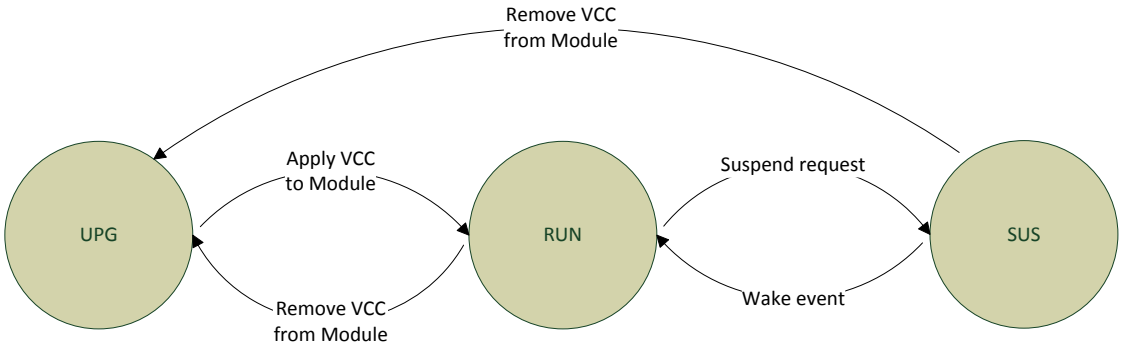


Figure 27: Power State Diagram

## 3.4 Power-Up Sequence

The Colibri module starts booting as soon as the main voltage rail is applied to the module. It is important that the main input voltage rises monotonically. The RTC rail (VCC_BACKUP) needs to be applied before or together with the main voltage. It is not allowed to apply the analogue voltage supply before applying the main voltage.

The peripheral power rails on the carrier board needs to be ramped-up in a correct sequence. The sequence starts normally with the highest voltage (e.g. 5V) followed by the lower voltages (e.g. 3.3V then 1.5V and so on). Peripherals normally require that a lower voltage rails is never present if a higher rail is missing. Check the datasheet of all peripheral components on the carrier board for a proper sequencing.

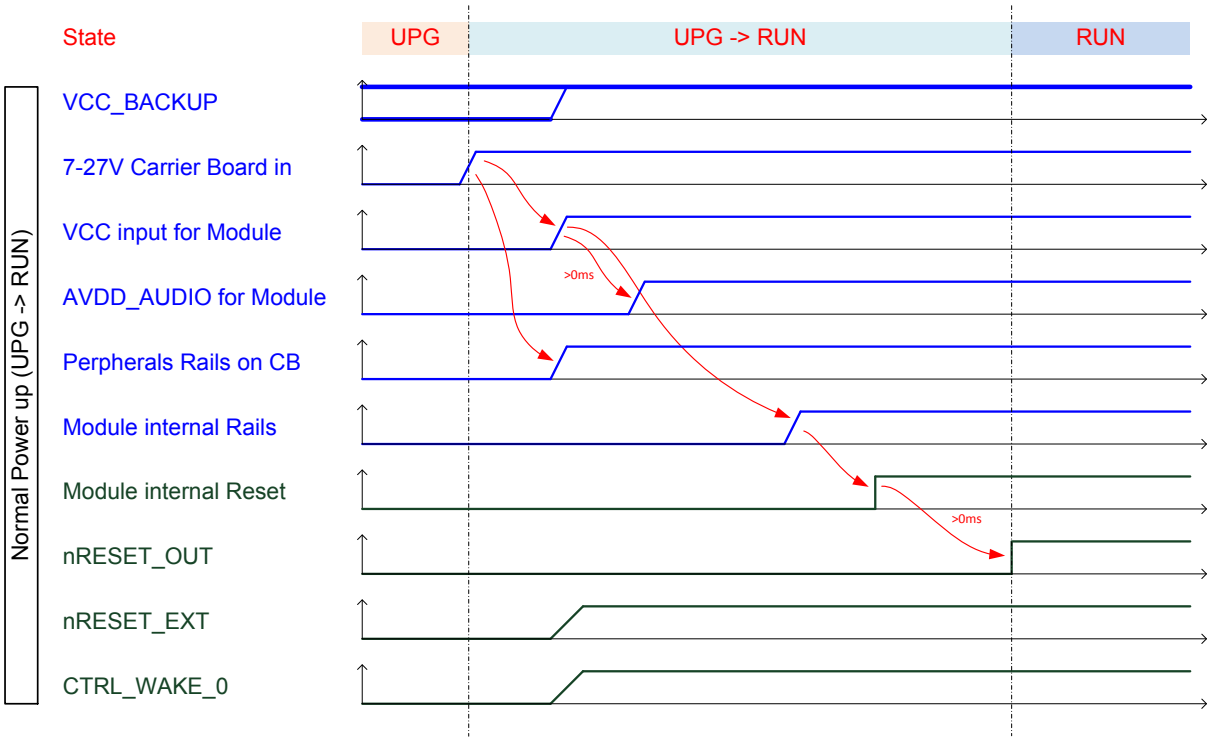


Figure 28: Power-Up Sequence

## 3.5 Reference Schematics

Place enough power supply bypass capacitors to the voltage inputs of the peripheral devices (see Toradex Layout Design Guide). Place a bypass capacitor to each power input pin of the Colibri module. Be wary of the total capacity on a voltage rail when switching the voltage. If the rails are switched on too fast, the current peaks for charging all the bypass capacitors can be very high. This can produce unacceptable disturbances or can trigger an overcurrent protection circuit. Maybe the switching speed needs to be limited. The following figure shows a simple voltage rail switch circuit. C1 and R1 limit the switching speed. The values need to be optimized according to the requirements. It is recommended to place a bypass capacitor (C2) close to the switching transistor.

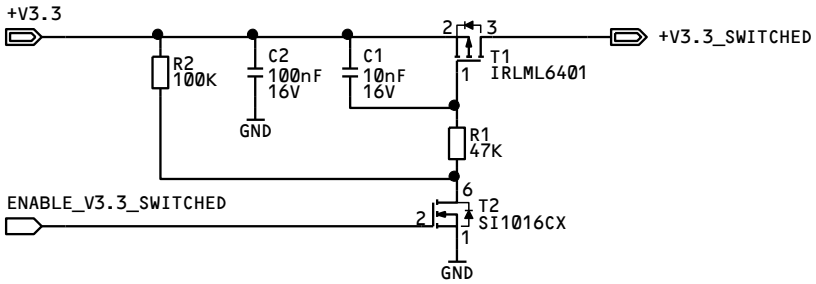


Figure 29: Simple Voltage Switch Circuit

The carrier board needs to provide the 3.3V main voltage for the module as well as all voltage rails for the peripheral devices. Check the maximum current consumption of the Colibri modules that

are intent to be used with the carrier board. Currently, the Colibri T30 is the module with the highest current consumption. This module can draw up to 1.2A. In order to leave enough margins, take 2A into the power budget for the Colibri T30 module. Do not forget taking the additional current consumption of the peripheral devices on the 3.3V rail into the budget.

The nRESET_EXT and nRESET_OUT do not need any pull-up resistors on the carrier board since these resistors are already placed on the module. The CTRL_WAKE_0 requires a pull-up resistor on the carrier board if the wake function is implemented.

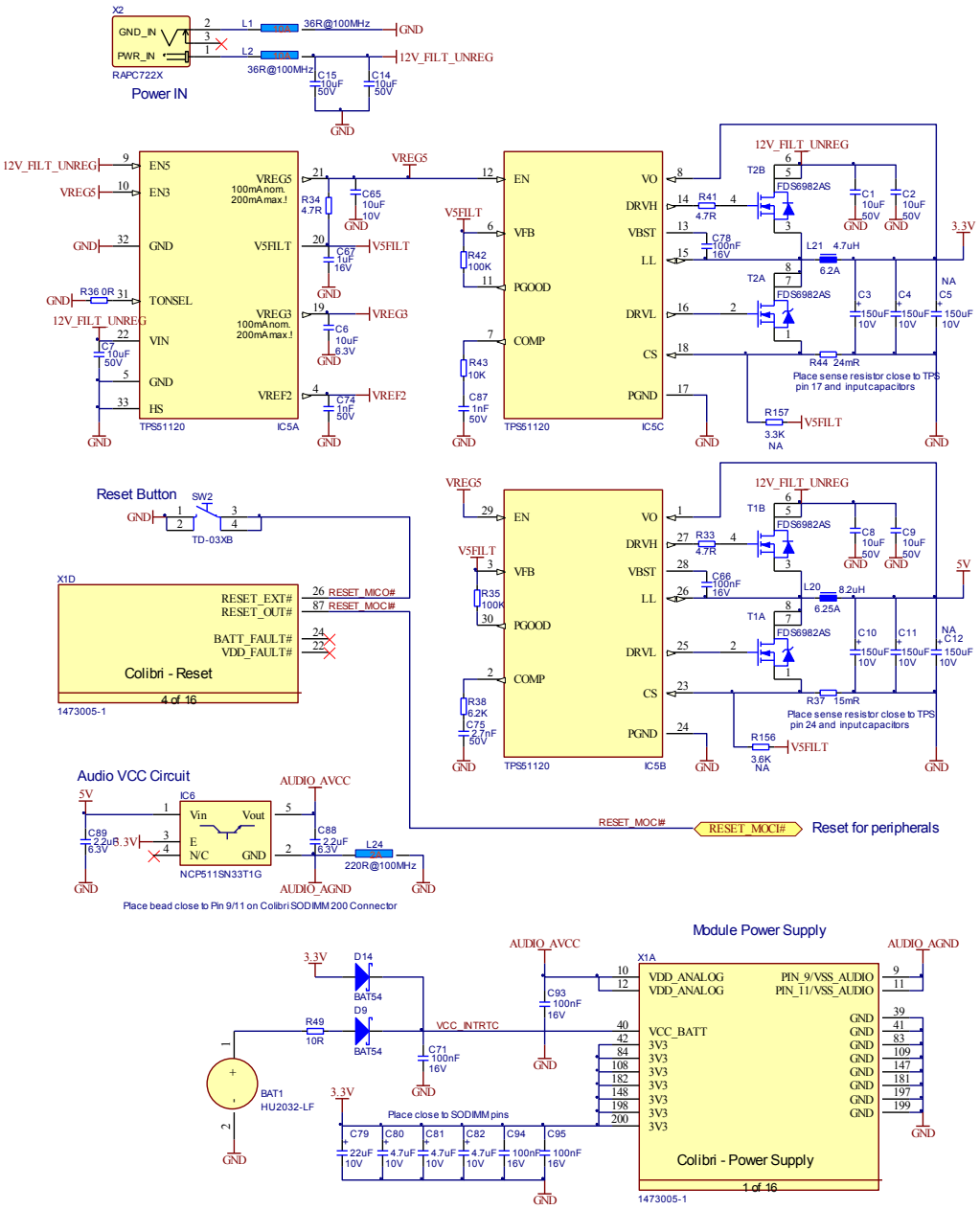


Figure 30: Simple Power Supply Reference Schematic

# 4 Mechanical and Thermal Consideration

## 4.1 Module Connector

The Colibri modules fit into a regular 2.5V (DDR1) SO-DIMM200 memory socket. Please note there are two version of 200pin SO-DIMM connector available. The Colibri module is only compatible with the variant that is designed for DDR1 modules with 2.5V. The 1.8V DDR2 variant has a different notch position and is therefore not compatible.

There are many suitable connectors from different manufacturers available in different stacking height. A selection of SO-DIMM200 socket manufacturers is listed below:

| | |
|---|---|
| CONCRAFT: | http://www.concraft.com.tw/products_connector/ct/ddr-1.html |
| Morethanall Co Ltd.: | http://www.morethanall.com |
| Tyco Electronics (AMP): | http://www.te.com |
| NEXUS COMPONENTS GmbH: | http://www.nexus-de.com |
| FCI | http://www.fci.com |

## 4.2 Fixation of the Module

The SO-DIMM connector features a locking mechanism which is reliable for many applications. In order to ensure the proper connection of a module at high vibration and/or shock situations, additional fixation might be required. The Colibri module offers different solutions for the fixation.

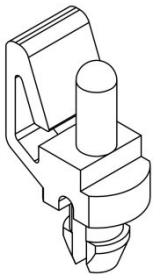

Figure 31: Colibri Fastener

Toradex offers Colibri Fastener for an easy to install fixation. Two fasteners are required for holding the module. The fastener support SO-DIMM connector height of 5.2mm only. If a connector with a different height is used, another fixation solution is required. Please note, inserting the Colibri module is critical, if done wrong the Colibri can be damaged due mechanical stress! More information including a module inserting guide can be found here: http://developer.toradex.com/product-selector/colibri-fastener

Figure 32: Colibri Module with Fastener

Instead of using the holes on the module for the fastener, it can also be used for fixing the module with screws. Select a suitable spacer which matches the SO-DIMM connector stacking height. The holes in the module have a diameter of 2.0mm. Therefore, M1.5, M1.6, or M1.8 screws can be used. Please note the maximum allowed head and washer diameter is 6mm.

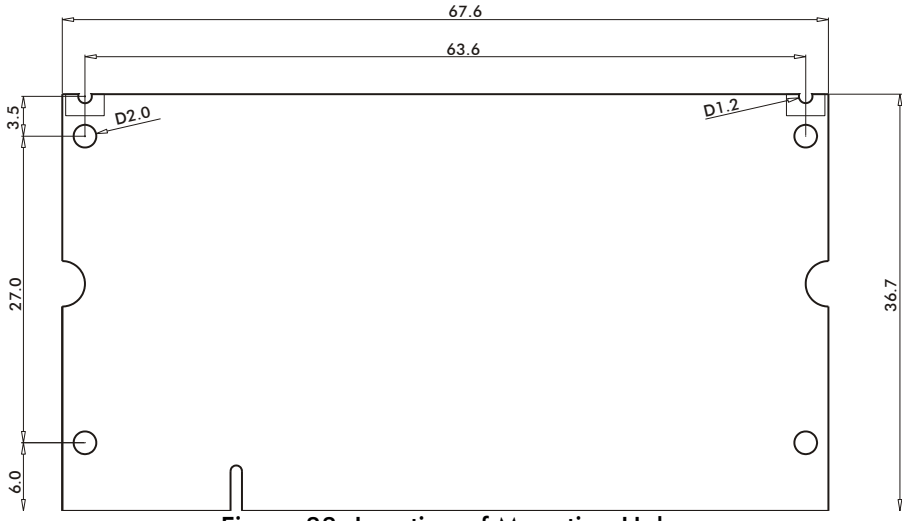


Figure 33: Location of Mounting Holes

The third option is to solder down the module. The modules feature a half open through-hole solder pad. These holes can be used for soldering the module down with solder pins. Please note the solder pads are connected to the ground plane of the module. Some of the older modules might do not feature the pads. Please contact the Toradex support team for more information.

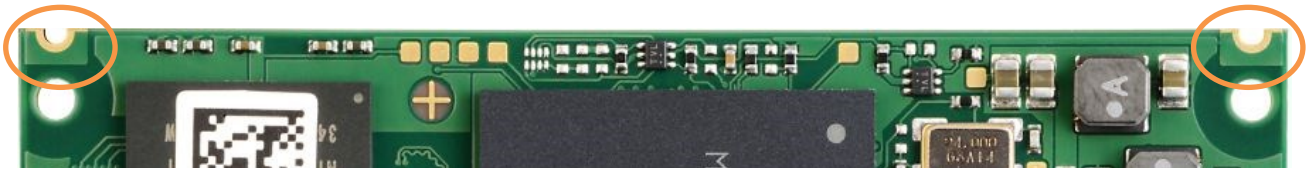

Figure 34: Thru-Hole Solder Pads for Fixation

## 4.3 Thermal Solution

The Colibri modules are designed to be used without additional heat spreader or heat sink. Most of the Colibri modules feature thermal throttling mechanism. The module measures the current temperature of the SoC. If it reaches a critical limit, it starts throttling down the CPU speed or shuts the system completely down in order to prevent damages. Please read the corresponding datasheets for more information to the thermal behavior.

- If you only use the peak performance for a short time period, heat dissipation is less of a problem because most of the module will reduce the power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to smaller leakage currents.
- If you need the full CPU/Graphics performance over a long period of time, make sure that you are able to dissipate sufficient thermal energy to the environment.

In general, more effectively the generated thermal energy is transported to the environment, the better performance you get out of the computer module. Therefore, it might be necessary to add a thermal solution. The best solution is to glue a suitable heat sink directly to the top of the SoC. Since the module PCB is only 1mm thick, the board is not very stiff. Appling force to the SoC can bend PCB which destroys the module. Therefore, pay attention when mounting a thermal solution on the module that the module is not cracked due to bending stress.

## 4.4 Module Size

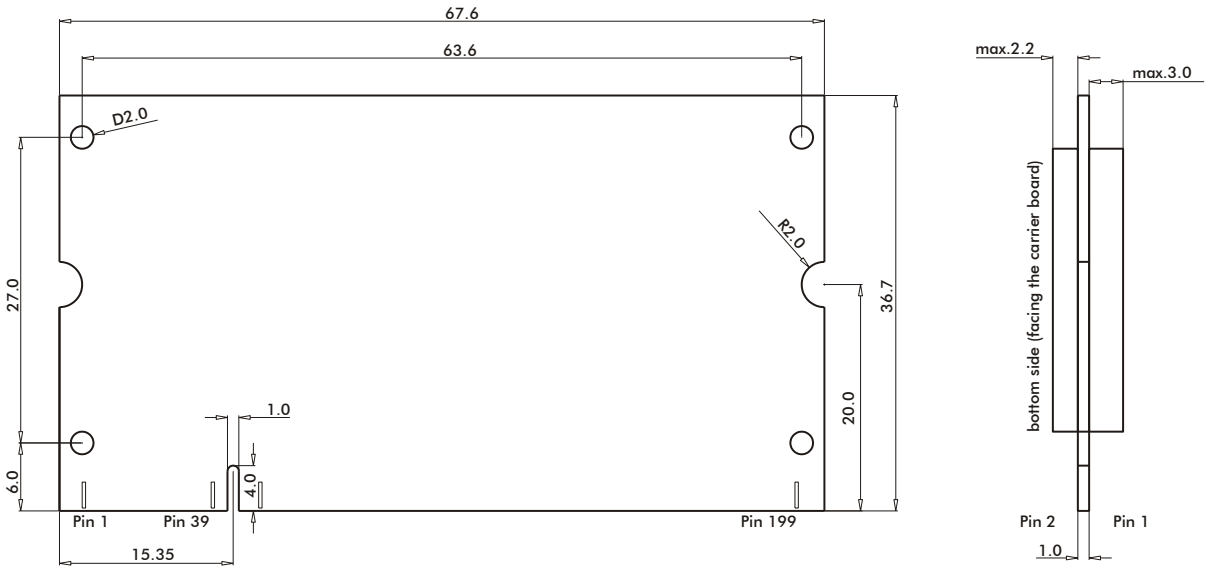


Figure 35: Module Dimensions Top Side (dimensions in mm)

# 5 Appendix A – Physical Pin Definition and Location

The following table contains the information about the standard functions on the module edge connector pins. Not all modules feature the complete set of standard function. Please read carefully the function lists in the datasheet of the modules. The Toradex Pinout Designer can be a useful tool for checking the availability of functions on certain modules. It helps configuring the pin muxing. More information and download link can be found here:
http://developer.toradex.com/knowledge-base/pinout-designer

| Module Bottom Side | SO-DIMM Pin | | Module Top Side |
|---|---|---|---|
| Analogue Input <3> | 2 | 1 | Audio Analogue Microphone Input |
| Analogue Input <2> | 4 | 3 | Audio Analogue Microphone GND |
| Analogue Input <1> | 6 | 5 | Audio Analogue Line-In Left |
| Analogue Input <0> | 8 | 7 | Audio Analogue Line-In Right |
| Audio_Analogue VDD | 10 | 9 | Audio_Analogue GND |
| Audio_Analogue VDD | 12 | 11 | Audio_Analogue GND |
| Resistive Touch PX | 14 | 13 | Audio Analogue Headphone GND |
| Resistive Touch MX | 16 | 15 | Audio Analogue Headphone Left |
| Resistive Touch PY | 18 | 17 | Audio Analogue Headphone Right |
| Resistive Touch MY | 20 | 19 | UART_C RXD |
| VDD Fault Detect | 22 | 21 | UART_C TXD |
| Battery Fault Detect | 24 | 23 | UART_A DTR |
| nReset In | 26 | 25 | UART_A CTS, Keypad_In<0> |
| PWM<B> | 28 | 27 | UART_A RTS |
| PWM<C> | 30 | 29 | UART_A DSR |
| UART_B CTS | 32 | 31 | UART_A DCD |
| UART_B RTS | 34 | 33 | UART_A RXD |
| UART_B RXD | 36 | 35 | UART_A TXD |
| UART_B TXD | 38 | 37 | UART_A RI, Keypad_In<4> |
| VCC_BATT | 40 | 39 | GND |
| | | | |
| 3V3 | 42 | 41 | GND |
| LCD RGB DE | 44 | 43 | WAKEUP Source<0>, SDCard CardDetect |
| LCD RGB Data<7> | 46 | 45 | WAKEUP Source<1> |
| LCD RGB Data<9> | 48 | 47 | SDCard CLK |
| LCD RGB Data<11> | 50 | 49 | SDCard DAT<1> |
| LCD RGB Data<12> | 52 | 51 | SDCard DAT<2> |
| LCD RGB Data<13> | 54 | 53 | SDCard DAT<3> |
| LCD RGB PCLK | 56 | 55 | PS2 SDA1 |
| LCD RGB Data<3> | 58 | 57 | LCD RGB Data<16> |
| LCD RGB Data<2> | 60 | 59 | PWM<A>, Camera Input Data<7> |
| LCD RGB Data<8> | 62 | 61 | LCD RGB Data<17> |
| LCD RGB Data<15> | 64 | 63 | PS2 SCL1 |
| LCD RGB Data<14> | 66 | 65 | Camera Input Data<9>, Keypad_Out<3>, PS2 SDA2 |
| LCD RGB HSYNC | 68 | 67 | PWM<D>, Camera Input Data<6> |
| LCD RGB Data<1> | 70 | 69 | PS2 SCL2 |
| LCD RGB Data<5> | 72 | 71 | Camera Input Data<0>, LCD Back-Light GPIO |
| LCD RGB Data<10> | 74 | 73 | |
| LCD RGB Data<0> | 76 | 75 | Camera Input MCLK |
| LCD RGB Data<4> | 78 | 77 | |
| LCD RGB Data<6> | 80 | 79 | Camera Input Data<4> |
| LCD RGB VSYNC | 82 | 81 | Camera Input VSYNC |
| 3V3 | 84 | 83 | GND |
| SPI CS | 86 | 85 | Camera Input Data<8>, Keypad_Out<4> |
| SPI CLK | 88 | 87 | nReset Out |
| SPI RXD | 90 | 89 | nWE |
| SPI TXD | 92 | 91 | nOE |

| | | | |
|---|---|---|---|
| Camera Input HSYNC | 94 | 93 | RDnWR |
| Camera Input PCLK | 96 | 95 | RDY |
| Camera Input Data<1> | 98 | 97 | Camera Input Data<5> |
| Keypad_Out<1> | 100 | 99 | nPWE |
| | 102 | 101 | Camera Input Data<2> |
| | 104 | 103 | Camera Input Data<3> |
| nCS2 | 106 | 105 | nCS0 |
| 3V3 | 108 | 107 | nCS1 |
| ADDRESS8 | 110 | 109 | GND |
| ADDRESS9 | 112 | 111 | ADDRESS0 |
| ADDRESS10 | 114 | 113 | ADDRESS1 |
| ADDRESS11 | 116 | 115 | ADDRESS2 |
| ADDRESS12 | 118 | 117 | ADDRESS3 |
| ADDRESS13 | 120 | 119 | ADDRESS4 |
| ADDRESS14 | 122 | 121 | ADDRESS5 |
| ADDRESS15 | 124 | 123 | ADDRESS6 |
| DQM0 | 126 | 125 | ADDRESS7 |
| DQM1 | 128 | 127 | |
| DQM2 | 130 | 129 | USB Host Power Enable |
| DQM3 | 132 | 131 | USB Host Over-Current Detect |
| ADDRESS25 | 134 | 133 | |
| ADDRESS24 | 136 | 135 | SPDIF_IN |
| ADDRESS23 | 138 | 137 | USB Client Cable Detect, SPDIF_OUT |
| ADDRESS22 | 140 | 139 | USB Host DP |
| ADDRESS21 | 142 | 141 | USB Host DM |
| ADDRESS20 | 144 | 143 | USB Client DP |
| ADDRESS19 | 146 | 145 | USB Client DM |
| 3V3 | 148 | 147 | GND |
| DATA16 | 150 | 149 | DATA0 |
| DATA17 | 152 | 151 | DATA1 |
| DATA18 | 154 | 153 | DATA2 |
| DATA19 | 156 | 155 | DATA3 |
| DATA20 | 158 | 157 | DATA4 |
| DATA21 | 160 | 159 | DATA5 |
| DATA22 | 162 | 161 | DATA6 |
| DATA23 | 164 | 163 | DATA7 |
| DATA24 | 166 | 165 | DATA8 |
| DATA25 | 168 | 167 | DATA9 |
| DATA26 | 170 | 169 | DATA10 |
| DATA27 | 172 | 171 | DATA11 |
| DATA28 | 174 | 173 | DATA12 |
| DATA29 | 176 | 175 | DATA13 |
| DATA30 | 178 | 177 | DATA14 |
| DATA31 | 180 | 179 | DATA15 |
| 3V3 | 182 | 181 | GND |
| ADDRESS18 | 184 | 183 | Ethernet Link/Activity Status |
| ADDRESS17 | 186 | 185 | Ethernet Speed Status |
| ADDRESS16 | 188 | 187 | Ethernet TXO- |
| SDCard CMD | 190 | 189 | Ethernet TXO+ |
| SDCard DAT<0> | 192 | 191 | Ethernet GND |
| I2C SDA | 194 | 193 | Ethernet RXI- |
| I2C SCL | 196 | 195 | Ethernet RXI+ |
| 3V3 | 198 | 197 | GND |
| 3V3 | 200 | 199 | GND |

Table 29: Physical Pin Definition and Location