IA-2(B)
Design and verify the 4- Bit Synchronous or Asynchronous Counter using JK Flip Flop

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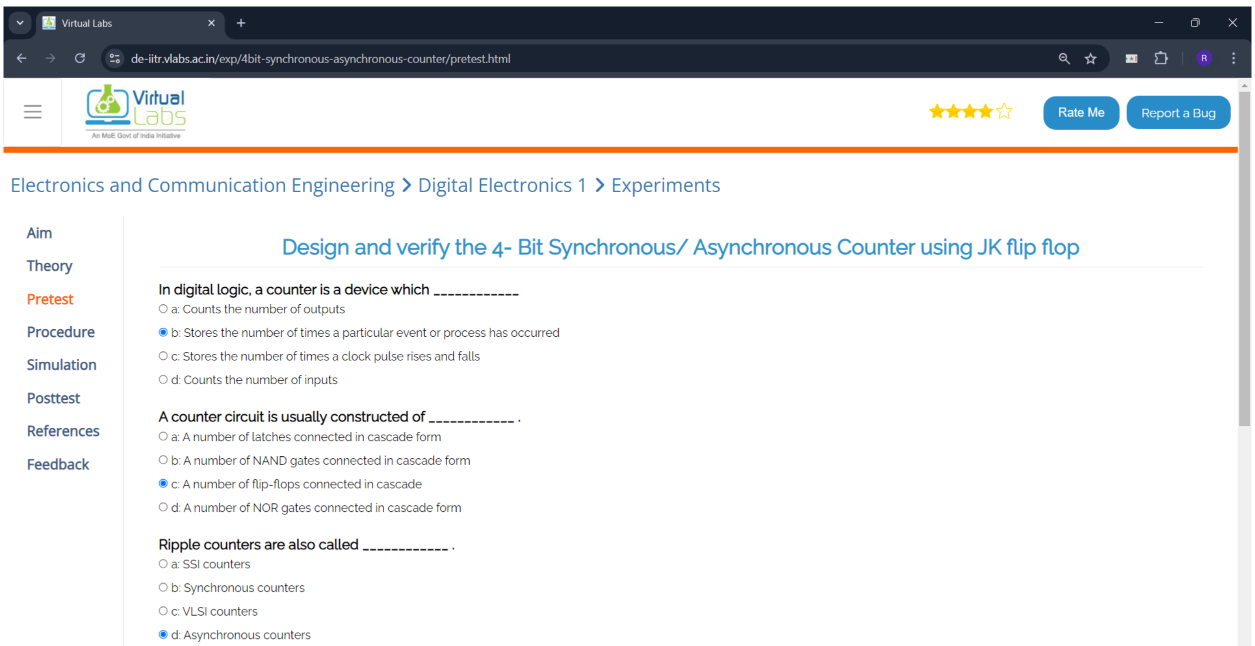
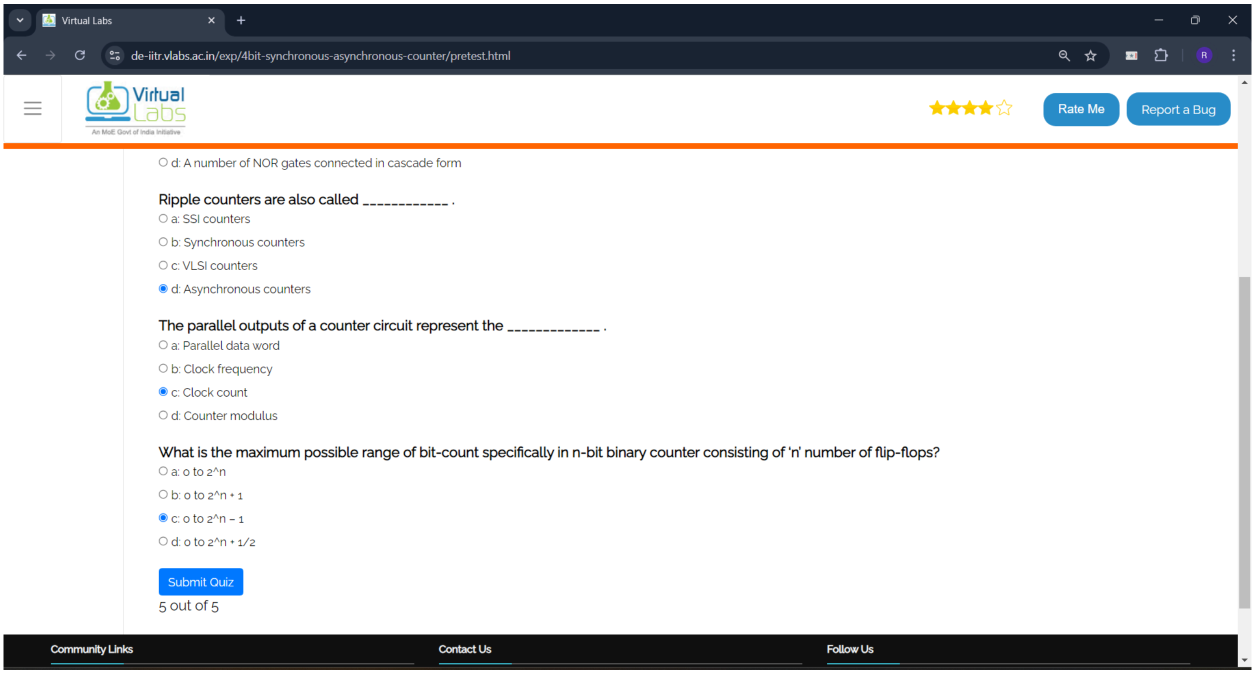
Class : SY-IT(B3)

Pretest :





Justifications for each of the answers :

- A counter is a circuit that keeps track of how often something happens, like clock ticks or other signals. Its main job is to count how many times an event occurs, not to count the inputs or outputs directly.
- Flip-flops are the basic building blocks of counters because they can store one of two states: 0 or 1 (binary). When you connect them in a chain, where one flip-flop's output triggers the next one, they can work together to count multiple bits. For example, using three flip-flops gives you 8 possible states (since 2^3 = 8).
- Ripple counters are called asynchronous because the flip-flops don't all get the clock signal at the same time. Instead, each flip-flop waits for the previous one to change before it updates, causing a "ripple" effect as the counting happens.
- The parallel outputs of a counter show the binary number that represents the current count. Each flip-flop's state contributes to the binary number, and together they form a "parallel" set of bits, which is basically a data word.
- An n-bit binary counter can show 2^n different values. Since counting starts at 0, the largest number it can show is 2^n - 1. So, if you have 3 bits, it counts from 0 to 7 (which is 2^3 - 1). The range is from 0 to 2^n - 1 because we're working with binary, and that's how the counting works.

Simulation :

1. Aynchronous Counter

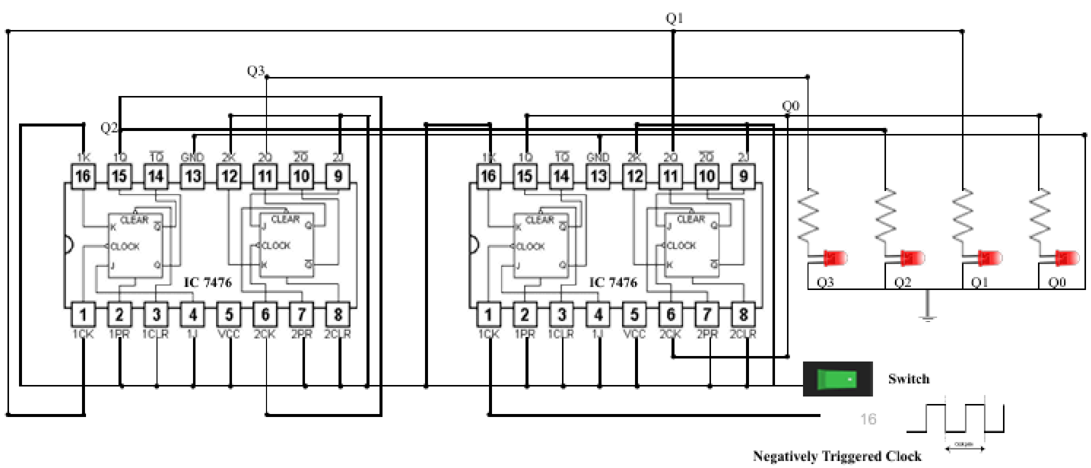
- **First Trigger:** The first flip-flop (usually a JK or D flip-flop) is directly controlled by the clock signal.
- **Cascading Trigger:** Once the first flip-flop changes, it triggers the next one, and this process continues with each flip-flop triggering the next in line.
- **Ripple Effect:** As the clock signal changes the first flip-flop, the change moves, or "ripples," through the other flip-flops one after another, which is why it's called a ripple counter.

10/7/24, 8:06 PM Asynchronous Counter

Instructions

4-Bit Asynchronous Parallel Counter using J-K Flip-Flop

Print

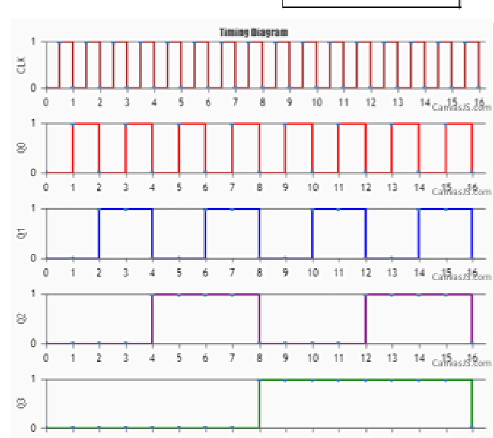


TRUTH TABLE

Serial No.	Clock	Q3	Q2	Q1	Q0
1	1	0	0	0	0
2	2	0	0	0	1
3	3	0	0	1	0
4	4	0	0	1	1
5	5	0	1	0	0
6	6	0	1	0	1
7	7	0	1	1	0
8	8	0	1	1	1
9	9	1	0	0	0
10	10	1	0	0	1
11	11	1	0	1	0
12	12	1	0	1	1
13	13	1	1	0	0
14	14	1	1	0	1
15	15	1	1	1	0
16	16	1	1	1	1

TIMING DIAGRAM

Generate Waveform



2. <u>Synchronous Counter</u>

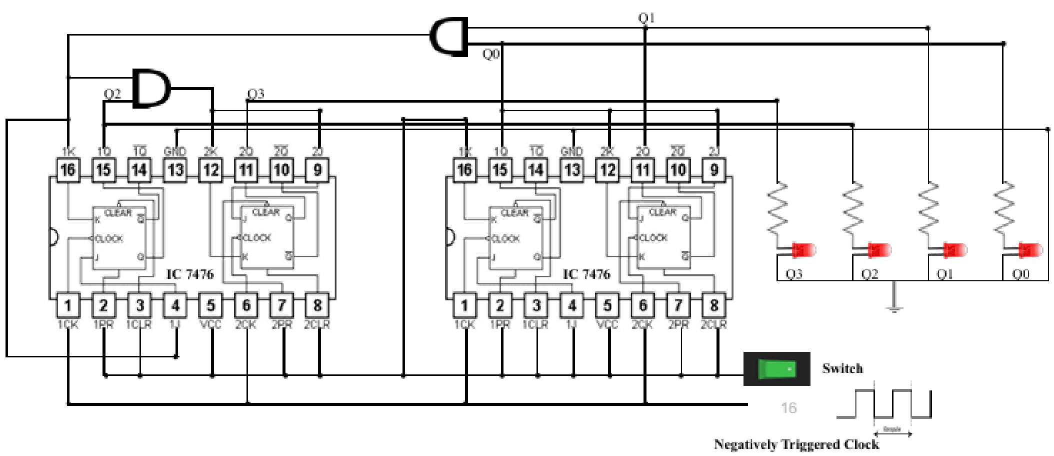
- **Simultaneous Clocking:** All the flip-flops in a synchronous counter are triggered by the same clock signal, so they all change at the same time.
- **No Ripple Effect:** Since all flip-flops get the clock signal together, there's no delay like in asynchronous counters. This allows synchronous counters to work faster.
- **More Complex:** Designing synchronous counters is more complicated because you need extra logic (like AND or OR gates) to control when each flip-flop should change based on the current count.

10/7/24, 8:06 PM Synchronous Counter

Instructions

4-Bit Synchronous Parallel Counter using J-K Flip-Flop

Print



TRUTH TABLE

Serial No.	Clock	Q3	Q2	Q1	Q0
1	1	0	0	0	0
2	2	0	0	0	1
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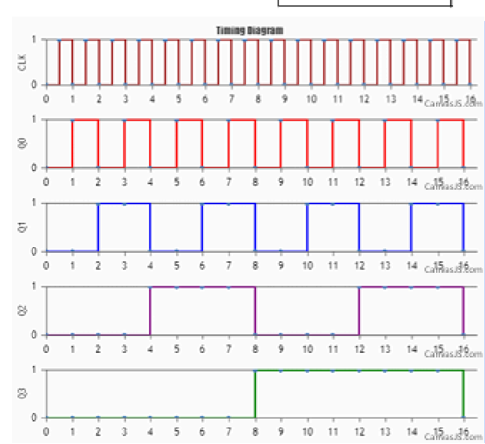
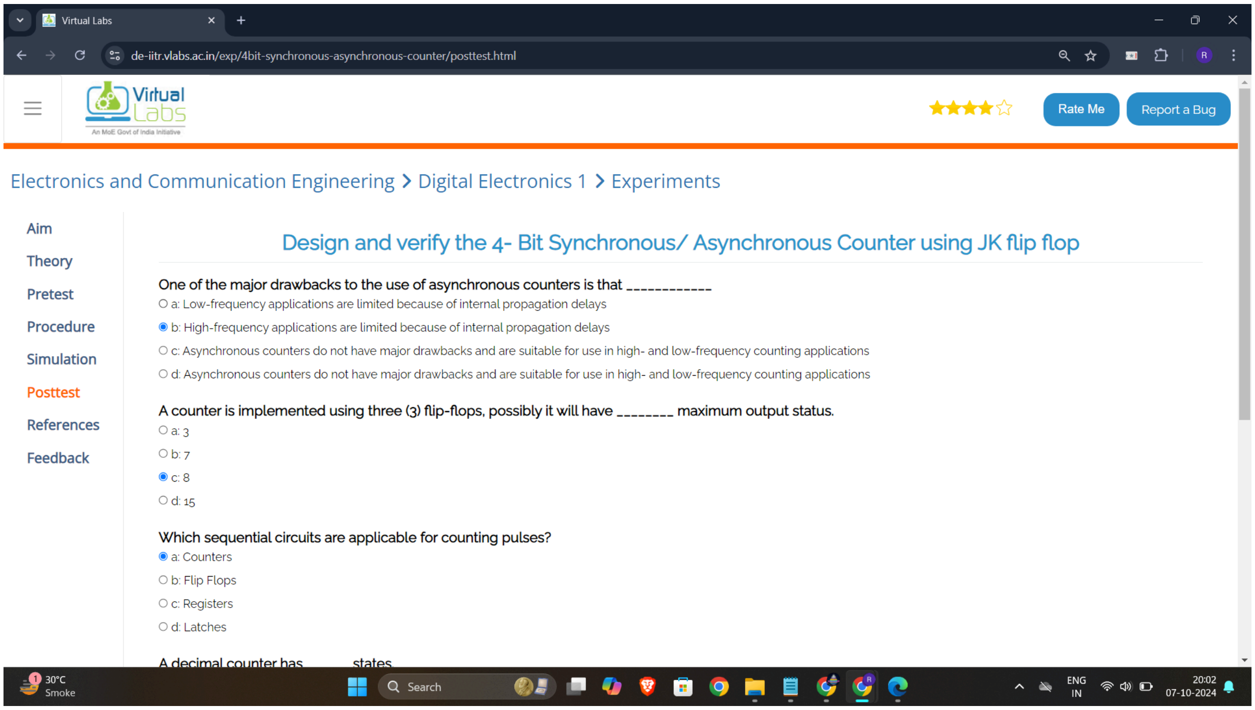
5	5	0	1	0	0
6	6	0	1	0	1
7	7	0	1	1	0
8	8	0	1	1	1
9	9	1	0	0	0
10	10	1	0	0	1
11	11	1	0	1	0
12	12	1	0	1	1
13	13	1	1	0	0
14	14	1	1	0	1
15	15	1	1	1	0
16	16	1	1	1	1

TIMING DIAGRAM

Generate Waveform



Post-test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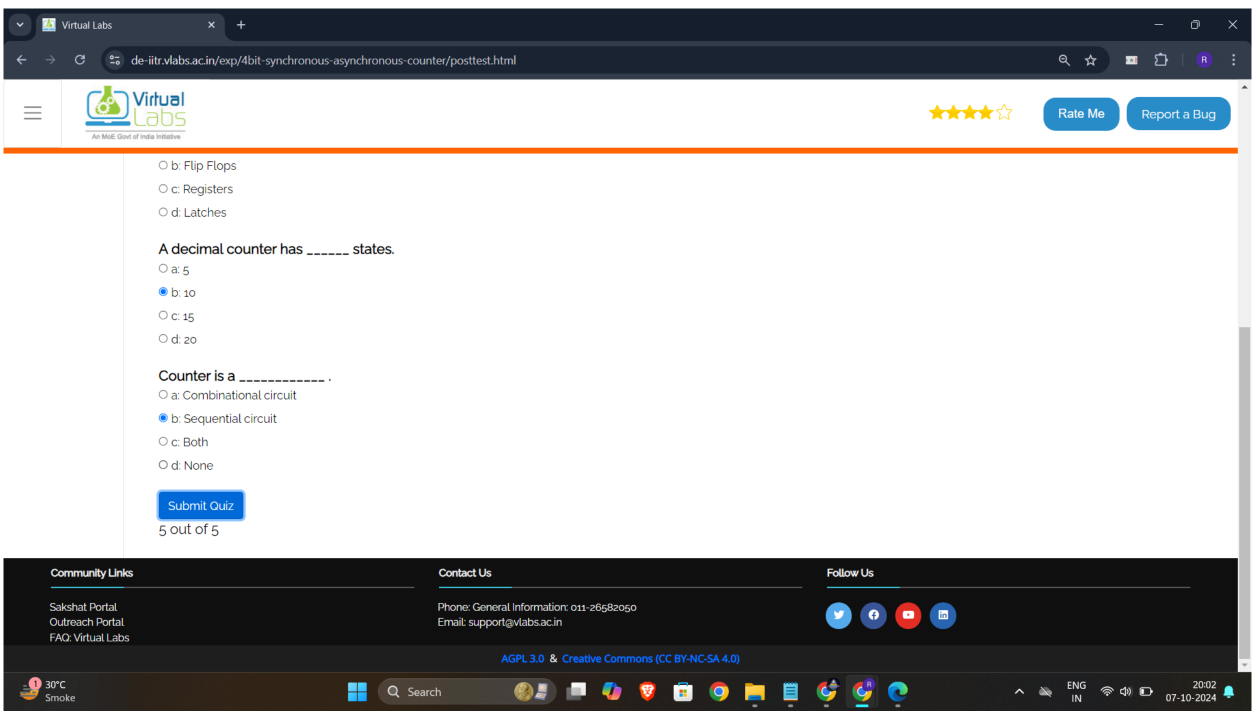
Electronics and Communication Engineering > Digital Electronics 1 > Experiments
Aim
Theory
Pretest
Procedure
Simulation
Posttest
References
Feedback
Design and verify the 4- Bit Synchronous/ Asynchronous Counter using JK flip flop
One of the major drawbacks to the use of asynchronous counters is that ____________
a: Low-frequency applications are limited because of internal propagation delays
b: High-frequency applications are limited because of internal propagation delays
c: Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
d: Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
A counter is implemented using three (3) flip-flops, possibly it will have ________ maximum output status.
a: 3
b: 7
c: 8
d: 15
Which sequential circuits are applicable for counting pulses?
a: Counters
b: Flip Flops
c: Registers
d: Latches
A decimal counter has ______ states.
30°C
Smoke
Search
ENG
IN
20:02
07-10-2024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b: Flip Flops
c: Registers
d: Latches
A decimal counter has ______ states.
a: 5
b: 10
c: 15
d: 20
Counter is a ____________ .
a: Combinational circuit
b: Sequential circuit
c: Both
d: None
Submit Quiz
5 out of 5
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