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Batch : SY-IT(B3)
Subject : Digital Systems IA2 : Subtask 1
Virtual lab: https://de-iitr.vlabs.ac.in/exp/4bit-sipo-shift-register/index.html

Design and Verify the 4-Bit Serial In - Parallel Out Shift Registers.

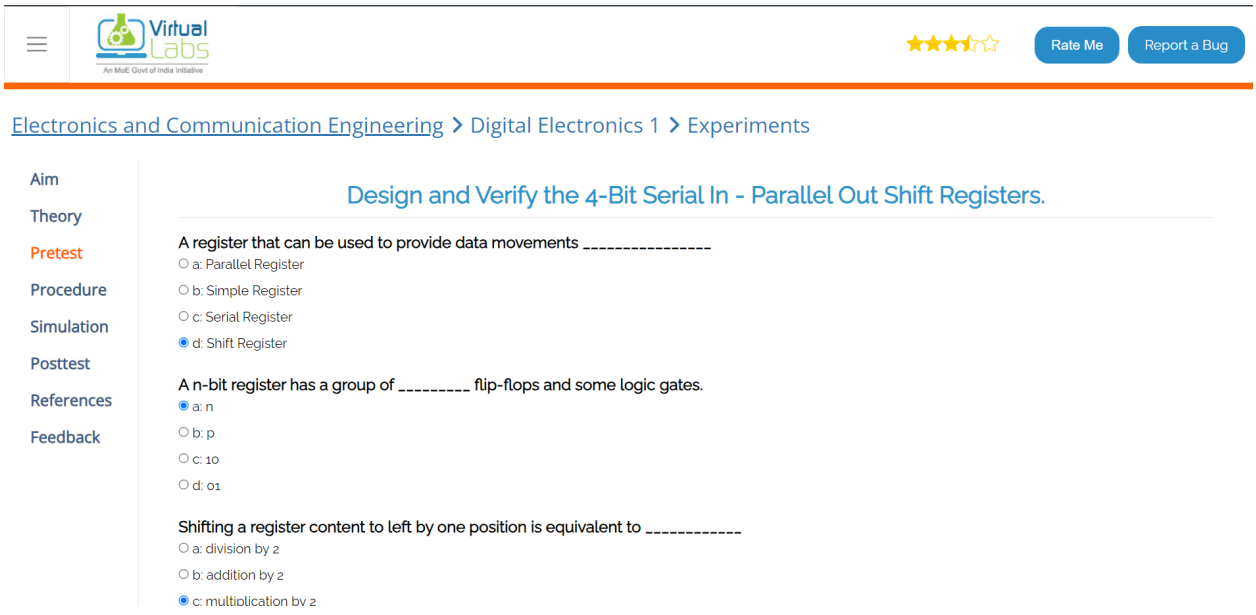
Aim :

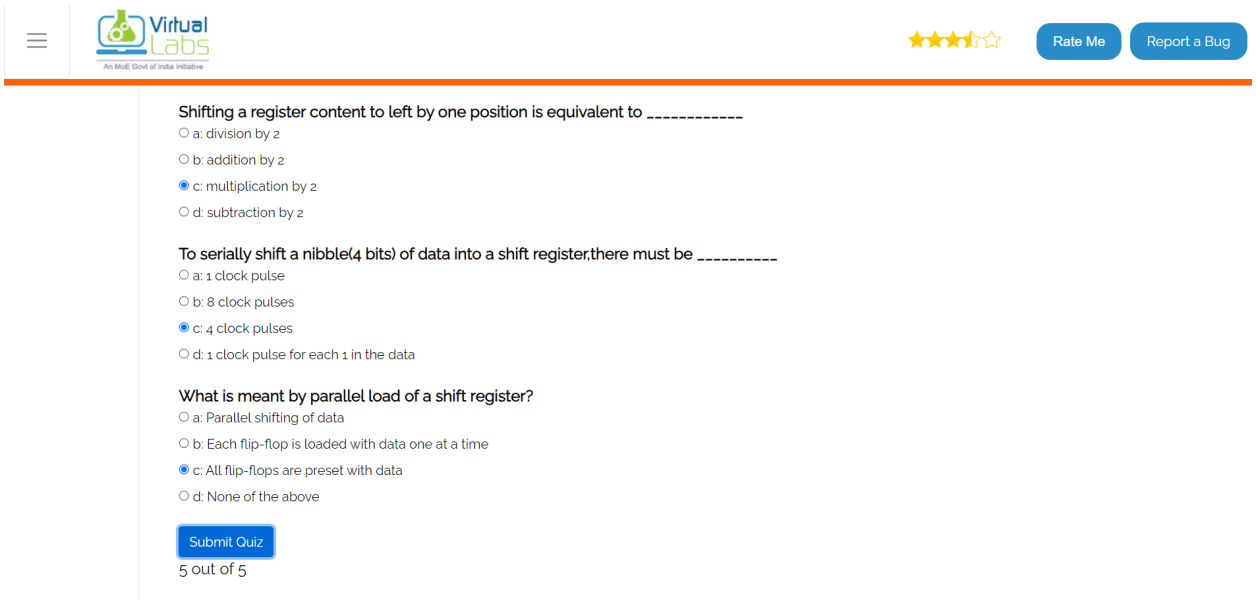
To analyse the circuit and truth table of 4-bit SIPO (serial input parallel output) shift register by using IC 7474 (D flip flop).

Theory :

In a Serial In Parallel Out (SIPO) shift register, data is entered one bit at a time and retrieved all at once in parallel. The first bit goes into the first flip-flop, and with each clock pulse, the data shifts to the next flip-flop while a new bit is added. The register is first cleared, and as each clock pulse comes in, the bits keep moving through the register until the entire data is stored across all the flip-flops. After n clock pulses, the n-bit input data is available as a parallel output. This process works for both right-shift and left-shift registers; the only difference is the direction in which the data moves.

Pretest :

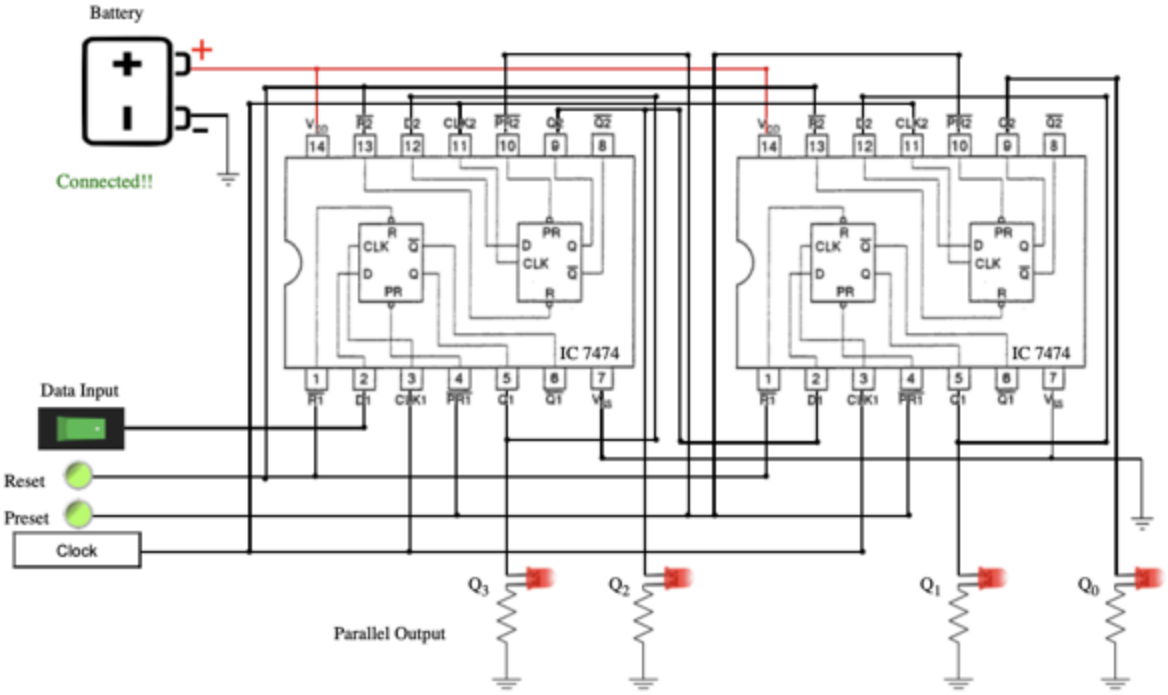




Justification of Pretest :

1. A shift register is used to move data either bit-by-bit (serially) or all at once (in parallel) by shifting its contents left or right.
2. An n-bit register has n flip-flops, where each flip-flop stores one bit of data, and logic gates control how it operates.
3. Shifting binary data left by one place multiplies the number by two because each bit moves to a higher value position.
4. Each clock pulse shifts one bit of data into the register, so it takes four clock pulses to fully load a 4-bit value (nibble).
5. Parallel loading means all flip-flops get data at once, unlike serial loading, where data is loaded one bit at a time.

Simulation :



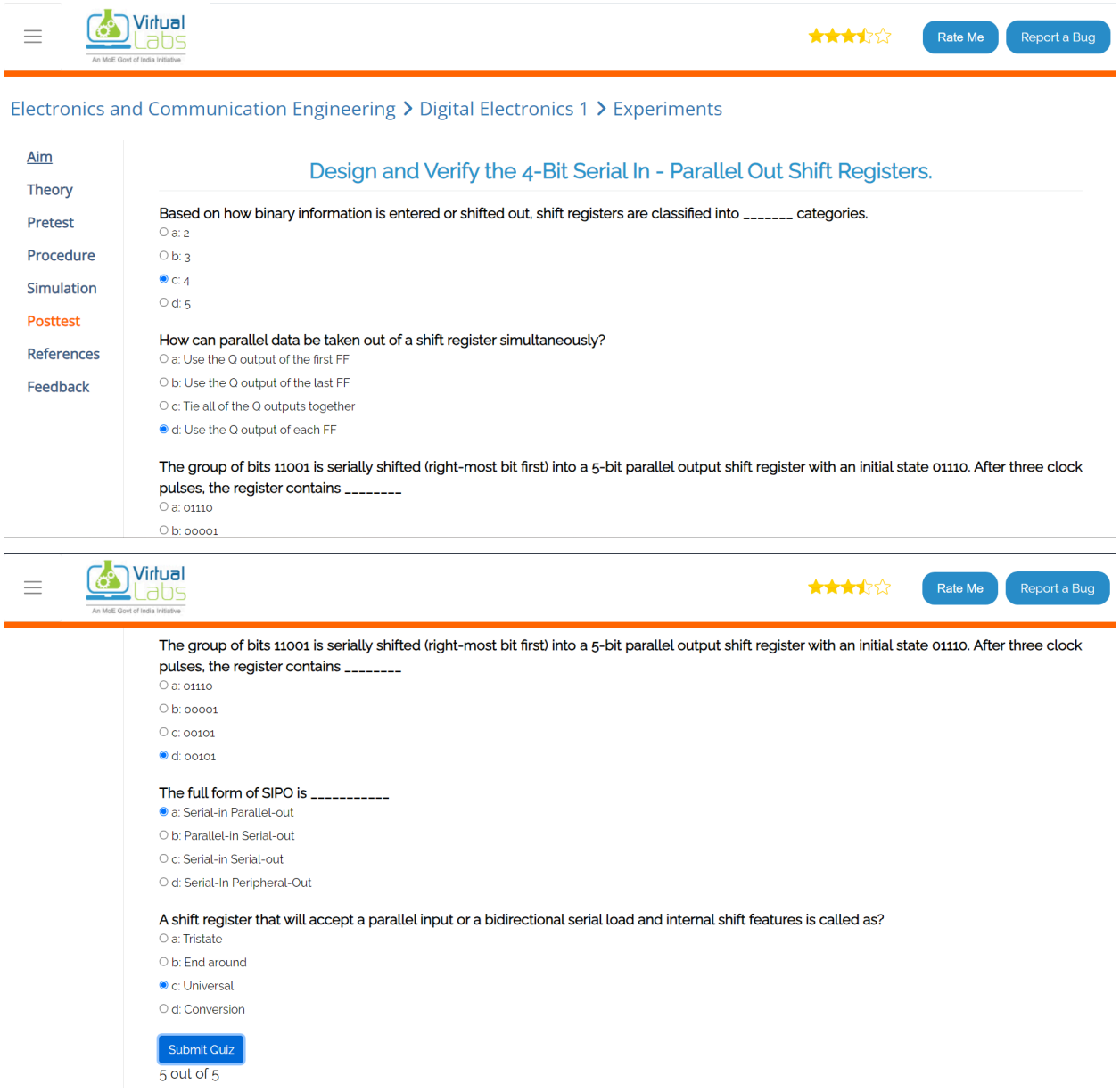
TRUTH TABLE

Serial No.	Clock	Data Input	Q_3	Q_2	Q_1	Q_0
1	1	1	1	0	0	0
2	2	1	1	1	0	0
3	3	1	1	1	1	0
4	4	1	1	1	1	1

Simulation Explanation :

1. **Power Supply Setup:** The circuit runs on a +5V supply, with the Reset pin ensuring the flip-flops are prepared for data input.
2. **Data Input and Shifting:** Data is fed serially at the input (D), and with each clock pulse, the data moves through the flip-flops.
3. **Initial Shift:** On the first clock pulse, the data is visible at Q3, indicated by the LED.
4. **Continuous Shifting:** With each additional clock pulse, data shifts from Q3 to Q2, and new input appears at Q3. This continues until all 4 bits are shifted, reaching Q0.
5. **Final Output:** After all 4 bits have shifted, the final states of Q3 to Q0 are displayed on the LEDs. The "Print" option saves the simulation results.

Postlab :



Conclusion :

I learned how a 4-bit Serial In Parallel Out (SIPO) shift register works by analyzing its circuit and truth table using IC 7474. I understood how data is shifted through the flip-flops with each clock pulse, moving one bit at a time and how the parallel output is retrieved. This helped me grasp how binary data is stored and transferred in digital circuits, as well as the difference between serial and parallel data loading.