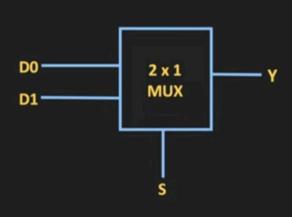
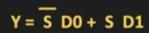
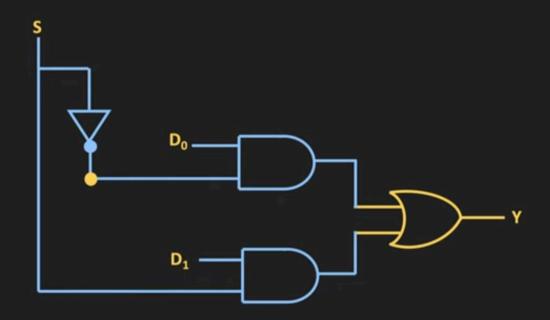
2 x 1 Multiplexer



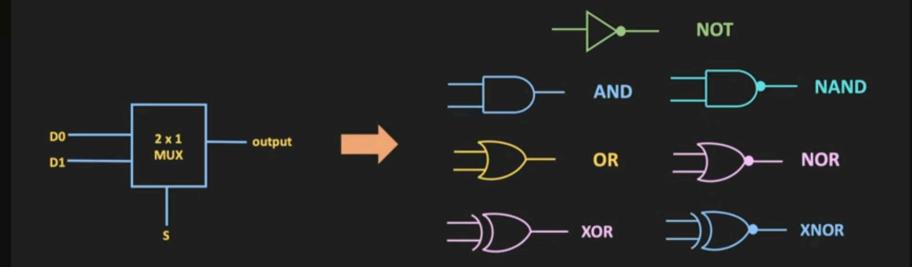








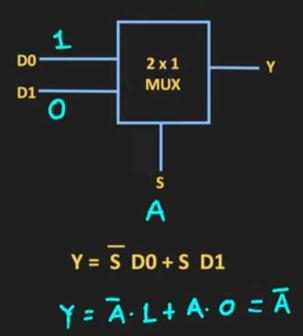
Logic Gates using Multiplexer







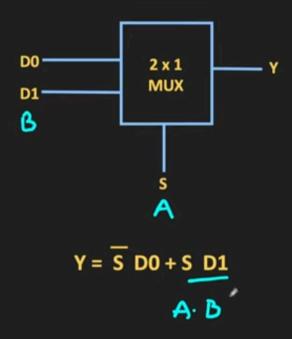
NOT gate using 2 x 1 MUX





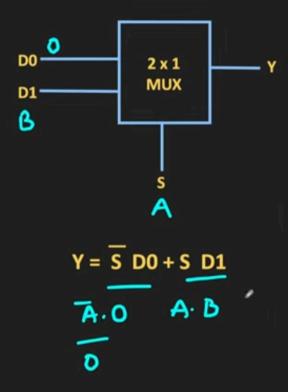


AND gate using 2 x 1 MUX



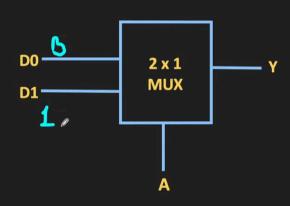


AND gate using 2 x 1 MUX





OR gate using 2 x 1 MUX



$$Y = \overline{S} D0 + S D1$$

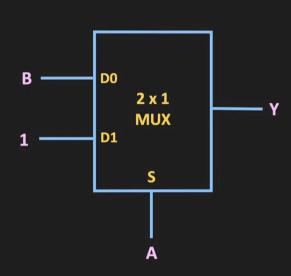


Truth Table

Α	В	Υ	
0	0	0	
0	1	1	Y = B
1	0	1	
1	1	1	Y = 1



OR gate using 2 x 1 MUX



$$\begin{array}{c}
A \\
B
\end{array}$$

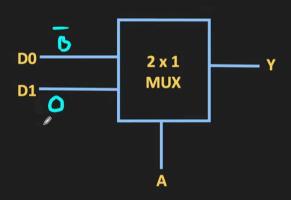
$$Y = A + B$$

$$Y = \overline{S} DO + S D1 = \overline{A} \cdot \overline{B} + A \cdot 1 = A + \overline{A} B$$

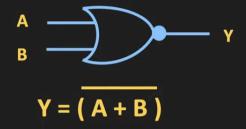
$$= (A + \overline{A}) \cdot (A + \overline{B})$$

-W-

NOR gate using 2 x 1 MUX



$$Y = \overline{S} D0 + S D1$$

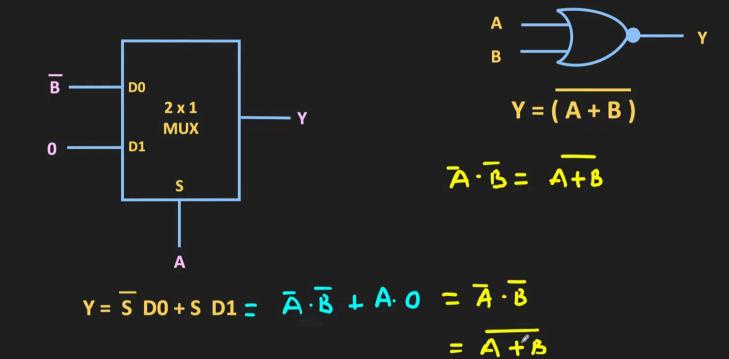


Truth Table

Α	В	Υ	
0	0	1	, <u>-</u>
0	1	0	Y = B
1	0	0	200 20
1	1	0	Y = 0

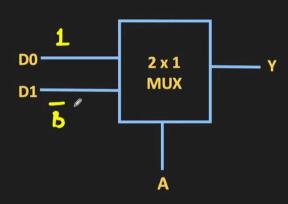


NOR gate using 2 x 1 MUX

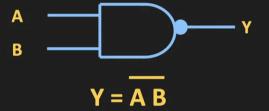




NAND gate using 2 x 1 MUX



$$Y = \overline{S} D0 + S D1$$

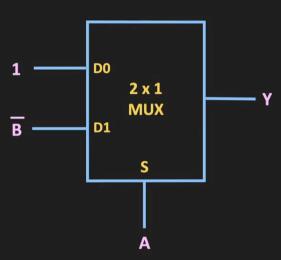


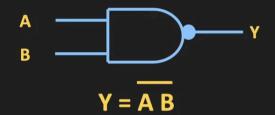
Truth Table

Α	В	Y	
0	0	1	Y = 1
0	1	1	
1	0	1	=
1	1	0	Y = B



NAND gate using 2 x 1 MUX





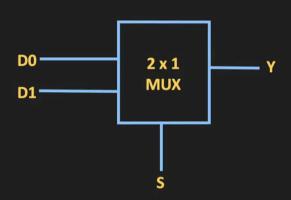
*Correction It should be (AB)'

$$Y = \overline{S} DO + S D1 = \overline{A} \cdot I + A \cdot \overline{B} = (\overline{A} + A) \cdot (\overline{A} + \overline{B})$$

$$= \overline{A} + \overline{B} = \overline{A} \cdot \overline{B}$$

-W-

XOR gate using 2 x 1 MUX

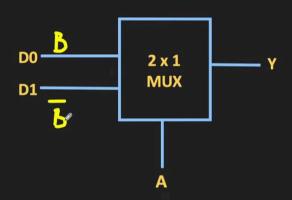


$$Y = \overline{S} D0 + S D1$$

A
B
$$Y = A \overline{B} + \overline{A} B$$
 $Y = A \oplus B$



XOR gate using 2 x 1 MUX



$$Y = \overline{S} D0 + S D1$$

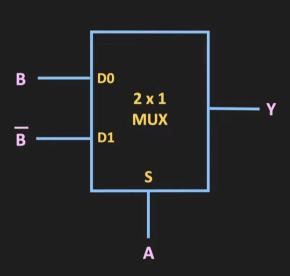


Truth Table

Α	В	Y	
0	0	0	Y = B
0	1	1	5
1	0	1	-
1	1_	0	Y = B



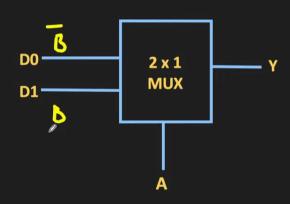
XOR gate using 2 x 1 MUX



$$Y = \overline{S} DO + S D1 = \overline{A} \cdot B + A \cdot \overline{B} = A \oplus B$$



XNOR gate using 2 x 1 MUX



$$Y = \overline{S} D0 + S D1$$



Truth Table

Α	В	Υ	
0	0	1	v -
0	1	0	Y = B
1	0	0	Y = B
1	1	1	I – D



XNOR gate using 2 x 1 MUX

