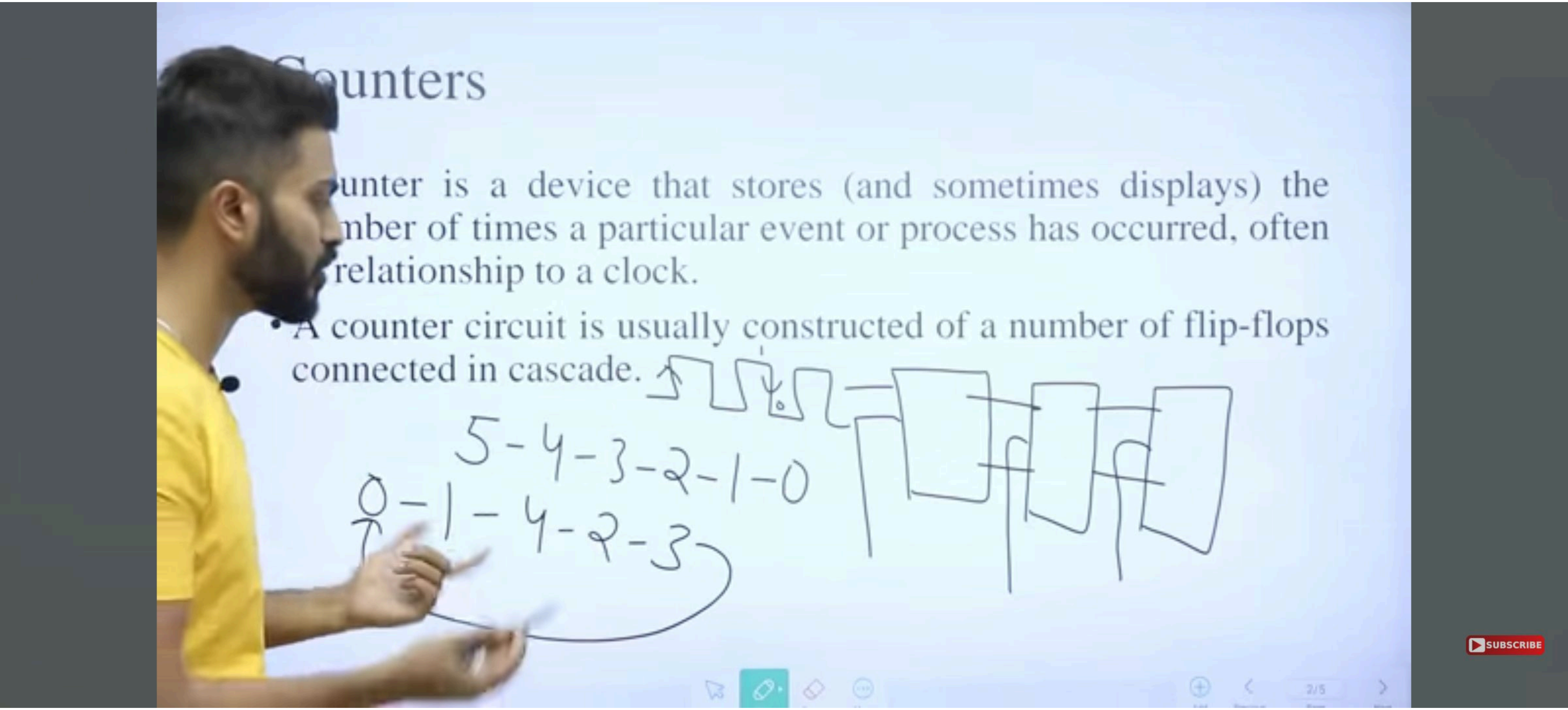
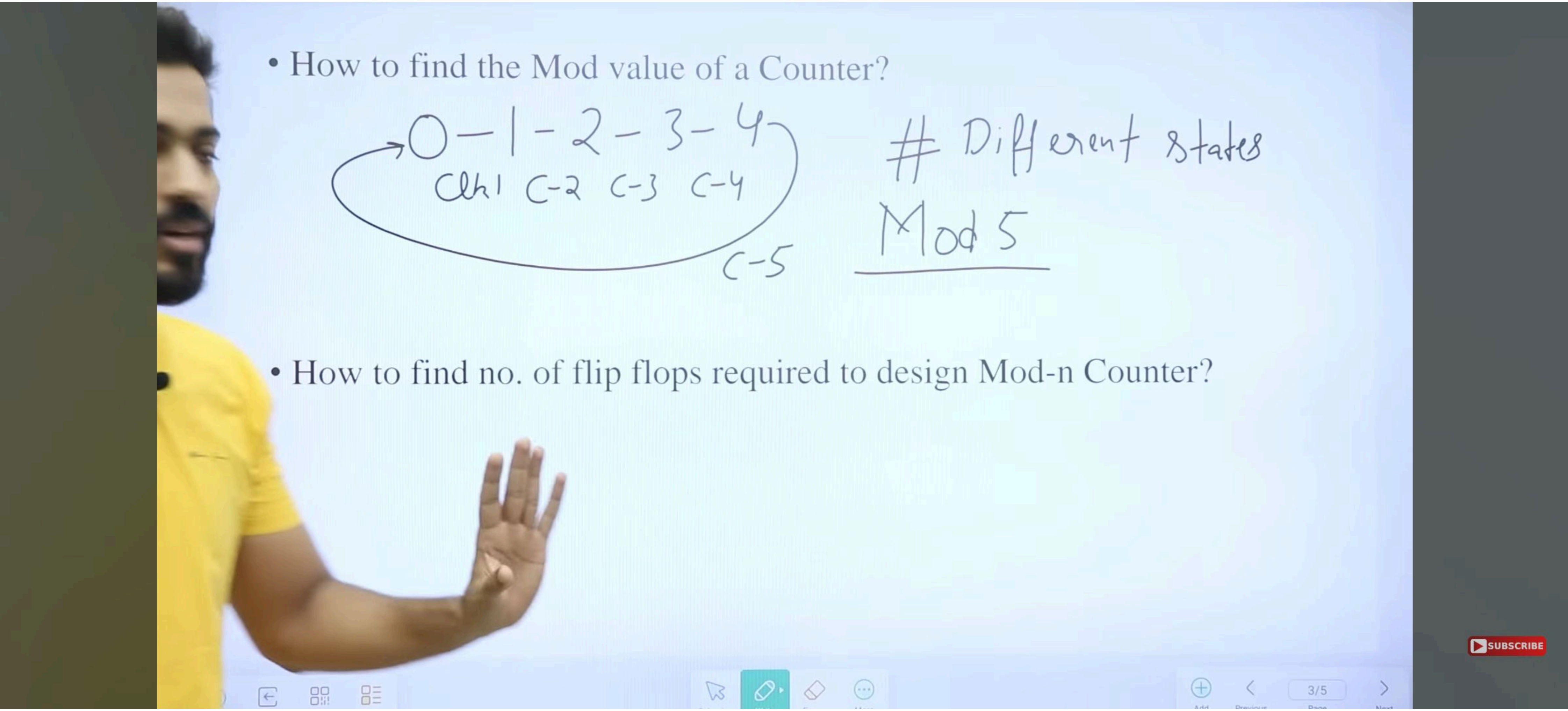
Counters

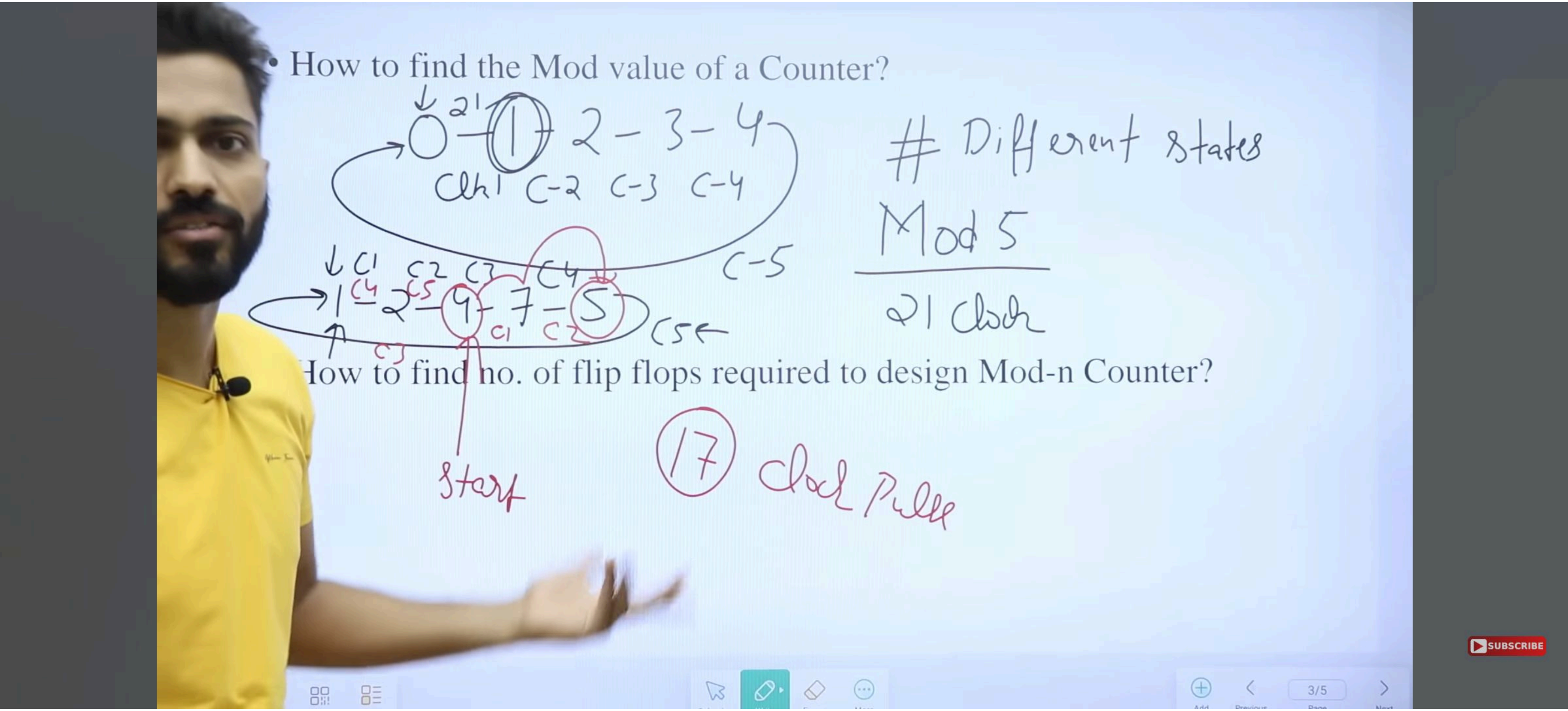
- Counter is a device that stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock.
- A counter circuit is usually constructed of a number of flip-flops connected in cascade.


ounters
unter is a device that stores (and sometimes displays) the
mber of times a particular event or process has occurred, often
relationship to a clock.
A counter circuit is usually constructed of a number of flip-flops
connected in cascade.
5-4-3-2-1-0
0-1-4-2-3
SUBSCRIBE
2/5

- How to find the Mod value of a Counter?

- How to find no. of flip flops required to design Mod-n Counter?


• How to find the Mod value of a Counter?
0 – 1 – 2 – 3 – 4
Clk1 C-2 C-3 C-4
C-5
Different states
Mod 5
• How to find no. of flip flops required to design Mod-n Counter?
3/5
SUBSCRIBE


• How to find the Mod value of a Counter?
0 — 1 — 2 — 3 — 4
Clk1 C-2 C-3 C-4
C-5
Different states
Mod 5
21 Clock
1 — 2 — 4 — 7 — 5
How to find no. of flip flops required to design Mod-n Counter?
17 Clock Pulse
Start
3/5
SUBSCRIBE

- How to find the Mod value of a Counter?

0 - 1 - 2 - 3 - 4

Clk1 C-2 C-3 C-4

C-5

Different states

Mod 5

21 Clock

1 - 2 - 4 - 7 - 5

- How to find no. of flip flops required to design Mod-n Counter?

$2^n \ge M$

$2^n \ge 5$

2^3

$8 \ge 5$

MOD-5

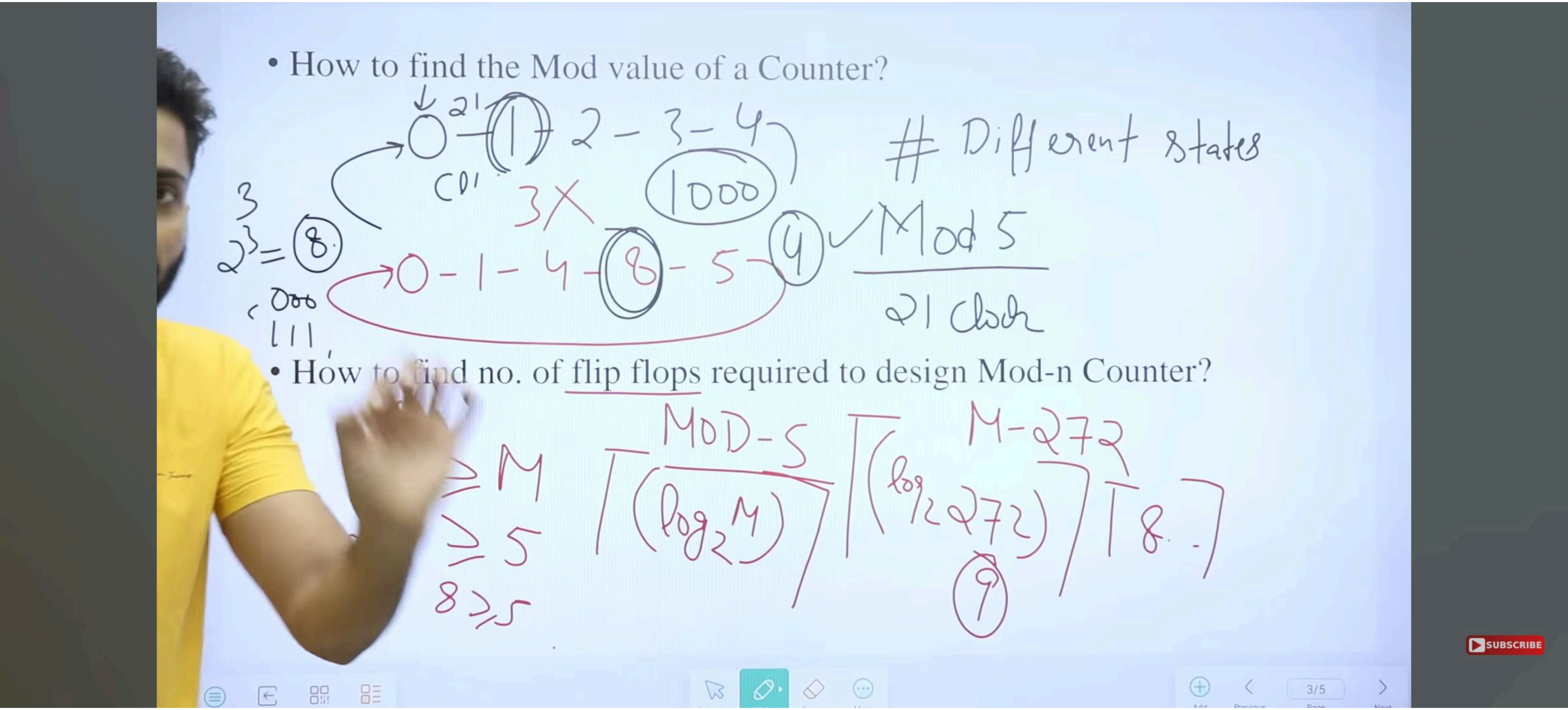
$\lceil \log_2 M \rceil$

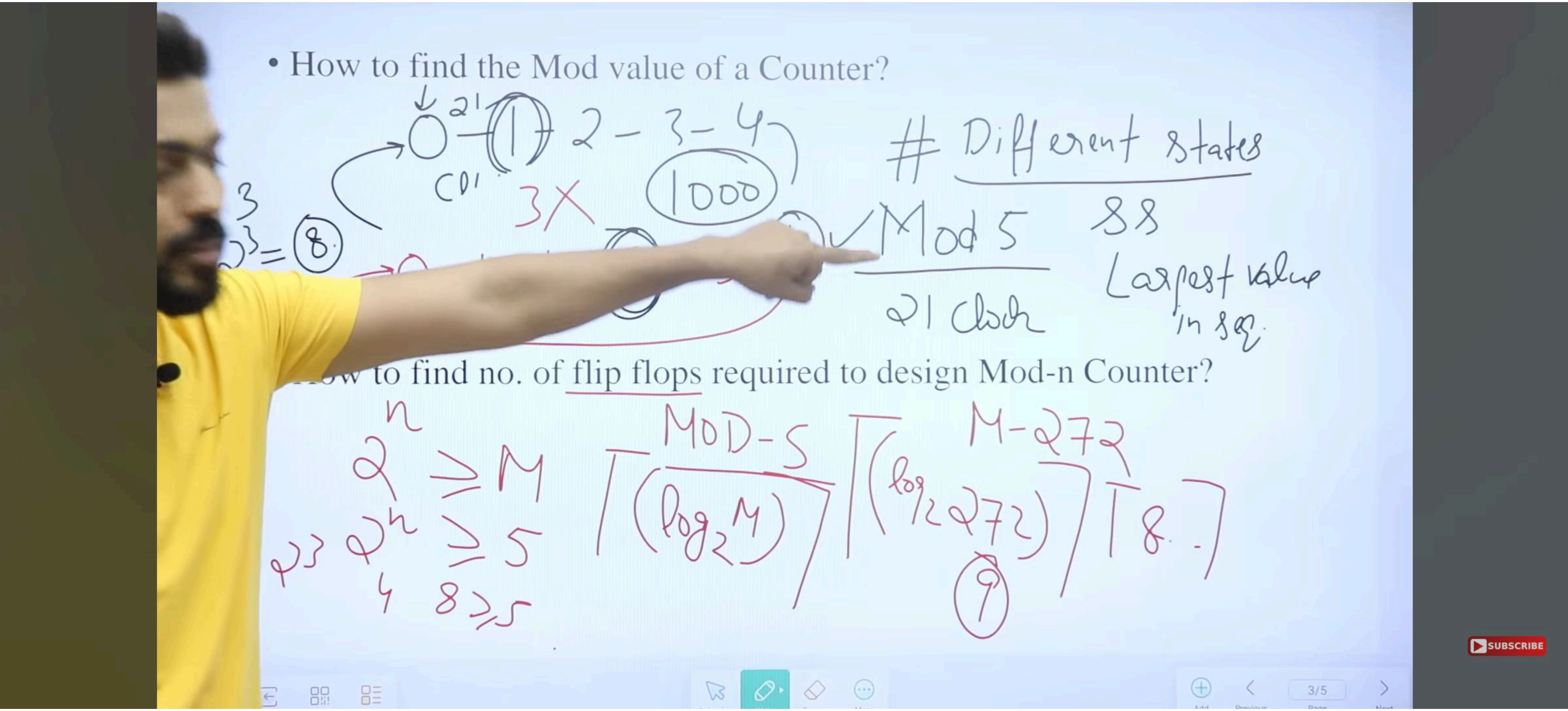
M-272

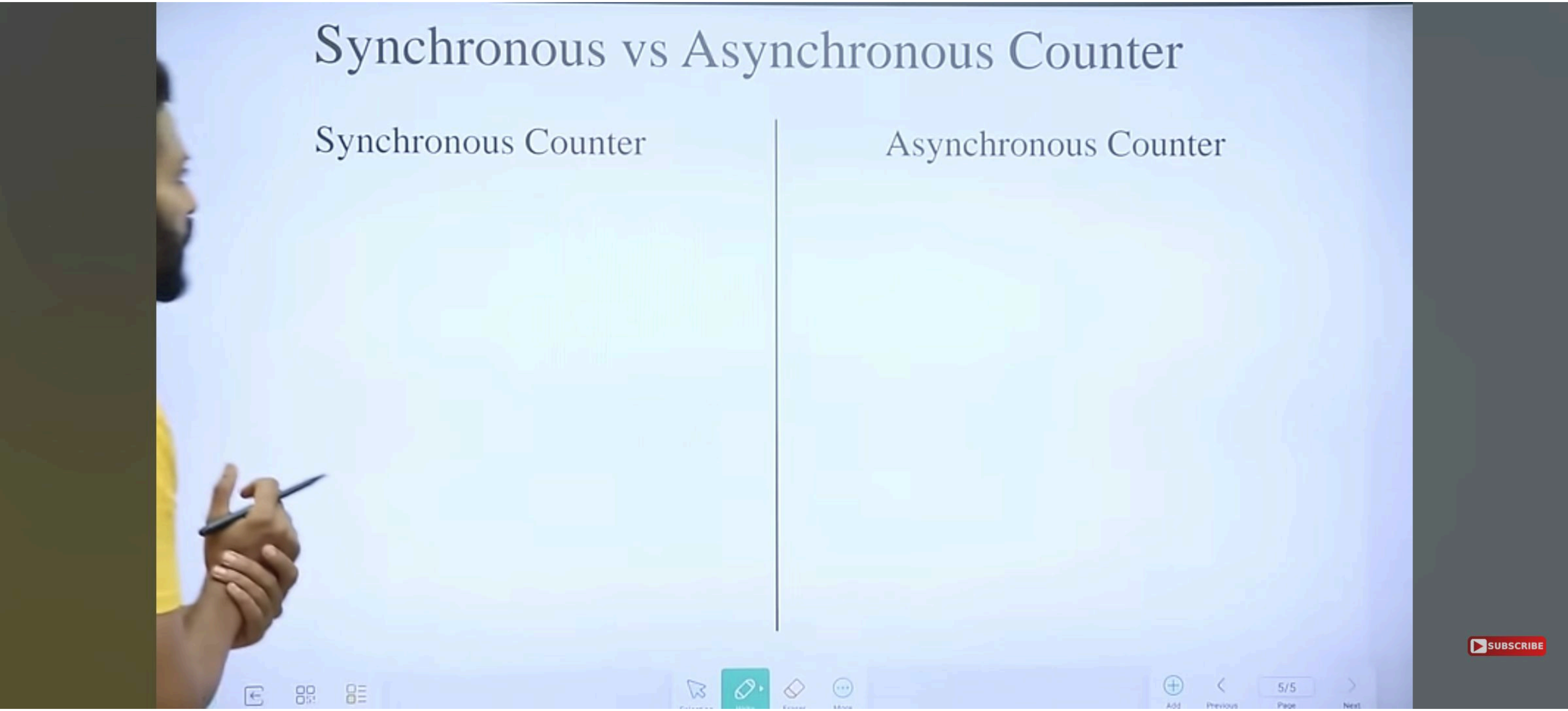
$\lceil \log_2 272 \rceil$

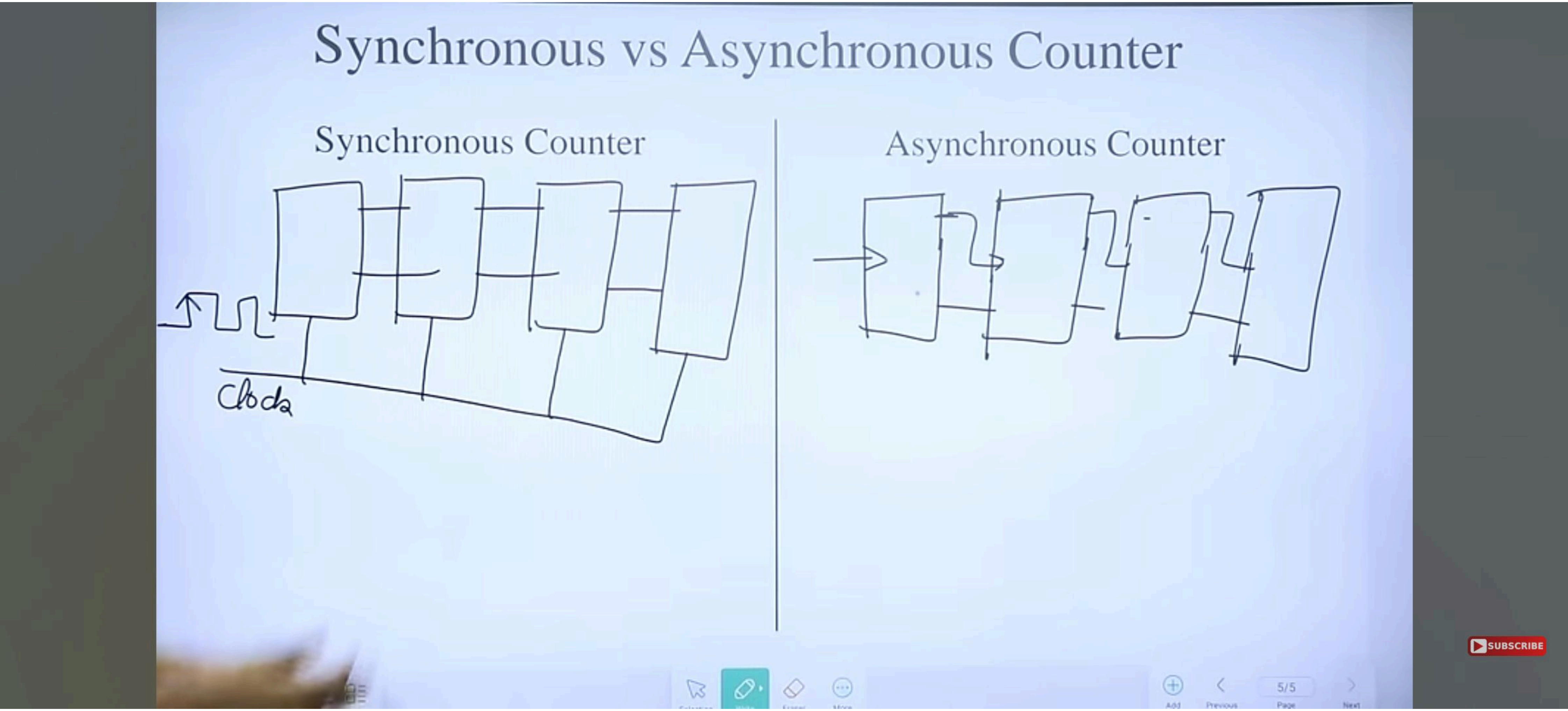
9

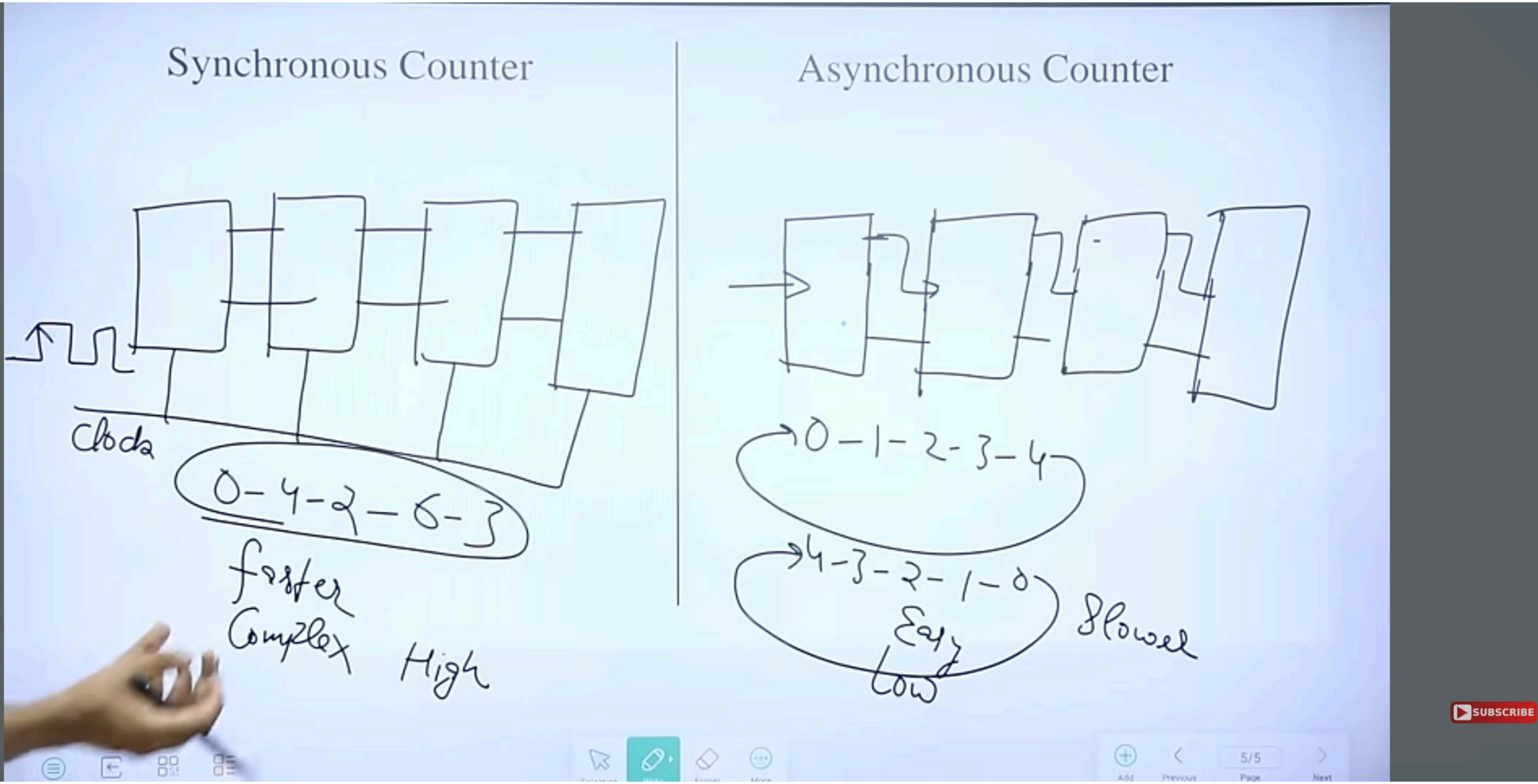
$\lceil 8.. \rceil$

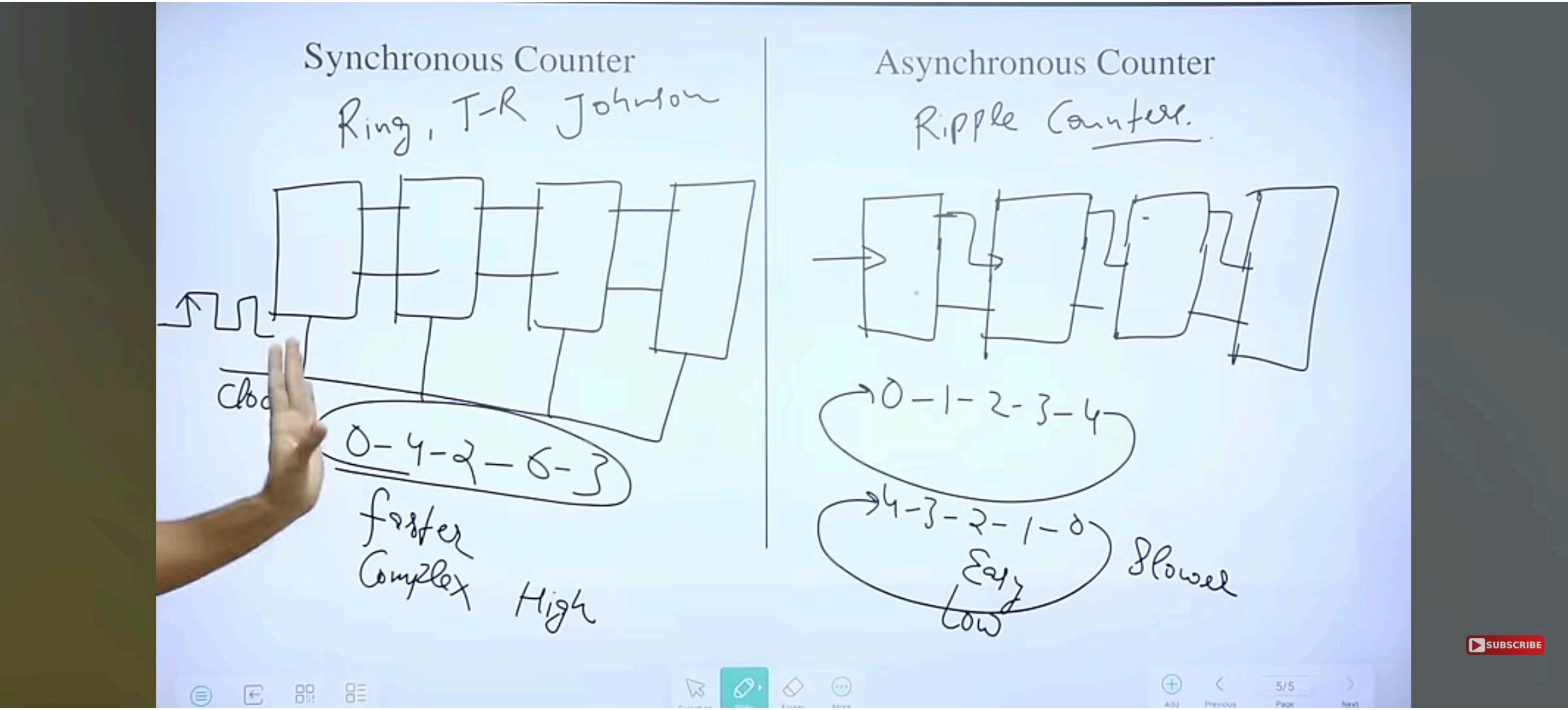

• How to find the Mod value of a Counter?
0 – 1 – 2 – 3 – 4
1000
Different states
$2^3 = 8$
0 – 1 – 4 – 8 – 5 – 9
Mod 5
21 Clock
• How to find no. of flip flops required to design Mod-n Counter?
MOD-5
$\lceil \log_2 M \rceil$
M-272
$\lceil \log_2 272 \rceil$
9
$8 \geq 5$
SUBSCRIBE
3/5


• How to find the Mod value of a Counter?
1000
Different states
Mod 5
21 Clock
Largest value in seq.
w to find no. of flip flops required to design Mod-n Counter?
MOD-5
M-272
SUBSCRIBE
3/5


Synchronous vs Asynchronous Counter
Synchronous Counter
Asynchronous Counter
5/5
SUBSCRIBE


Synchronous vs Asynchronous Counter
Synchronous Counter
Asynchronous Counter
Clock
SUBSCRIBE
5/5


Synchronous Counter
Asynchronous Counter
Clock
0-4-2-6-3
faster
Complex
High
0-1-2-3-4
4-3-2-1-0
Easy
Low
Slower
5/5
SUBSCRIBE


Synchronous Counter
Ring, T-R Johnson
0-4-2-6-3
faster
Complex
High
Asynchronous Counter
Ripple Counter.
0-1-2-3-4
4-3-2-1-0
Easy
Low
Slower
SUBSCRIBE
5/5

Design Synchronous counter

0 - 1 - 3 - 2

2 ff

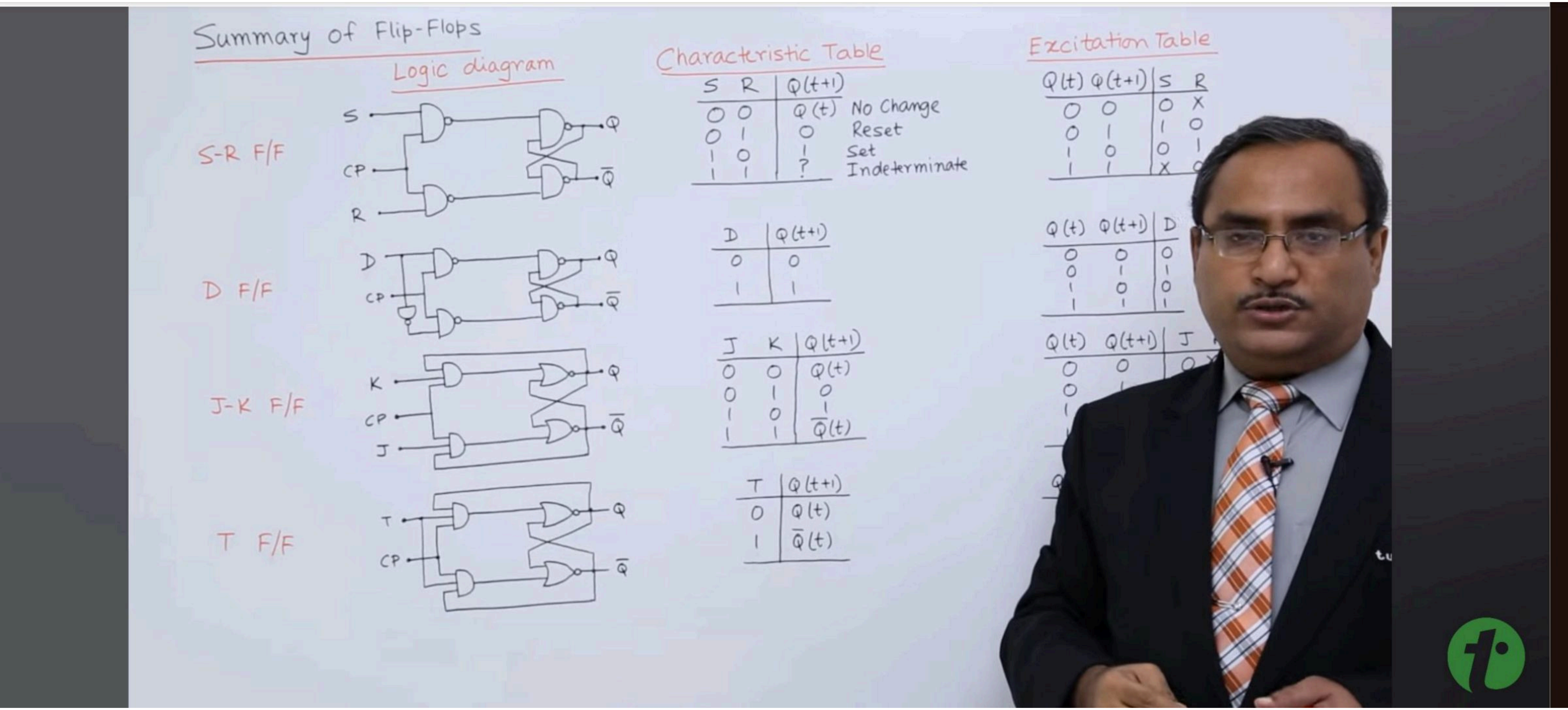
$0 - 1 - 3 - 2$

2 ff

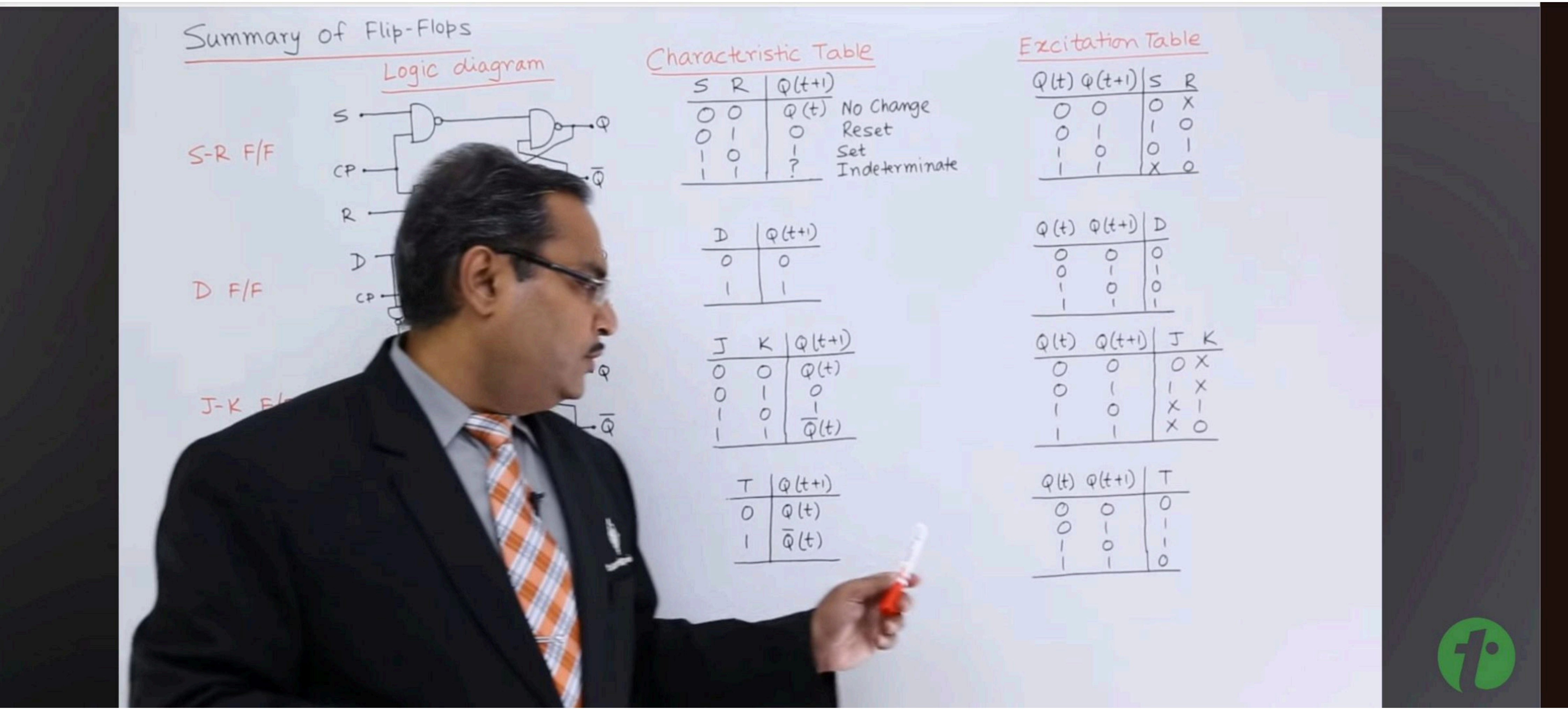
PS		Next state	
Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	1
1	0	0	0
1	1	1	0

Here we are using D flipflop

And we will make use of its excitation table



Summary of Flip-Flops
Logic diagram
Characteristic Table
Excitation Table
S-R F/F
D F/F
J-K F/F
T F/F
S
CP
R
Q
Q̄
D
K
J
T
S R | Q(t+1)
0 0 | Q(t) No Change
0 1 | 0 Reset
1 0 | 1 Set
1 1 | ? Indeterminate
D | Q(t+1)
0 | 0
1 | 1
J K | Q(t+1)
0 0 | Q(t)
0 1 | 0
1 0 | 1
1 1 | Q̄(t)
T | Q(t+1)
0 | Q(t)
1 | Q̄(t)
Q(t) Q(t+1) | S R
0 0 | 0 X
0 1 | 1 0
1 0 | 0 1
1 1 | X
Q(t) Q(t+1) | D
0 0 | 0
0 1 | 1
1 0 | 0
1 1 | 1
Q(t) Q(t+1) | J


Summary of Flip-Flops
Logic diagram
Characteristic Table
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S-R F/F
D F/F
S
CP
R
Q
Q̄
D
CP
S R | Q(t+1)
0 0 | Q(t) No Change
0 1 | 0 Reset
1 0 | 1 Set
1 1 | ? Indeterminate
Q(t) Q(t+1) | S R
0 0 | 0 X
0 1 | 1 0
1 0 | 0 1
1 1 | X 0
D | Q(t+1)
0 | 0
1 | 1
Q(t) Q(t+1) | D
0 0 | 0
0 1 | 1
1 0 | 0
1 1 | 1
J K | Q(t+1)
0 0 | Q(t)
0 1 | 0
1 0 | 1
1 1 | Q̄(t)
Q(t) Q(t+1) | J K
0 0 | 0 X
0 1 | 1 X
1 0 | X 1
1 1 | X 0
T | Q(t+1)
0 | Q(t)
1 | Q̄(t)
Q(t) Q(t+1) | T
0 0 | 0
0 1 | 1
1 0 | 1
1 1 | 0

$0 - 1 - 3 - 2$

00	0
01	1
10	0
11	1

$0\,0\,1$ — 1
MSB LSB

$0\,0\,1$ — 4
LSB MSB

2 ff

PS		Next state			
Q_1	Q_0	Q_1^+	Q_0^+	D_1	D_0
0	0	0	1	0	
0	1	1	1	1	
1	0	0	0	0	
1	1	1	0	1	

0 - 1 - 3 - 2

00	0
01	1
10	0
11	1

0 0 1 — 1
MSB LSB

0 0 1 — 4
LSB MSB

2 ff

PS Q_1	Q_0	Next state Q_1^+	Q_0^+	D_1	D_0
0	0	0	1	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	1	1	0	1	0

$0 - 1 - 3 - 2$

2 ff

	PS Q_1	Q_0	Next state Q_1^+	Q_0^+	D_1	D_0
	0	0	0	1	0	1 –
1 –	0	1	1	1	1 –	1 –
	1	0	0	0	0	0
3 –	1	1	1	0	1 –	0

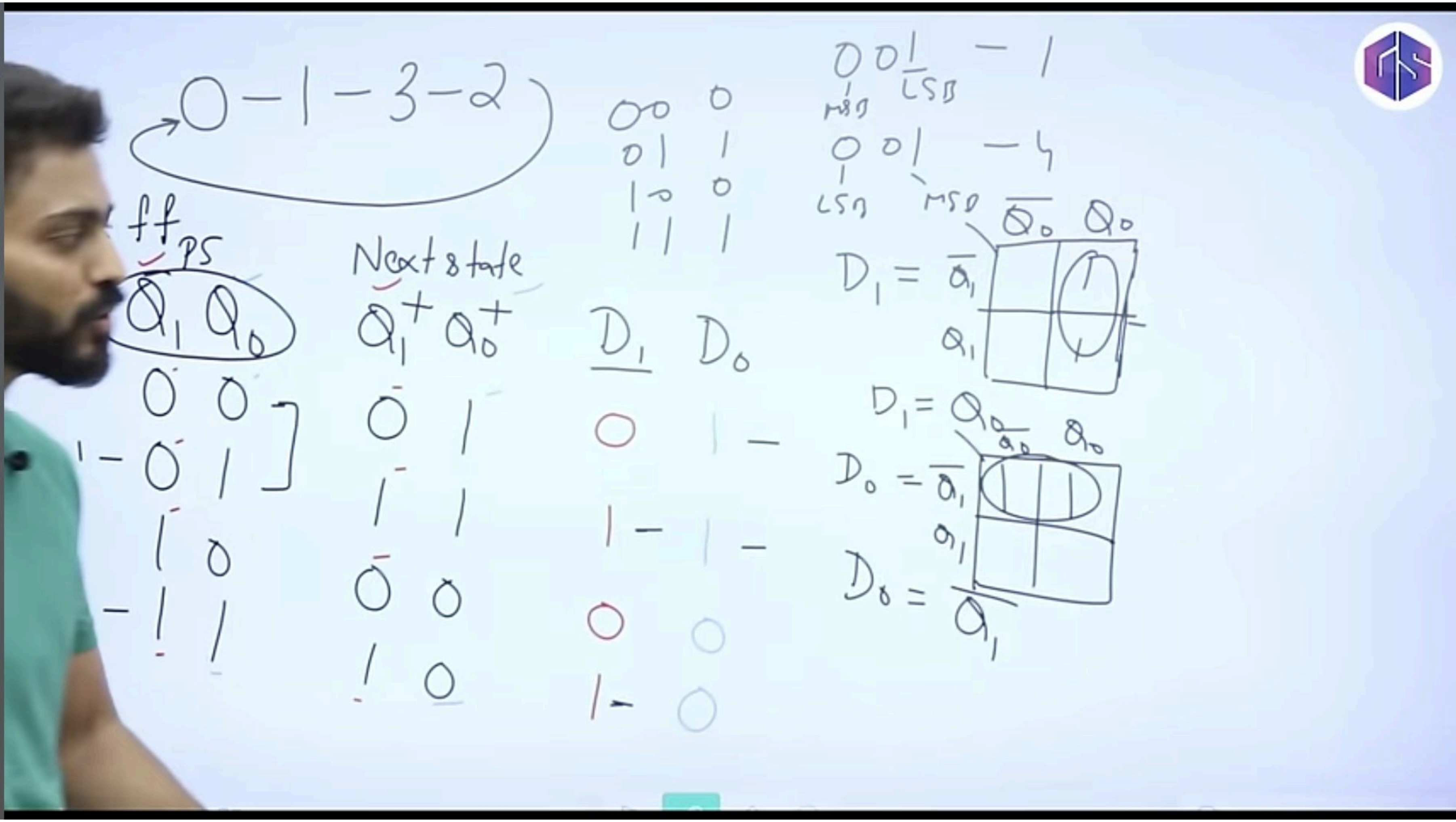
00	0
01	1
10	0
11	1

001 – 1 (MSB … LSB)

001 – 4 (LSB … MSB)

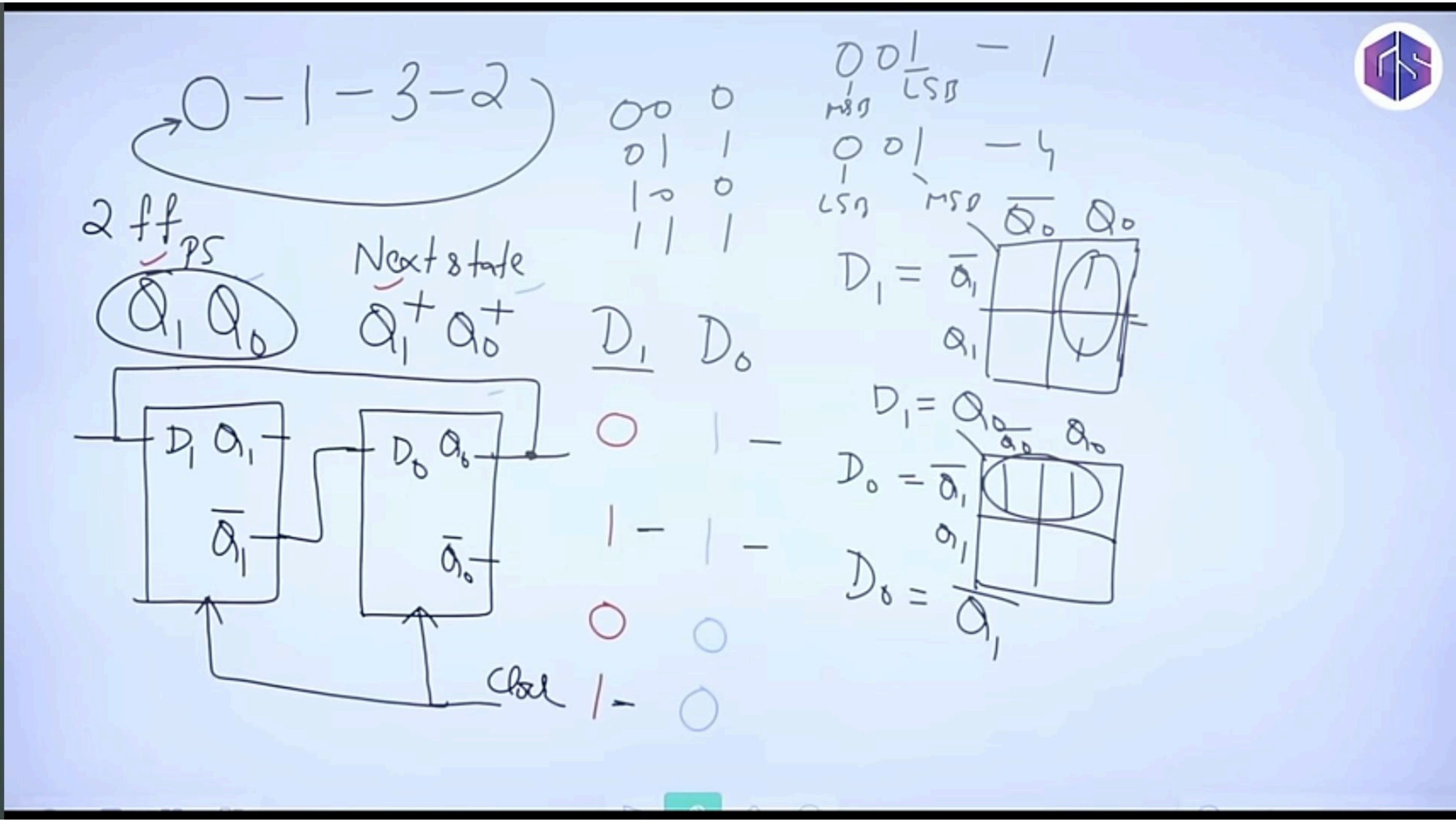
$D_1 =$

	$\overline{Q_0}$	Q_0
$\overline{Q_1}$		
Q_1		



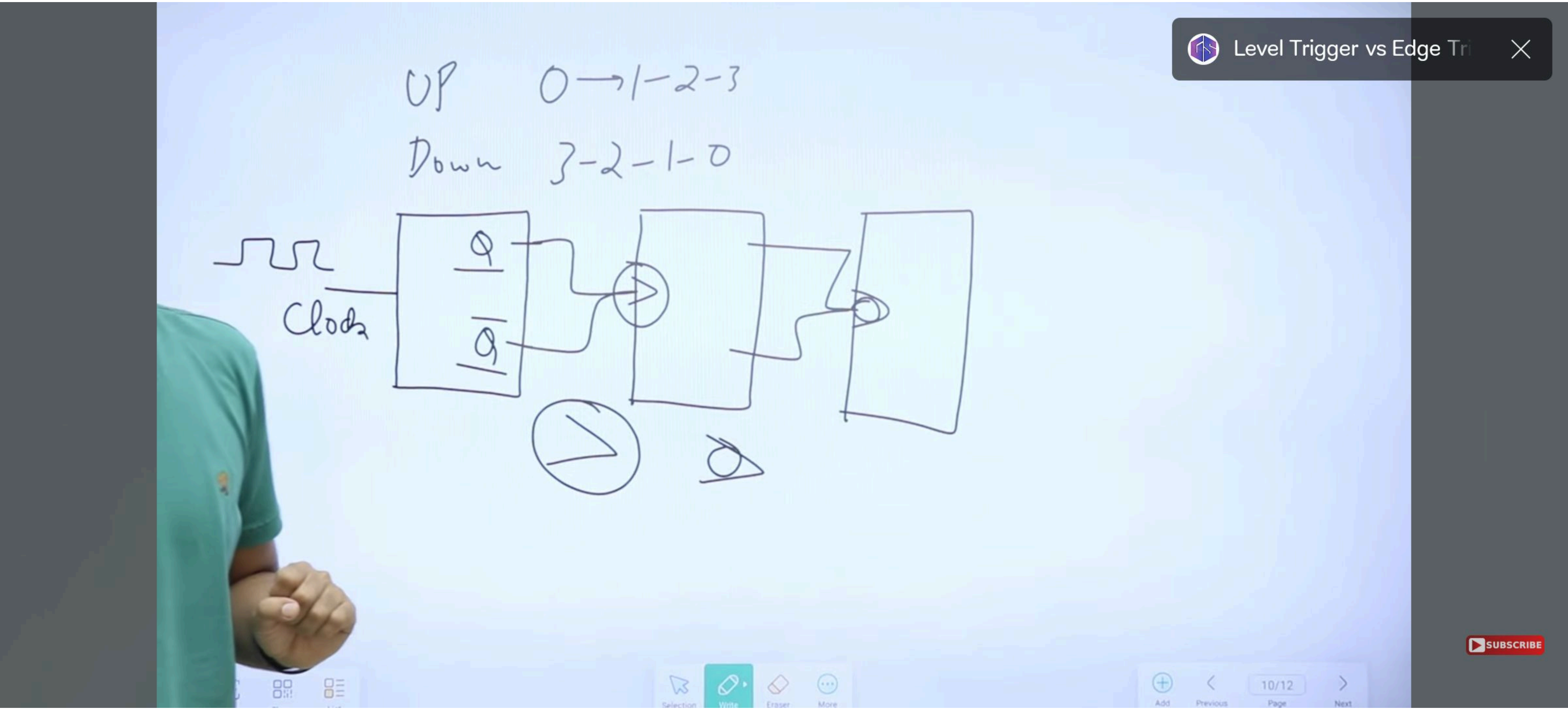
0-1-3-2
ff
PS
Next state
Q1 Q0
Q1+ Q0+
D1 D0
00 0
01 1
10 0
11 1
001 - 1
MSB
LSB
001 - 4
LSB
MSB
D1 =
D1 = Q0
D0 =
D0 =

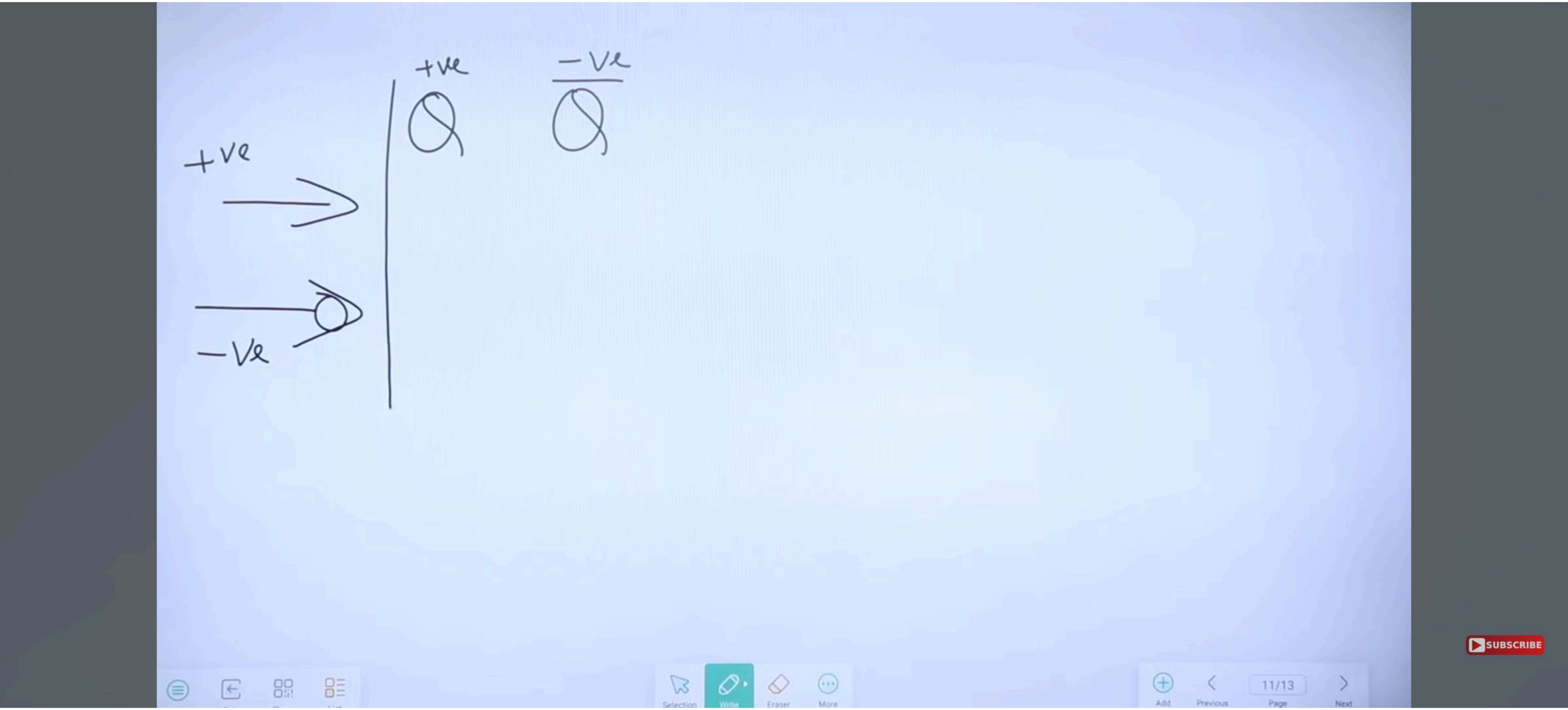
SUBSCRIBE



0 − 1 − 3 − 2
2 ff
PS
Q_1 Q_0
Next state
Q_1^+ Q_0^+
D_1 D_0
00 0
01 1
10 0
11 1
0 0 1 − 1
MSB LSB
0 0 1 − 4
LSB MSB
$D_1 = \bar{Q}_1$
$D_1 = Q_0$
$D_0 = \bar{Q}_1$
$D_0 = \bar{Q}_1$
Clk

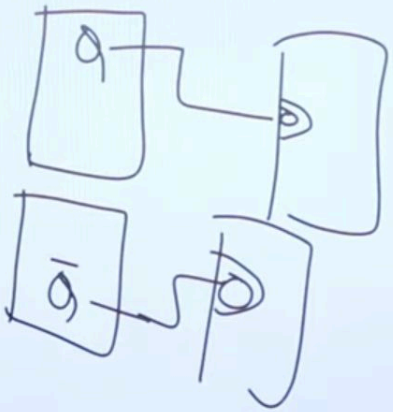
Up and Down counters


UP 0→1-2-3
Down 3-2-1-0
Q
Q
Clock
Level Trigger vs Edge Tri
SUBSCRIBE
10/12

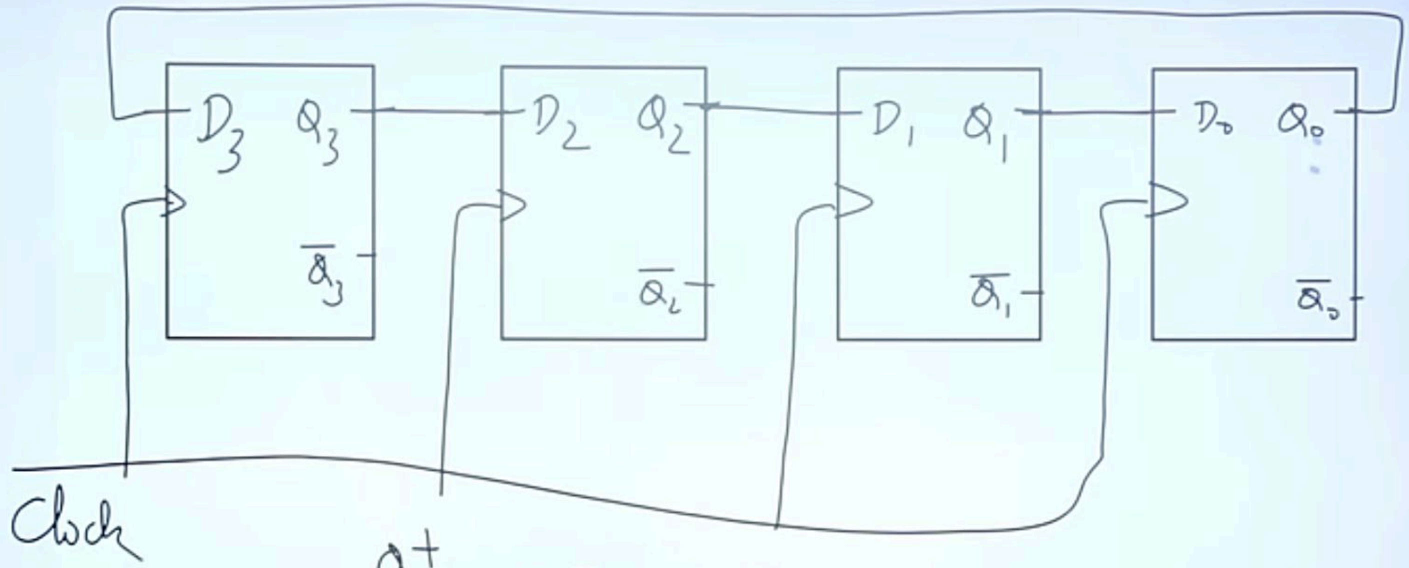

+ve
−ve
+ve
−ve
SUBSCRIBE
Selection
Write
Eraser
More
Add
Previous
11/13
Page
Next

	+ve q	−ve $\bar{q}$
+ve	Down	UP
−ve	UP	Down

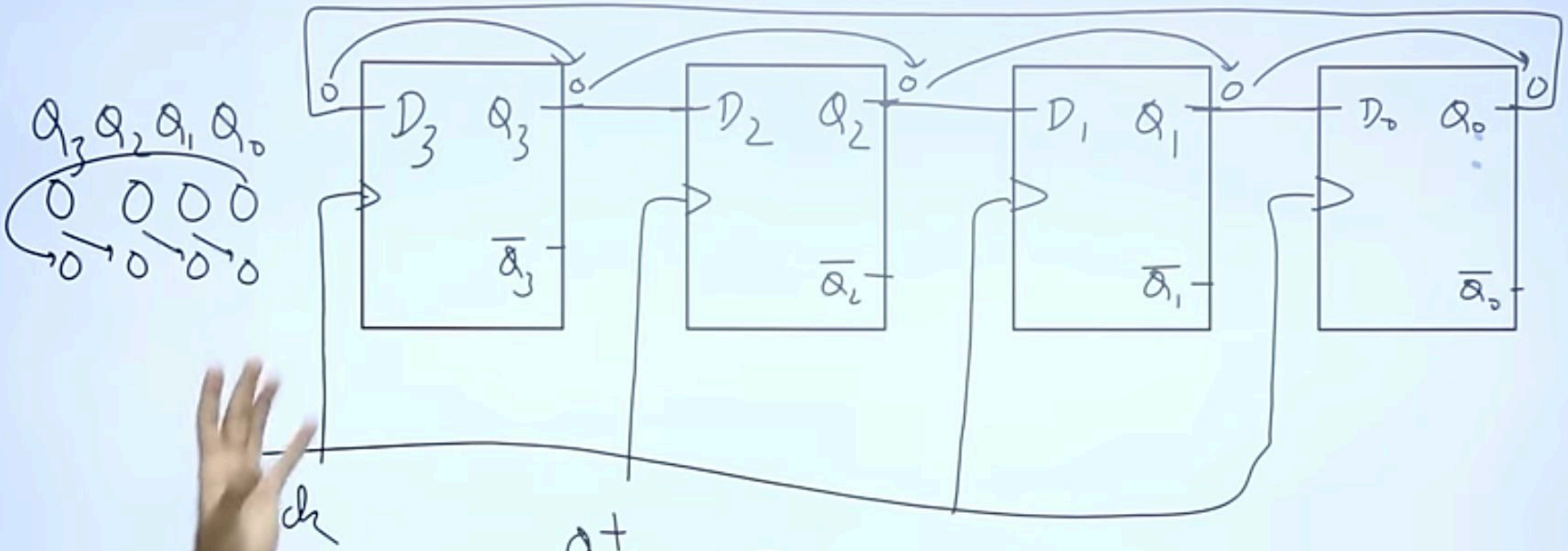
Same − Down
Diff = UP



Ring counter and Johnson Counter (Types of Synchronous Counter)

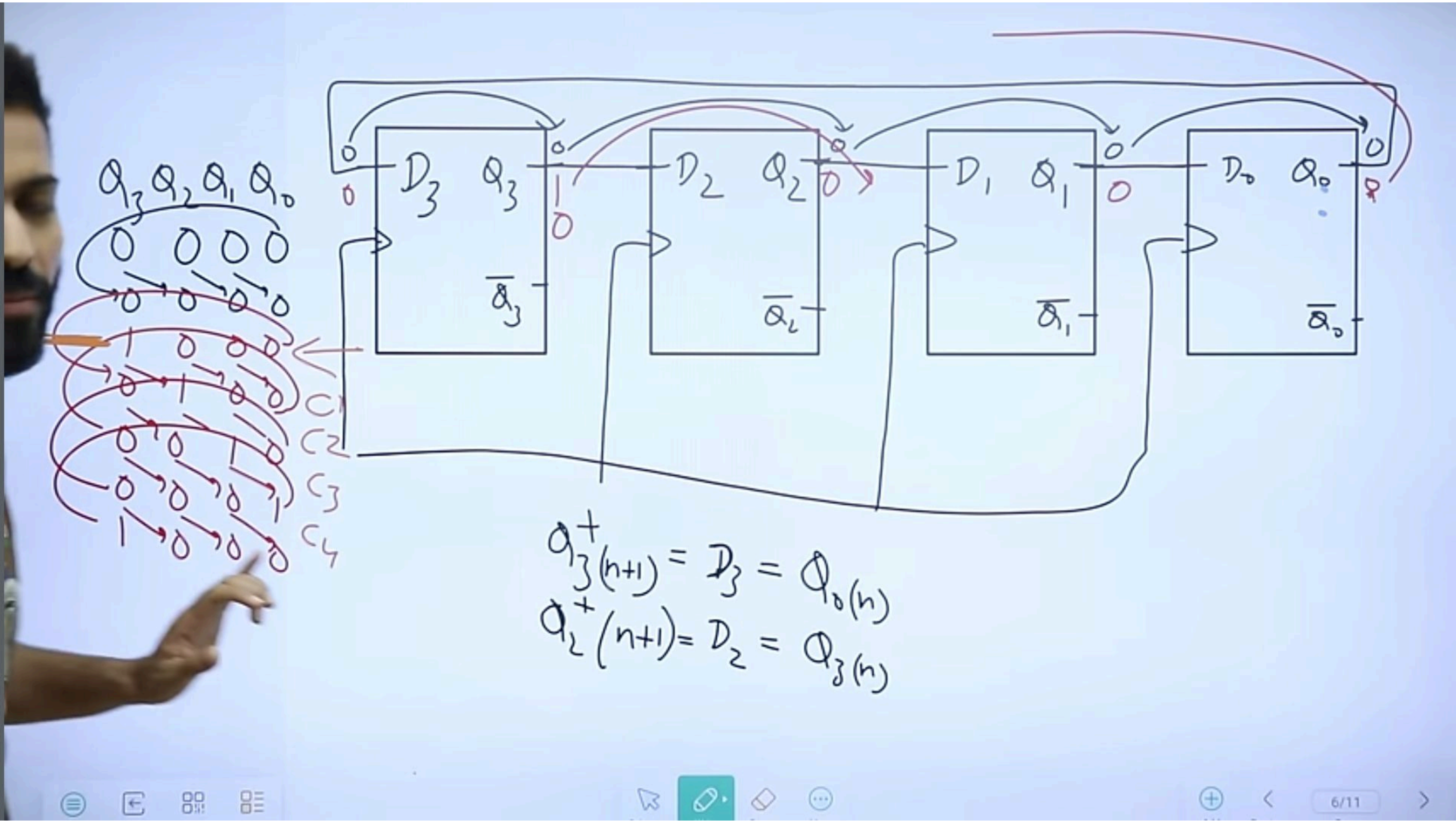


$$Q_3^+(n+1) = D_3 = Q_0(n)$$
$$Q_2^+(n+1) = D_2 = Q_3(n)$$

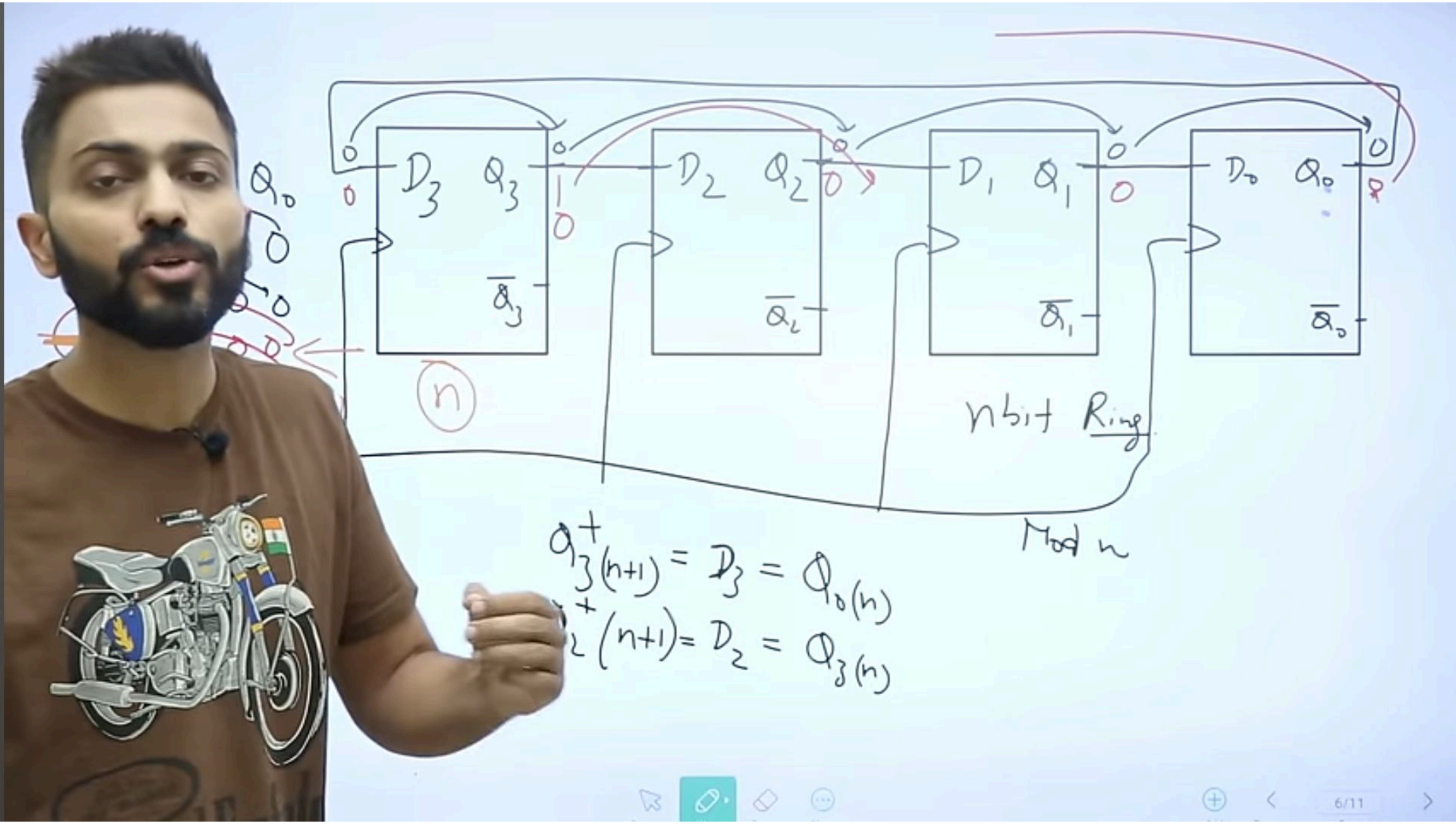


$$Q_3^+(n+1) = D_3 = Q_0(n)$$

$$Q_2^+(n+1) = D_2 = Q_3(n)$$

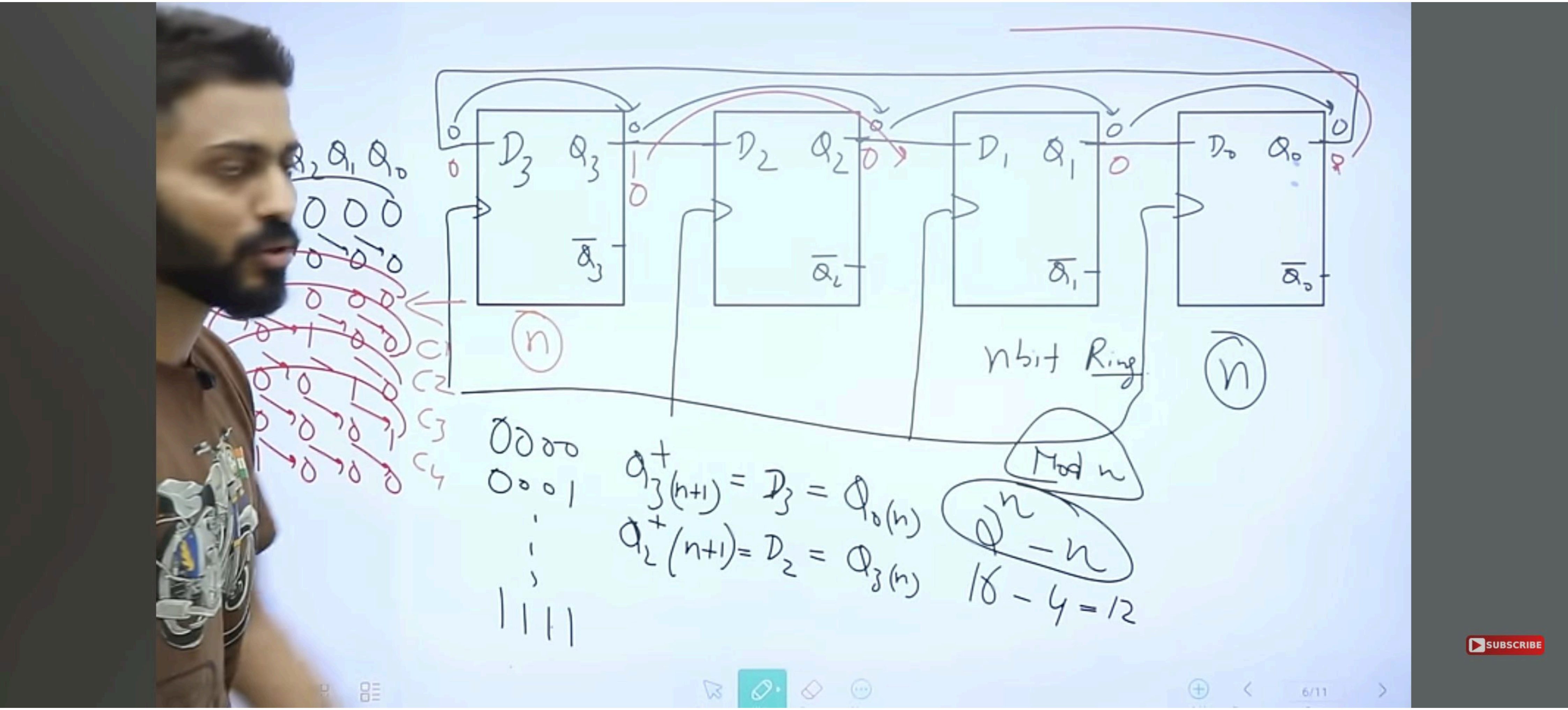


D3 Q3
D2 Q2
D1 Q1
D0 Q0
Q3 Q2 Q1 Q0
0 0 0 0
0 0 0 0
1 0 0 0
0 1 0 0 C1
0 0 1 0 C2
0 0 0 1 C3
1 0 0 0 C4
$Q_3^+(n+1) = D_3 = Q_0(n)$
$Q_2^+(n+1) = D_2 = Q_3(n)$
SUBSCRIBE
6/11

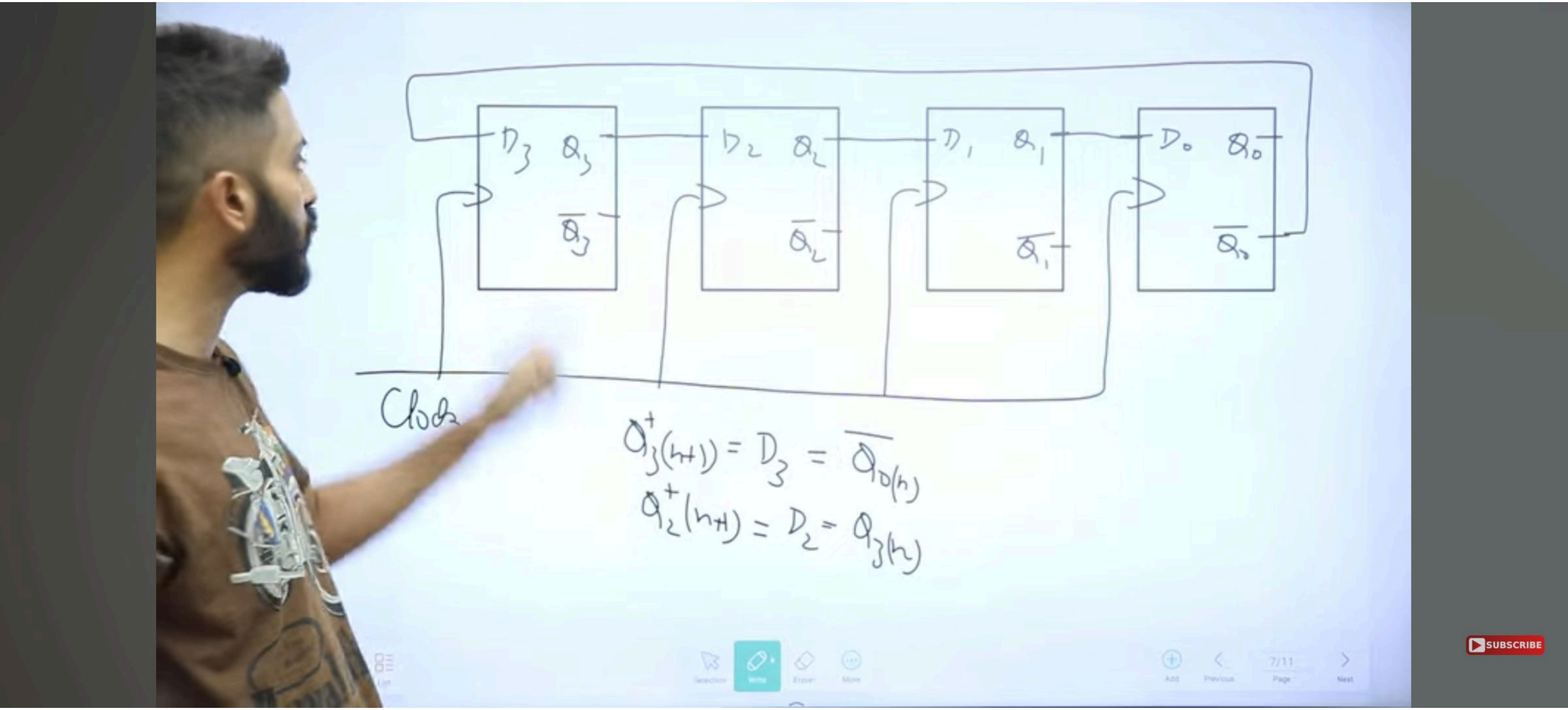


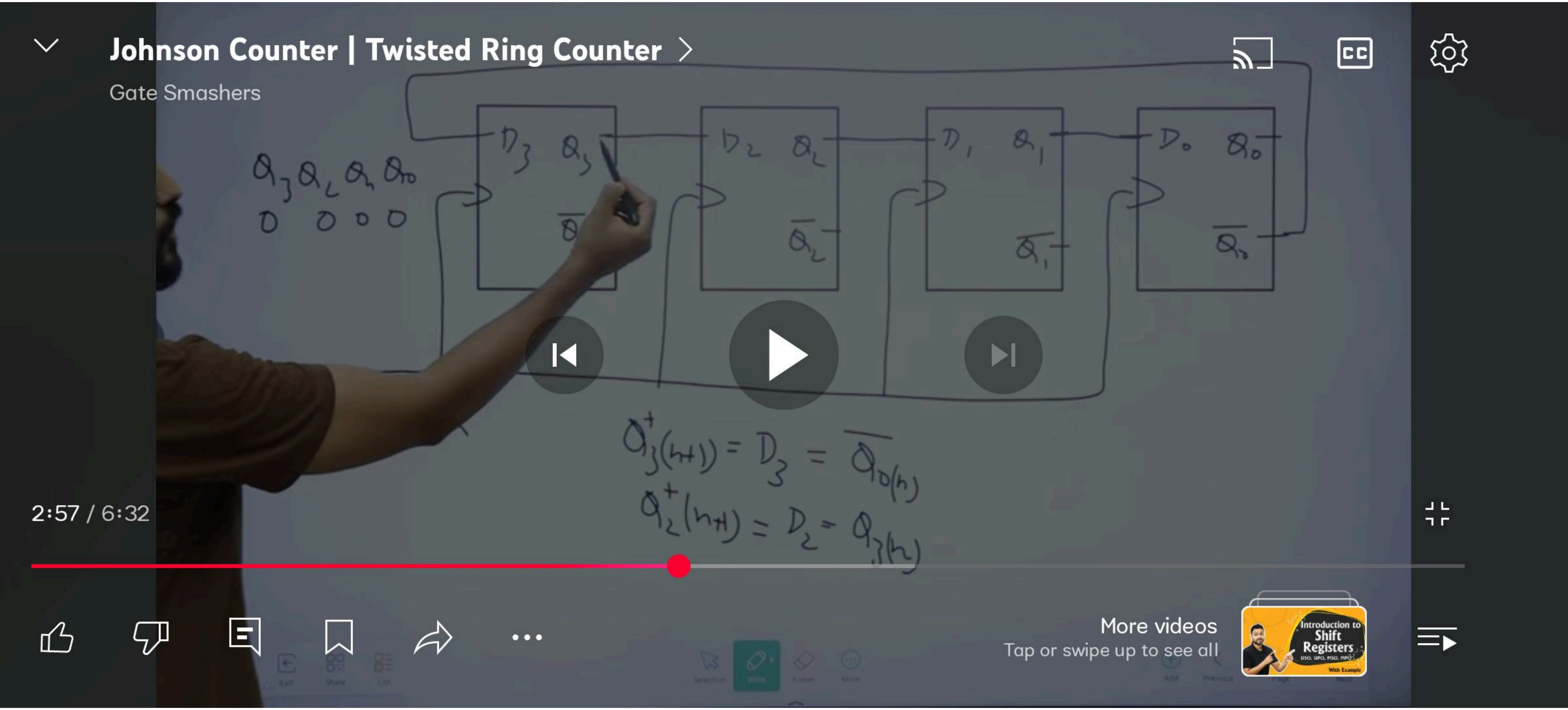
D_3 Q_3 $\overline{Q}_3$
D_2 Q_2 $\overline{Q}_2$
D_1 Q_1 $\overline{Q}_1$
D_0 Q_0 $\overline{Q}_0$
Q_0
n
nbit Ring
Mod n
$Q_3^+(n+1) = D_3 = Q_0(n)$
$Q_2^+(n+1) = D_2 = Q_3(n)$
6/11

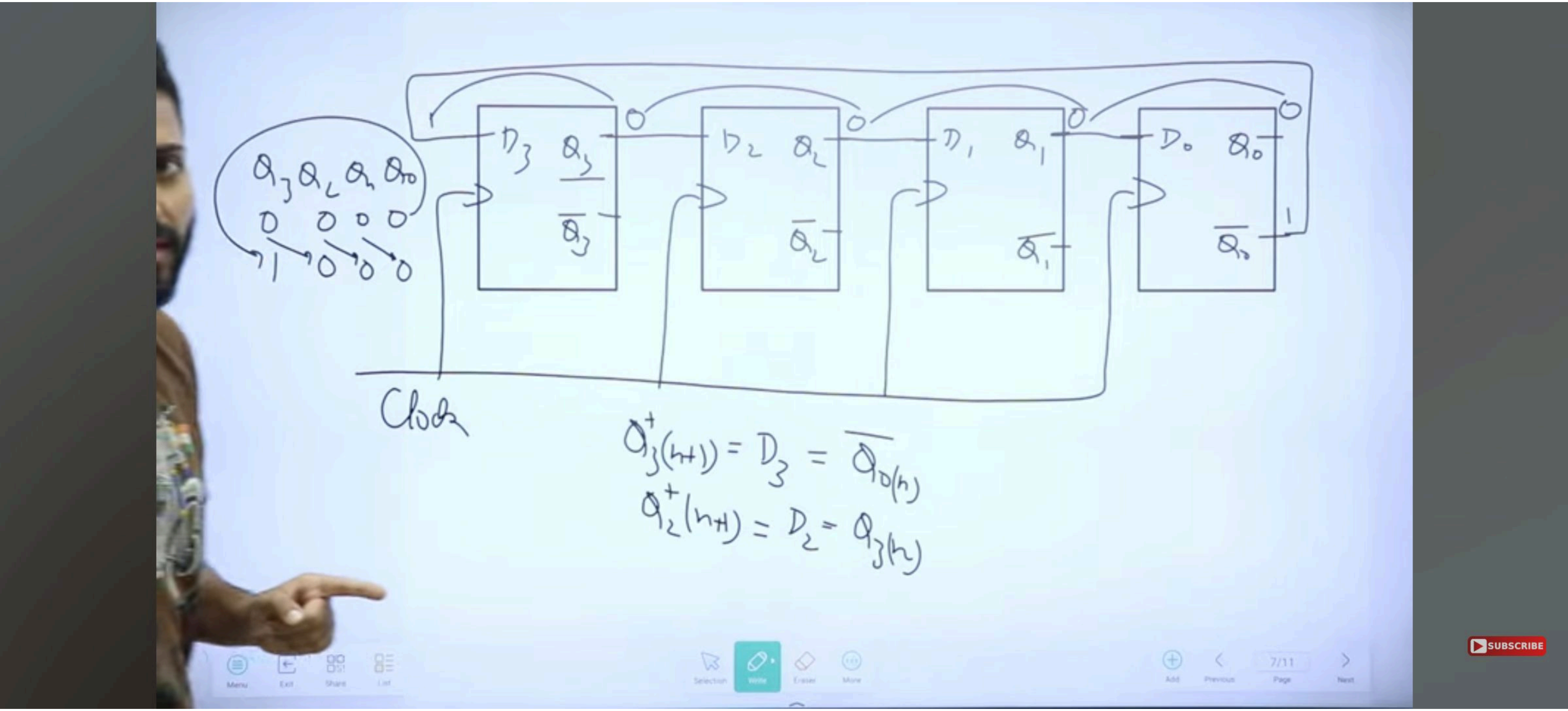
SUBSCRIBE

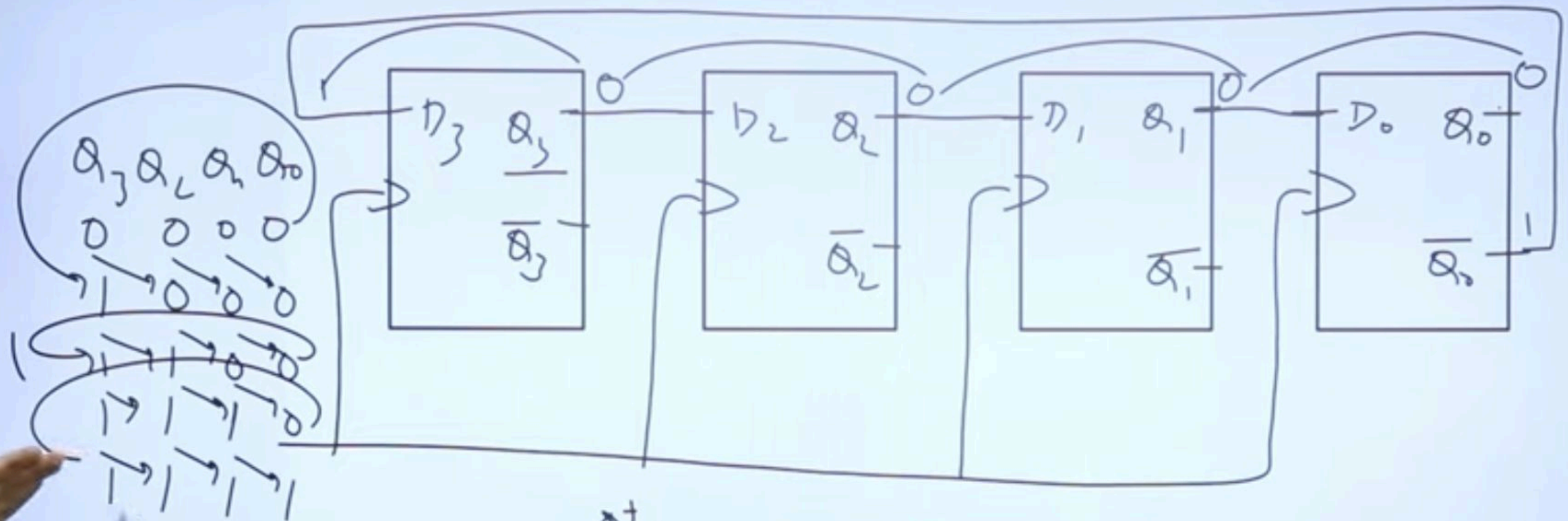


D3 Q3
D2 Q2
D1 Q1
D0 Q0
Q2 Q1 Q0
n bit Ring
Mod n
0000
0001
1111
$Q_3^+(n+1) = D_3 = Q_0(n)$
$Q_2^+(n+1) = D_2 = Q_3(n)$
$2^n - n$
16 - 4 = 12
C1
C2
C3
C4
6/11
SUBSCRIBE


D_3 Q_3 $\overline{Q_3}$
D_2 Q_2 $\overline{Q_2}$
D_1 Q_1 $\overline{Q_1}$
D_0 Q_0 $\overline{Q_0}$
Clock
$Q_3^+(n+1) = D_3 = \overline{Q_{0(n)}}$
$Q_2^+(n+1) = D_2 = Q_{3(n)}$
7/11
SUBSCRIBE


Johnson Counter | Twisted Ring Counter
Gate Smashers
$Q_3 Q_2 Q_1 Q_0$
0 0 0 0
D_3 Q_3
D_2 Q_2 $\overline{Q_2}$
D_1 Q_1 $\overline{Q_1}$
D_0 Q_0 $\overline{Q_0}$
$Q_3^+(n+1) = D_3 = \overline{Q_0}(n)$
$Q_2^+(n+1) = D_2 = Q_3(n)$
2:57 / 6:32
More videos
Tap or swipe up to see all
Introduction to Shift Registers

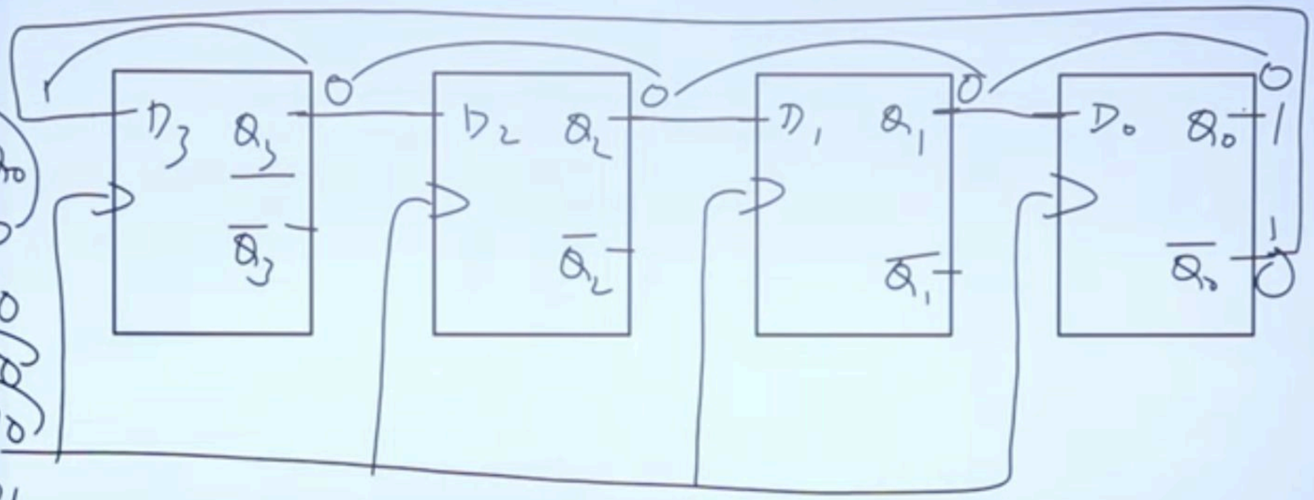

Q3 Q2 Q1 Q0
0 0 0 0
1 0 0 0
D3 Q3
D2 Q2
D1 Q1
D0 Q0
Clock
Q3+(n+1) = D3 = Q̄0(n)
Q2+(n+1) = D2 = Q3(n)
SUBSCRIBE
7/11



$$Q_3^+(n+1) = D_3 = \overline{Q_{0(n)}}$$

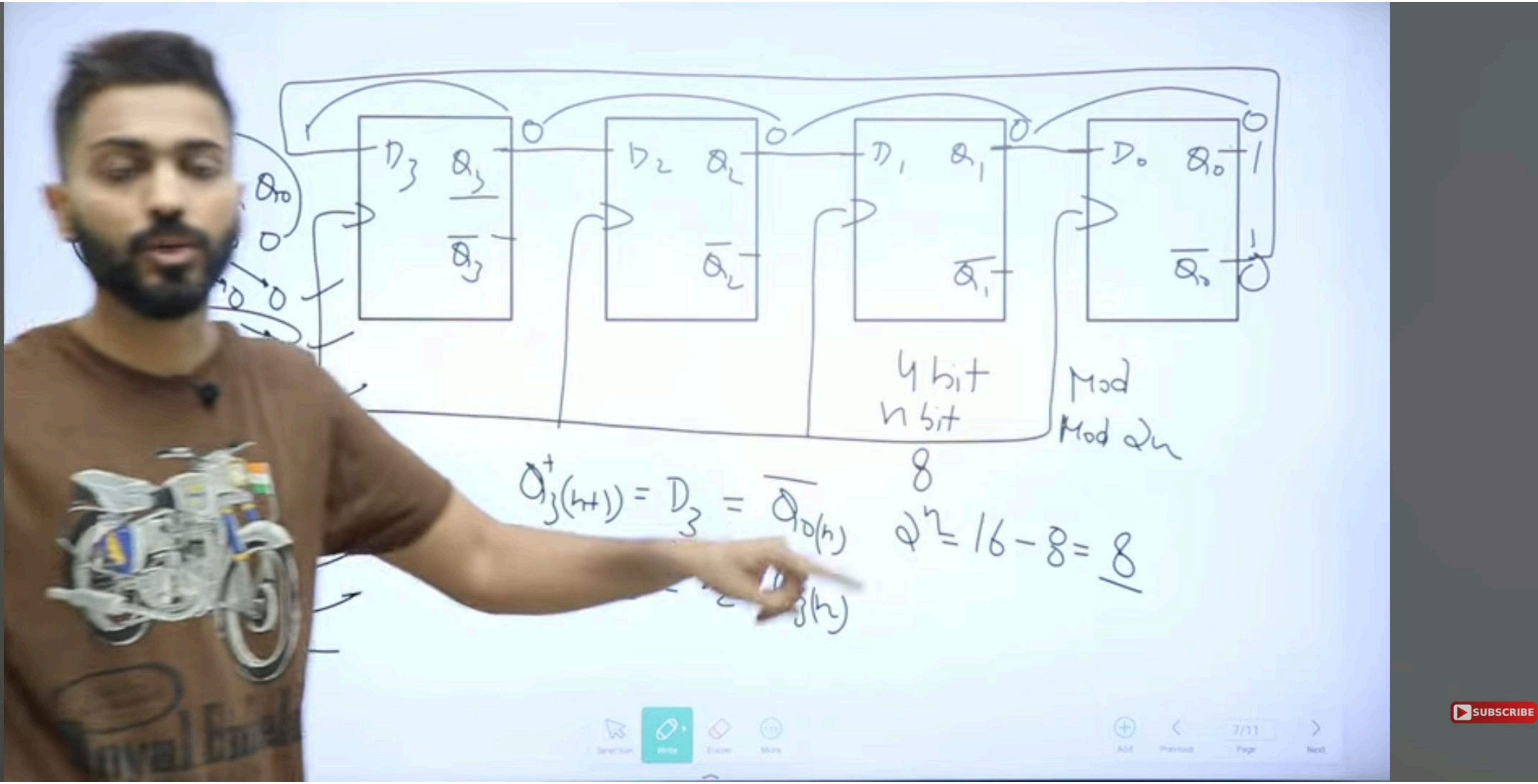
$$Q_2^+(n+1) = D_2 = Q_{3(n)}$$

Q_3	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
0	0	0	0



$$Q_3^+(n+1) = D_3 = \overline{Q_{0(n)}}$$

$$Q_2^+(n+1) = D_2 = Q_{3(n)}$$



4 bit
n bit
Mod
Mod 2n
8
16 - 8 = 8
SUBSCRIBE

Twisted ring/johnson is still better

Total states - unused states = usable

16-12=4(Ring)

16-7=8(Johnson)