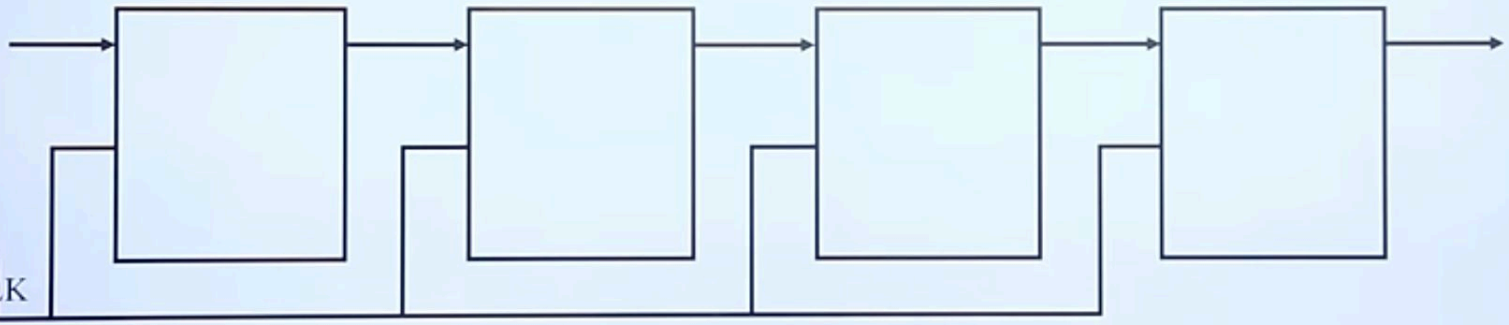
Shift Registers

- Shift registers are used to implement arithmetic operations.
- e.g. Left shift, Right shift
- Basic flip flop used in the register is D ff.

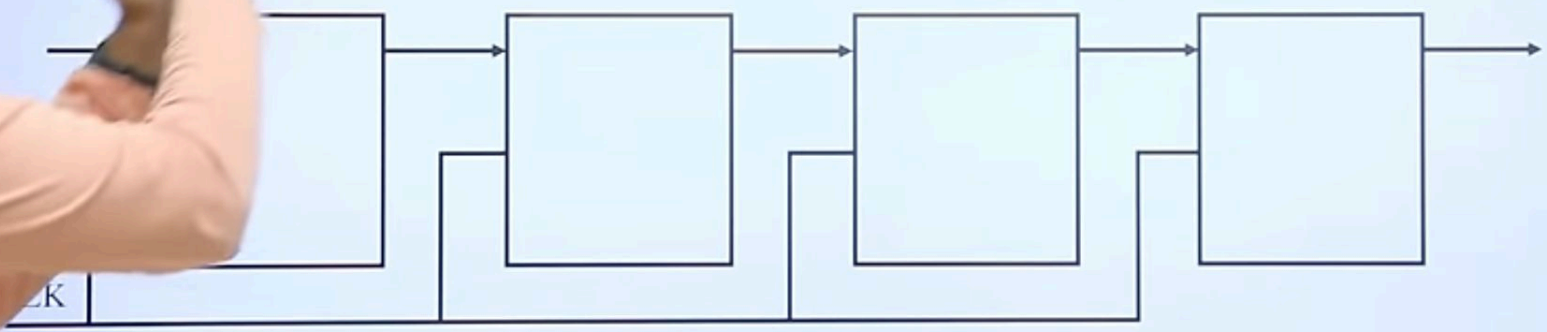


Shift Registers

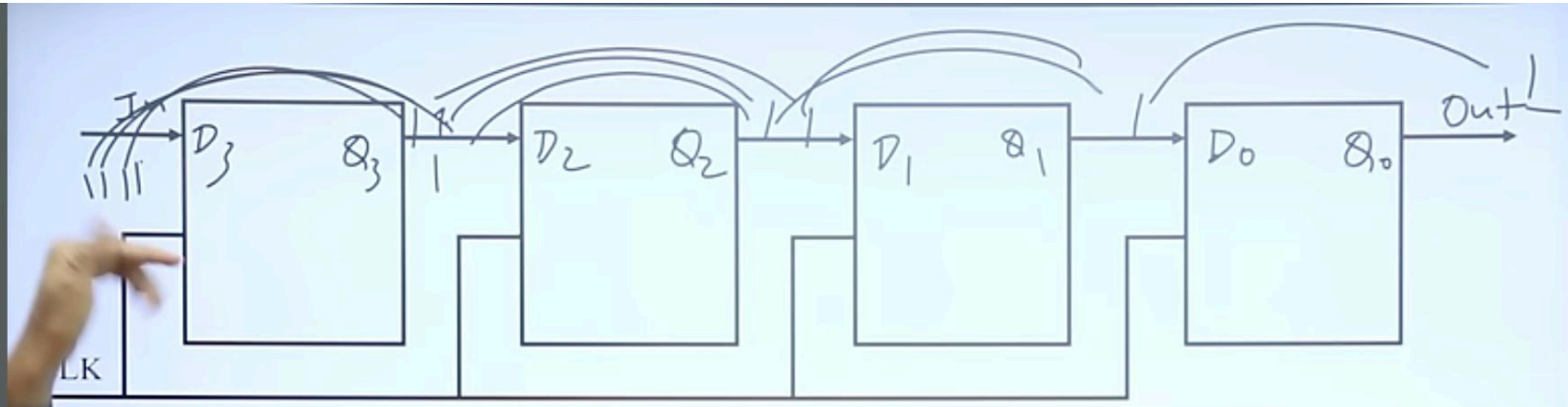
- Shift registers are used to implement arithmetic operations.
- e.g. Left shift, Right shift
- Basic flip flop used in the register is D ff.

0001 - 1
0010 - 2
0100 - 4
1000 - 8

2×3=6
2+2+2=



Mode	Clocks needed for n-bit shift register		
	Loading	Reading	Total
SISO	n	n-1	2n-1
SIPO	n	0	n
PISO	1	n-1	n
PIPO	1	0	1



1111 $Q_3\ Q_2\ Q_1\ Q_0$

C1 0 0 0 0

C2 1 0 0 0

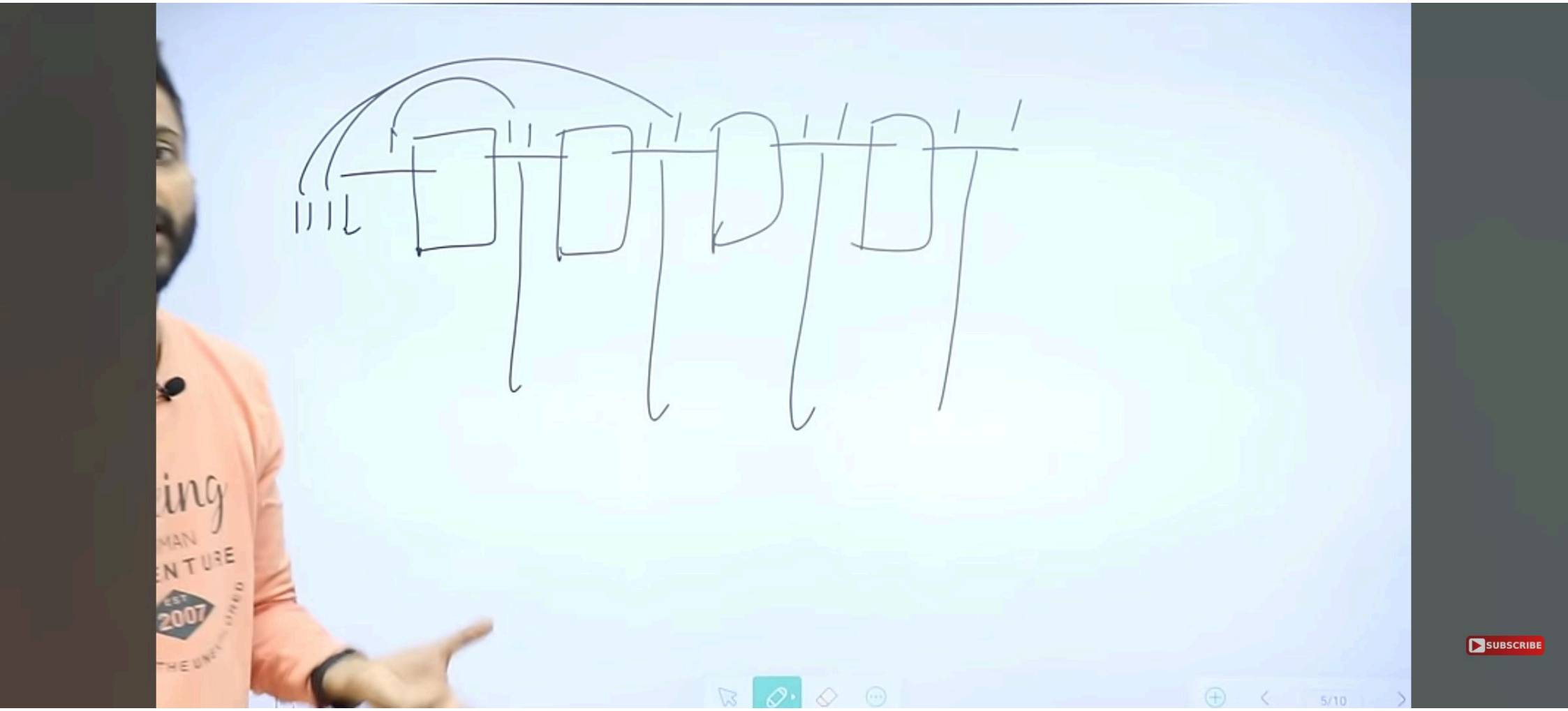
C3 1 1 0 0

C4 1 1 1 0

C5 1 1 1 1

n

n-1


SUBSCRIBE
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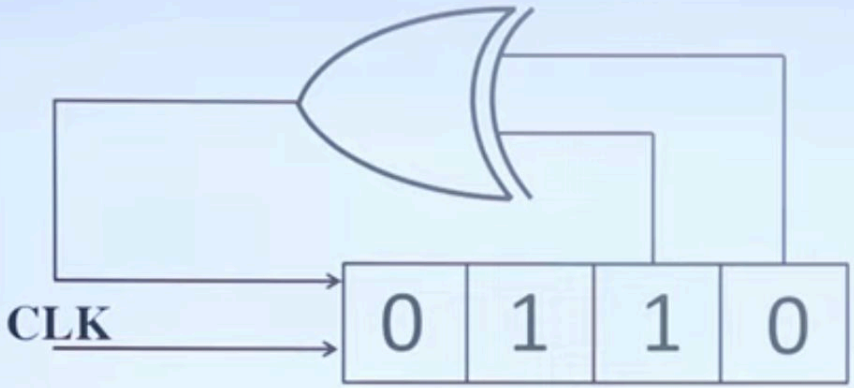
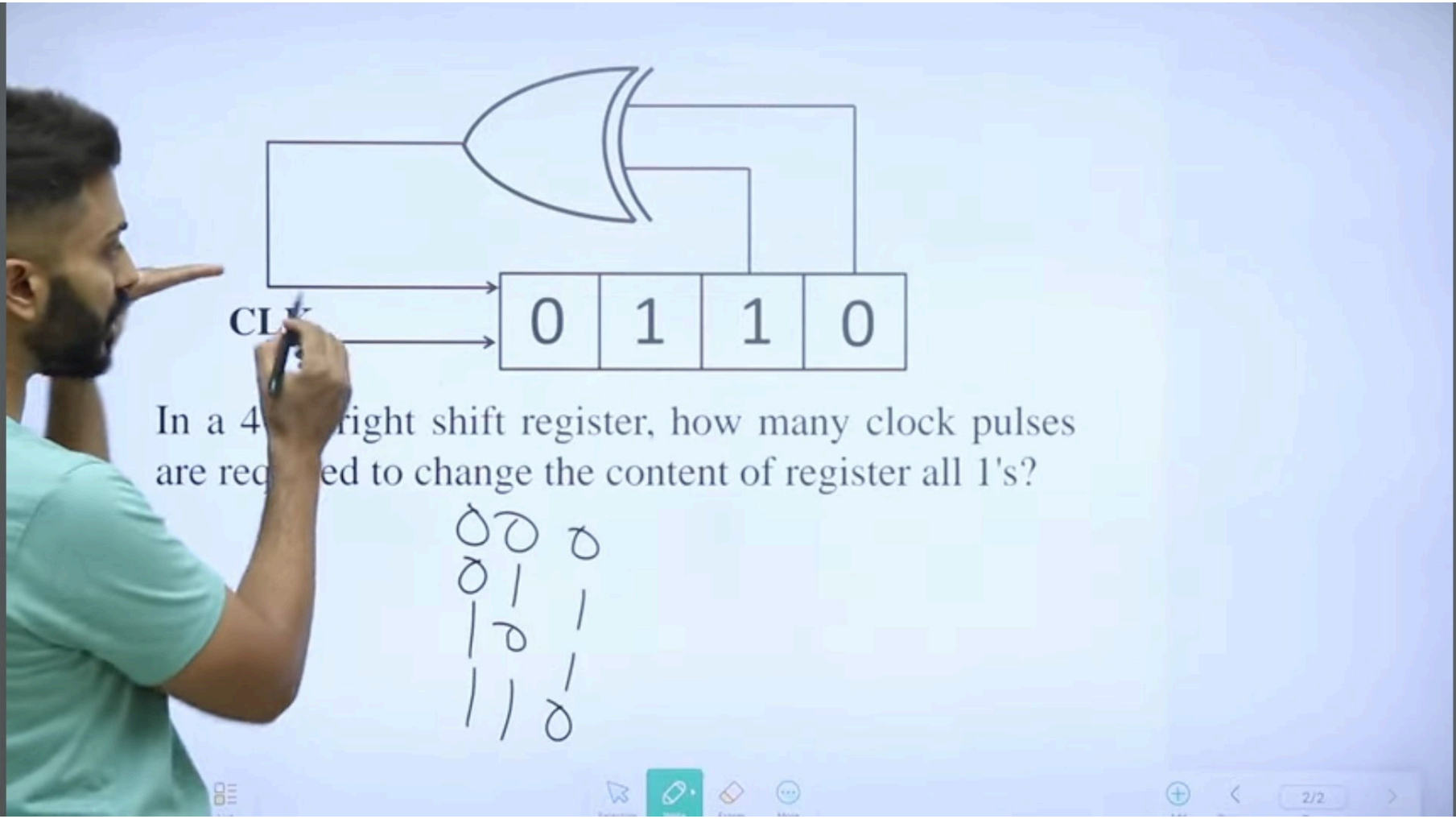
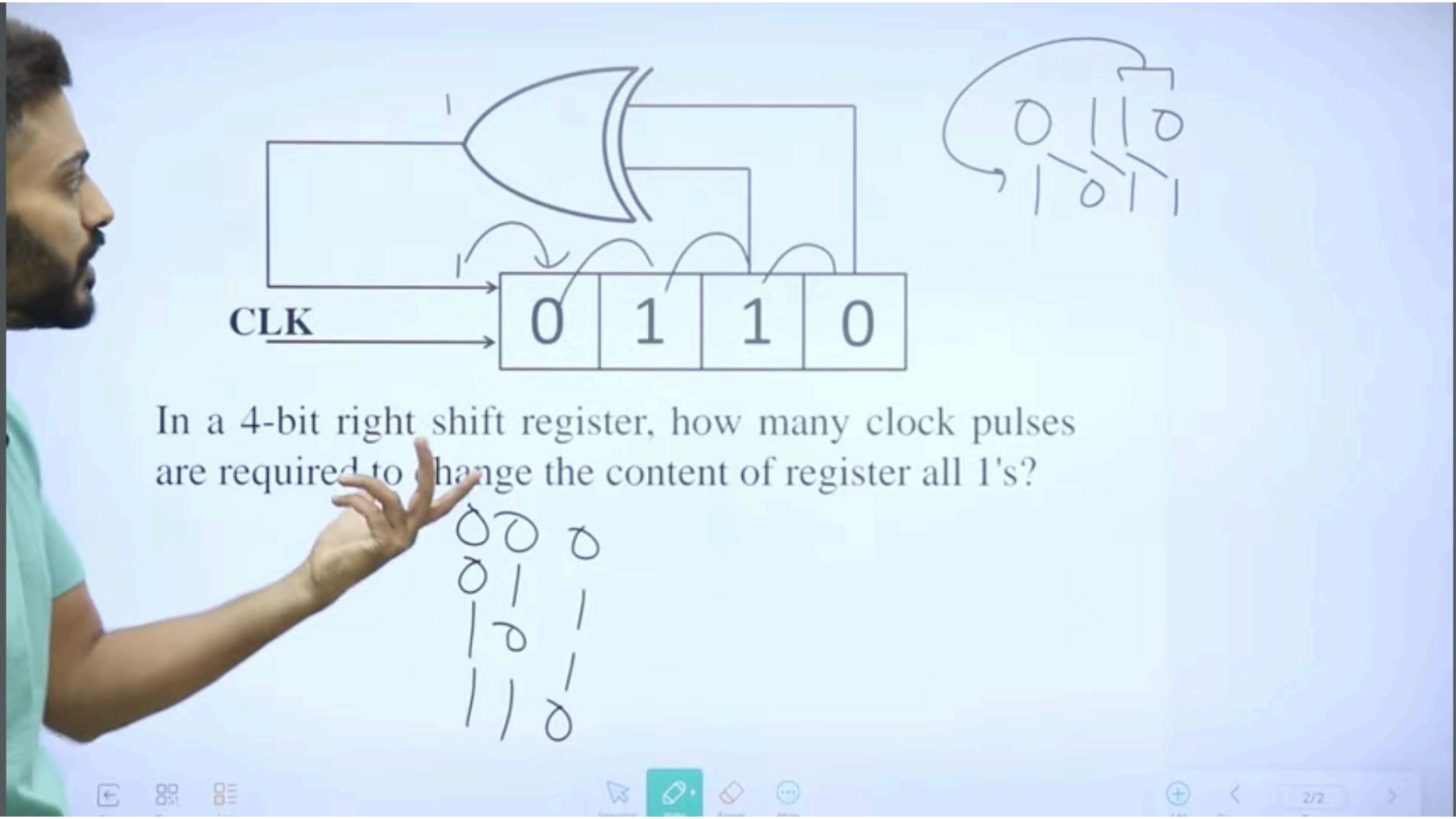
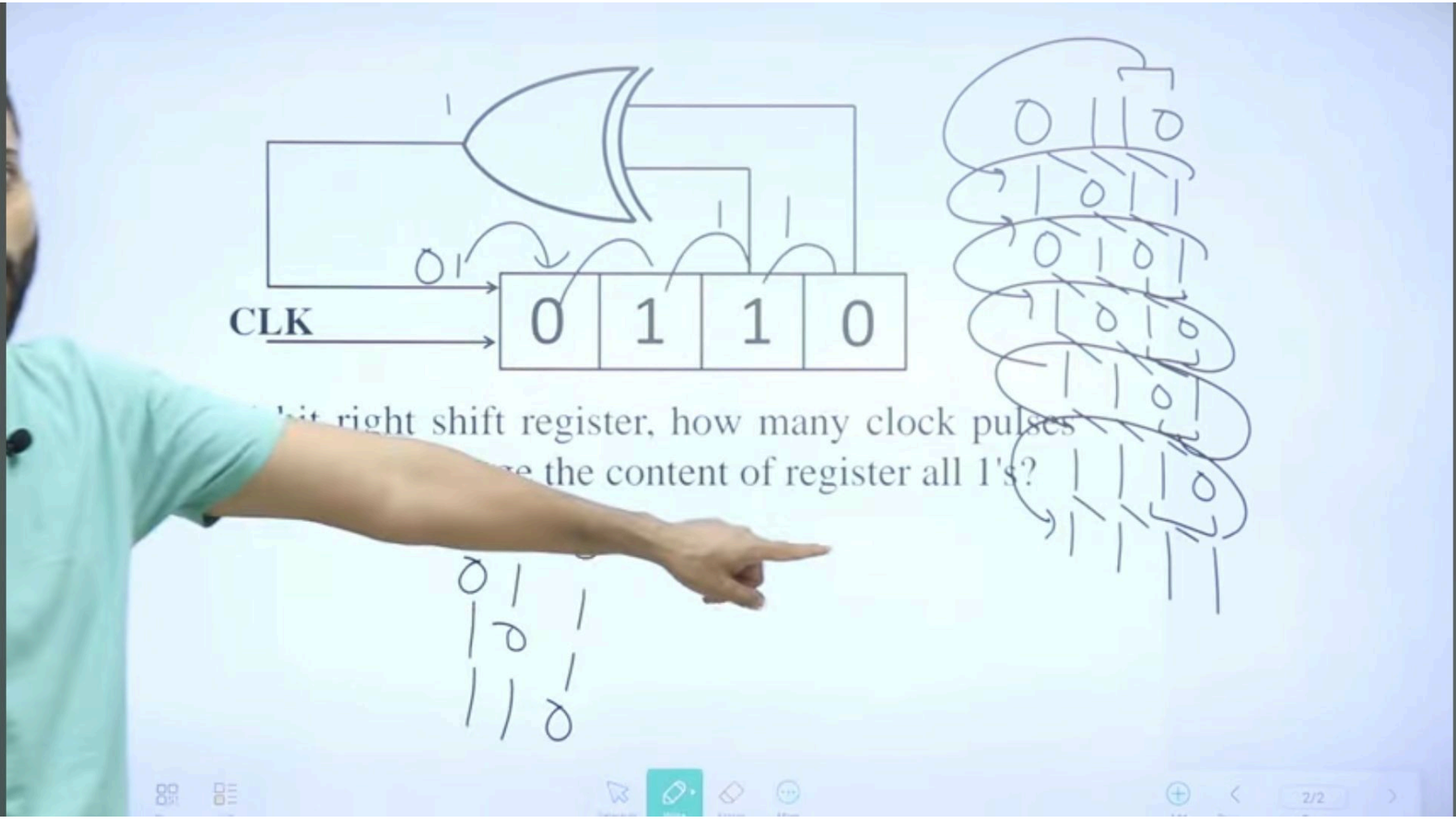


In a 4-bit right shift register, how many clock pulses are required to change the content of register all 1's?

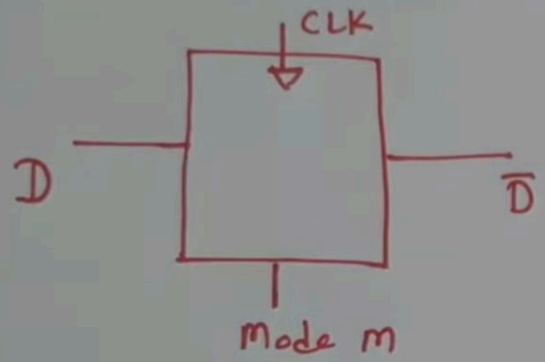

CLK
0 1 1 0
In a 4 right shift register, how many clock pulses are req ed to change the content of register all 1's?


CLK
0
1
1
0
In a 4-bit right shift register, how many clock pulses are required to change the content of register all 1's?
SUBSCRIBE


CLK
0
1
1
0
right shift register, how many clock pulses
the content of register all 1's?

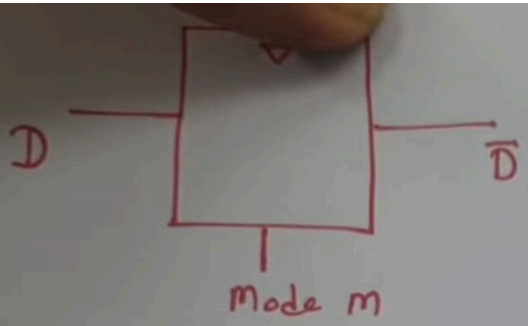
Bidirectional shift register

Bidirectional Shift Register



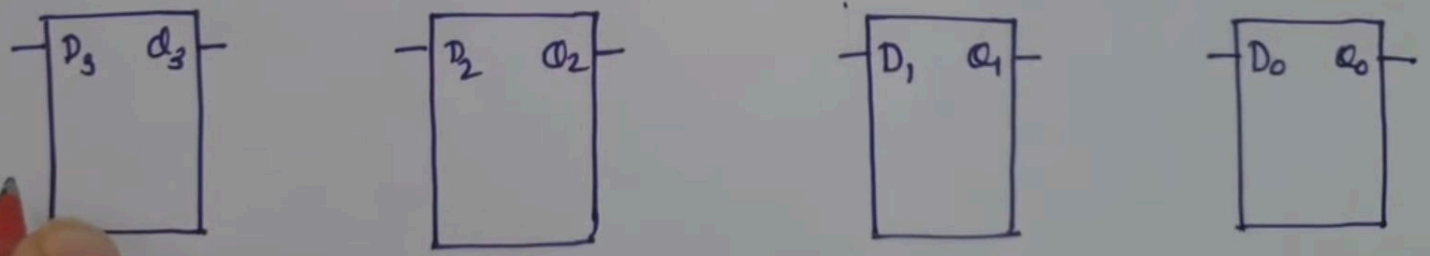
m = 1 , Shift Right

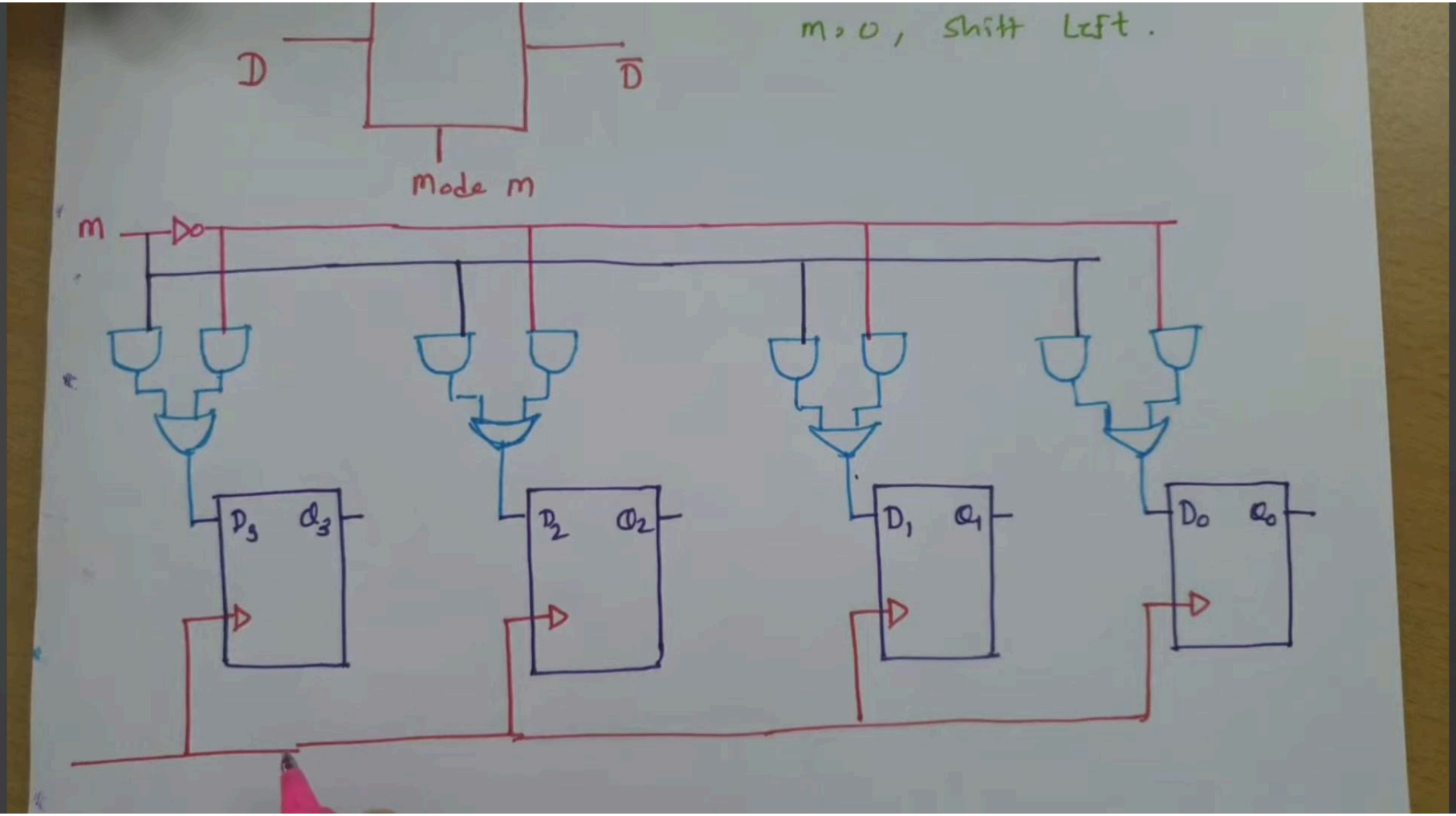
m = 0 , Shift Left .

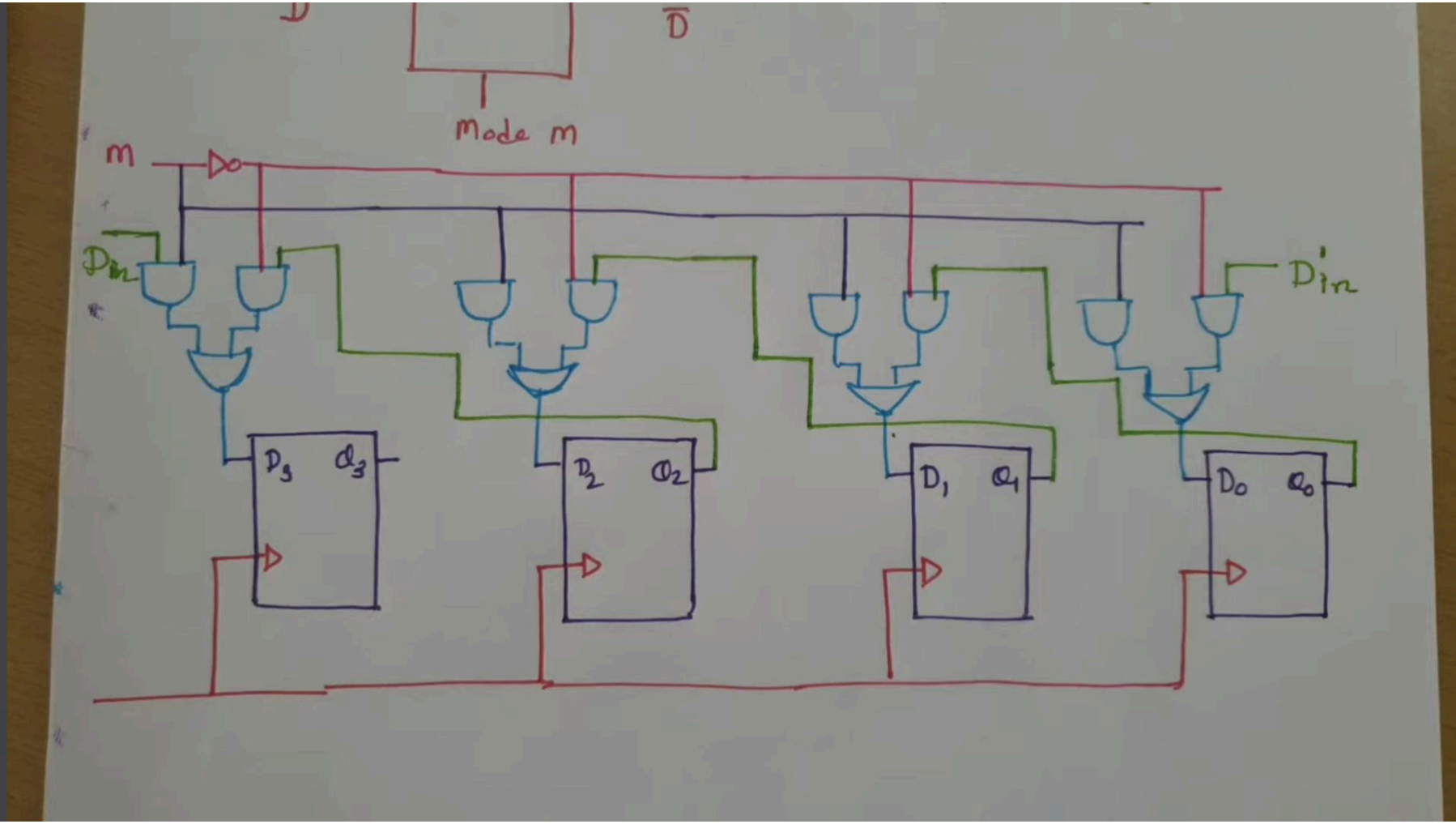


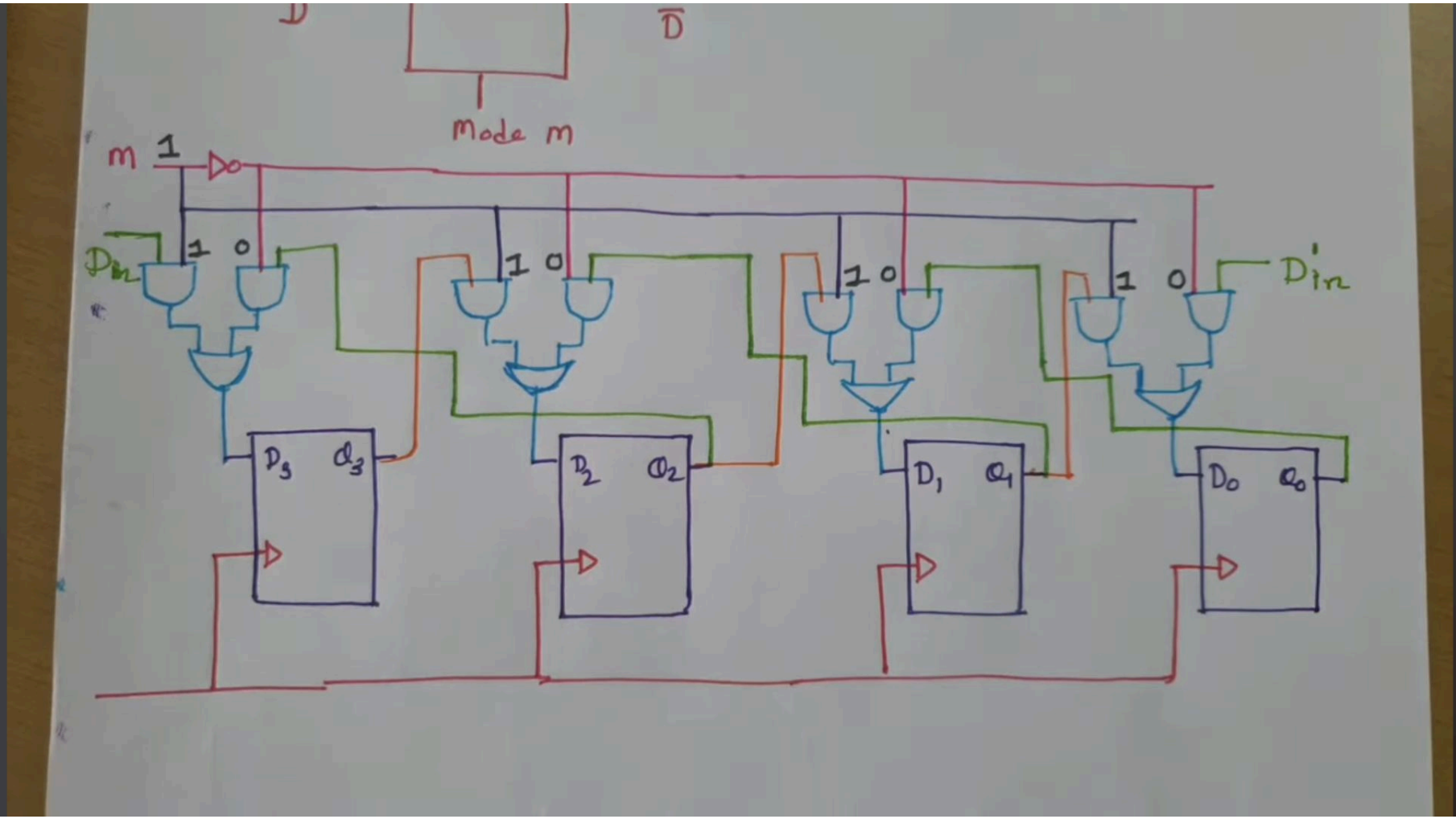
m = 1 , Shift Right

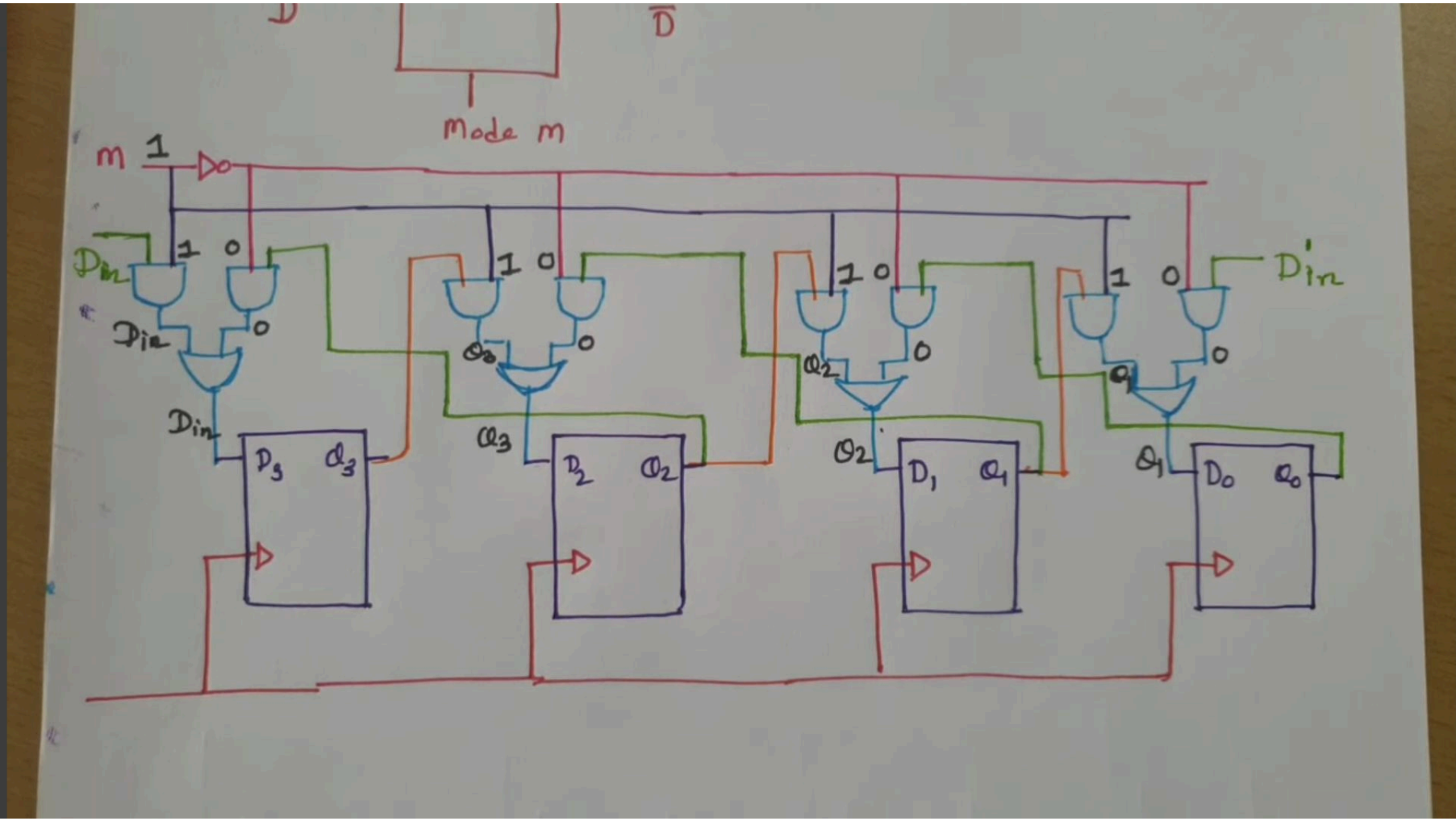
m = 0 , Shift Left .

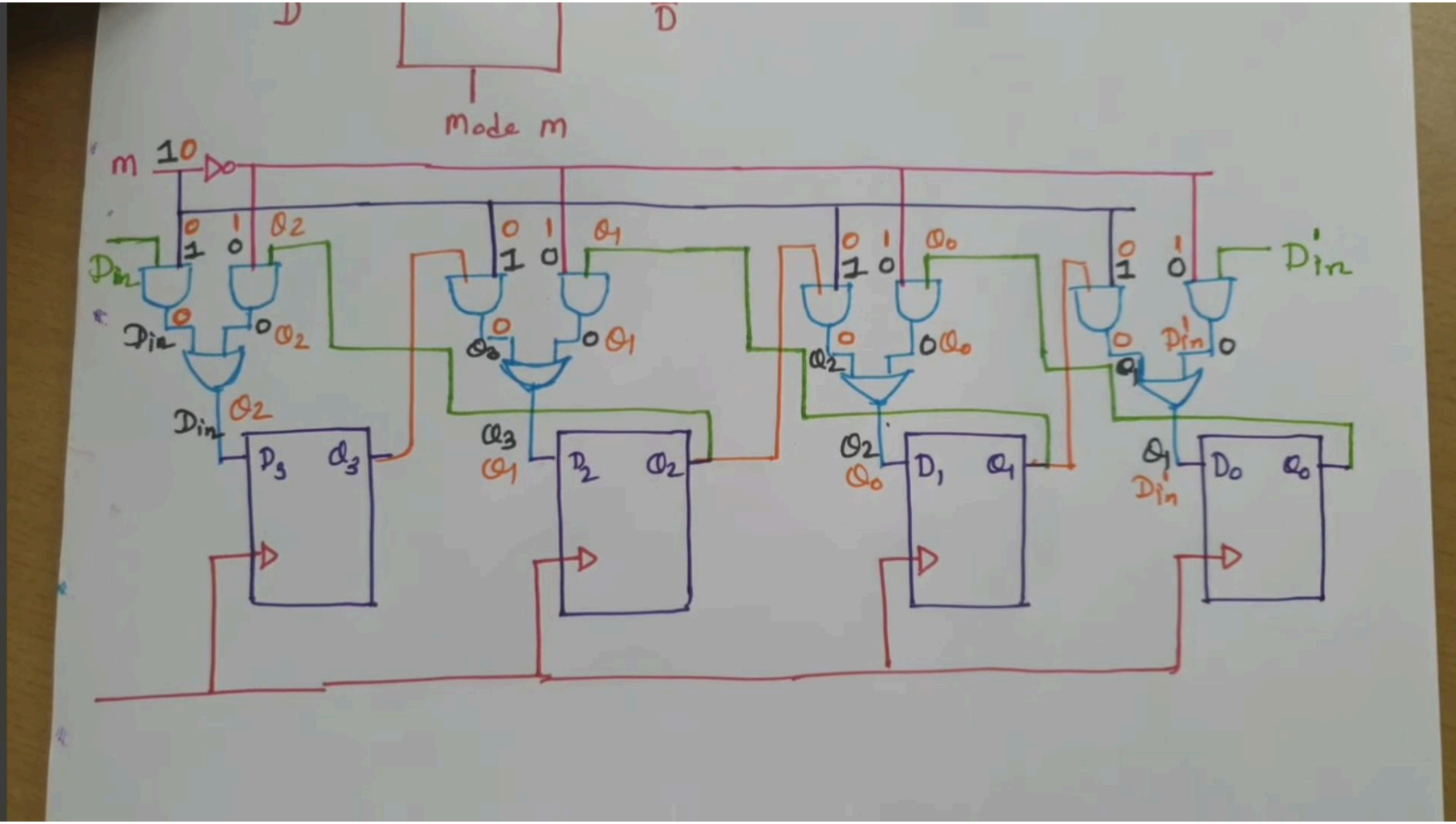



m = 0, Shift Left.
D
$\overline{D}$
Mode m
m
D_3
Q_3
D_2
Q_2
D_1
Q_1
D_0
Q_0


D
$\overline{D}$
Mode m
m
D_{in}
D'_{in}
D_3 Q_3
D_2 Q_2
D_1 Q_1
D_0 Q_0


D
$\overline{D}$
Mode m
m
1
0
1
0
1
0
1
0
1
0
D_{in}
D'_{in}
D_3
Q_3
D_2
Q_2
D_1
Q_1
D_0
Q_0


D
$\overline{D}$
Mode m
m
1
0
D_{in}
D_{in}
D_{in}
D'_{in}
Q_3
Q_2
Q_1
Q_0
D_3
Q_3
D_2
Q_2
D_1
Q_1
D_0
Q_0


D
D
Mode m
m
Din
Din
Din
Din
Q2
Q1
Q0
Q3
Q2
Q1
Q0
Q1
Din
D3 Q3
D2 Q2
D1 Q1
D0 Q0