FUNDAMENTALS OF VLSI ARCHITECTURES

Course Project

Design and Implementation of 16-point FFT using CORDIC in Verilog

Submitted by,

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EEE - VLSI & NANOELECTRONICS

Contents

1 Introduction

The Fast Fourier Transform (FFT) is a widely used algorithm for computing the Discrete Fourier Transform (DFT) efficiently. It is essential in applications such as spectral analysis, image processing, and wireless communication. The CORDIC (COordinate Rotation DIgital Computer) algorithm offers a hardware-friendly approach to compute sine, cosine, magnitude, and phase, making it suitable for FFT implementations on FPGAs. This report presents the design and implementation of a 16-point Fast Fourier Transform (FFT) using the CORDIC algorithm in Verilog. The FFT is a fundamental tool in signal processing, and the CORDIC method enables efficient computation of trigonometric functions without multipliers. The document discusses the theoretical background, architectural design, simulation results, and synthesis metrics for FPGA deployment.

2 CORDIC Algorithm Overview

CORDIC is an iterative algorithm that performs vector rotations using only shift and add operations. It is particularly useful for computing trigonometric functions, polar-to-rectangular conversions, and vice versa. The algorithm operates in two modes:

- **Rotation Mode**: Used for computing sine and cosine.
- **Vectoring Mode**: Used for computing magnitude and phase.

3 FFT Architecture

The 16-point FFT is implemented using a radix-2 decimation-in-time (DIT) structure. Each butterfly unit uses CORDIC to compute the twiddle factors. The architecture includes:

- Input buffer for 16 complex samples
- 4 stages of butterfly computation
- CORDIC-based twiddle factor generator
- Output buffer for transformed data

4 Design Considerations

Key considerations in the design include:

- Fixed-point representation for CORDIC precision
- Pipelining for throughput optimization
- Resource sharing for area efficiency
- Latency vs accuracy trade-offs in CORDIC iterations

5 Verilog Implementation

The design is modularized into:

- `cordic-block.v`: Implements the CORDIC core
- `Butterfly.v`: Performs butterfly operations
- `Eight-point-fft.v`: performs 8 point fft operation
- `Sixteen-point-fft.v`: Performs 16 point fft operation using Eight-point-fft blocks.
- `FFT-top.v`: Top-level module integrating all components including input and output buffers.

6 RTL Schematic

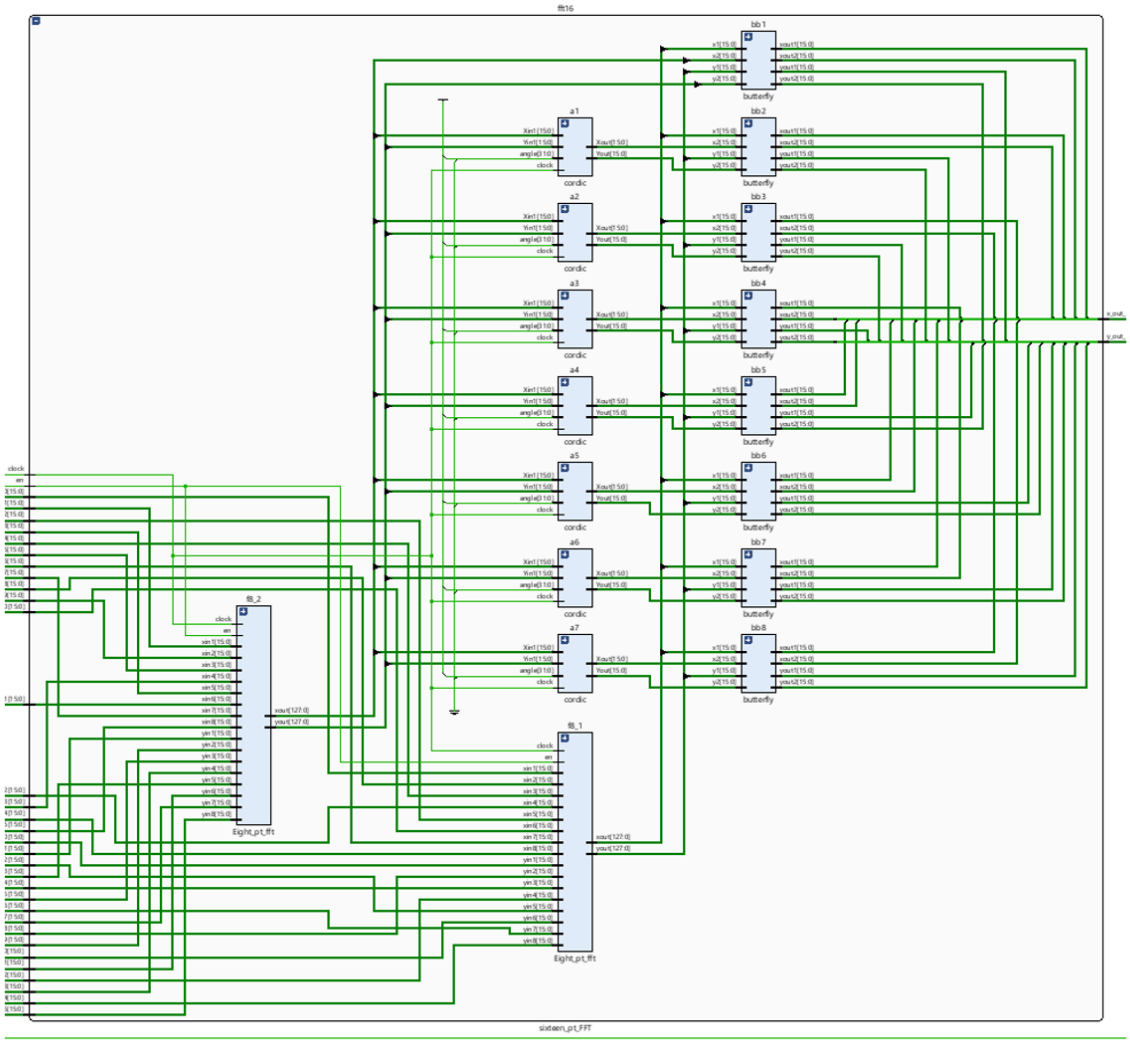

Figure 1: RTL Schematic of 16-point FFT using CORDIC

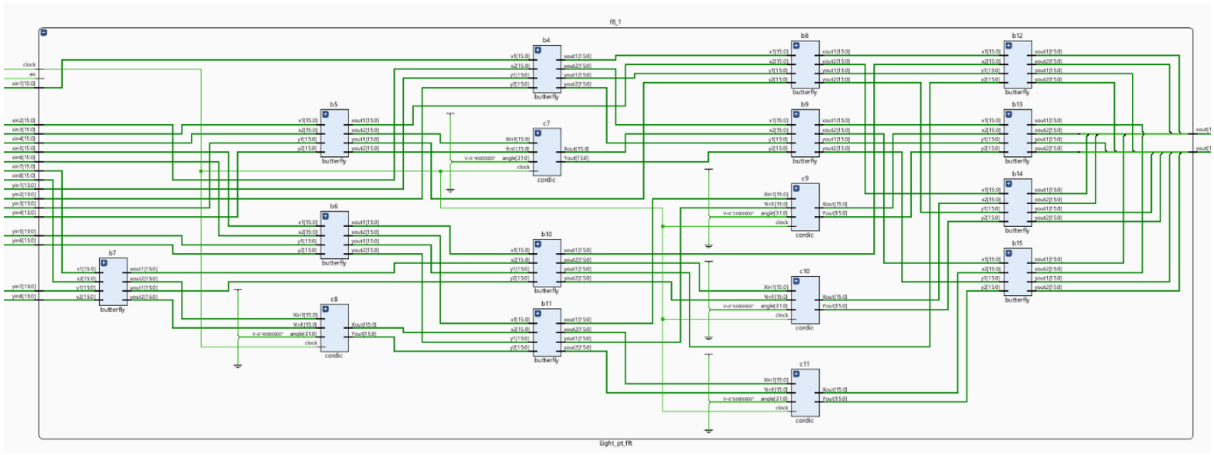

Figure 2: RTL Schematic of 8-point FFT using CORDIC

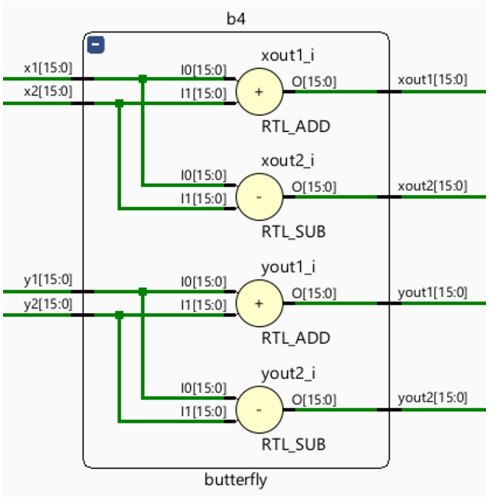

Figure 3: RTL Schematic of Butterfly block

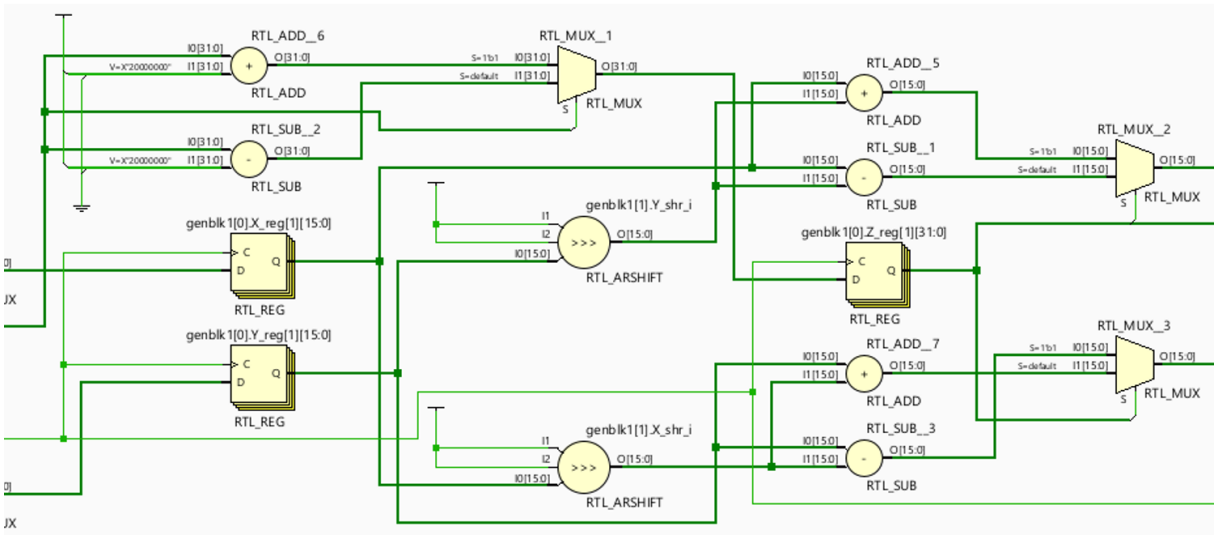

Figure 4: RTL Schematic of single iteration CORDIC block

7 Behavioral Simulation

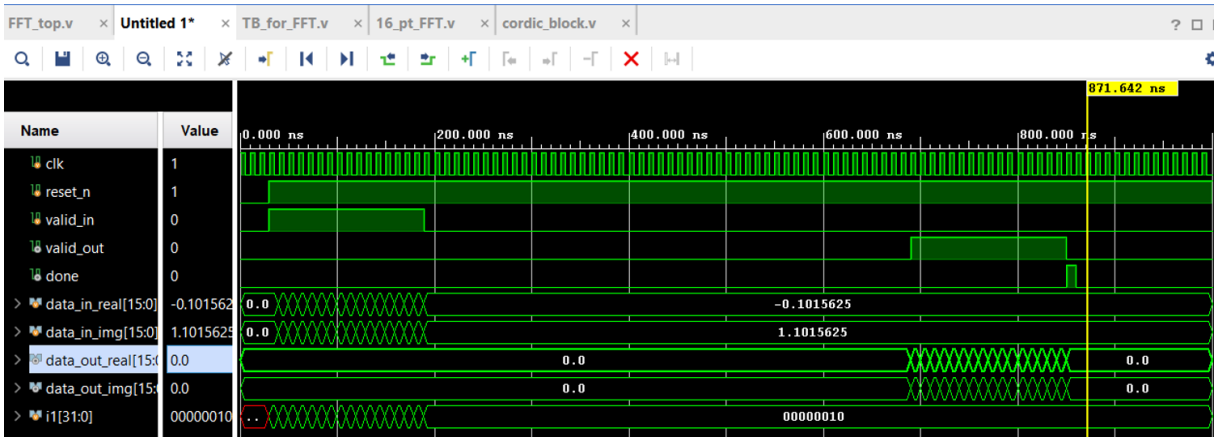

Figure 5: Simulation waveforms

7.1 inputs

Figure 6: Time Domain Inputs

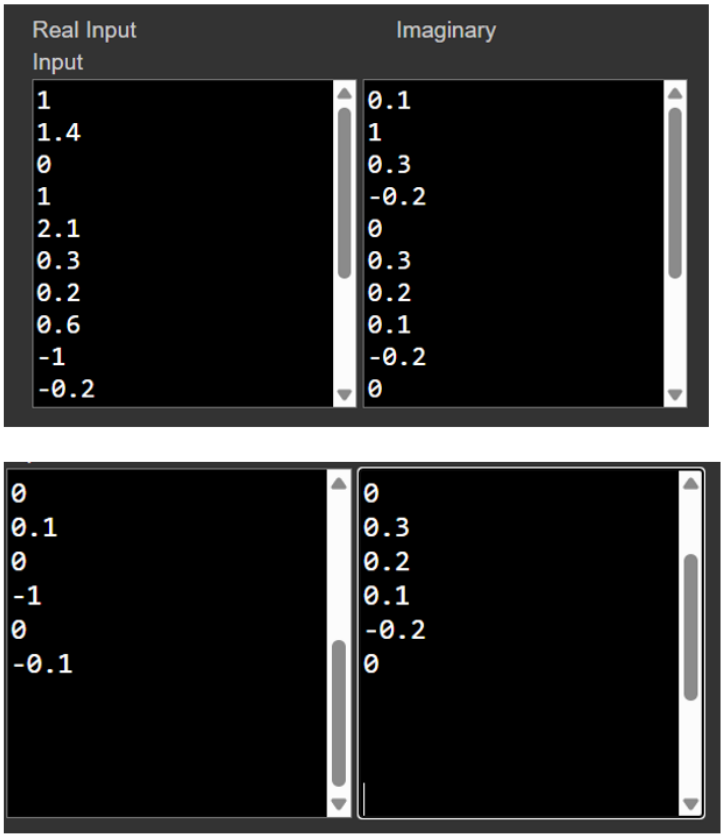

Figure 7: Time Domain Inputs

7.2 Outputs

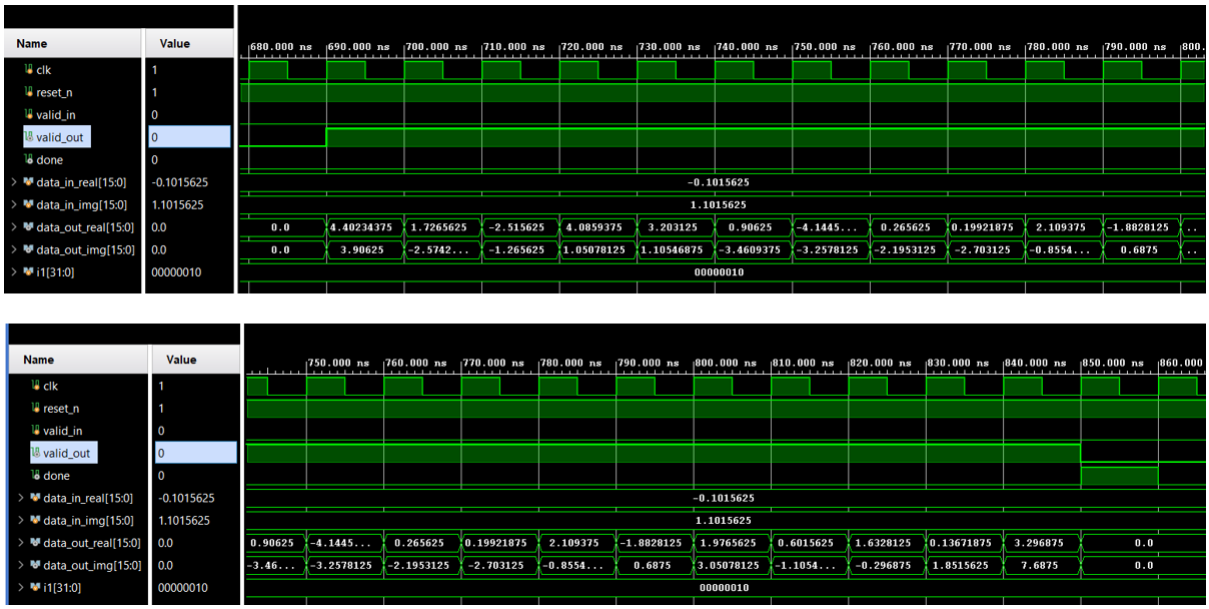

Figure 8: FFT Simulation: Frequency Domain Output

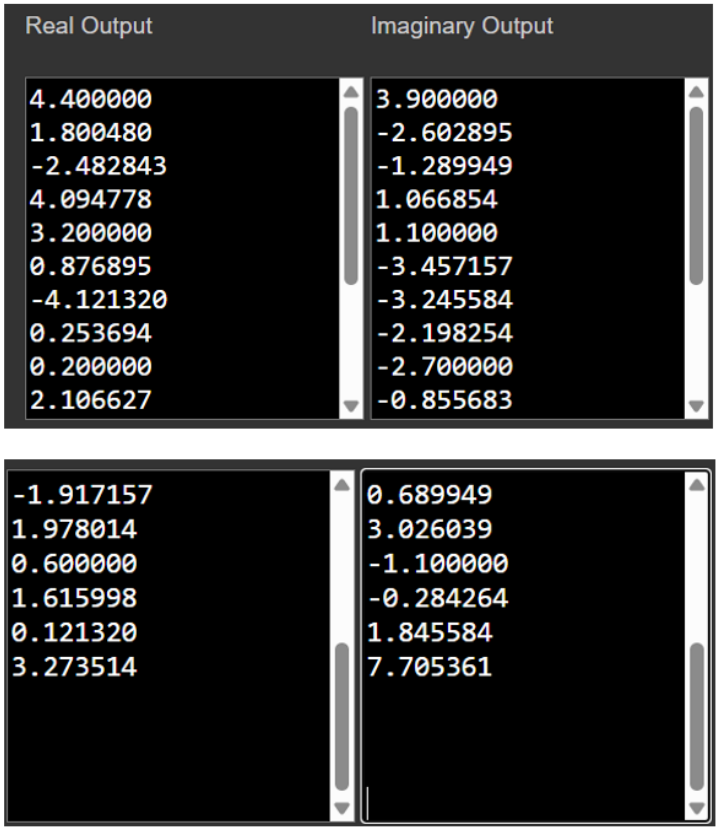

Figure 9: Results form Software based Calculator for comparison between expected results and actual results

7.3 Results

Outputs from the simulation was compared with outputs from software-based calculation and the results matched.

Maximum Absolute Error = 0.024

Average Absolute Error = 0.012

8 Synthesis Results (Kintex-7 FPGA)

8.1 Power Consumption

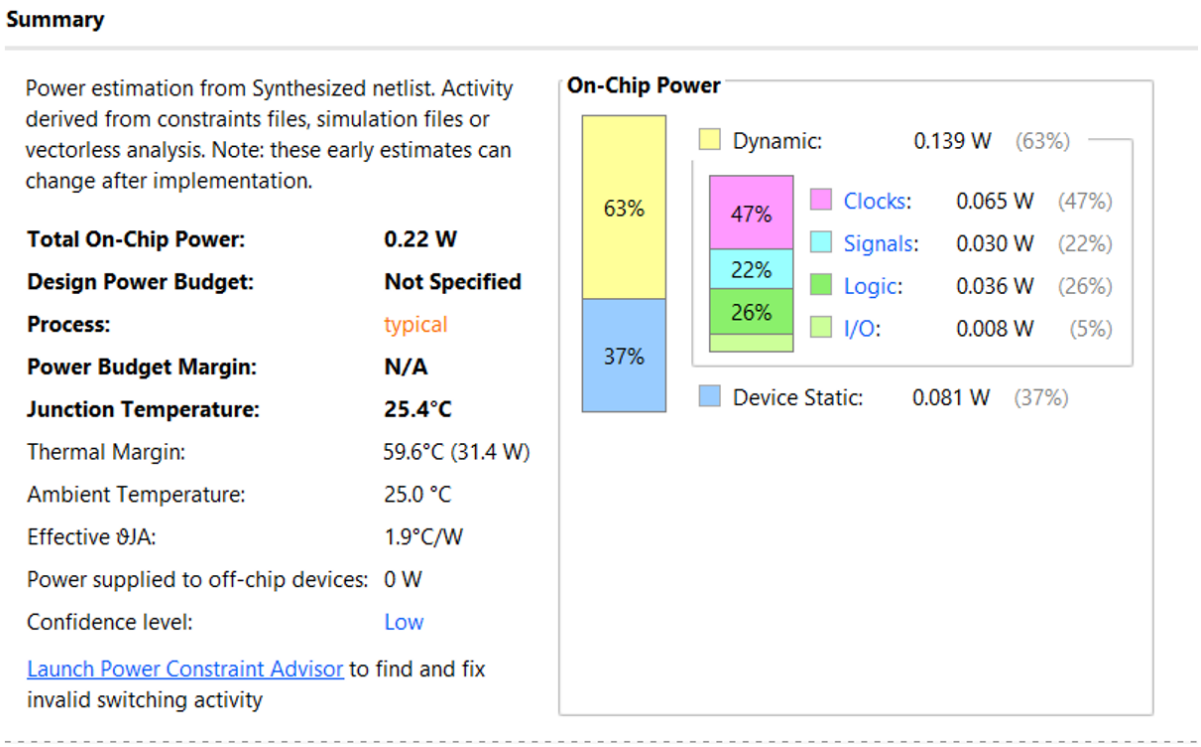

Figure 10: Power Consumption Report

8.2 Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.428 ns	Worst Hold Slack (WHS):	0.064 ns	Worst Pulse Width Slack (WPWS):	4.650 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	10393	Total Number of Endpoints:	10393	Total Number of Endpoints:	9791

All user specified timing constraints are met.

Clock Summary

Name	Waveform	Period (ns)	Frequency (MHz)
virtual	{0.000 5.000}	10.000	100.000

Figure 11: Timing Summary

8.3 Utilization

Hierarchy

Name	Slice LUTs (41000)	Slice Registers (82000)	F7 Muxes (20500)	Bonded IOB (300)	BUFGCTRL (32)
FFT_top	11346	9790	32	69	1
fft16 (sixteen_pt_FFT)	11136	8704	0	0	0
a1 (cordic)	508	512	0	0	0
a2 (cordic_0)	508	512	0	0	0
a3 (cordic_1)	508	512	0	0	0
a4 (cordic_2)	508	512	0	0	0
a5 (cordic_3)	508	512	0	0	0
a6 (cordic_4)	524	512	0	0	0
a7 (cordic_5)	516	512	0	0	0
bb1 (butterfly)	0	0	0	0	0
bb2 (butterfly_6)	0	0	0	0	0
bb3 (butterfly_7)	0	0	0	0	0
bb4 (butterfly_8)	0	0	0	0	0
bb5 (butterfly_9)	0	0	0	0	0
bb6 (butterfly_10)	0	0	0	0	0
bb7 (butterfly_11)	16	0	0	0	0
bb8 (butterfly_12)	8	0	0	0	0
f8_1 (Eight_pt_fft)	3936	2560	0	0	0
f8_2 (Eight_pt_fft_13	3666	2560	0	0	0

Summary

Resource	Utilization	Available	Utilization %
LUT	11346	41000	27.67
FF	9790	82000	11.94
IO	69	300	23.00

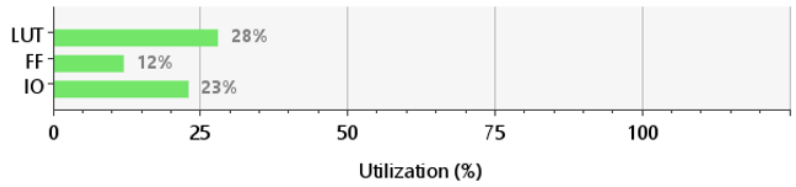

Figure 12: Resource Utilization Report

9 Post Synthesis Functional Simulation

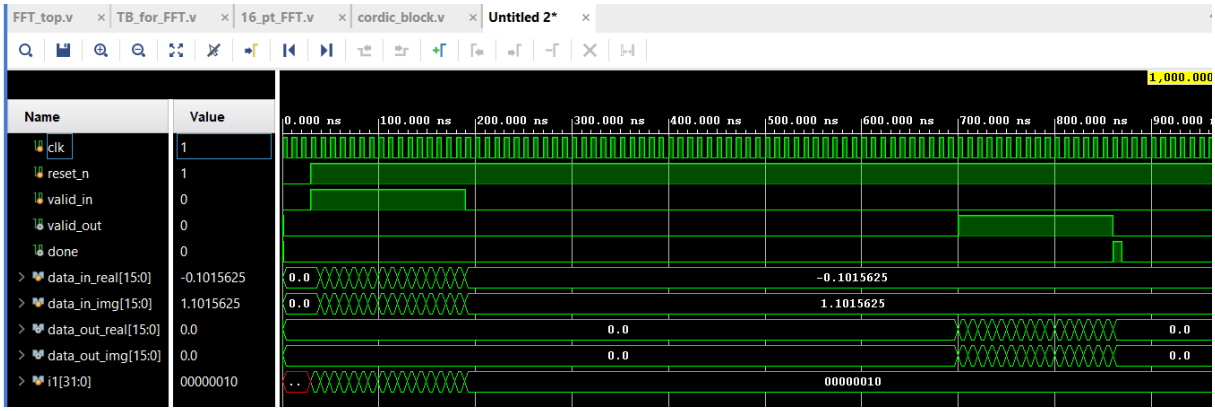

Figure 13: Simulation waveforms

9.1 inputs

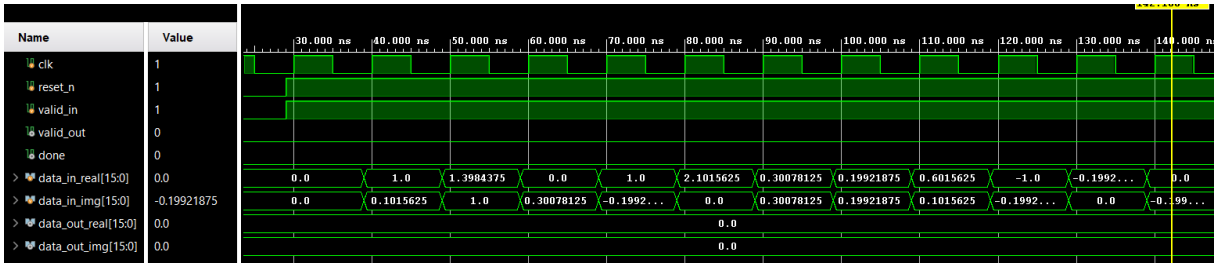

Figure 14: Time Domain Inputs

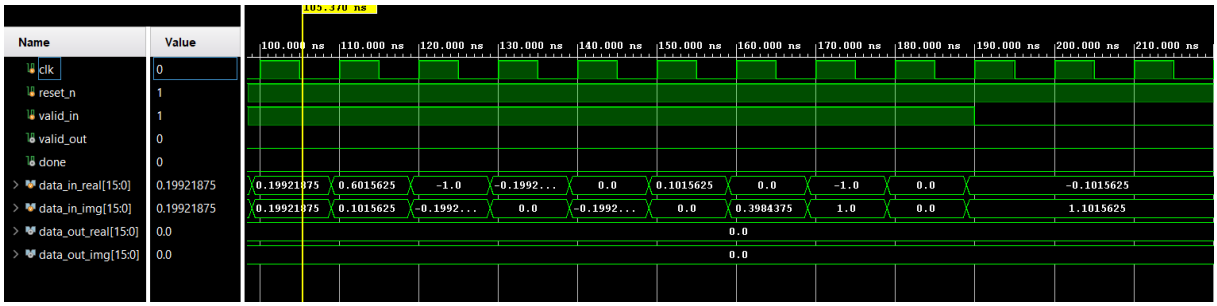

Figure 15: Time Domain Inputs

9.2 Outputs

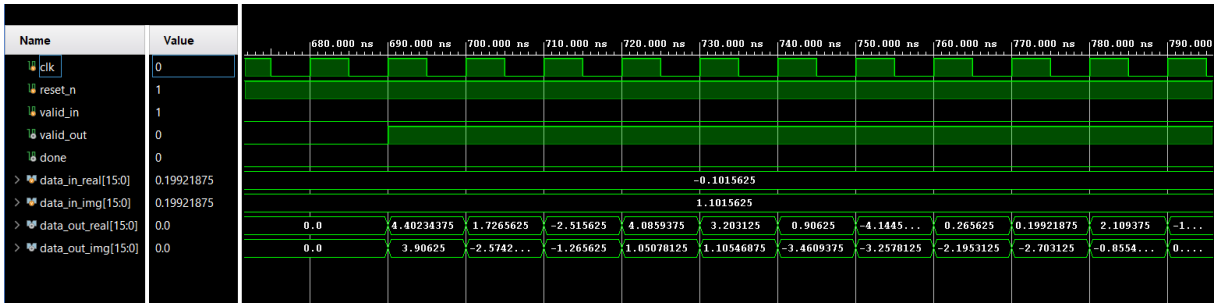

Figure 16: FFT Simulation: Frequency Domain Output

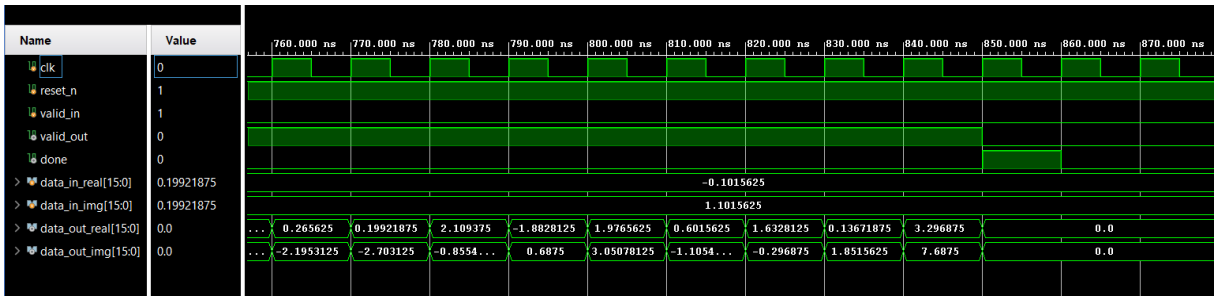

Figure 17: FFT Simulation: Frequency Domain Output