# EE517: ANALOG IC DESIGN LAB

## Analog IC Design Project

## Design and analysis of a 2-stage op-amp.


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EEE - VLSI & NANOELECTRONICS

# Contents

# 1 Project

Design a 2-stage Op-amp in 180 nm technology targeting different target specifications by gm/Id methodology. The following are the general requirements for an Amplifier.

1. High Gain
2. High Gain Band Width (GBW)
3. Low area
4. Low Power

## 1.1 General Specification:

- Supply voltage ($V_{DD}$) = 1.8 V
- Reference current source ($I_{ref}$) = 20 µA
- Slew rate = 1 V/µs
- Phase margin $\geq 60^{\circ}$
- Load capacitance ($C_L$) = 1 pF
- Input Common Mode Range (ICMR) = 0.6-1.4 V

## 1.2 Targeted Outcomes:

- High Gain Bandwidth (GBW)
- Gain $\geq$ 40 dB
- GBW $\geq$ 70 MHz
- Power Dissipation ($P_{diss}$) $\leq$ 1 mW
- Maximum Length ($L_{max}$) $\leq$ 2 µm

# 2 Theory

## 2.1 Introduction

A two-stage operational amplifier consists of two cascaded amplification stages to achieve high gain while maintaining a reasonable output voltage swing. It is commonly used in analog circuit design due to its flexibility and performance.

## 2.2 First Stage: Differential Amplifier

The first stage is a differential amplifier with an active load, responsible for the following Operation:

- Amplifying the differential input signal.
- Attenuating Common Mode signals.
- Providing high gain.
- Converting the differential signal to a single-ended signal.

This stage includes input transistors (M1, M2), active load transistors (M3, M4), and a current source (M5, M8) for biasing.

## 2.3 Second Stage: Gain Stage (CS Amplifier)

The second stage is a common-source amplifier formed by M6, which further amplifies the signal and drives the output load.

### Key Benefits

- Increases the overall gain of the op-amp.
- Provides a better voltage swing at the output compared to a single-stage amplifier.

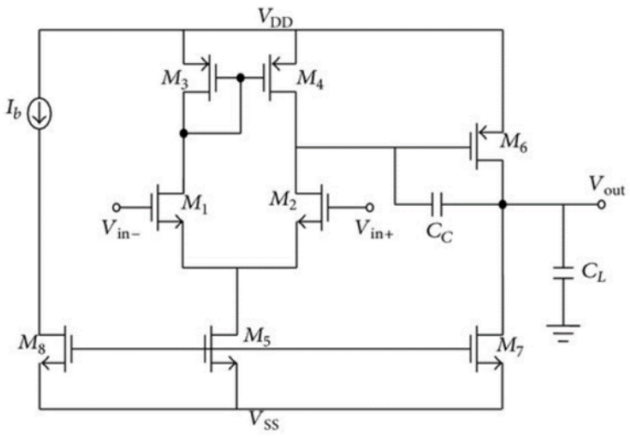



Figure 1: Two Stage Opamp

# 3 Literature Review

## 3.1 Drawbacks of Traditional Design Methodology

Traditional approaches to analog IC design often rely on simplified square-law equations for MOSFET behavior, assuming ideal conditions that neglect various second-order effects. These shortcomings include:

1. Ignoring short-channel effects such as velocity saturation and drain-induced barrier lowering.
2. Neglecting the dependence of threshold voltage ($V_{TH}$) on device dimensions such as Width and Length of the Channel and bias conditions.
3. Threshold Voltage also depends heavily on Source Node Voltage, assuming all the Body Terminals are connected to either Vdd (for PMOS) and gnd (for NMOS ).
4. Oversimplification of channel-length modulation, leading to inaccuracies in gain calculations.

Such assumptions result in significant discrepancies between theoretical predictions and actual performance, particularly for modern sub-micron processes. To overcome these limitations, the gm/Id methodology offers a more accurate and comprehensive approach to transistor characterization and design.

## 3.2 gm/Id Methodology

The gm/Id methodology provides a systematic framework for analog circuit design by directly leveraging the transconductance efficiency ($gm/I_d$) as a key design parameter. This approach involves the following steps:

1. Characterize MOSFETs by simulating various operating points to obtain the following plots:
   - Transconductance ($gm$) versus gate-source voltage ($V_{GS}$).
   - Drain current ($I_d$) versus gate-source voltage ($V_{GS}$).
   - Transconductance efficiency ($gm/I_d$) versus gate-source voltage ($V_{GS}$).
2. Extract derived parameters such as:
   - Intrinsic gain: $\frac{gm}{g_{ds}}$, representing the maximum achievable gain.
   - Transit frequency: $\frac{gm}{2\pi C_{gs}}$, indicating the bandwidth potential.
3. Use these plots to design devices for optimal performance metrics tailored to the application requirements.

The gm/Id charts serve as lookup tables, enabling precise calculations and bridging the gap between simulation results and analytical design.

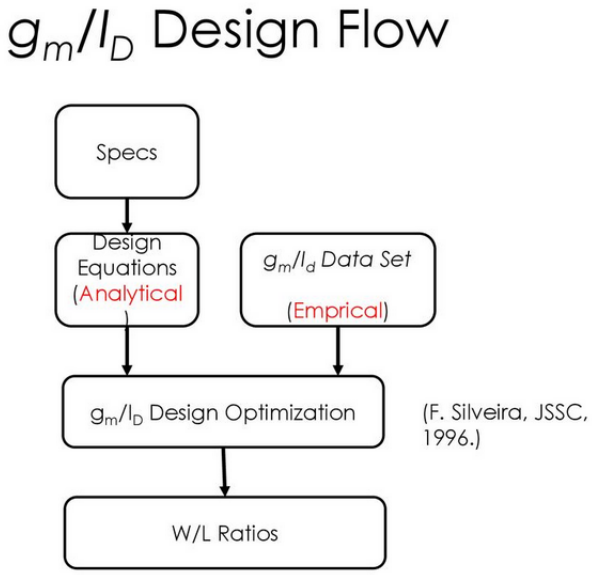



Figure 2: Flow Chart of gm/Id Methodology

### 3.3 Using gm/Id Charts for Circuit Design

The gm/Id methodology simplifies analog circuit design by leveraging the efficiency of transconductance-to-current ratio ($gm/I_d$). This parameter remains largely independent of the transistor's aspect ratio when the gate overdrive voltage ($V_{GS} - V_{TH}$) is greater than zero. Key considerations for implementing this approach include:

1. Selection of gm/Id Values:
    - A smaller gm/Id is suitable for devices that do not contribute directly to gain, such as active loads, or when compact area and high speed are desired.
    - A larger gm/Id is preferable for gain-contributing devices, such as the input stage of an amplifier, or when low flicker noise, better mismatch, and large voltage swings are required.
2. Device Parameters:
    - Drain current ($I_d$): Chosen based on the power budget.
    - Channel length ($L$): Set to ensure that intrinsic gain ($gm/g_{ds}$) meets the required specifications. Excessive values of $gm/g_{ds}$ may lead to reduced bandwidth due to lower $f_T$, necessitating careful trade-off analysis.
    - Width ($W$): Determined from the $I_d/W$ versus $gm/I_d$ chart after selecting $I_d$.
    - DC Operating Voltage: Extracted from the $gm/I_d$ versus $V_{OV}$ chart to ensure consistent operation at the specified $gm/I_d$ value.

This systematic design approach bridges the gap between theoretical insights and practical implementation, providing a robust framework for achieving optimal circuit performance.

# 4 MOSFET Characterization

## 4.1 Simulation Setup

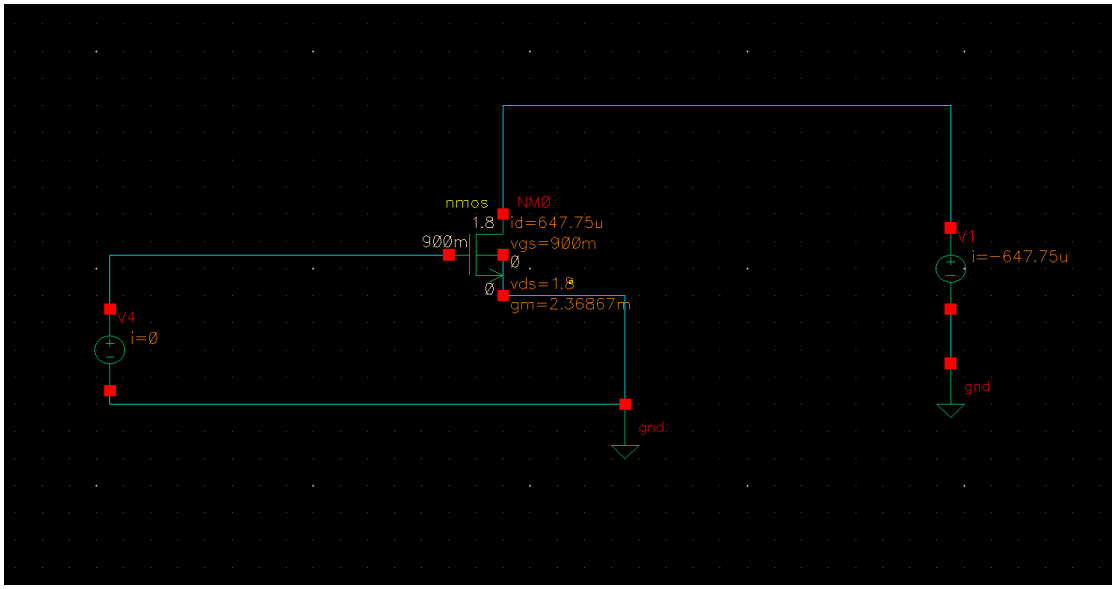



Figure 3: Schematic of NMOS characterization simulation setup

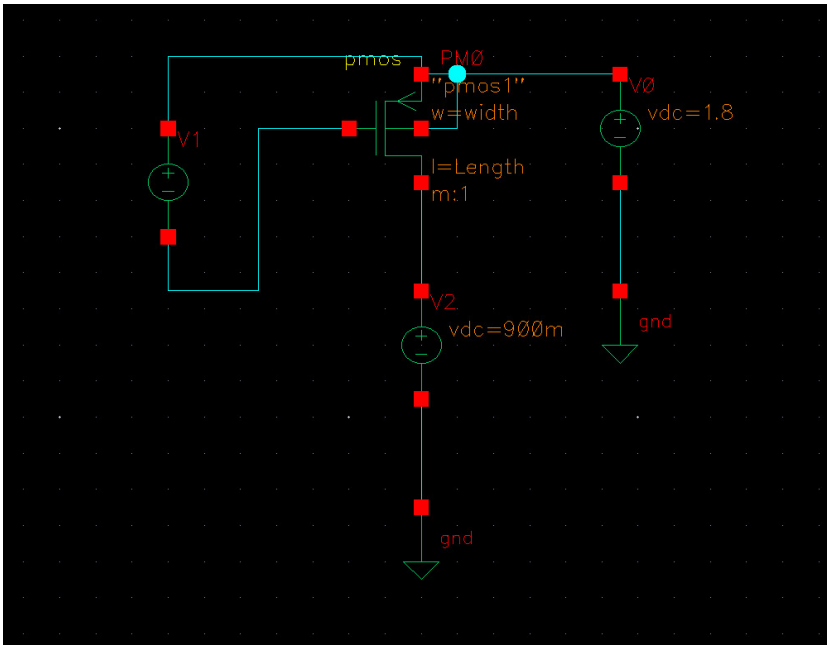



Figure 4: Schematic of PMOS characterization simulation setup

## 4.2 Procedure

- **Step 1:** Plot $I_D$, $g_m$, $g_m/I_D$, $f_T$, $g_m/g_{ds}$, $V_{ov}$ and $I_D/W$ versus $V_{GS}$.
- **Step 2:** From the above data, the $g_m/I_D$ charts can be generated for the PMOS and NMOS transistors. These include the following plots:
  1. $g_m/I_D$ versus $V_{ov}$
  2. $f_T$ versus $g_m/I_D$
  3. $g_m/g_{ds}$ versus $g_m/I_D$
  4. $I_D/W$ versus $g_m/I_D$

## 4.3 NMOS Characterization Plots

### 4.3.1 Plots w.r.t $V_{GS}$

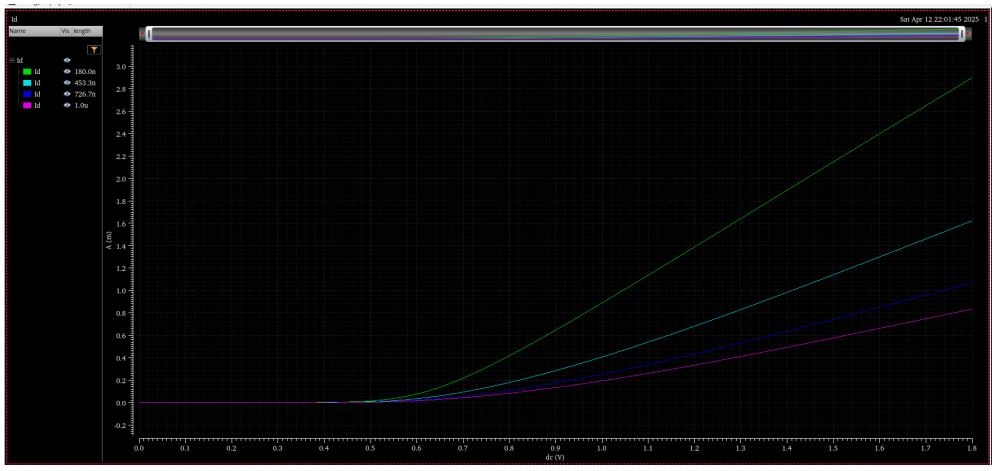


Figure 5: Drain current ($I_D$) vs $V_{GS}$

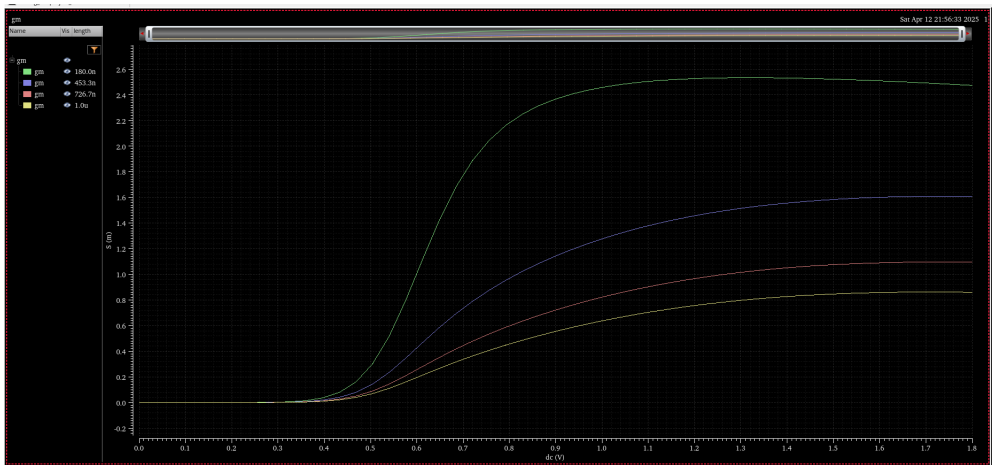


Figure 6: Transconductance ($g_m$) vs $V_{GS}$

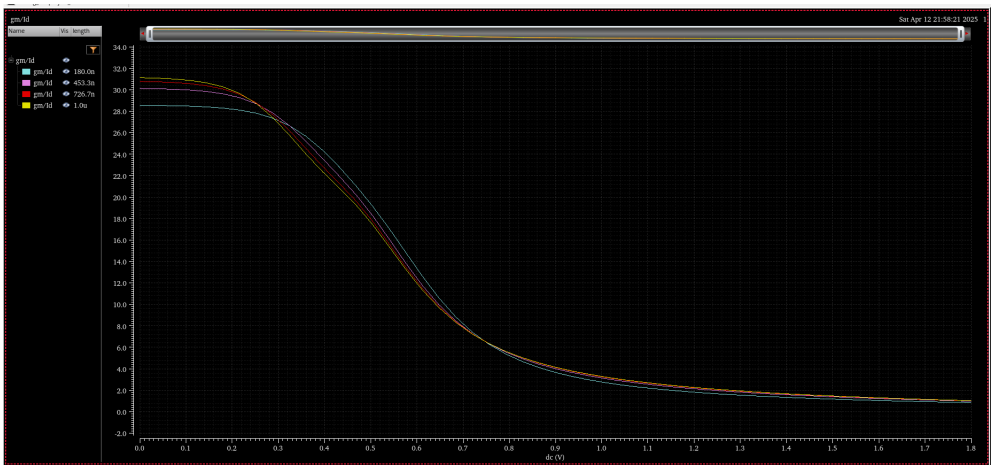



Figure 7: Transconductance efficiency ($g_m/I_D$) vs $V_{GS}$

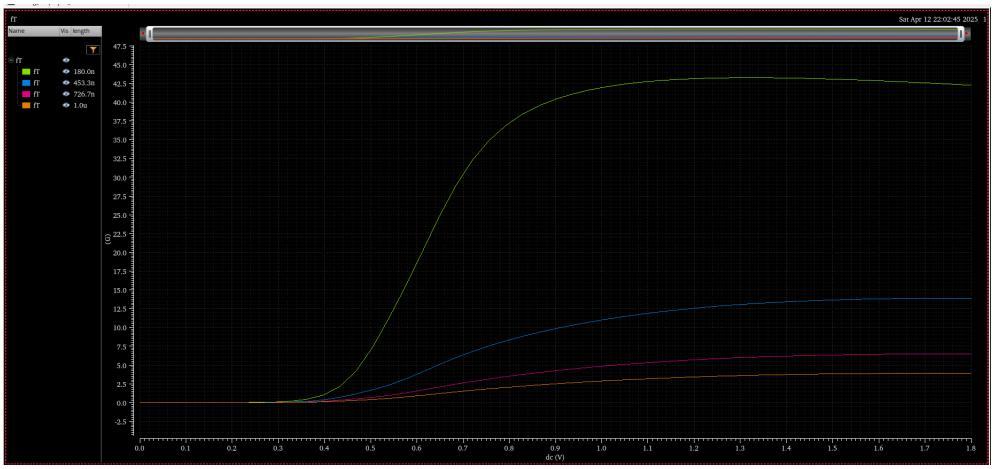



Figure 8: Transition frequency ($f_T$) vs $V_{GS}$

### 4.3.2 $g_m/I_D$ Plots

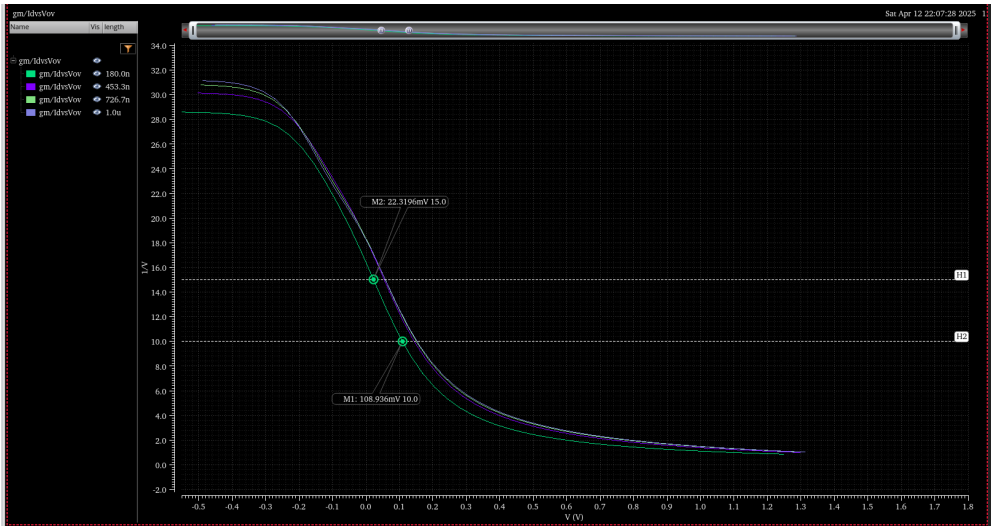



Figure 9: $g_m/I_D$ vs $V_{OV}$

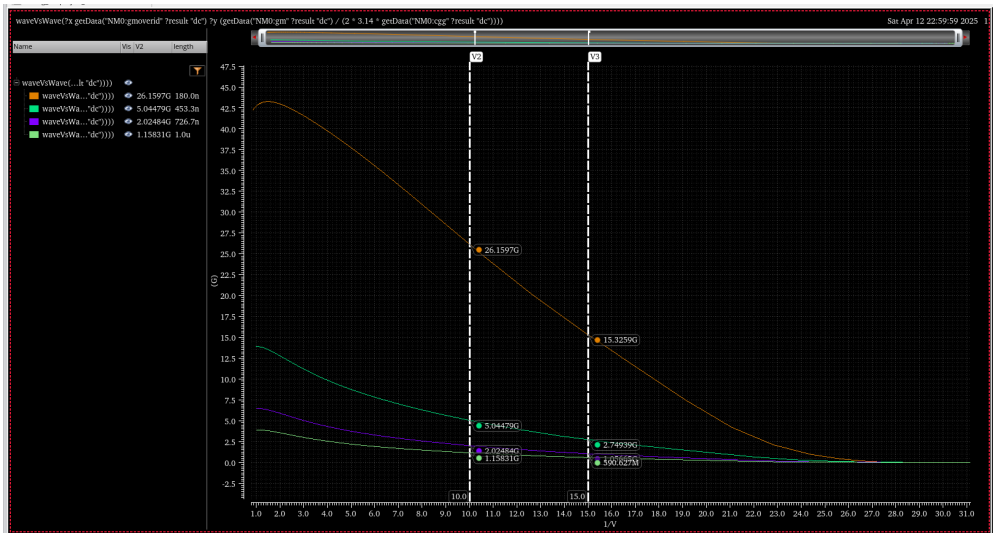



Figure 10: $f_T$ vs $g_m/I_D$

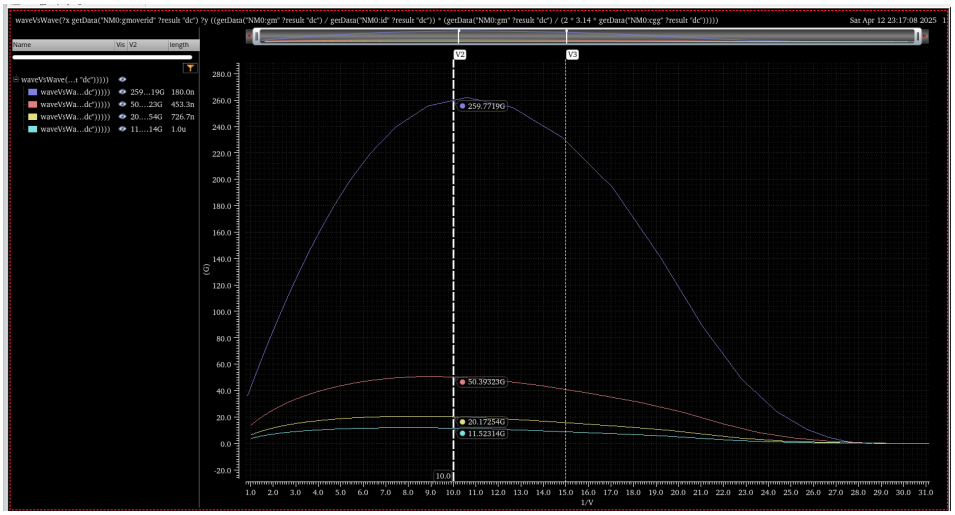



Figure 11: $f_T \cdot (g_m/I_D)$ vs $g_m/I_D$

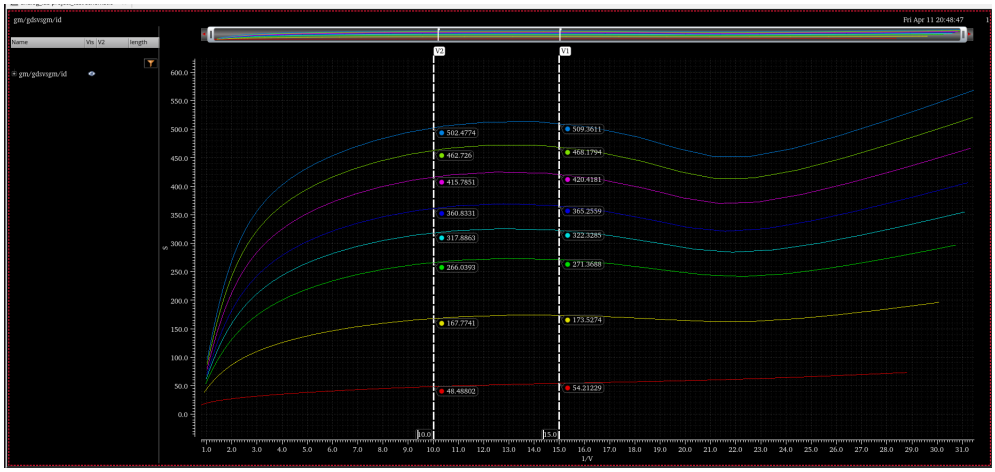



Figure 12: $g_m/g_{ds}$ vs $g_m/I_D$

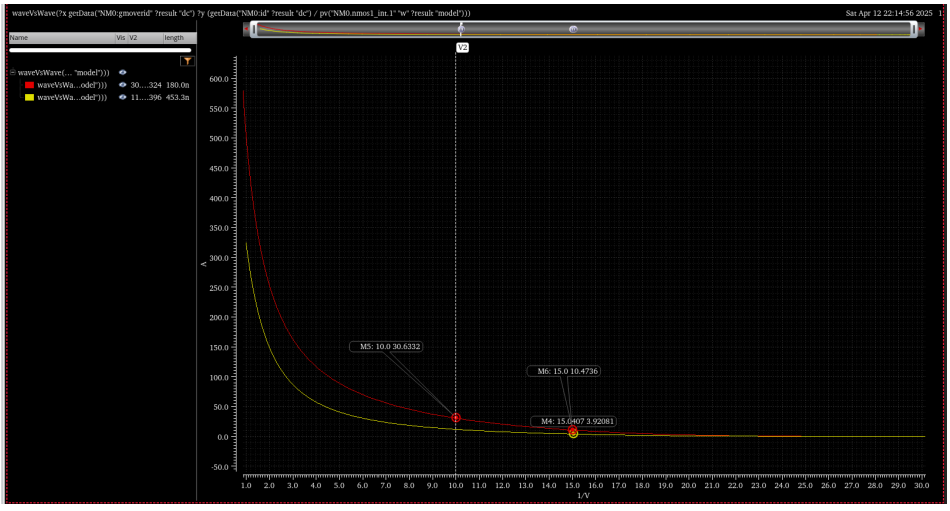



Figure 13: $I_D/W$ vs $g_m/I_D$

## 4.4 PMOS Characterization Plots

### 4.4.1 Plots w.r.t $V_{GS}$

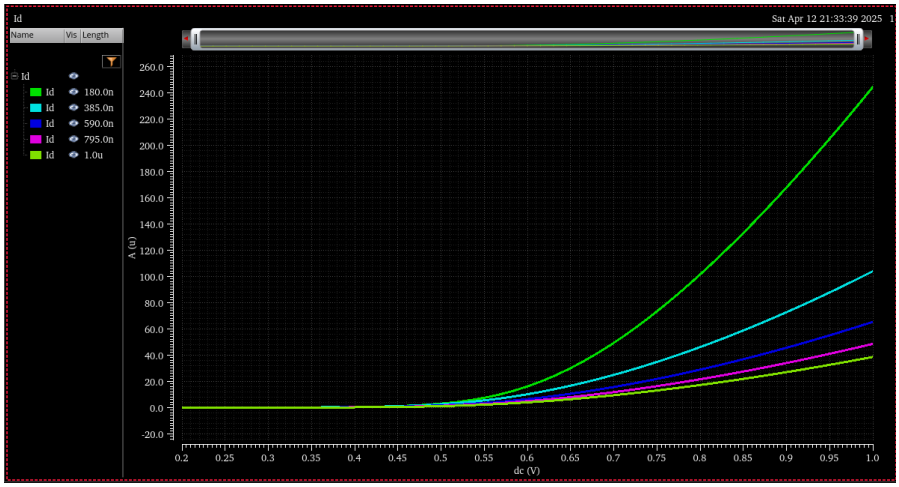



Figure 14: Drain current ($I_D$) vs $V_{GS}$

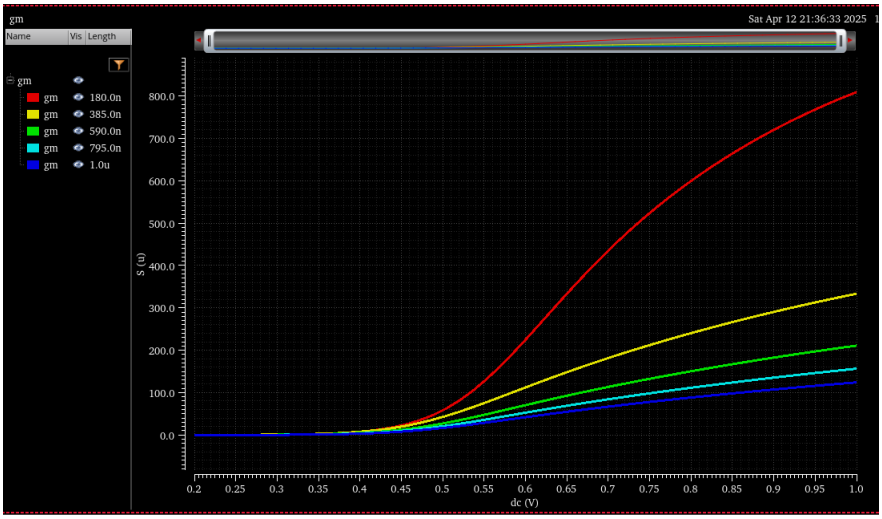



Figure 15: Transconductance ($g_m$) vs $V_{GS}$

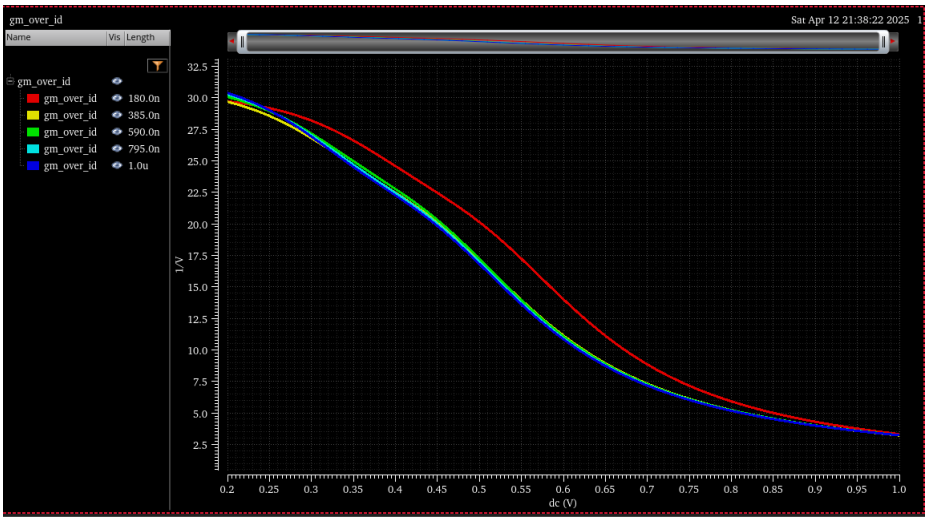



Figure 16: Transconductance efficiency ($g_m/I_D$) vs $V_{GS}$

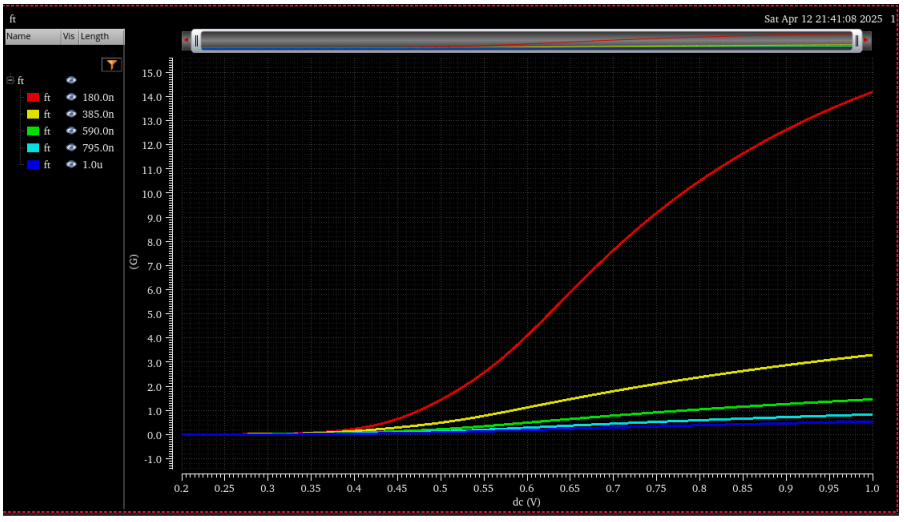



Figure 17: Transition frequency ($f_T$) vs $V_{GS}$

### 4.4.2 $g_m/I_D$ Plots

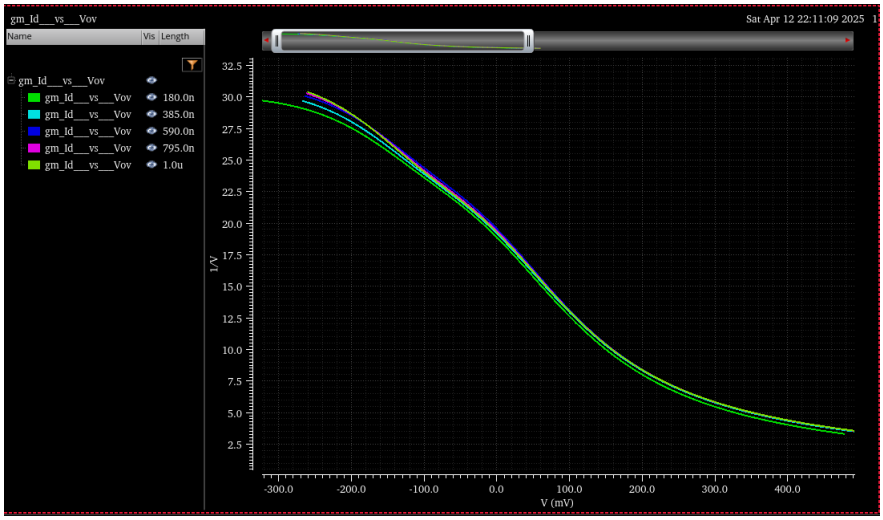



Figure 18: $g_m/I_D$ vs $V_{OV}$

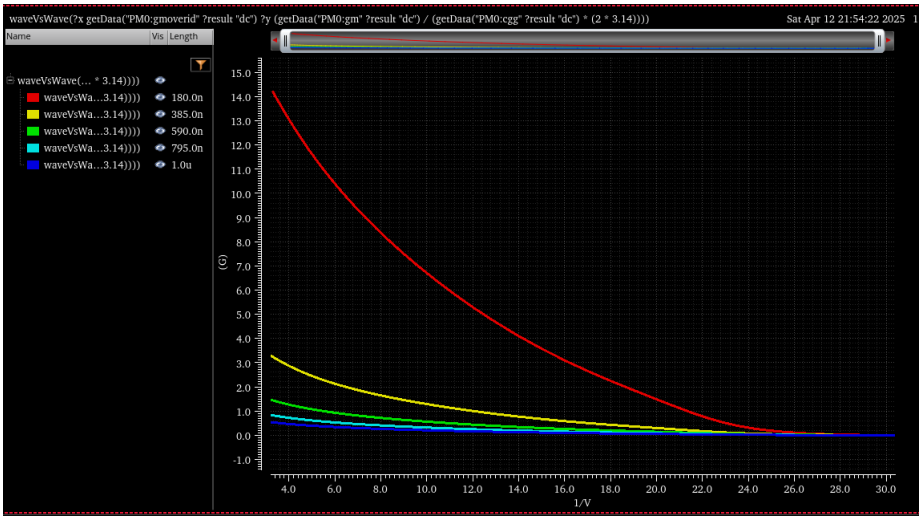



Figure 19: $f_T$ vs $g_m/I_D$

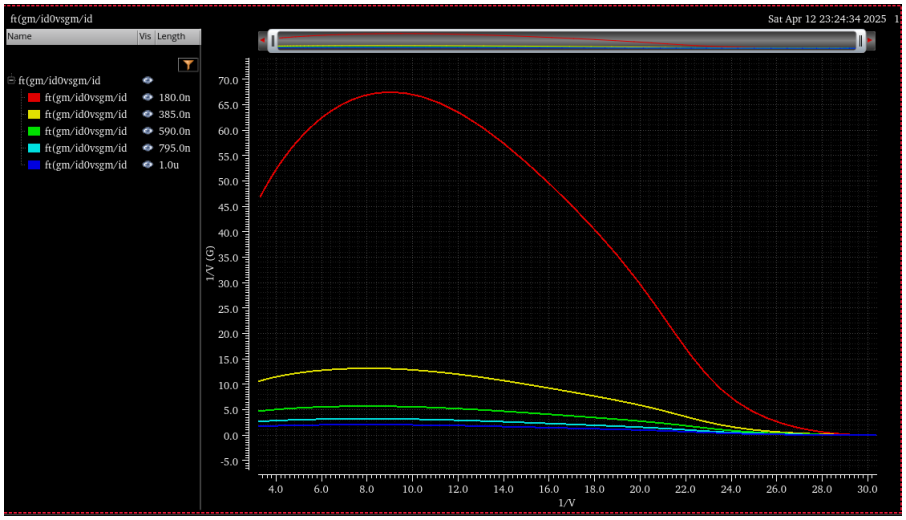



Figure 20: $f_T \cdot (g_m/I_D)$ vs $g_m/I_D$

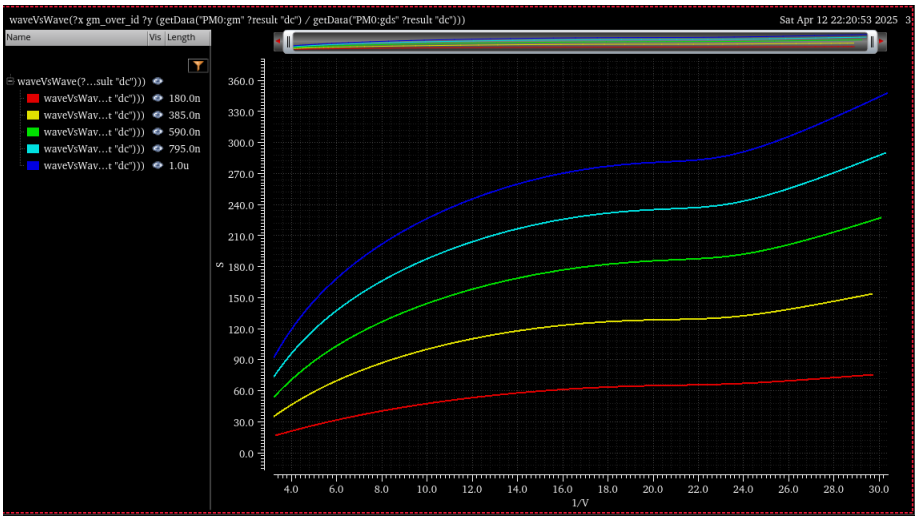



Figure 21: $g_m/g_{ds}$ vs $g_m/I_D$

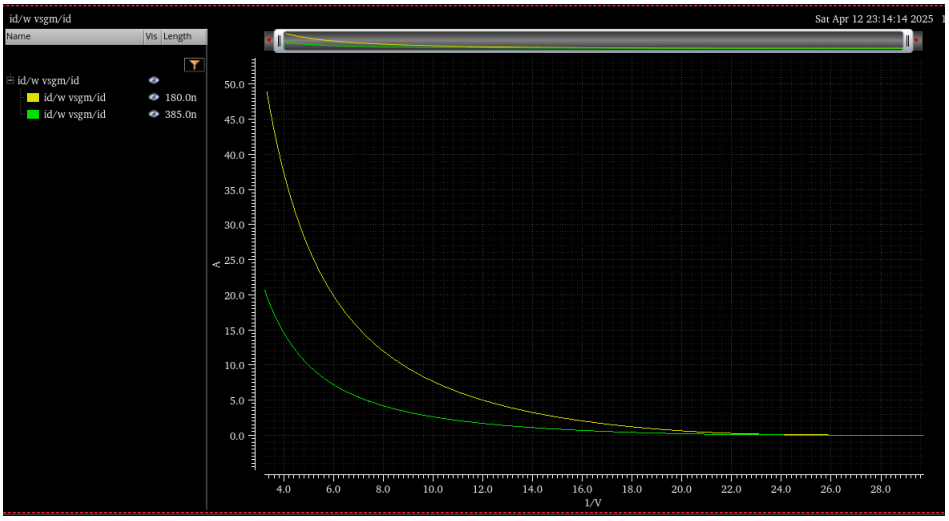



Figure 22: $I_D/W$ vs $g_m/I_D$

# 5 Hand Calculations

# Two-Stage Op-Amp Design Calculations

## Step 1: Compensation Capacitor ($C_c$) Selection

Given:

$$C_L = 1 \text{ pF}$$

Theoritical calculation for a phase margin of 60 degrees in a two-stage op-amp:

$$C_c \geq 0.22 \cdot C_L \Rightarrow C_c \geq 0.22 \cdot 1 \text{ pF} = 220 \text{ fF}$$

We select slightly higher value of Cc considering the effect of parasitic capacitance,

$$C_c = 330 \text{ fF}$$

## Step 2: Transconductance Calculations for Required GBW

Given:

$$\text{Target GBW} \geq 70 \text{ MHz}, \quad \text{Assume } GBW = 100 \text{ MHz}$$

For a two-stage op-amp:

**Input Transconductance $g_{m1}$**

$$g_{m1} = 2\pi \cdot GBW \cdot C_c = 2\pi \cdot 100 \times 10^6 \text{ Hz} \cdot 330 \times 10^{-15} \text{ F}$$
$$g_{m1} = 207.345 \ \mu\text{A/V}$$

**Second Stage Transconductance $g_{m2}$**

$$g_{m2} \geq 2.2 \cdot 2\pi \cdot GBW \cdot C_L = 2.2 \cdot 2\pi \cdot 100 \times 10^6 \text{ Hz} \cdot 1 \times 10^{-12} \text{ F}$$
$$g_{m2} = 1381.6 \ \mu\text{A/V}$$

## Step 3: Bias Currents Using $g_m/I_D$

Assumed:

- $g_m/I_D = 15$ for $M_1$, $M_2$, and $M_6$
- $g_m/I_D = 10$ for all other transistors

**Currents for $M_1$, $M_2$**

$$I_{D1} = \frac{g_{m1}}{g_m/I_D} = \frac{207.345 \ \mu\text{A/V}}{15} = 13.823 \ \mu\text{A}$$
$$I_{D2} = I_{D1} = 13.823 \ \mu\text{A}$$

**Current for $M_6$**

$$I_{D6} = \frac{g_{m2}}{g_m/I_D} = \frac{1381.6 \ \mu\text{A/V}}{15} = 92.1066 \ \mu\text{A}$$

## Step 4: Transistor Sizing Using $I_D/W$ Graph

From the graph of $I_D/W$ vs $g_m/I_D$:

- For $g_m/I_D = 15$, $I_D/W = 10.4736$ for $M_1$, $M_2$(NMOS)
- For $g_m/I_D = 15$, $I_D/W = 2.56264$ for $M_6$(PMOS)
- For $g_m/I_D = 10$, $I_D/W = 7.6443$ for $M_3$, $M_4$(PMOS)
- For $g_m/I_D = 10$, $I_D/W = 30.633$ for $M_5$(NMOS)

**Widths of $M_1$, $M_2$**

$$W_1 = W_2 = \frac{I_{D1}}{I_D/W} = \frac{13.823\ \mu\text{A}}{10.4736} = 1.32\ \mu\text{m}$$

**Width of $M_6$**

$$W_6 = \frac{I_{D6}}{I_D/W} = \frac{92.1066\ \mu\text{A}}{2.56264} = 35.94\ \mu\text{m}$$

**Widths of $M_3$, $M_4$**

$$W_3 = W_4 = \frac{I_{D3}}{I_D/W} = \frac{13.823\ \mu\text{A}}{7.6443} = 1.808\ \mu\text{m}$$

**Width of $M_5$**

$$I_{D5} = I_{D1} + I_{D2} = 27.646\ \mu\text{A}$$

$$W_5 = \frac{I_{D5}}{I_D/W} = \frac{27.646\ \mu\text{A}}{30.633} = 0.9025\ \mu\text{m}$$

**Width of $M_7$**

$$W_7 = \frac{I_{D7}}{I_D/W} = \frac{92.1066\ \mu\text{A}}{7.6433} = 12.048\ \mu\text{m}$$

## Step 5: Channel Length Selection

As per the $g_m/g_{ds}$ vs $g_m/I_D$ graph, we choose the channel length for all transistors as:

$$L = 180\ \text{nm}$$

# 6 Two Stage Op-amp Design Procedure

## 6.1 Problem Statement

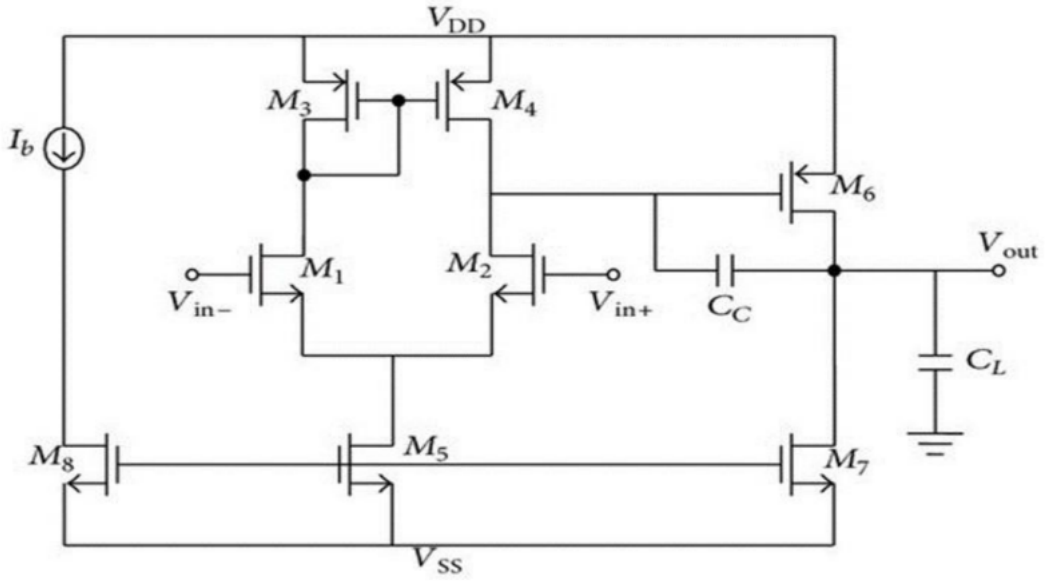



Figure 23: Circuit Diagram of Two Stage Op-amp

Design a basic two-stage op-amp based on the following specifications:

- Open loop voltage gain $\geq 40dB$
- Unity gain frequency $\geq 70MHz$
- Phase margin $\geq 60°$
- ICMR : 0.6V - 1.4V
- Power dissipation $\leq 1mW$

Consider $V_{DD} = 1.8V$ and load capacitance $C_L = 1pF$.

## 6.2 Schematic

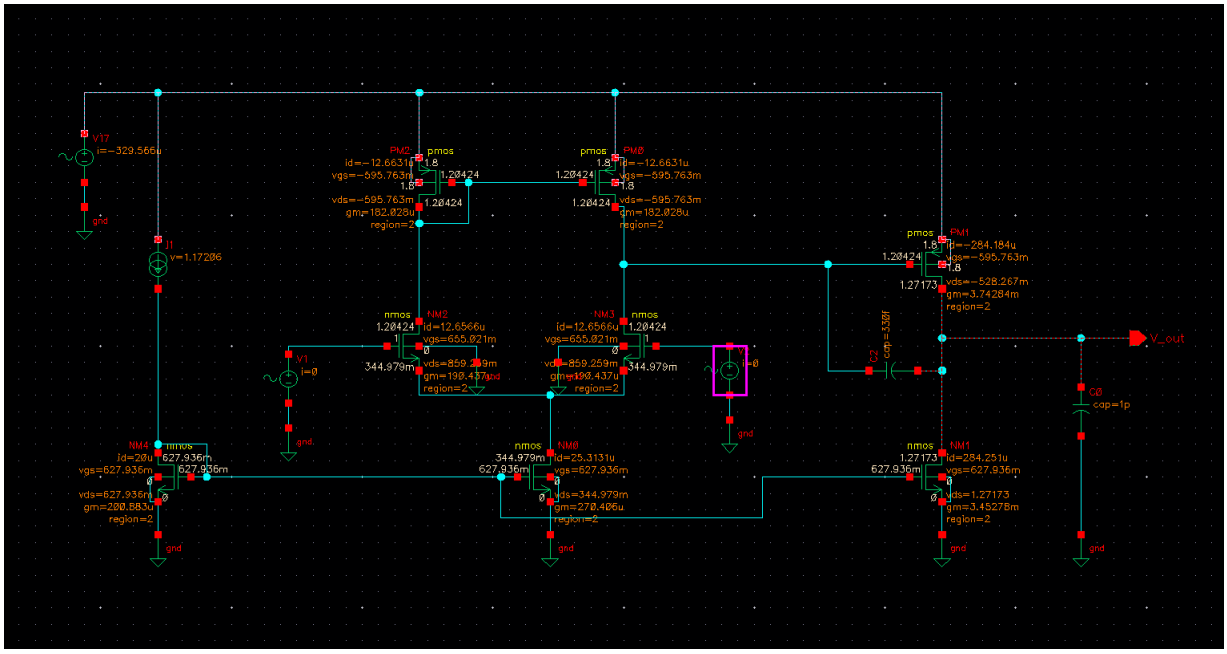



Figure 24: Schematic in Cadence of Two Stage Op-amp

## 6.3 Design Methodology

The design process for the two-stage operational amplifier involves the following key steps:

1. Determine the $g_m/I_d$ values for each transistor. These are generally chosen between 10 and 20, based on their specific roles in the circuit.

2. For transistors contributing to the gain ($M_1, M_2, M_6$), higher $g_m/I_d$ values are preferred, while current source load transistors benefit from lower values.

3. Begin the design by assigning typical $g_m/I_d$ values: 15 for gain-contributing transistors and 10 for others.

4. Select transistor lengths based on $g_m/g_{ds}$ versus $g_m/I_d$ curves for various channel lengths. Hand calculations can help determine the minimum length that meets gain requirements.

5. Use the power budget to calculate current through each transistor, deriving transistor widths from the $I_d/W$ versus $g_m/I_d$ chart.

6. Verify bandwidth requirements by consulting the $f_T$ versus $g_m/I_d$ curve for the chosen $L$ and $g_m/I_d$.

7. Once transistor dimensions are finalized, obtain bias voltages using $g_m/I_d$ versus $V_{ov}$ charts.

## 6.4 Device Size Calculation

1. The total power consumption is set to 1mW, corresponding to a bias current limit of 550$\mu$A. A current mirror biasing strategy is applied, allocating 20$\mu$A to the bias transistor. The tail current for the differential stage and the current for the common-source stage are set to 27.5$\mu$A and 92.10$\mu$A respectively.

2. Aiming for an open-loop gain of 100, assuming differential stage gain to be 10 and common source stage gain to be 10. the intrinsic gain ($g_m/g_{ds}$) is at 20. Transistor length $L$ is initially chosen 180nm as minimum channel length yeilded the required gain.

3. For transistors $M_1$ and $M_2$, the $I_d/W$ ratio derived from $g_m/I_d$ charts (at $g_m/I_d = 15$) is 10.4736, leading to $W_{M_1} = W_{M_2} = 1.31823\mu$m.

4. For $M_3$ and $M_4$, the $I_d/W$ ratio at $g_m/I_d = 10$ is 7.64435, giving $W_{M_3} = W_{M_4} = 1.80\mu$m.

5. For $M_6$ with $I_d/W$ at $g_m/I_d = 15$ being 2.56264, the width is $W_{M_6} = 35.94$m .

6. For $M_7$ with $I_d/W$ at $g_m/I_d = 10$ being 7.64435, the width is $W_{M_7} = 12.048$m .

7. For $M_5 with \mathrm{I}_d/W$ at $g_m/I_d = 10$ being 30.63324, the width is $W_{M_5} = 900$nm .

## 6.5 Miller Compensation

Assuming $p_1$, $p_2$ denote the dominant poles, $z$ the zero, $GBP$ the gain-bandwidth product, and $PM$ the phase margin of the op-amp, we calculate:

$$PM = 180^\circ - \tan^{-1}\left(\frac{GBP}{p_1}\right) - \tan^{-1}\left(\frac{GBP}{p_2}\right) - \tan^{-1}\left(\frac{GBP}{z}\right) \tag{1}$$

Given $\tan^{-1}\left(\frac{GBP}{p_1}\right) \approx 90^\circ$, we require $p_2 = 2.2GBP$ for a 60° phase margin. Using:

Where,

$$p_1 = \frac{1}{g_{m6}R_1R_2C_c}$$

$$p_2 = \frac{g_{m6}}{2\pi C_L}$$

$$z = \frac{g_{m6}}{2\pi C_c}$$

**Assumption:**

- As zero is right hand plane zero , it makes the system unstable. It adds $-90^\circ$ to phase margin hence it should be atleast 10 times of GBP. To minimize its effect on phase margin.

**Phase Margin Calculation:**

$$PM = 180^\circ - \tan^{-1}\left(\frac{GBP}{p_1}\right) - \tan^{-1}\left(\frac{GBP}{p_2}\right) - \tan^{-1}\left(\frac{GBP}{z}\right) \tag{2}$$

Where,

$$\tan^{-1}\left(\frac{GBP}{z}\right) = 5.71^\circ$$

$$PM = 180^\circ - 90^\circ - 5.71^\circ - \tan^{-1}\left(\frac{GBP}{P_2}\right)$$

Thus,

$$PM = 84.29^\circ - \tan^{-1}\left(\frac{GBP}{P_2}\right)$$

For a desired phase margin of 60°:

$$\frac{GBP}{P_2} = \tan\left(24.29^\circ\right)$$

$$\frac{GBP}{P_2} = 0.4153$$

$$P_2 >= 2.2 \times GBP$$

Hence, $P_2$ should be at least $2.2 \times GBP$ for a phase margin of 60°.

$$P_2 = \frac{g_{m6}}{2\pi C_L}$$

$$GBP = \frac{g_{m1}}{2\pi C_C}$$

$$P_2 = \frac{g_{m6}}{2\pi C_L}$$

$$\text{GBP} = \frac{g_{m1}}{2\pi C_L}$$

$$\frac{g_{m6}}{2\pi C_L} \geq 2.2\left(\frac{g_{m1}}{2\pi C_L}\right)$$

$$g_{m6} \geq 10 g_{m1}$$

As mentioned above,

$$g_{m6} \geq 10 g_{m1}$$

$$C_c \geq 0.22 C_L$$

## 6.6 Design Summary

Below is the summary of the device dimensions and operating conditions:

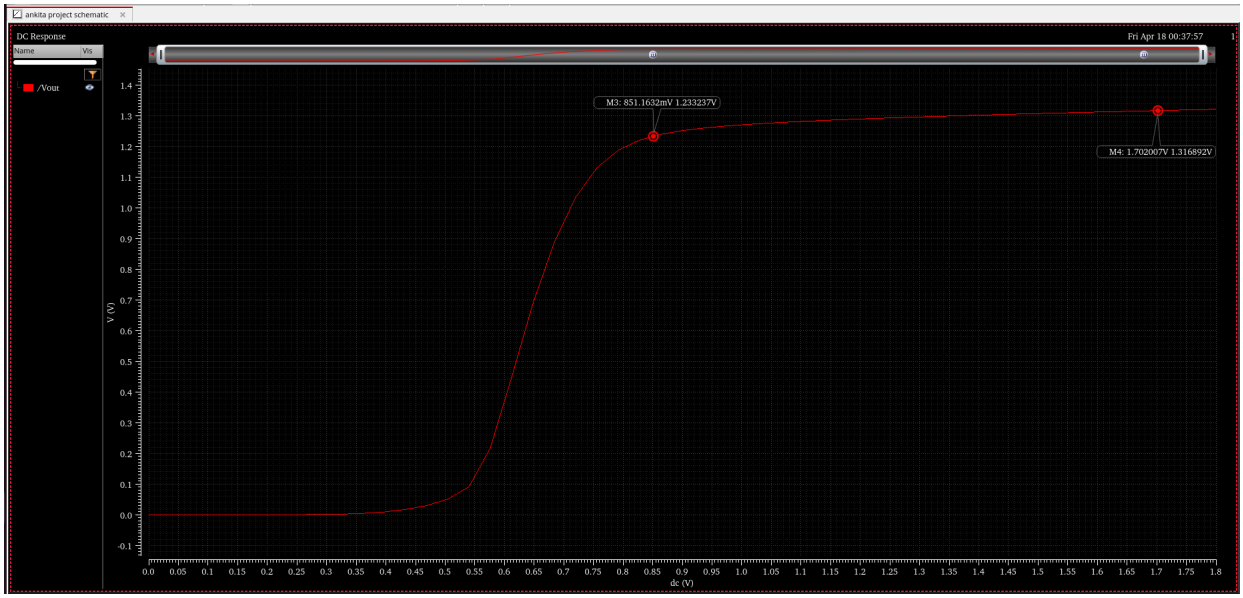
| Device | $L$ (nm) | $W$ ($\mu$m) | $g_m/I_d$ ($V^{-1}$) | $I_d$ ($\mu$A) |
|---|---|---|---|---|
| $M_1$ | 180 | 1.3 | 15.17 | 12.657 |
| $M_2$ | 180 | 1.3 | 15 | 12.657 |
| $M_3$ | 180 | 4.54 | 14.376 | 12.657 |
| $M_4$ | 180 | 4.54 | 14.376 | 12.657 |
| $M_5$ | 1000 | 6.02 | 10.683 | 25.314 |
| $M_6$ | 180 | 72 | 14.17 | 284.178 |
| $M_7$ | 180 | 15 | 12.1 | 284.178 |

Table 1: Device dimensions and operating currents

# 7 Simulation Results

## 7.1 DC Analysis

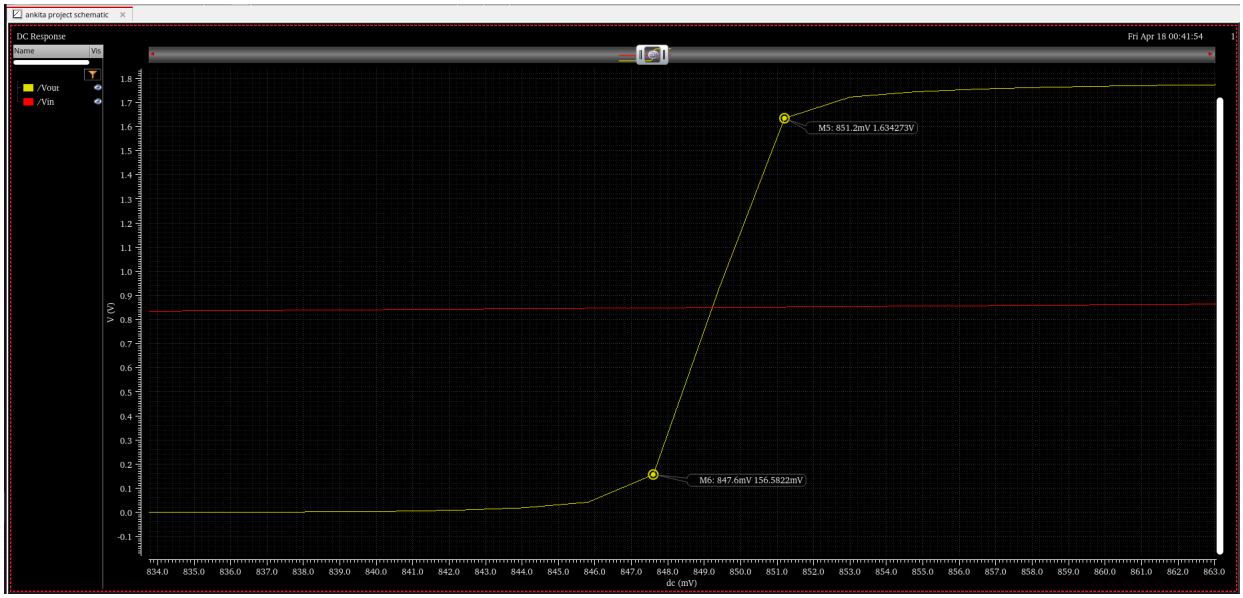
### 7.1.1 ICMR and OCMR



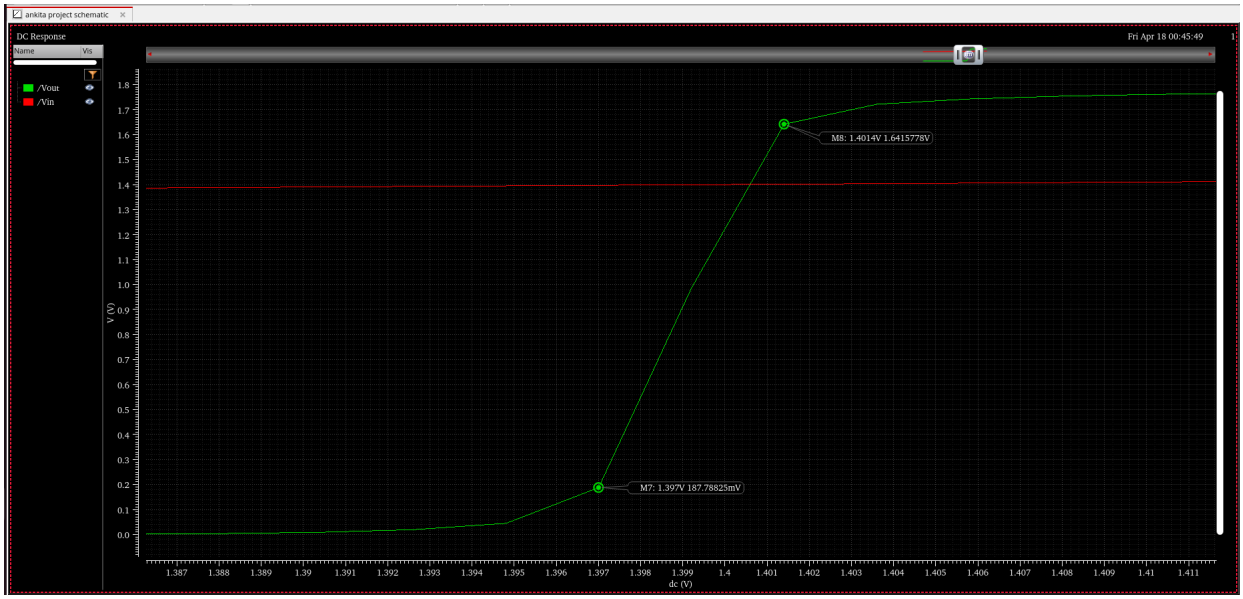

| ICMR | 851.163mV - 1.702V |
|---|---|
| OCMR | 1.233V - 1.316V |

### 7.1.2 Output Swing

**At input common mode voltage of 850mV**



**At input common mode voltage of 1.4V**




| Input Common Mode Voltage | Output Swing |
|---|---|
| 850mV | 156.582mV - 1.6343V |
| 1.4V | 187.788mV - 1.6415V |

## 7.2 Summary of DC Parameters

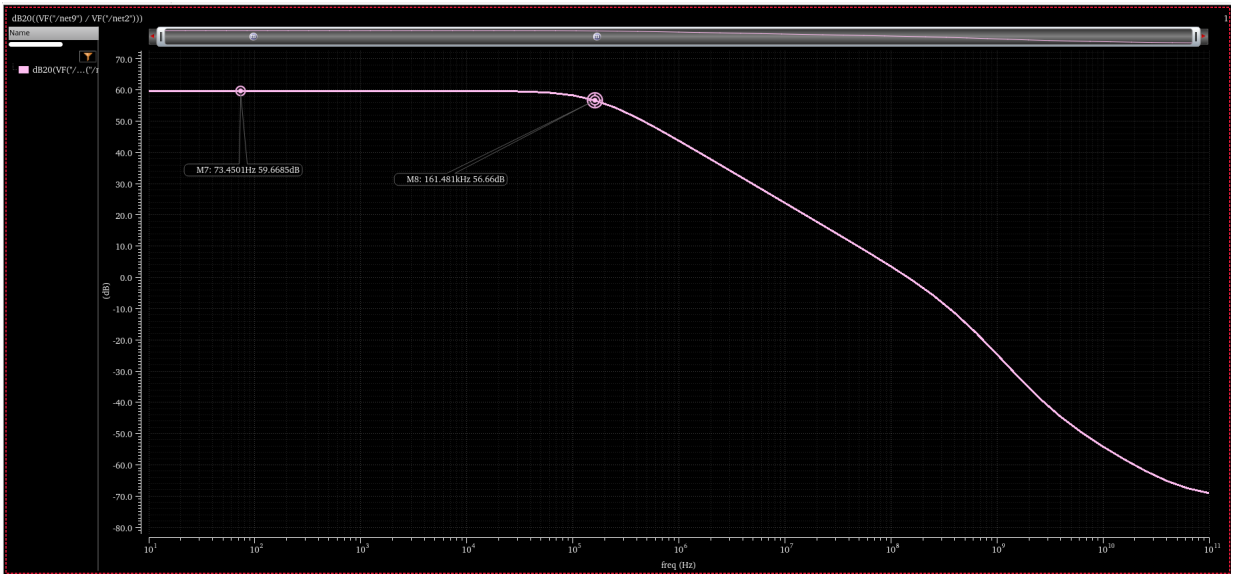
The DC performance parameters of the op-amp as obtained from the DC analysis are enlisted below:

1. DC differential-mode gain = 794
2. DC common-mode gain = 0.48
3. Worst case CMRR = 64.25 dB
4. Lower saturation limit = 74.73mV
5. Upper saturation limit = 1.72 V
6. Power dissipation = 581 $\mu$W

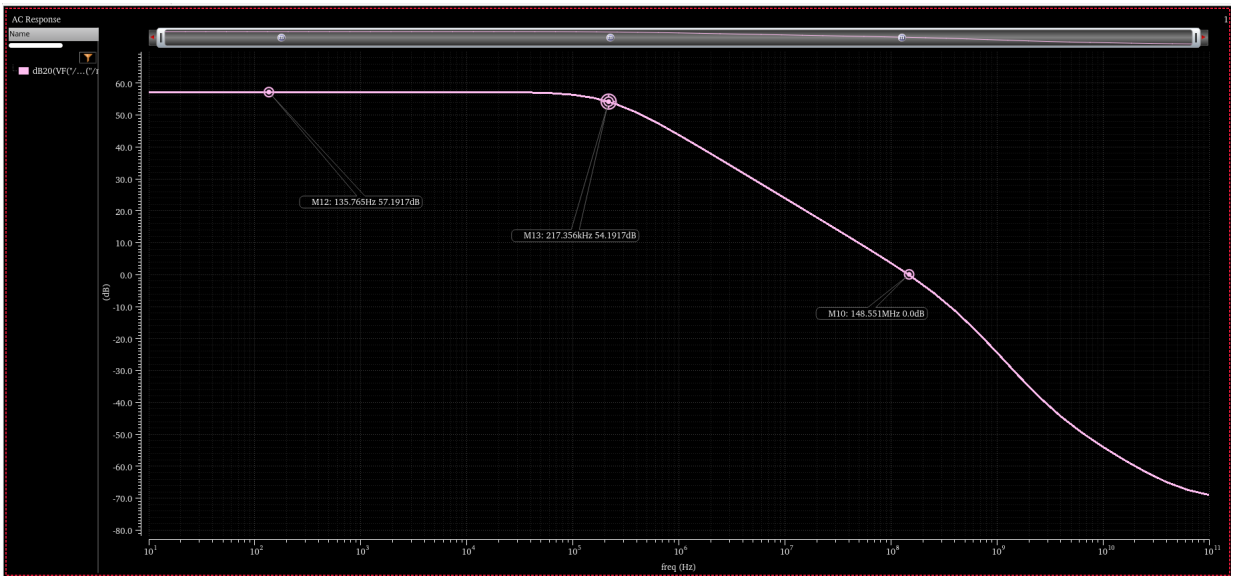
## 7.3 AC Analysis

### 7.3.1 Gain and 3dB Bandwidth

**At input common mode voltage of 850mV**



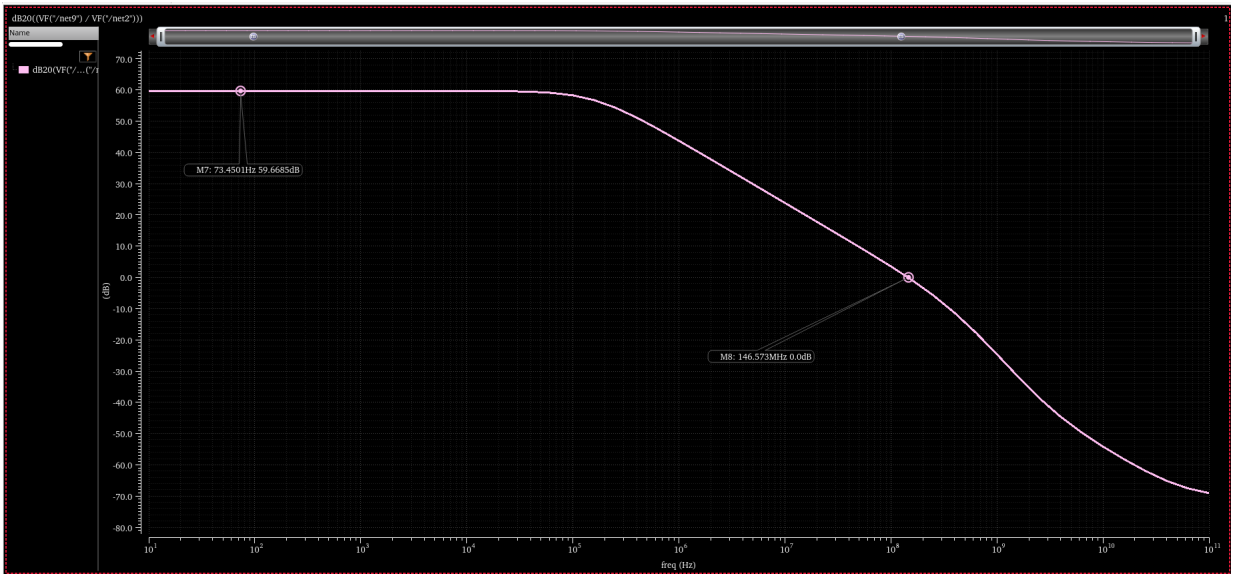

**At input common mode voltage of 1.4V**



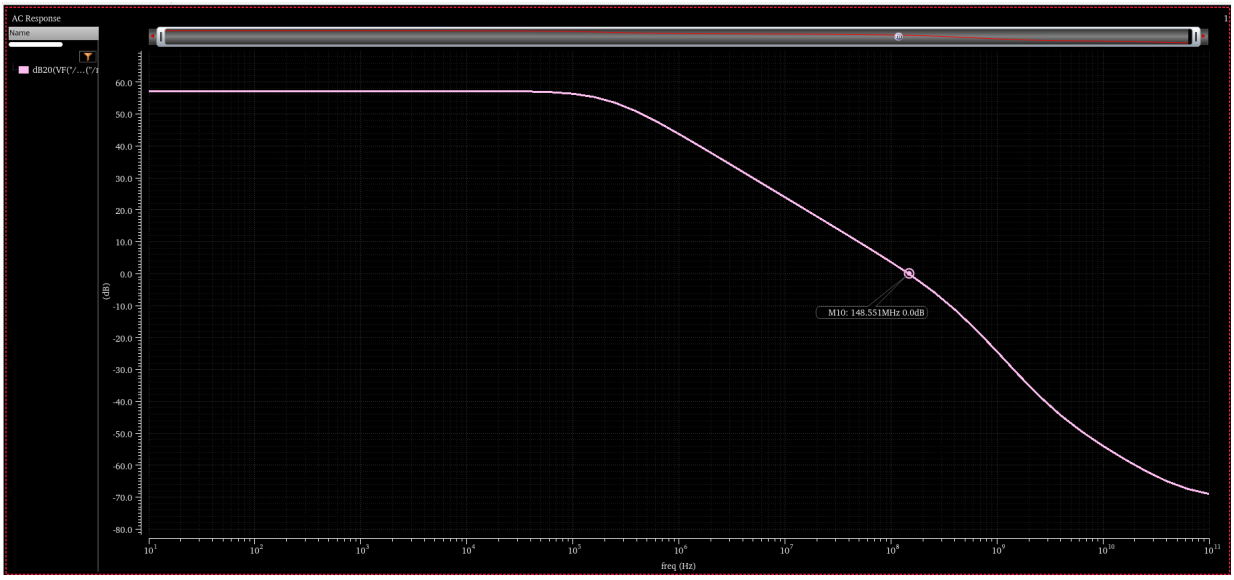

| Input Common Mode Voltage | Gain | 3dB Bandwidth |
|---|---|---|
| 850mV | 59.6685 dB | 161.481 kHz |
| 1.4V | 57.1917 dB | 217.356 kHz |

### 7.3.2 Unity Gain Frequency

**At input common mode voltage of 850mV**



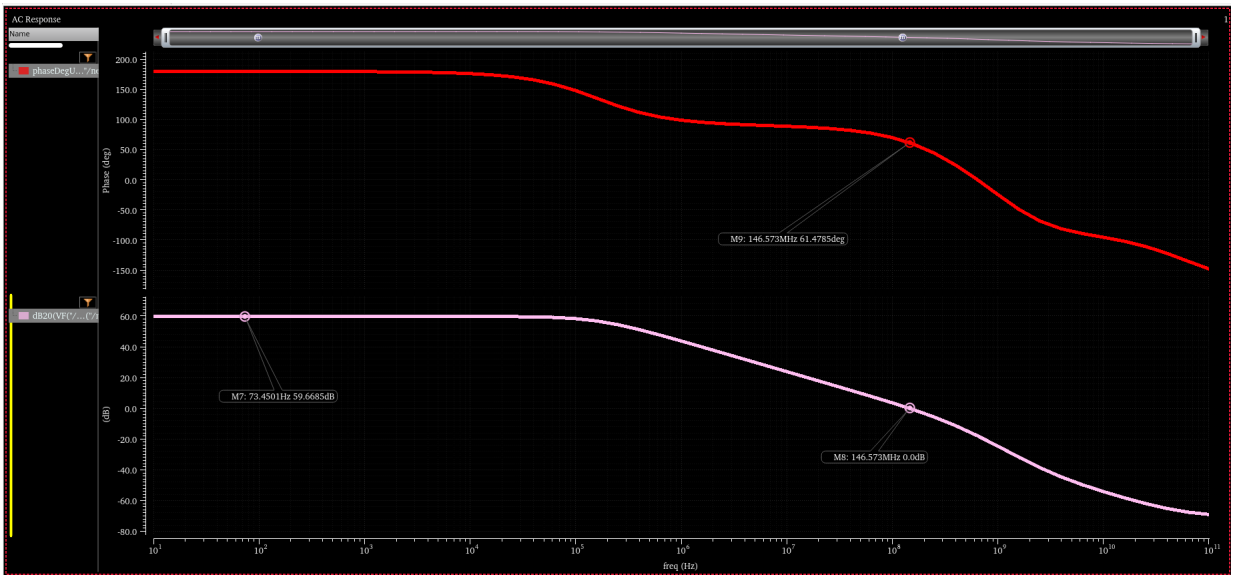

**At input common mode voltage of 1.4V**



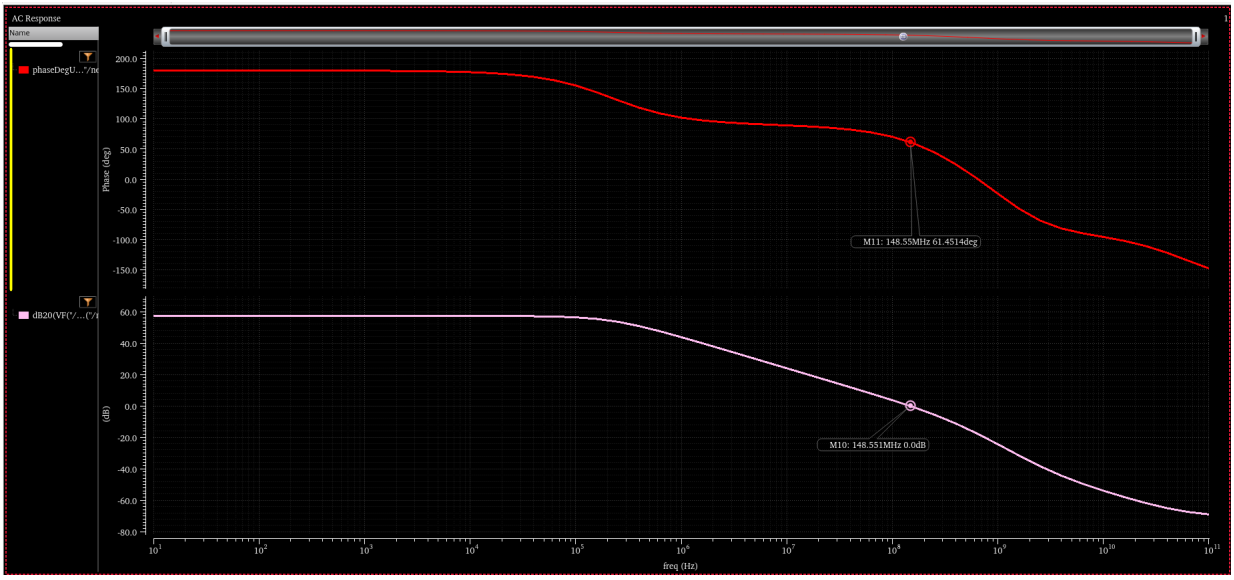

| Input Common Mode Voltage | Unity Gain Frequency |
|---|---|
| 850mV | 146.573 MHz |
| 1.4V | 148.551MHz |

### 7.3.3 Phase Margin

**At input common mode voltage of 850mV**



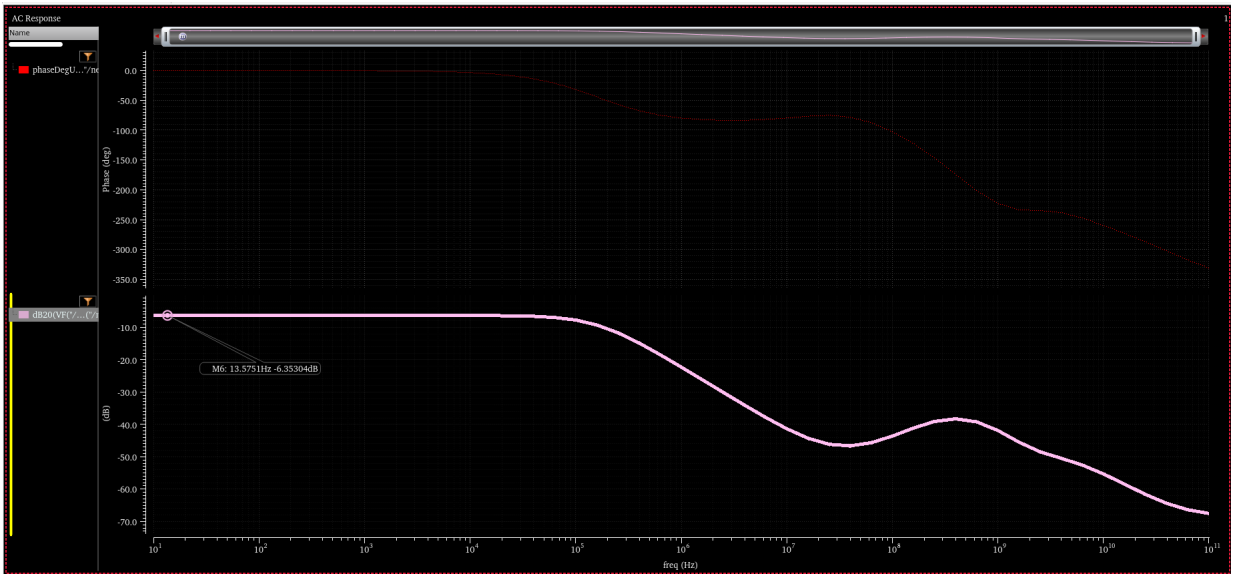

**At input common mode voltage of 1.4V**



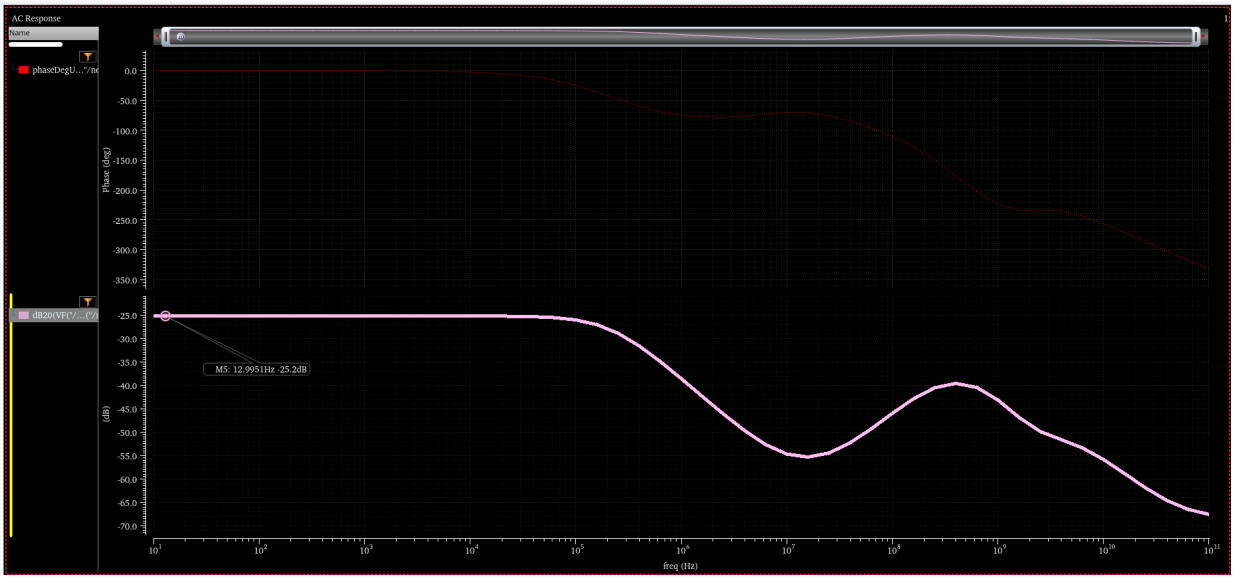

| Input Common Mode Voltage | Phase Margin |
|---|---|
| 850mV | 61.4785deg |
| 1.4V | 61.4514deg |

### 7.3.4 Common Mode Gain

**At input common mode voltage of 850mV**



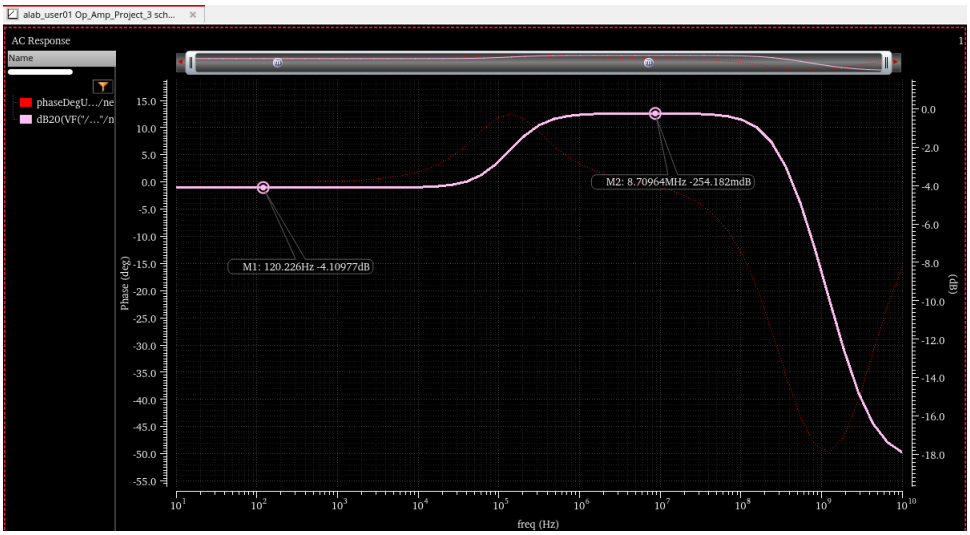

**At input common mode voltage of 1.4V**



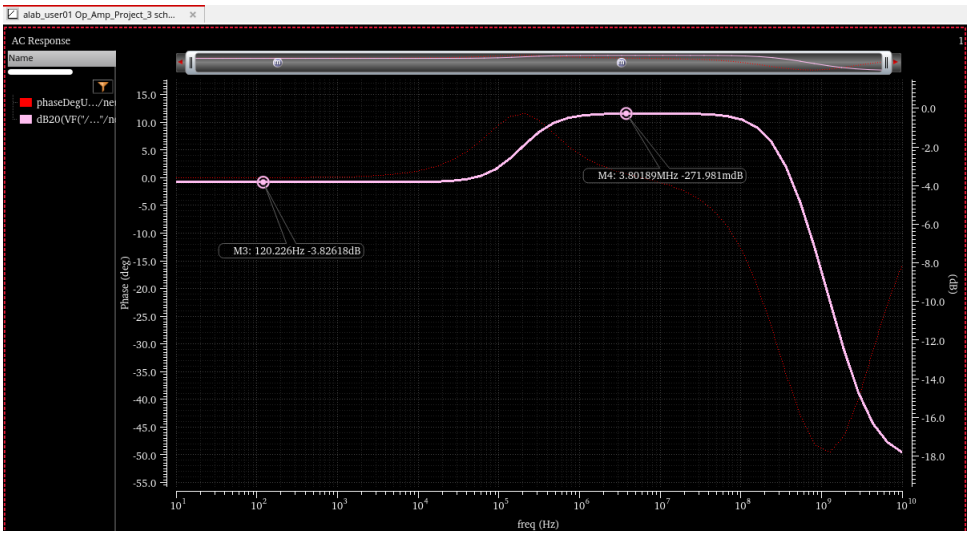

| Input Common Mode Voltage | CM Gain |
|---|---|
| 850mV | -6.353 dB |
| 1.4V | -25.2 dB |

### 7.3.5 PSRR

**At input common mode voltage of 850mV**




**At input common mode voltage of 1.4V**




| Input Common Mode Voltage | PSRR |
|---|---|
| 850mV | -4.10977 dB |
| 1.4V | -3.82618 dB |

## 7.4 Transient Analysis

### 7.4.1 Slew rate

## Uncompensated Opamp

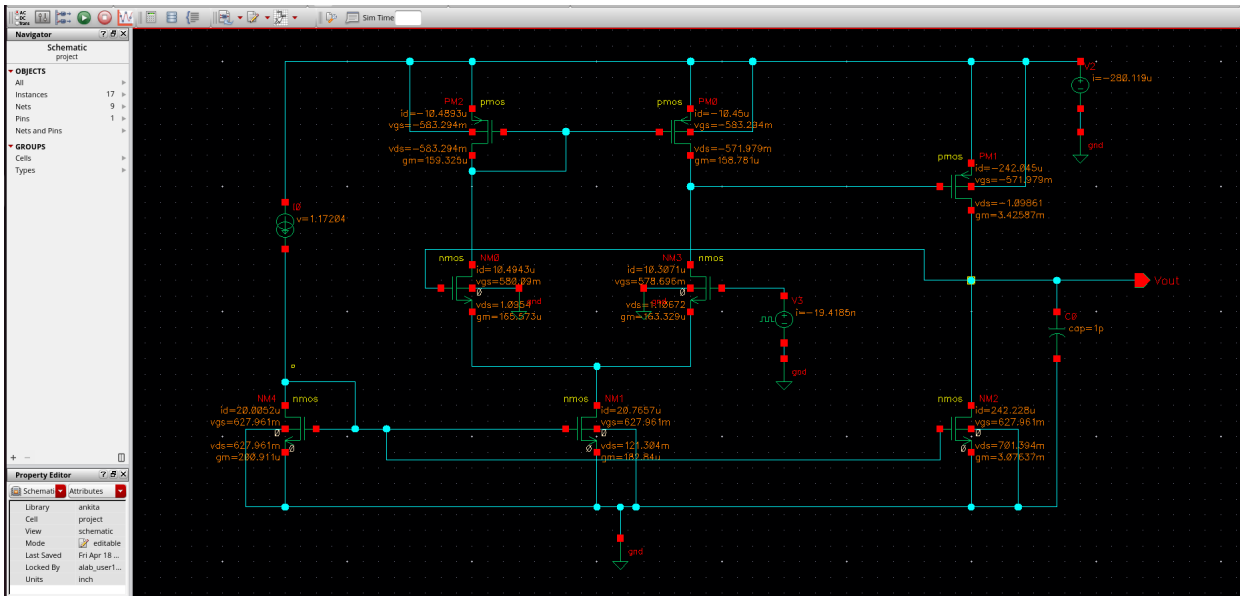



Figure 25: Schematic for transient analysis for uncompensated opamp

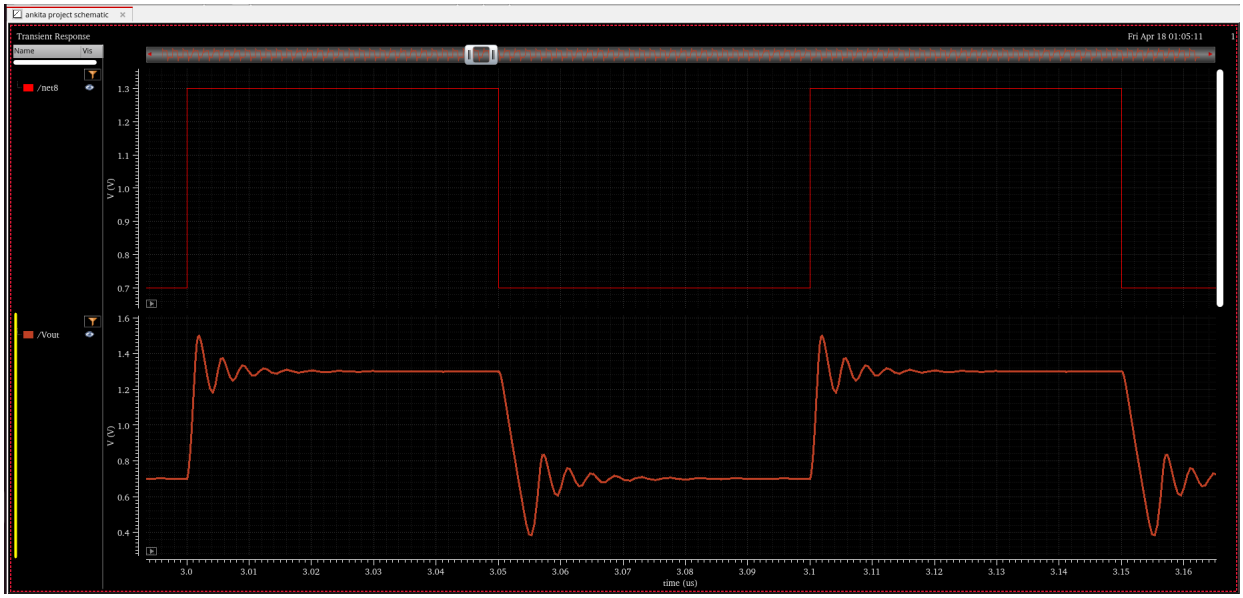



Figure 26: Transient simulation output of uncompensated op-amp

# Compensated Opamp

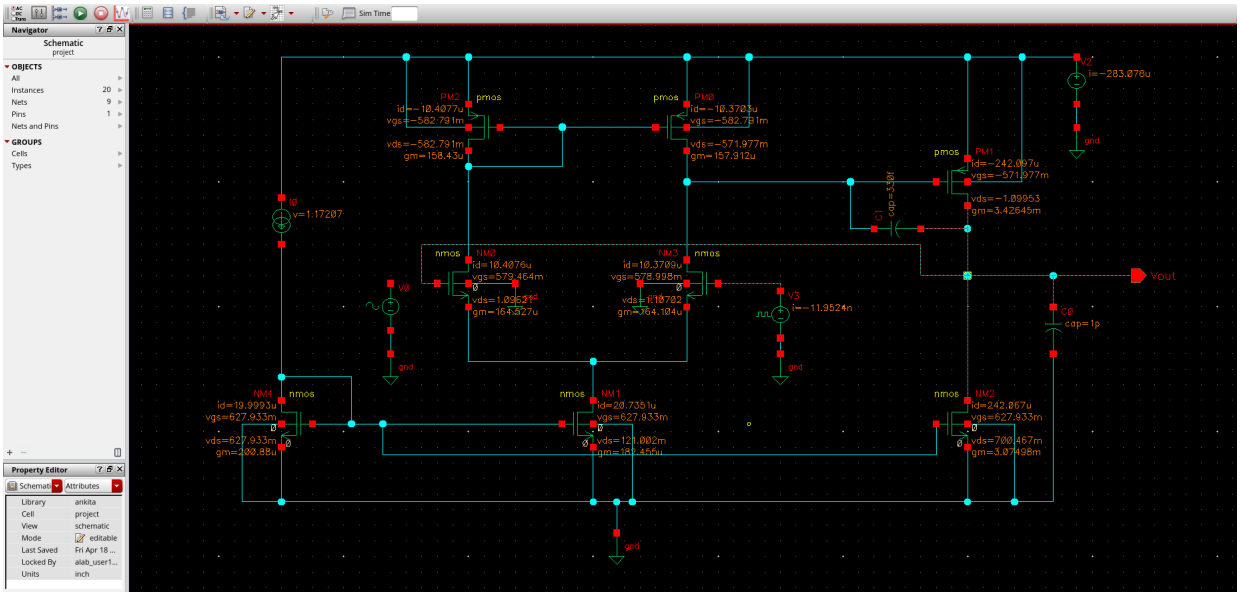



Figure 27: Schematic for transient analysis for compensated opamp

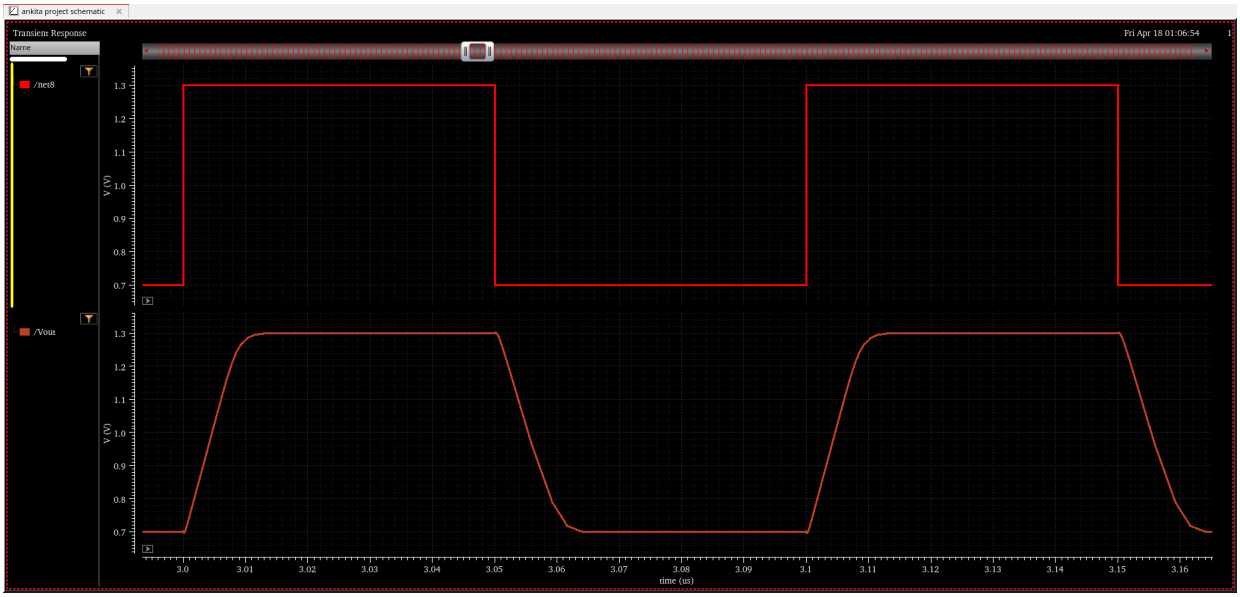



Figure 28: Transient simulation output of compensated op-amp

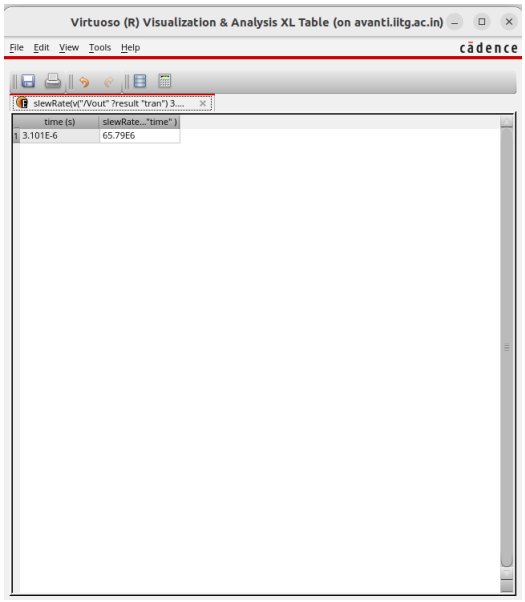



Figure 29: Slew Rate for rising edge

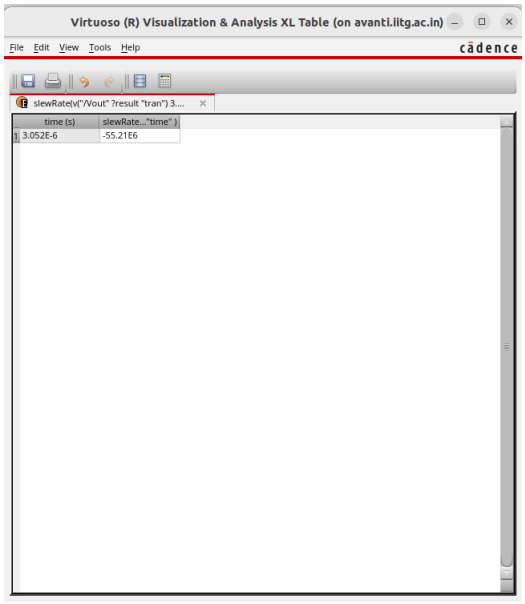



Figure 30: Slew Rate for falling edge

| | Slew Rate (V/$\mu$s) |
|---|---|
| Rising edge | 65.79 |
| Falling edge | 55.21 |
| Total | 60.5 |

# 8 Conclusion:

1. The amplifier achieved a slew rate of 60.5V/$\mu$s, which is higher than the required 1V/$\mu$s, indicating good dynamic performance.
2. The output swing was observed to be 156.582mV – 1.6343V at 850mV and 187.788mV – 1.6415V at 1.4V common mode voltage.
3. A phase margin of approximately 61.45° was observed, satisfying the stability criterion of $\geq$60°.
4. Input Common Mode Range (ICMR): Achieved 851mV – 1.702V.
5. Gain: Achieved 57–59dB, well above the minimum requirement of 40dB.
6. Gain Bandwidth Product (GBW): Achieved 161.481MHz at 850mV and 217.356MHz at 1.4V, exceeding the target of $\geq$70MHz.
7. The unity gain frequency was recorded as 146.573MHz at 850mV and 148.551MHz at 1.4V.
8. Common Mode Gain: The common mode gain was found to be -6.353dB at 850mV and -25.2dB at 1.4V, reflecting effective common-mode signal rejection.
9. Power Supply Rejection Ratio (PSRR) values were -4.11dB at 850mV and -3.83dB at 1.4V.
10. Power Dissipation: Recorded at 581$\mu$W, well below the 1mW limit.