AVLSID Assignment

Tool: LT SPICE TSMC 180 nm CMOS Devices, VDD = 1.8V

Your Name and ID should be written as TEXT within the Schematic

Submit one zip folder containing all the .asc files

Place one additional word document in the folder which gives important takeaways from each of the simulation runs

Assignment-1 (10 Marks): Last Date for Submission is 01st March 2023.

1. Design Schematic and simulate a SR-Latch.
2. Design Schematic and simulate a D latch using transmission gates.
3. Design Schematic and simulate a Master-Slave FF.

Assignment-2 (10 Marks): Last Date for Submission is 30th April 2023

4. Design a CMOS Schmitt trigger circuit with hysteresis width 500 mV approximately and simulate.
5. Design a CMOS Level Shifter which can shift level VDDL of 0.5 V to VDDH = 1V