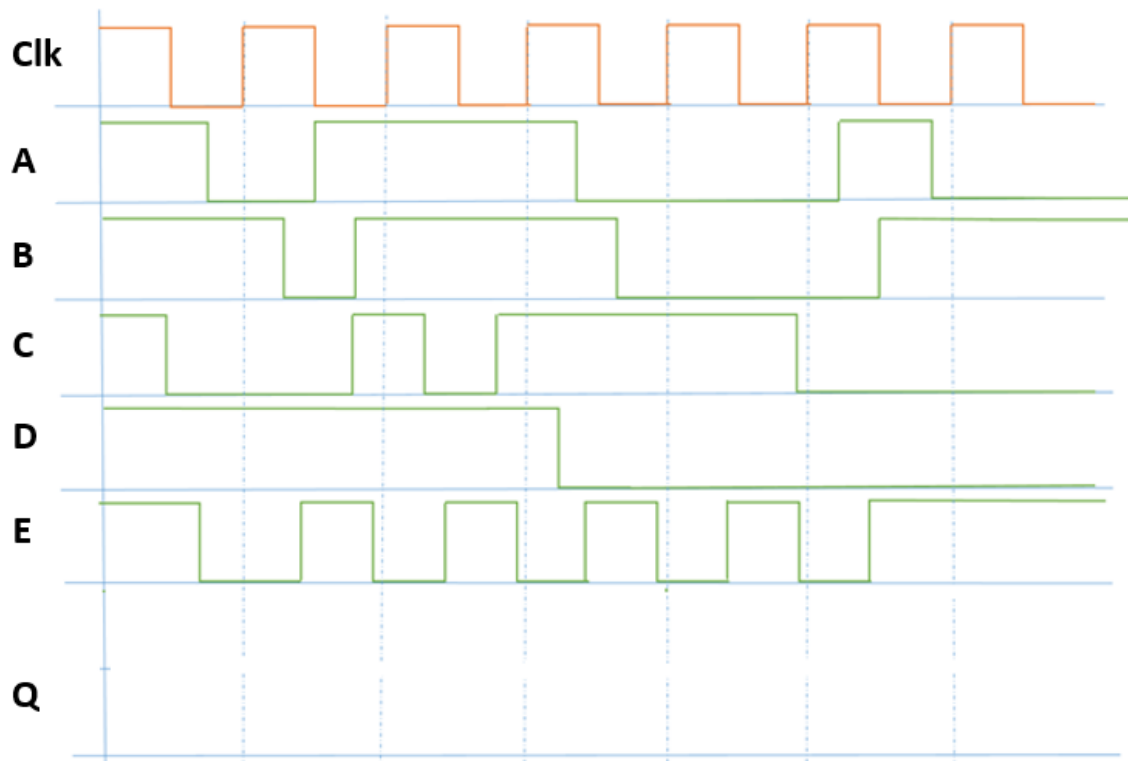
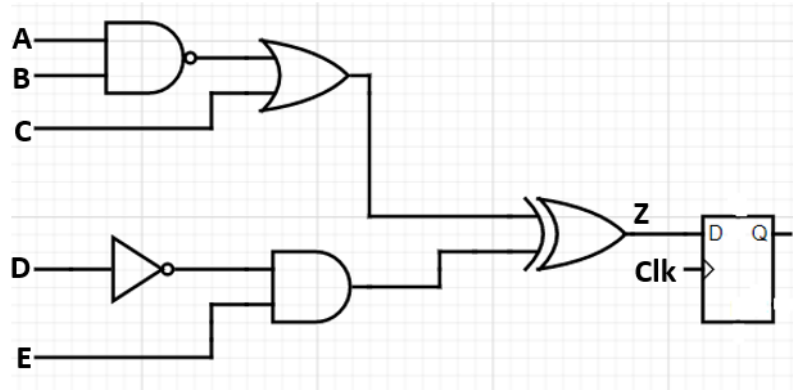


1. Refer to the circuit below. Complete the timing diagram assuming the starting state of the flip-flop output Q is 1. Complete the truth table by taking the inputs from the timing diagram. (10)



[illegible]