Birla Institute of Technology & Science, Pilani
Work Integrated Learning Programmes Division
First Semester 2022-2023

Comprehensive Examination
(EC-3 Regular)

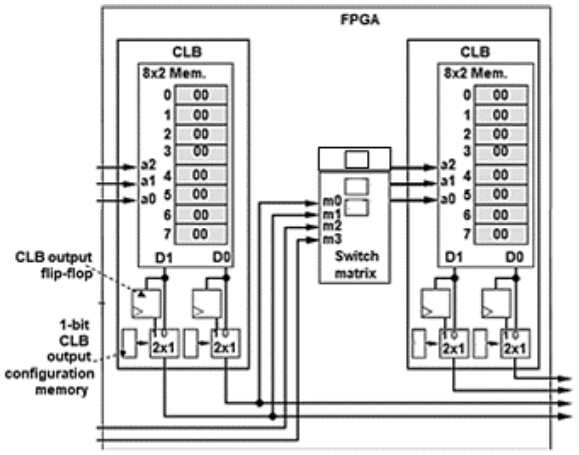
Course No.	: ES ZG554 / MEL ZG554
Course Title	: Reconfigurable Computing
Nature of Exam	: Open Book
Weightage	: 45%
Duration	: 2 Hours
Date of Exam	:

No. of Pages = 2
No. of Questions = 5

Note to Students:

1. Please follow all the *Instructions to Candidates* given on the cover page of the answer book.
2. All parts of a question should be answered consecutively. Each answer should start from a fresh page.
3. Assumptions made if any, should be stated clearly at the beginning of your answer.

Q1. Implement a 3-bit incrementer using the FPGA CLB block shown below. The 3-bit incrementer will have A2A1A0 (A) as input and S2S1S0 (S) as output. Clearly mention all the signal names and 8x2 memory contents of the CLB shown below. (The output S is equal to input i.e. A plus 1 i.e. if A=000 i.e. A2=0, A1=0 and A0=0, then output S = 001 i.e. S2=0, S1=0, S0=1, similarly when A=001, S=010;… A=111, S=000) **[6]**



Q2 Consider a technology-dependent library that contains the following cells: (NAND2 with cost 2, NAND3 with cost 3, NAND4 with cost 4, AOI21 with cost 5, AOI22 with cost 6 and INV with cost 1. [5+5+3+4]

a. For the Boolean function, **F = [AB + (A+C) D] E**, draw the subject graph using the base functions (2 input NAND and inverter). Find a minimum cost cover of the subject graph so as to minimize the area.

b. Using Chortle algorithm, find the minimum mapping function to cover the Boolean network of part (a). Assume K is equal to 3. (Assume fan-in and fan-out of each node in DAG is 2 and 1 respectively.) Show all the steps of the algorithm.

c. Using the Chortle-crf algorithm, find the minimum number of 3-LUTs needed to cover the Boolean function of part (a).

d. For the same function in part (a), assume logical AND and OR operators are replaced by multiplication and addition operators. The delay of multiplier unit is 3 clock cycles and that of adder unit is 1 clock cycle. Using ASAP algorithm, find the minimum bound on the latency. Using this latency, schedule the tasks using ALAP algorithm. Find mobility of each node?

Q3. (a) Xilinx XC4000 contains three function generators, F, G and H. F and G are 4-input function generators and H-is a three input function generator. Give an example of a 9-input function that cannot be implemented using XC4000 device. Justify. Can you generalize using your answer the class of functions that cannot be implemented using XC4000. **[5]**

(b) Computations are implemented either in hardware or software. Give examples of some devices for each domain. What are the important characteristics of both these domains that help the designer choose between the two? Where does FPGA fit in? What do you understand by the terms: Spatial and Temporal Computing? Say, you need to implement the following function using spatial and temporal computing. Show the implementation for both.

$$F = 0.50 * X + 0.25 * Y + 0.25 * Z \quad [6]$$

Q4. The Programmable Array Logic is sued to implement the following Boolean functions:

W = ABC' + A'B'CD'
X = A + BCD
Y = A'B + CD + B"D'
Z = ABC' + AC'D' + A'B'C'D + A'B'CD'

The OR gate in each section of the PAL can take a maximum of three product terms. If one section of the PAL takes 5 ns, compute the worst-case delay required to compute all four functions. [5]

Q5. Algebraic division helps simplify Boolean functions if we follow polynomial rules of real numbers and apply them to Boolean network.

a. How is Boolean division different from Algebraic Division? Give a list of lemmas of Boolean functions that do not apply to Algebraic Division. [2]
b. Divide the given function with the divisor, **D = a + b** and express the function as F = Q.D+R
F = ab + ac+ ad' + bc + bd' **[4]**

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