Birla Institute of Technology & Science, Pilani
Work-Integrated Learning Programmes Division
Second Semester 2022-2023

Mid-Semester Test
(EC-2 Regular)

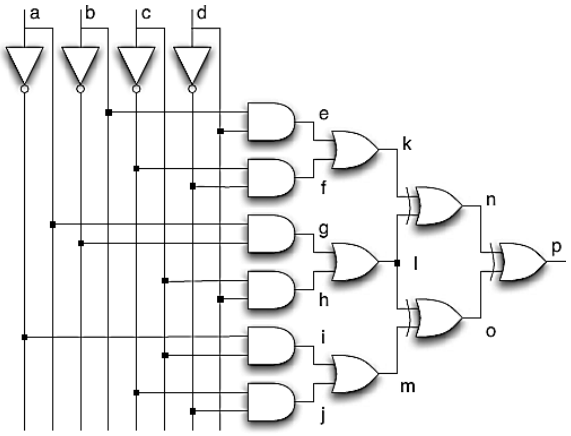
Course No.	: AEL ZG 554 /ES ZG554 / MEL ZG554
Course Title	: RECONFIGURABLE COMPUTING
Nature of Exam	: Closed Book
Weightage	: 30%
Duration	: 2 Hours
Date of Exam	:

No. of Pages = 2
No. of Questions = 5

Note:

1. Please follow all the *Instructions to Candidates* given on the cover page of the answer book.
2. All parts of a question should be answered consecutively. Each answer should start from a fresh page.
3. Assumptions made if any, should be stated clearly at the beginning of youranswer.

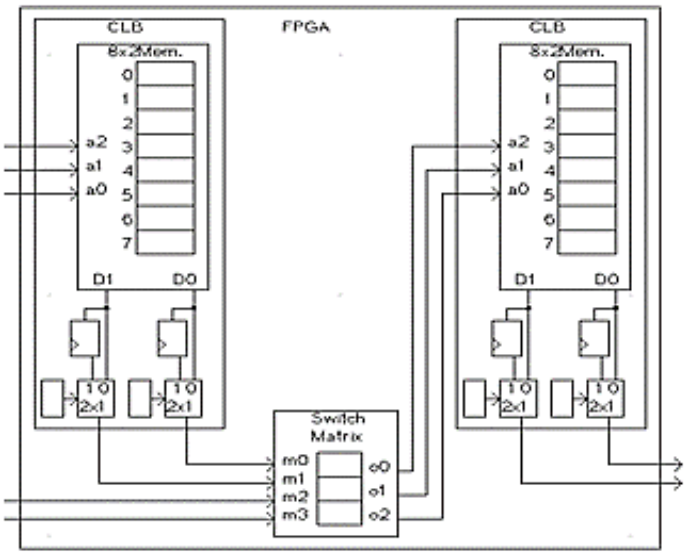
Q1. Small sized LUTs can implement big-sized functions. Using only 3-input, 1-output lookup tables (LUTs), implement the circuit using minimum number of LUTs. Do not simplify the gate-level circuit before mapping it to LUTs. How many LUTs are required to implement the design? Using the truth table approach, show the inputs and output of each LUT. If any input is not used, mark it as "X". **[6]**



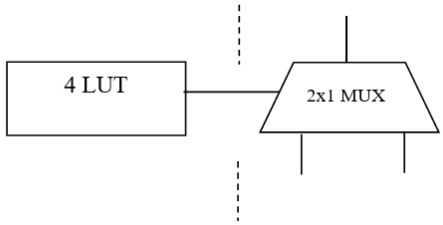
Q2. a. Implement 8-input Boolean function,

Z = A'B'C'D + AG'H + AG + A'B'CE + A'BF' using minimum number of 3-LUTs. **[4]**

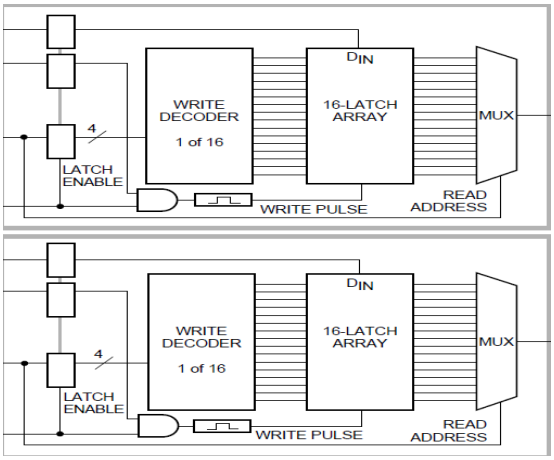
b. Generate the configuration bit- stream needed to program the two CLBs shown in fig for the functions F = AB+ B'C + AC + D and G = A' implemented on them. The LUTs are initialized with value '0'. **[4]**



Q3. A designer wants to implement a 5-bit comparator using the carry logic of XC4000. A simplified block of a CLB is shown in the figure, using one or more such blocks, show how a 6 bit comparator can be built. Also show the circit diagram of the logic implemented by the LUTs. **[6]**



Q4. Using the simplified block diagram of the XC4000 CLB configured as 16x1 memory, show it can be used to build a 8x1 dual-port RAM. Show all signals explicitly needed for the CLB to act as dual-port distributed memory. **[4]**



Q5. Answer in brief:

a. Over the years, FPGA vendors have been increasing the size of the LUTs on their devices, for example, 3-LUTs have now been replaced by 6-LUTs in Virtex devices. Mention two advantages of choosing larger LUTs. Is it always true? List two good reasons to have smaller sized LUTs. **[2]**

b. FPGAs allow programming any kind of function as far as this can fit onto the device. This is possible because of the low granularity of the function generators available. However, the cross point programmable interconnections act as a bottleneck to the performance of FPGAs. Why? Suggest a way to improve this drawback. **[2]**

c. Which of the two Anti-fuse technologies is used to make interconnections with minimum resistance. Why? List two advantages over SRAM technology. **[2]**

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