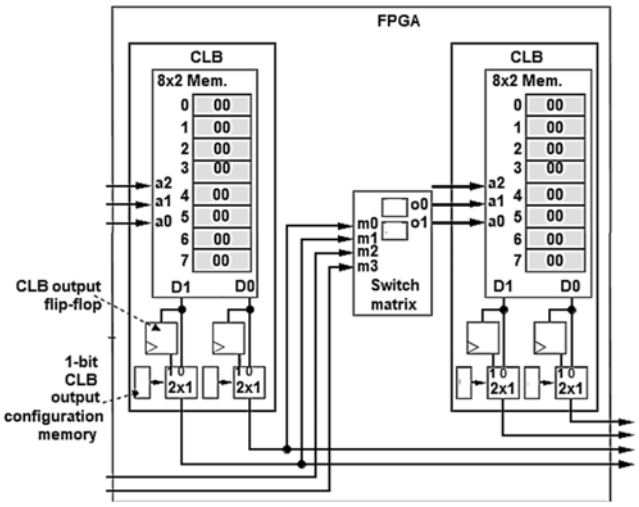
Birla Institute of Technology and Science, Pilani
Work Integrated Learning Programmes Division
First Semester 2022-2023
Mid-Smester Test
(EC2 Regular)

Course No. : ES ZG554
Course Title : RECONFIGURABLE COMPUTING
Nature of Exam :
Weightage : 30%
Duration :
Date of Exam :

No. of Pages = 2
No. of Questions = 5

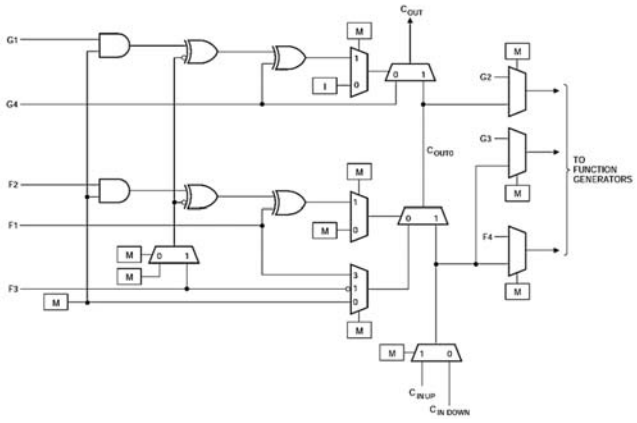
Q1. You need to design a network collision detector using FPGA. If two or more computers connected on the network start sending messages simultaneously, it's a collision and the message must be sent again. The network consists of four inputs A, B, C and D. that are 1 when the corresponding computer is sending a message and 0 otherwise. The circuit has a single output labeled U that is 1 when a collision is detected and the message requires re-sending and 0 otherwise. Implement the design using the FPGA block shown below. [6]



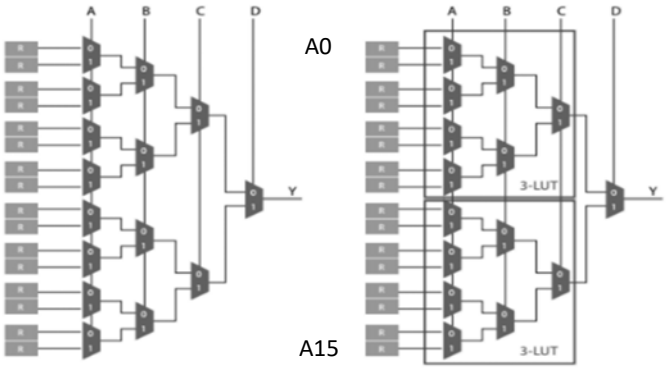
Q2. Consider an FPGA has a number of 4-input and 1-output LUTs and 2x1 MUXs. A designer wants to implement a seven input arbitrary function. Compute the minimum number of LUTs and MUXs required. If MUXs are also implemented using LUTs, re-compute the number of LUTs. Generalize an expression that presents the number, 'n' of 4-LUTs required to implement an arbitrary 'a' input function. [6]

Q3. The figure shows the detailed architecture of carry logic of XC4000 FPGA. The carry logic can perform a variety of arithmetic functions. Show the configuration bit (memory) values and required architecture (which blocks of this architecture) can be used to perform the operations of:

a. Subtractor
b. Down Counter [6]



Q4. A 4-LUT is implemented using 3-LUTs and a set of 2x1 MUXs as shown in figure. If a bit file comprising of bit pattern 0xFFFE (A_{15} to A_0 addresses in hex) is transferred, what logic function is implemented by the circuit at Y output. A single event upset (SEU) error caused to flip A0 and A15 bits. How does it affect the output? [6]



Q5. Justify pros and cons of using large sized LUTs inside FPGAs. For example, to implement a 9 input function, would you prefer to have a 9-input LUT or go with multiple 3 input LUTs. [3]

Q6. Justify using an example where the choice of using an FPGA for a system may go wrong against choice of an ASIC. [3]

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