**Q1.** Implement a 3-bit incrementer using the FPGA CLB block shown below. The 3-bit incrementer will have A2A1A0 (A) as input and S2S1S0 (S) as output. Clearly mention all the signal names and 8x2 memory contents of the CLB shown below. (The output S is equal to input i.e. A plus 1 i.e. if A=000 i.e. A2=0, A1=0 and A0=0, then output S = 001 i.e. S2=0, S1=0, S0=1, similarly when A=001, S=010;… A=111, S=000) **[6]**