Q1. You need to design a network collision detector using FPGA. If two or more computers connected on the network start sending messages simultaneously, it's a collision and the message must be sent again. The network consists of four inputs A, B, C and D. that are 1 when the corresponding computer is sending a message and 0 otherwise. The circuit has a single output labeled U that is 1 when a collision is detected and the message requires re-sending and 0 otherwise. Implement the design using the FPGA block shown below. [6]