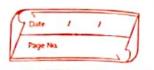


	Page No.
	Question -
1.0.	and the second of the second o
- 4	Assignment -2
2.00	the state of the s
8	Virtual Memory for Windows
	- 1
×	Windows uses demand paging with clustering meaning they page in multiple pages whenever a page fault occurs.
	they page in multiple pages whenever a page fault prouve
1	The second sections of the second sections of the second sections.
*	The morking let minimum and maximum are normally set at 50 and 345 pages respectively.
	50 and 345 pages respectively.
	The Control of the Co
*	Free pages are maintained on a free list, with a minimum threshold indicating when there are enough free frames anaitable.
	threshold indicating when there are enough free frames
	available.
炔	It a page fault occurs and the process is below their maximum, then additional pages are allocated. Otherwise some
	maginum, then additional pages are allocated. Otherwise some
	projes from this process must be replaced using a local
	page replacement algorithm.
la a s	The transfer of the transfer of
灾	If the amount of free frances fells below the available
	Herneshold then marking set training secure taking frames
	away from any processes which are above their minumum
	with all are at their minimums. Then additional frames
	ean be allocated to process that need their.
-	and the second of the second o
14.	Virtual Memony for Solanis
*	
Late	one to faulting thread whenever a fault occurs It is
	therefore imperative that a minimum amount of free memony be
	kept en hand at all times.
	vijeta



	- Miles
	* Solari's also maintains a cuche of pages that have been
-	reclaimed but which have not yet been onerwriten, as
	opposed to the free list which only holds pages whose
-	current contents are invalid. Ty one of the pages
	from the eache is needed before it gets moved to the
1	free list, then it can be quickly necessaried.
24. 72.0.0	
, ,	If free memony falls wellow mainfree, then pages
,——	rules with every page fault.
,	
, 4	e Recent releases of Jolan's have enhanced the virtual
	memony management system including recognizing
1	pages from shared libraries and protecting
	their from burg paged out.
82.	A rough Admen does not when he
	accual existing address, mover, it defens to an
	abstract address in an abstract address space
	contrast this with a physical address that refers
	to an actual physical address in neurony: A hogical
	address is generated by CPU and is translated
to Market	into a physical address by the MMU.
- 14 D	The state of the s
0.7	* Y AU T L Y C 12 (V .)
88.3	Paging is implemented by breaking up an
	address into a page and affect number. It is
	most efficient to break the address into X page
	I tillet but nather them bentomy and with
14 40	the address to calculate the page number and
	Start a to the sale
)	vijeta



	offset Because each but position represents a power of 2,
	offset. Because each bit position reparesents a power of 2, splitting an address between bits nesults in a page till
1.5	that is a power of 2.
	The state of the s
98.4	a) Logical address : 16 bits
	b) Physical address: 16 bits
patina	Landieran (storer Fig 1913 & red well to
8.5	By allowing two entries in a page table to point to the
200	same page frame in memory, users can share code and
	data. If the code is reentrant, much memory. Space can
	be seved through the should use of large programs
	such as tent éditors, compilère and database systems
	copying large amounts of memory center be effected by
	having different page tables point to the same memory
2-2	beaton. Level 1 121 121 121 121
	Carley 1200 Brief
8.10	y In a rouneutional single-kenel page table
	10000 2 -2" < 4000 K112" ship a will die
5.	what were the control is the control of the
TRAL	So we need 12 out of 32-bit logical address for
	the offset. Then me have 32-12=20 bits left for
	the page number.
10	and the state of t
⇒	220 = 1048576 entries
	in the it is a man and the second of the second
1	the expression of the same of
	vijeta

	Page Na.
-	
	An innerted page sable
	Size of physical address space = No. of frames & frame tize
	Dhere page size = frame size
	No. of frames = $2^{2a}/2^{12} = 2^{17}$
3)	Number of entries = 217 = 131072/1024 = 128 K entries
२ १. 15	The configuous memory allocation scheme suffer from external fragmentation and does not allow processes to shore code.
	processes to share code
100	Pure eignentation also siffers from external. fragmentation and enables process share use.
	rure paging suffers from internal pragmentation and anables processes.
	- 12 2 y 12.6. d - with a Tarded
1 88.19 C	In a dystem with paging a process cannot seems memony that it does not own breams
า	un address on a paging system is a logical page
1 00	ased on the logical page number to produce a
r CC	injerical page number. The OS controls the process
- 0	secessing only twose physical pages allocated the process.
U	rijeta

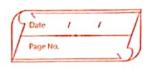


- 31	There is no may for a process to refer to a page it does not
	own breause the page will not be in the page table.
	the second parameter and the second s
12.	we have an breaking a marketing of the
88.19	when the TLB attempts to resolve virtual page numbers, it
oju.	ensures that the Address space plentifies (Mess.) for the
	anymouther acres through the party material than the Asia and and
	currently running process matches the ASID astociated
	with the wirtual page. If the Acros do not match, the
	attempt is treated as a TLB miss.
	So ASIDS are used to promole address space protection
	in the TIB as well as supporting TIB entires for several
	different processes at the same time.
	u ji
	1 01 2
29.1	A page fault occurs when an access to a page that was not
	been brought into main newsry takes place. The or newfiles
	The memony areas, aborting the programe if it is invalid. If it is negrested
	to read the needed page into free frame. Upon complition
	of I/o the process table and page table are updated and
	the instruction is restanted.
89 2	a) lower bound on the number of page faults = n
yies	() () () () () () () () () ()
1.3	la > ultras haved as the angles of freeze landle =
7.1	b) upper bound on the number of peage faults = p
OO F	To all and a dollar of tool are and the areas are to The benefit
Q7. 3	The costs are adoltional hardmane and slower access time. The benefit
	are good utilization of neurony and larger logical address space attour
	physical address space.

1	_		
Date	,	,	
Page No			7
			$\sim \nu$

09.1	C
89.6	For every memory access operation, the page table needs to
}	be consulted to check whether the corresponding page is
	resident or not and sobether the program has need
	or write proveleges for accuracy me perge these chicks
	would have to be penformed in handware, A TLB
- VI.	could could serve as a cache and improve
×	penformence of the lookup operation.
- L	I - for a and sal to long for the white thing
	attended to be a supplied to the supplied of
89-8	No. of frames LRU FIFO Optimal
148	2000 2000 2000
Sa. 8020.	12 12 18 15
	3 15 16 11
	4 10 14 8
	5 8 10 7
Hay ou	But by an passe To eader Adver the Trees do 1. 12
المكاولكم	3 22 Those water of Thom signs I so, with the road
188 6 20	we come are a pharty in the pre- and the 11 th .
Kan an	of had been a make a little
29.9	LRU = 18 wh the long beloven we have the
1 1	FLF0 = 17
	Optimal = 13 Norganitude wir weith with the
29.10	You can use the valid invalid bit supported in handward
•	to similate the reference but. Initially let the but to invalid.
	On hirst relevance a track to un account to unvaller.
	On first reference a trap to the Os is generated the Os
العليا	will let a software bit to I and reset the nation invalid bit to valid.
and de la	· Le La TE La ige will. I be wromen to another hospe to
	. I had sorkha he sould

vijeta



Q9.11	NO. An oppinal alamile III est enview hour Reladita
	NO. An ophinal algorithm will not elyfer from Belady's
	anounally becomes - by definition an optimal algorithm replaces
	the page that will not be used for the longest time, relady's
	anomaly occurs when a page replacement algorithm emichs
	a pege that will be needed in the Immediate future. An optimal
	algorithm would not have selected such a page.
Jan.	it is not not also soon to be town it will all the
89.12	a) Threshing is occurring
	b) CPU utilization is sufficiently high to leave takinge
	alone, and increase degree of multiprogramming.
	c) Increase the degree of multiprogramming.
09.14	The page table can be set up to similarle base and littuet registers
7	Drowded that the walled in allocated in the of a second
1 1 No	provided that the memory is allocated in thread size signients
1	In this may, the base of definent can be entered winto a
	page table and the nalvel/invalid bit used to indicate that
	position of the signest as resident in the neurony, There mil
	be some problem with internal fragmentation.
09.5	
99.17	a) ear occur to the world a wing of page
<u></u>	b) can occur
	c) can occur
04	d) conit occur
6-	Line principle of president of and employed bus
Ad.	he fall of the distribution of the matter of the
29.20	Given ? virtual memory = 232 bytes
	physical memony = 222 bytes
	programmes of the second of th

Dute	,	,	
Page No.			

ļ	
	page size = 2 ² bytes Given physical address = 11123456
Yar 1	Size of page table = Virtual memory = 232 = 220. page size 212
=>	20 bits are used for page table entry and its frame number rehereas tast 12 bits are used from displacement into page. 00010001000100 100011 010001010
	page table size page size
1807216-1	Software and Handmane Handmare part of the system handless dynamic address translation; whereas software openations take care of faulty pages, reading the resulting page and repeating the process whenever required.
ह्याव. प्	A cyclem ean perform only at the speed of it dowest bottleneck. Dieks or disk toutrollers are freghently the bottleneck in modern systems as their individual performance teament keep up with that of the CPU and eyetem bus. By balaneing I/o among disks and controllers writher an individual disk nor a controller is overwhelmed. So that bottleneck is avoided.



	DMA increases system concurrency by allowing the CPU to perform tasks while the DMA controller to be a bus masters data up a the system and memory buses. Hardmane design is complicated because the DMA must be integrated into the system and the system must allow the DMA controller to be a bus master. Cycle stealing may also be necessary to allow the CPU
	and DMA controller to share use of the memory bus.
શ્. 1	The STREAMS driver controls a physical denice that could be impossed in a STREAMS operation. The STREAMS module modifies the flow of clocks between the head (the user swenface) and the driver.
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