Spring 2015 Week 6 Module 29

Digital Circuits and Systems

State Machines 1

*Shankar Balachandran**
Associate Professor, CSE Department
Indian Institute of Technology Madras

*Currently a Visiting Professor at IIT Bombay

JK Flipflop

CLK	J	K	Q*
↓	0	0	Q
↓	0	1	0
↓	1	0	1
↓	1	1	Q

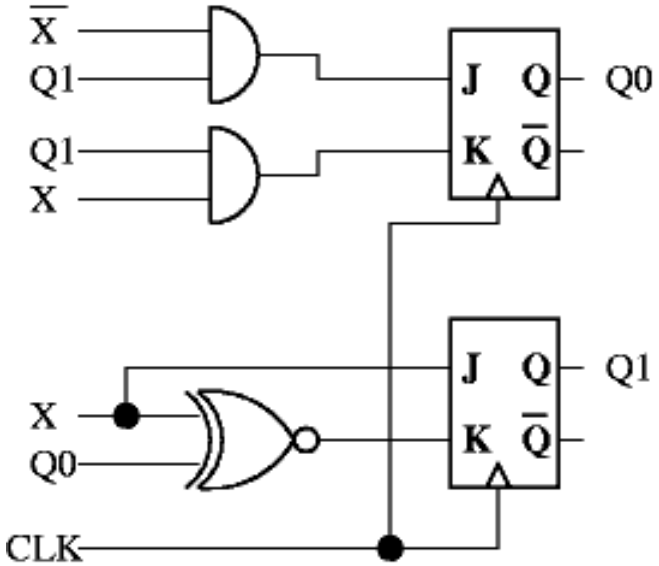
J: Set

K: Reset

J=K=0: Keep old value

J=K=1: toggle

Example:



1. **Input/Output logic equations**:

$$J_0 = Q_1\overline{X}; \quad K_0 = Q_1 X;$$

$$J_1 = X; \quad K_1 = \overline{X \oplus Q_0} = XQ_0 + \overline{X}\,\overline{Q_0}$$

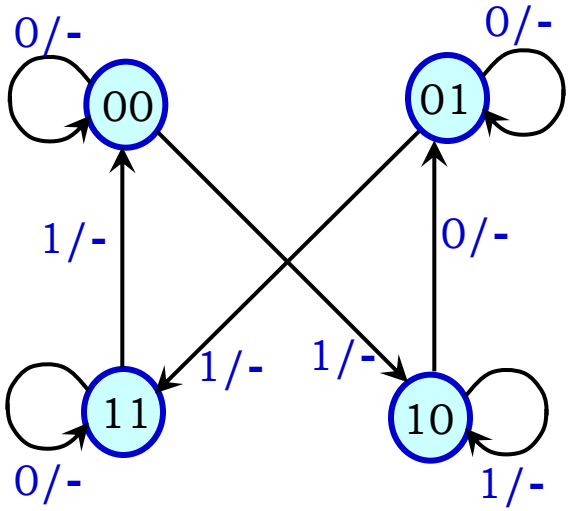
2. State table:

$$J_0 = Q_1\overline{X}; \quad K_0 = Q_1 X;$$

$$J_1 = X; \quad K_1 = \overline{X \oplus Q_0} = XQ_0 + \overline{X}\,\overline{Q_0}$$

Input X	Present State		Flip-flop Inputs				Next State		Out (*none*)
	Q_1	Q_0	J_1	K_1	J_0	K_0	Q_1*	Q_0*	
0	0	0	0	1	0	0			
0	0	1	0	0	0	0			
0	1	0	0	1	1	0			
0	1	1	0	0	1	0			
1	0	0	1	0	0	0			
1	0	1	1	1	0	0			
1	1	0	1	0	0	1			
1	1	1	1	1	0	1			

3. State Diagram:



Sequential Logic Synthesis

- Sequential network design is simply the inverse process of sequential network analysis:
  1. Construct a state diagram
  2. Choose a set of state variables and assign state-variable combinations to the named states in the state diagram.
  3. Construct the excitation table: For a given transition from a present state to its next state, this table indicates the inputs that must be applied to the flip-flops.
  4. Derive the boolean equations for flip-flop excitation and the explicit outputs.
  5. Draw a logic diagram to implement the above equations using logic gates and flip-flops.

Flip-flop Excitation Tables

- Excitation tables for D and T flip-flops:

Q	Q*	D
0	0	0
0	1	1
1	0	0
1	1	1

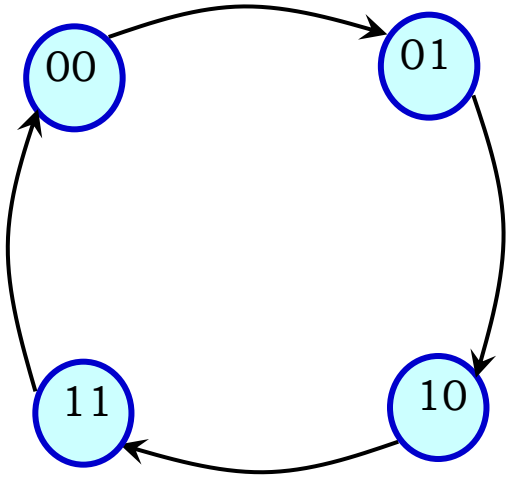
T
0
1
1
0

- Excitation table for JK flip-flop:

Q	Q*	J	K	J	K
0	0	0	0 or 1	0	X
0	1	1	0 or 1	1	X
1	0	0 or 1	1	X	1
1	1	0 or 1	0	X	0

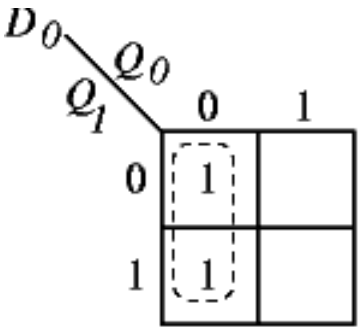
Example:

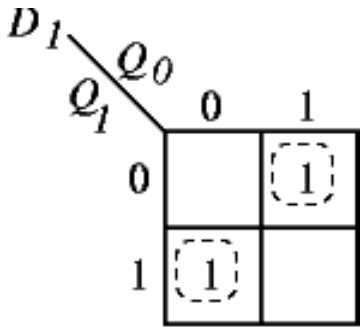
- Design a 2-bit binary counter using D flip-flops.
  - **State diagram**:



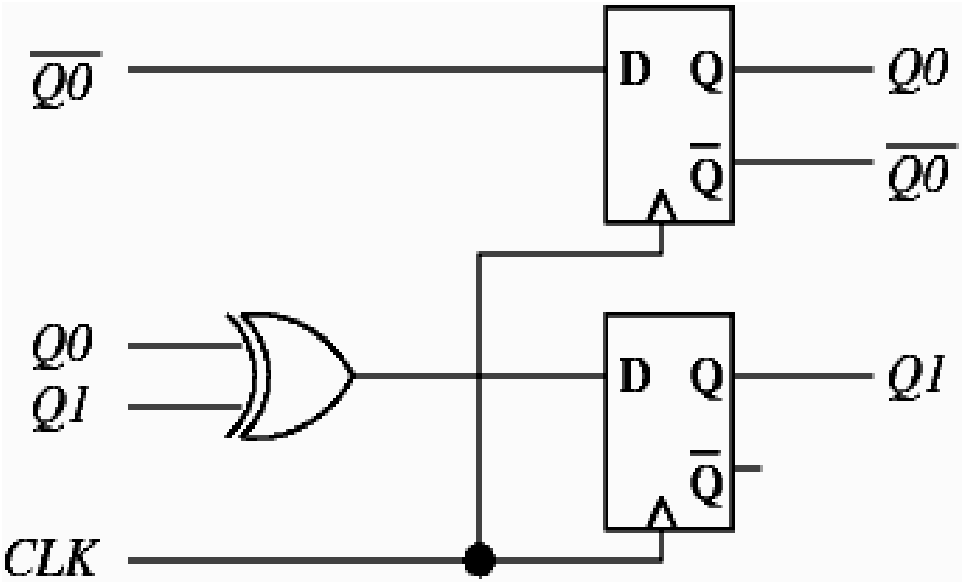
- **Excitation table:**

Input (*none*)	Present State		Next State		Flip-flop Inputs		Output (*none*)
	Q_1	Q_0	Q_1*	Q_0*	D_1	D_0	
	0	0	0	1	0	1	
	0	1	1	0	1	0	
	1	0	1	1	1	1	
	1	1	0	0	0	0	





- **Circuit implementation**:



End of Week 6: Module 29

Thank You