Assignment -2 (EC-262)

Due Date : 10/04/21

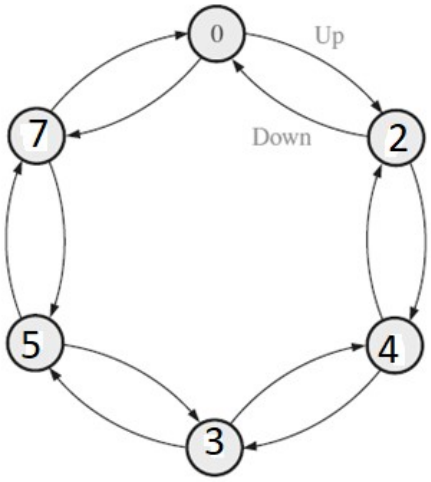
AY-2020-21

Question 1: For the 8-bit bidirectional register in Figure shown below, determine the state of the register after each clock pulse for the RIGHT/$\overline{LEFT}$ control waveform given. A HIGH on this input enables a shift to the right, and a LOW enables a shift to the left. Assume that the register is initially storing the decimal number seventy-six in binary, with the right-most position being the LSB. There is a LOW on the data-input line.

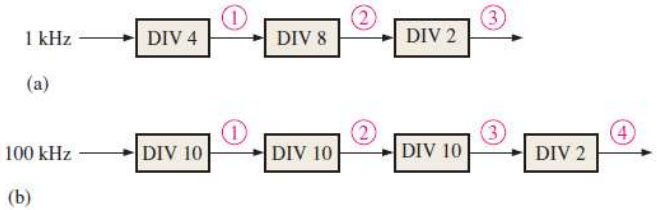
Question 2 : Design a counter to produce the following sequence 00, 10, 01, 11, 00, ……

a. Using J-K FF
b. Using D FF
c. Using JK FF for MSB bit and D FF for LSB.

Question 3: Design a binary counter with the sequence shown in the state diagram



Question 4 : For each of the cascaded counter configurations in Figure a & b, determine the frequency of the waveform at each point indicated by a circled number, and determine the overall modulus.



Question 5 : Determine f_{max} for the counter shown if t_{pd} for each FF is 50 ns and t_{pd} for each AND gate is 20ns.