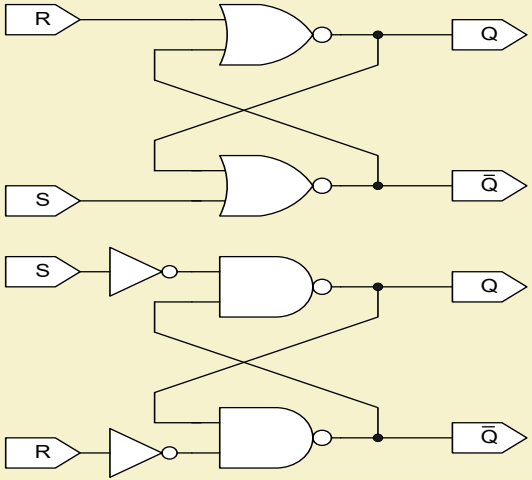
# The Set/Reset (SR) Latch

The Set/Reset latch is the most basic unit of sequential digital circuits. It has two inputs (S and R) and two outputs outputs Q and Q'. The two outputs must always be complementary, i.e if Q is 0 then Q' must be 1, and vice-versa. The S input sets the Q output to a logic 1. The R input resets the Q output to a logic 0.

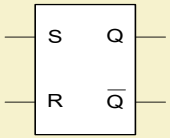
Circuit Diagram




Truth Table

| S | R | Q+ | Q´+ | Function |
|---|---|---|---|---|
| 0 | 0 | Q | Q´ | Latch |
| 0 | 1 | 0 | 1 | Reset |
| 1 | 0 | 1 | 0 | Set |
| 1 | 1 | 0 | 0 | Illegal |

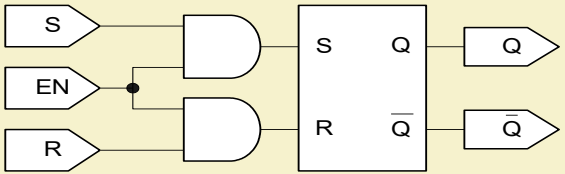
Logic Symbol



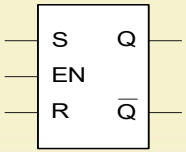
# The Gated Set/Reset (SR) Latch

To be able to control when the S and R inputs of the SR latch can be applied to the latch and thus change the outputs, an extra input is used. This input is called the Enable. If the Enable is 0 then the S and R inputs have no effect on the outputs of the SR latch. If the Enable is 1 then the Gated SR latch behaves as a normal SR latch.

Circuit Diagram




Logic Symbol




Truth Table

| EN | S | R | Q+ |
|---|---|---|---|
| 0 | 0 | 0 | Q |
| 0 | 0 | 1 | Q |
| 0 | 1 | 0 | Q |
| 0 | 1 | 1 | Q |
| 1 | 0 | 0 | Q |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | U |

Truth Table

| EN | S | R | Q+ | Function |
|---|---|---|---|---|
| 0 | X | X | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

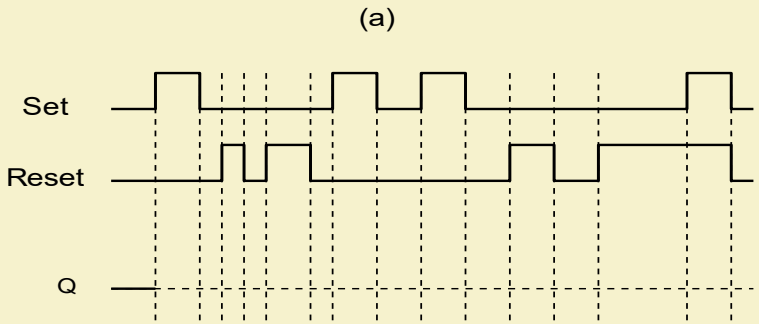
# SR Latch :- Example

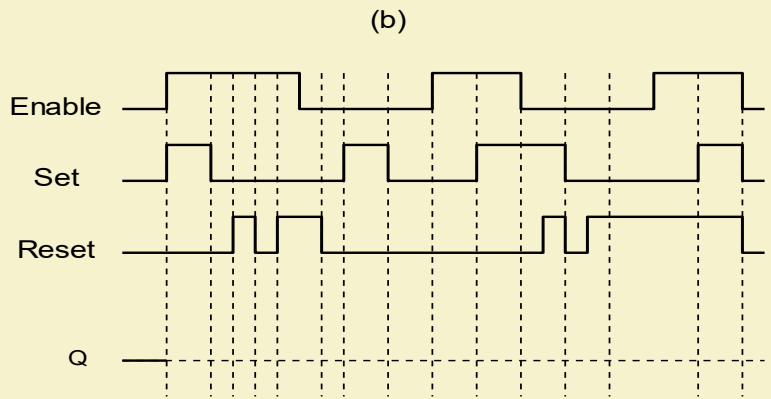
Complete the timing diagrams for :

(a) Simple SR Latch

(b) SR Latch with Enable input.

Assume that for both cases the Q output is initially at logic zero.

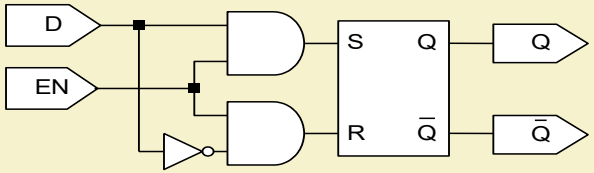


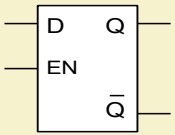
# The Data (D) Latch

A problem with the SR latch is that the S and R inputs can not be at logic 1 at the same time. To ensure that this can not happen, the S and R inputs can by connected through an inverter. In this case the Q output is always the same as the input, and the latch is called the Data or D latch. The D latch is used in Registers and memory devices.

Circuit Diagram




Logic Symbol




Truth Table

| EN | D | Q | Q+ |
|---|---|---|---|
| 0 | 0 | 0 | Q |
| 0 | 0 | 1 | Q |
| 0 | 1 | 0 | Q |
| 0 | 1 | 1 | Q |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

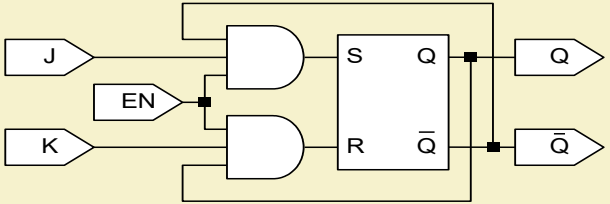
Truth Table

| EN | D | Q+ | Function |
|---|---|---|---|
| 0 | 0 | | |
| 0 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |

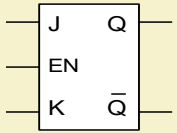
# The JK Latch

Another way to ensure that the S and R inputs can not be at logic 1 simultaneously, is to cross connect the Q and Q' outputs with the S and R inputs through AND gates. The latch obtained is called the JK latch. In the J and K inputs are both 1 then the Q output will change state (Toggle) for as long as the Enable 1, thus the output will be unstable. This problem is avoided by ensuring that the Enable is at logic 1 only for a very short time, using edge detection circuits.

Circuit Diagram




Logic Symbol




Truth Table

| EN | J | K | Q | Q+ |
|---|---|---|---|---|
| 0 | X | X | X | Q |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

Truth Table

| EN | J | K | Q+ | Function |
|---|---|---|---|---|
| 0 | X | X | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

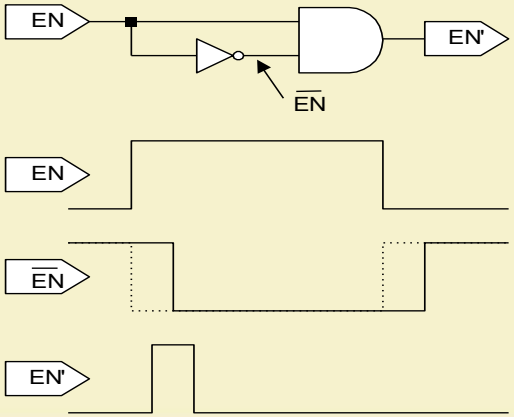
# Latches and Flip-Flops

- **Latches** are also called **transparent** or **level triggered** flip flops, because the change on the outputs will follow the changes of the inputs as long as the Enable input is set.
- **Edge triggered** flip flops are the flip flops that change there outputs only at the transition of the Enable input. The enable is called the Clock input.

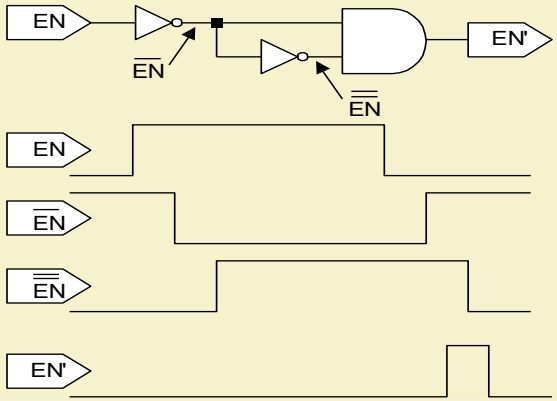
# Edge Detection Circuits

Edge detection circuits are used to detect the transition of the Enable from logic 0 to logic 1 (positive edge) or from logic 1 to logic 0 (negative edge). The operation of the edge detection circuits shown below is based on the fact that there is a time delay between the change of the input of a gate and the change at the output. This delay is in the order of a few nanoseconds. The Enable in this case is called the Clock (CLK)

Positive Edge Detection



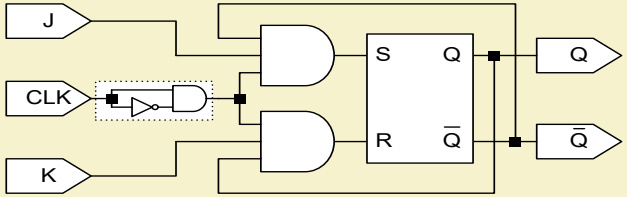

Negative Edge Detection



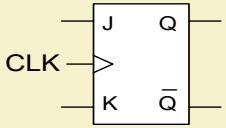
# The JK Edge Triggered Flip Flop

The JK edge triggered flip flop can be obtained by inserting an edge detection circuit at the Enable (CLK) input of a JK latch. This ensures that the outputs of the flip flop will change only when the CLK changes (0 to 1 for +ve edge or 1 to 0 for –ve edge)

## Positive Edge JK Flip Flop

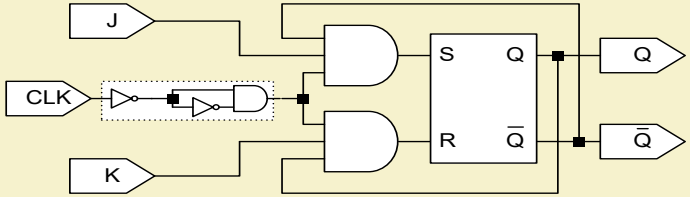



Logic Symbol

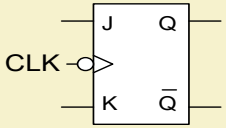



| CLK | J | K | $Q_{N+1}$ | Function |
|---|---|---|---|---|
| ⌐ | X | X | Q | |
| ↑ | 0 | 0 | Q | |
| ↑ | 0 | 1 | 0 | |
| ↑ | 1 | 0 | 1 | |
| ↑ | 1 | 1 | Q’ | |

## Negative Edge JK Flip Flop




Logic Symbol

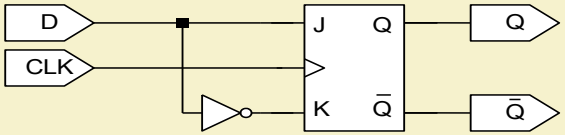



| CLK | J | K | $Q_{N+1}$ | Function |
|---|---|---|---|---|
| ⌐ | X | X | | |
| ↓ | 0 | 0 | | |
| ↓ | 0 | 1 | | |
| ↓ | 1 | 0 | | |
| ↓ | 1 | 1 | | |

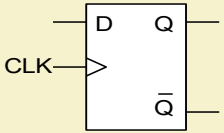
# The D Edge Triggered Flip Flop

The D edge triggered flip flop can be obtained by connecting the J with the K inputs of a JK flip through an inverter as shown below. The D edge trigger can also be obtained by connecting the S with the R inputs of a SR edge triggered flip flop through an inverter.

## Positive Edge D Flip Flop

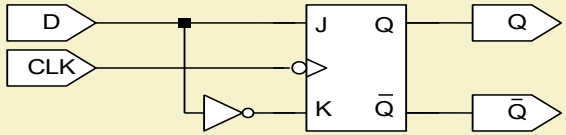



Logic Symbol

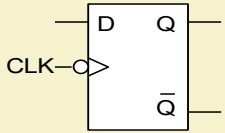



| CLK | D | $Q_{N+1}$ | Function |
|---|---|---|---|
| ↓ | X | Q | |
| ↑ | 0 | 0 | |
| ↑ | 1 | 1 | |

## Negative Edge D Flip Flop




Logic Symbol

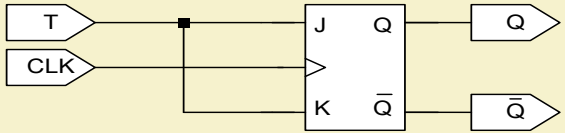



| CLK | D | $Q_{N+1}$ | Function |
|---|---|---|---|
| ↑ | X | Q | |
| ↓ | 0 | 0 | |
| ↓ | 1 | 1 | |

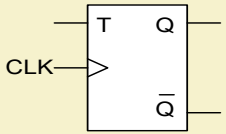
# The Toggle (T) Edge Triggered Flip Flop

The T edge triggered flip flop can be obtained by connecting the J with the K inputs of a JK flip directly. When T is zero then both J and K are zero and the Q output does not change. When T is one then both J and K are one and the Q output will change to the opposite state, or toggle.

## Positive Edge T Flip Flop

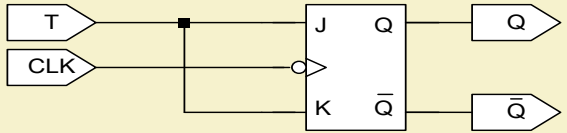



Logic Symbol

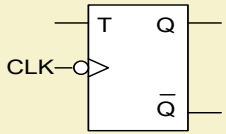



| CLK | T | $Q_{N+1}$ | Function |
|---|---|---|---|
| ↓ | X | Q | |
| ↑ | 0 | Q | |
| ↑ | 1 | Q´ | |

## Negative Edge T Flip Flop




Logic Symbol

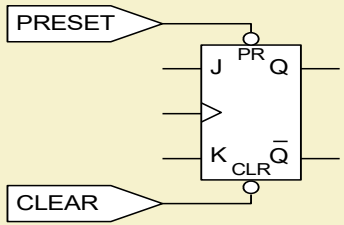



| CLK | T | $Q_{N+1}$ | Function |
|---|---|---|---|
| ↑ | X | Q | |
| ↓ | 0 | Q | |
| ↓ | 1 | Q´ | |

# Flip Flops with asynchronous inputs (Preset and Clear)

Two extra inputs are often found on flip flops, that either clear or preset the output. These inputs are effective at any time, thus are called asynchronous. If the Clear is at logic 0 then the output is forced to 0, irrespective of the other normal inputs. If the Preset is at logic 0 then the output is forced to 1, irrespective of the other normal inputs. The preset and the clear inputs can not be 0 simultaneously. If the Preset and Clear are both 1 then the flip flop behaves according to its normal truth table.

Positive Edge JK Flip Flop with Preset and Clear




| CLK | PR | CLR | J | K | $Q_{N+1}$ | Function |
|---|---|---|---|---|---|---|
| ↓ | 0 | 0 | X | X | | |
| ↑ | 0 | 1 | X | X | 1 | |
| ↑ | 1 | 0 | X | X | 0 | |
| ↑ | 1 | 1 | 0 | 0 | Q | |
| ↑ | 1 | 1 | 0 | 1 | 0 | |
| ↑ | 1 | 1 | 1 | 0 | 1 | |
| ↑ | 1 | 1 | 1 | 1 | Q’ | |

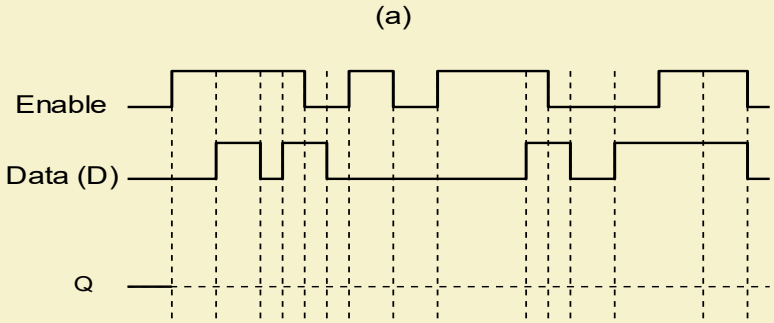
# Data (D) Latch :- Example

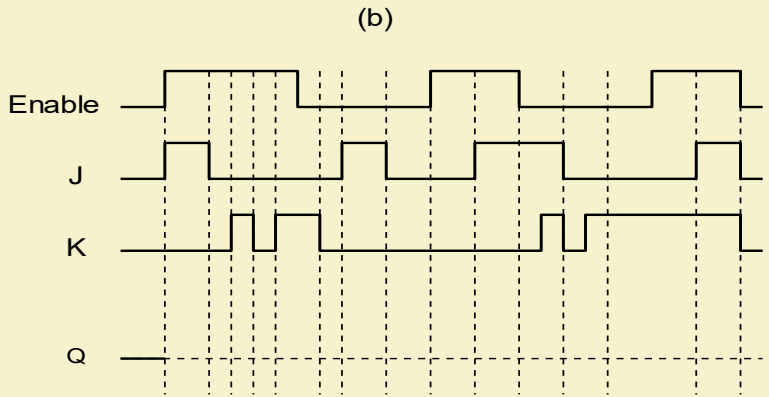
Complete the timing diagrams for :

(a) D Latch

(b) JK Latch

Assume that for both cases the Q output is initially at logic zero.



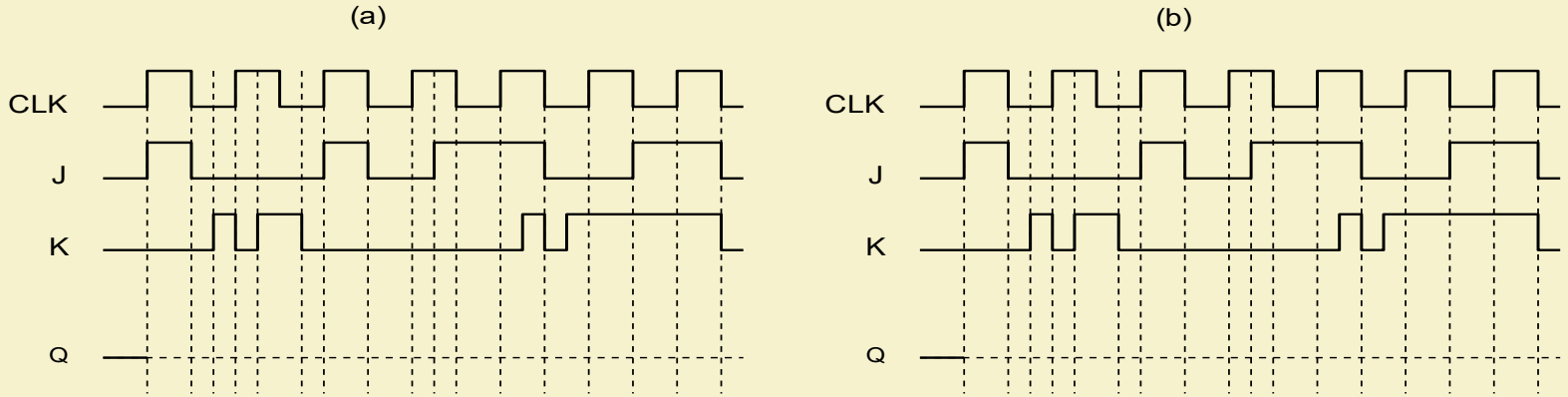
# JK Edge Triggered Flip Flop :- Example

Complete the timing diagrams for :

(a) Positive Edge Triggered JK Flip Flop

(b) Negative Edge Triggered JK Flip Flop

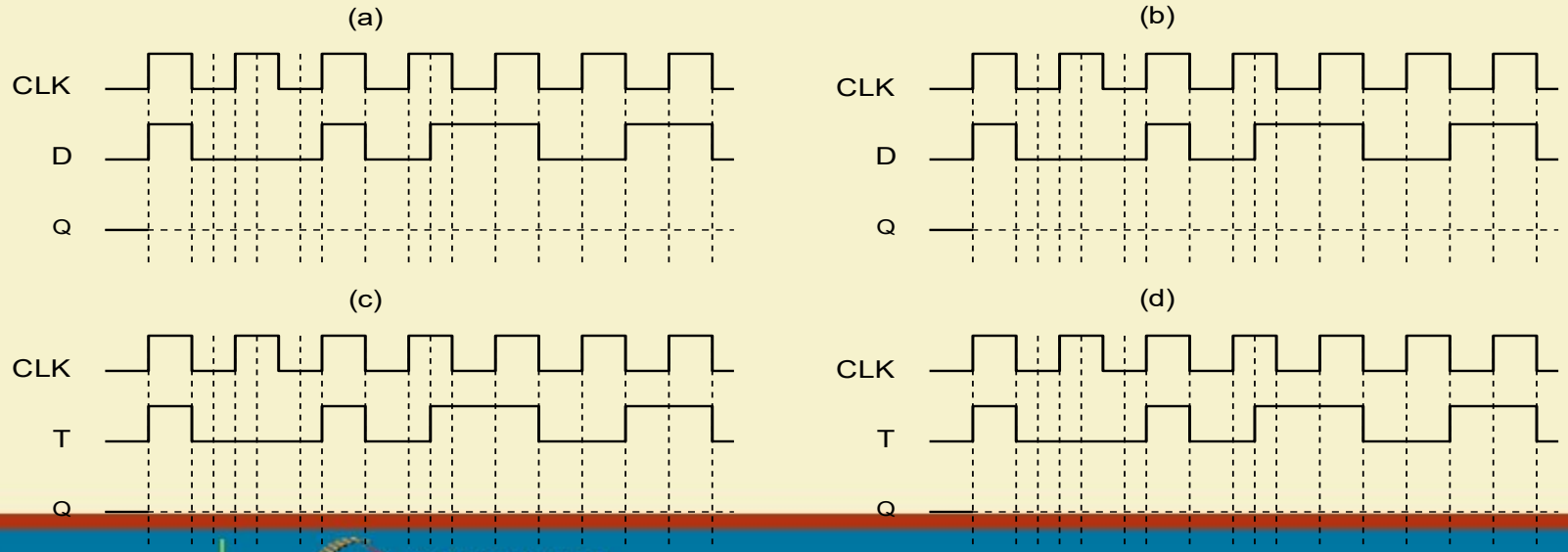
Assume that for both cases the Q output is initially at logic zero.



# D and T Edge Triggered Flip Flops :- Example

Complete the timing diagrams for :

(a) Positive Edge Triggered D Flip Flop
(b) Positive Edge Triggered T Flip Flop
(c) Negative Edge Triggered T Flip Flop
(d) Negative Edge Triggered D Flip Flop



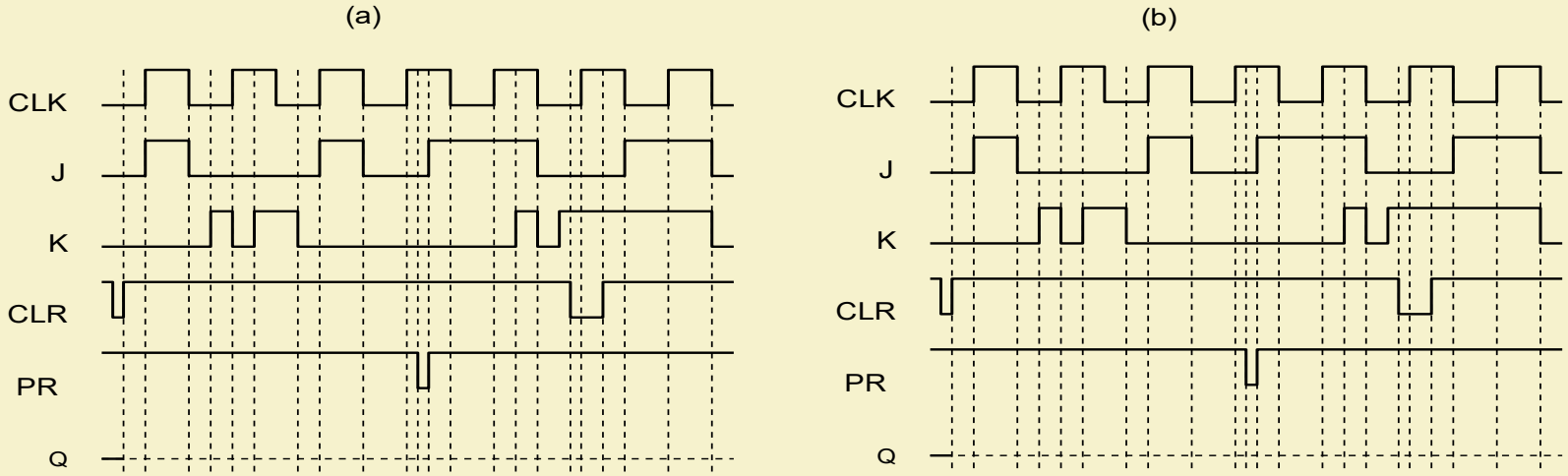
# JK Flip Flop With Preset and Clear:- Example

Complete the timing diagrams for :

(a) Positive Edge Triggered JK Flip Flop

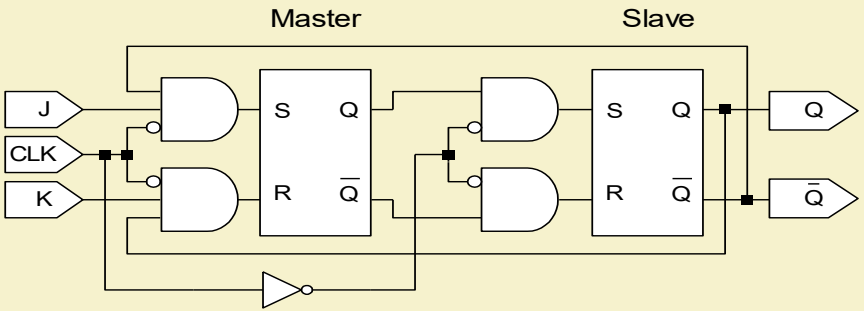
(b) Negative Edge Triggered JK Flip Flop.

Assume that for both cases the Q output is initially at logic zero.

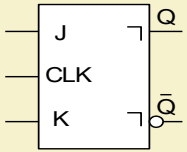


# Level Triggered Master Slave JK Flip Flop

A Master Slave flip flop is obtained by connecting two SR latches as shown below. This flip flop reads the inputs when the clock is 1 and changes the output when the clock is at logic zero.



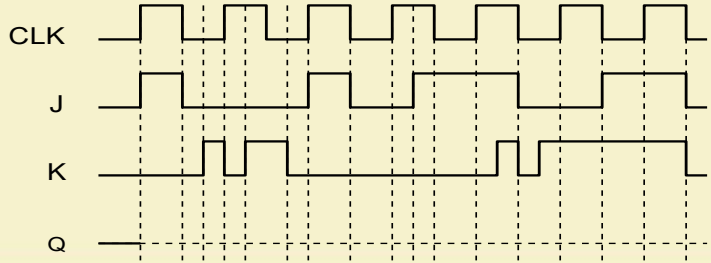

Logic Symbol



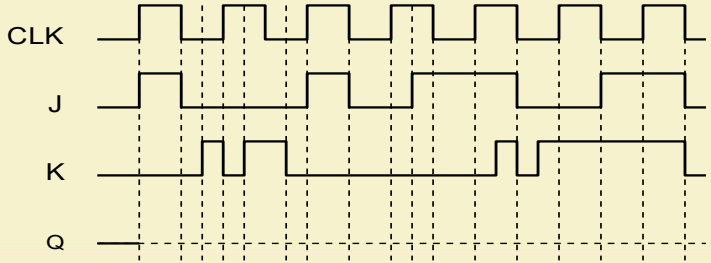

Truth Table

| CLK | J | K | Q | Function |
|---|---|---|---|---|
| ⎍ | 0 | 0 | | |
| ⎍ | 0 | 1 | | |
| ⎍ | 1 | 0 | | |
| ⎍ | 1 | 1 | | |

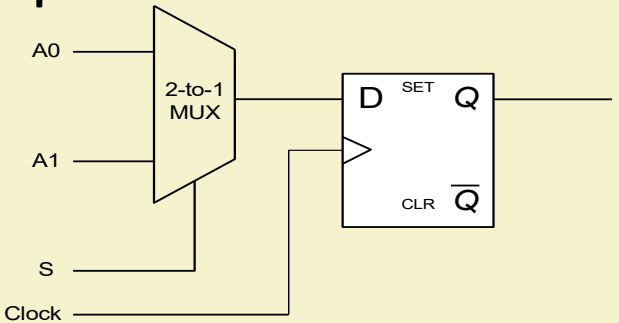
(a) Positive Master Slave JK Flip Flop

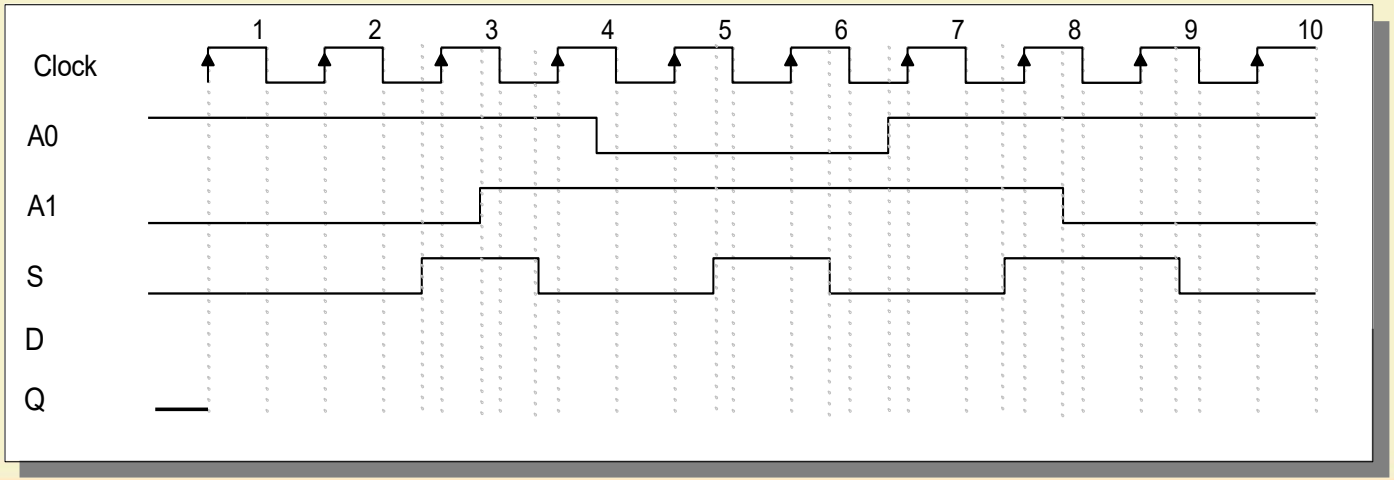



(b) Negative Master Slave JK Flip Flop



# Sequential circuit example



# Sequential circuit example