Spring 2015 Week 5 Module 27

Digital Circuits and Systems

Introduction to State Machines

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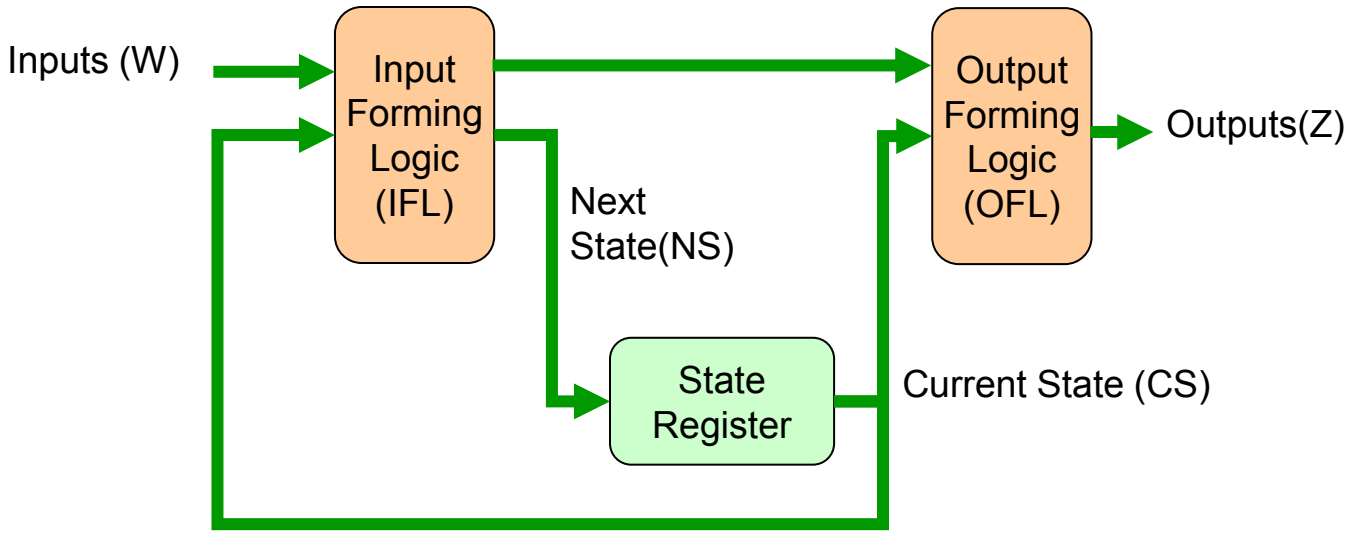
Synchronous Sequential Circuits

- Realized using combinational logic and one or more flipflops
- Circuit has a set of primary inputs W
- It has a set of primary outputs Z
- The value of the flipflops at any point of time is called the *state* of the system

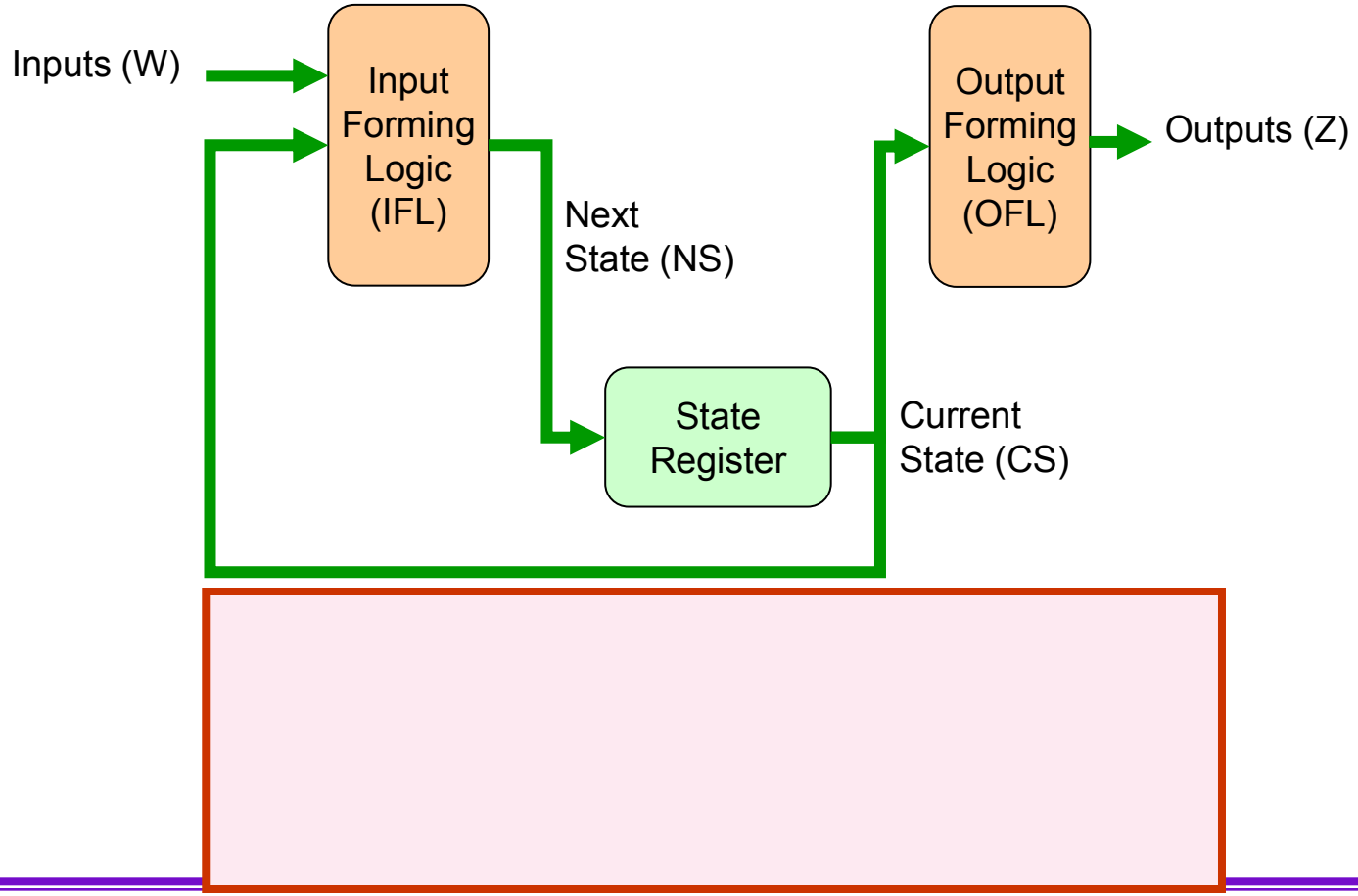
Canonical Sequential Circuit



Mealy Model

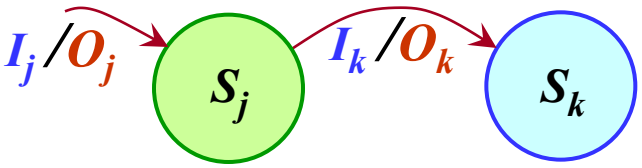
Sequential Logic – *Moore Model*

- In a Moore model outputs of a circuit are function of the present state only.

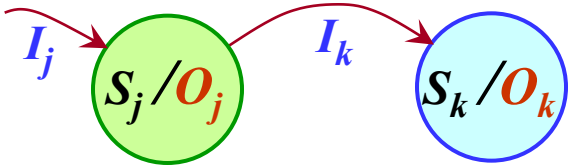


Analysis of Sequential Logic Circuits

- Given a sequential circuit, what does it do? What do the state transitions look like ?
- Analysis of sequential networks is done in three steps:
  1. **Logic Equations:** Determine the *flip-flop excitation* and sequential circuit *output logic equations*.
  2. **State Table:** State table is a tabular representation of the behavior of a sequential logic circuit. For a given input and present state of a circuit, it gives the output and the next state of the circuit. It is created using the characteristic table for the appropriate flip-flop.
  3. **State Diagram:** State diagram is a graphical depiction of a sequential logic circuit. Circles in this diagram depict the states and directed arcs depict the transitions.

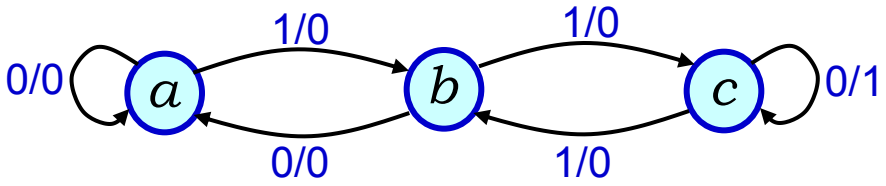


Mealy Model



Moore Model

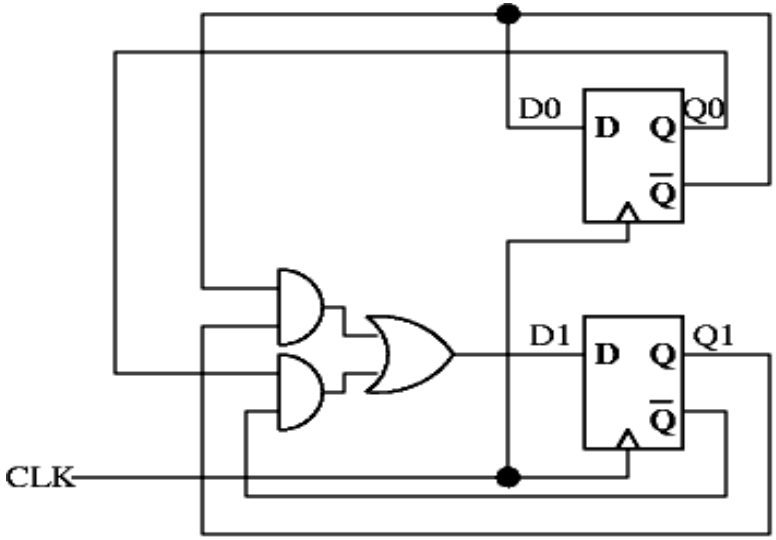
State Table and State Diagram



Present State	Next State		Output (z)	
	$x = 1$	$x = 0$	$x = 1$	$x = 0$
a	b	a	0	0
b	c	a	0	0
c	b	c	0	1

Input (x)	Present State	Next State	Output (z)
0	a	a	0
0	b	a	0
0	c	c	1
1	a	b	0
1	b	c	0
1	c	b	0

Problem: What does the circuit do?



1. Determine the **flip-flop excitation** and **sequential circuit output logic equations**.

$$D_0 = \overline{Q_0}$$

$$D_1 = Q_1\overline{Q_0} + \overline{Q_1}Q_0$$

(*there are no explicit outputs in the above circuit*)

2. **State Table**: Use the characteristic table for D flip-flop

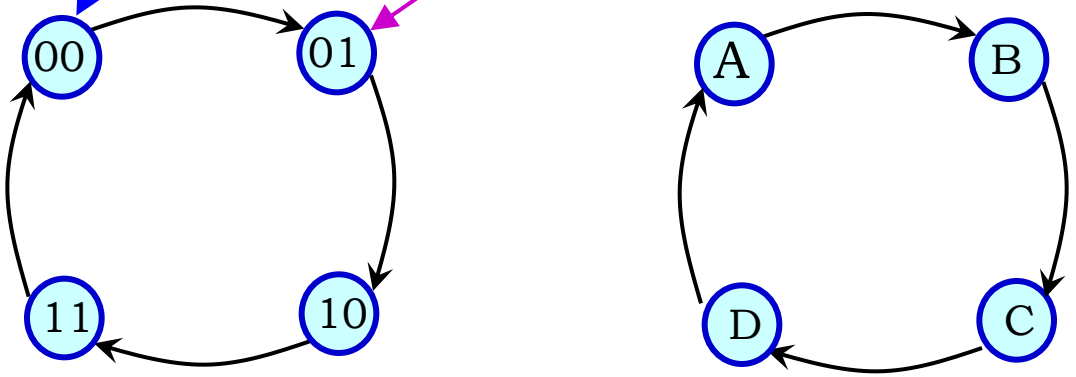
CLK	D	Q*
↑	0	0
↑	1	1

$$D_0 = \overline{Q_0}$$

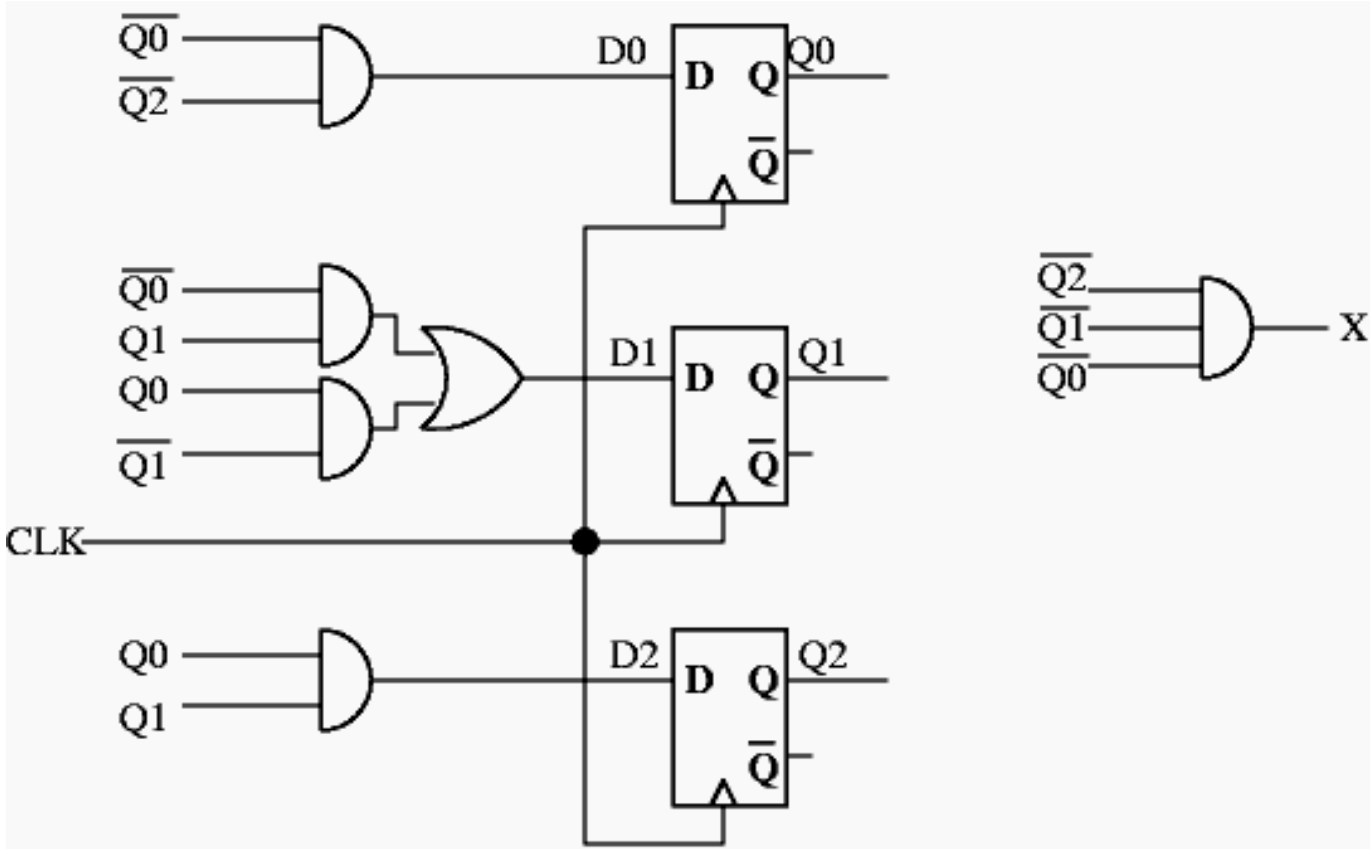
$$D_1 = Q_1\overline{Q_0} + \overline{Q_1}Q_0$$

Input (none)	Present State		Flip-flop Inputs		Next State		Output (none)
	Q_1	Q_0	D_1	D_0	Q_1*	Q_0*	
	0	0	0	1	0	1	
	0	1	1	0	1	0	
	1	0	1	1	1	1	
	1	1	0	0	0	0	

3. **State Diagram**:



Homework



Problem: Detect two consecutive 1's

- A single input bit *w* is coming in one bit at a time.
- All changes must occur in the positive edge of the clock
- Detect two consecutive 1's. Output *z* must be 1 if for two immediately preceding cycles the input *w* was 1.

Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	0
z:	0	0	0	0	1	0	0	1	1	0	0

Problem: Detect two consecutive 1's or 0's

- A single input bit *w* is coming in one bit at a time.
- All changes must occur in the positive edge of the clock
- Detect two consecutive 1's. Output *z* must be 1 if for two preceding cycles the input *w* had 1 in both cycles or 0 in both cycles.

Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	0
z:	0	1	0	0	1	0	0	1	1	0	1

Problem: Detect 011

- A single input bit *w* is coming in one bit at a time.
- All changes must occur in the positive edge of the clock
- Detect two consecutive 1's. Output *z* must be 1 if for three preceding cycles the input *w* had 011 as the input pattern.

Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	0
z:	0	0	0	0	1	0	0	1	0	0	0

End of Week 4: Module 27

Thank You