Computer Organisation and Architecture

Course Code: CO206

Module-5- Input Output Organisation-Modes of Transfer

Contents of Module 5

- Programmed I/O
- Interrupt initiated I/O
- Direct Memory Access
- I/O Channels and Processors
- Serial Communication: Synchronous Communication
- Asynchronous Communication
- Standard Communication Interfaces

Modes of Data Transfer in I/O

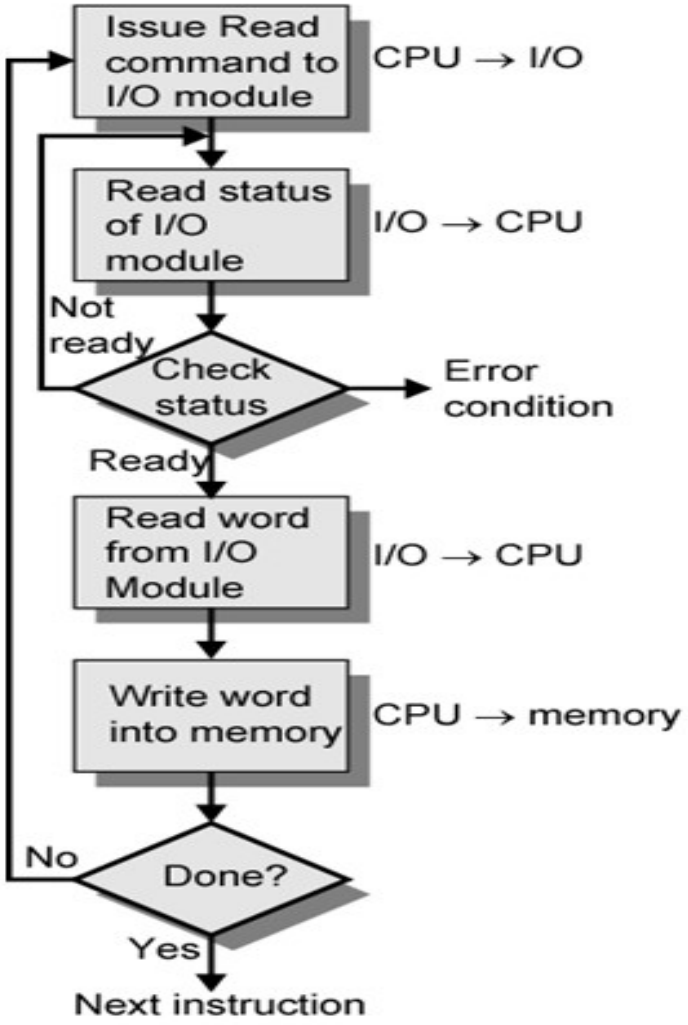
- Programmed I/O
- Interrupt Driven I/O
- Direct Memory Access(DMA)

Programmed I/O

- **Programmed I/O operations** are the **result of I/O instructions written** in the computer **program**.
- Each **data item transfer** is **initiated by an instruction** in the program.
- Usually the **transfer is to and from CPU registers and Peripheral**.
- **Transferring** data **under program control requires constant monitoring** of the **peripheral by the CPU**
- **Once** a **data transfer** is **initiated**, the **CPU** is **required to monitor** the **interface** to see when a transfer can again be made.
- In this method, **the CPU stays in program loop until the I/O unit indicates** that it is **ready for data transfer**.
- It is a **time consuming process** since it **keeps the processor busy** needlessly.

Programmed I/O

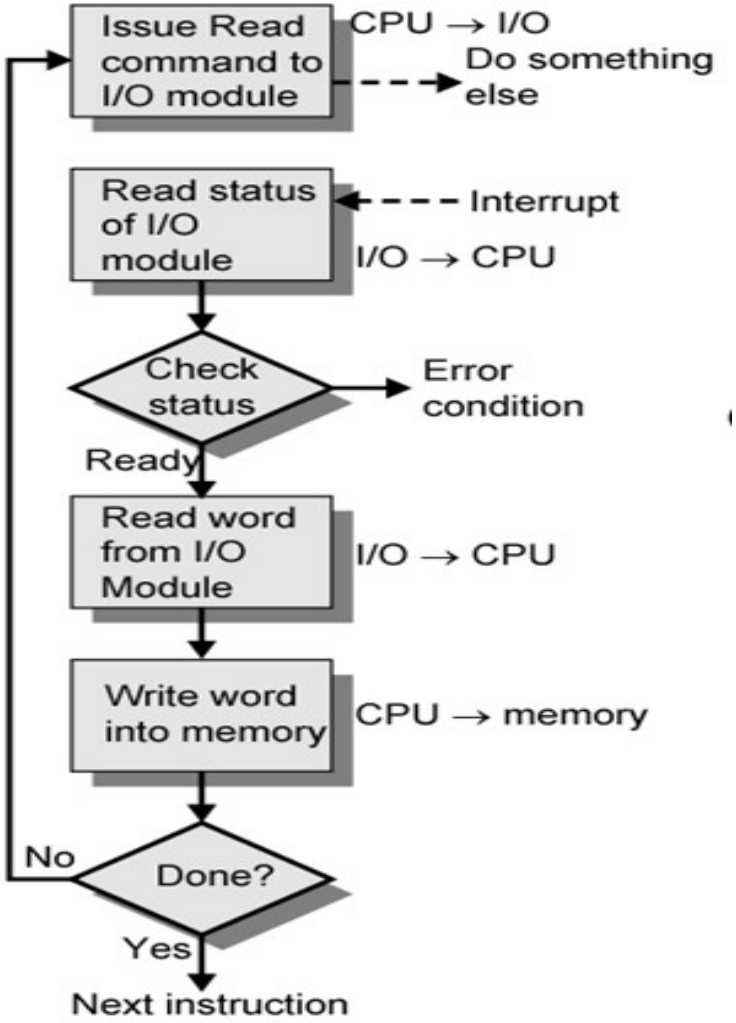
- **CPU** while executing a program **encounters an I/O instruction**
- CPU **issues I/O command** to I/O module
- **I/O module performs the requested action** and **set status registers**
- **CPU** is **responsible to check** the **status register periodically** to see if I/O operation is complete
- **No interrupt** to **alert** the CPU



Interrupt Initiated I/O

- **Programmed I/O needs continuous CPU involvement.**
- CPU **needs to slow down** to I/O speed.
- It can be **avoided by Interrupt**: Open **communication only** when some **data** has **to be transferred**
- **I/O interface**, instead of the CPU, **monitors the I/O device**
- **When** the **interface determines** that the **I/O device** is **ready** for data transfer, it **generates** an **Interrupt Request** to the CPU.
- In the **mean time** the **CPU** can **proceed** to execute **another program**.
- Upon **detecting** an **interrupt**, **CPU stops momentarily** the task it is doing, **branches to** the **service routine** to **process** the **data transfer**, and **then returns** to the **task** it was performing

Interrupt Initiated I/O

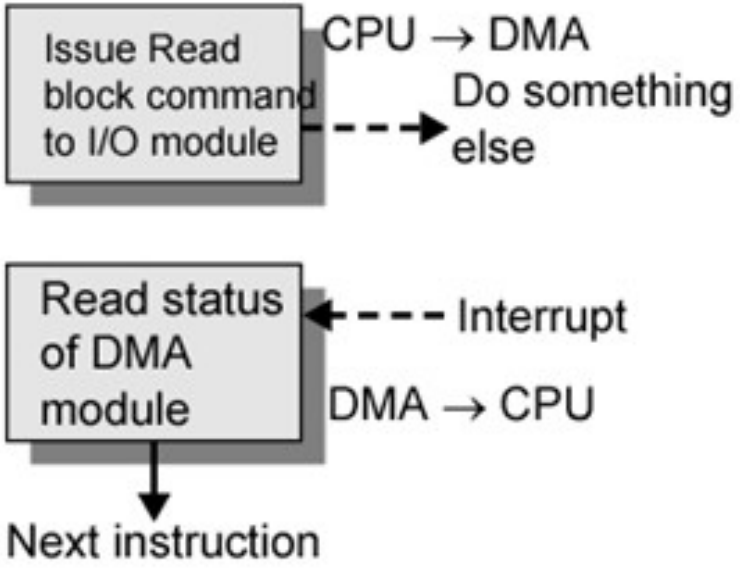


Direct Memory Access

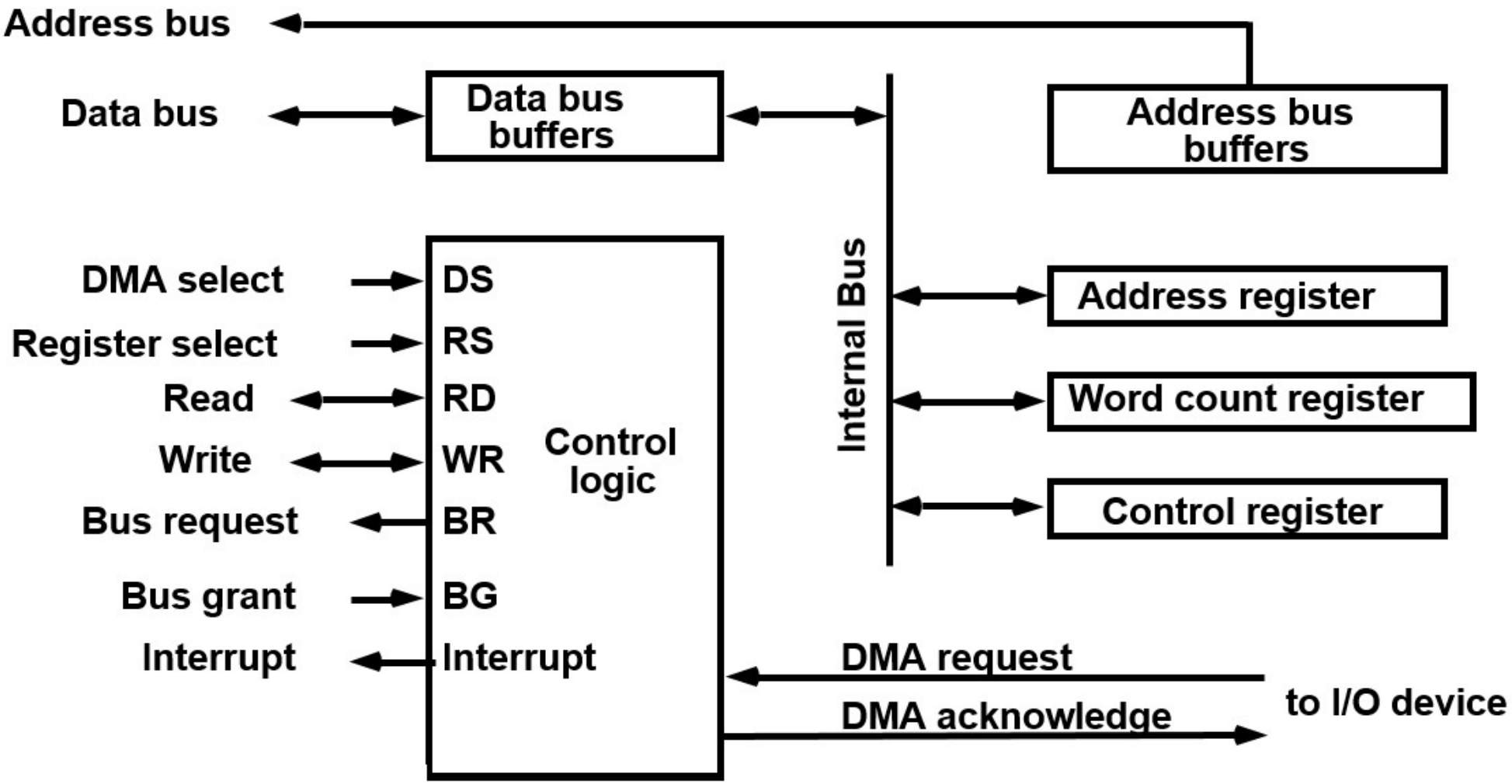
- It is **an I/O technique used for high speed data transfer.**
- In DMA, the **interface transfers data into and out of the memory unit** through the memory bus.
- In DMA, the **CPU releases the control of the bus to a device** called a **DMA controller**
- **Removing** the **CPU from** the **path** and **letting the peripheral device manage** the **memory buses directly** would **improve** the **speed of transfer**.
- The **CPU initiates** the **transfer by supplying the interface** with the **starting address** and **the number of words** needed to be transferred and **then proceeds to execute** the **other tasks**.
- **When** the **transfer is to be made**, the **DMA requests** the **memory cycles** through the memory bus.

Direct Memory Access

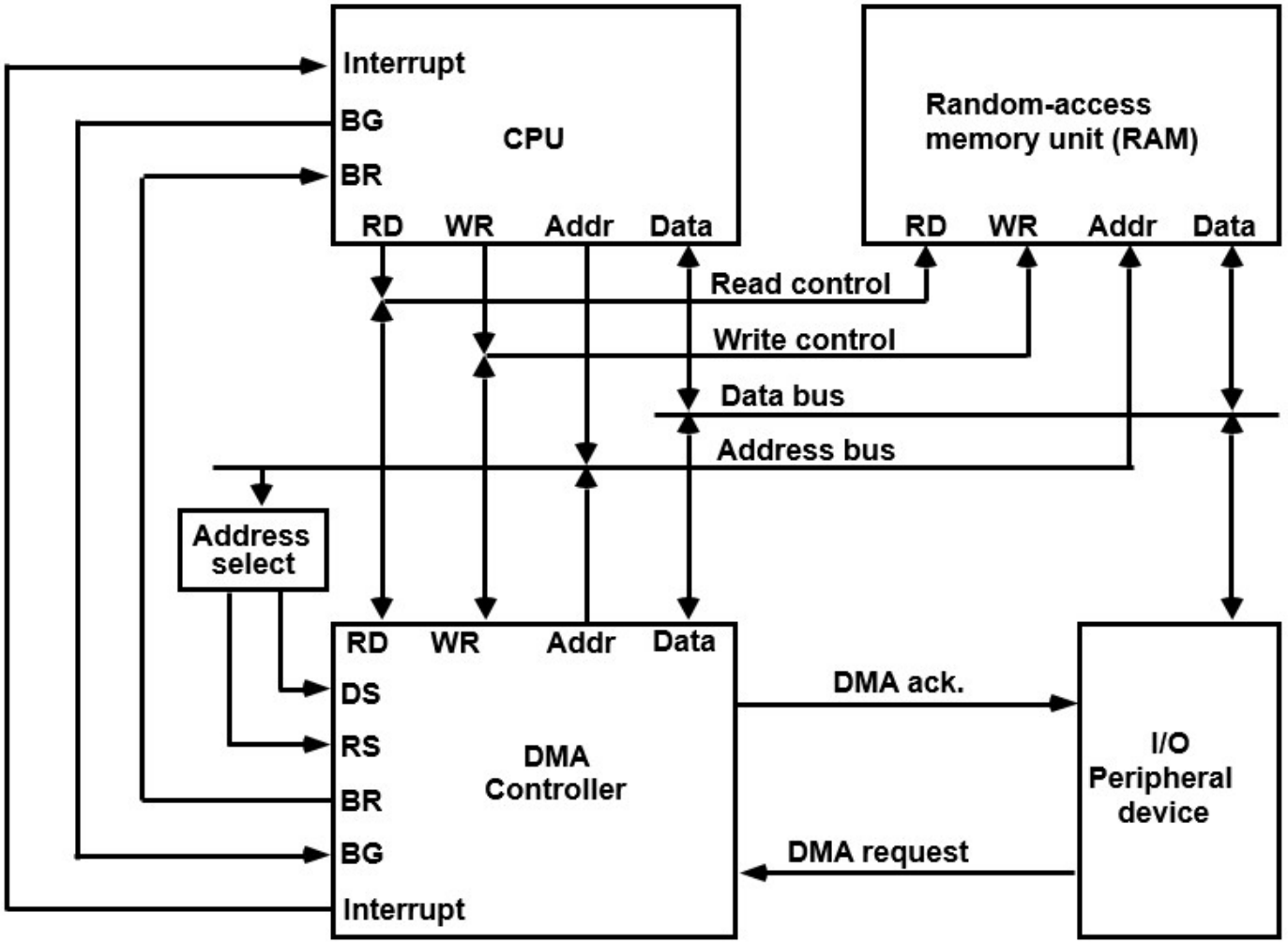
- **When** the **request is granted** by the memory controller, the **DMA transfers the data directly into memory**
- The **CPU merely delays its memory access operation to allow the direct memory I/O transfer.**



Block Diagram of DMA Controller



DMA Transfer

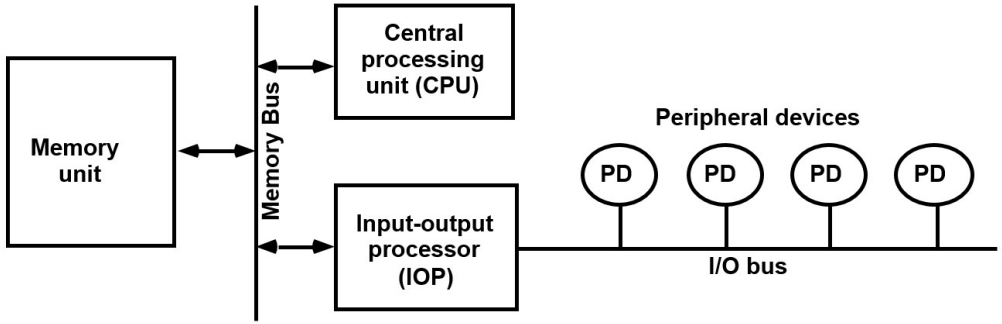


Burst Transfer and Cycle Stealing

- **When** the **DMA takes control of** the **bus system**, **it communicates directly with the memory**. The transfer can be made in several ways.
- In **DMA burst transfer**, **a block** sequence consisting **of** a number of **memory words** is **transferred in a continuous burst** while the DMA controller is master of the memory buses.
- **This mode** of transfer is **needed for fast devices** such as magnetic disks, where **data transmission cannot be stopped or slowed down until an entire block is transferred**.
- An alternative technique called **cycle stealing** allows the **DMA controller** to **transfer one data word at a time**, after which **it must return control of the buses to the CPU**.
- The **CPU merely delays** its **operation for one memory cycle** to allow the direct memory I/O transfer to **“steal” one memory cycle**.

I/O Processors

- **Instead** of **having each interface communicate with** the **CPU**, a **computer may incorporate one or more external processors** and **assign** them the **task of communicating directly with all I/O devices**.
- An **input–output processor (IOP)** may be classified as a processor **with direct memory access capability that communicates with I/O devices**.
- The IOP is **similar to a CPU except** that **it is designed to handle the details of I/O processing**.
- **Unlike** the **DMA controller that must be set up entirely by the CPU**, the **IOP can fetch and execute its own instructions**



CPU and IOP Communication