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Question -

Assignment - 2

Q Virtual Memory for Windows

* Windows uses demand paging with clustering meaning they page in multiple pages whenever a page fault occurs.

* The working set minimum and maximum are normally set at 50 and 345 pages respectively.

* Free pages are maintained on a free list, with a minimum threshold indicating when there are enough free frames available.

* If a page fault occurs and the process is below their maximum, then additional pages are allocated. Otherwise some pages from this process must be replaced, using a local page replacement algorithm.

* If the amount of free frames falls below the available threshold then working set trimming occurs, taking frames away from any processes which are above their minimum until all are at their minimums. Then additional frames can be allocated to processes that need them.

Virtual Memory for Solaris

* Solaris maintains a list of free pages and allocates one to faulting thread whenever a fault occurs. It is therefore imperative that a minimum amount of free memory be kept on hand at all times.

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- Solari's also maintains a cache of pages that have been reclaimed but which have not yet been overwritten, as opposed to the free list which only holds pages whose current contents are invalid. If one of the pages from the cache is needed before it gets moved to the free list, then it can be quickly recovered.

- If free memory falls below minfree, then pages runs with every page fault.

- Recent releases of Solari's have enhanced the virtual memory management system including recognizing pages from shared libraries and protecting them from being paged out.

Q8.1 A logical address does not refer to an actual existing address, rather, it refers to an abstract address in an abstract address space contrast this with a physical address that refers to an actual physical address in memory. A logical address is generated by CPU and is translated into a physical address by the MMU.

Q8.3 Paging is implemented by breaking up an address into a page and affect number. It is most efficient to break the address into X page Y offset bits, rather than perform arithmetic on the address to calculate the page number and

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offset. Because each bit position represents a power of 2, splitting an address between bits results in a page size that is a power of 2.

Q8.4 a) Logical address : 16 bits

b) Physical address : 15 bits

Q 8.5 By allowing two entries in a page table to point to the same page frame in memory, users can share code and data. If the code is reentrant, much memory space can be saved through the shared use of large programs such as text editors, compilers and database systems. "copying" large amounts of memory could be effected by having different page tables point to the same memory location.

Q 8.10 a) In a conventional single-level page table

$$-2^{11} < 4000 < 2^{12}$$

So we need 12 out of 32-bit logical address for the offset. Then we have 32-12=20 bits left for the page number.

⇒ 2^{20} = 1048576 entries

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b) An inverted page table

Size of physical address space = No. of frames x frame size

Where page size = frame size

No. of frames = $2^{29}/2^{12} = 2^{17}$

⇒ Number of entries = 2^{17} = 131072 / 1024 = 128 K entries

Q8.15 The contiguous memory allocation scheme suffers from external fragmentation and does not allow processes to share code.

Pure segmentation also suffers from external fragmentation and enables process share code.

Pure paging suffers from internal fragmentation and enables processes.

Q8.16 On a system with paging a process cannot access memory that it does not own because an address on a paging system is a logical page number and an offset.
The physical page is found by searching a table based on the logical page number to produce a physical page number. The OS controls the contents of this table, which limits the process of accessing only those physical pages allocated to the process.

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There is no way for a process to refer to a page it does not own because the page will not be in the page table.

Q8.19 When the TLB attempts to resolve virtual page numbers, it ensures that the Address space Identifies (ASIDs) for the currently running process matches the ASID associated with the virtual page. If the ASIDs do not match, the attempt is treated as a TLB miss.

So ASIDs are used to provide address space protection in the TLB as well as supporting TLB entries for several different processes at the same time.

Q9.1 A page fault occurs when an access to a page that has not been brought into main memory takes place. The OS verifies the memory access, aborting the programe if it is invalid. If it is valid a free frame is located and I/O is requested to read the needed page into free frame. Upon completion of I/O the process table and page table are updated and the instruction is restarted.

Q9.2 a) lower bound on the number of page faults = n

b) upper bound on the number of page faults = p

Q9.5 The costs are additional hardware and slower access time. The benefits are good utilization of memory and larger logical address space than physical address space.

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Q9.6 For every memory access operation, the page table needs to be consulted to check whether the corresponding page is resident or not and whether the program has read or write priveleges for accessing the page. These checks would have to be performed in hardware. A TLB could could serve as a cache and improve performance of the lookup operation.

Q9.8

No. of frames	LRU	FIFO	Optimal
1	20	20	20
2	18	18	15
3	15	16	11
4	10	14	8
5	8	10	7
6	7	10	7
7	7	7	7

Q9.9 LRU = 18
FIFO = 17
Optimal = 13

Q9.10 You can use the valid/invalid bit supported in hardware to simulate the reference bit. Initially set the bit to invalid. On first reference a trap to the OS is generated. The OS will set a software bit to 1 and reset the valid/invalid bit to valid.

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Q9.11 NO. An optimal algorithm will not suffer from Belady's anomaly because - by definition an optimal algorithm replaces the page that will not be used for the longest time. Belady's anomaly occurs when a page replacement algorithm evicts a page that will be needed in the immediate future. An optimal algorithm would not have selected such a page.

Q9.12 a) Thrashing is occuring
b) CPU utilization is sufficiently high to leave things alone, and increase degree of multiprogramming.
c) Increase the degree of multiprogramming.

Q9.14 The page table can be set up to simulate base and limit registers provided that the memory is allocated in fixed size segments In this way, the base of segment can be entered into a page table and the valid/invalid bit used to indicate that position of the segment as resident in the memory. There will be some problem with internal fragmentation.

Q9.17 a) can occur
b) can occur
c) can occur
d) can't occur

Q9.20 Given : virtual memory = 2^{32} bytes
physical memory = 2^{22} bytes

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page size = 2^{12} bytes

Given physical address = 1112345 6

Size of page table = $\frac{\text{Virtual memory}}{\text{page size}} = \frac{2^{32}}{2^{12}} = 2^{20}$.

⇒ 20 bits are used for page table entry and its frame number whereas last 12 bits are used from displacement into page.

$$\underbrace{00010001000100\,100011}_{\text{page table size}} \quad \underbrace{010001010110}_{\text{page size}}$$

Software and Hardware

Hardware part of the system handless dynamic address translation, whereas software operations take care of faulty pages, reading the resulting page and repeating the process whenever required.

Q10.4 A cystem can perform only at the speed of it slowest bottleneck. Disks or disk controllers are frequently the bottleneck in modern systems as their individual performance cannot keep up with that of the CPU and system bus. By balancing I/O among disks and controllers, neither an individual disk nor a controller is overwhelmed, so that bottleneck is avoided.

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Q11.5 DMA increases system concurrency by allowing the CPU to perform tasks while the DMA system transfers data v/a the system and memory buses. Hardware design is complicated because the DMA must be integrated into the system and the system must allow the DMA controller to be a bus master. Cycle stealing may also be necessary to allow the CPU and DMA controller to share use of the memory bus.

Q11.7 The STREAMS driver controls a physical device that could be involved in a STREAMS operation. The STREAMS module modifies the flow of data between the head (the user interface) and the driver.

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