ECE213: Digital Electronics SET-E

Regd. No:..... Roll no... ……

Section…….....

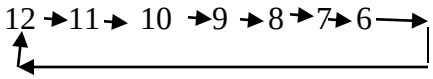
Time Allowed: 45 Min Max Marks: 30

This paper contains 6 questions of 5 marks. All questions are compulsory.

Q1 Design PQ flip flop using SR for which truth table is given below.

P	Q	Q_{N+1}
0	1	0
1	1	X
0	0	Q'n
1	0	Qn

Q2. Design a ripple counter for the following state diagram.



Q3. Draw the diagram of SISO 4-bit using SR flip flop. Each flip flop triggered on a positive clock pulse. Draw the output waveform for all flip flop when input data is 0101 which is fed from right to left.

Q4. Design a synchronous counter using negative edge clock pulse using T flip flop for the following sequence.

$1^2 \rightarrow 2^2 \rightarrow 3^2 \rightarrow 0^2 \rightarrow 1^2$

Q5. If the input clock frequency of 40 GHz is applied to 10-bit ring counter, then to MOD-8 twisted ring counter then to MOD-10 ripple counter after that it is passed to BCD synchronous counter. What is the output frequency?

Q6 Consider the JK FF using positive edge clock pulse. Draw its logic diagram along its truth table and design output waveform for Q, initially Q=1.