IEC 103

Assignment - 9

Analog to Digital Converters

1. A 12 bit ADC of the dual slope type utilizes a 1 MHz clock and has $V_{ref} = 10V$. Its analog input voltage is in the range of 0 to -10V. The fixed interval T_1 is the time taken for the counter to accumulate a count of 2^N. What is the time required to convert an input voltage equal to the full scale value? If the peak voltage reached at the output of the integrator is 10V, what is the integrator time constant? If through aging R increases by 2% and C decreases by 1%, what does V_{peak} become? Does the conversion accuracy change?

2. Consider the design of a 4 bit flash ADC. How many comparators are required? For an input signal in the range of 0 to +10V, what are the reference voltages needed? Show how they can be generated using a 10V reference voltages needed? Show how they can be generated using a 10V reference and several 1KΩ resistors. If a comparison is possible in 50ns and the associated logic requires 35ns, what is the maximum possible conversion rate? Indicate the digital code you expect at the logic output for an input of (a) 0V (b) +5.1V and (c) 10V.

3. An 8 bit ADC produces a full scale output of 11111111 with a 2V input signal. Determine the output word given the following inputs.
   a. 100 mV
   b. 10 μV
   c. 0V
   d. 1.259V

4. Given a 14 bit ADC,
   a. Determine the number of comparators needed for flash technique.
   b. Determine the number of comparisons needed if successive approximation is used.

5. Assume that comparators / logic delays, amplifier settling times and other factors require 4 μs total in a particular IC fabrication technique. If this technology is used to create A/D converters, determine the maximum conversion time for the following 8 bit converters:
   a. Flash
   b. Successive Approximation
   c. Staircase / Ramp type.