Assignment-1

1. An amplifier operating from a single 15V supply provides a 12-V peak to peak sine wave signal to a 1KΩ load and draws negligible input current from the signal source. The dc current drawn from the 15V supply is 8mA. What is the power dissipated in the amplifier and what is the amplifier efficiency?

2. Consider a transistor amplifier with transfer characteristic:

$$V_o = 10 - 10^{-11} e^{40V_I}$$

, which applies for $V_I \geq 0V$ and $V_o \geq 0.3V$. Suppose a positive input signal of 1mV is superimposed on the dc bias voltage V_I. Find the dc input voltage, V_I, corresponding to a mean output voltage $V_o = 5V$. Determine the output signal.

3. Plot I_{our} as a function of V_{out} for the circuit shown in figure 1 as V_{out} varies from 0V to 10V in 2V increments. Plot this characteristic for $I_b = 10\mu A$, $20\mu A$ and $30\mu A$.

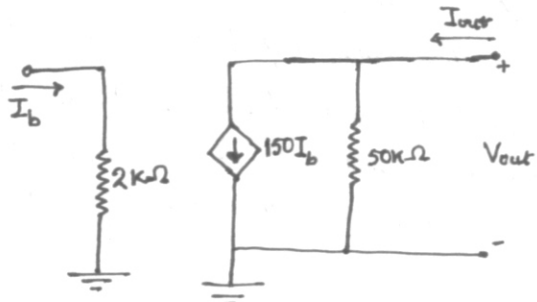
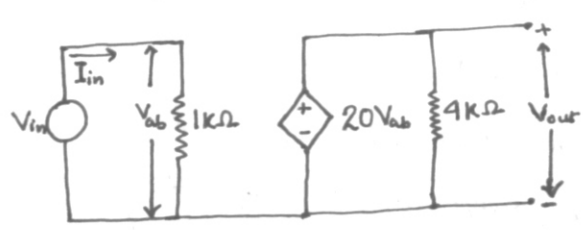
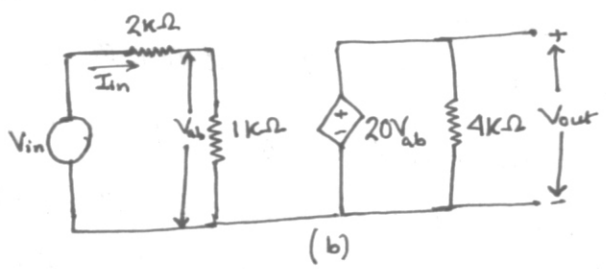


Figure 1

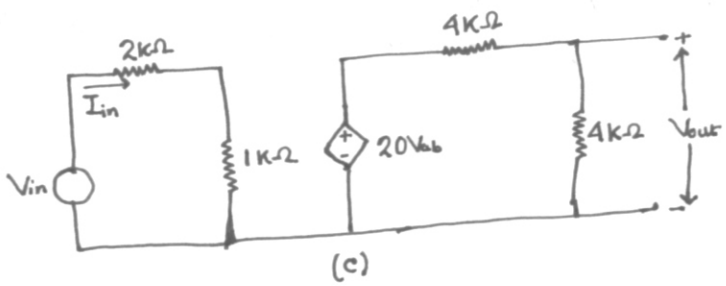
4. If $V_{in} = 0.5\cos\omega t$, calculate V_{out} for circuits in figures 2 (a), (b) and (c).



(a)



(b)



(c)

Figure 2

5. An amplifier with 40dB of small signal open circuit voltage gain, an input resistance of 1MΩ, and an output resistance of 10Ω drives a load of 100Ω. What voltage and power gains (expressed in dB) would you expect with the load connected? If the amplifier has a peak output current limitation of 100mA, what is the rms value of the largest sine wave input for which an undistorted output is possible? What is the corresponding output power available?

6. A 10mV signal source having an internal resistance of 100KΩ is connected to an amplifier for which the input resistance is 10KΩ, the open circuit voltage gain is 1000V/V, and the output resistance is 1KΩ. The amplifier is connected in turn to a 100Ω load. What overall voltage gain results as measured from the source internal voltage to the load? Where did all the gain go? What would the gain be if the source was connected directly to the load? What is the ratio of these two gains? What can you conclude from this?

7. Suppose you are given two amplifiers, A and B to connect in cascade between a 10mV, 100KΩ source and a 100Ω load. The amplifiers have voltage gain, input resistance and output resistance as follows:— For A, 100V/V, 10KΩ, 10KΩ respectively and for B 1V/V, 100KΩ, 100KΩ respectively. Suggest how the amplifiers are to be connected from source S to load L, ie. which one of SABL and SBAL is a better configuration. Explain your answer with necessary reasons.

8. Design an amplifier that provides 0·5W of signal power to a 100Ω load resistance. The signal source provides a 30mV rms signal and has a resistance of 0·5MΩ. Three types of voltage amplifier stages are available:

(a) A high input resistance type with $R_i = 1M\Omega$, $A_{vo} = 10V/V$ and $R_o = 10K\Omega$.

(b) A high gain type with $R_i = 10K\Omega$, $A_{vo} = 100V/V$ and $R_o = 1K\Omega$.

(c) A low output resistance type with $R_i = 10K\Omega$, $A_{vo} = 1V/V$ and $R_o = 20\Omega$. Design a suitable amplifier using a combination of these stages. Your design should utilize the minimum number of amplifier stages and should ensure that the signal level is not reduced below 10mV at any point in the amplifier chain. Find the load voltage and output power of your realized design.

9. It is required to design a voltage amplifier to be driven from a signal source having a 10mV peak amplitude and a source resistance of 10KΩ to supply a peak output of 3V across a 1KΩ load.
(a) What is the required voltage gain from the source to the load?
(b) If the peak current available from the source is 0.1μA, what is the smallest input resistance allowed? For the design with this value of R_i, find the overall current gain and power gain.
(c) If the amplifier power supply limits the peak value of the output open circuit voltage to 5V, what is the largest output resistance allowed?
(d) For a design with input resistance as in part (b) and output resistance as in part (c), what is the required value of open circuit voltage gain of the amplifier?
(e) If as a possible design option, you are able to increase R_i to the nearest value of the form $1\times10^n\Omega$ and to decrease R_o to the nearest value of the form $1\times10^m\Omega$ find (i) the input resistance achievable (ii) output resistance achievable (iii) open circuit voltage gain now required to meet the specifications.

10. A voltage amplifier with an input resistance of 10KΩ, an output resistance of 200Ω, and a gain of 1000 V/V is connected between a 100KΩ source with an open circuit voltage of 10mV and a 100Ω load. For this situation:-
(a) What output voltage results?
(b) What is the voltage gain from source to load?
(c) What is the voltage gain from the amplifier input to the load?
(d) If the output voltage across the load is twice that needed and there are signs of internal amplifier overload, suggest the location and value of a single resistor that would produce the desired output. Choose an arrangement that would cause minimum disruption to an operating circuit.

11. A current amplifier for which $R_i = 1K\Omega$, $R_o = 10K\Omega$, and $A_{is} = 100 A/A$ is to be connected between a 100mV source with a resistance of 100KΩ and a load of 1KΩ. What are the values of current gain i_o/i_i, of voltage gain V_o/V_s, and of power gain expressed directly and in dB?

12. A transconductance amplifier with $R_i = 2K\Omega$, $G_m = 40 mA/V$ and $R_o = 20K\Omega$ is fed with a voltage source having a source resistance of 2KΩ and is loaded with a 1KΩ resistance. Find the voltage gain realized.

13. A designer is required to provide across a 10KΩ load, the weighted sum, $V_o = 10V_1 + 20V_2$ of input signals V_1 and V_2 each having a source resistance of 10KΩ. She has a number of transconductance amplifiers for which the input and output resistances are both 10KΩ and $G_m = 20mA/V$, together with a selection of suitable resistors. Sketch an appropriate amplifier topology with additional resistors selected to provide the desired result.

14. Figure 3 shows a transconductance amplifier whose output is fed back to its input. Find the input resistance of the resulting one port network.

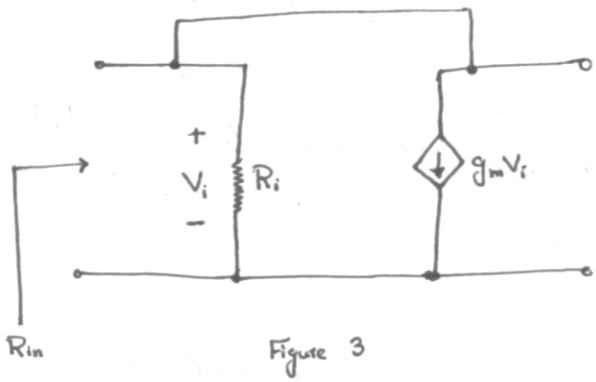


Figure 3

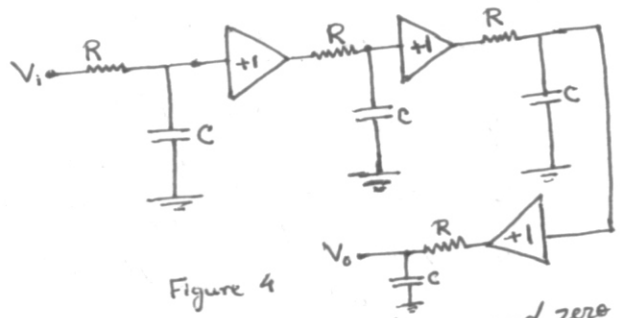


Figure 4

15. The unity gain voltage amplifiers in the circuit of figure 4 have infinite input resistances and zero output resistances, and thus they function as perfect buffers. Show that the overall gain V_o/V_i will drop by 3dB below the value at dc at the frequency for which the gain of each RC circuit is 0.75 dB down. What is that frequency in terms of C and R?

16. An internal node of a high frequency amplifier, whose Thevenin equivalent node resistance is 100KΩ, is accidentally shunted to ground by a capacitor (ie. the node is connected to ground through a capacitor), through a manufacturing error. If the measured 3dB bandwidth of the amplifier is reduced from the expected 5MHz to 100KHz, estimate the value of the shunting capacitor. If the original cut off frequency can be attributed to a small parasitic capacitor at the same internal node (ie. between the node and ground), what would you estimate it to be?

17. A designer wishing to lower the overall high frequency response of a three stage amplifier to 10KHz considers shunting one of the two nodes between the output of one stage and the input of the next stage to ground with a small capacitor. While measuring the overall frequency response of the amplifier, she shunts a capacitor of 1nF, first to node A, then to node B, lowering the 3-dB frequency from 1MHz to 100KHz and 20KHz respectively. If she knows that each amplifier stage has an input resistance of 100KΩ, what output resistance must the driving stage have at node A? What will be the output resistance at node B? What capacitor value should he connect to which node to solve his design problem most economically?

18. It is required to design an amplifier to sense the open circuit output voltage of a transducer and to provide a proportional voltage across a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1KΩ to 10KΩ. Also the load resistance varies in the range of 1KΩ to 10KΩ. The change in load voltage corresponding to the specified change in R_s should be 10% at most. Similarly, the change in load voltage corresponding to the specified change in R_L should be limited to 10%. Also, corresponding to a 10mV transducer open circuit output voltage, the amplifier should provide a minimum of 1V across the load. What type of amplifier is required? Sketch its circuit model, and specify the values of its parameters. Specify appropriate values for R_i and R_o of the form $1\times10^{m}\Omega$.

19. It is required to design an amplifier to sense the short circuit output current of a transducer and to provide a proportional current through a load resistor. The equivalent source resistance of the transducer is specified to vary in the range of 1KΩ to 10KΩ. Similarly, the load resistance is known to vary over the range of 1KΩ to 10KΩ. The change in load current corresponding to change in R_s is required to be limited to 10%. Similarly, the change in load current corresponding to the specified change in R_L should be 10% at most. Also, for a nominal short circuit output current of the transducer of 10μA, the amplifier is required to provide a minimum of 1mA through the load. What type of amplifier is required? Sketch the circuit model of the amplifier, and specify the values of its parameters. Select appropriate values for R_i and R_o of the form $1\times10^{m}\Omega$.

20. An amplifier has an input resistance of 100KΩ and an output resistance of 1KΩ. The amplifier is required to be capacitively coupled to a 10KΩ source and a 1KΩ load. Available capacitors have values only of the form 1×10^{-n}F. What are the values of the smallest capacitors needed to ensure that the corner frequency associated with each is less than 100Hz? What actual corner frequencies result? For the situation in which the basic amplifier has an open circuit voltage gain (A_{vo}) of 100 V/V, find an expression for $T(s)=\frac{V_o(s)}{V_s(s)}$.