

# Olivia Hsu

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## EDUCATION

### Stanford University

Ph.D. in Computer Science (CS)

Expected June 2025

Stanford, USA

- Advisors: Kunle Olukotun and Fredrik Kjolstad
- Thesis Topic: Efficient Mapping of Sparse Applications to Accelerated Systems

### University of California, Berkeley

B.S. Electrical Engineering and Computer Science (EECS)

May 2019

Berkeley, USA

- Advisor: Vladimir Stojanović

## RESEARCH EXPERIENCE

### • Stanford Pervasive Parallelism Lab [\[🔗\]](#)

PhD Student Researcher

Jan 2020 – Present

Stanford, USA

- Researching the automatic compilation and mapping of sparse applications to domain-specific architectures, reconfigurable dataflow architectures, and hardware accelerators under professors Kunle Olukotun and Fredrik Kjolstad.
- During my PhD, I led research projects [1, 7, 10, 15, 4, 2], mentored research projects [6, 3, 14], and have helped on research projects [5, 19].

### • UC Berkeley Group Matching Project

Student Collaborator

Aug 2020 – Aug 2021

Remote

- Helped develop a scalable and inclusive study group matching process for student collaboration under Professor Gireeja Ranade, which led to [8].

### • Stanford VLSI Group

PhD Student Researcher

Sep 2019 – Jan 2020

Stanford, USA

- Researching fully digital ADC-based high-speed link equalization techniques under Professor Mark Horowitz.

### • Berkeley Wireless Research Center

Undergraduate Researcher

Sep 2019 – Jan 2020

Berkeley, USA

- Designed photonic devices using the Berkeley Photonics Generator (BPG) and digital circuits for high-speed communication in Python and Verilog for an ultrasound receive-array system fabricated in the Global Foundries 45nm RFSOI process.
- Built the lab setup and tested the sensitivity of silicon photonic ring modulators when disturbed with ultrasonic waves.

## PUBLICATIONS

### Refereed Conference and Journal Papers

- [1] **Olivia Hsu**, Alexander Rucker, Tian Zhao, Kunle Olukotun, and Fredrik Kjolstad. “Stardust: Compiling Sparse Tensor Algebra to a Reconfigurable Dataflow Architecture”. In: *International Symposium on Code Generation and Optimization (CGO)*. To Appear. 2025.
- [2] Kalhan Koul, Maxwell Strange, Jackson Melchert, Alex Carsello, Yuchen Mei, **Olivia Hsu**, Taeyoung Kong, Po-Han Chen, Huifeng Ke, Keyi Zhang, Qiaoyi Liu, Gedeon Nyengele, Akhilesh Balasingam, Jayashree Adivarahan, Ritvik Sharma, Zhouhua Xie, Christopher Torng, Joel Emer, Fredrik Kjolstad, Mark Horowitz, and Priyanka Raina. “Onyx: A Programmable Accelerator for Sparse Tensor Algebra”. In: *2024 IEEE Hot Chips 36 Symposium (HCS)*. Los Alamitos, CA, USA: IEEE Computer Society, Aug. 2024, pp. 1–91. URL: [🔗](#)
- [3] Genghan Zhang, **Olivia Hsu**, and Fredrik Kjolstad. “Compilation of Modular and General Sparse Workspaces”. In: *Proc. ACM Program. Lang.* 8.PLDI (June 2024). URL: [🔗](#)

- [4] Kalhan Koul, Maxwell Strange, Jackson Melchert, Alex Carsello, Yuchen Mei, **Olivia Hsu**, Taeyoung Kong, Po-Han Chen, Huifeng Ke, Keyi Zhang, Qiaoyi Liu, Gedeon Nyengele, Akhilesh Balasingam, Jayashree Adivarahan, Ritvik Sharma, Zhouhua Xie, Christopher Torng, Joel Emer, Fredrik Kjolstad, Mark Horowitz, and Priyanka Raina. “Onyx: A 12nm 756 GOPS/W Coarse-Grained Reconfigurable Array for Accelerating Dense and Sparse Applications”. In: *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. 2024. URL: [↗](#)
- [5] Erik Orm Hellsten, Artur Souza, Johannes Lenfers, Rubens Lacouture, **Olivia Hsu**, Adel Ejeh, Fredrik Kjolstad, Michel Steuwer, Kunle Olukotun, and Luigi Nardi. “BaCO: A Fast and Portable Bayesian Compiler Optimization Framework”. In: *Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 4*. ASPLOS ’23. Vancouver, BC, Canada: Association for Computing Machinery, 2024, pp. 19–42. URL: [↗](#)
- [6] Manya Bansal, **Olivia Hsu**, Kunle Olukotun, and Fredrik Kjolstad. “Mosaic: An Interoperable Compiler for Tensor Algebra”. In: *Symposium on Programming Languages Design and Implementation (PLDI)*. **Distinguished Paper Award**. 2023. URL: [↗](#)
- [7] **Olivia Hsu**, Maxwell Strange, Ritvik Sharma, Jaeyeon Won, Kunle Olukotun, Joel S. Emer, Mark A. Horowitz, and Fredrik Kjolstad. “The Sparse Abstract Machine”. In: *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*. ASPLOS 2023. Vancouver, BC, Canada: Association for Computing Machinery, 2023, pp. 710–726. URL: [↗](#)
- [8] Sumer Kohli, Neelesh Ramachandran, Ana Tudor, Gloria Tumushabe, **Olivia Hsu**, and Gireeja Ranade. “Inclusive Study Group Formation at Scale”. In: *Proceedings of the 54th ACM Technical Symposium on Computer Science Education V. 1*. SIGCSE 2023. Toronto ON, Canada: Association for Computing Machinery, 2023, pp. 11–17. URL: [↗](#)
- [9] Panagiotis Zarkos, Sidney Buchbinder, Christos Adamopoulos, Sarika Madhvapathy, **Olivia Hsu**, Jake Whinnery, Pavan Bhargava, and Vladimir Stojanovic. “Fully Integrated Electronic-Photonic Ultrasound Receiver Array for Endoscopic Applications in a Zero-Change 45-nm CMOS-SOI Process”. In: *IEEE Journal of Solid-State Circuits* 58.6 (2023), pp. 1719–1734. URL: [↗](#)
- [10] Rawn Henry\*, **Olivia Hsu\***, Rohan Yadav, Stephen Chou, Kunle Olukotun, Saman Amarasinghe, and Fredrik Kjolstad. “Compilation of sparse array programming models”. In: *Proceedings of the ACM on Programming Languages (OOPSLA)*. 2021. URL: [↗](#) *Note: \* signifies equal contribution.*
- [11] Panagiotis Zarkos, Sidney Buchbinder, Christos Adamopoulos, Sarika Madhvapathy, **Olivia Hsu**, Jake Whinnery, Pavan Bhargava, and Vladimir Stojanovic. “Fully Integrated Electronic-Photonic Ultrasound Receiver Array for Endoscopic Imaging Applications in a Zero-Change 45nm CMOS-SOI Process”. In: *2021 Symposium on VLSI Circuits*. 2021, pp. 1–2. URL: [↗](#)
- [12] Panagiotis Zarkos, Sidney Buchbinder, Christos Adamopoulos, **Olivia Hsu**, Sarika Madhvapathy, Jake Whinnery, Pavan Bhargava, and Vladimir Stojanovic. “Monolithically Integrated Electronic-Photonic Ultrasound Receiver Using Microring Resonator”. In: *2021 Conference on Lasers and Electro-Optics (CLEO)*. 2021, pp. 1–2.
- [13] Panagiotis Zarkos, **Olivia Hsu**, and Vladimir Stojanovic. “Ring Resonator Based Ultrasound Detection in a Zero-Change Advanced CMOS-SOI Process”. In: *2019 Conference on Lasers and Electro-Optics (CLEO)*. 2019, pp. 1–2. URL: [↗](#)

## Refereed Workshop Papers

- [14] Rubens Lacouture, **Olivia Hsu**, Kunle Olukotun, and Fredrik Kjolstad. *Challenges with Hardware-Software Co-design for Sparse Machine Learning on Streaming Dataflow*. Workshop on Programming Languages and Architecture (PLARCH) co-located with FCRC/ISCA/PLDI. 2023.
- [15] **Olivia Hsu**, Maxwell Strange, Kunle Olukotun, Mark Horowitz, and Fredrik Kjolstad. *Designing a Dataflow Hardware Accelerator with an Abstract Machine*. Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE) co-located with ASPLOS. 2023.

## Under Review and In Progress

- [16] Rubens Lacouture, **Olivia Hsu**, Nathan Zhang, Ritvik Sharma, Fredrik Kjolstad, and Kunle Olukotun. *FuseFlow: A Fusion-Centric Compilation Framework for Sparse Deep Learning on Streaming Dataflow*. Under Review. 2024.

- [17] Marco Siracusa, **Olivia Hsu**, Victor Soria-Pardos, Joshua Randall, Arnaud Grasset, Eric Biscondi, Doug Joseph, Fredrik Kjolstad, Miquel Moretó Planas, and Adrià Armejach. *Ember: A Compiler for Embedding Operations on Decoupled Access-Execute Architectures*. Under Review. 2024.
- [18] Kalhan Koul\*, **Olivia Hsu\***, et al. *Onyx: A 12nm 756 GOPS/W Coarse-Grained Reconfigurable Array for Accelerating Dense and Sparse Applications*. In Progress. 2024. Journal. Note: \* signifies equal contribution.
- [19] Sho Ko, Nathan Zhang, **Olivia Hsu**, Ardavan Pedram, and Kunle Olukotun. *DFModel: Design Space Optimization of Large-Scale Systems Exploiting Dataflow Mappings*. In Progress. 2024.

## TEACHING EXPERIENCE

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- **Stanford Agile Hardware Design (AHA) Tutorial at MICRO 2024** Nov 2024  
*Presenter* Austin, USA
  - Teaching the sparse application flow for the Stanford AHA project, which includes the front-end sparse Custard compiler [7, 18], the sparse abstract machine (SAM) dataflow intermediate representation [7], and sparse optimizations for the Onyx coarse-grained reconfigurable array (CGRA) [2, 4, 18].
- **Stanford University CS 143: Compilers** Spring 2023, Spring 2024  
*Course Assistant* Stanford, USA
  - Taught under professor Fredrik Kjolstad.
  - Duties include running office hours, managing course logistics, developing written assignments, debugging exams, writing exam problems, and homework and exam grading.
- **Stanford University CS149: Parallel Programming** Fall 2021  
*Course Assistant* Stanford, USA
  - Taught under professors Kayvon Fatahalian and Kunle Olukotun.
  - Duties included running office hours, debugging exams, and exam and homework grading.
- **UC Berkeley Decal EE 198: Hands-on PCB Engineering (HOPE)** Fall 2018  
*Student Instructor* Berkeley, USA
  - Co-created and developed the curriculum for the first-ever offering of this course, an undergraduate-led class on printed circuit board design affiliated with the UC Berkeley IEEE student chapter.
  - Taught the course to approximately 30 students, teaching these students how to read design documentation, design circuits, use PCB design tools, package design files for PCB fabrication, and populate and test their own PCB designs.
- **UC Berkeley EECS 16A: Designing Information Devices and Systems I** Fall 2016 – Fall 2017  
*Undergraduate Student Instructor (UGSI)* Berkeley, USA
  - Administrative and Lab UGSI (Fall 2016) and Head and Lab UGSI (Spring – Fall 2017) for the introductory electrical engineering course. The largest offering I taught had 850+ students, and I was in charge of 30+ teaching assistants.
  - Duties included managing course administration and policies, responding to all student emails related to the course, teaching and debugging labs, creating exam problems, running office hours, grading exams, and hiring course readers and other teaching assistants.

## MENTORING

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- **Varun Desai** Jan 2024 – Present  
*Stanford University M.S. expected 2025*
  - Varun is currently looking into strategies for estimating the number of operations of a sparse workload given unknown input data.
  - Varun also helped on the GPU evaluation of the Stardust compiler [1].
- **Sai Gautham Ravipati** Jan 2024 – Present  
*Stanford University M.S. expected 2025*
  - Gautham is looking into compilation techniques for automatically generating tilings across memory hierarchies that target host-accelerator systems. We have already deployed this compilation flow to automatically generate tilings for testing the Onyx CGRA in [18].
- **Genghan Zhang** Feb 2022 – Jun 2024  
*Tsinghua University B.S. 2023, now Stanford Ph.D. expected 2029*
  - Genghan designed a compiler for optimized sparse tensor operations that detects the need for and inserts sparse temporary tensors (intermediate workspaces). This work achieved up to a 27x speedup and improved memory efficiency over dense temporary tensors while maintaining adaptability across various tensor expressions and user-defined implementations. This undergraduate research led to a publication at PLDI 2024 [3].
- **Manya Bansal** Feb 2022 – July 2023  
*Stanford University B.S. 2023, now MIT Ph.D. expected 2029 University*

- Manya developed Mosaic, an extensible compiler enabling flexible integration of external, high-performance libraries for tensor algebra, achieving up to a  $206\times$  speedup by combining custom calls with efficient fused code generation. This undergraduate research led to a publication at PLDI 2023 and a distinguished paper award [6].
- **Rubens Lacouture** Sep 2021 – Present  
Stanford University Ph.D. expected 2027
  - Rubens is currently looking into the compilation of sparse machine learning applications to dataflow backends, particularly focusing on extending ideas from the sparse abstract machine [7] to encompass machine learning operations [14] and the automatic fusion of distinct expressions to generated fused dataflow graphs [16].
- **Zhouhua Xie** Jun 2023 – Present  
Stanford University B.S. and M.S. expected 2025
  - Zhouhua is now looking into an FPGA emulation platform for the Onyx CGRA [4, 2].
  - Zhouhua investigated the performance bottlenecks and bugs in the sparse applications running on the Onyx CGRA [2, 4] and updated RTL implementations of the sparse primitives to fix those performance bottlenecks.
- **Parthiv Krishna** Sep 2022 – May 2024  
Stanford University B.S. 2023, Stanford University M.S. expected 2024
  - Parthiv looked into implementing the sparse abstract machine primitives from [4, 2] on an FPGA.
- **Jayashree Adivarahan** Jun 2023 – Sep 2024  
Arizona State University B.S. expected 2025
  - Jayashree helped with the evaluation of the Onyx CGRA [4, 2], specifically developing scripts that process and tile input tensor data before sending that data to the CGRA chip.
  - Jayashree looked into implementing the sparse abstract machine primitives from [4, 2] on an FPGA.
- **Akhilesh Balasingam** Jun 2023 – Feb 2024  
Stanford University B.S. expected 2025
  - Akhilesh helped with the evaluation of the Onyx CGRA [4, 2], specifically running timing measurements on the physical CGRA and developing scripts that process and tile input tensor data.
- **Gloria Tumushabe** Sep 2016 – Mar 2023  
UC Berkeley B.S. 2020, UC Berkeley M.S. 2021, Now Salesforce Senior Software Engineer
  - Gloria implemented techniques that help students form optional study groups in large-scale EECS courses at UC Berkeley that take into account inclusivity, which led to the Master’s thesis “[Inclusive and Scalable Study Group Formation](#)” and a publication at SIGCSE TS 2023 [8].

## HONORS AND AWARDS

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|---|---|
| • <b>Rising Stars in EECS Awardee</b><br>MIT  | 2024<br><a href="#">[🔗]</a>   |
| • <b>NextProf Nexus Future Faculty Awardee</b><br>University of Michigan, University of California Berkeley, and Georgia Tech | 2024  |
| • <b>Distinguished Paper Award for Mosaic [6]</b><br>PLDI   | 2023<br><a href="#">[🔗]</a>   |
| • <b>Alton B. Zerby and Carol T. Koerner Outstanding Student Award</b><br>IEEE–Eta Kappa Nu (HKN)                             | 2019<br><a href="#">[📺]</a> <a href="#">[🔗]</a> <a href="#">[🔗]</a> |
| • <b>Graduate Research Fellowship (GRFP)</b><br>National Science Foundation (NSF)   | 2019  |
| • <b>Arthur M. Hopkin Award</b><br>University of California, Berkeley EECS Department   | 2018–2019<br><a href="#">[🔗]</a>                                    |
| • <b>Outstanding Graduate Student Instructor (OGSI) Award</b><br>University of California, Berkeley                           | 2017–2018<br><a href="#">[🔗]</a>                                    |
| • <b>National Electrical Engineering Honor Society Member and Officer</b><br>IEEE–Eta Kappa Nu (HKN)                          | 2016  |
| • <b>National Engineering Honor Society Member and Officer</b><br>Tau Beta Pi (TBP)   | 2016  |
| • <b>Leadership Award</b><br>Cal Alumni Association   | 2015–2016<br><a href="#">[🔗]</a>                                    |

## WORK EXPERIENCE

- **Samsung Semiconductor** Jun 2023 - Sep 2023  
Hardware Architecture Intern San Jose, USA
  - Researching the programmability and characterization of sparse workloads on next-generation supercomputing systems.
- **Ayar Labs** Jun 2020 - Sep 2020  
Hardware VLSI Intern Santa Clara, USA
  - In charge of updating the design of multiple digital circuit blocks in System Verilog to match provided specifications, digital verification of those blocks, and pushing those blocks through the physical design process until they were met timing and were DRC and LVS clean.
- **Apple** Jun 2019 - Sep 2019, May 2018 – Aug 2018  
CPU Design Verification Intern Cupertino, USA
  - Created instruction set architecture pseudocode for the Apple CPU in 2019.
  - Developed a runtime co-simulation checker using and added debug features into a C++ functional model of the Apple CPU in 2018.
- **NASA Jet Propulsion Laboratory (JPL)** Jun 2016 - Aug 2016  
Hardware Research Intern Pasadena, USA
  - Developed a sensor testbed that verified the communication systems on a radiation-hardened, deep-space CubeSat avionics board.

## TALKS

- **Mapping Sparse Applications to Accelerated Computing Systems** [📺]  
PLDI 2024: Sparse Workshop June 2024  
Carnegie Mellon University (CMU) Systems Design and Implementation (SDI) Seminar April 2024
- **The Sparse Abstract Machine** April 2024  
Stanford and U-Tokyo Workshop: Agile and low-cost HW design workshop for domain-specific computing era
- **Architectural and compiler support for accelerating embedding operations on general purpose processors** February 2024  
MIT Computer Science and Artificial Intelligence Laboratory (CSAIL)
- **Beyond the Sparse Abstract Machine: Mapping sparse applications to accelerated computing systems** December 2023  
UC Santa Barbara Computer Science Department Colloquium
- **The Sparse Abstract Machine** June 2023  
PLDI 2023: Compilation Techniques for Sparse Tensor Algebra (CTSTA)
- **Sparse Abstract Machine and Dataflow Hardware** November 2022  
NVIDIA Tutorial on Sparse Tensor Algebra Compilation
- **The Sparse Abstract Machine: Sparse Tensor Algebra as Dataflow Graphs** October 2022  
University of Washington: SAMPL Lunch Talk  
Samsung Semiconductor System Architecture Lab (SAL) September 2022  
AHA Agile Hardware Project Retreat August 2022
- **Compilation of Sparse Array Programming Models** April 2022  
Google Brain: ML compilation seminar  
University of California, Santa Cruz: LSD Seminar April 2022

## SERVICE

- **LATTE Program Committee** 2024
- **SIGGRAPH External Reviewer** 2024
- **Engineering Students for Diversity, Equity, and Inclusion (ES4DEI) College Track Co-Lead** 2023 – 2024
- **Stanford University CS Department PhD Admissions Committee** 2023
- **Stanford CS Department Student-Applicant Support Program Volunteer** 2020 – 2021
- **AfroFemCoders Advisor, Co-founder, and Instructor** 2020 – 2021
- **UC Berkeley EECS Department Inaugural Women's History Month** 2019

## REFERENCES

**Kunle Olukotun**  
Professor in Electrical Engineering and Computer Science  
Stanford University  
[kunle@stanford.edu](mailto:kunle@stanford.edu)  
Relationship: Primary Thesis Advisor

**Fredrik Kjolstad**  
Assistant Professor in Computer Science  
Stanford University  
[kjolstad@stanford.edu](mailto:kjolstad@stanford.edu)  
Relationship: Thesis Co-advisor

**Joel Emer**  
Professor of the Practice in Electrical Engineering and Computer Science, Researcher  
MIT, NVIDIA  
[emer@csail.mit.edu](mailto:emer@csail.mit.edu)  
Relationship: Thesis Committee Member and Research Mentor

**Mark Horowitz**  
Professor in Electrical Engineering and Computer Science  
Stanford University  
[horowitz@ee.stanford.edu](mailto:horowitz@ee.stanford.edu)  
Relationship: Research Mentor