Lab 7: Carry-Ripple Addition II

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ECE 429-01

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1 Introduction

The purpose of this lab is to continue the design process of the carry-ripple adder from lab 6. Specifically, the layout of the carry-ripple adder will be designed and implemented. It will then be verified using Design Rule Checking (DRC) and Layout v.s. Schematic Verification (LVS).

2 Theory/Pre-Lab

2.1 Theory

When designing the layout of a large or complex circuit, it is incredibly important to be meticulous so that too many design rules are not violated when the layout is complete. Many errors in the layout design will result in an extremely difficult process of correction. Using the reference design shown in Figure 1 as a design rule guideline, the stick diagram can easily be built with minimal errors. Figures 3 - 7 show the stick diagrams for the full adder.

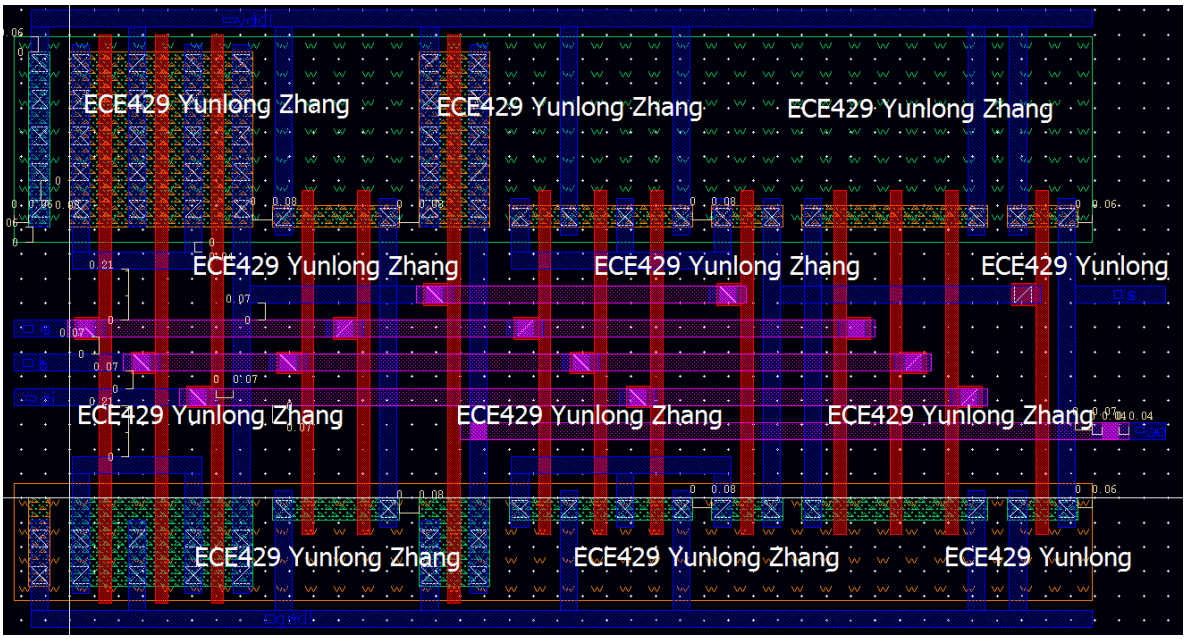


Figure 1: Reference Mirror Adder Layout

2.2 Pre-Lab

Due to the size of the layout of this circuit, the sketch of the stick diagram was separated into the individual parts of the schematic. This was done to accurately show the connections involved in this circuit due to the fact that layers of metal cannot be easily drawn using pen and paper. The original schematic is shown in Figure 2.

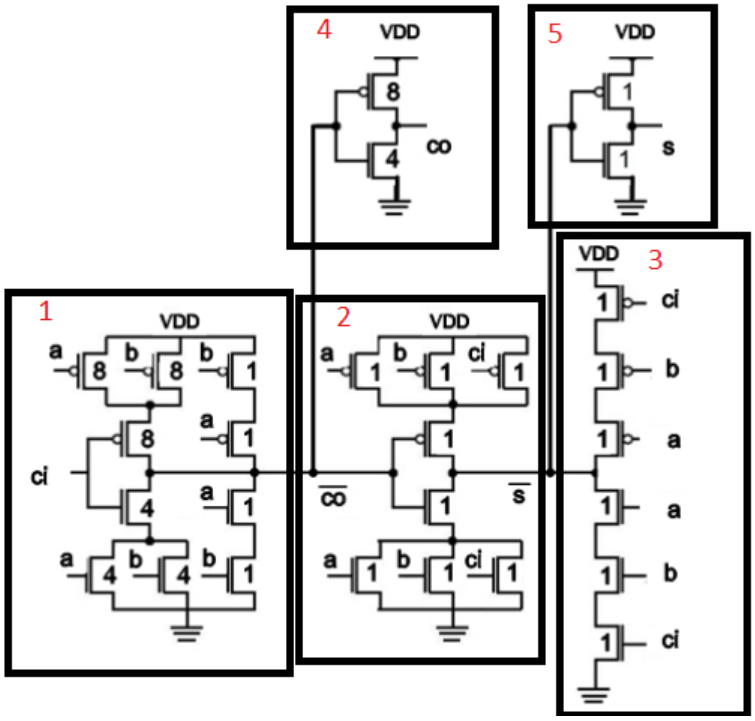


Figure 2: Mirror Adder Schematic

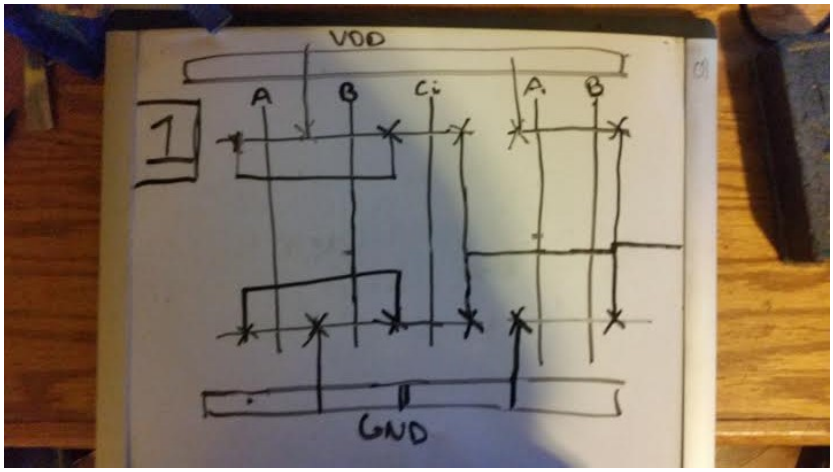


Figure 3: Section 1

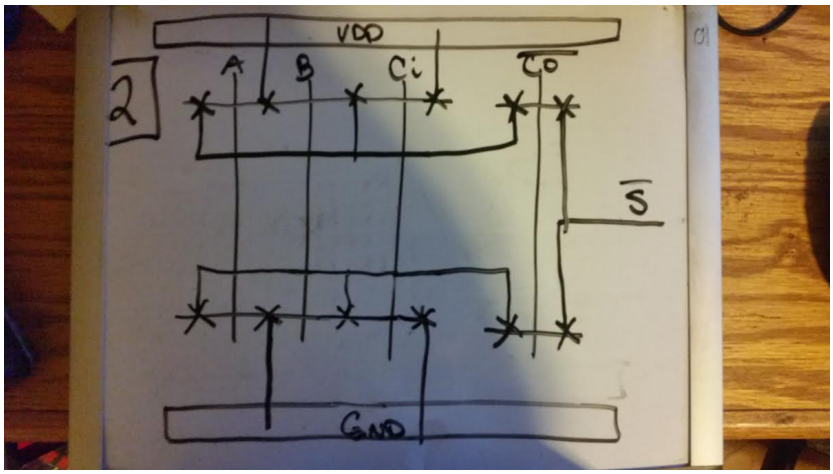


Figure 4: Section 2

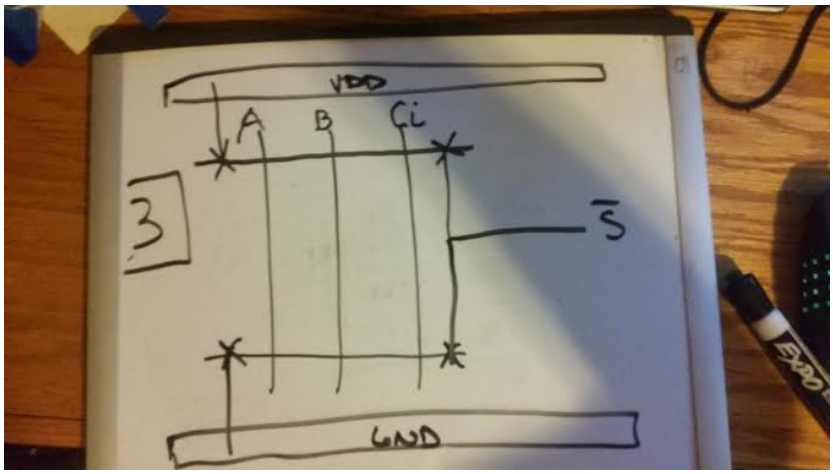


Figure 5: Section 3

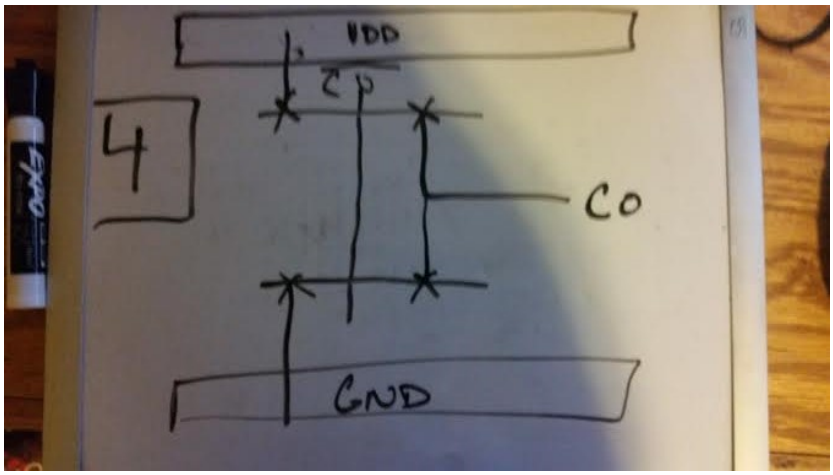


Figure 6: Section 4

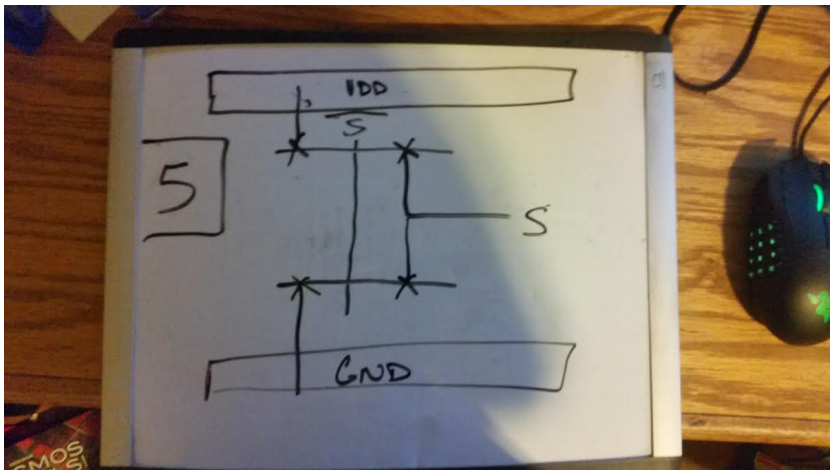
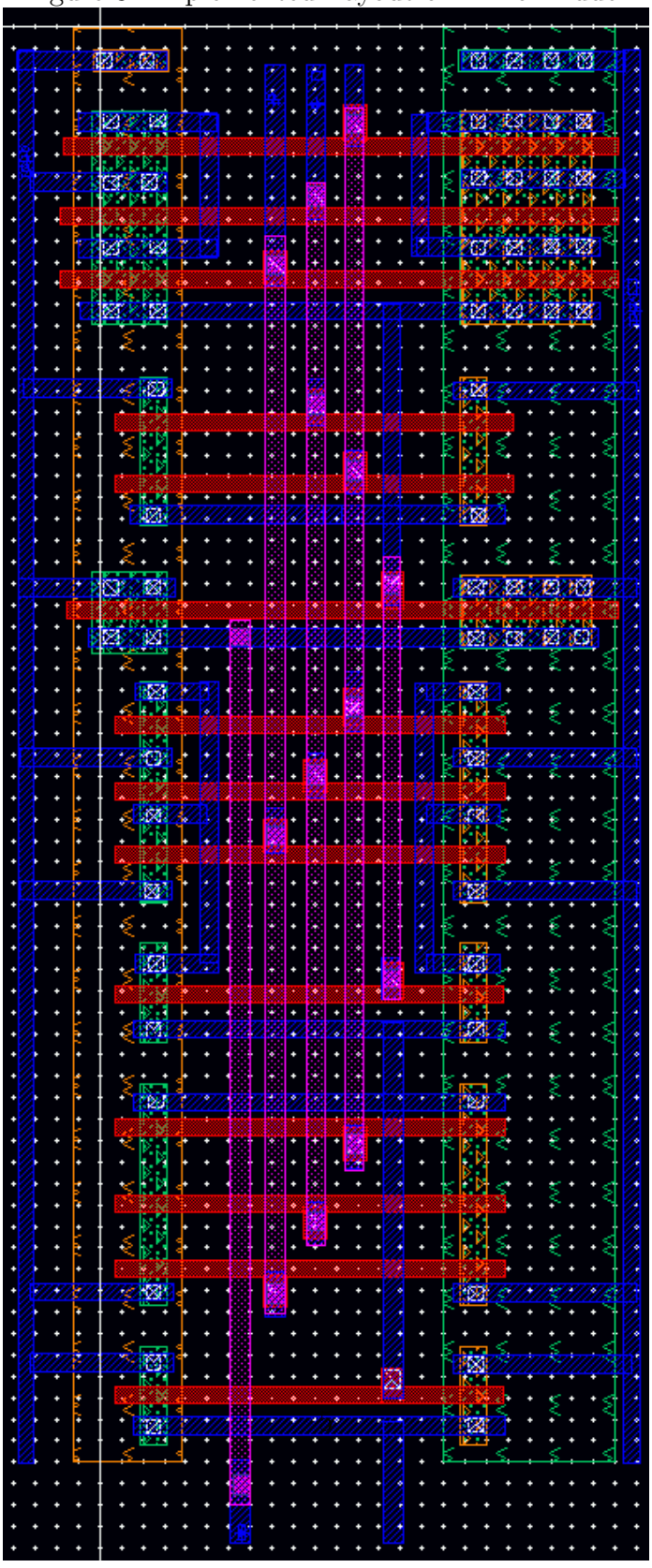


Figure 7: Section 5

3 Implementation

3.1 Schematics

Figure 8: Implemented Layout of Mirror Adder



3.2 Procedure

First the layout of the full adder was constructed. After several hours of hard meticulous work and constant DRC to make sure the design followed the guidelines, LVS was performed and any errors were corrected until the smiley face was generated.

3.3 Results

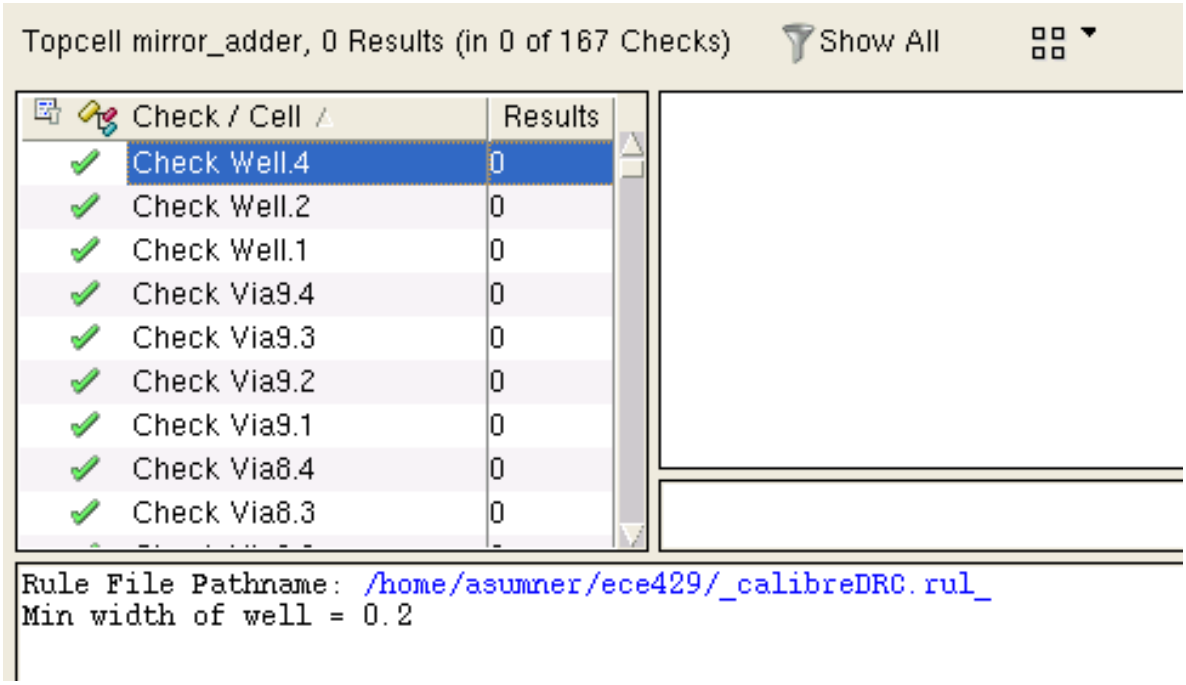


Figure 9: DRC Verification

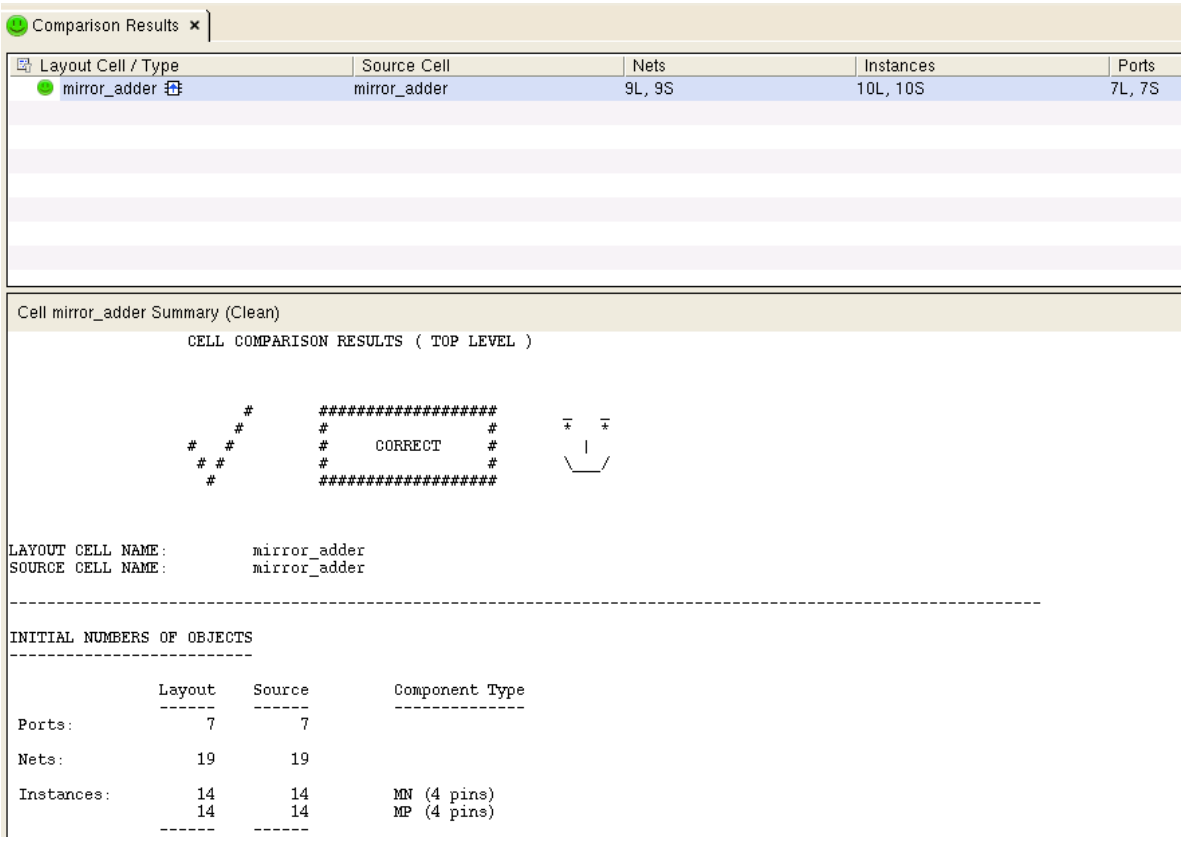


Figure 10: LVS Verification

3.4 Discussion

While this lab did not seem to have a long procedure, the physical construction of the layout to minimize the size of the design took several hours (5+). Upon construction and verification of the design, it was noted that the focus needed to be a competent VLSI design engineer is quite intense. Luckily, the hard work paid off as Figures 9 and 10 demonstrate the successful work completed in this lab. In order to succeed in layout design, constant DRC must be utilized. It's incredibly easy to misplace an object by 1 nm, which in turn can lead to a lot of DRC errors later on if not caught early. The key to layout design is patience, great planning skills, and an appetite for paying attention to close detail.

4 Conclusions

Overall this lab was a success. The layout of the mirror adder was completed and its functionality was successfully verified. It may now be used in future designs, such as constructing a 4-bit adder.