Lab 9: Standard Cell Based ASIC Design Flow

Adam Sumner

Illinois Institute of Technology

ECE 429-01

Lab Date: November 9th, 2015 **Due Date:** November 16th, 2015

1 Introduction

2 Theory/Pre-Lab

2.1 Theory

Standard cell based ASIC design flow automatically synthesizes a chip layout from a register transfer level (RTL) description of a chip. The design flow utilizes the standard cell library to synthesize a chip layout according to design constraints including cost, performance, power consumption, etc. While this may seem like a nice tool to completely replace manual chip design, in practice, the tool will seldom generate a satisfactory design in the beginning. It is necessary for chip designers to understand the various steps of the design flow to guide the tool through multiple iterations before an optimum solution is found. In general, the standard cell based ASIC design flow consists of two steps: Logic Synthesis and Physical Design.

2.1.1 Standard Cell Library

A standard cell is a logic gate with a lay

2.2 Pre-Lab

3 Implementation

3.1 Schematics

3.2 Procedure

3.3 Results

3.4 Discussion

4 Conclusions