

## EXPERIMENT #6

### Input / Output Design

#### 1.0 Purpose

The purpose of this experiment is to introduce the user to the concepts of memory mapped I/O and interrupts.

#### 2.0 Component Requirements

Quantity:	Description: (Mfr.; Mfr. Part No.)
2	Octal Latch; Motorola; SN74LS373N
2	7-Segment Display Driver; Motorola; SN74LS48N
2	7-Segment Display; G.I. Opto; MAN74
1	DIP Switch, SPST, 8 position; Grayhill; 76RSB08
8	Resistors, 1K ohm, 1/4 W, 5%
TBD	Misc. TTL Logic Gates (AND, OR, inverters, buffers, decoders, etc.)

#### 3.0 Background

##### A. Memory-Mapped Input / Output (I/O)

There are two different types of philosophies when it comes to interfacing to I/O devices. These are known as “Memory Mapped” I/O and “Isolated” I/O. The MC68000 uses the memory-mapped I/O philosophy. This implies that all I/O devices are accessed by reading and writing to memory locations within the microprocessor’s address space.

The discussion provided in Experiment #5 concerning the timing relationships of asynchronous bus cycles is also relevant to I/O design.

##### B. Interrupts

The MC68000 microprocessor is equipped with 3 interrupt request signals (\*IPL2, \*IPL1, \*IPL0) which provide a maximum of 7 distinct interrupt levels, and a normal operating level (level 0). The Status Register contains three Interrupt Mask Bits (I2, I1, I0) which are the logical complement of the interrupt hardware signals. The following chart illustrates the relationship between the interrupt request signals and the interrupt mask bits.

Interrupt Request Signals			Interrupt Mask Bits			Requested Interrupt Level
*IPL2	*IPL1	*IPL0	I2	I1	I0	
0	0	0	1	1	1	7 (highest priority)
0	0	1	1	1	0	6
0	1	0	1	0	1	5
0	1	1	1	0	0	4
1	0	0	0	1	1	3
1	0	1	0	1	0	2
1	1	0	0	0	1	1 (lowest priority)
1	1	1	0	0	0	0 (none)

When dealing with interrupts, the device requesting service activates a hardware signal called an Interrupt Request line. (\*IRQ). The interrupt request lines from several peripheral devices are prioritized, encoded and inputted to the three interrupt request lines of the MC68000. The interrupt requests are made pending until the CPU completes the current instruction being executed. Once the instruction is completed, the current state of the processor is saved on the stack, and an interrupt acknowledge cycle begins.

The MC68000 compares the incoming interrupt request to the current interrupt priority level stored in the Status Register's Interrupt Mask Bits. If the incoming level is less than or equal to the current interrupt priority level, then the interrupt is not serviced.

The following is a list of the interrupt level settings for the SANPER-1 Educational Lab Unit.

<u>Interrupt Level</u>	<u>Interrupting Device</u>	<u>Vector No. (Decimal)</u>
7	ABORT Switch	31
6	ACIA2 (Host Port)	30
5	ACIA1 (Terminal Port)	29
4	ACIA3, Speech, PIA devices	28
3	PI/T Parallel Ports (*PIRQ)	U.V.
2	PI/T Timer (*TOUT)	U.V.
1	System Expansion Board	A.V. or U.V.
0	Normal CPU Operation (No interrupt pending)	Not Used

Where: U.V. = User-vectored interrupt  
A.V. = Auto-vectored interrupt

Interrupt Level 1 (\*IRQ1) is made accessible to the user through the System Expansion Board. This interrupt level may be either Auto-Vectored or User-Vectored depending upon the jumper configurations on the SANPER-1 System

Board. The user may assume that the SANPER-1 ELUs have been configured for Auto-Vectored Interrupts on Interrupt Level 1.

#### 4.0 Statement of Problem

In this experiment the student will design and implement the hardware and software to read data from a DIP switch, pass this data to a software counter, and display the counter's outputs on two 7-Segment Displays.

#### 5.0 Preliminary Assignment

1. Design and draw a detailed schematic diagram of the hardware required to perform the input function of reading data from a DIP Switch, and the output function of writing data to two 7-Segment displays.

Your schematic diagram should include the following devices and circuitry:

- the address decoder logic
- the \*DTACK signal generator logic
- the I/O latches
- the DIP Switch
- the pull-up resistors
- the 7-Segment Display Drivers
- the 7-Segment Displays

The MC68000 inputs or reads data from the 8-position DIP switch through one of the latches. The resistors perform a pull-up function for the latch inputs. The MC68000 outputs or writes data to the 7-Segment drivers and displays through the other latch.

The input and output latches must reside within the 64K address range of \$060000 to \$06FFFF. Both latches must use the same even address. Not all of this address range is available however. The following addresses are reserved for other hypothetical devices in the system.

Device 1: \$060000 - \$0607FF

Device 2: \$063000 - \$065FFF

Device 3: \$068000 - \$0680FF

Device 4: \$06B000 - \$06B00F

Device 5: \$06D000 - \$06DFFF

The latches may be placed in any non-occupied address location. The user must decode around the existing devices, so that no other device is unintentionally selected. The user must initially use full address decoding to enter within the 64K address space at \$060000. The user may then employ partial decoding and use a minimal number of address lines to select the latches.

**HINT:** Use one of the SANPER-1 ELU's Block Select lines as part of your address decoding implementation.

Additionally, the user must design circuitry to generate a \*DTACK signal to the MC68000 whenever the latches are accessed. The user must determine if any wait states need to be inserted based upon the propagation delay through the address decoding logic and the latches.

2. Using your schematic diagram and parts kit, build your I/O circuit on a breadboard strip. If a DIP switch is not available, simulate it by tying the latch inputs either to +5V DC or ground.
3. Write an interrupt service routine that performs an input function of reading data from a DIP switch, and performs an output function of writing data to two 7-Segment displays.

The MC68000 reads and writes data to the latches in Binary Coded Decimal (BCD) format. The range of a BCD number is 0 to 9.

The routine should read the value set on an 8-position DIP switch every time the ABORT Switch is depressed. The 8-bit value should be read in as two BCD numbers, with the four least significant bits comprising the least significant BCD digit, and the four most significant bits comprising the most significant BCD digit. Once the value is read in, it should immediately be displayed on the 7-segment displays. This value is then passed to a two-digit BCD counter. The counter begins counting at the value read from the DIP switch, and increments one count at a time at a minimum rate of one count per second. The current counter value is always displayed in BCD notation on the two 7-Segment displays. The counter will count up to a maximum value of 99, and then this interrupt service routine should exit and return back to TUTOR.

**Note:** Due to the fact that the numbers are BCD, the counter must be implemented with the MC68000's BCD instructions. An example of such an instruction is "ABCD" or "Add Decimal with Extend".

## 6.0 Procedure

1. Connect your hardware up to the SANPER-1 Educational Lab Unit.
2. Use TUTOR's Memory Modify (MM) Command to write data to the 7-Segment displays. If the displays do not show the proper value, debug your hardware.

**Debugging Hint:** Create a small test program to repeatedly write data to the 7-Segment displays. Run the program and then enter the SANPER-1's Hardware Single-Step Mode. Continually single step through the test program until the problem is identified and fixed.

3. Set the appropriate exception vector to point to the interrupt service routine from Prelim #3. Each time the user presses the ABORT Switch, the routine from Prelim #3 will begin executing.
4. Set the DIP switch to a BCD value of 25.
5. Run the program and verify that your hardware and software are working correctly. Test your design thoroughly by entering several values at the DIP switch, and verifying that the counter begins and ends counting at the proper values.

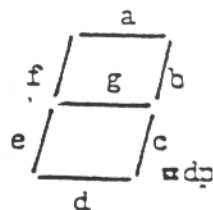
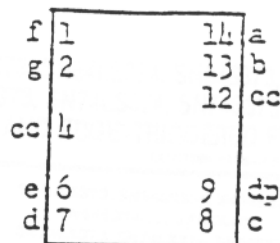
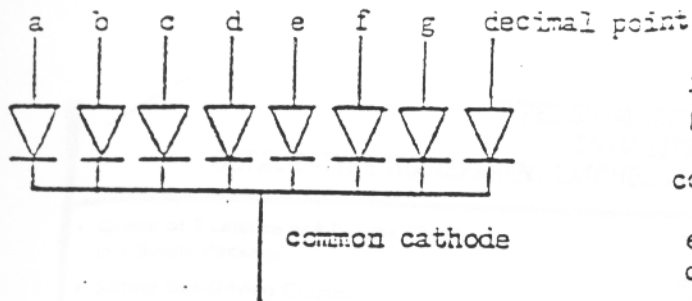
For each BCD digit, the only valid DIP switch values are in the range of 0000 to 1001.

6. Demonstrate to your Lab Instructor that your program is operating correctly.

## 7.0 Discussion

Submit the following to your Lab Instructor as a Final Report:

1. A commented listing for the programs of Prelim #3.
2. A schematic diagram of your hardware design for Prelim #1.
3. Review Chapter 7, “Hardware Description” of the Motorola Educational Computer Board User’s Manual. Also, review Chapter 8 and examine Figure 8-3, Sheet 2 of 3 of the MC68000 Educational Computer Board Schematic Diagram, and redraw only the ABORT switch circuitry. Describe in detail how this ABORT Switch circuitry operates.
4. The Exception Vector Table has vectors assigned for Uninitialized Interrupts and Spurious Interrupts. Discuss how each of these types of interrupts occurs. Discuss the significance and applications of each of these types of interrupts.
5. Discuss the differences between Auto Vectored and User Vectored interrupts. For how many of each type does the MC68000 allow?
6. Discuss the events that occur during an Interrupt Acknowledge (IACK) Bus Cycle.



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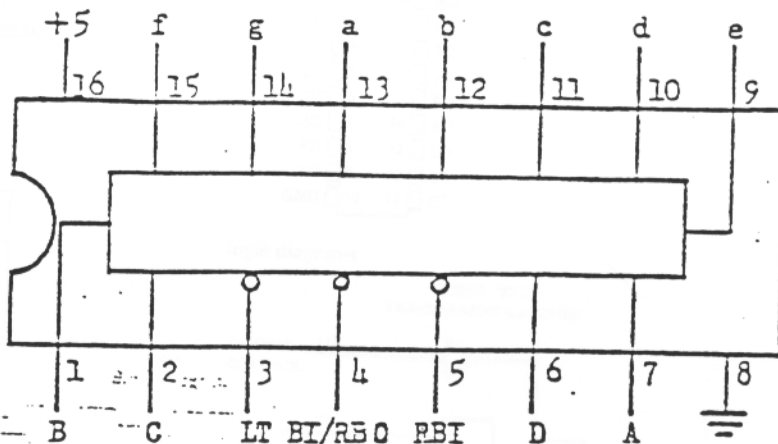
## BCD/7-Segment Decoders/Drivers

BI Blanking Input

REO Ripple Blanking Output

RBI Ripple Blanking Input

LT Lamp Test



NOTE: Any output can be directly connected to an LED since a dropping resistor is included in the output circuit.

Truth Table

HEXADECIMAL OR FUNCTION	INPUTS						BI/REO	OUTPUTS						
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H
3	H	X	L	L	H	H	H	H	H	H	L	L	L	H
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H
5	H	X	L	H	L	L	H	H	L	H	H	L	H	H
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H
A	H	X	H	L	H	L	H	L	L	L	H	H	L	H
B	H	X	H	L	H	H	H	L	L	H	H	L	L	H
C	H	X	H	H	L	L	H	L	H	L	L	L	H	H
D	H	X	H	H	L	H	H	H	L	L	H	L	H	H
E	H	X	H	H	H	L	H	L	L	L	H	H	H	H
F	H	X	H	H	H	H	H	L	L	L	L	L	L	L
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H



# OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

## PIN NAMES

D <sub>0</sub> –D <sub>7</sub>	Data Inputs
LE	Latch Enable (Active HIGH) Input
CP	Clock (Active HIGH going edge) Input
OE	Output Enable (Active LOW) Input
O <sub>0</sub> –O <sub>7</sub>	Outputs (Note b)

## LOADING (Note a)

	HIGH	LOW
D <sub>0</sub> –D <sub>7</sub>	0.5 U.L.	0.25 U.L.
LE	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
OE	0.5 U.L.	0.25 U.L.
O <sub>0</sub> –O <sub>7</sub>	65 (25) U.L.	15 (7.5) U.L.

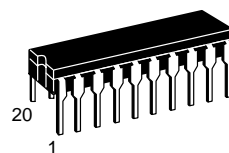
## NOTES:

- a) 1 TTL Units Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

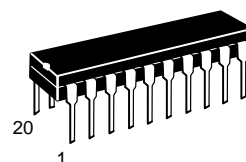
**SN54/74LS373**  
**SN54/74LS374**

**OCTAL TRANSPARENT LATCH  
WITH 3-STATE OUTPUTS;  
OCTAL D-TYPE FLIP-FLOP  
WITH 3-STATE OUTPUT**

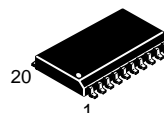
**LOW POWER SCHOTTKY**



**J SUFFIX**  
CERAMIC  
CASE 732-03



**N SUFFIX**  
PLASTIC  
CASE 738-03



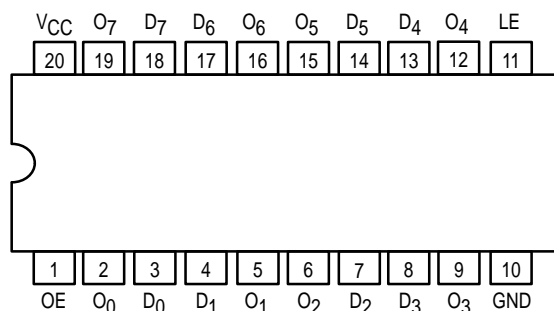
**DW SUFFIX**  
SOIC  
CASE 751D-03

## ORDERING INFORMATION

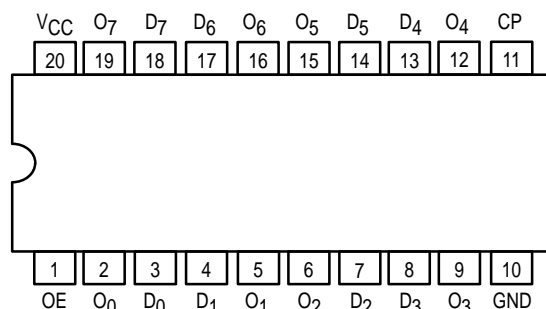
SN54LSXXXJ Ceramic  
SN74LSXXXN Plastic  
SN74LSXXXDW SOIC

## CONNECTION DIAGRAM DIP (TOP VIEW)

### SN54/74LS373



### SN54/74LS374





NOTE:  
The Flatpak version  
has the same pinouts  
(Connection Diagram) as  
the Dual In-Line Package.

SN54/74LS373 • SN54/74LS374

TRUTH TABLE

LS373			
D <sub>n</sub>	LE	OE	O <sub>n</sub>
H	H	L	H
L	H	L	L
X	L	L	Q <sub>0</sub>
X	X	H	Z*

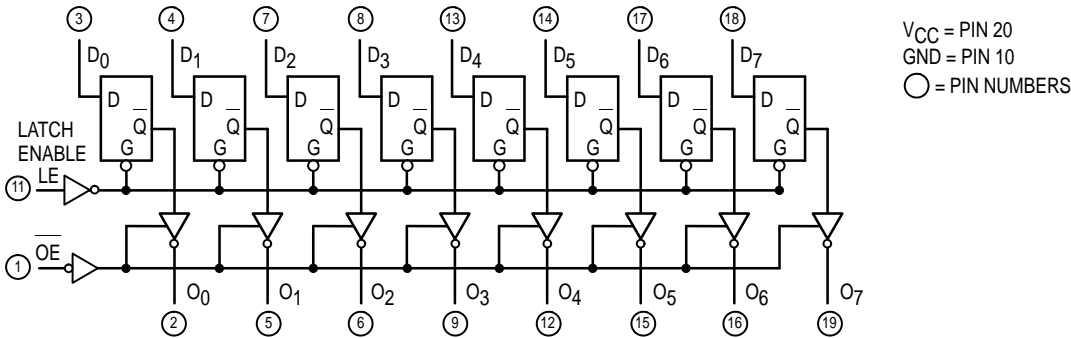
LS374			
D <sub>n</sub>	LE	OE	O <sub>n</sub>
H		L	H
L		L	L
X	X	H	Z*

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

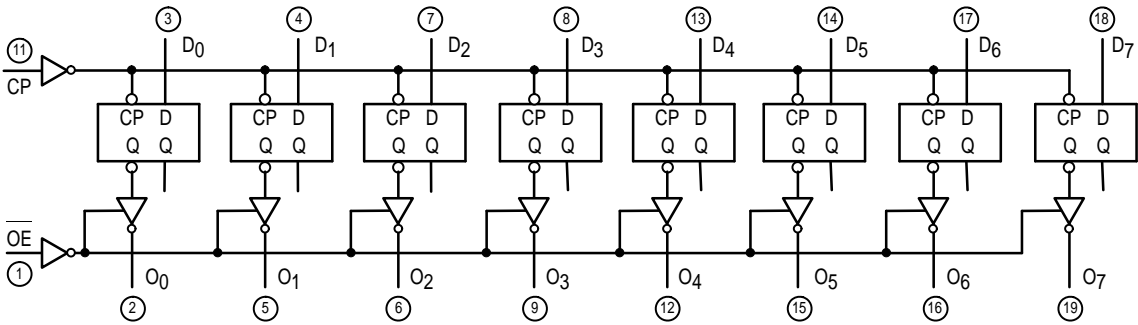
\* Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE).

LOGIC DIAGRAMS

SN54LS/74LS373



SN54LS/74LS374



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54 74			-1.0 -2.6	mA
I <sub>OL</sub>	Output Current — Low	54 74			12 24	mA



# SN54/74LS373 • SN54/74LS374

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage			−0.65	−1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = −18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.4	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.4	3.1		V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 12 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	I <sub>OL</sub> = 24 mA	
I <sub>OZH</sub>	Output Off Current HIGH				20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V	
I <sub>OZL</sub>	Output Off Current LOW				−20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V	
I <sub>IH</sub>	Input HIGH Current				20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
					0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current				−0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)		−30		−130	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current				40	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
fMAX	Maximum Clock Frequency				35	50		MHz	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
tPLH tPHL	Propagation Delay, Data to Output		12 12	18 18				ns	
tPLH tPHL	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
tPZH tPZL	Output Enable Time		15 25	28 36		20 21	28 28	ns	
tPHZ tPLZ	Output Disable Time		12 15	20 25		12 15	20 25	ns	C <sub>L</sub> = 5.0 pF

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
t <sub>W</sub>	Clock Pulse Width	15		15		ns
t <sub>S</sub>	Setup Time	5.0		20		ns
t <sub>h</sub>	Hold Time	20		0		ns

## DEFINITION OF TERMS

**SETUP TIME (t<sub>S</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>H</sub>)** — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

SN54/74LS373

AC WAVEFORMS

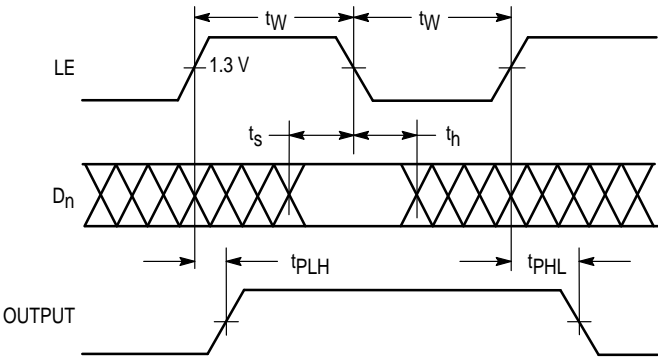


Figure 1

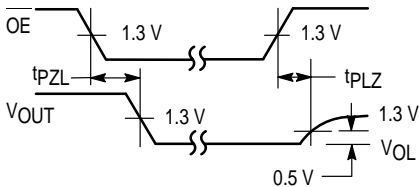


Figure 2

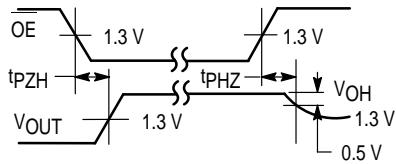
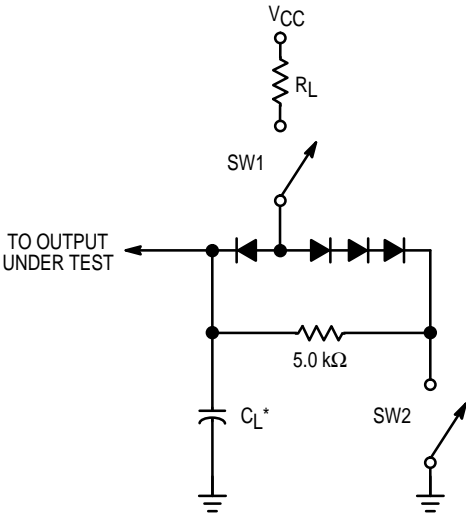


Figure 3

AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed

Figure 4

SN54/74LS374

AC WAVEFORMS

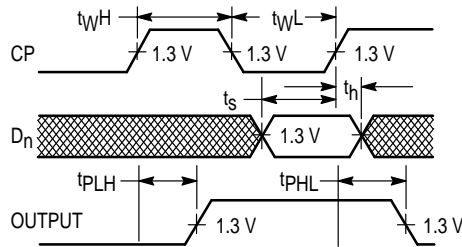


Figure 5

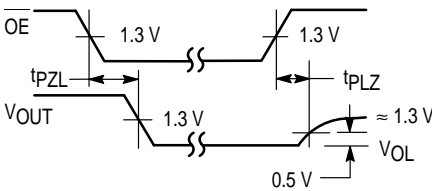


Figure 6

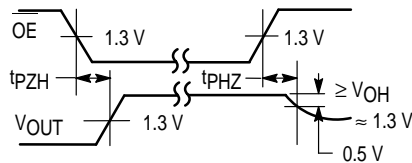
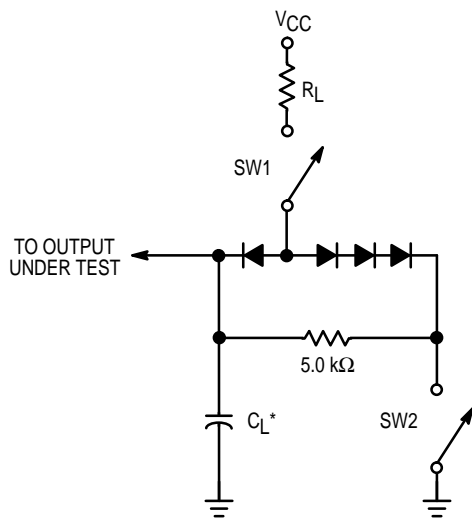


Figure 7

AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

Figure 8

SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed