ECE 429 Laboratory 4
Gate Delay and Power

Announcements:

1. **Teaching Assistants**
   Lab-1: Yunlong Zhang (yzhan167@hawk.iit.edu), Office Hours: 11:30 AM. - 1:30 PM. at SH309 on Mondays
   Lab-2: Shuai Li (sli97@hawk.iit.edu), Office Hours: 11:30 - 1:30 PM. at SH309 on Fridays

2. **Time Frame for Lab-04**

- In-Class students
  - ECE-429-01 (every Monday 1:50 - 4:30 PM.) -10/05/2015
  - ECE-429-02 (every Wednesday 6:25 - 9:05 PM.) -09/30/2015
  - ECE-429-03 (every Friday 1:50 - 4:30 PM.) -10/02/2015
- Internet Students
  - Every Monday (Report due: every Monday at 4:30 PM.)

3. **Account Administrator**
   If you have account issues or remote access problems, please contact Mr. Upendra Gandhi (support@ece.iit.edu).

1. Introduction

Delay and power consumption are the most important characteristics of gates and circuits. In this lab, instead of building a real gate and measuring its delay and power using scopes and meters, we will draw the schematic of a 2-input NAND gate and use HSPICE to study how the transistor sizes, load capacitances, and input transitions will affect gate delay and power.

2. Delay and Power Measurements

While you can always use CosmosScope to measure the delays for your design, it is more convenient to perform measurements within a SPICE netlist so that you can obtain the delays directly from the output of the HSPICE simulation. Assume your NAND gate

has two inputs ’a’ and ’b’ and one output ’f ’. Suppose ’b’ is connected to the supply voltage and the changes in ’a’ will trigger ’f ’ to change. You can use the following SPICE statements to measure the rising and falling delays.

```
.measure tpdr
+ TRIG v(a) VAL='0.55' FALL=1
+ TARG v(f) VAL='0.55' RISE=1
.measure tpdf
+ TRIG v(a) VAL='0.55' RISE=1
+ TARG v(f) VAL='0.55' FALL=1
```

More details can be found in Chapter 8.2.4.

On the other hand, it is more tricky to measure the power consumptions. Since a gate is always powered by the supply voltage, the power consumption of the gate is proportional to the current passing through it. Therefore, to obtain the correct power measurement, one must use a dedicated voltage source (vdc) to power the gate. Furthermore, since the current will change rapidly when the output is rising/falling, it only makes sense to compute the average power consumption over a long period of time.

Suppose the **vdc** that supplies power to your NAND gate is called ’v2’. You can use the following SPICE statements to measure the average power consumption of your gate from 0ns to 5ns.

```
.measure pwr AVG P(v2) FROM=0 TO=5n
```

More details can be found in Chapter 8.5.4.

To view and store the HSPICE output at the same time, use the following command:

```
username@host:~% hspice lab4.sp | tee lab4.hspice.log
```

3. Preparing for the Laboratory (Pre-Lab)

Please make sure you have the following prepared before you come to lab.

- Refresh yourself of elements in SPICE netlists. A tutorial can be found in Chapter 8.2.
- Sketch a schematic for a static CMOS 2-input NAND gate.
- Decide the input transitions that would lead to the maximum rising or falling delays for the NAND gate.

4. Lab Instructions

Create the schematic of a 2-input NAND gate in Virtuoso. The schematic should be stored in a cell view so that it can be reused in this and later labs. All the transistors

(PMOS and NMOS) in the gate should have the minimum width (90nm) and length (50nm).

Create a testing circuit to test your NAND gate design. Use a load capacitance of 1fF and a transient analysis stopping at 5ns with 1ps step size. Export your circuit as a SPICE netlist 'lab4.sp'.

Edit 'lab4.sp' to include the following three settings of excitations, one at a time, to test your NAND gate design for various signal transitions.

- ab=01 → 11 and 11 → 01
  v0 a 0 PULSE 0 1.1 0 10p 10p 490p 1n
  v1 b 0 DC=1.1
- ab=10 → 11 and 11 → 10
  v0 a 0 DC=1.1
  v1 b 0 PULSE 0 1.1 0 10p 10p 490p 1n
- ab=00 → 11 and 11 → 00
  v0 a 0 PULSE 0 1.1 0 10p 10p 490p 1n
  v1 b 0 PULSE 0 1.1 0 10p 10p 490p 1n

Simulate your NAND gate for these three settings. Compute the rising propagation delay and the falling propagation delay as the maximum of the corresponding three delays and record the input transition corresponding to the maximum. Pay attention to the time you are measuring and if you still have doubts you can double check the measurement with cscope (Note that this lab is intended to teach you how to measure using hspice). Compute the average power consumption as the average of the three average power consumptions.

The delay and power measurement results are stored in "lab4.mt0". We can also find the results in "lab4.hspice.output". Note that measured power would be negative because the direction of current is from VDD (positive side of the supply voltage source) to GND (negative side of the supply voltage source). Please report its absolute value as the power.

Edit 'lab4.sp' to use a load capacitance of 2fF, 4fF, and 8fF for additional simulations. It is not necessary to modify the schematic of the testing circuit and re-generate the SPICE netlist. We can just modify the line "c0 f 0 1f" in "lab4.sp" by changing the value of cap-acitance into 2f, 4f, or 8f.

There are at least two different ways to use the sweep command for our purpose:

(1) change the line "c0 f 0 1f" and the line starting with ".TRAN" into:
c0 f 0 CAP
.TRAN 1p 5n START=0.0 SWEEP CAP POI 4 1f 2f 4f 8f

(2) change the line "c0 f 0 1f" and the line starting with ".TRAN" into:
c0 f 0 CAP
.TRAN 1p 5n START=0.0 SWEEP DATA=D

.DATA D
+ CAP
+ 1f
+ 2f
+ 4f
+ 8f
.ENDDATA

Method (a) uses a sequence of CAP values for simulation, while method (b) takes a data table D which defines the values of CAP. Both methods give the same functionality, and we can use either one for our purpose.

The following table is provided for your convenience to record the data.

w=90nm l=50nm	Load Capacitance			
	1f	2f	4f	8f
Rising Propagation Delay				
Falling Propagation Delay				
Average Power Consumption				

Note that you can obtain the rising/falling delays and the average power consumption for one set of excitations and ALL load capacitances within one HSPICE simulation by using the SWEEP command. See Chapter 8.5.3 for more details.

Modify your schematic to change the transistor widths to 180nm and 270nm. **We should modify the width of transistor in the schematic design,** and re-generate the SPICE netlist, because the change of transistor width may result in the change of some other parameters of the transistor (e.g., AD, AS, PD, PS). Repeat the above experiments. Two more tables are provided for your convenience.

w=180nm l=50nm	Load Capacitance			
	1f	2f	4f	8f
Rising Propagation Delay				
Falling Propagation Delay				
Average Power Consumption				

w=270nm l=50nm	Load Capacitance			
	1f	2f	4f	8f
Rising Propagation Delay				
Falling Propagation Delay				
Average Power Consumption				

5. Deliverables

The requirement of the lab/project reports with a template can be found on the Blackboard. *NEVER share your writings/screenshots with others.* We prefer to receive reports electronically as either .pdf or .doc files through the Assignments section on the Blackborad.

Follow the template for lab/project reports posted on the Blackboard to structure your lab report. Briefly describe the tasks you have accomplished. Report your measure-ments of propagation delays/corresponding input transitions and power consumptions (you may use the above three tables for such purpose). Discuss your lab by addressing at least the following questions.

- What input transitions will you expect to have the maximum rising or falling delay? Why? Do the experimental results match your expectations?
- Does the relationship between transistor sizes, load capacitances, and propagation delays follow the linear delay model? If yes, use figures to visualize the relation-ships and then derive the parasitic delay (in ps) and the logical effort (in ps·fF/nm) for your NAND gates.
- How power consumptions change as transistor sizes and load capacitances change?
- Among dynamic power, static power, and short circuit power, what are measured in this lab?

Finally, attach a screenshot of your NAND gate schematic, and one version of 'lab4.sp' plus its corresponding HSPICE output as the appendix.

6. Bonus Work

You can obtain an additional 20% in the grade of this lab if you study how input slew rates (also known as slops) affect propagation delays and output slew rate. Design a set of experiments to collect necessary data and fit them into a model similar to that in Chapter 4.6.1. You should discuss your approach, present the experimental results and the obtained model, and attach relevant screenshots to your lab report for grading.