Assignment 1

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Problem 1.3

Describe the steps that transform a program written in a high-level language such as C into a representation that is directly executed by a computer processor.

We can thank compilers for allowing computer programmers to be as productive as they are today. The compiler will look at the syntax of a high-level language and translate the statement into the corresponding assembly code that will produce the same functionality. For example the compiler would translate this C code:

```
swap(int v[], int k){
    int temp;
    temp = v[k];
    v[k] = v[k+1];
    v[k+1] = temp;
}
```

into:

```
swap:
    multi $2, $5,4
    add   $2, $4,$2
    lw    $15, 0($2)
    lw    $16, 4($2)
    sw    $16, 0($2)
    sw    $15, 4($2)
    jr    $31
```

After this, the assembler takes the translation and converts these statement into binary, or machine code, so that the operations can be executed in the hardware.

Problem 1.7

Compilers can have a profound impact on the performance of an pllication. Assume that for a program , compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.

1a. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns

$$\begin{aligned}\text{Clock Cycles for A} &= \frac{\text{Execution time}}{\text{Clock Cycle Time}} \\ &= \frac{1.1s}{1.0E{-}9s} \\ &= 1.1E9\end{aligned}$$

$$\begin{aligned}\text{Clock Cycles for B} &= \frac{\text{Execution time}}{\text{Clock Cycle Time}} \\ &= \frac{1.5s}{1.0E{-}9s} \\ &= 1.5E9\end{aligned}$$

$$\begin{aligned}\text{CPI for A} &= \frac{\text{Clock Cycles}}{\text{Instruction}} \\ &= \frac{1.1E9}{1.0E9} \\ &= \mathbf{1.1}\end{aligned}$$

$$\begin{aligned}\text{CPI for B} &= \frac{\text{Clock Cycles}}{\text{Instruction}} \\ &= \frac{1.5E9}{1.2E9} \\ &= \mathbf{1.25}\end{aligned}$$

b. Assume the compiled program run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

$$\begin{aligned}\text{Execution time} &= \text{Instructions} \times \text{CPI} \times \text{Clock Cycle Time} \\ \text{AInstr.} \times \text{A CPI} \times \text{A CCT} &= \text{BInstr.} \times \text{B CPI} \times \text{B CCT} \\ 1.0E9 \times 1.1 \times ACCT &= 1.2E9 \times 1.25 \times BCCT \\ \frac{\text{A CCT}}{\text{B CCT}} &= \frac{1.5E9}{1.1E9} \\ &\approx \mathbf{1.363} \text{ times faster}\end{aligned}$$

c. A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using the new compiler versus using compiler A or B on the original processor?

$$\begin{aligned}\text{C Clock Cycles} &= \text{Instructions} \times \text{C CPI} \\ &= 6.0E8 \times 1.1 \\ &= 6.6E8 \text{ clock cycles} \\ \text{Execution time} &= \text{Clock Cycles} \times \text{Clock Cycle Time} \\ &= 6.6E8 \times 1.0E{-}9 \\ &= 0.66s\end{aligned}$$

$$\begin{aligned}\frac{\text{Execution time of A}}{\text{Execution time of C}} &= \frac{1.1}{0.66} \\ &\approx \textbf{1.67} \text{ times faster than A}\end{aligned}$$

$$\begin{aligned}\frac{\text{Execution time of B}}{\text{Execution time of C}} &= \frac{1.5}{0.66} \\ &\approx \textbf{2.27} \text{ times faster than B}\end{aligned}$$

Problem 1.8

The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25V. Assume that, on average, it consumed 10W of static power and 90W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9V. Assume that on average, it consumed 30W of static power and 40W of dynamic power.

1. For each processor find the average capactive loads

$$\begin{aligned}\text{Capacitive Load of Pentium 4} &= \frac{\text{Power}}{\text{Voltage}^2 \times ClockRate} \\ &= \frac{90}{1.25^2 \times 3.6 \times 10^9} \\ &= \boldsymbol{1.6 \times 10^{-8} W}\end{aligned}$$

$$\begin{aligned}\text{Capacitive Load of i5} &= \frac{\text{Power}}{\text{Voltage}^2 \times ClockRate} \\ &= \frac{40}{0.9^2 \times 3.4 \times 10^9} \\ &= \boldsymbol{1.4524 \times 10^{-8} W}\end{aligned}$$

2. Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

$$\begin{aligned}
\text{Total Power for Pentium 4} &= 10W + 90W = 100W \\
\text{Total Power for i5} &= 30W + 40W = 70W \\
\text{Pentium 4 Static Power Percent} &= \frac{10}{100} \times 100 = \mathbf{10\%} \\
\text{i5 Static Power Percent} &= \frac{30}{70} \times 100 \approx \mathbf{42.86\%} \\
\text{Pentium 4 ratio} &= \frac{\text{Static Power}}{\text{Dynamic Power}} \\
&= \frac{10W}{90W} = \mathbf{1:9} \\
\text{i5 ratio} &= \frac{\text{Static Power}}{\text{Dynamic Power}} \\
&= \frac{30W}{40W} = \mathbf{3:4}
\end{aligned}$$

3. If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

$$\begin{aligned}
\text{Power} &= \text{Voltage} \times \text{Current} \\
\text{Current}_{\text{old}} &= \text{Current}_{\text{new}} \\
\text{Reduced Power Pentium 4} &= 90W \\
\text{Reduced Power i5} &= 63W \\
\frac{\text{Power}_{\text{old}}}{\text{Voltage}_{\text{old}}} &= \frac{\text{Power}_{\text{new}}}{\text{Voltage}_{\text{new}}} \\
\text{Voltage}_{\text{new}} &= \frac{90 \times 1.25}{100} \\
&= 1.125V \\
\frac{1.25V}{1.125} &\approx \mathbf{1.1} \text{ times reduction}
\end{aligned}$$

Problem 1.10

Assume a 15cm diameter wafer has a cost of 12, contains 84 dies, and has 0.020 defects/cm^2. Assume a 20cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm^2.

1. Find the yield for both wafers.

$$
\begin{aligned}
\text{Wafer Area} &= \pi \times r^2 \\
\text{Wafer Area 1} &= \pi \times 7.5^2 \\
&\approx 176.71\text{cm}^2 \\
\text{Wafer Area 2} &= \pi \times 10^2 \\
&\approx 314.159\text{cm}^2 \\
\text{Die Area 1} &= \frac{\text{Wafer Area 1}}{\text{Dies per Wafer 1}} \\
&\approx 2.1\text{cm}^2 \\
\text{Die Area 2} &= \frac{\text{Wafer Area 2}}{\text{Dies per Wafer 2}} \\
&\approx 3.14\text{cm}^2 \\
\text{Yield} &= \frac{1}{(1 + (\text{Defects per area} \times \text{Die area}/2))^2} \\
\text{Yield 1} &= \frac{1}{(1 + (0.020 \times 2.1/2))^2} \\
&= \frac{1}{1.021^2} \\
&\approx \mathbf{0.959} \\
\text{Yield 2} &= \frac{1}{(1 + (0.031 \times 3.14/2))^2} \\
&= \frac{1}{1.04867^2} \\
&\approx \mathbf{0.909}
\end{aligned}
$$

2. Find the cost per die for both wafers

$$
\begin{aligned}
\text{Cost per die} &= \frac{\text{Cost per wafer}}{\text{Dies per wafer} \times \text{yield}} \\
\text{Cost per die 1} &= \frac{12}{84 \times 0.959} \\
&\approx \mathbf{0.1489} \\
\text{Cost per die 2} &= \frac{15}{100 \times 0.909} \\
&\approx \mathbf{0.165}
\end{aligned}
$$

3. If the number of dies per wafer is increased by 10% and the defects per area unit increases by 15%, find the die area and yield.

$$\begin{aligned}
\text{New Dies per Wafer } 1 &= 1.1 \times 84 = 92.4 \\
\text{New Dies per Wafer } 2 &= 1.1 \times 100 = 110 \\
\text{New defects/cm}^2 1 &= 1.15 \times 0.020 = 0.023 \text{ defects/cm}^2 \\
\text{New defects/cm}^2 2 &= 1.15 \times 0.031 = 0.03565 \text{ defects/cm}^2 \\
\text{New Die Area } 1 &= \frac{176.71}{92.4} = \mathbf{1.912}\text{cm}^2 \\
\text{New Die Area } 2 &= \frac{314.159}{110} = \mathbf{2.855}\text{cm}^2 \\
\text{New Yield } 1 &= \frac{1}{(1 + (0.023 \times 1.912/2))^2} \\
&= \frac{1}{1.0219^2} \approx \mathbf{.9574} \\
\text{New Yield } 2 &= \frac{1}{(1 + (0.03565 \times 2.855/2))^2} \\
&= \frac{1}{1.05^2} \approx \mathbf{.9054}
\end{aligned}$$

4. Assume a fabrication process improves the yield from 0.92 to 0.95. Find the defects per area unit for each version of the technology given a die area of 200 mm^2.

$$\begin{aligned}
\text{Yield}^{1/2} &= \frac{1}{(1 + \text{defects per area} \times \text{die area}/2)} \\
(1 + \text{defects per area} \times \text{die area}/2) &= \text{Yield}^{-1/2} \\
\text{Defects per area} &= \frac{(\text{Yield}^{-1/2} - 1) \times 2}{\text{Die area}} \\
\text{Defects per area Version } 1 &= \frac{0.92^{-1/2} - 1 \times 2}{200\text{mm}^2} = \mathbf{0.000425} \text{ defects/mm}^2 \\
\text{Defects per area Version } 2 &= \frac{0.95^{-1/2} - 1 \times 2}{200\text{mm}^2} = \mathbf{0.000259} \text{ defects/mm}^2
\end{aligned}$$

Problem 1.14

Assume a program requires the execution of 50×10^6 FP instructions, 110×10^6 INT instructions, 80×10^6 L/S instructions, and 16×10^6 branch instructions. The CPI for each type of instructions is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate.

1. By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

$$\begin{aligned}
\Sigma\text{Clock Cycles} &= (50 \times 10^6 \cdot 1) + (110 \times 10^6 \cdot 1) + (80 \times 10^6 \cdot 4) + (16 \times 10^6 \cdot 2) \\
&= 512 \times 10^6
\end{aligned}$$

$$\text{Desired clock cycles} = 256 \times 10^6$$

$$256 \times 10^6 = (50 \times 10^6 \cdot \text{Desired CPI}) + (110 \times 10^6 \cdot 1) + (80 \times 10^6 \cdot 4) + (16 \times 10^6 \cdot 2)$$

$$\text{Desired CPI} = \frac{256 \times 10^6 - 462 \times 10^6}{50 \times 10^6} = -4.12$$

This improvement is IMPOSSIBLE!

2. By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?

$$\text{Desired clock cycles} = 256 \times 10^6$$

$$256 \times 10^6 = (50 \times 10^6 \cdot 1) + (110 \times 10^6 \cdot 1) + (80 \times 10^6 \cdot \text{Desired CPI}) + (16 \times 10^6 \cdot 2)$$

$$\text{Desired CPI} = \frac{256 \times 10^6 - 192 \times 10^6}{80 \times 10^6} = \mathbf{0.8}$$

CPI must be reduced by 1/5

3. By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?

$$\text{CPI}_{\text{INT}} = 0.4$$

$$\text{CPI}_{\text{FP}} = 0.4$$

$$\text{CPI}_{\text{L/S}} = 1.2$$

$$\text{CPI}_{\text{Branch}} = 0.6$$

$$\text{Execution time} = \frac{\text{Clock cycles}}{\text{Clock rate}}$$

$$= \frac{512 \times 10^6}{2 \times 10^9} = 0.256s$$

$$\Sigma\text{Clock Cycles} = (50 \times 10^6 \cdot 0.4) + (110 \times 10^6 \cdot 0.4) + (80 \times 10^6 \cdot 1.2) + (16 \times 10^6 \cdot 0.6)$$

$$= 169.6 \times 10^6$$

$$\text{New Execution Time} = \frac{169.6 \times 10^6}{2 \times 10^9} = \mathbf{0.0848\ s}$$

Execution time reduced to $\approx 1/3$ original time