Lab 4: BJT Characterisitics/Biasing Circuits

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ECE 311-03
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1 Introduction

The purpose of this experiment is to demonstrate the use of a curve tracer to record the CE collector characteristics of BJT circuits. After this, the Q point node voltages V_B, V_C, and V_E shown in the circuits of Figures 1 through 5 are calculated at room temperature and at an elevated temperature.

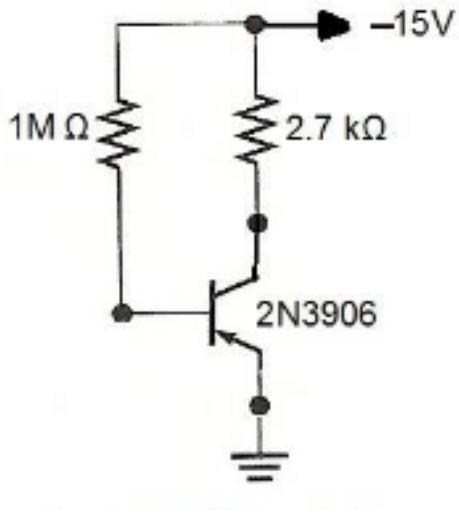

Figure 2: PNP Fixed Bias Circuit

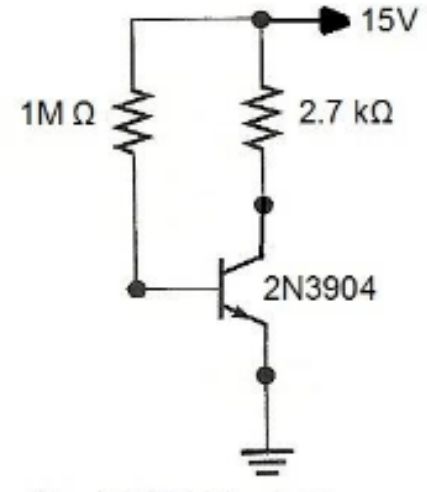

Figure 1: NPN Fixed Bias Circuit

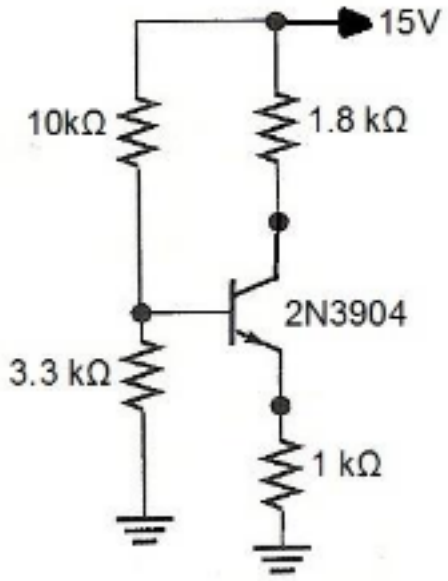

Figure 3: NPN Four Resistor Bias Circuit

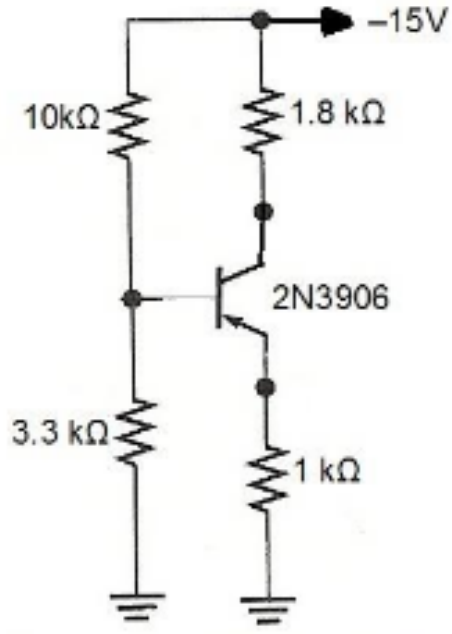

Figure 4: PNP Four Resistor Bias Circuit

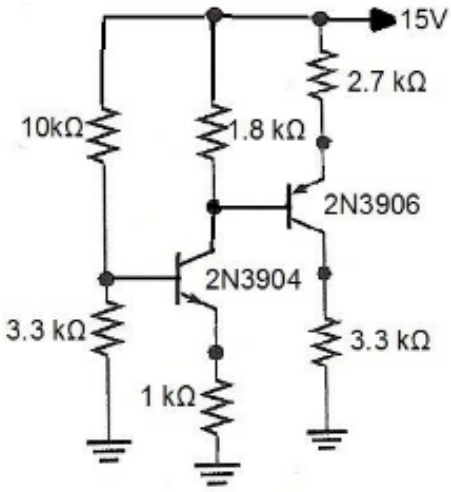

Figure 5: NPN-PNP Four Resistor Bias Circuit

2 Theory

The Q point, also known as the operating point, of a fixed bias scheme BJT circuit is sensitive to changes in the DC circuit gain, β. In a classical four resistor bias network, the Q point is usually isnensitive to the value of β. Using circuits with transistors that have different values of β, the sensitivity of each biasing circuit can be compared. In order to obtain transistors with different values of β, a lab tech measures the value manually and sorts the respective transistor into a category of low, medium, and high. These categories correspond to values of roughly 50, 100, and 200 respectively. To study the effect of a changing β, the operating temperature of the transistor can be changed. This can be done by using the most technical of equipment, the modern day hair dryer.

3 Procedure

The equipment used in the lab was:

- Breadboard
- DC Power Supply
- Function Generator
- Curve Tracer
- $1M\Omega, 2.7k\Omega$, $10k\Omega$, $1.8k\Omega$, $3.3k\Omega$, and $1k\Omega$ resistors
- 2N3904 NPN BJT Chip
- 2N3906 PNP BJT Chip

- Wire
- Multimeter

The first part of the lab is a demonstration of the use of the curve tracer. The steps to obtain the curve are:

1. Insert an NPN transistor into the left side of the test jig and a PNP transistor in the right side of the jig
2. Set the polarity switch to NPN
3. Set the left-off-right selection switch to left and observe the result
4. Heat the transistor with a hair dryer
5. Reset the collector supply to 75V max and decrease the horizontal sensitivity to keep the trace on screen and observe the result
6. Reset the collector voltage to 15V
7. Set the polarity switch to PNP, the left-off-right switch to right and observe the result
8. Go back to the NPN setup
9. Reverse the Transistors (switch the collector and emitter) and observe the results

The latter half of the lab involves constructing each circuit of Figures 1 through 5 and measuring the Q point node voltages. This is done by connecting the black lead of the multimeter to ground and touching the red lead to the base, emitter, and collector of each circuit configuration.

4 Interpretation

Due to lab equipment failure, the first half of the experiment could not be executed. However, since this was supposed to act as a demonstration, this malfunction did not damage the integrity of the results of this experiment. The results from the second part are shown below in Tables 1 through 12.

Q Point Voltage	Volts
V_C	10.57V
V_B	9.97V
V_E	0.4V

Table 1: Room Temperature NPN Fixed Bias Q Point voltages

Q Point Voltage	Volts
V_C	-8.95V
V_B	-8.31V
V_E	-0.3V

Table 2: Room Temperature PNP Fixed Bias Q Point voltages

Q Point Voltage	Volts
V_C	10.8V
V_B	10.25V
V_E	0.45V

Table 3: High Temperature NPN Fixed Bias Q Point voltages

Q Point Voltage	Volts
V_C	-9.1V
V_B	-8.6V
V_E	0V

Table 4: High Temperature PNP Fixed Bias Q Point voltages

Q Point Voltage	Volts
V_C	7.13V
V_B	6.45V
V_E	2.94V

Table 5: Room Temperature NPN Four Resistor Bias Q Point voltages

Q Point Voltage	Volts
V_C	-8.11V
V_B	-7.43V
V_E	-2.01

Table 6: Room Temperature PNP Four Resistor Bias Q Point voltages

Q Point Voltage	Volts
V_C	7.00V
V_B	6.35V
V_E	2.70

Table 7: High Temperature NPN Four Resistor Bias Q Point voltages

Q Point Voltage	Volts
V_C	-8.0V
V_B	-7.28V
V_E	-1.93V

Table 8: High Temperature PNP Four Resistor Bias Q Point voltages

Q Point Voltage	Volts
V_C	7.0V
V_B	6.4V
V_E	2.9V

Table 9: Room Temperature NPN-PNP Four Resistor Bias NPN Q Point voltages

Q Point Voltage	Volts
V_C	9.4V
V_B	7.09V
V_E	6.4V

Table 10: Room Temperature NPN-PNP Four Resistor Bias PNP Q Point voltages

Q Point Voltage	Volts
V_C	6.9V
V_B	6.3V
V_E	2.75V

Table 11: High Temperature NPN-PNP Four Resistor Bias NPN Q Point voltages

Q Point Voltage	Volts
V_C	9.2V
V_B	7.0
V_E	6.48V

Table 12: High Temperature NPN-PNP Four Resistor Bias PNP Q Point voltages

Compared to the results calculated in the preliminary questions, the experimental results obtained in lab differed by a negligible amount, thus reinforcing the accuracy of the laboratory data.

5 Conclusion

Overall, this lab was a success. Even though the first demonstration could not be completed due to factors out of the students' control, the data obtained from the Q point node voltages was accurate.