Lab 3: Inverter Layout

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1 Introduction

The purpose of this experiment is to design the physical layout of an inverter using the Cadence Virtuoso Platform. The objectives are to implement the inverter layout design following industry standard design rules, and to validate the design using simulation software.

2 Theory/Pre-Lab

2.1 Theory

Layout design is often referred to as the "Grunt work" of VLSI design. Regardless of its tedious nature, it is considered the most important part of the VLSI design process. This work is done through the use of a layout editor.

The underlying idea of a layout editor can be compared to a simple paint program, where individual pixels are modified. However, in a layout editor, the pixels are actually grid points, and "paint operations" assign rectangular regions to layers that represent layout objects such as metal, polysilicon, contacts, etc. Using the FreePDK45 library, the minimum manufacturing grid is 2.5nm, however, this can require a lot of time fine tuning the design. While this size is preferred by experienced layout designers, this lab will use a minimum size of 10nm, since wasting small amounts of silicon area is not of this lab's concern.

The FreePDK45 library has a list of design rules that need to be followed to ensure a proper layout. They are listed here: `http://www.eda.ncsu.edu/wiki/FreePDK45:` Because they can be quite complex, it is a silly thing to memorize them. Instead, design rule checking is a common practice used in industry. By frequently using DRC, violations of these design rules can be detected early to make the process go as smoothly as possible.

Because Layout designs and Schematics are created separately, there is a need to be able to easily compare the two. Luckily, Calibre is prepared with this functionality knwon as Layout vs. Schematic (LVS). Calibre LVS extracts a SPICE netlist from both the layout and the schematic, and then they are compared to see if they have the same set of transistors/connections.

Once the comparison is complete and the famous smiley face has been generated (no errors), a simulation can be be run. Because all layout related parasistics can be considered in the simulation, this is a more accurate representation of the functionality of the circuit in the real world.

2.2 Pre-Lab

3 Implementation

3.1 Schematics

3.2 Procedure

3.3 Results

3.4 Discussion

3.5 Questions

1. **What determines the minimum transistor width and length for a specific technology?**

2. **Why should well-taps connect to implanted regions instead of the wells directly?**

3. **What are the benefits of a twin-well process?**

4. **How do the delays of your inverter layout compare to that of the schematic in Lab 2? Do you expect them to be larger or smaller? Why?**

4 Conclusions