# ECE 429 Laboratory 2
# Inverter Schematic

## Announcements:

1. **Teaching Assistants**
   Lab-1: Yunlong Zhang (yzhan167@hawk.iit.edu), Office Hours: 11:30 AM. - 1:30 PM. at SH309 on Mondays
   Lab-2: Shuai Li (sli97@hawk.iit.edu), Office Hours: 11:30 - 1:30 PM. at SH309 on Fridays

2. **Time Frame for Lab-02**
- In-Class students
  - ECE-429-01 (every Monday 1:50 - 4:30 PM.) -09/21/2015
  - ECE-429-02 (every Wednesday 6:25 - 9:05 PM.) -09/16/2015
  - ECE-429-03 (every Friday 1:50 - 4:30 PM.) -09/18/2015
- Internet Students
  - Every Monday (Report due: every Monday at 4:30 PM.)

3. **Account Administrator**
   If you have account issues or remote access problems, please contact Mr. Upendra Gandhi (support@ece.iit.edu).

## 1. Introduction

As it is very costly to manufacture VLSI chips and very difficult to test nanoscale devices, the majority amount of VLSI design work is done on computers. The designers rely heavily on computer-aided design (CAD) techniques to validate their designs before taping-out and silicon debugging. In Lab 2 and 3, you will be introduced to the Cadence Virtuoso platform. This is one of the most widely used commercial electronic design automation (EDA) platform that supports custom IC designs. It serves as a central point for design entry and provides various interfaces to other EDA tools.

The EDA tools rely on information regarding process parameters to determine the behavior of a design in the real world. Usually, such information will be provided by the foundry that will fabricate the design. In this course, we will adopt the open-source

FreePDK45 library that supports a 45nm process derived from the Predictive Technology Model (PTM). It provides necessary information, e.g. SPICE device parameters, layer definitions, parasitic capacitances, and rules for DRC/LVS, for the EDA tools to generate meaningful results. You are encouraged to learn more about the FreePDK libraries from the Internet.

In this lab, you will design a transistor level schematic of an inverter and perform a SPICE simulation on your inverter design. We will utilize Virtuoso Schematic Editor for schematic drawing and use Synopsys HSPICE for circuit simulation. HSPICE is treated as 'golden' for circuit simulation because with proper device parameters, its results faithfully indicate how a circuit would behave in the real world. The Tutorial I: Inverter Schematic and Simulation posted on the Blackboard will guide you through the lab.

## 2. Preparing for the Laboratory (Pre-Lab)

Please make sure you have the following prepared before you come to lab.

- Refresh yourself of elements in SPICE netlists. A tutorial can be found in Chapter 8.2.
- Sketch a schematic for a static CMOS inverter with power sources connected.
- Familiarize yourself with Tutorial I: Inverter Schematic and Simulation.

## 3. Lab Instructions

Create the schematic of an inverter in Virtuoso. The schematic should be stored in a cell view so that it can be reused in this and later labs.

Create a testing circuit to test your inverter design by introducing excitations and load. Export your circuit as a SPICE netlist 'lab2.sp'.

Modify 'lab2.sp' as suggested in the tutorial to inform the SPICE simulator to store all nodal waveforms. Use HSPICE to perform a transient analysis of your circuit and then measure the rising and falling delays of your inverter.

Tips for lab2:

- Setting up your ECE account by using the following command:
  **gedit(space)~/.cshrc**

  Then add following commands to the bottom line:
  **source(space)/import/scripts/ece429.cshrc**
  **source(space)/import/scripts/hspice.cshrc**
  **source(space)/import/scripts/synopsys2012.cshrc**

- You need to sketch a schematic for a static CMOS inverter in your pre-lab part of your final report.
- When you export SPICE netlist, please choose the following path for model: **/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include**

## 4. Deliverables

The requirement of the lab/project reports with a template can be found on the Black board. *NEVER share your writings/screenshots with others.* We prefer to receive reports electronically as either .pdf or .doc files through the Assignments section on the Blackboard.

Follow the template for lab/project reports posted on the Blackboard to structure your lab report. Briefly describe the tasks you have accomplished. Discuss your lab by addressing at least the following questions.

- Where are the bodies of the transistors in your schematic?
- What are the widths and lengths of your transistors?
- How much is the supply voltage?
- What do 'Rise time' and 'Pulse width' mean for 'vpulse' ? Can you locate these two values in the waveforms obtained from the SPICE simulation?
- Tutorial I shows a maximum rising delay of 7.1892p. How long is that in seconds?
- To obtain an inverter design with equal rising and falling delays, will you make the PMOS transistor larger or smaller?

Finally, attach screenshots of your inverter schematic, testing circuit, and delay measurement as the appendix.

## 5. Bonus Work

You can obtain an additional 20% in the grade of this lab if you generate the DC transfer characteristics (similar to Fig. 2.26 (c)) of your inverter design via SPICE simulations and measure its noise margins. A hint is to modify 'lab2.sp' for such purpose. You should discuss your approach, present the noise margins, and attach relevant screenshots to your lab report for grading.