ECE 429 Laboratory 7
Carry-Ripple Addition II

Announcements:

1. **Teaching Assistants**
   Lab-1: Yunlong Zhang (yzhan167@hawk.iit.edu), Office Hours: 11:30 AM. - 1:30 PM. at SH309 on Mondays
   Lab-2: Shuai Li (sli97@hawk.iit.edu), Office Hours: 11:30 - 1:30 PM. at SH309 on Fridays

2. **Time Frame for Lab-07**

- In-Class students
  - ECE-429-01 (every Monday 1:50 - 4:30 PM.) -10/26/2015
  - ECE-429-02 (every Wednesday 6:25 - 9:05 PM.) -10/28/2015
  - ECE-429-03 (every Friday 1:50 - 4:30 PM.) -10/23/2015
- Internet Students
  - Every Monday (Report due: every Monday at 4:30 PM.)

3. **Account Administrator**
   If you have account issues or remote access problems, please contact Mr. Upendra Gandhi (support@ece.iit.edu).

1. Introduction

In this lab, you will design a layout for the full adder and verify its functionality. This layout, together with the full adder schematic from Lab 6, will be used to build a 4-bit carry ripple adder in Lab 8.

2. Preparing for the Laboratory (Pre-Lab)

Please sketch a stick diagram for the mirror adder schematic before you come to lab. Here are a few hints.

- When placing the input ci and the output co, keep in mind that for a carry-ripple adder, co of a full adder should be connected to ci of the next full adder.
- You may refer to either Fig. 11.5 (a) or (b) from the textbook. Be aware that a few

wires are missing from Fig. 11.5 (a).

- Since the pull-up and the pull-down networks are symmetric to each other, the connections for the p-diffusion(s) and the n-diffusion(s) could be symmetric (i.e. the same) in your stick diagram.
- You may use the metal2 layer if you have any difficulty to route the interconnects.

3. Lab Instructions

Follow your stick diagram to create the layout of the mirror adder (Take care with the width of the transistors and try to do your design as small as possible).

For the design rules you can refer to:

http://www.eda.ncsu.edu/wiki/FreePDK45

You can use the "metal2" layer if you have difficulty to route the interconnects. Please note that "metal2" can only be connected with "metal1" using "via1". If you want to connect "poly" with "metal2", you must use "contact " to connect "ploy" with "metal1" first, then use "via1" to connect "metal1" with "metal2". The minimum size of "via1" is 65nm x 65nm according to the design rule, please use 70nm x 70nm in your layout (the same size as "contact"). Please pay attention to the design rules when you draw the layout. You may refer to the "FreePDK45 Documentation" or your previous DRC report about the description on the rules related to "via1" and "metal2".

If you violate too many design rules, it may be very difficult to fix them when you almost finish your drawing.

As some students may have difficulty in sketching the stick diagram, I attached the screenshot of my layout for your reference. Input signals on the left hand side are a, b, and ci from top to bottom. Output signals on the right hand side are s and co from top to bottom. Note that this is just a reference design, not the golden solution, and it can be further optimized to reduce area and wiring. You may come up with different designs.

Run Design rule checking (DRC) and layout v.s. schematic verification (LVS).

4. Deliverables

The requirement of the lab/project reports with a template can be found on the Blackboard. *NEVER share your writings/screenshots with others.* We prefer to receive reports electronically as either .pdf or .doc files through the Assignments section on the Blackborad.

Follow the template for lab/project reports posted on the Blackboard to structure your lab report. Briefly describe the tasks you have accomplished. Discuss how you design the mirror adder layout. Attach screenshots of your mirror adder layout and the LVS report.