Homework 1

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ECE 429

September 21st, 2015

1 Explain the Following Terminologies Briefly

- **Moore's Law** - The observation that the number of transistors in dense integrated circuits has doubled approximately every two years. Named after Gordan E. Moore
- **Feature Size** - The minimum dimension of a transistor that can be reliably built
- **VLSI Design for Power** - Discipline of design that aims to reduce power dissipations while maintaining adequate throughput rate
- **VLSI Design for Manufacturing** - Discipline of design that aims to produce a product in a timely manner with sufficient yield to be profitable
- **ASIC** - Application-Specific Integrated Circuit. An integrated circuit customized for a particular use, rather than general-purpose use
- **Logical Synthesis** - Process by which an abstract from of circuit behavior (usually represented at RTL) is turned into a design implementation
- **Physical Synthesis** - Step in the design cycle that converts circuit representations of components into geometric representations of shapes which, when they are manufactured in their corresponding layers, will ensure the correct functionality
- **Dynamic Power and Leakage Power** - The power consumed during the switching of a transistor, and the power lost to leakage current of transistors
- **Conduction Band** - The lowest range of vacant electronic states. Determines conductivity of the solid
- **Valence Band** - The highest range of electron energies in which electrons are normally present at absolute zero. Determines conductivity of the solid
- **Velocity Saturation** - Sate of a semiconductor when the carrier velocity reaches a maximum value
- **Subthreshold Conduction** - The current between the source and drain of a MOSFET when the transistor is in the subthreshold region

- **Hot Carriers** - Electrons (holes) in a solid-state electronic device that gains sufficient kinetic energy to overcome a potential barrier in order to break an interface state
- **MOSFET Operation Regions** - Three separate modes of a MOSFET depending on the voltage at the terminals: Cutoff, Triode, and Saturation

2 Exercise 1.5

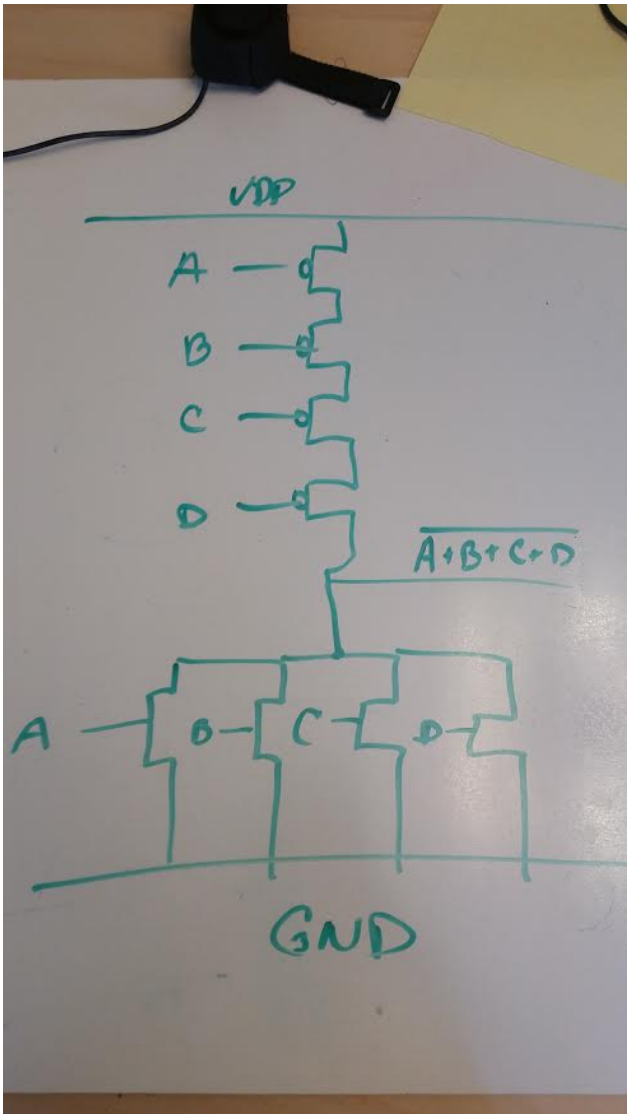

Figure 1: 4 Input NOR Gate

3 Exercise 1.3

a)

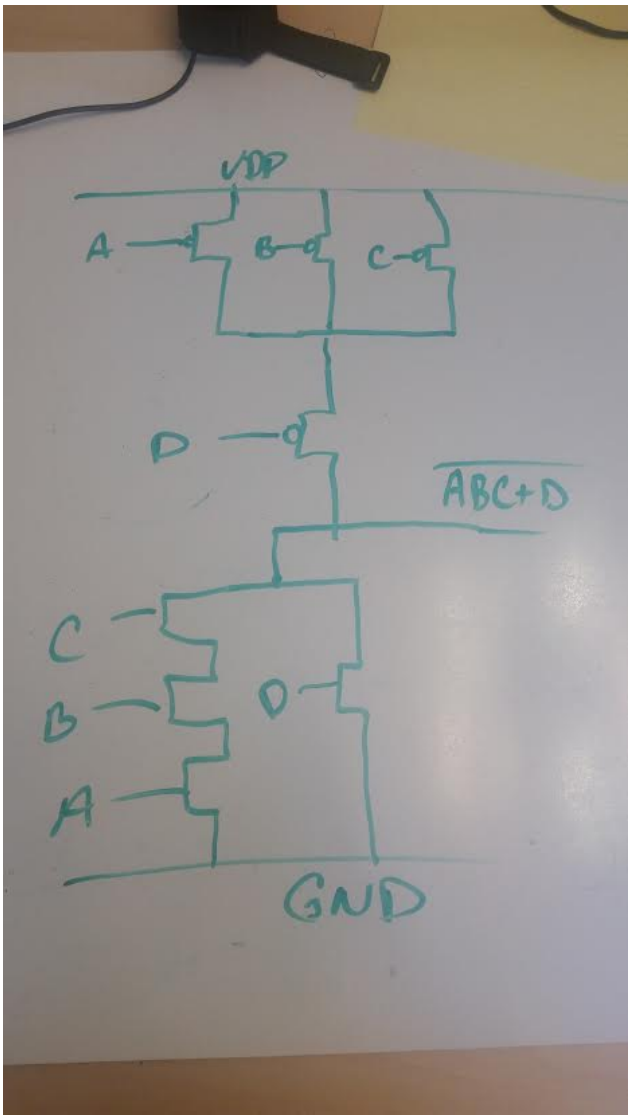

Figure 2: $\overline{ABC + D}$

b)

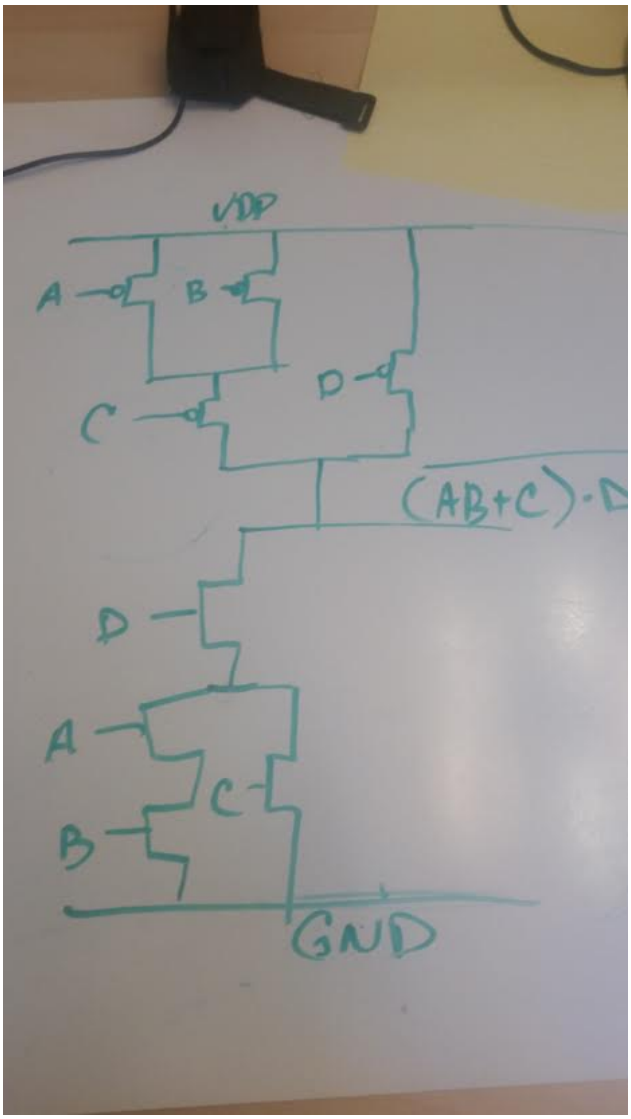

Figure 3: $\overline{(AB + C) \cdot D}$

c)

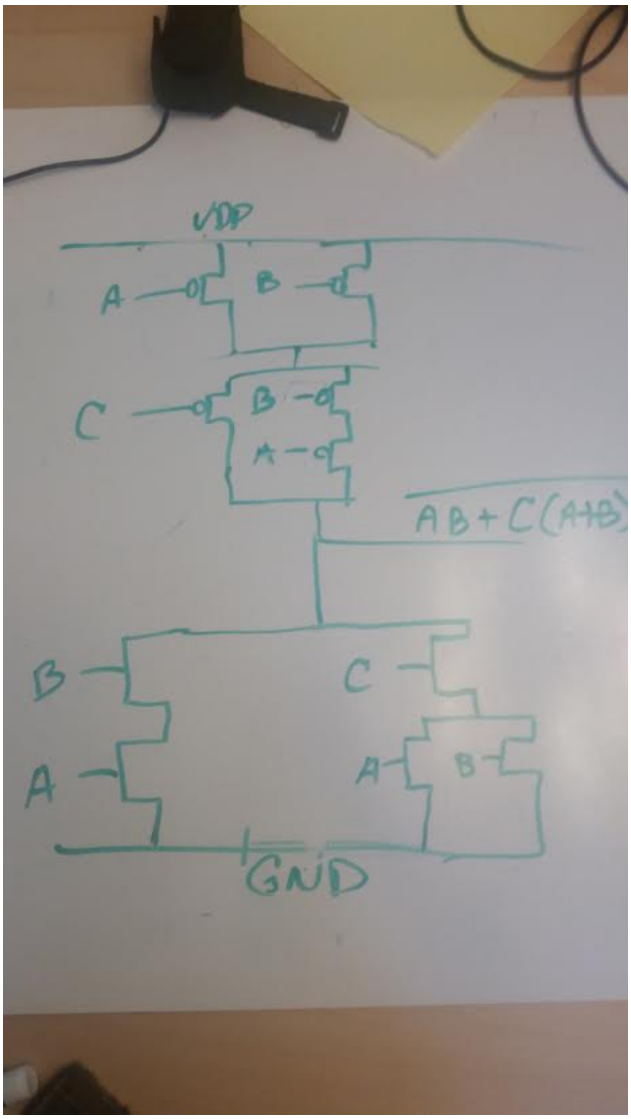

Figure 4: $\overline{AB + C(A + B)}$

4 Exercise 1.10

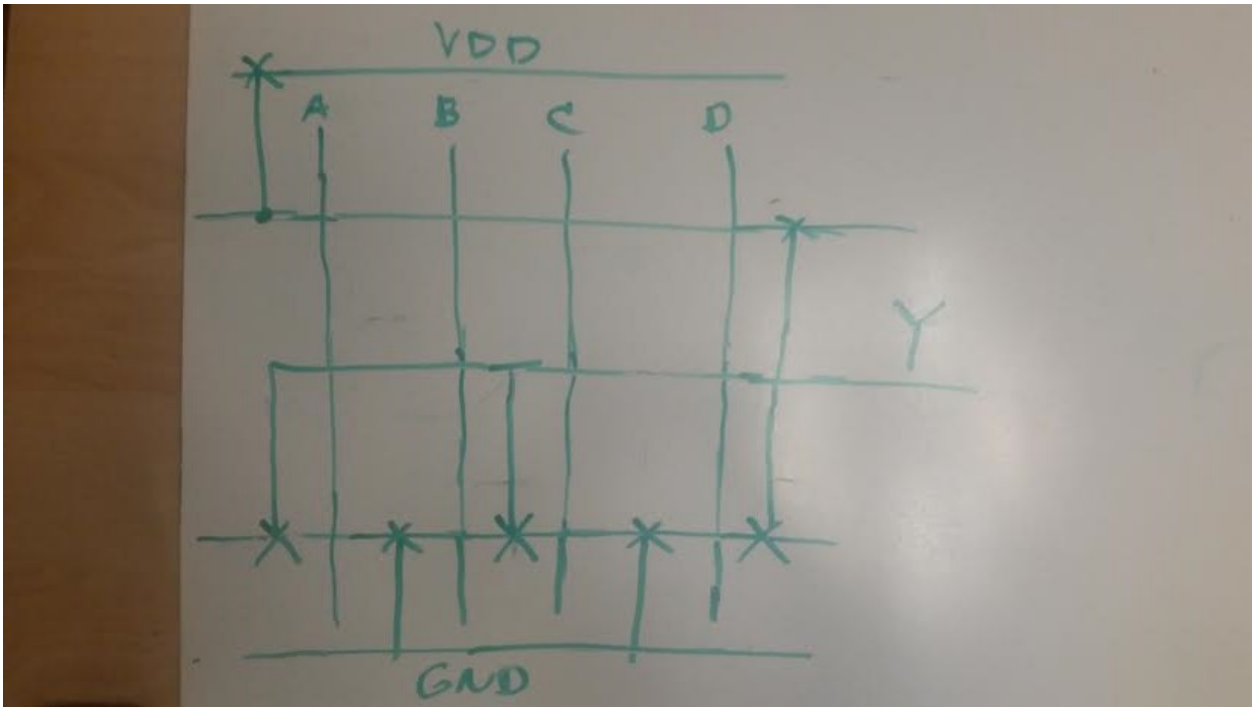

Figure 5: Stick Diagram for 4 Input NOR Gate

5 Exercise 2.2

6 Exercise 2.3

7 Exercise 2.7

8 Exercise 2.9

9 Light Switch Design

Truth Table

A	B	C	F
0	0	0	0
0	0	1	1
0	1	1	0
0	1	0	1
1	0	0	1
1	0	1	0
1	1	1	1
1	1	0	0

Karnaugh Map

A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

a)

$$F = AB'C' + A'B'C + ABC + ABC'$$

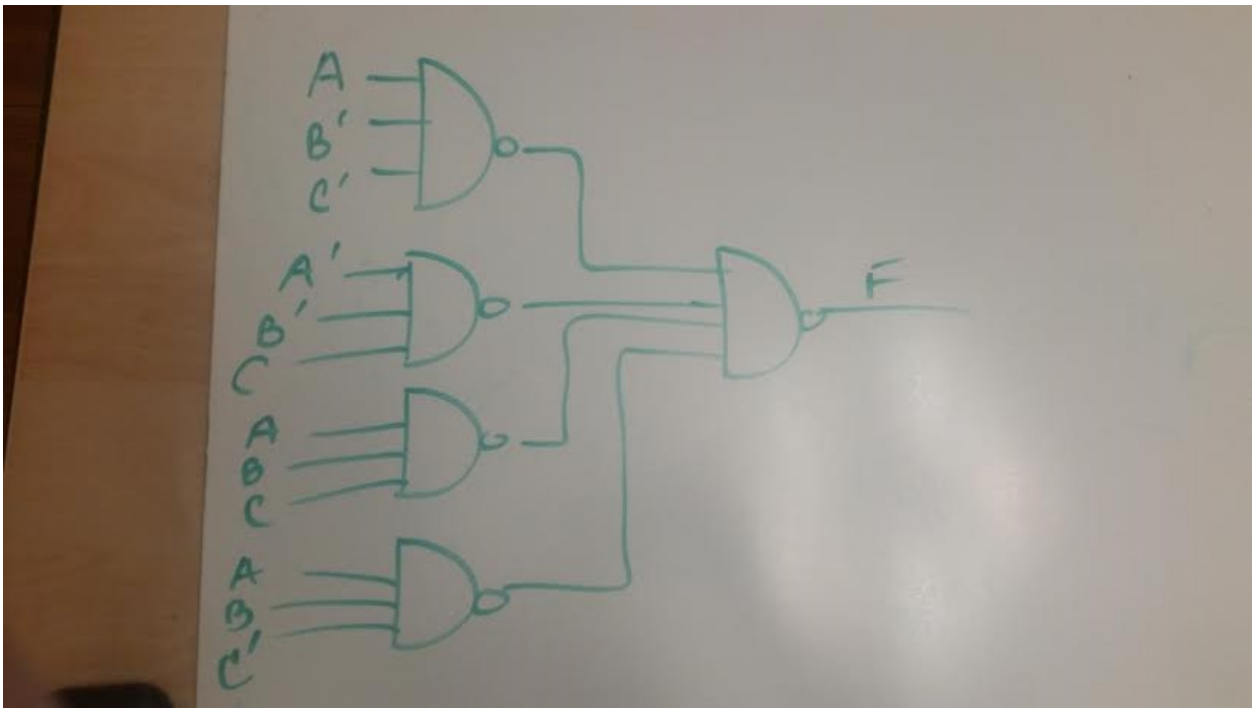

Figure 6: NAND Gate Implementation

b)

$$F = (A + B + C)(A + B' + C')(A' + B + C')(A' + B' + C)$$

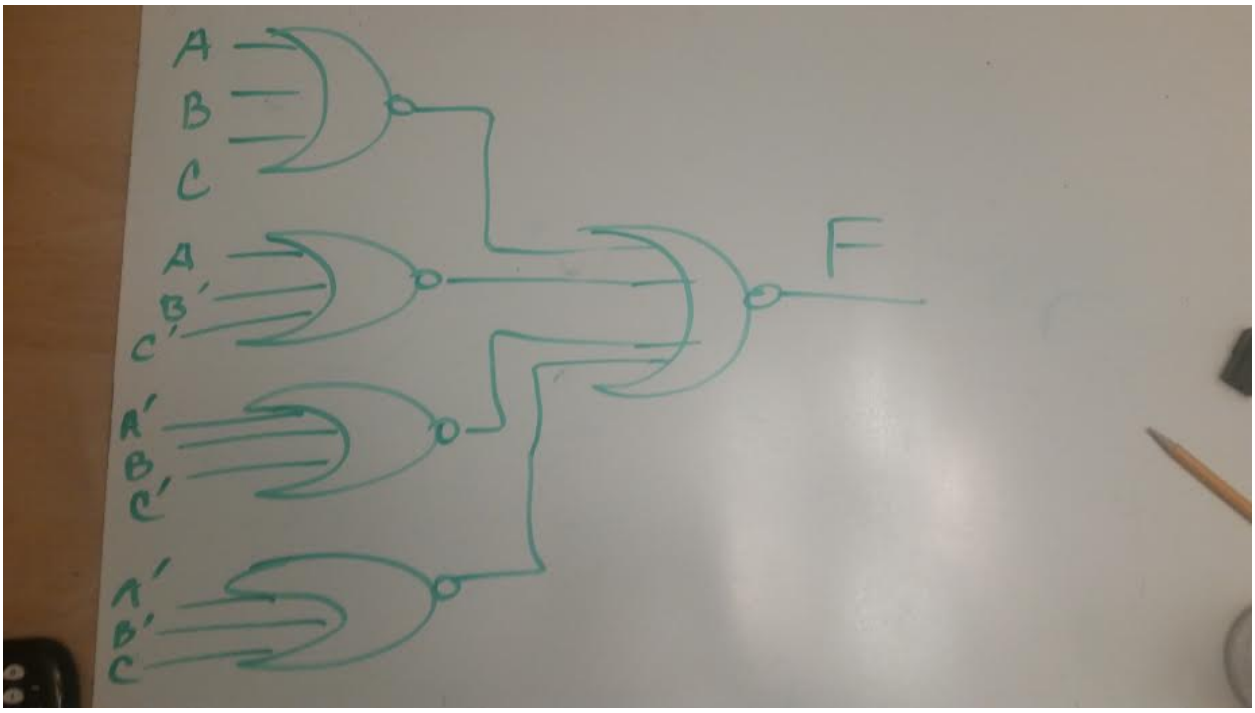

Figure 7: NOR Gate Implementation

10 CMOS Compound Gate