Lab 4: Gate Delay and Power

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ECE 429-01

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1 Introduction

The purpose of this lab is to construct a 2-input NAND gate in Virtuoso. Once created, a test circuit will be constructed to simulate and verify the functionality of the gate, and the delay and power measurements will also be analyzed.

2 Theory/Pre-Lab

2.1 Theory

Power and delay are a huge concern of VLSI designers when designing a chip. As a consequence, it is important to analyze these characteristics of a design before pushing it into production. Luckily, HSPICE simulation is equipped to measure both, which allows the designer to perform measurements within a SPICE netlist using a `.measure` statement. For example, to measure the rising and falling delays, this segment of code can be added to the `*.sp` file:

```
1  .measure tpdr
2  + TRIG v(a) VAL= 0.55 FALL=1
3  + TARG v(f) VAL= 0.55 RISE=1
4  .measure tpdf
5  + TRIG v(a) VAL= 0.55 RISE=1
6  + TARG v(f) VAL= 0.55 FALL=1
```

Since a gate is always powered by a supply voltage, power consumption is dependent on the current passing through a gate. Therefore, it is necessary to use a dedicated voltage source to power the gate and since the current will change rapidly when then output is rising/falling, the average power consumption is measured. Using this measure statement:

```
1  .measure pwr AVG P(voltage_source) FROM=start_time TO=end_time
```

the power consumption of the gate can be measured from start_time to end_time.

2.2 Pre-Lab

A schematic was to be sketched for a CMOS 2-input NAND gate. It is shown in Figure 1.

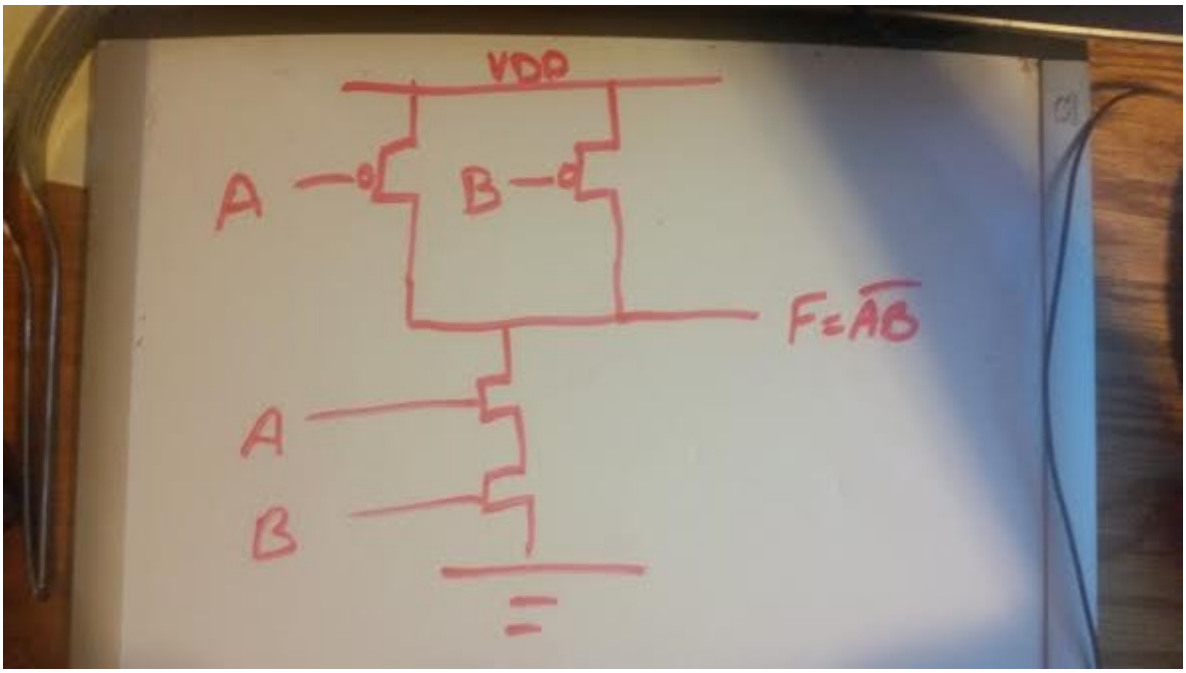

Figure 1: Schematic for 2-Input CMOS NAND Gate

3 Implementation

3.1 Schematics

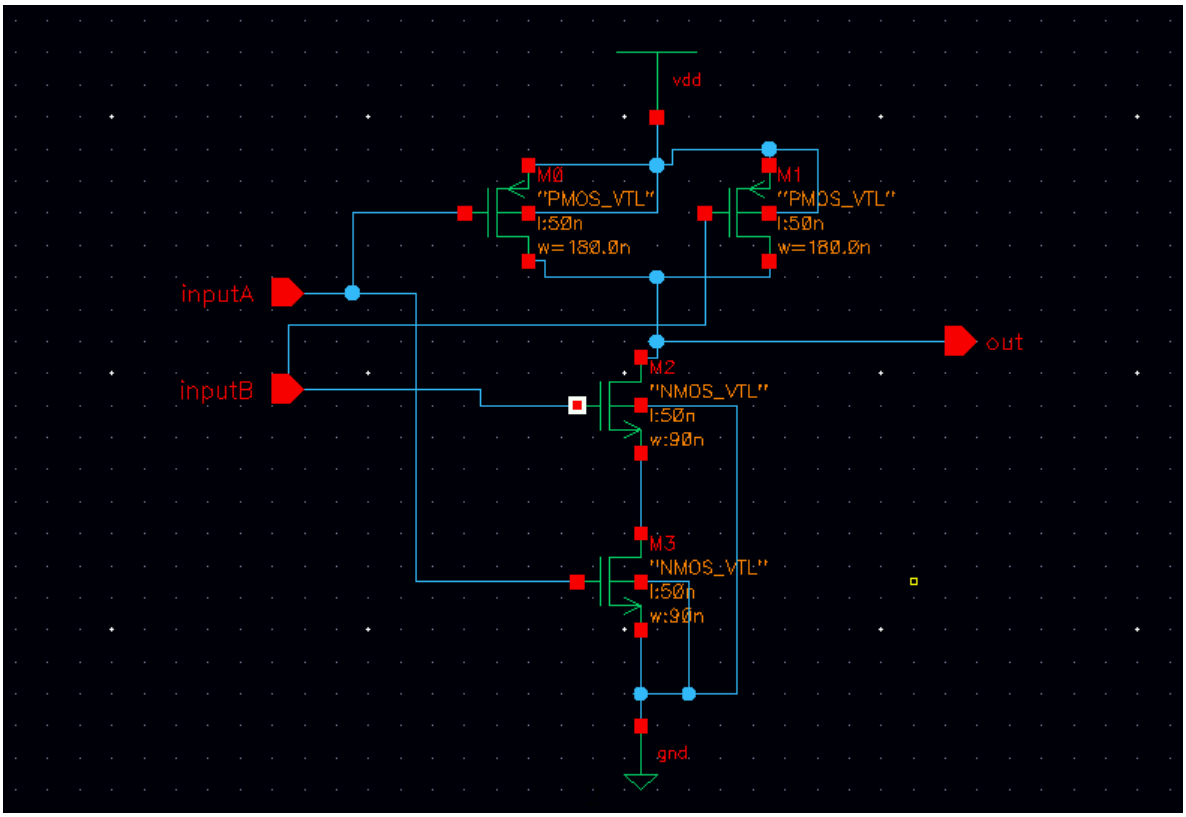

Figure 2: Schematic for 2-Input CMOS NAND Gate

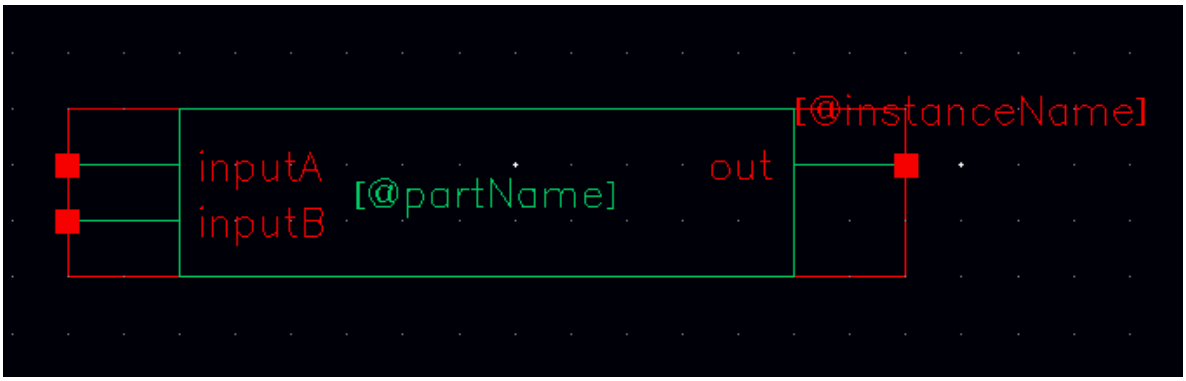

Figure 3: Symbol for 2-Input CMOS NAND Gate

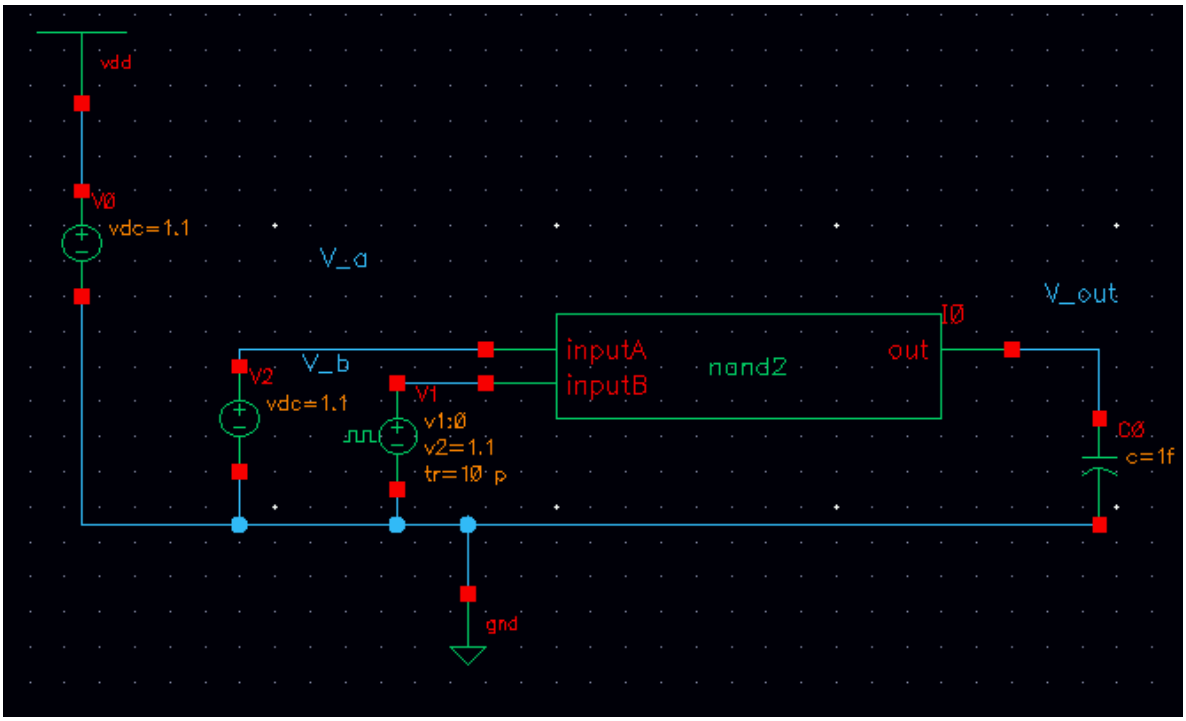

Figure 4: Test Circuit for Simulation

3.2 Procedure

The procedure of this lab involved constructing the 2-Input CMOS NAND gate schematic shown in Figure 1 in virtuoso. Once created, a symbol was created to easily utilize the newly constructed schematic in other circuits. After this, a test circuit was designed to test the functionality of the NAND gate. This is shown in Figure 4. The last step involved simulating the test circuit using HSPICE to verify the functionality of the gate, as well as to measure the delay and power consumption under a load capacitance of 1f, 2f, 4f, and 8f. The results are shown in Tables 1 - 3.

3.3 Results

w=90nm l=50nm	Load Capacitance			
	1f	2f	4f	8f
Rising Propogation Delay	5.32e-12 s	8.56e-12 s	1.36e-11 s	2.14e-11 s
Falling Propogation Delay	1.78e-11 s	2.64e-11 s	4.24e-11 s	7.63e-11 s
Average Power Consumption	2.54e-06 W	3.76e-06 W	6.21e-06 W	1.11e-05 W

Table 1: Width of 90nm

w=180nm l=50nm	Load Capacitance			
	1f	2f	4f	8f
Rising Propogation Delay	7.37e-12 s	1.03e-11 s	1.47e-11 s	2.14e-11 s
Falling Propogation Delay	1.06e-11 s	1.46e-11 s	2.27e-11 s	3.85e-11 s
Average Power Consumption	1.66e-06 W	2.26e-06 W	3.47e-06 W	5.73e-06 W

Table 2: Width of 180nm

w=270nm l=50nm	Load Capacitance			
	1f	2f	4f	8f
Rising Propogation Delay	1.51e-12 s	2.93e-12 s	5.73e-12 s	9.67e-12
Falling Propogation Delay	1.01e-11 s	1.29e-11 s	1.85e-11 s	2.90e-11 s
Average Power Consumption	2.29e-06 W	2.85e-06 W	4.17e-06 W	6.58e-06 W

Table 3: Width of 270nm

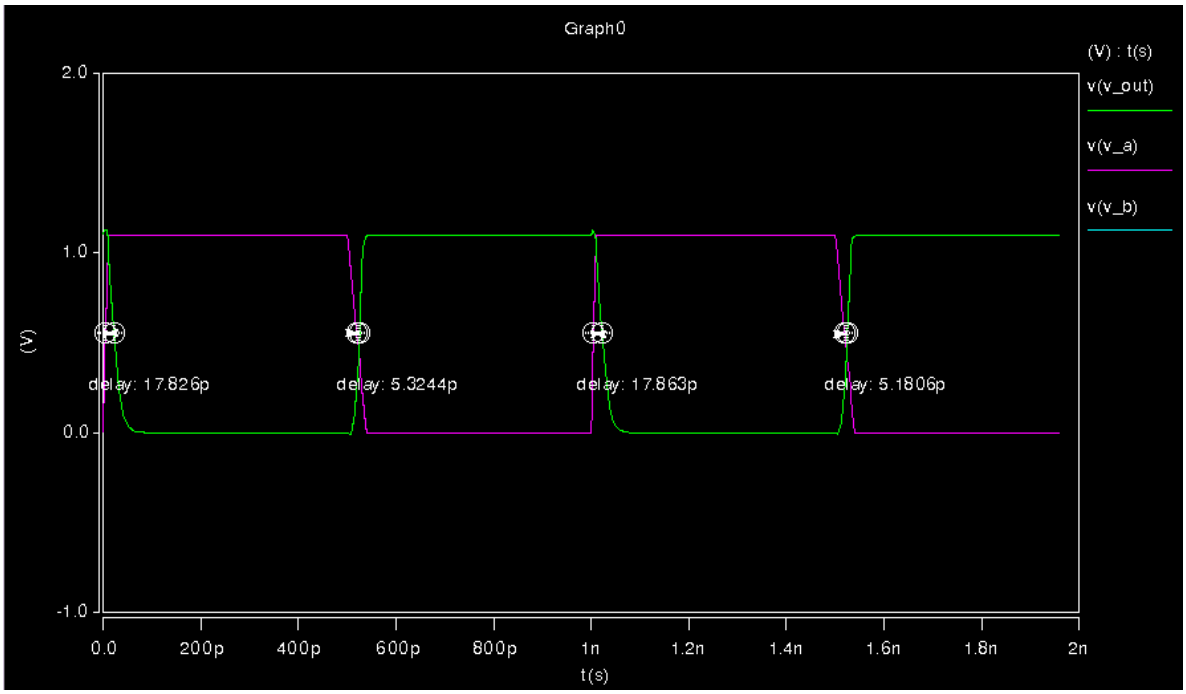

Figure 5: 00 → 11, 11 → 00 Transition Delay

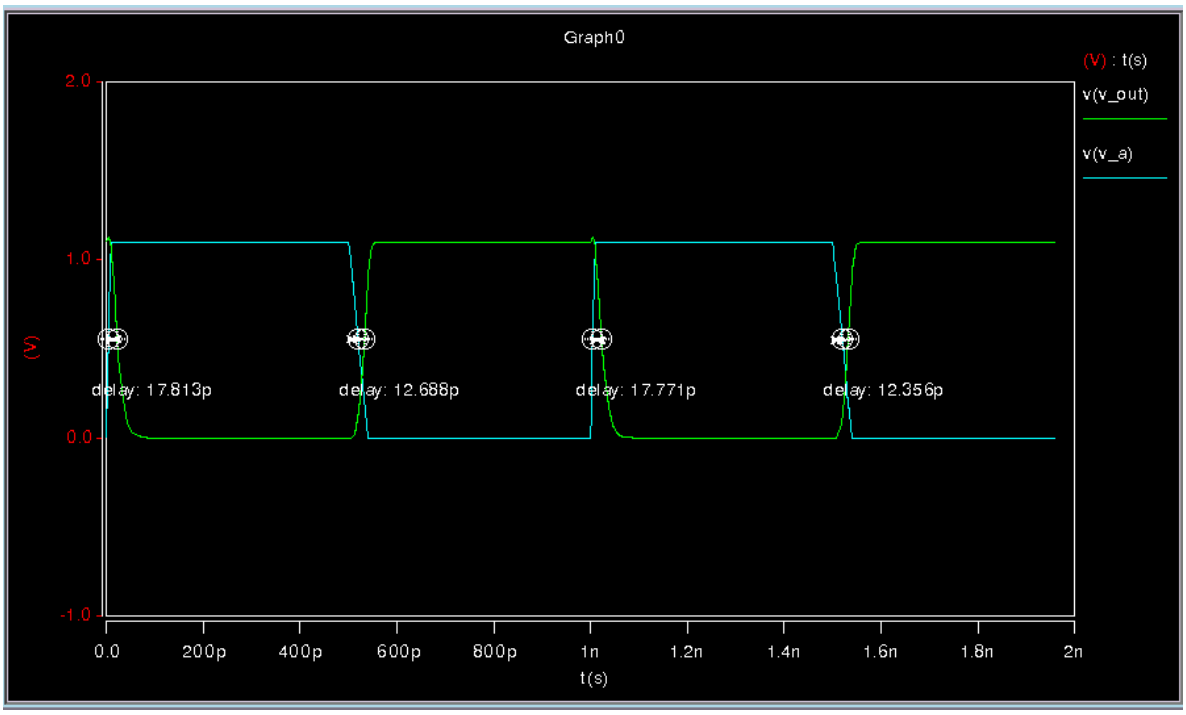

Figure 6: 01 → 11, 11 → 01 Transition Delay

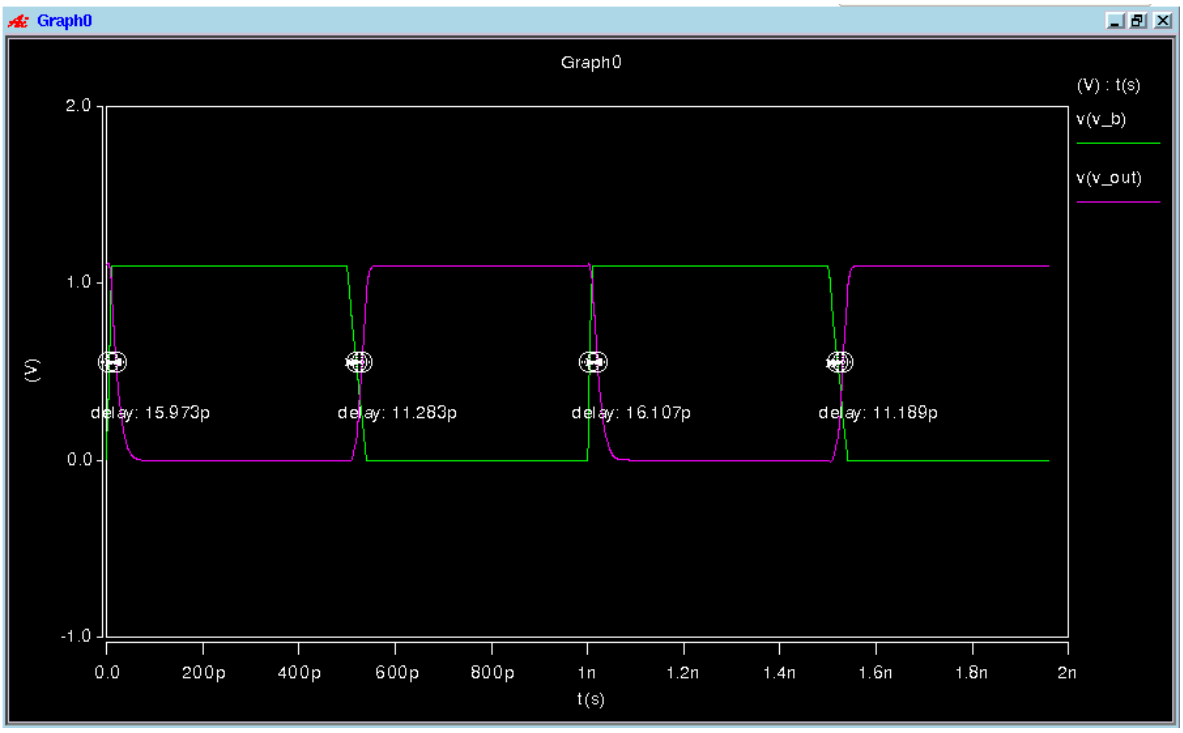

Figure 7: 10 → 11, 11 → 10 Transition Delay

3.4 Discussion

The results gathered in this lab demonstrate the correlation between transistor size, load capacitance, and how these attributes affect delay and power consumption. Looking at Table 1, as load capacitance was increased the rising delay decreased, the falling delay increased, and the power consumption increased. Table 2 shows a similar pattern, while Table 3 shows that both delays increased. Nonetheless, in all three cases, power consumption increased linearly as the load capacitance was incremented by factors of 2. Furthermore, it is clear from the data gathered that the functionality of the NAND gate is indeed correct.

3.5 Questions

1. **What input transitions will you expect to have the maximum rising or falling delay? Why? Do the experimental results match your expectations?** I expected 10 → 11, 11 → 10 to have the maximum delay. Depending on how the gates are positioned in the NAND gate, I expected when the transition depended on the transistor furthest from the output, there would be a maximum delay. The results showed that 01 → 11, 11 → 01 showed a maximum. This is because input A, or the first bit, was furthest from the output.

2. **Does the relationship between transistor sizes, load capacitances, and**

propagation delays follow the linear delay model? Yes. According to the data gathered in this lab, it can be concluded that this relationship follows the linear delay model.

3. **How does power consumptions change as transistor sizes and load capacitances change?** Power consumption increases

4. **Among dynamic power, static power, and short circuit power, what are measured in this lab?** Dynamic power is measured in this lab

4 Conclusions

Overall the lab was a success. A 2-input CMOS NAND gate was designed and simulated, and its delay and power consumption was measured. It can now be used in further labs and in other circuits that involve 2-input NAND gate functionality.