Lab 2: Op-Amp Circuit Imperfections

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ECE 311-03
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Lab Date: 9/26/14
Due Date: 10/10/14

1 Introduction

The purpose of this experiment is to explore offset, frequency response, maximum peak output voltage, rise-time, and slew rate limiting in Op-Amp circuits. The scope of this experiment involves specific Op-Amp configurations from the preliminary section of the lab.

2 Theory

Offset voltage is a practical concern in many configurations of Op-Amp circuits. It is the effect of having the output voltage being something other than the expected value of zero volts when the input terminals are both shorted. An ideal op-amp would output a value of zero volts if both inputs are grounded and shorted as well, however, in the real world, this is not the case. When expressing offset voltage, it can be expressed as a perfect op-amp with a small voltage being applied in series with one of the inputs to force the output voltage a certain direction. Offset voltage can introduce slight errors in any op-amp circuit, so it is critical to identify this effect in any op-amp circuit configuration.

An ideal op-amp has an infinite frequency response, meaning that it can amplify any frequency signal from DC to very high AC frequencies. However, real op-amps do not have an infinite gain or bandwidth, but they have something called Open Loop Gain. As the frequency increases, the output gain decreases until it hits unity.

When analyzing op-amp circuits, the rate at which the output voltage can change is often looked at. The limiting rate of change for the circuit is called its slew rate. These slew rates impose high-frequency limitations on the circuit, therefore, it is critical to recognize this rate.

3 Experimental Procedure

The equipment used in the lab was:

- Breadboard
- 3kΩ resistor
- 1kΩ resistor
- 100kΩ resistor
- $0.1p$F capacitor
- Oscilloscope with probe
- Power Supply
- Function Generator
- TI ua741 chip

The first circuit constructed was built from preliminary question 8 shown in Figure 5 and Figure 9 with an R_L of $2k\Omega$, and a phase voltage of $15V_{pp}$ was applied to the circuit. For R_2 = $10M\Omega$, R_1 and R were found. Then with $R = 0$, the value for R_1 was found. After this, R_2 was set to $10k\Omega$, and the previous two experiments were repeated. Once this was completed an offset null circuit was used to eliminate the offset voltage. This circuit is

shown in Figure 4. A $10k\Omega$ variable resistor was used in order to force the current $I = 0$.

Once this was completed, the circuit in Figure 1 was constructed to verify Figures 2 and 3. The $100pF$ capacitor was then removed and the slew rate was analyzed.

The last circuit constructed was from preliminary question 2 shown in Figure 10. The answers were verified, and then R_2 was chosen to obtain gains of $40dB$, $20dB$, and $0dB$. Data was taken up to a frequency of 1MHz.

4 Interpretation

Below are the results obtained from the first circuit constructed shown in Figure 5:

	R_2	R_1	R
Part a	$10M\Omega$	$1M\Omega$	$1M\Omega$
Part b	$10M\Omega$	$1M\Omega$	0Ω
Part c	$10k\Omega$	$1k\Omega$	$1k\Omega$

This data solidified that the values obtained in the preliminary question calculations were correct.

The results from the second circuit were similar to Figures 2 and 3. In Figure 3, it is apparent that the output voltage does not rise instantly. This is due to the slew-rate limitation. Figure 6 shows the waveform that was recorded.

The results from the same circuit with the capacitor removed are shown in Figure 7. It was found that this data did not have any slew-rate, which means that the input was equal to the output.

The results from the last circuit constructed are shown below.

Close Loop AV	**Frequency**	V_{in}	V_{out}	**Phase**
40	100kHz	230mV_{pp}	200mV_{pp}	-299ns
20	100kHz	115mV_{pp}	160mV_{pp}	-328ns
0	1MHz	130MV_{pp}	187mV_{pp}	-224ns

As shown in the table, a $100k\Omega$ resistor was used to obtain the gain of 40dB, a $9k\Omega$ resistor was used for the gain of 20dB, and for the gain of 0dB, a buffered circuit was constructed.

5 Conclusion

Overall the results from this experiment were a success. The goal was to observe the different types of imperfections encountered with op-amp circuits. For each circuit constructed, these imperfections were correctly identified and analyzed.

6 Appendix

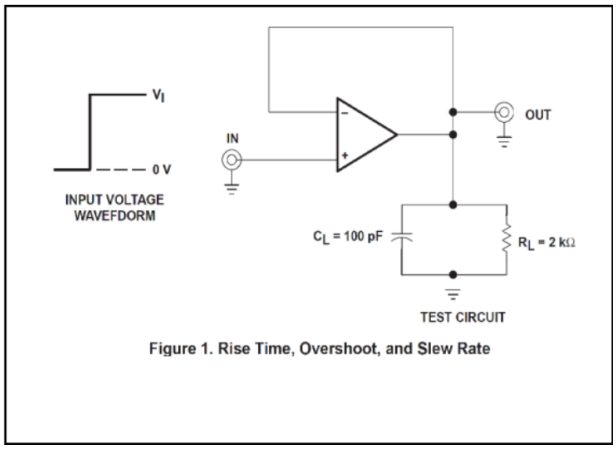

Figure 1: Second circuit Constructed

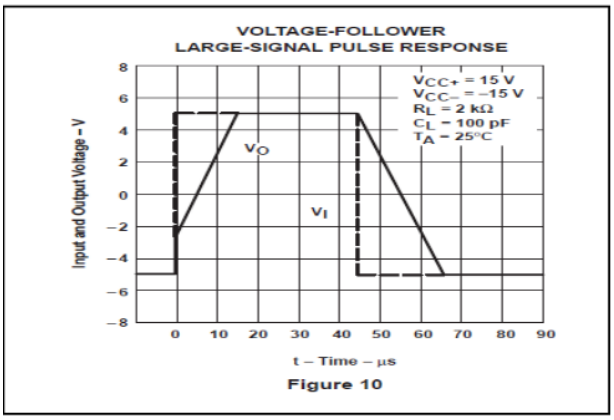

Figure 3:

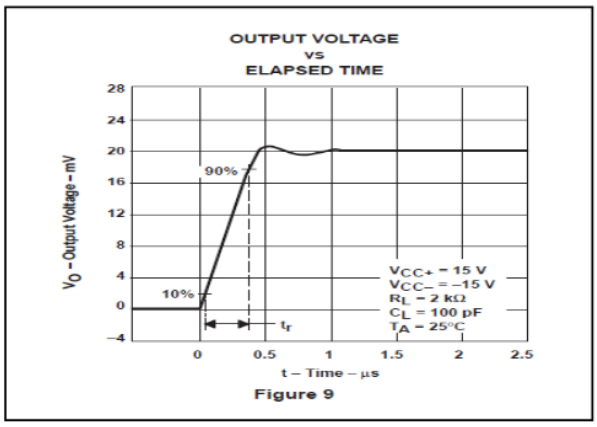

Figure 2:

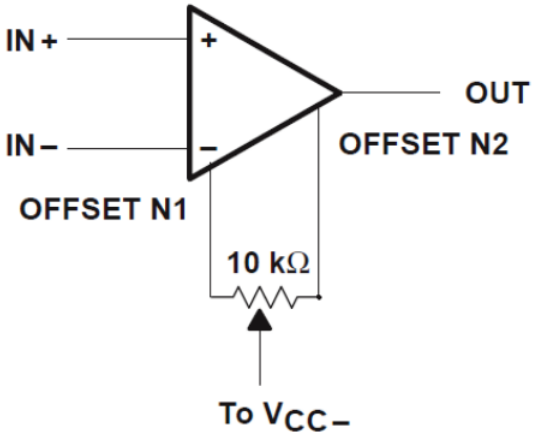

Figure 4: Null Offset Circuit

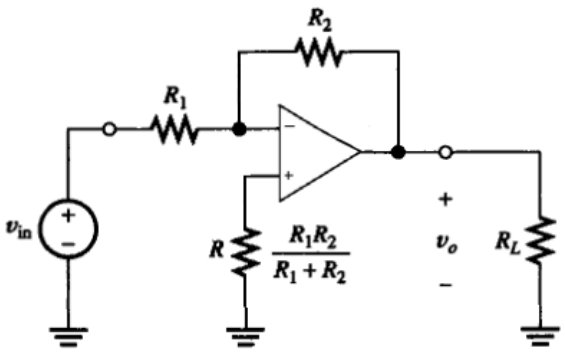

Figure 5: First circuit constructed

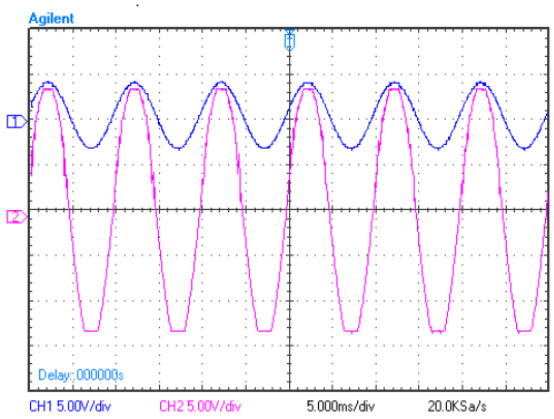

Figure 6: Prelim 2 Waveform

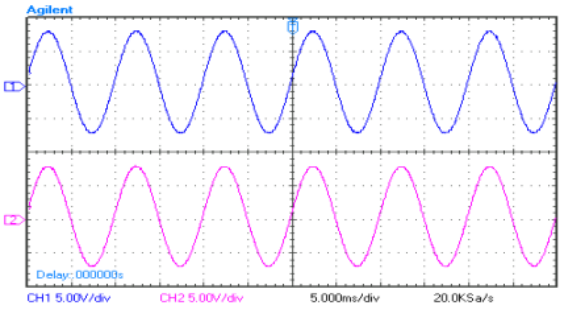

Figure 7: Prelim Five Waveform

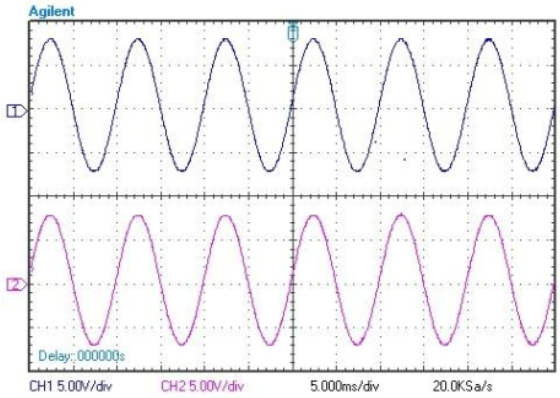

Figure 8: Prelim Three Waveform

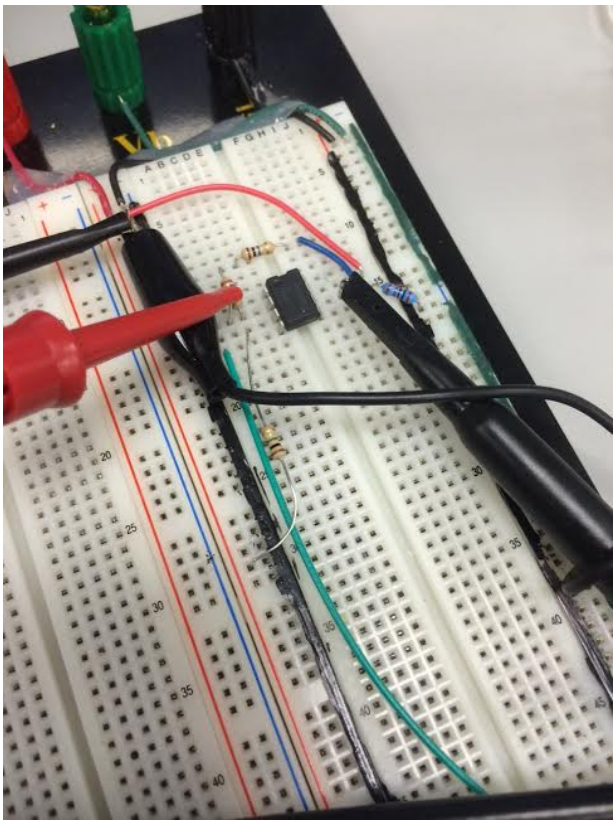

Figure 9: Circuit Construction

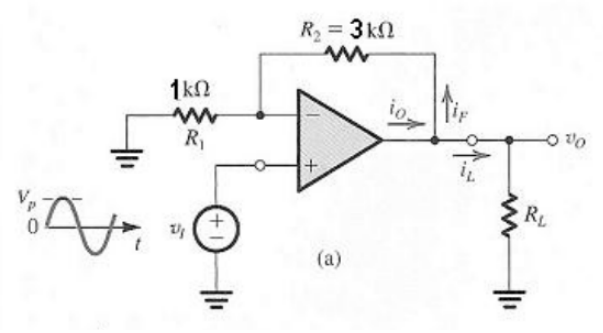

Figure 10: Prelim 2 Circuit