Lab 5: Hierarchial Design and Formal Verification

Adam Sumner

Illinois Insititute of Technology

ECE 429-01

Lab Date: October 14th, 2015 **Due Date:** October 21st, 2015

1 Introduction

The purpose of this lab is to introduce the student to hierarchal design and formal verification techniques that are essential when constructing complex circuits. A layout for a 2-input NAND gate will be built, and then a 2 input AND gate will be constructed using the schematics built from previous labs.

2 Theory/Pre-Lab

2.1 Theory

Since chip fabrication can be incredibly costly, it is a must to verify that the design will work correctly before sending it out for tapeout. Verifying functionality is one of the many important tasks that validates the success of a specific chip's design. While it is possible to give specific input to validate the functionality, there could potentially be a high number of inputs, producing hundreds of possibilities for output. Manual verification can become tedious and a waste of time. To resolve this issue, formal verification techniques have been proposed which can provide evidence for the functional correctness of a design. One such methodology is called equivalence checking. This technique takes two designs and verifies that both designs operate with the same functionality. LVS is one example of equivalence checking, as it shows where the layout is exactly the same as the schematic, while other factors such as transistor size are also verified. Because circuit designs can become complex, it's necessary to specify designs at a higher abstraction level. Due to the fact that the design in this lab is digital, boolean logic can be used for verification.

2.2 Pre-Lab

A stick diagram for a 2-input static CMOS NAND gate and a 2-input AND gate design were both sketched. They are shown in Figures 1 and 2.

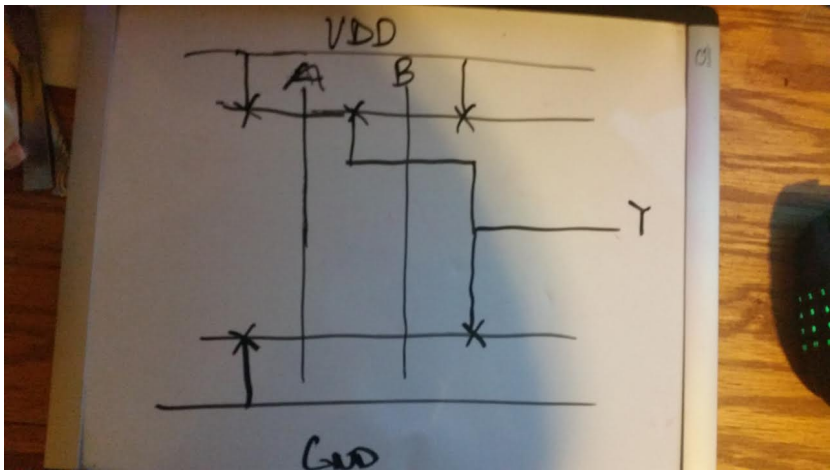

Figure 1: Stick Digram for Static CMOS 2-input NAND Gate

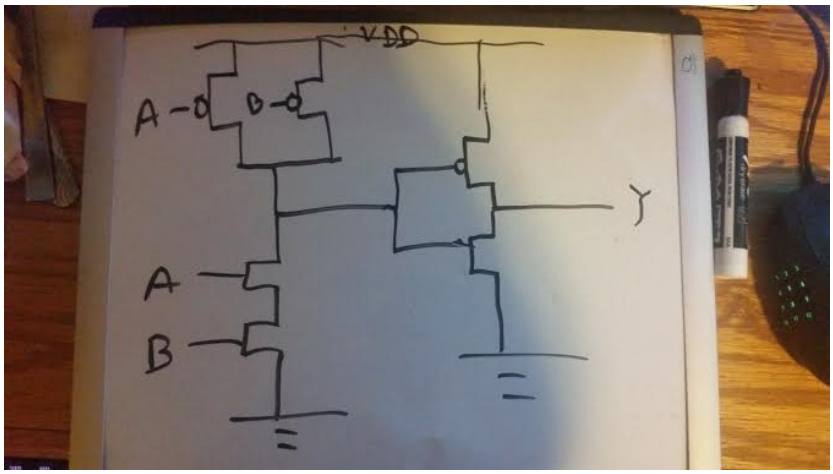

Figure 2: 2-input AND Gate Design

3 Implementation

3.1 Schematics

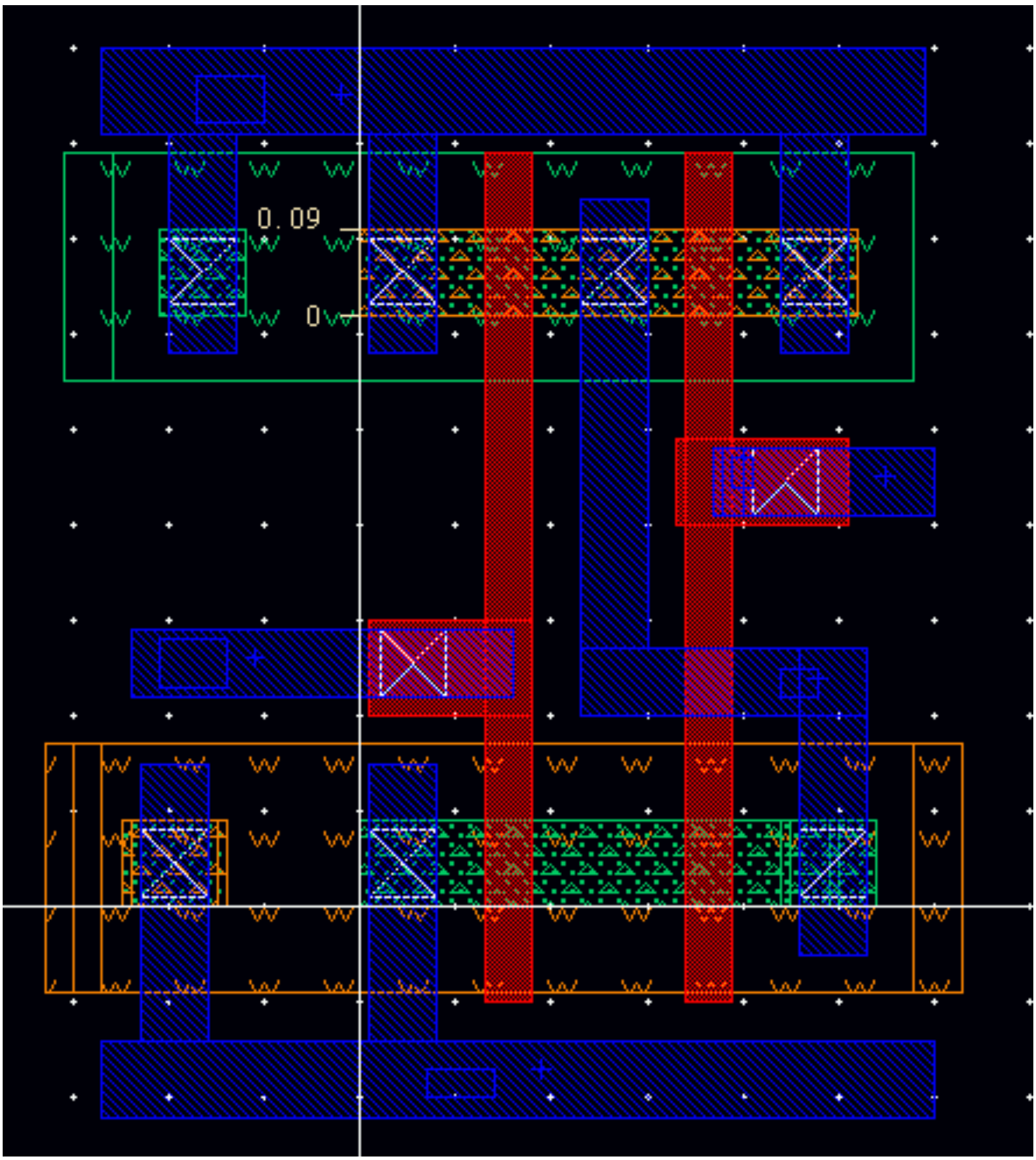

Figure 3: 2-input NAND Gate Layout

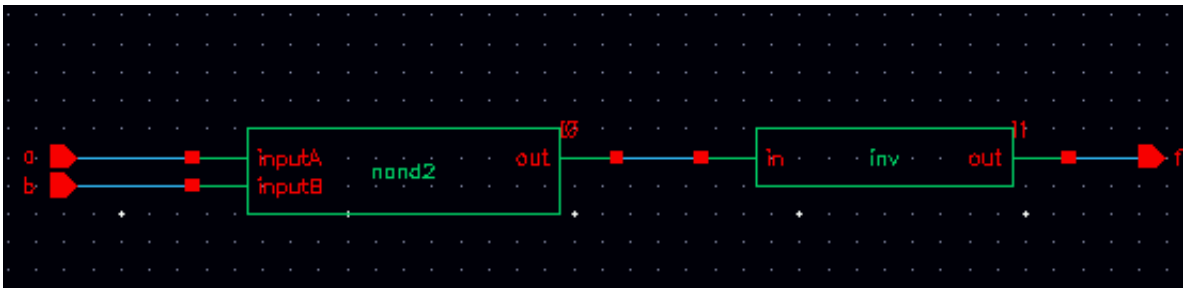

Figure 4: 2-input And Gate Schematic

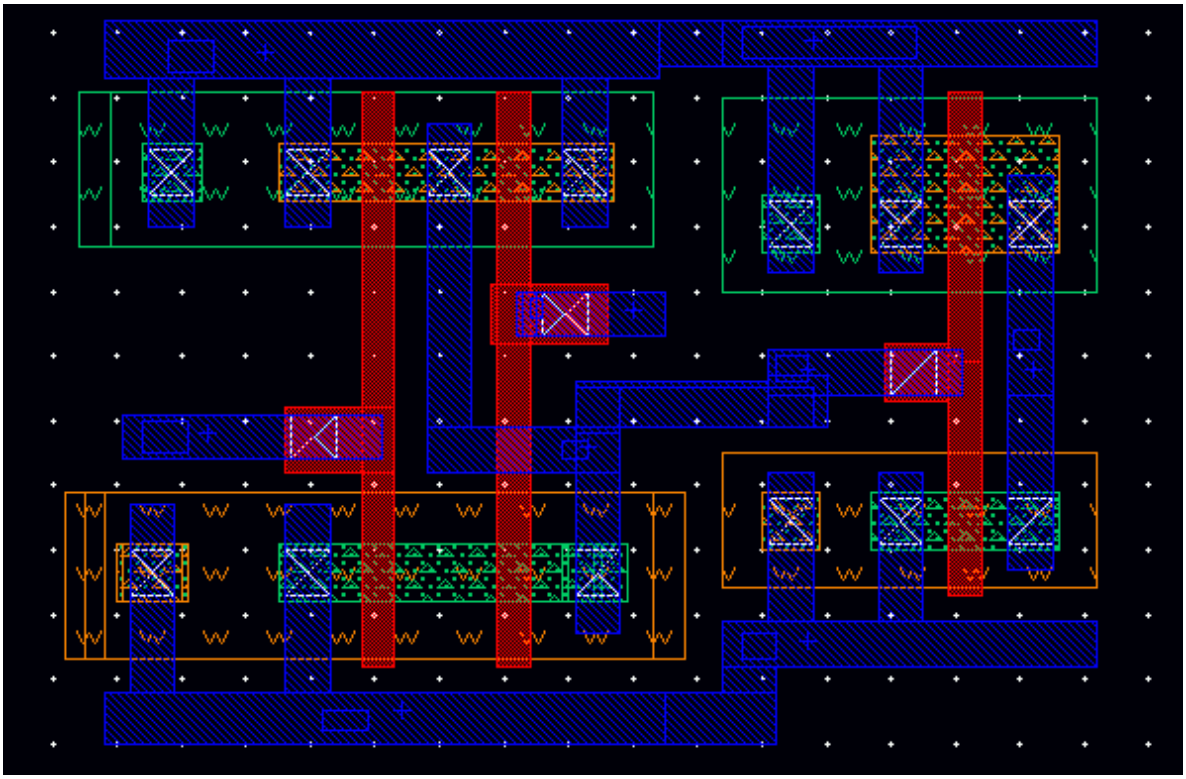

Figure 5: 2-input AND Gate Layout

3.2 Procedure

A NAND gate layout was created in Virtuoso and was verified using LVS. After this, a 2-input AND gate was designed using both the schematic and layout view. This was then verified using LVS, and it was also verified against the verilog model. Delay was then calculated for the AND gate design.

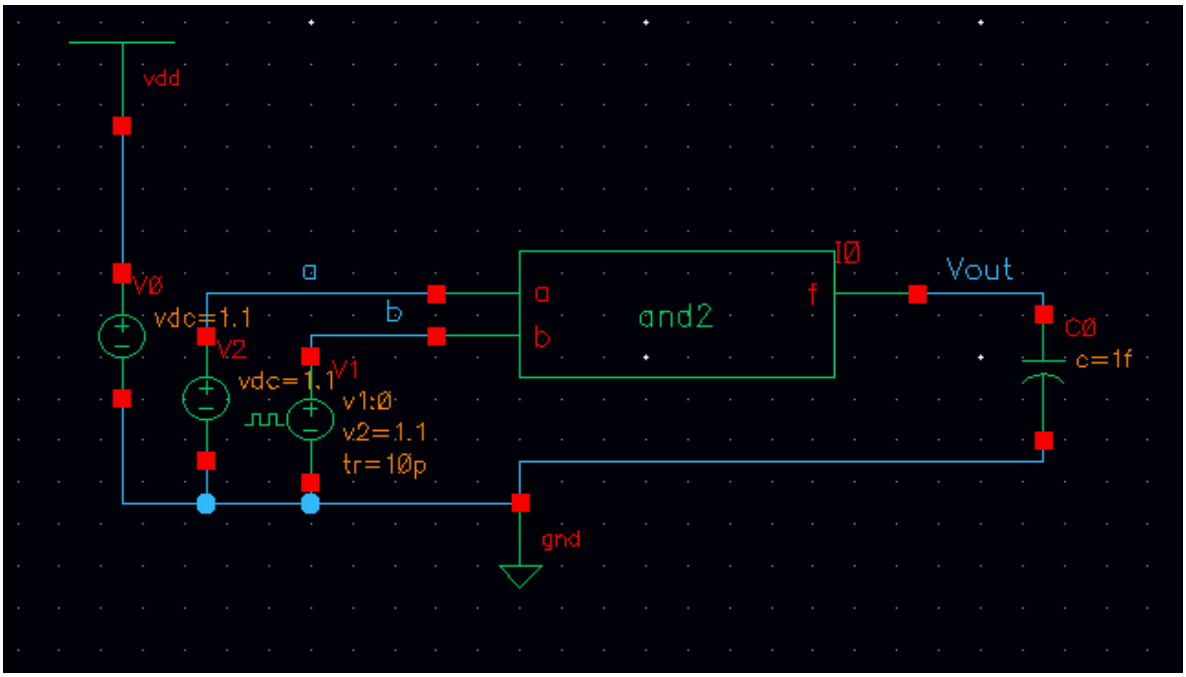

Figure 6: Test Circuit for 2-input AND Gate

3.3 Results

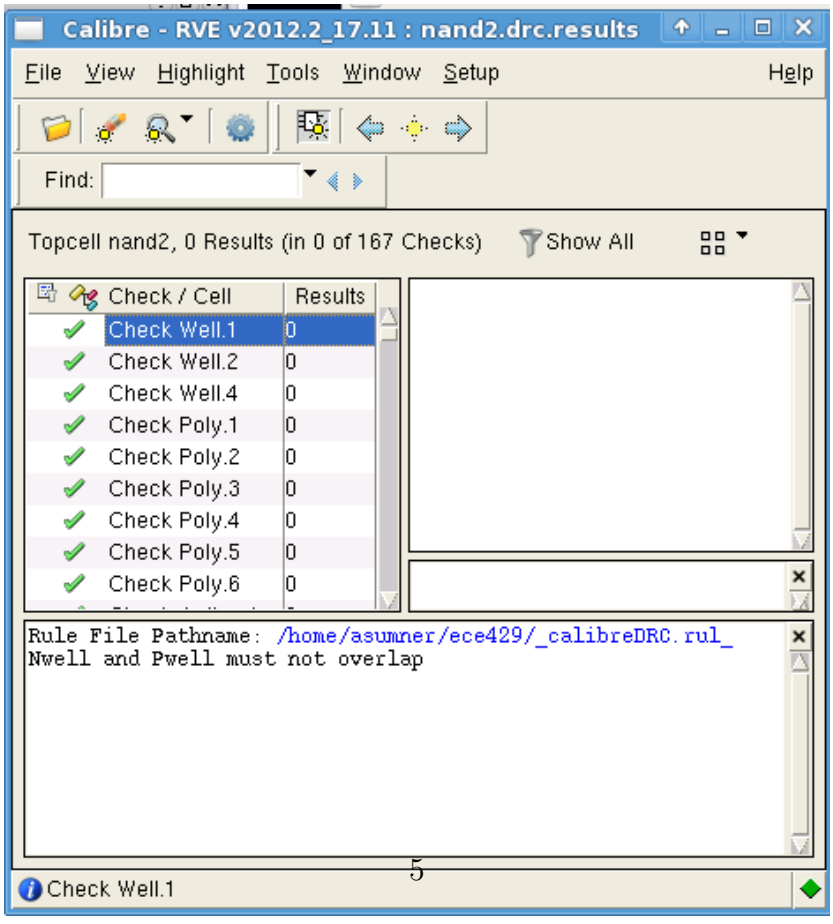

Figure 7: 2-input NAND Gate DRC Results

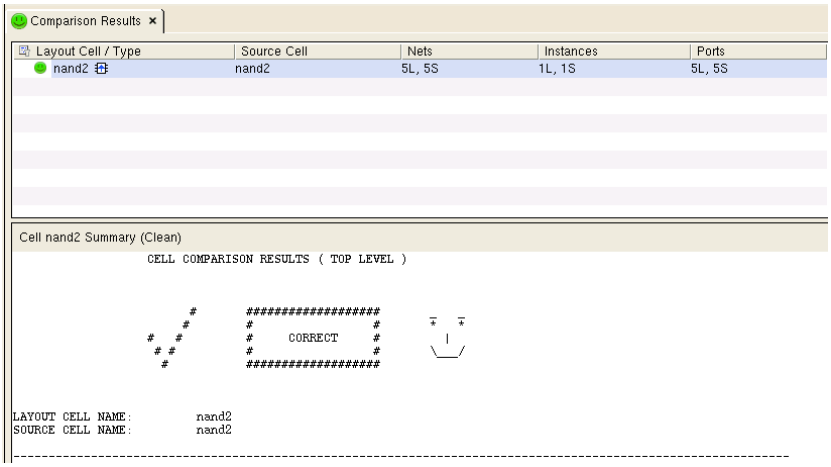

Figure 8: 2-input NAND Gate LVS Results

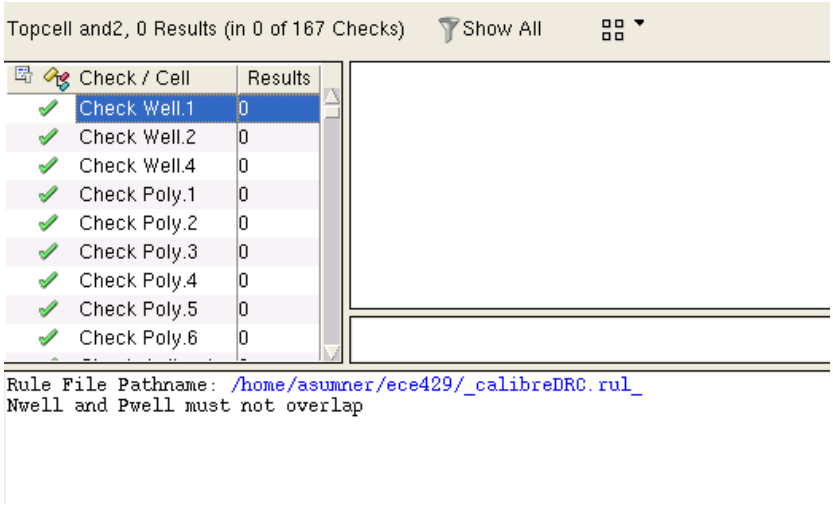

Figure 9: 2-input AND Gate DRC Results

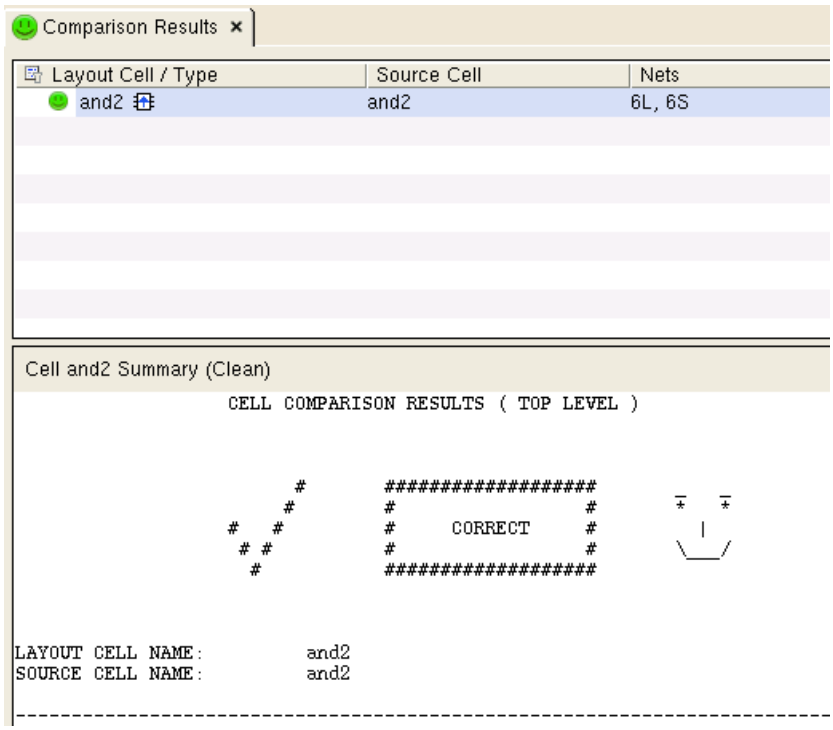

Figure 10: 2-input AND Gate LVS Results

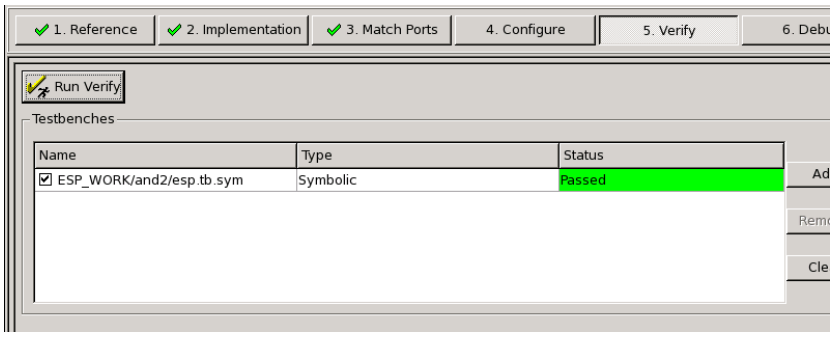

Figure 11: Verilog Equivalence Validated

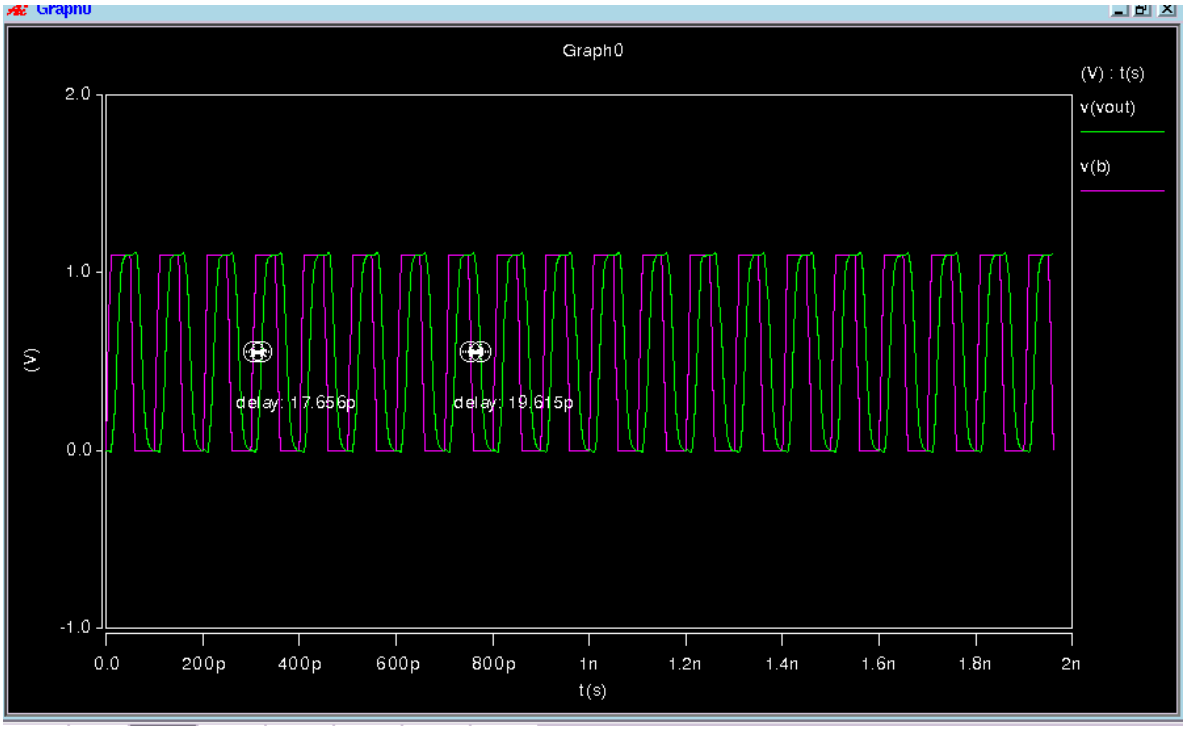

Figure 12: 10 → 11 Delay Measurements

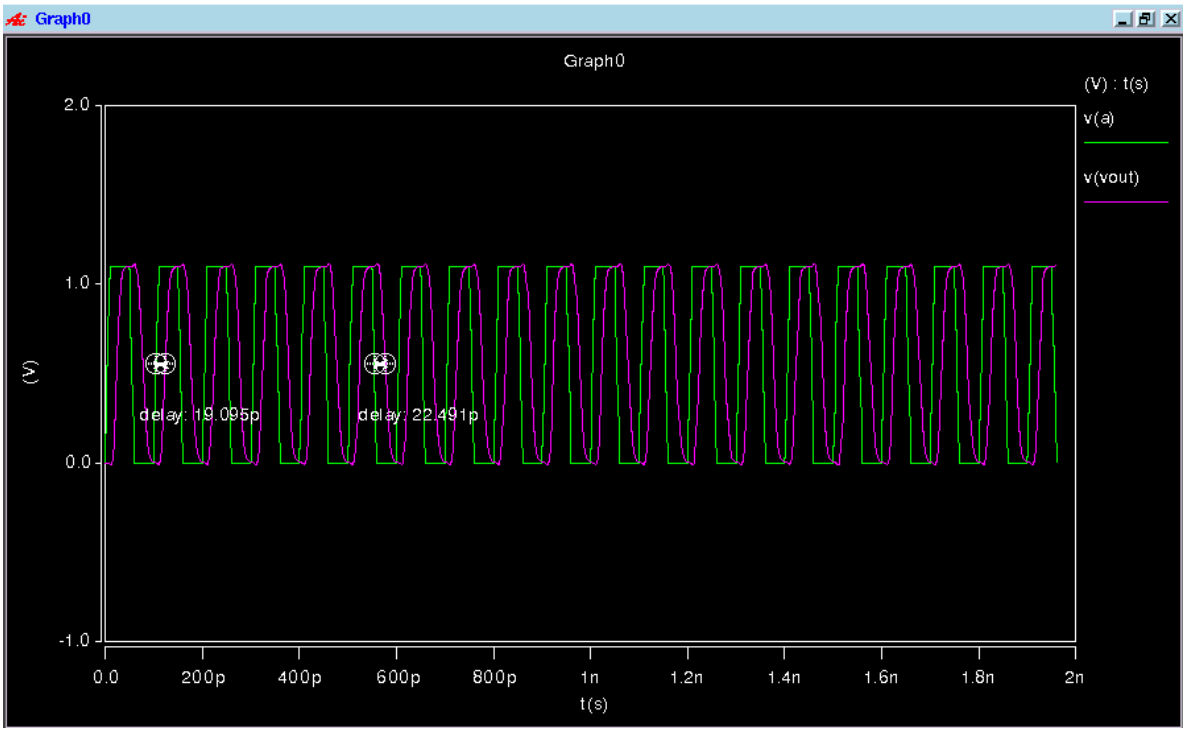

Figure 13: 01 → 11 Delay Measurements

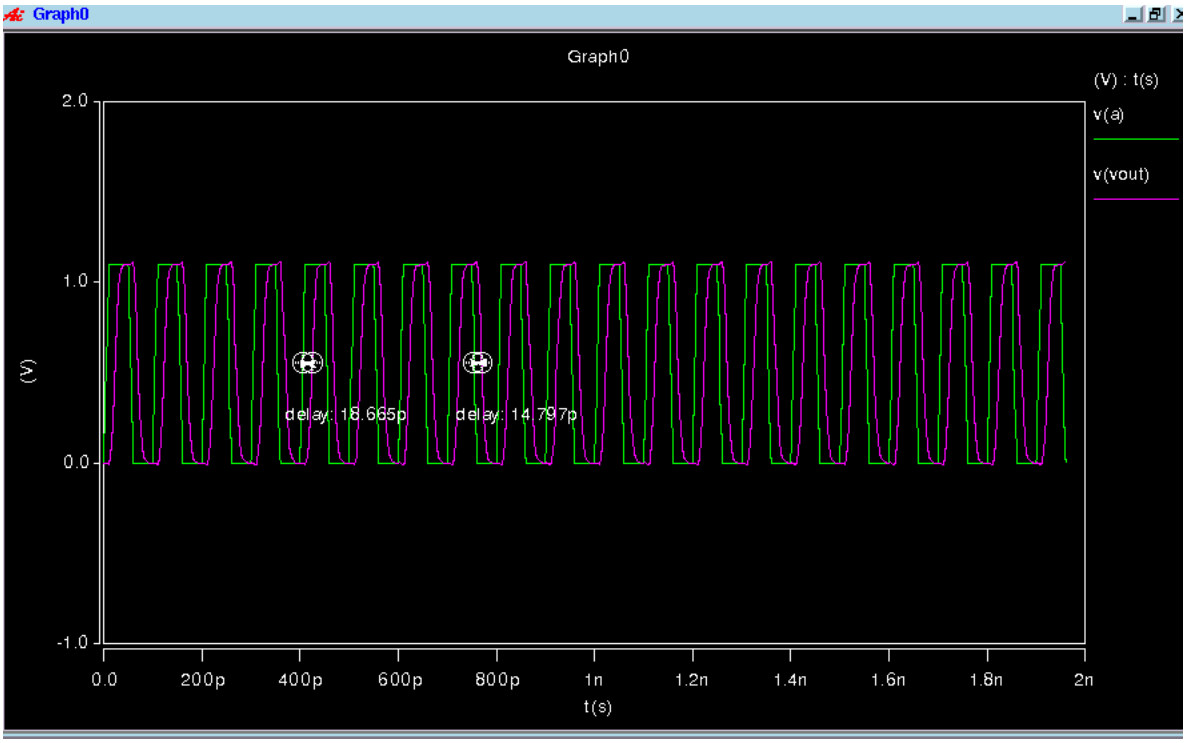

Figure 14: 00 → 11 Delay Measurements

w=90nm l=50nm	Transition		
	10→11	01→11	00→11
Rising Propogation Delay	17.656e-12 s	19.095e-12 s	18.665e-11 s
Falling Propogation Delay	19.615e-11 s	22.491e-11 s	14.797e-11 s
Average Power Consumption	3.17-05 W	3.26e-05 W	3.23e-05 W

Table 1: Delay and Power Consumption of Each Excition with 1f Load Capacitance

3.4 Discussion

3.5 Questions

4 Conclusions