ECE 429 Laboratory 3
Inverter Layout

Announcements:

1. **Teaching Assistants**
   Lab-1: Yunlong Zhang (yzhan167@hawk.iit.edu), Office Hours: 11:30 AM. - 1:30 PM. at SH309 on Mondays
   Lab-2: Shuai Li (sli97@hawk.iit.edu), Office Hours: 11:30 - 1:30 PM. at SH309 on Fridays

2. **Time Frame for Lab-03**

- In-Class students
  - ECE-429-01 (every Monday 1:50 - 4:30 PM.) -09/28/2015
  - ECE-429-02 (every Wednesday 6:25 - 9:05 PM.) -09/23/2015
  - ECE-429-03 (every Friday 1:50 - 4:30 PM.) -09/25/2015
- Internet Students
  - Every Monday (Report due: every Monday at 4:30 PM.)

3. **Account Administrator**
   If you have account issues or remote access problems, please contact Mr. Upendra Gandhi (support@ece.iit.edu).

1. Introduction

Layout design is the “grunt work” of VLSI design since it involves deciding where layout objects will actually be placed to create a circuit design. Chip designers often refer to layout design as “polygon pushing”. However, although it is unloved, layout design is a crucial part of the chip design process. For this reason, we will spend a significant amount of time learning to do layout in the lab.

The purpose of this lab is to gain experience creating layouts within an industrial setting. We stay in the popular Cadence Virtuoso platform to complete the various tasks for layout and layout verification. Since the FreePDK45 library follows industrial practices to specify layout design rules in microns, we heavily rely on the Calibre toolset from Mentor Graphics to check for design rule violations during the layout process. Later on, Calibre is also used for layout verification and parasitic extraction. Finally, we will

perform post-layout simulation by Synopsys HSPICE using the extracted parasitics.

The Tutorial II: Inverter Layout posted on the Blackboard will guide you through the lab.

2. Layout and Layout Verification

2.1 Layout Editor

The underlying idea of a layout editor is something like that of a painting program, where individual pixels are assigned colors by painting operations. However, in a layout editor the “pixels” are actually “grid points” - rectangular areas that are defined by the manufacturing grid, and paint operations assign rectangular regions of grid points to layers that represent rectangular layout objects: rectangles of polysilicon, diffusion, metal, and contacts/vias between layers.

Since the FreePDK45 library uses a minimum manufacturing grid of 2.5nm, the corresponding minimum pixels are 2.5nm square. Such minimum grid size is preferred by experienced layout designers since less silicon area will be wasted for smaller sizes. However, it would require much more time to fine-tuning the layout. Therefore, in Tutorial II, we use a size of 10nm to simplify the layout process as silicon area is not a major concern for our labs.

One usual confusion about layout drawing is how to draw a piece of wire that turns and branches. The answer is that since rectangles of the same layer are connected as long as their borders touch or their areas overlap, you can draw the wire as multiple rectangles. Note that at small grid sizes, you don’t need to make such connections deliberately - the design rule checking (DRC) will catch all small vacant spaces between rectangles at the same layer.

2.2 Layout Design

Keep in mind that we will reuse the layouts we created in subsequent labs. Therefore, it is important to follow a certain methodology to design these cells properly. The following is the methodology we are going to use:

- Keep VDD on top of your cell and GND on the bottom of your cell.
- All inputs ports should enter into the left hand side of the cell.
- All output ports should leave the right side of the cell.
- Use only poly and metal1 to route signals.
- Do not forget the well taps.
- Try to place the input and output ports at the same height in each layout. Try in general to create your layouts of the same height and the input and output ports at

the same location in each file. Our goal here is to be able to use some of these cells together in conjunction. Having your input and output ports at the same height in your layout will enable you to have your input and output ports lined up and connected together, similar to a puzzle.

2.3 Design Rule Checking (DRC)

Layout design rules, or simply design rules, are the rules you must follow to draw a layout for a specific technology. The FreePDK45 design rules can be found at http://www.eda.ncsu.edu/wiki/FreePDK45: Contents. Similar to industrial design rules, the FreePDK45 design rules are specified in microns. It is obviously too complicated for one to memorize. Moreover, such complicated rules will make corrections at the end of the layout process almost impossible. Therefore, it is a common practice for modern layout design to perform design rule checking (DRC) frequently during the layout process such that the violations can be detected and corrected as soon as possible.

The DRC tool we are going to use is part of the Calibre toolset from Mentor Graphics. Integrated with the Virtuoso platform, Calibre DRC allows the designers to locate and correct violations interactively, which is very convenient.

2.4 Layout vs. Schematic (LVS)

Layout is lots of fun once you get familiar with the tools. However, it is hard to guarantee that the circuit you draw will be the one you want. Therefore, there must be some way of verifying whether the circuit you just made as a layout is the same as the schematic you desire. This process of checking your layout to your schematic is called Layout vs. Schematic (LVS). Most layout tools will always have some way of performing LVS.

In this lab, we will accomplish verification through Calibre LVS. Calibre LVS will extract a SPICE netlist from the layout view of your inverter cell and generate another SPICE netlist from the schematic view. The two SPICE netlists are then compared to see if they have the same set of transistors and the same connections between transistors. If the circuits are the same, you will see the famous smiley face. Otherwise, discrepancies are shown interactively so that you can quickly locate the problems.

2.5 Post-Layout Simulation

With all the information available from the layout, we have better chance to predict its actual behavior in the real world because all layout-related parasitics can be considered in simulation. We will first use Calibre PEX to extract parasitic capacitances from the layout and then use HSPICE to simulate the circuit consisting of both transistors

and parasitics, which is usually known as post-layout simulation.

3. Preparing for the Laboratory (Pre-Lab)

Please make sure you have the following prepared before you come to lab.

- FreePDK45 is a twin-well process. Learn more details from Chapter 3.2.3.
- Study the FreePDK45 design rules at http://www.eda.ncsu.edu/wiki/FreePDK45: Contents. You don't need to memorize them but you need to know where to find the rules related to specific layers.
- Familiarize yourself with Tutorial II: Inverter Layout.
- You may notice that your virtuoso window looks different from the snapshots in the tutorial, because we are using the latest version of the tool. For most part, we can do exactly as stated in the tutorial. The major different is that the LSW (layer Selection Window) is now embedded in the layout window, while the window options are the same.
- In step 3(a) Create Pins, in the terminal name display window, please select "metal1 drw", because there is no "metal1 dg" available.
- In step 4(b) Post-Layout Simulation, when you modify the line starting with "xi0 vin ……" in "lab3.sp", please make sure that the order of the pin signals are the same as that of "inv.pex.netlist". Otherwise, the simulation results will be incorrect because of wrong connection of the inverter.

4. Lab Instructions

Create the layout of an inverter in Virtuoso. The layout should be stored in the layout view of the inverter cell you created in Lab 2 so that it can be reused in this and later labs.

Make sure your layout passes LVS.

Perform a post-layout simulation after parasitic extraction. Measure the rising and falling delays of your inverter layout.

5. Deliverables

The requirement of the lab/project reports with a template can be found on the Blackboard. NEVER share your writings/screenshots with others. We prefer to receive reports electronically as either .pdf or .doc files through the Assignments section on the Blackboard.

Follow the template for lab/project reports posted on the Blackboard to structure your lab report. Briefly describe the tasks you have accomplished. Discuss your lab by addressing at least the following questions.

- What determines the minimum transistor width and length for a specific technology?
- Why should well-taps connect to implanted regions instead of the wells directly?
- What are the benefits of a twin-well process?
- How do the delays of your inverter layout compare to that of the schematic in Lab2? Do you expect them to be larger or smaller? Why?

Finally, attach screenshots of your inverter layout, LVS report (the smiley face), and delay measurement as the appendix.