ECE 429 HW#1

Fall 2015

(Due Date: Sept. 21th, Monday, 10:00 am in LS113)

Homework Policy: Homework is due at the start of class. Late homework will not be accepted. Working together on homework is encouraged, but *copying assignments will call for disciplinary action*.

Note: For internet students, please upload your hoemwork in pdf or word format in the 'Digital Dropbox' in Blackboard before the due date. TA will check the submission date.

1. Explain the following terminologies briefly.

   A. Moore's Law
   B. Feature Size
   C. VLSI Design for Power
   D. VLSI Design for Manufacturing
   E. ASIC
   F. Logical Synthesis
   G. Physical Synthesis
   H. Dynamic Power and Leakage Power
   I. Conduction Band
   J. Valence Band
   K. Velocity Saturation
   L. Subthreshold Conduction
   M. Hot Carriers
   N. MOSFET Operational Regions

2. Solve Exercise 1.5 (p57 in the Textbook)
3. Solve Exercise 1.6 (p57 in the Textbook)
4. Solve Exercise 1.10 (p58 in the Textbook)
5. Solve Exercise 2.2 (p95 in the Textbook)
6. Solve Exercise 2.3 (p95 in the Textbook)
7. Solve Exercise 2.7 (p96 in the Textbook)
8. Solve Exercise 2.9 (p96 in the Textbook)

9. A light in a long hallway is to be controlled by three switches A, B, and C. If the switch is up, its logic value is 1. If an odd number of switches are up, the light is on; if an even number, the light is off. Design the logic circuit for *F (F=1 for light on)* from A, B, and C:
   A. As an all-NAND circuit
   B. As an all-NOR circuit

10. Consider the design of a CMOS compound gate computing $Y=\overline{(A+B+C)\cdot D}$

    a) Design a transistor-level circuit
    b) Draw a stick diagram
    c) Estimate the cell width and height in terms of the number of metal tracks