

LAB 2: INVERTER SCHEMATIC

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ECE 429-01

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1 Introduction

The purpose of this lab is to introduce the student to the various tools that will be used throughout the semester. The student will design a schematic of a CMOS inverter, create the inverter in Virtuoso, and test the correctness of the design using HSPICE.

2 Theory/Pre-Lab

2.1 Theory

Due to the costly nature of manufacturing VLSI chips and the difficulty of testing devices on the nanoscale level, a majority of VLSI design work is done using computers and simulation software. Designers rely heavily on CAD techniques to validate their designs before the designs are pushed into production. The Cadence Virtuoso platform is one of the most widely used commercial electronic design automation platform that supports custom IC designs. It serves as a central point for design entry, and it also provides various interfaces for use with other EDA tools. Throughout this lab, the FreePDK45 library, which supports a 45 nm process derived from the Predictive Technology Model, will be used.

Complementary MOSFET or CMOS technology is widely used in industry today. Devices ranging from Cell phones to CPU's all utilize CMOS due to its advantages over pure NMOS or pure PMOS designs. CMOS offers devices low power dissipation, relatively high speed, and high noise margins in both states. The most basic logic gate that can be implemented using CMOS is an inverter. This involves the use of only 2 MOSFETs, one PMOS type and one NMOS type. Figure 1 shows the layout of a CMOS inverter.

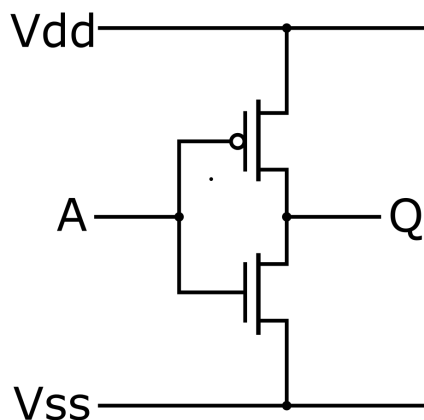


Figure 1: CMOS Inverter Schematic

2.2 Pre-Lab

The pre-lab involved a refreshment of the various SPICE netlists, an overview of Tutorial I: Inverter Schematic and Simulation, and the creation of a schematic for a static CMOS inverter with power sources connected. The drawn schematic is shown below:

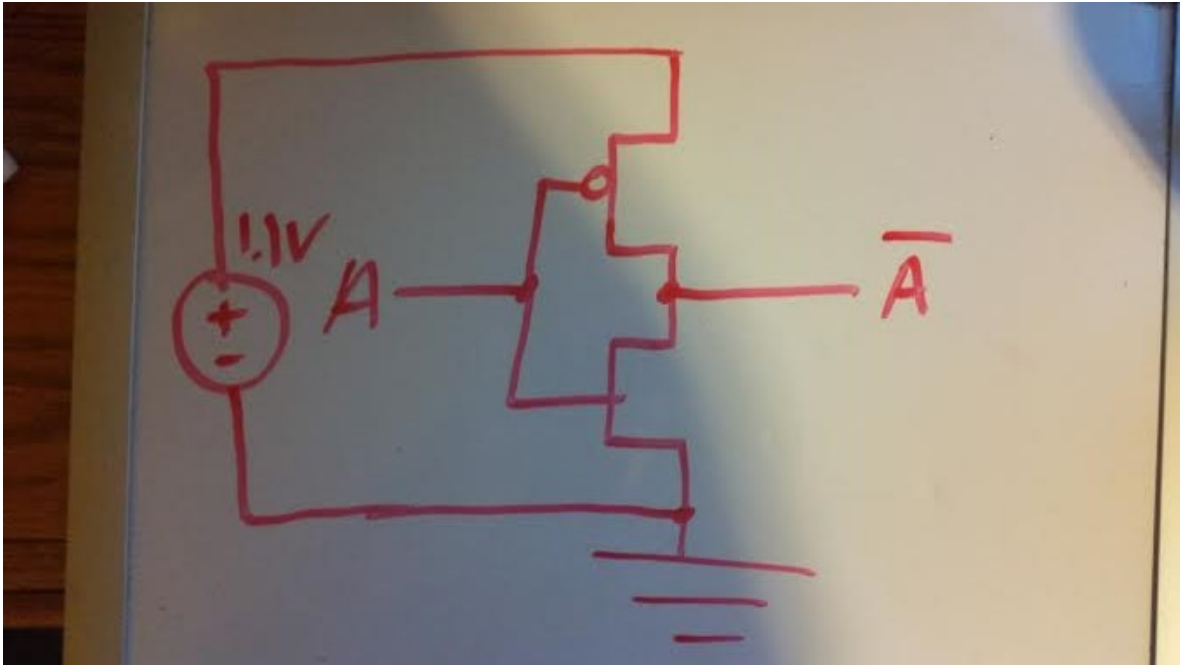


Figure 2: Static CMOS Inverter with Power Source

3 Implementation

4 Conclusions