Homework 1

Adam Sumner
ECE 429

September 21st, 2015

1 Explain the Following Terminologies Briefly

- **Moore's Law** - The observation that the number of transistors in dense integrated circuits has doubled approximately every two years. Named after Gordan E. Moore
- **Feature Size** - The minimum dimension of a transistor that can be reliably built
- **VLSI Design for Power** - Discipline of design that aims to reduce power dissipations while maintaining adequate throughput rate
- **VLSI Design for Manufacturing** - Discipline of design that aims to produce a product in a timely manner with sufficient yield to be profitable
- **ASIC** - Application-Specific Integrated Circuit. An integrated circuit customized for a particular use, rather than general-purpose use
- **Logical Synthesis** - Process by which an abstract from of circuit behavior (usually represented at RTL) is turned into a design implementation
- **Physical Synthesis** - Step in the design cycle that converts circuit representations of components into geometric representations of shapes which, when they are manufactured in their corresponding layers, will ensure the correct functionality
- **Dynamic Power and Leakage Power** - The power consumed during the switching of a transistor, and the power lost to leakage current of transistors
- **Conduction Band** - The lowest range of vacant electronic states. Determines conductivity of the solid
- **Valence Band** - The highest range of electron energies in which electrons are normally present at absolute zero. Determines conductivity of the solid
- **Velocity Saturation** - Sate of a semiconductor when the carrier velocity reaches a maximum value
- **Subthreshold Conduction** - The current between the source and drain of a MOSFET when the transistor is in the subthreshold region

- **Hot Carriers** - Electrons in a solid-state electronic device that gains sufficient kinetic energy to overcome a potential barrier in order to break an interface state
- **MOSFET Operation Regions** - Three separate modes of a MOSFET depending on the voltage at the terminals: Cutoff, Triode, and Saturation

2 Exercise 1.5

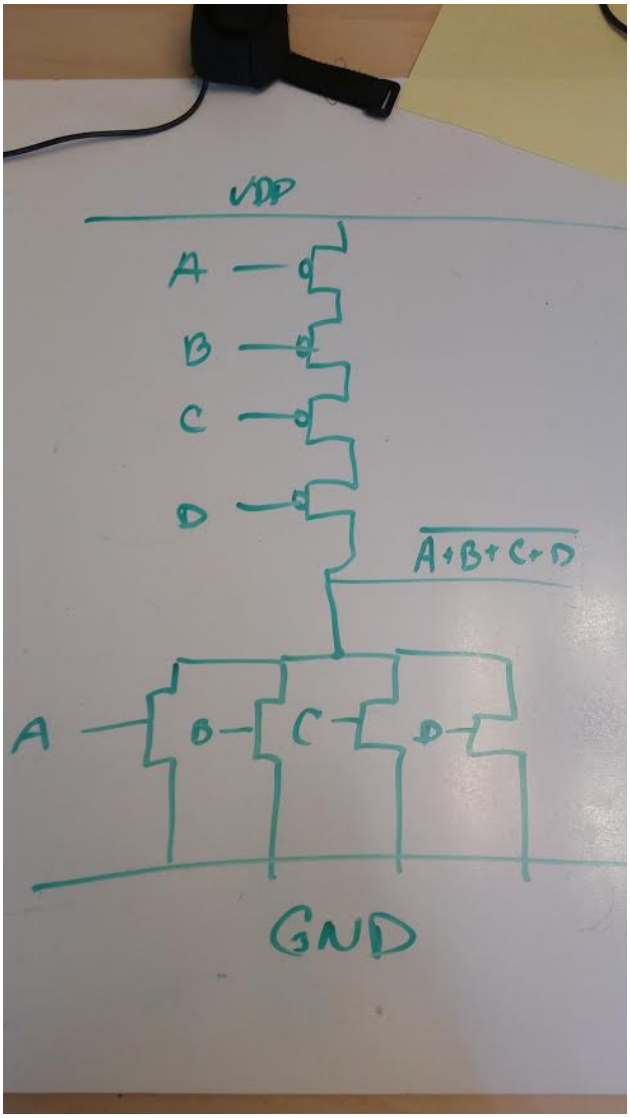

Figure 1: 4 Input NOR Gate

3 Exercise 1.3

a)

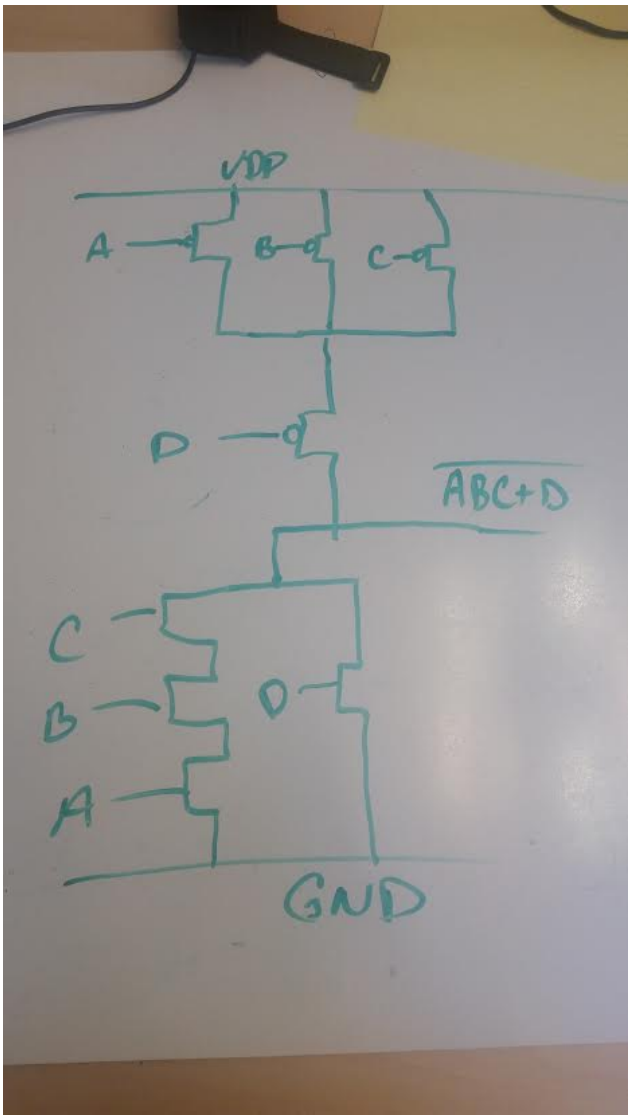

Figure 2: $\overline{ABC + D}$

b)

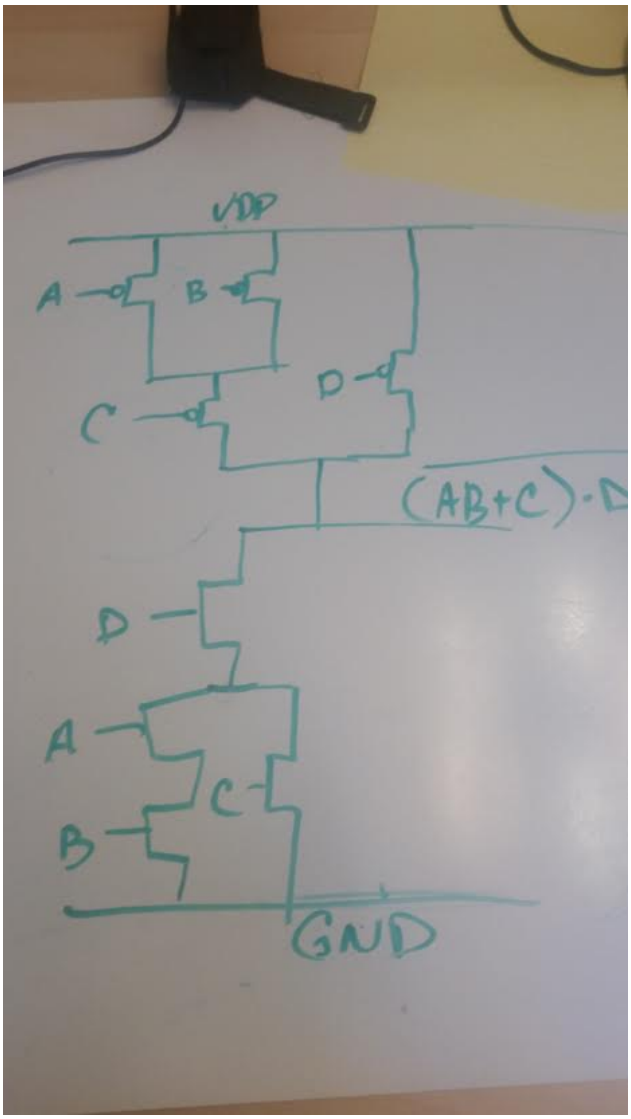

Figure 3: $\overline{(AB + C) \cdot D}$

c)

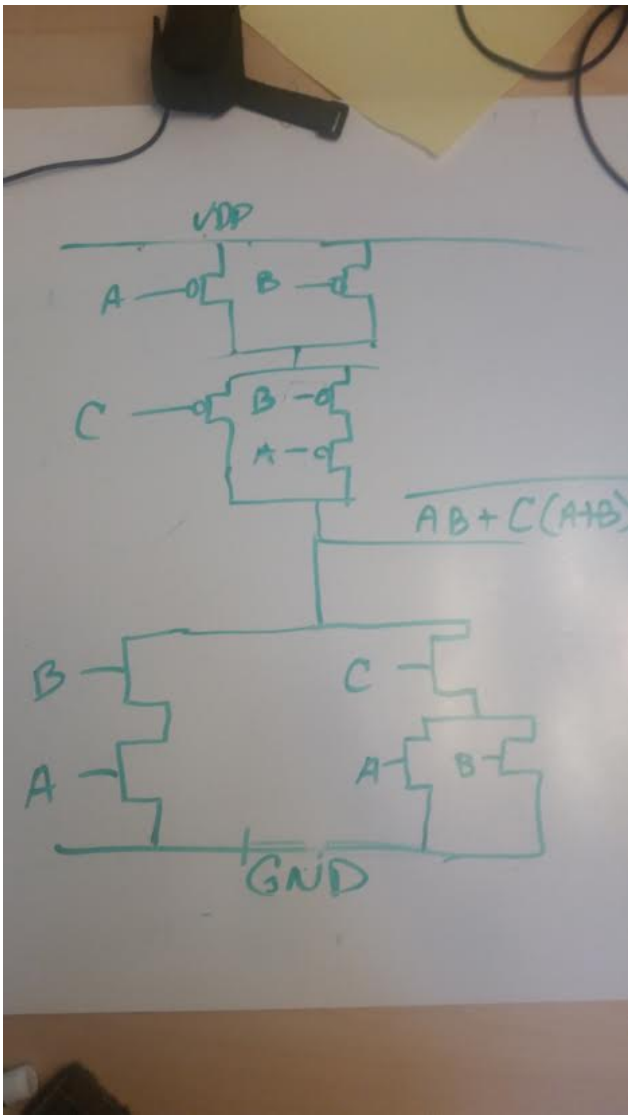

Figure 4: $\overline{AB + C(A + B)}$

4 Exercise 1.10

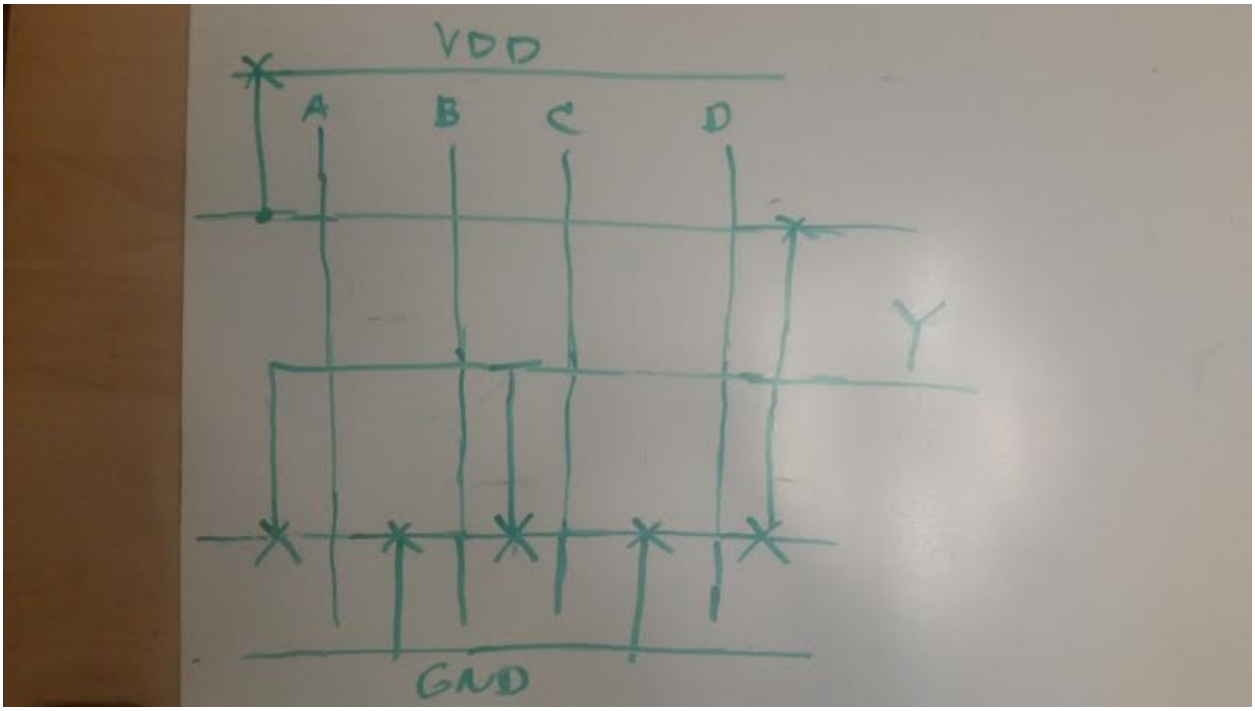

Figure 5: Stick Diagram for 4 Input NOR Gate

5 Exercise 2.2

Shockley Equation:

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{Cutoff} \\ \mu C_{ox} \frac{W}{L}(V_{GT} - 0.5V_{ds})V_{ds} & V_{ds} < V_{dsat} \quad \text{Linear} \\ \mu C_{ox} \frac{W}{2L} V_{GT}^2 & V_{ds} > V_{dsat} \quad \text{Saturation} \end{cases}$$

Assuming the linear region, the current through the bottom transistor is:

$$\begin{aligned} I_{ds2} &= \mu C_{ox} \frac{W}{L}(V_{GT} - 0.5V_{ds})V_{ds} \\ &= \mu C_{ox} \frac{W}{L}(V_{DD} - V_t - 0.5V_1)V_1 \end{aligned}$$

The current through the top transistor is:

$$\begin{aligned} I_{ds2} &= \mu C_{ox} \frac{W}{L}(V_{GT} - 0.5V_{ds})V_{ds} \\ &= \mu C_{ox} \frac{W}{L}(V_{DD} - V_1 - V_t - 0.5(V_{ds} - V_1))(V_{ds} - V_1) \end{aligned}$$

Solving for V_1, where V_1 is the voltage between the top and bottom transistors, we can obtain a quadratic expression:

$$\begin{aligned}
\mu C_{ox}\frac{W}{L}(V_{DD}-V_t-0.5V_1)V_1 &= \mu C_{ox}\frac{W}{L}(V_{DD}-V_1-V_t-0.5(V_{ds}-V_1))(V_{ds}-V_1)\\
(V_{DD}-V_t-0.5V_1)V_1 &= (V_{DD}-V_1-V_t-0.5(V_{ds}-V_1))(V_{ds}-V_1)\\
(V_{DD}-V_t)V_1-0.5V_1^2 &= (V_{DD}-V_t-0.5V_{ds})+0.5V_1^2-V_1(V_{DD}-V_T)\\
0 &= V_1^2-2V_1(V_{DD}-V_t)+V_{ds}(V_{DD}-0.5V_{ds}-V_t)\\
V_1 &= \frac{2(V_{DD}-V_t)\pm\sqrt{4(V_{DD}-V_t)^2-4V_{ds}(V_{DD}-0.5V_{ds}-V_t)}}{2}
\end{aligned}$$

Plugging V_1 into the original equation and doing a lot of tedious calculations we get:

$$I_{ds2}=\mu C_{ox}\frac{W}{2L}(V_{DD}-V_t-0.5V_{ds})V_{ds}$$

The equation for I_{ds1} is:

$$I_{ds1}=\mu C_{ox}\frac{W}{2L}(V_{DD}-V_t-0.5V_{ds})V_{ds}$$

Therefore the two currents are equivalent

6 Exercise 2.3

I_{ds2} will be less than I_{ds1} because in the case of having one transistor, $V_{sb}=0$, however, when two transistors are in use, there is a voltage $V_{sb}\neq 0$ in the top transistor. The body effect will cause the threshold voltage to be greater than V_{to}, thus resulting in a lower value of I_{ds2}.

7 Exercise 2.7

Body Effect:

$$\begin{aligned}
V_t &= V_{to}+\gamma(\sqrt{\phi_s+V_{sb}}-\sqrt{\phi_s})\\
\gamma &= \frac{t_{ox}}{\epsilon_0 k_{ox}}\sqrt{2q\epsilon_{si}N_A}\\
\phi_s &= 2v_T\ln(\frac{N_A}{n_i})
\end{aligned}$$

Solving for γ and ϕ_s:

$$\phi_s = 2(0.026)\ln\frac{2\times10^{17}\ \text{cm}^{-3}}{1.45\times10^{10}\ \text{cm}^{-3}}\approx 0.8548$$

$$\gamma=\frac{100\times10^{-}8}{3.9\cdot 8.85\times10^{-14}}\sqrt{2(1.6\times10^{-19})(11.7)(8.85\times10^{-14})(2\times10^{17})}\approx 0.7458$$

Solving for the new threshold voltage we get:

$$V_t = 0.7+0.7458(\sqrt{0.8548+4}-\sqrt{0.8548})\approx 1.653\text{V}$$

The voltage level changes by 0.95V

8 Exercise 2.9

A negative substrate bias should be used

9 Light Switch Design

Truth Table

A	B	C	F
0	0	0	0
0	0	1	1
0	1	1	0
0	1	0	1
1	0	0	1
1	0	1	0
1	1	1	1
1	1	0	0

Karnaugh Map:

A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

a)

$$F = AB'C' + A'B'C + ABC + ABC'$$

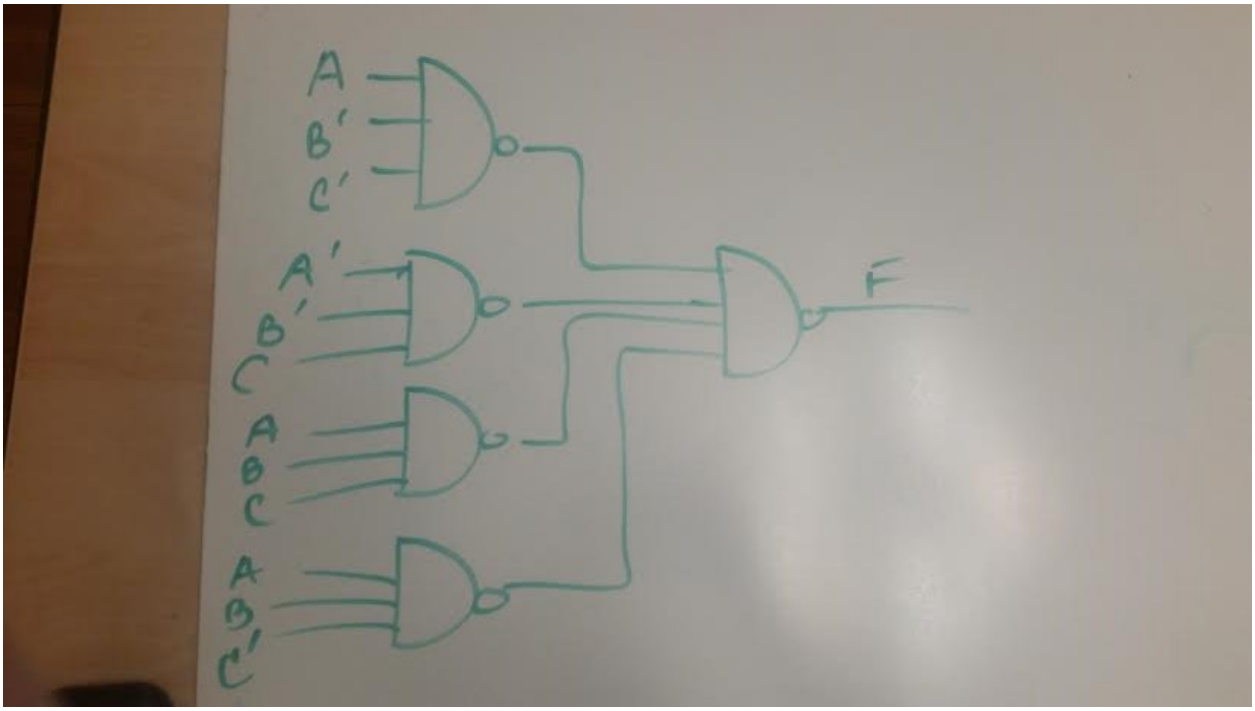

Figure 6: NAND Gate Implementation

b)

$$F = (A + B + C)(A + B' + C')(A' + B + C')(A' + B' + C)$$

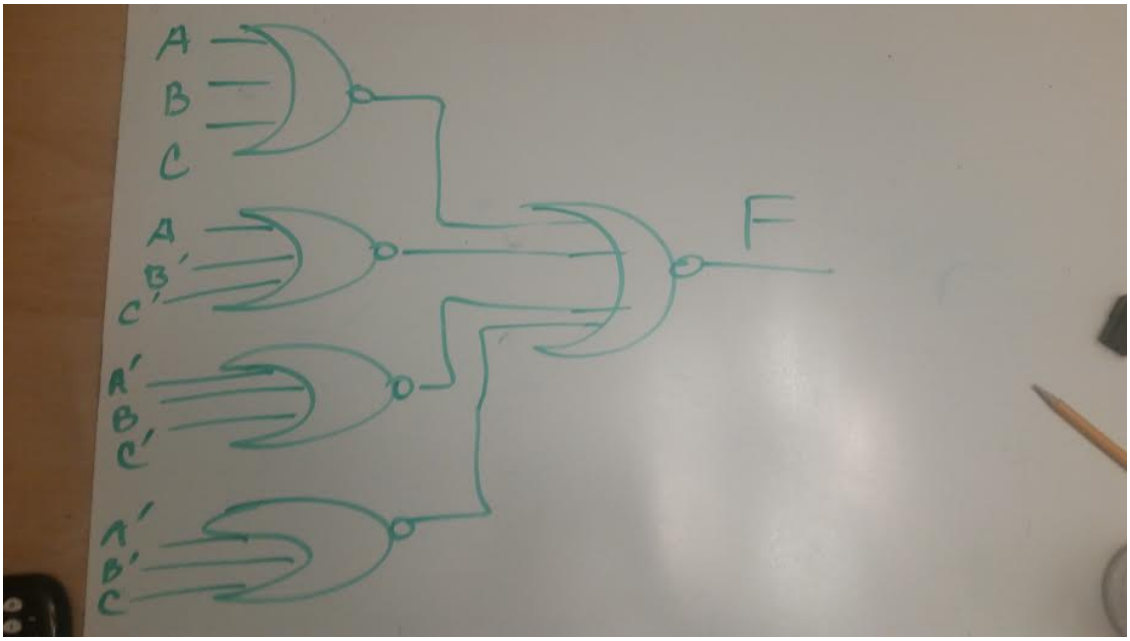

Figure 7: NOR Gate Implementation

10 CMOS Compound Gate

a)

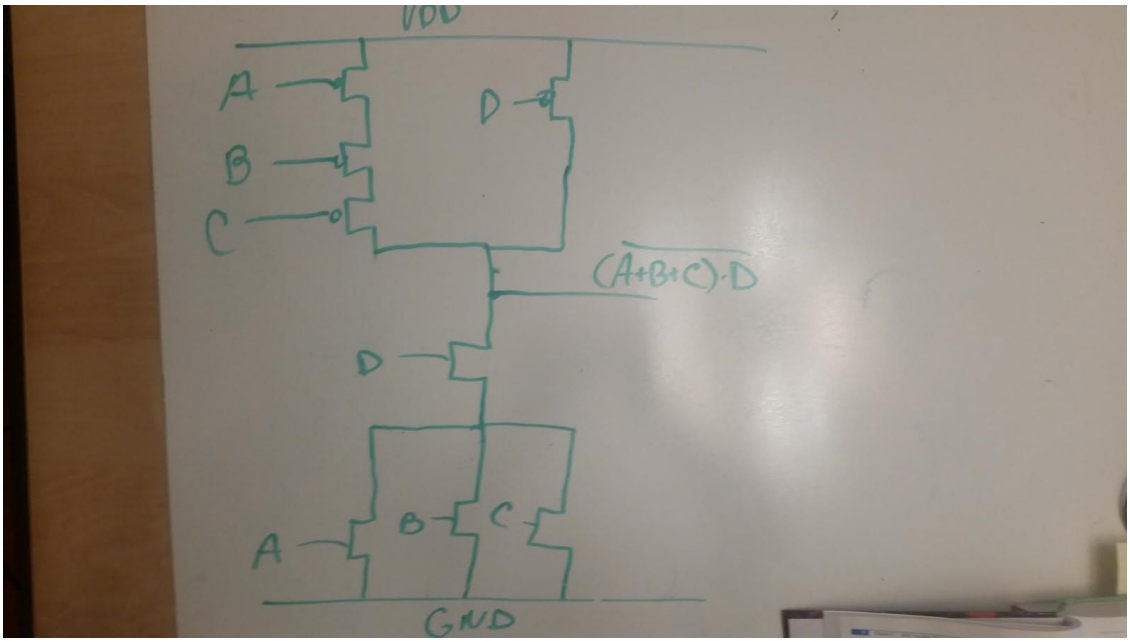

Figure 8: Transistor-Level Circuit

b)

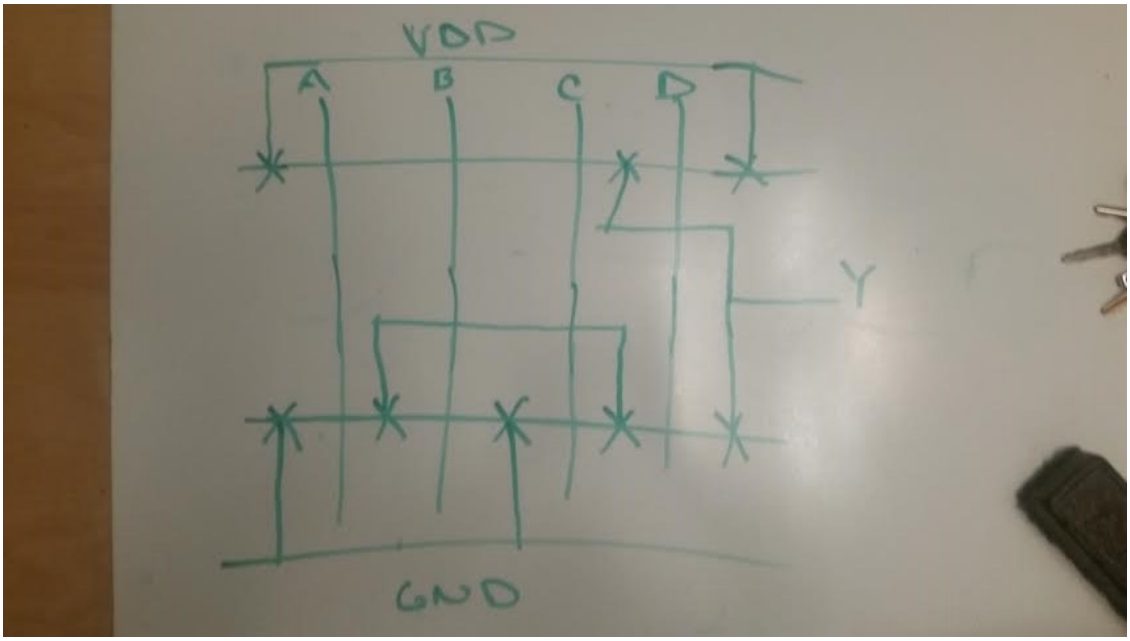

Figure 9: Stick Diagram

c)

Height = 6 tracks $\times$ $8\lambda = 48\lambda$
Width = 5 tracks $\times$ $8\lambda = 40\lambda$