Lab 9: Standard Cell Based ASIC Design Flow

Adam Sumner

Illinois Institute of Technology

ECE 429-01

Lab Date: November 9th, 2015 **Due Date:** November 16th, 2015

1 Introduction

The purpose of this lab is to introduce the student to the concept of standard cell based ASIC design flow. The student will follow a tutorial to create the layout of an accumulator and then verify its correctness using equivalence checking.

2 Theory/Pre-Lab

2.1 Theory

Standard cell based ASIC design flow automatically synthesizes a chip layout from a register transfer level (RTL) description of a chip. The design flow utilizes the standard cell library to synthesize a chip layout according to design constraints including cost, performance, power consumption, etc. While this may seem like a nice tool to completely replace manual chip design, in practice, the tool will seldom generate a satisfactory design in the beginning. It is necessary for chip designers to understand the various steps of the design flow to guide the tool through multiple iterations before an optimum solution is found. In general, the standard cell based ASIC design flow consists of two steps: Logic Synthesis and Physical Design.

2.1.1 Standard Cell Library

A standard cell is a logic gate with a layout designed for a specific fabrication process. Standard cells for different types of logic gates and different sizes of the same gate are generally grouped into a standard cell library. Cells from the same library are most likely with the same height. Since the layout of a standard cell is known, characteristics of the cell can easily be obtained via SPICE simulations.

2.1.2 Logic Synthesis

The purpose of logic synthesis is to transform RTL descriptions of chip functionality into a netlist consisting of standard cells. Currently, it is very common to have datapath or arithmetic operations in a RTL description. The logic synthesis tool should first implement these operations as boolean logic. After this synthesis, the tool performs generic logic optimizations on the design without any information form the standard cell library. After this, the netlist is generated with standard cells that have the same boolean functionality as the one generated by the tool in the beginning.

2.1.3 Physical Design

The purpose of the physical design is to create a physical implementation of the netlist consisting of standard cells. Due to the fact that every standard cell consumes silicon surface to form transistors, no two cell should overlap. Therefore, the most straightforward method is to place cells row by row, using metal layers to route wires.

2.2 Pre-Lab

The pre-lab involved familiarizing with Tutorial IV and the verilog code and testbench for the 8-bit accumulator. This was all done successfully.

3 Implementation

3.1 Schematics

3.2 Procedure

3.3 Results

3.4 Discussion

4 Conclusions