VES019

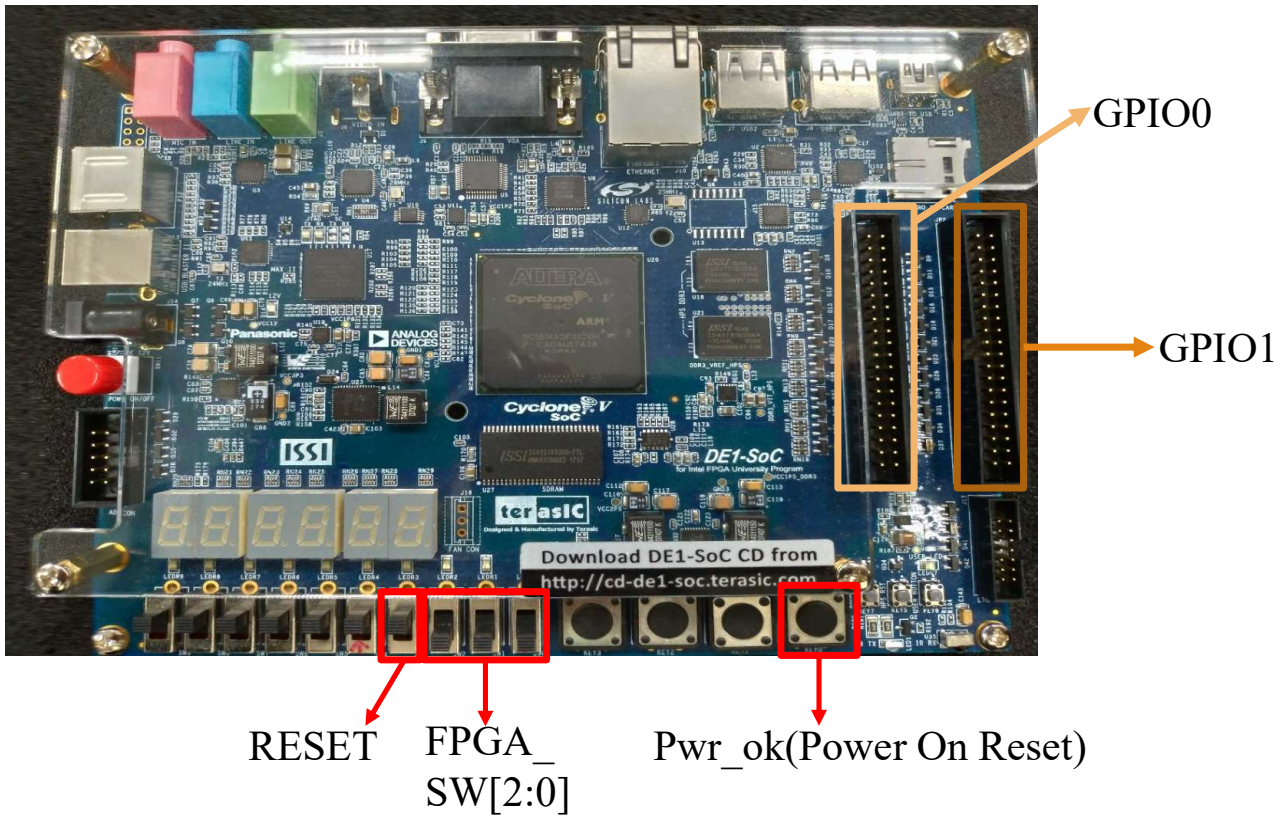
FPGA User Guide

2020_08_20

勝薪科技股份有限公司

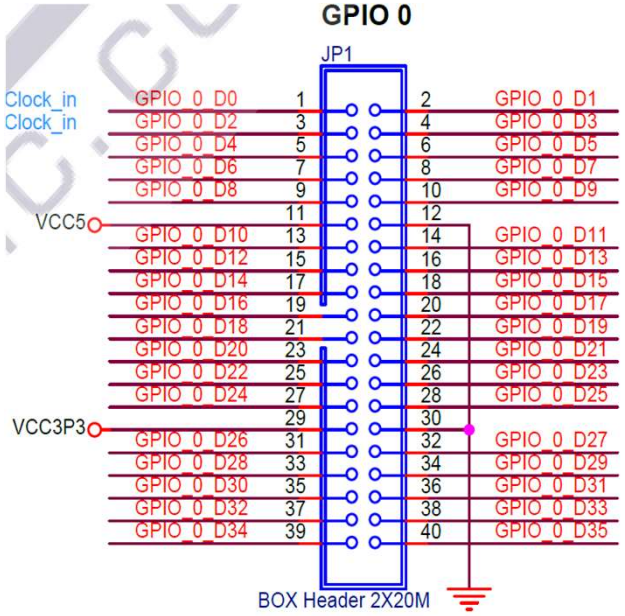
VISUAL SENSING TECH. CORP.

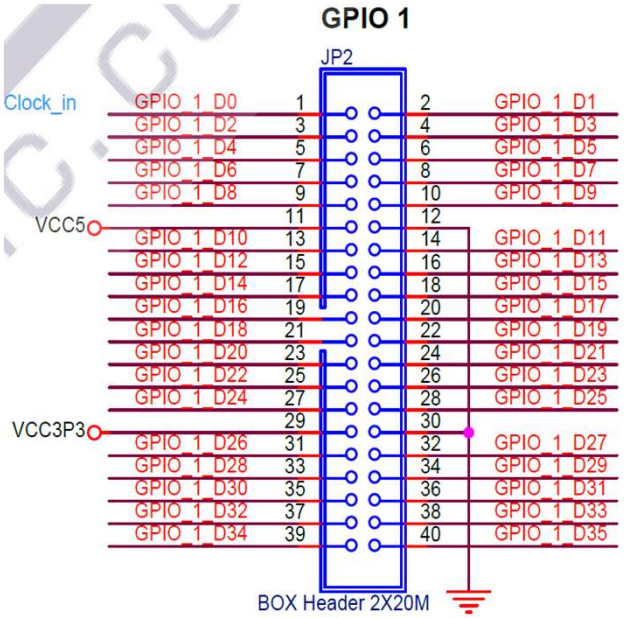
VES019 in
DE1 FPGA Platform



Interface Connection to FPGA Platform

- I2C Interface
  - GPIO_1_D21 : SCL
  - GPIO_1_D20 : SDA
- Video Bus
  - GPIO_1_D24 : VSYNC
  - GPIO_1_D23 : HSYNC
  - GPIO_1_D25 : PCLK
- SPI Interface
  - GPIO_0_D5 : SPI_SCK
  - GPIO_0_D1 : SPI_CS
  - GPIO_0_D4 : SPI_MOSI





P.S I2C需外掛500歐姆提升電阻 (3.3v)

設定參數建議(1/3)

◆ **PCLK = 0.5Khz**

- Sys_ck = 1Mhz -> I2C_ID=0x40 , I2C_Addr=20, data=70
- PCLK = 0.5Khz -> I2C_ID=0x40, I2C_Addr=18, data= Reg_DigNp[7:0]
  I2C_ID=0x40, I2C_Addr=19, data= Reg_DigNp[11:8]
  Reg_DigNp = 1998
- SPI_SCK = 9khz -> I2C_ID=0x40, I2C_Addr=21, data=111

P.S 只有當wp_code[7:0] = 0x5A時,其它暫存器才可寫入

詳細參考"Register Table"

Register Table : "VES019_register_客人.xls"

設定參數建議(2/3)

◆ **PCLK = 15Khz**

- Sys_ck = 17.5Mhz -> I2C_ID=0x40 , I2C_Addr=20, data=4
- PCLK = 15Khz -> I2C_ID=0x40, I2C_Addr=18, data= Reg_DigNp[7:0]

  I2C_ID=0x40, I2C_Addr=19, data= Reg_DigNp[11:8]

  Reg_DigNp = 1170
- SPI_SCK = 270khz -> I2C_ID=0x40, I2C_Addr=21, data=65

Register Table : “VES019_register_for_customer.xls”

設定參數建議(3/3)

◆ **PCLK = 150Khz**

- Sys_ck = 35Mhz ->I2C_ID=0x40 , I2C_Addr=20, data=2
- PCLK = 150Khz ->I2C_ID=0x40, I2C_Addr=18, data= Reg_DigNp[7:0]

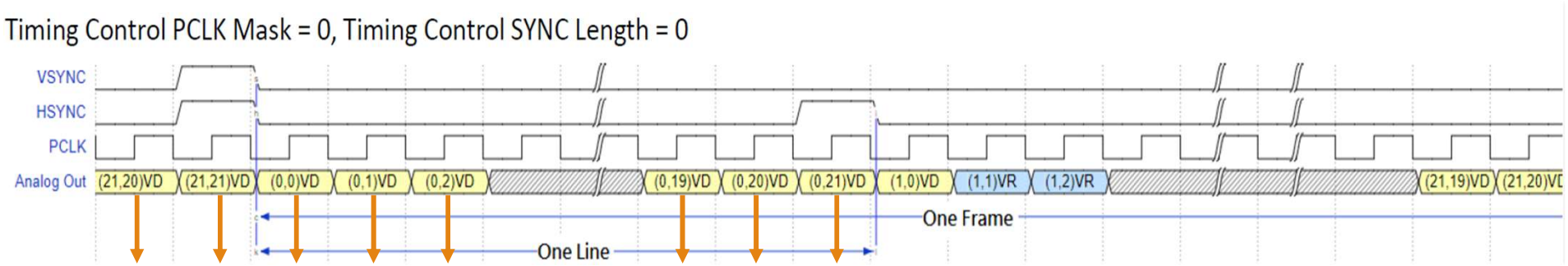
  I2C_ID=0x40, I2C_Addr=19, data= Reg_DigNp[11:8]

  Reg_DigNp = 234
- SPI_SCK = 2.7Mhz ->I2C_ID=0x40, I2C_Addr=21, data=13

Register Table : “VES019_register_for_customer.xls”

資料輸出（1/2）

◆ Disable ADC/Enable Analog out ：Reg_T_ANA_EN=‘1’ (細節參考Register Table)



SPI_Data[15:0] 0x2B3 0x2B4 0x2B5 0x0 0x1 0x12 0x13 0x14

P.S 此模式只是方便FPGA驗證，實際IC不會有 “類比輸出” + ”SPI 輸出”

資料輸出（2/2）

◆ Enable ADC/Disable Analog out : Reg_T_ANA_EN='0'