GTM016A Target Spec 20200904

Information:

INO Vox Pixel Thermal Radiation Sensitivity

Vr = 2V

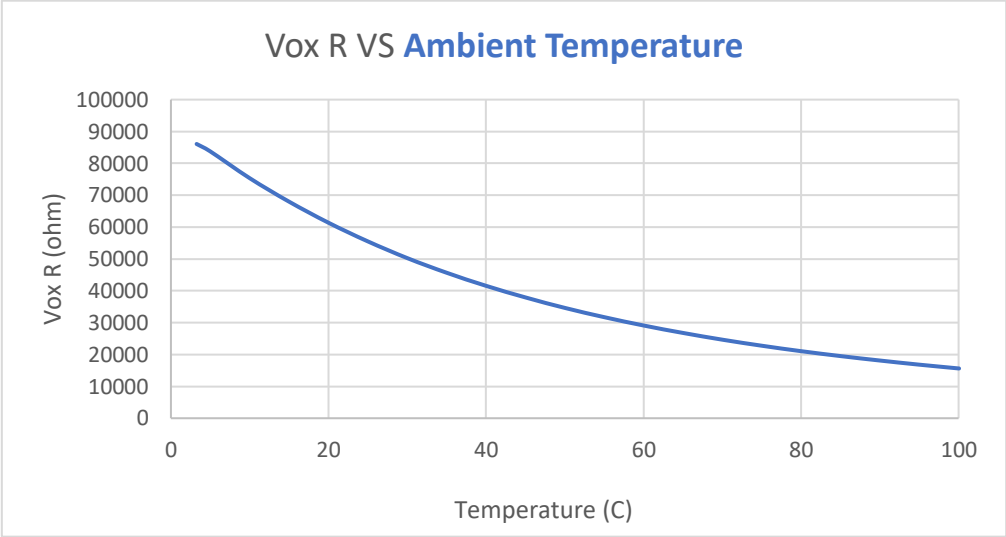
Gain = x4

Sensitivity = 500uV/˚C

INO Pixel △R/R (per ˚C)

= (500uV / 4) / 2V = 0.0000625

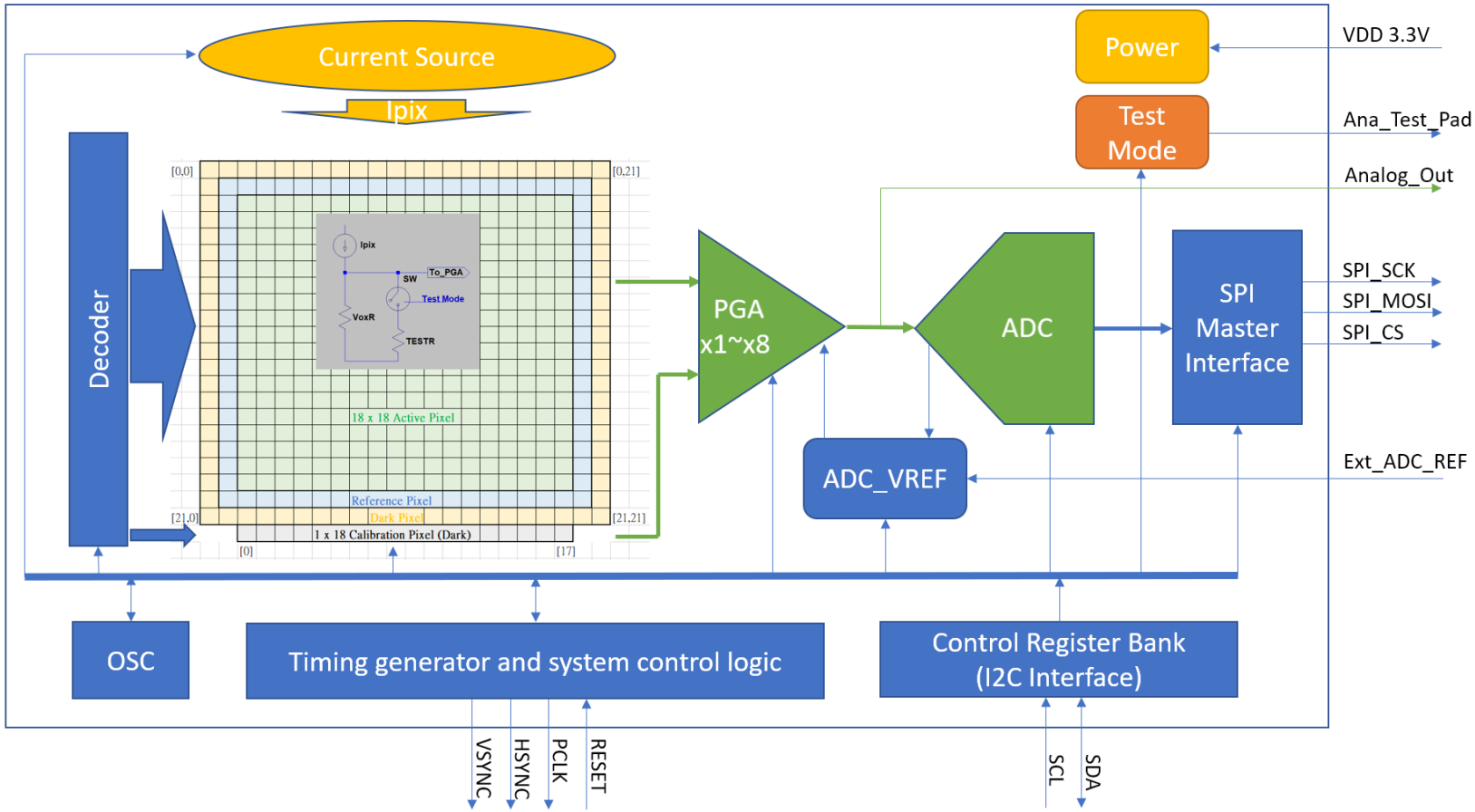
= 62.5ppm



IF NETD Target = 100mK

Analog Output Noise △V/V: Noise must < 6.25ppm

1. Block Diagram



*Ana_Test_Pad 增為三個，分別為 Ipix Out, ADC_VREF, Vbg

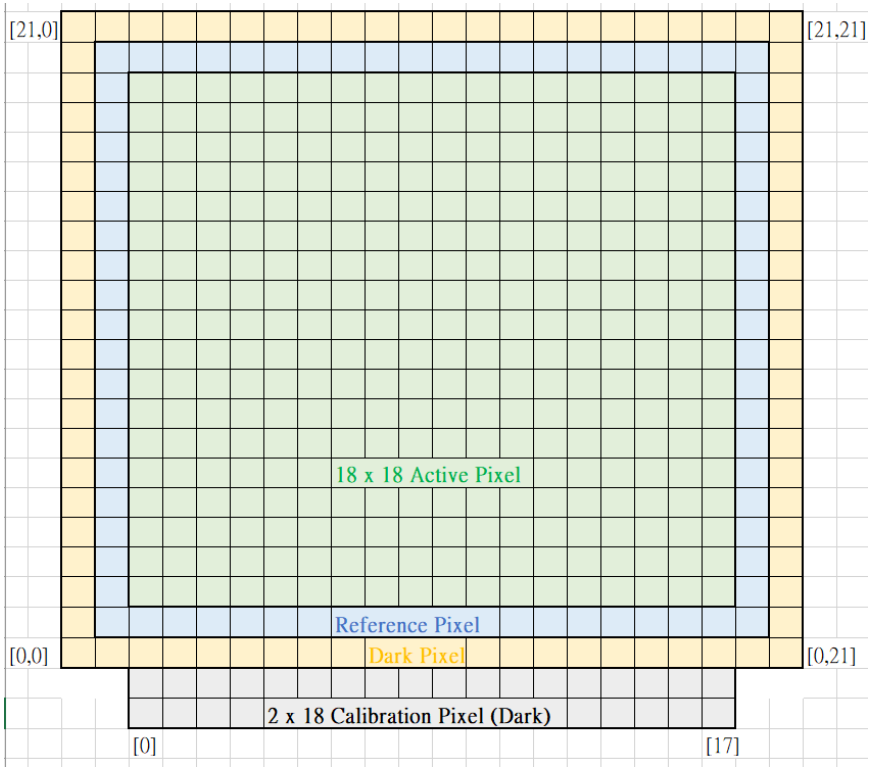
2. Electrical Specifications

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Supply voltage[1]	VDD	3.0	3.3	3.6	V
Supply current	IDD		20		mA
Analog Out Voltage Range	Vout	0.3	2.0	VDD-0.3	V
Frame Rate	fFrame	1	30	300	FPS
PCLK Frequency	fPCLK	500	15K	150K	Hz
SPI SCK Frrequency	fSCK	fPCLK * 18			Hz
I2C Frequency	fI2C	100K	400K		Hz
Digital I/O Input Voltage Low	VIL			0.7	V
Digital I/O Input Voltage High	VIH	VDD-0.7			V
Digital I/O Output Voltage Low	VOL			0.3	V
Digital I/O Output Voltage High	VOH	VDD-0.3			V
*NETD	NETD			1	K
ADC_VREF Voltage Range	ADC_VREF	0.8		2	V
Ext_ADC_REF supply current	iExRef	1			mA
Pixel_TurnOn Time(@PCLK:15KHz)	tPixelON	1			PCLK

RESET Pin: Low Reset

*NETD maximum = 1K => Analog Output Noise △V/V < 62.5ppm

3. Sensor Array



A. Output Sensor Array : 22*22

最外圈 = **Dark Pixel**

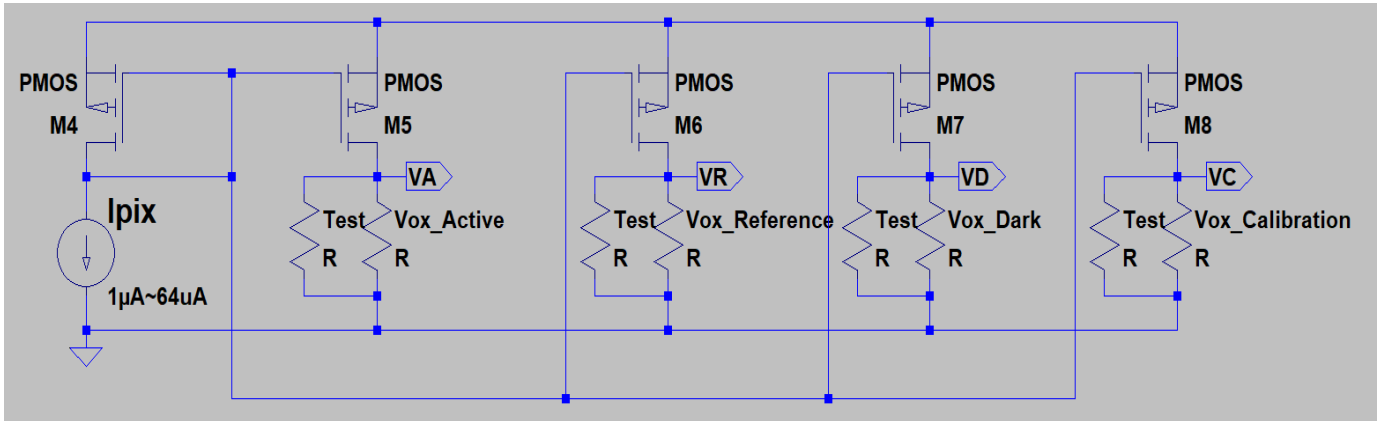
次外圈 = **Reference Pixel**

中間 18*18 = **Active Pixel**

B. 兩個獨立的 **Calibration Dark Row**: 2*18

4. Current Source(mirror)

示意圖

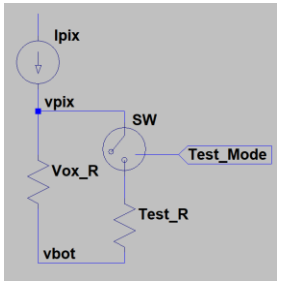


A. 一個 Current Source “Ipix” for Dark, Reference, Active, Calibration Pixel

B. Current Source 可調電流, 1uA ~ 64uA

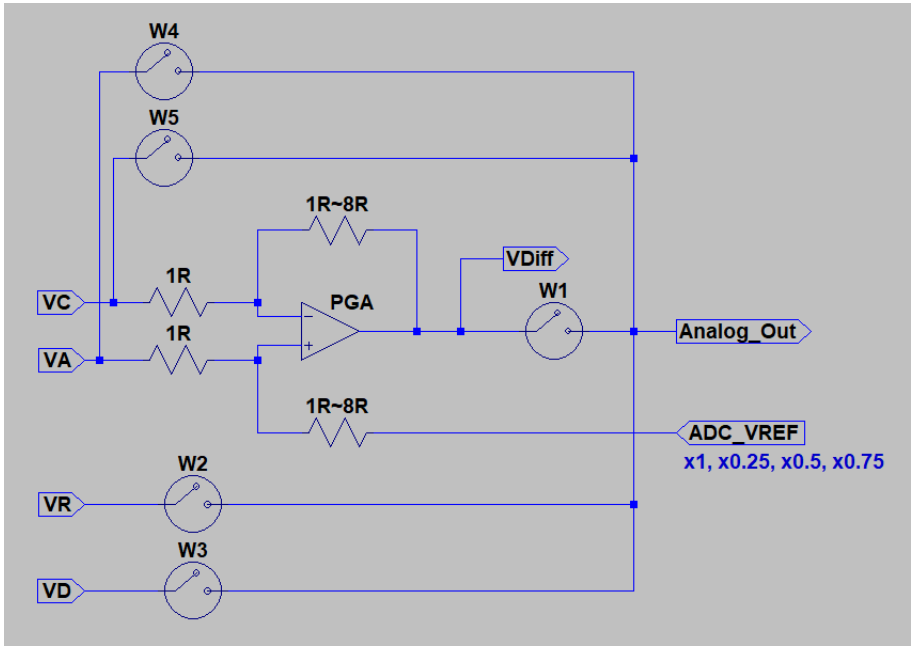
C. Current Source temporal ΔI/Iout < 62.5ppm, Iout in range 10uA ~ 64uA

D. 每個 Vox Pixel 都需並聯一個可開關的 Test R, 分別由 4 個 Register 控制開關(Active, Reference, Dark, Calibration)



5. PGA

示意圖



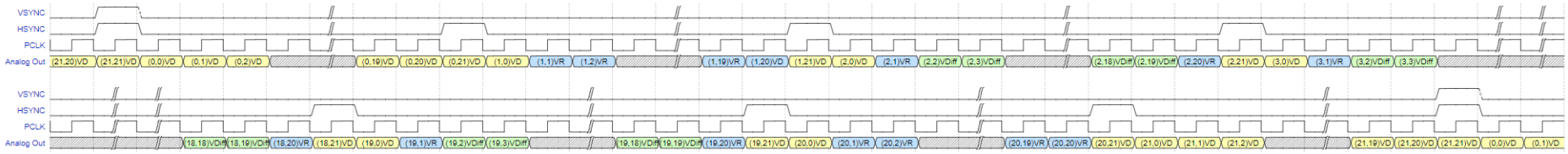
A. PGA x1 ~ x8
B. PGA Differential Input from Output Sensor Array & Calibration Row
C. PGA bypass mode: VA/VR/VD/VC direct to Analog Out PAD.
D. ADC_VREF Voltage controlled by Register x1, x0.25, x0.5, x0.75
E. VDiff = ((VA-VC)*Gain)+ADC_VREF

下方時序圖的 Register Setting:

PGA Output Control = VDiff Enable, Timing Control PCLK Mask = 0, Timing Control SYNC Length = 0,

Array Column Begin Address = 0, Array Column End Address = 21, Array Row Begin Address = 0, Array Row End Address = 21,

Calibration Row Begin Address = 0, Calibration Row End Address = 17



Analog Out 輸出條件式

```
If((DecodeAddress = [0,X]) || ((DecodeAddress = [21,X]) || ((DecodeAddress = [X,0]) || ((DecodeAddress = [X,21]))
        Analog Out = VD; // Decode Address 為 Pixel Array 最外圈時
else If((DecodeAddress = [1,(1~20)]) || ((DecodeAddress = [20,(1~20)]) || ((DecodeAddress = [(1~20),1]) || ((DecodeAddress = [(1~20),20]))
        Analog Out = VR; // Decode Address 為 Pixel Array 次外圈時
// Decode Address 為 Pixel Array 中間的 18x18 時
else if(VA_Direct_Enable)       Analog Out = VA;
else if(VC_Direct_Enable)       Analog Out = VC;
else if(VDiff_Enable)      Analog Out = VDiff;
```

6. ADC

Input from PGA Analog_Out

Resolution: <50uV @1LSB

Noise: <125uV* (To be confirm)

7. Digital Interface

1. I2C for register read write
2. SPI 16bit for Internal ADC output
3. Pixel Clock, HS, VS

8. Register

Current Source Control

Ipix [5:0], 1uA~64uA Default : 40uA

Clock Control

Default : Set PCLK = 15KHz

Clock Divider High Byte [3:0]

Clock Divider Low Byte [7:0]

Address Decoder Control

Array Column Begin Address [4:0], 0~21 Default : 0, 5'b00000

Array Column End Address [4:0], 0~21 Default : 21, 5'b10101

Array Row Begin Address [4:0], 0~21 Default : 0, 5'b00000

Array Row End Address [4:0], 0~21 Default : 21, 5'b10101

Calibration Row Select Bit [17:0], 0~17 Default : 0, 17'b00000000000000000

- End Address – Begin Address must > =1.

PGA

PGA_Gain[2:0]	000: x1, 001: x2, 010: x3, 011: x4, 100: x5, 101: x6, 110: x7, 111: x8	Default : x4, 3'b100
ADC_VREF[2:0]	[2]: ADC VREF Select. 0: Internal, 1: From Ext_ADC_VREF Pad	Default : Internal, x1, 3'b000
	[1:0] 00: ADC_VREF x1	
	[1:0] 01: ADC_VREF x0.25	
	[1:0] 10: ADC_VREF x0.5	

[1:0] 11: ADC_VREF x0.75

Output_Control[1:0] 00: VA Direct Enable, 01: VC Direct Enable, 1X: VDiff Enable Default : VDiff, 2'b10

Analog Output Enable bit: 0: Disable, 1: Enable Default : Enable 1'b1

Test Mode

TestR Enable bit[3:0], [3]Active TestR EN, [2]Reference TestR EN, [1]Dark TestR EN, [0]Calibration TestR EN. 1: Enable, 0: Disable Default : All Disable, 4'b0000

VSYNC, HSYNC, PCLK Timing Control :

PCLK Mask bit: 0: Disable, 1: Enable Default : 1'b0

SYNC Length[4:0] 0~31. Default : 5'b00000

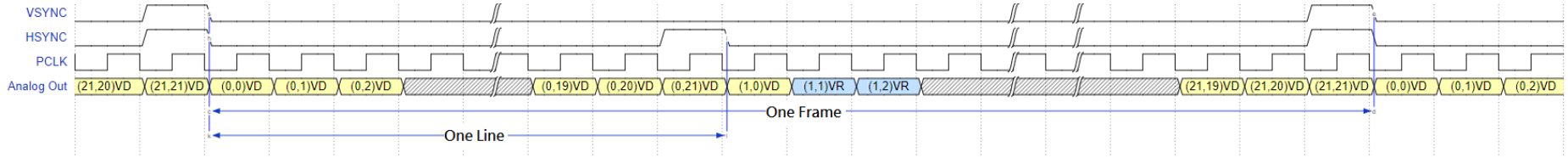
- 不存在 PCLK Mask = 0, 而 SYNC Length > 0 的情況.

SPI Control:

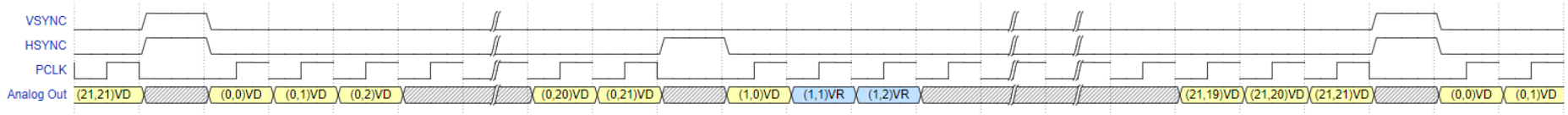
SPI CS Mode bit: 0: Toggle the CS Pin on each pixel data Default : 1'b0

1: Toggle the CS Pin when changing frame

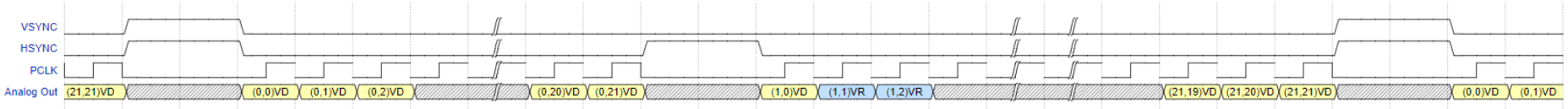
Timing Control PCLK Mask = 0, Timing Control SYNC Length = 0



Timing Control PCLK Mask = 1, Timing Control SYNC Length = 0

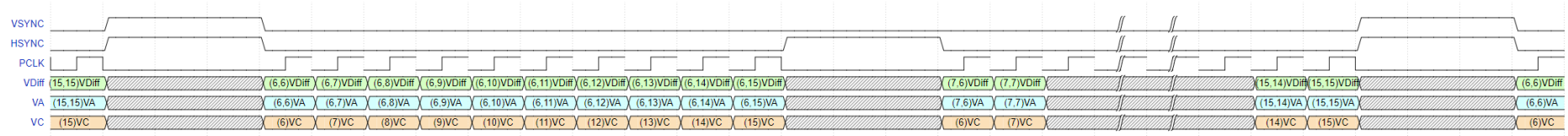


Timing Control PCLK Mask = 1, Timing Control SYNC Length = 1



Ex: Timing Control PCLK Mask = 1, Timing Control SYNC Length = 2

Array Column Begin Address = 6, Array Column End Address = 15, Array Row Begin Address = 6, Array Row End Address = 15,



SPI Timing:

SPI Out 限制條件:

ADC_EN = 1, PXCL_MASK =0, SYNC_LEN must = 0

SPI Out 與 Analog Out 只能二擇一

PCLK_Mask=0/1 對於 SPI_SCK 的影響 => 沒有 PCLK 時就沒有 SPI_SCK

SPI CS Mode = 0

SPI CS Mode = 1

允收標準　　測試環境: 室溫

1. Register Read/Write PASS.
2. Register setting Functions, Timing, PASS
3. Electrical Spec PASS.
4. Analog Out Noise:

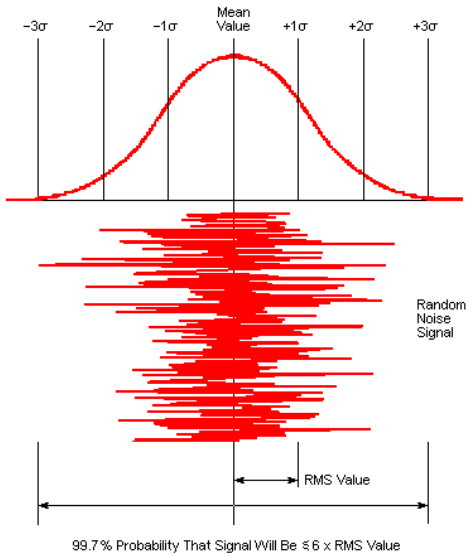
   Enable All Test R, Test R Typical 50k ohm, Gain Setting : x4, ADC VREF: x0.5

   量測 Analog Out(VDiff) Noise Level:

   @ Ipix = 10uA, Noise RMS Value < 125uV

   @ Ipix = 40uA, Noise RMS Value < 500uV

   @ Ipix = 60uA, Noise RMS Value < 750uV



5. ADC
   Resolution: <50uV @1LSB
   Noise: <125uV

20200904 Change List

Page 2

1. Ana_Test_Pad 增為三個，分別為 Ipix Out, ADC_VREF, Vbg (取消 Register Ana_Test_Pad Function[2:0])

Page 3

2. 增加敘述 Ext_ADC_REF input current >1mA
3. 增加敘述 Analog Out 跟 SPI Out 一樣, Pixel 通電時間最短 1 個 PCLK, PCLK typ.15KHz

Page 4

4. 增加一條 Calibration Row(Total 2 Row)
5. Array Start address(0,0) 移到左下角

Page 5

6. 增加敘述 Test R 分別控(Active, Reference, Dark, Calibration)

Page 6

7. 增加敘述 VDiff = ((VA-VC)*Gain)+ADC_VREF

Page 10

8. 移除 Calibration Row Begin/End Address Register
9. 增加 Calibration Row Select Bit [17:0]
10. 增加敘述 End Address – Begin Address must > =1.

Page 11

11. 移除 Ana_Test_Pad Function Register

Page 12

12. 配合 Calibration Row 的修改, 修改 Example 的 Timing.

Page 13

13. SPI Out 增加限制條件: ADC_EN = 1, PXCL_MASK =0, SYNC_LEN must = 0

14. 增加限制條件: Analog Out 與 SPI Out 只能二擇一

15. 增加敘述: PCLK_Mask=0/1 對於 SPI_SCK 的影響 => 沒有 PCLK 時就沒有 SPI_SCK

16. SPI Timing 後移一個 tSPI_SCK