Lab 2

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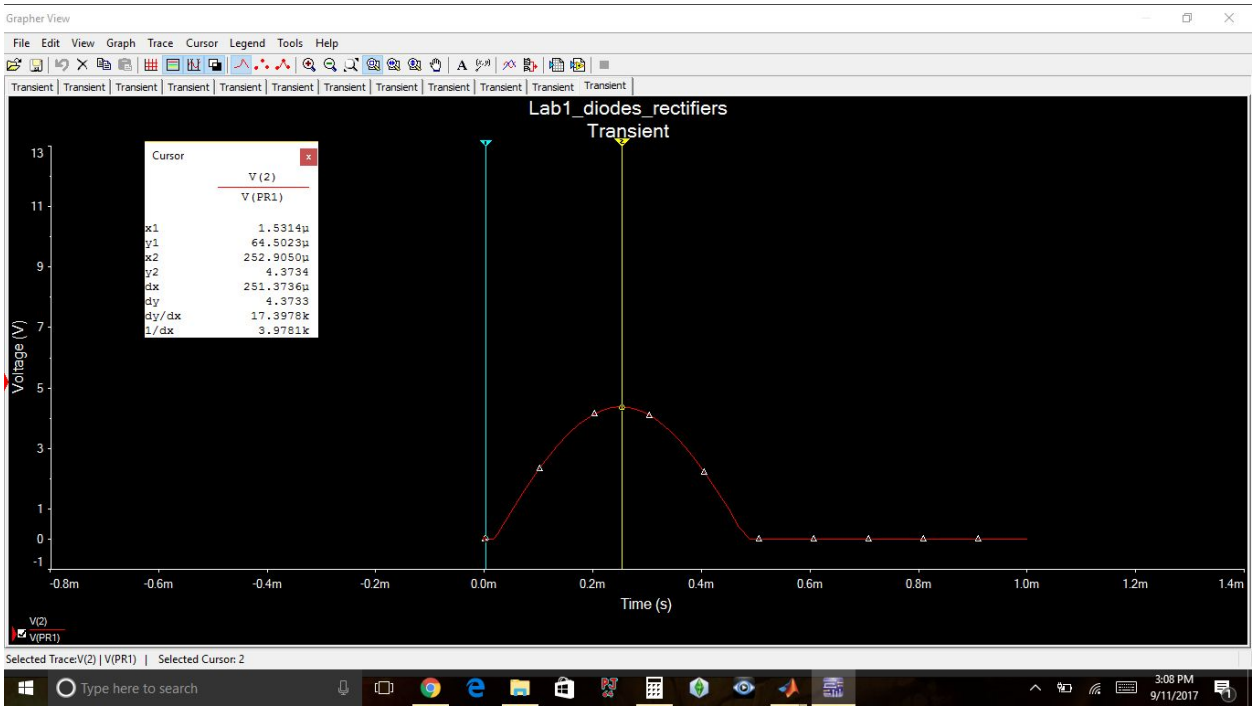
Derek Lomax

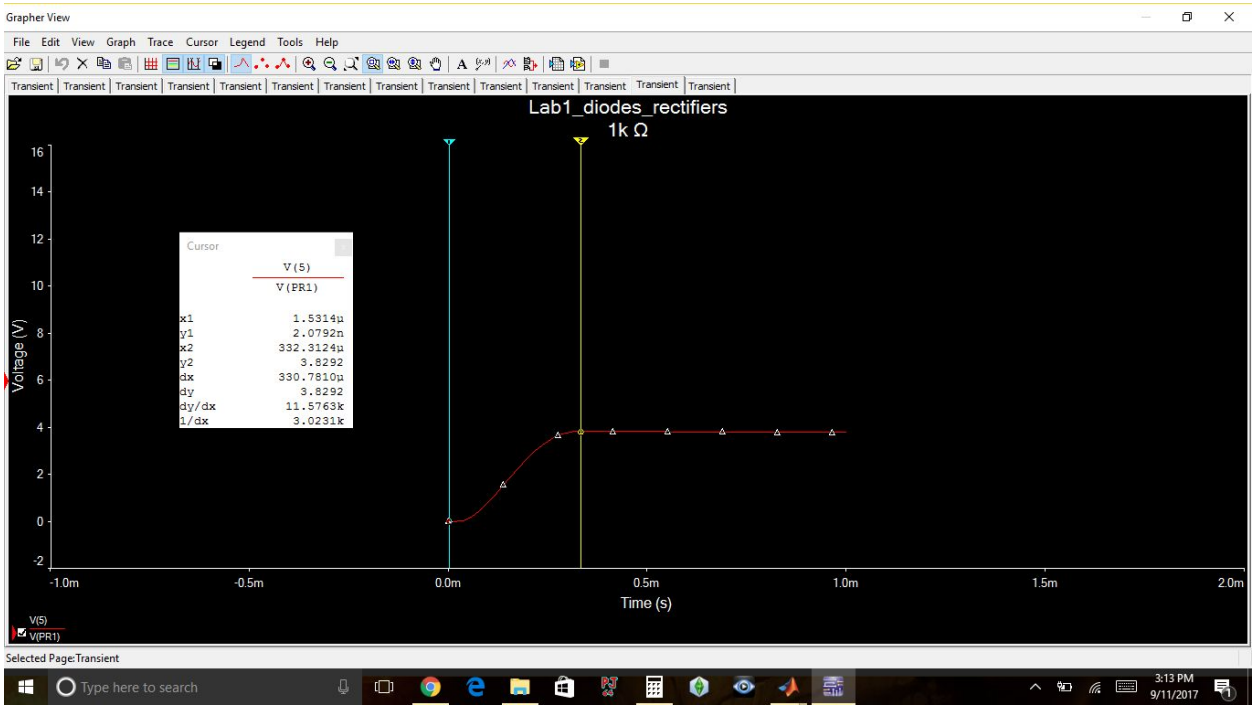
Part 1

5. Record the plot for Vin and Vout. Record the peak voltage value for Vout and label it as Vp. Peak voltage is 4.37 V

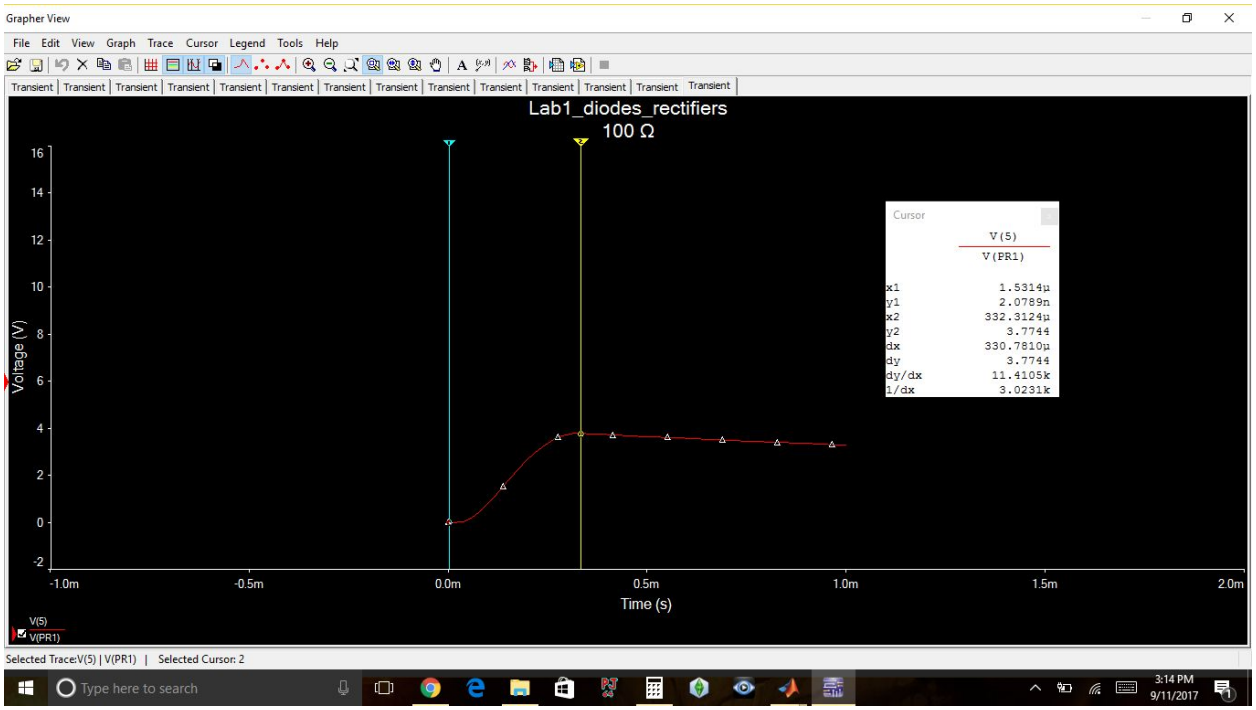


Part 2

Peak Rectifier	
1 k Ω	100Ω
Peak voltage = 8.36 V	Peak voltage = 8.25 V
Vaverage = 4.121 V	Vaverage = 4.104



1k graph (above)
100 Ω (below)



Half Wave Rectifier	Peak Rectifier	
Peak voltage = 4.37	1 k Ω	100Ω
	Peak voltage = 3.83 V	Peak voltage = 3.77 V
	Vaverage = 3.756 V	Vaverage = 3.586
	Ripple Voltage 1kΩ	Ripple voltage 100 Ω
	0.027 V	0.265 V
	DC voltage 1kΩ	DC voltage 100 Ω
	3.817 V	3.637 V

1. Get checked off
2. The best rectifier would be the full/peak rectifier with the higher resistance.
3. The capacitor charges and discharges during the transient analysis boosting the output at the end.

Lab 2

Part 1:

1. Build the Half-wave rectifier circuit on the breadboard.
2. Using the function generator, provide a sinusoidal input of 10Vpk-pk and 1kHz.
3. Using the oscilloscope, capture the input and output waveforms.
4. Record the peak voltage value for Vout and label it as Vp.

Peak voltage = 4.48V

Part 2:

1. Using the same input source as Part 1, build the following:

a. Peak detector I: Use $\mathbf{R_L}$ = 1 kΩ, $\mathbf{C_L}$ = 47 μF.
3.52V peak value

b. Peak Detector II: Use $\mathbf{R_L}$ = 100 Ω, $\mathbf{C_L}$ = 47 μF

2. For both the circuits, record the plot for Vin and Vout. Record the peak voltage (Vp), ripple voltage (V_R), and DC voltage (V_{DC}).

Part 3:

1. Using the same input source as Part 1, build the precision half-wave rectifier circuit.
2. Record the oscilloscope plots for Vin and Vout vs. time.
3. Record the peak output voltage (Vp).
4. Using the X-Y mode on the oscilloscope, plot Vout vs. Vin.
5. How does the rectifier work for input voltage amplitude less than the diode voltage drop?

Conclusion:

1. Compare the measured values with the simulation results from Lab 1 & 2 calculated results in a tabular form. *Get your summary table checked off by the instructor.*

	Half Wave	Full Wave 1KΩ peak	Ripple	DC	Full Wave 100Ω peak	Ripple	DC	SUPER DIODE Max
Simulated	4.37	3.83	0.027 V	3.817 V	1.77 V	0.025 V	2.637 V	5.0
Measured	4.48	3.32	0.16 V	3.24 V	1.56 V	0.400 V	1.4 V	5.36
Percent Difference	5.5	15.5	.25	31	5	0.5	1.5	18

Lab 3

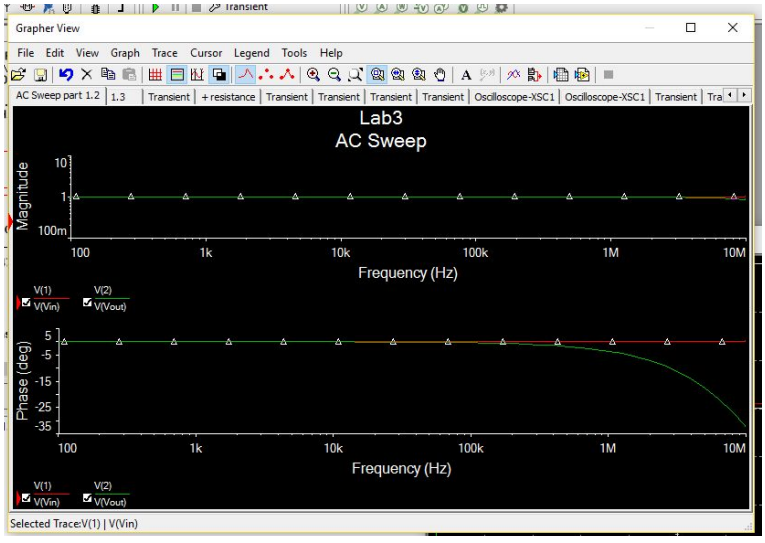
<u>Part 1:</u> Diode Limiter (Fig. 3.1)

1. Use D_1, D_2 = 1N4003 (or similar), R = 1 kΩ.2. For input voltage, use a sinusoid with 5Vpp, 100Hz and no DC component.

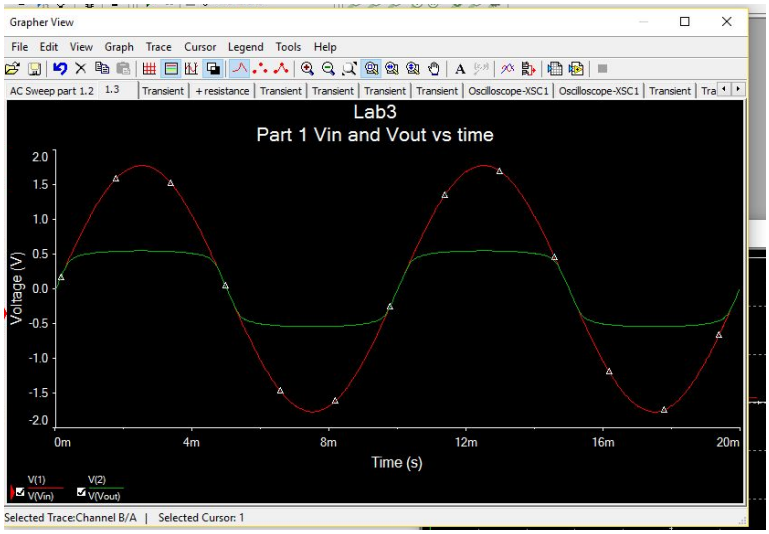
<u>Note:</u> *Use small time steps for finer resolution. Note the highest and lowest voltage values. Note how abruptly the diodes cut off th*

e input waveform. This is known as hard-limiting. Try playing with the input voltage amplitude, input voltage frequency and resistor values. For frequencies, try 100 Hz, 1kHz, 10kHz, 100 kHz, 1MHz, 10MHz. How does the output change?

Done ac sweep part 1

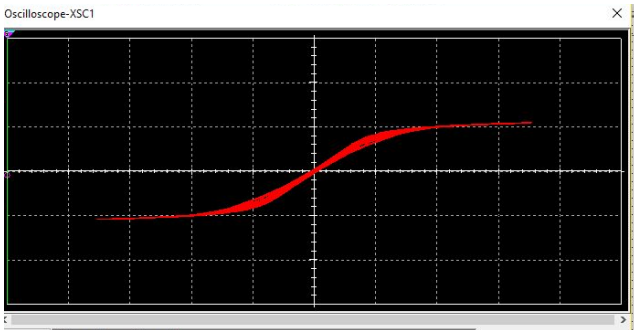


3. Record the plot of V_I vs time and V_O vs time. What are the highest and lowest voltage values? Why do we get these values?



Done: transient part 1.3

4. Record the plot of V_O vs V_I; use frequency=100 Hz, amp=2.5V

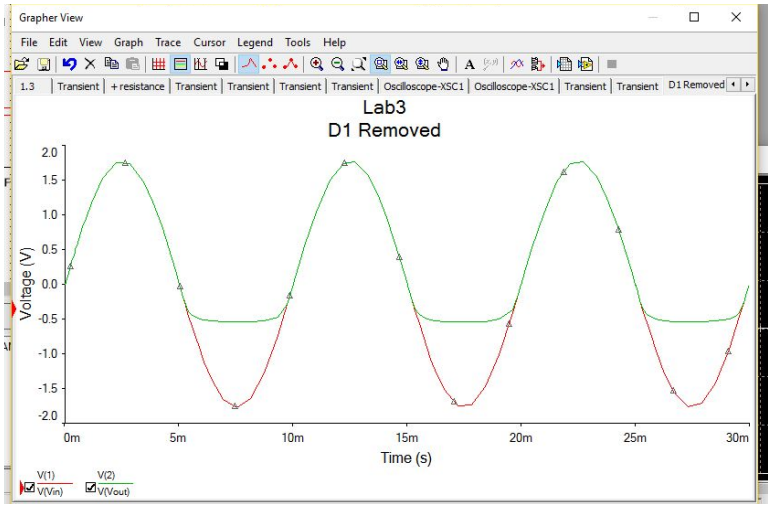


5. What happens to the waveform if you change the resistor value or input voltage amplitude or the input voltage frequency?

The output voltage is decreased

6. Keep D_1 and Remove D_2 from the circuit and simulate. What is the result? Next, keep D_2 and remove D_1 from the circuit and simulate. What is the result?

Remove D1 and only the bottom is chopped off, Remove only D2 and only the top is cut off

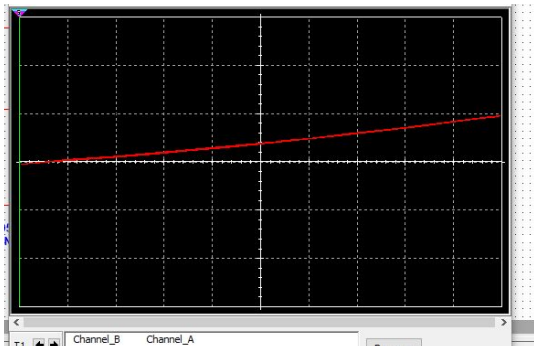


Part 2: Zener Diode Limiter (Fig. 3.2)

1. Use Z_1, Z_2 = 1N4733A (or similar) zener diodes, R = 1 kΩ.
2. For input voltage, use a sinusoid with 14Vpp, 100Hz and no DC component.

Note: *In the simulator, you will need to replace the generic zener with a zener that has low breakdown voltage (In the experiment, we will use the zener- 1N4733A that has breakdown rating of 5.1 V). Pick the one with breakdown rating closest to 5.1 V. Note how the circuit cuts off the input waveform gradually. This is known as soft-limiting.*

3. Note the min and max values of the output voltage.
4. Increase and decrease the resistor value. Note the change in the output voltage. Where is it smoothest?
5. Record the plot of Vin and Vout vs time.
6. Record the plot of Vout vs Vin.



Part 3: Clamper (Fig. 3.3)

1. Use D_1= 1N4003 (or similar), R = 10 kΩ, C = 47 μF,
2. For input voltage, use a **square wave** with 2 Vpp, 100 Hz, DC=0 V.

Hint:

a. Time period = 1/frequency.

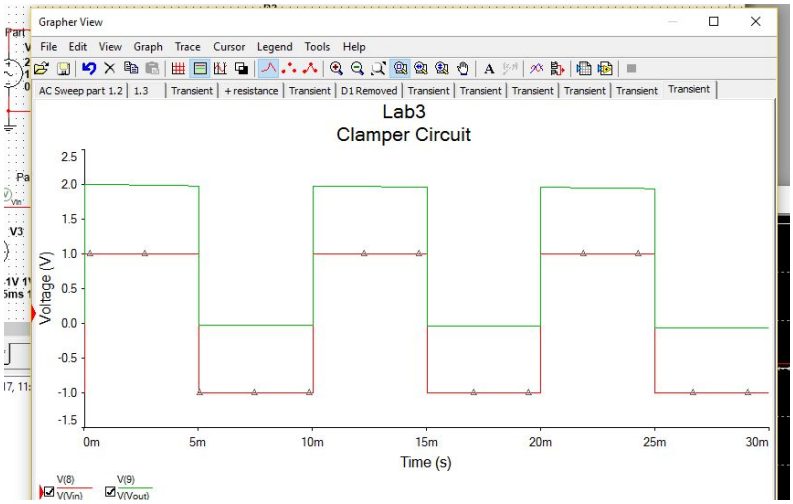
b. In order to generate a square wave you want the pulse to be ON and OFF for equal amounts of time.

Note: *Larger the capacitor, better the shape of the output voltage.*

3. Note the min and max values of the output voltage.

Max = 2V Min = 0V

4. Record the plot of Vin and Vout vs time.



<u>Part 3:</u> Voltage doubler (Fig. 3.4)

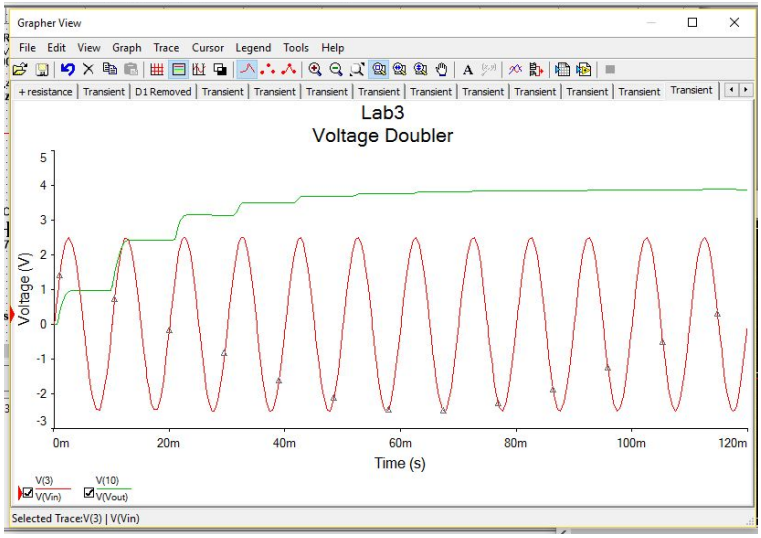
1. Use D_1, D_2 = 1N4003 (or similar), R = 100 kΩ, C_1 ,C_2 = 47 μF,
2. For input voltage, use a sinusoid with 5Vpp, 100Hz and no DC component.

a. Note how a voltage doubler (and hence multiplier) can take AC voltage, and multiply that voltage by some factor giving a larger DC voltage (the output voltage should be 2 diode drops lower than twice the peak input voltage). Probe/Measure the voltage across D_1. Note the peak value. Now probe/measure the output voltage.

3. Note the min and max values of the output voltage.

Min = 0V Max approaches 3.8V

4. Record the plot of Vin and Vout vs time.

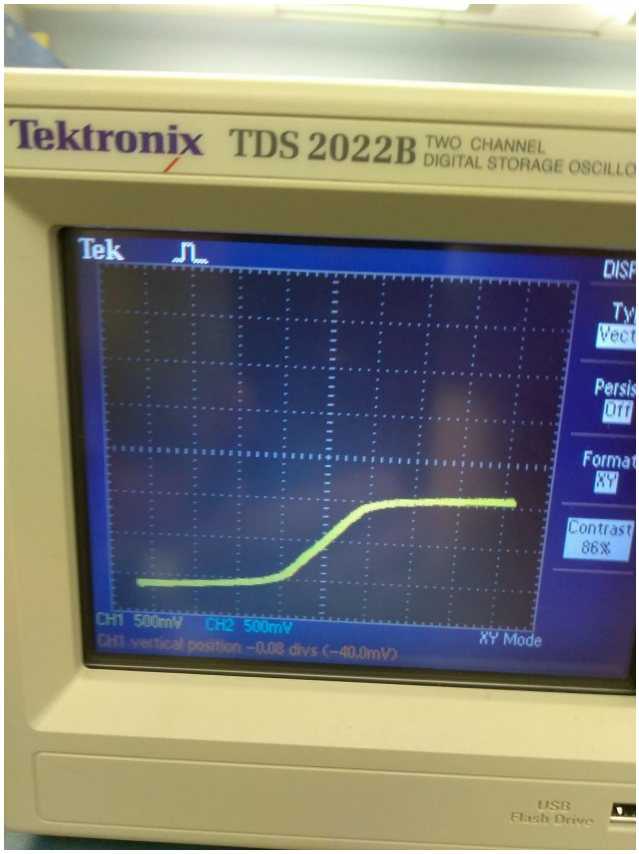


Procedure:

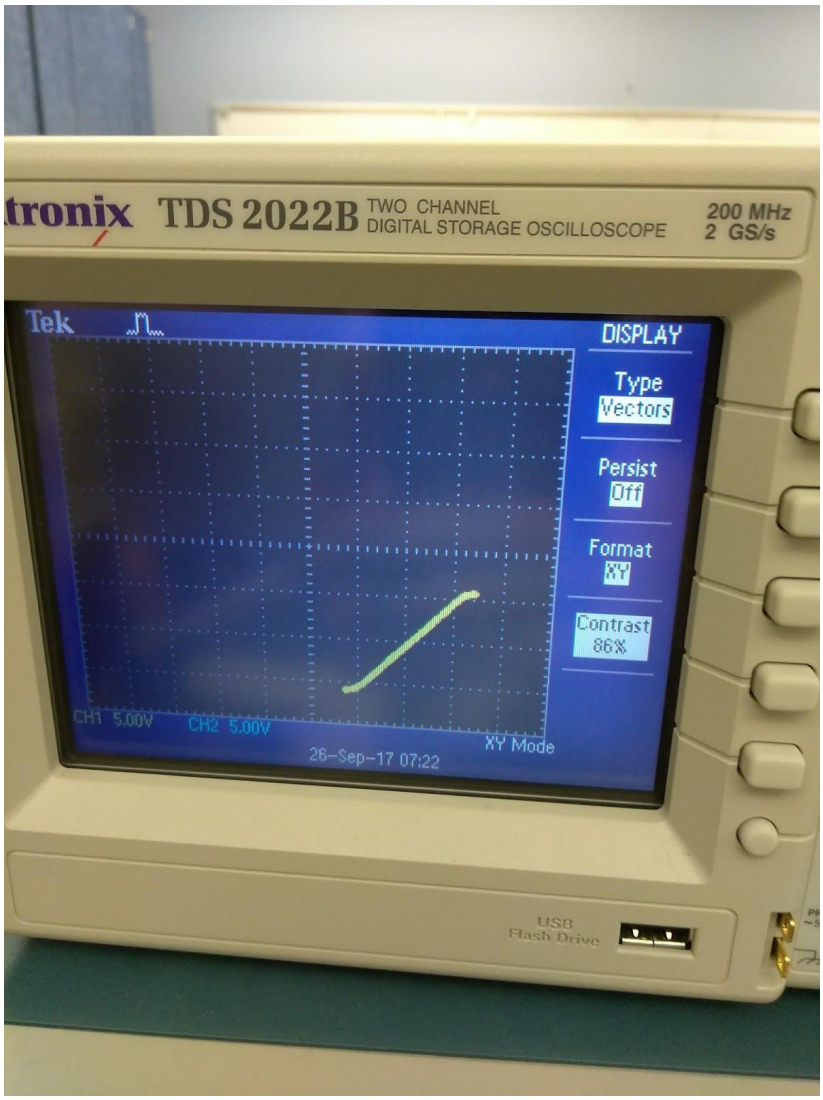
1. Build the simulated circuits on a breadboard.
2. Record the oscilloscope plot of Vin and Vout vs time, for each of the circuit.
3. Record the highest and lowest output voltage values. How does they compare to the simulated value?
4. For circuits in Part 1 &and 2, use the oscilloscopes XY mode and record the Vout vs. Vin plot.

Get the recorded outputs in your lab report checked off by the instructor.

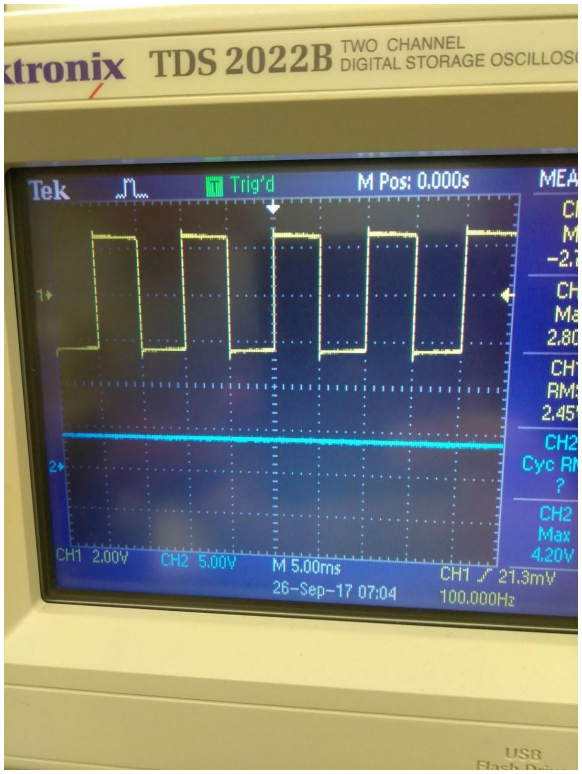
	Part 1 Diode limter	Part 2 Zener Diode limiter	Clamper Part 3	Part 4 Doubler
Measured	Max Voltage +-600mV	Max 5.2 V Min -1.2V	Max 1.44 V Min -.56 V	Max 4.2 V
Simulated	-+546mV	Max 4.73V Min 0 V	Max 2.0 V Min 0.0 V	Max 3.85 V



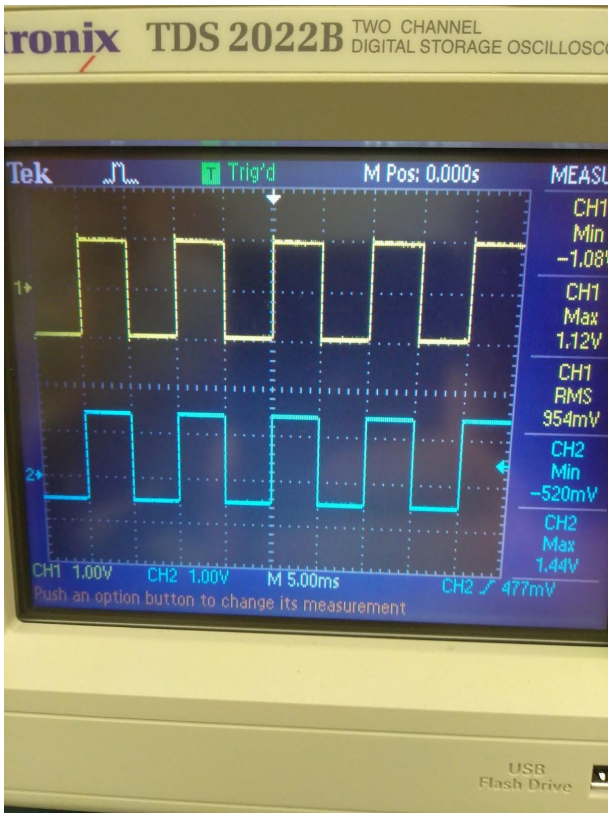
Part 1 in vs out



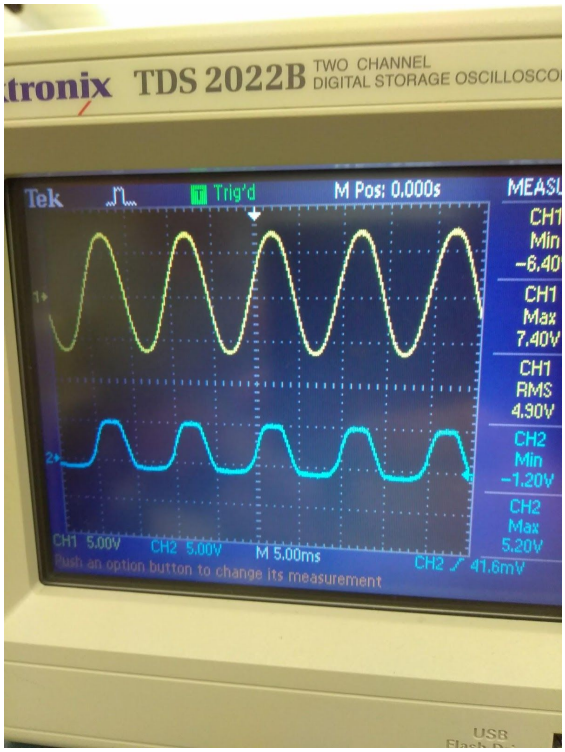
Part 2 in vs out



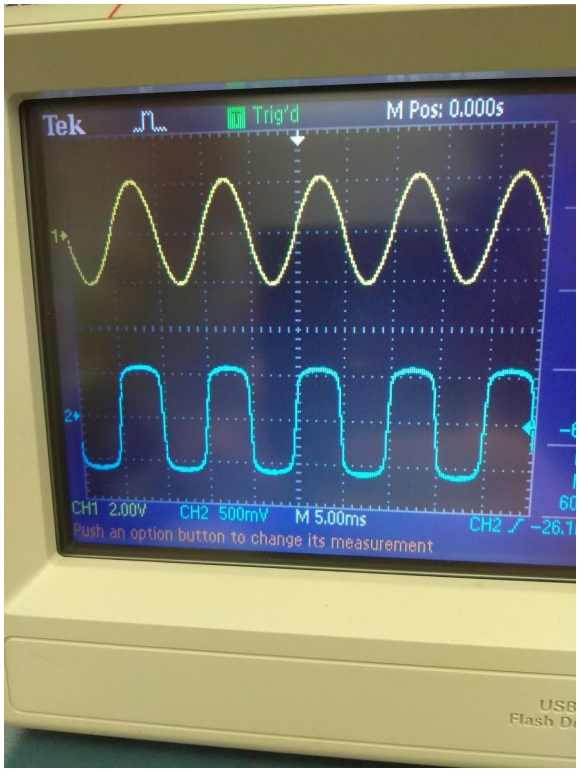
Voltage doubler



Clamper



Zener Diode



Diode limiter

Conclusion:

1. For the diode limiter circuit, how would you change the limiting voltage to approximately +1.4V and -1.4V?
2. Can you think of an application for each of the circuits?

Lab 4

<u>Part 1</u>: NMOS in Saturation Mode

Design/ Calculate: (Use Example 5.6 as a guide)

1. Design the circuit in Fig. 2 such that $\boldsymbol{I_D}$ **= 1 mA**, $\boldsymbol{V_D}$ **= 10 V**, and $\boldsymbol{V_{DD}}$ **= 15 V**.
2. Assume $\boldsymbol{R_1}$ **=** $\boldsymbol{R_2}$ **= 3 MΩ,** and $\boldsymbol{k_n}$ **= 1.08 mA/V²**. Use **2N700TA** (or 2N7002) as the NMOS transistor.
3. Calculate the overdrive voltage, V_{OV}.

   V_{OV} = 3.3V

4. Determine V_{GS}.

   V_{GS} = 5.4 V

5. Find V_S, and use it to calculate R_S and R_D

   V_s = 5.4V R_s = 5.4K R_D = 5K

Simulate:

1. Using the values found above, simulate the circuit.
2. Record the values of V_S, V_D, V_G, and I_D
3. ***<u>Note:</u>*** The simulator has its own, more complex model of the real transistor, so there should be some small variations.

<u>Part 2:</u> NMOS in Triode Mode

Design/ Calculate:

1. Redesign the circuit for Triode Mode, such that $\boldsymbol{I_D}$ **= 1 mA**, $\boldsymbol{V_D}$ ***= 6*** **V**, $\boldsymbol{V_{DS}}$ **= 0.26 V**, and $\boldsymbol{V_{DD}}$ **= 15 V**.
2. Calculate the overdrive voltage, V_{OV}, V_G, and V_{GS}.

   V_{OV} = 5.4 V V_G = 7.5 V V_{GS} = 5.4 V

3. Calculate R_S and R_D.

   R_S = 9k R_D = 5.4k

Simulate:

1. Using the values found above, simulate the circuit.
2. ***<u>Note:</u>*** You may need to adjust the values of R_D and R_S until you achieve $V_D \sim 6$ V. Verify that you are still in the triode region ($V_{DS} < V_{OV}$).
3. Record the values of V_S, V_D, V_G, and I_D

Procedure:

Part 1: NMOS in Saturation Mode

1. On a breadboard, assemble the circuit using values from pre-lab Part 1.
2. Using a digital multimeter, measure V_S, V_D, V_G.
3. Now, measure all the resistors to three significant digits.
4. ***Note:*** The circuit should not be powered while measuring resistance.
5. Using the measured values of V_S, V_D, and the resistors, what is the measured value of I_D?

Part 2: NMOS in Triode Mode

1. On a breadboard, assemble the circuit using values from pre-lab Part 2. You may need to adjust the values of R_D and R_S until you achieve $V_D \sim 6$ V.
2. Using a digital multimeter, measure V_S, V_D, V_G.
3. Now, measure all the resistors to three significant digits.
4. Using the measured values of V_S, V_D, and the resistors, what is the measured value of I_D?

Part 1	R1	R2	VG	VS	RS	VD	RD	ID	Vov	VGS	VDS
Theoretical	3.00E+06	3.00E+06	7.5	5.4	5.40E+03	10	5.00E+03	1.00E-03	5.4	2.1	0.34
Measured	2.97E+06	2.93E+06	6.5	5.3	5.38E+03	10.2	4.90E+03	9.77E-04	5.3	1.2	0.349
Difference (percent)	1.0667	2.2333	13.3333	1.8519	0.2963	-2.0000	2.0000	2.3000	1.8519	42.8571	-2.6471
Part 2	R1	R2	VG	VS	RS	VD	RD	ID	Vov	VGS	VDS
Theoretical	9.00E+05	3.00E+06	11.53	5.74	5.74E+03	6	9.00E+03	1.00E-03	3.69	5.79	0.26
Measured	9.60E+05	3.50E+06	10.5	5.75	5.70E+03	5.76	9.15E+03	9.80E-04	3.05	5.15	0.25
Difference (percent)	-6.67	-16.67	8.93	-0.17	0.70	4.00	-1.67	2.00	17.34	11.05	3.85

Lab 5

<u>Part 1:</u> DC Analysis

1. Sketch the DC model of the circuit in your lab book.
2. ***<u>Note:</u>*** Replace the capacitors with open circuit.
3. Calculate V_{OV}, V_G, V_S, and V_{GS}.
4. Determine the value of transconductance, $\boldsymbol{gm}$ **= 1.47mA/V**
5. Find R_S.

Note: At this stage, we know neither $\boldsymbol{V_{DS}}$ nor $\boldsymbol{R_D}$.

<u>Part 2:</u> AC (small-signal) Analysis

1. Sketch small-signal model of the circuit in your lab book.
2. ***<u>Note:</u>*** Replace the transistor with its small-signal model, capacitors with short circuits, and V_{DD} with an AC ground. What happens to R_S?

   Rs will be bypassed because Cs turns into short.

3. Calculate r_o (Use V_A = 70V).

   70K

4. Label the gate of the transistor as v_i, i.e. the small-signal voltage at the input. Find the ratio, $\boldsymbol{v_i / v_{SIG}}$.
5. Derive the expression for $A_V = v_o / v_i$. What is the value of R_D that produces a small-signal gain of at least A_V*= - 5 V/V*?
6. What is the DC voltage at the drain, V_D? What region is the transistor operating in?

Simulate:

1. Using the values found above, and $\boldsymbol{C_G = C_L = C_S}$ = 47 μF, simulate the circuit.
2. Set the input v_{sig} to 50mVpp, 1kHz with no DC component.
3. Record the DC values: V_{GS}, V_{DS}, and I_D?
4. Determine *Av*.

Procedure:

<u>Note:</u> You may need to adjust values of the components as necessary in the actual circuit in order to meet the design specifications, $\boldsymbol{A_{Vmin}}$ **= -5 V/V**. Also, you should not include $\boldsymbol{R_{SIG}}$ because it represents the internal resistance of the function generator.

1. Assemble the circuit using values from pre-lab.

2. Using a digital multimeter, measure the DC voltages at the gate (V_G), source (V_S), and drain (V_D).
3. Using the function generator, apply an input $\boldsymbol{v_{SIG}}$ of 50 mV_{pk-pk} at 1 kHz.
4. Using oscilloscope, plot v_0 and v_i vs. time.
5. Measure all the resistors to three significant digits.
6. Calculate V_{GS}, V_{DS}, and I_D based on the above measurements.
7. What is the measured value of Av ?
8. What is the maximum gain that you can achieve without distorting the output signal?
9.

<u>*Optional:*</u> Measure Ro as follows (it is important to know Ro so that you would know what the next stage or the load sees as the overall amplifier resistance.)

Replace R_L with 1 MΩ resistor and repeat the AC measurements. Note the amplitude of the output waveform. Now adjust R_L such that the output amplitude is 50% of what it was for 1 MΩ load. This new value of R_L is the output resistance Ro.

1. How does it compare with your calculations and simulations? Note that this value of Ro cannot be greater than RD.
2. What is Rin (looking into the gate of the transistor)?

Part 1	R1	R2	VG	VS	RS	VD	RD	ID	Vov	VGS	VDS	Gain Av
Theoretical	4.70E+06	4.70E+06	7.5	5.34	5.34E+03	14.6	4.18E+02	1.00E-03	0.1596	2.16	9.26	-5
Simulated	3.00E+06	3.00E+06	7.5	5.36	5.34E+03	14.6	4.18E+02	1.00E-03	1.6	2.14	9.24	-3.78
Measured	4.60E+06	4.60E+06	6	5.3	4.90E+03	14.5	4.60E+02	1.08E-03	-1.3	0.7	9.2	-4
Difference (percent)	2.1277	2.1277	20.0000	0.7491	8.2397	0.6849	-10.0478	-8.0000	914.5363	67.5926	0.6479	

Lab 4 a)

Procedure:

<u>Part1: Measuring Vtn</u>

Simulate:

1. For the circuit shown in Fig. 1, set V_{DS} = 5V.
2. Sweep the gate voltage from 0V to 5V in increments of 0.1V.
3. Plot a curve for I_D vs. V_{GS}.
4. Note the value of VGS at which the current turns on. This is the Vtn for the particular NMOS.

Build:

1. Set V_{DS} to a constant 5V.
2. Sweep V_{GS} from 1V to 3.5V in increments of 0.25V, and measure the drain current from the power supply.

Note: If the power supply is not capable of measuring small values of current (in μA), add a 100Ω resistor in series to the drain end and measure the voltage drop across it to obtain the current.

3. Plot the I_D vs. V_{GS} curve on an engineering paper.
4. Note the value of V_{GS} at which the current turns on.

Part 2: Measuring kn

Simulate:

1. For the circuit shown in Fig. 2, set Vin = 12V.
2. Measure the current flowing through the NMOS, i_D.
3. Measure the voltage across the 1kΩ resistor.
4. Calculate the voltage drop V_{DS} and V_{GS} based on KVL.
5. Using Vtn value from Part 1, and saturation current equation (ignoring λ), calculate kn.

Build:

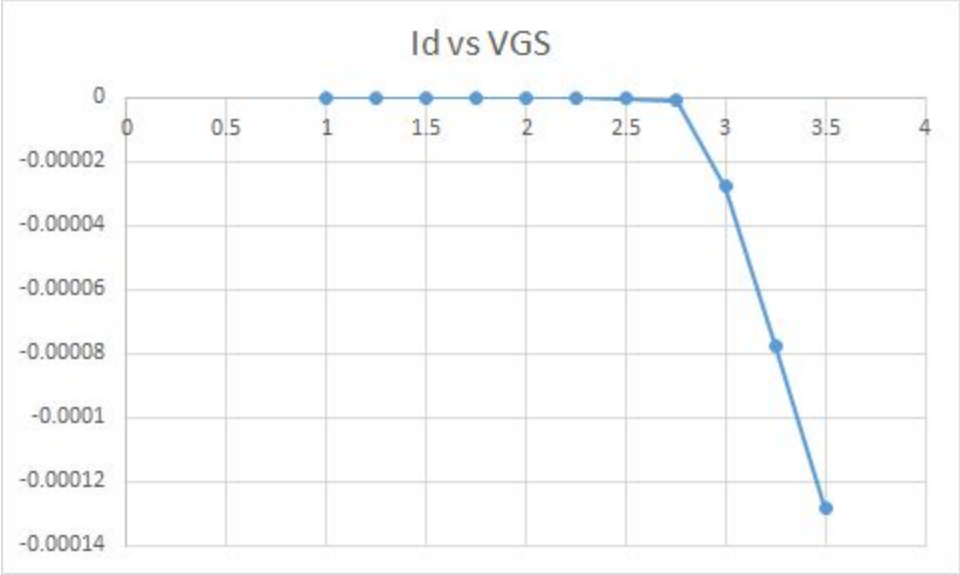
1. For the circuit shown in Fig. 2, set Vin = 12V.
2. Measure the voltage across the 1kΩ resistor. The remaining drop is across the NMOS.
3. Using the voltage drop across the resistor determine the current flowing through the transistor.
4. Using Vtn value from Part 1, and saturation current equation (ignoring λ), calculate kn.

Conclusion:

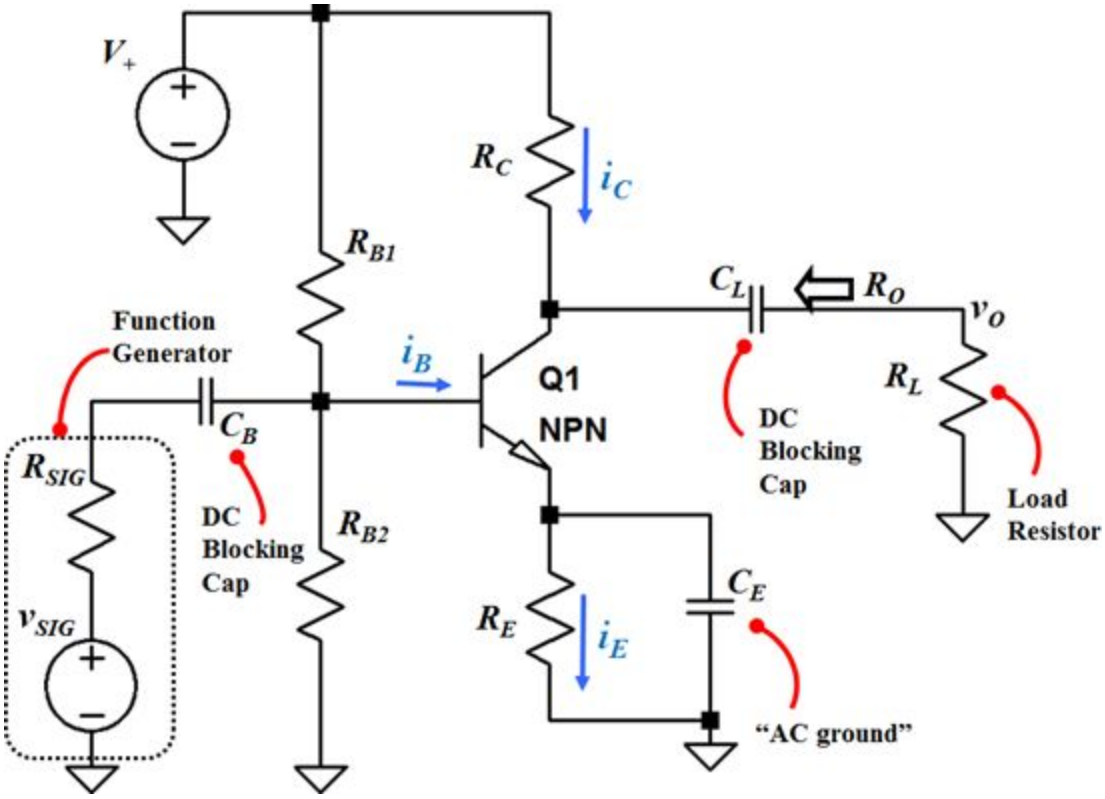
1. Summarize the simulated and measured values for Vt and Kn in a table. Explain any discrepancy.

2. Keep this transistor with you for the future NMOS labs.

Vt	Kn
Simulated 1.9V	80.1 mA/V2
Measured 2.0V	80.8



Lab 6: NPN Common Emitter Amplifier



Preliminary:

*Design/ Calculate: (*Use Example 5.10 as a guide, but note that we don't have the feedback R_G)

Design the amplifier circuit to achieve a small-signal gain of at least $\boldsymbol{A_V}$ = -200 V/V and $\boldsymbol{I_C}$ = 1 mA. Use $\boldsymbol{V_{CC}}$=15 V, $\boldsymbol{R_{SIG}}$ = 50 Ω, $\boldsymbol{R_L}$ = 10 kΩ, $\boldsymbol{R_{B1}}$ = 80 kΩ, and $\boldsymbol{R_{G2}}$ = 20 kΩ.

<u>Part 1:</u> DC Analysis

1. Sketch the DC model of the circuit in your lab book.

<u>Note:</u> Replace the capacitors with open circuit.

2. Calculate $\boldsymbol{I_B}$ and $\boldsymbol{I_E}$. What is the value of $\boldsymbol{V_B}$?

3. Determine the value of $\boldsymbol{R_E}$ that produces $v_{\mathbf{BE}}$ = 0.7 V. What is $\boldsymbol{V_E}$?

Note: At this stage, we know neither $\boldsymbol{V_{CE}}$ nor $\boldsymbol{R_C}$.

<u>Part 2:</u> AC (small-signal) Analysis

1. Sketch small-signal model of the circuit in your lab book.

<u>Note:</u> Replace the transistor with its small-signal model, capacitors with short circuits, and V_+ with an AC ground. Assume V_A is large, and ignore r_O. What would happen to R_E?

2. Label the base of the transistor as v_i, i.e. the small-signal voltage at the input. What are the values of $\boldsymbol{g_m}$ and $\boldsymbol{r_\pi}$?

3. Find the ratio, $\boldsymbol{v_i / v_{SIG}}$.

4. Derive the expression for $A_V = v_o / v_i$. What is the value of R_C that produces a small-signal gain of at least $A_V = -200\ V/V$? What would be the overall gain G_V?

5. What is the DC voltage at the collector, V_C? What region is the transistor operating in?

6. What is the output resistance, R_o?

Simulate:

1. Using the values found above, and $\boldsymbol{C_G} = \boldsymbol{C_L} = \boldsymbol{C_S} = 47\ \mu$F, simulate the circuit.

2. Set the input v_{sig} to 10mVpp, 1kHz with no DC component.

3. Record the DC values: V_{BE}, V_{CE}, I_B, I_C and I_E.

4. Determine *Av and* G_V.

Procedure:

Note: You may need to adjust values of the components as necessary in the actual circuit in order to meet the design specifications, $\boldsymbol{A_{Vmin}} = \mathbf{-200\ V/V}$. Also, you should not include $\boldsymbol{R_{SIG}}$ because it represents the internal resistance of the function generator.

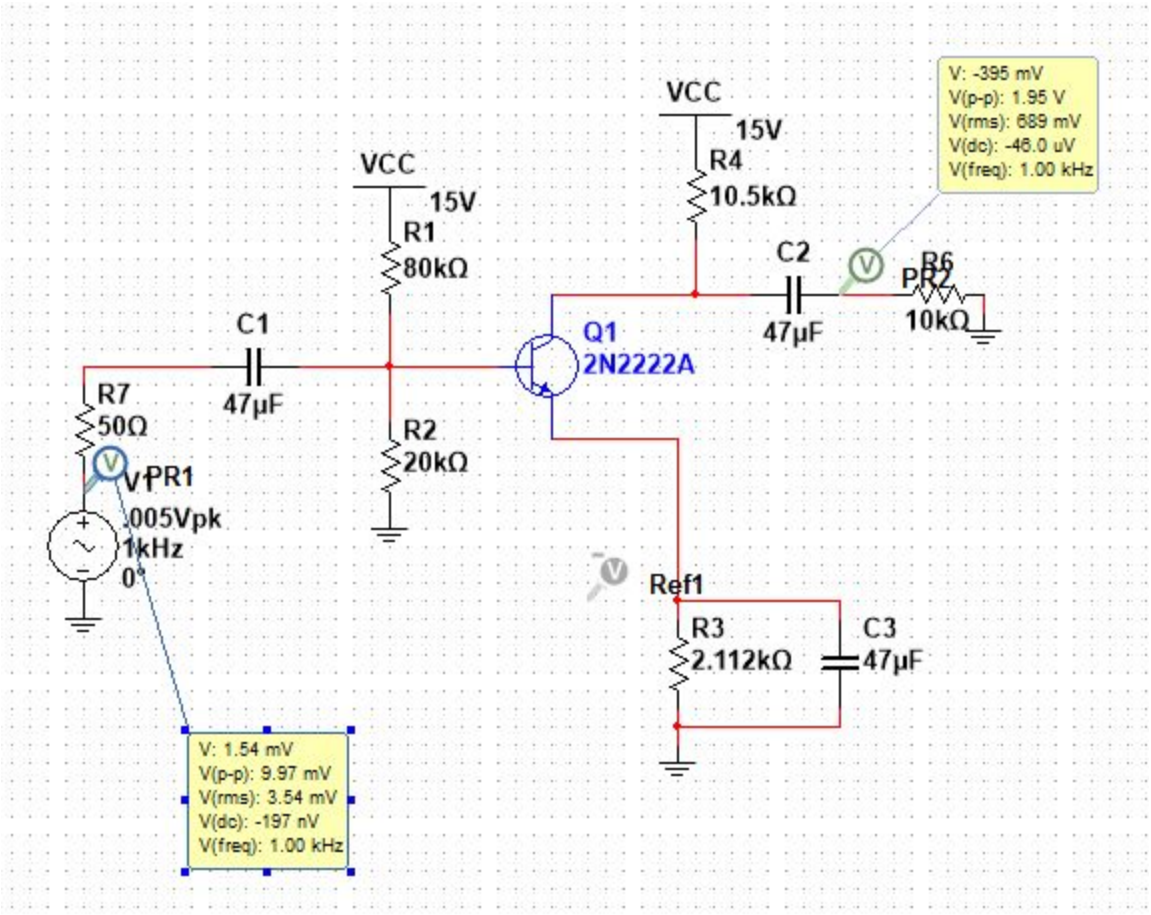
1. Assemble the circuit using values from pre-lab.
2. Measure the DC voltages at the base (V_B), emitter (V_E), and collector (V_C).
3. Apply an input $\boldsymbol{v_{SIG}}$ of 10 mVpp at 1 kHz.

Note: If 10mV is not available, use the smallest amplitude possible, but expect some distortion in the output waveform.

4. Generate the plots for v_0 and v_i vs. time.
5. Measure all the resistors to three significant digits.
6. Calculate V_{BE}, V_{CE}, I_B, I_C and I_E based on the above measurements.
7. What is the measured value of *Av and* G_V ?
8. Increase the input voltage amplitude until you start seeing distortion in the output voltage. What is the maximum gain that you can achieve without distorting the output signal?

	Measured	Theoretical
Rb1	80k	78.5k
Rb2	20k	22k
RL	10k	10.4k
Rc	10.5k	10.4k
Re	2.1k	1.83k

	Measured	Simulated	Calculated
Vb	2.93	2.92	2.83
Vc	2.5	3.7	4.1
Ve	2.39	2.29	2.13
Vbe	0.54	0.63	
Vce	0.11	1.4	
Gv	-	194.633	
Av	-	197.421	200



Conclusion:

1. Summarize the calculated, simulated, and measured results in a tabular form. The table should include the following parameters: V_{BE}, V_{CE}, I_B, I_C, I_E, *Av and Gv*. Explain any discrepancies.

Get your summary table checked off by the instructor.