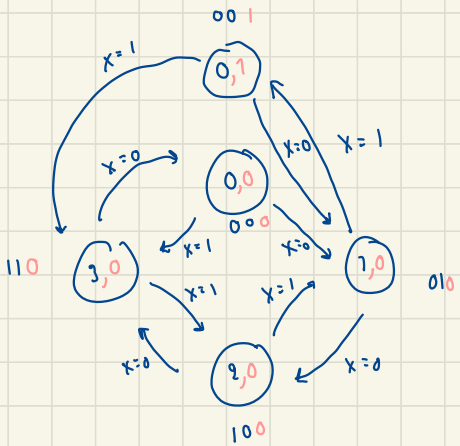
State Machine



transition table

X	$Q1_{t-1}$	$Q0_{t-1}$	$Q1_t$	$Q0_t$	New Output
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	1	0
1	1	1	1	0	0

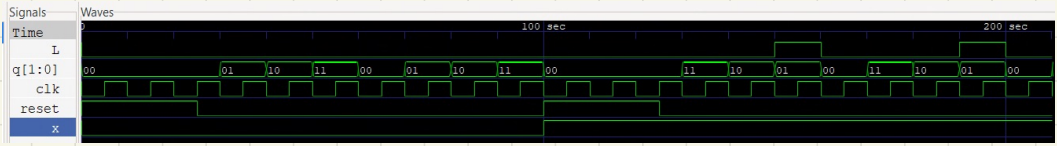
K-map New output

New output

X \ $Q1_{t-1}$ $Q0_{t-1}$	00	01	11	00
0	0	0	0	0
1	0	1	0	0

New output = $X \overline{Q1}\, Q0$

ผลการทำงาน




```
 25 output L = 0  q = 0 (00) reset = 0 x = 0
 30 output L = 0  q = 1 (01) reset = 0 x = 0
 40 output L = 0  q = 2 (10) reset = 0 x = 0
 50 output L = 0  q = 3 (11) reset = 0 x = 0
 60 output L = 0  q = 0 (00) reset = 0 x = 0
 70 output L = 0  q = 1 (01) reset = 0 x = 0
 80 output L = 0  q = 2 (10) reset = 0 x = 0
 90 output L = 0  q = 3 (11) reset = 0 x = 0
100 output L = 0  q = 0 (00) reset = 1 x = 1
125 output L = 0  q = 0 (00) reset = 0 x = 1
130 output L = 0  q = 3 (11) reset = 0 x = 1
140 output L = 0  q = 2 (10) reset = 0 x = 1
150 output L = 1  q = 1 (01) reset = 0 x = 1
160 output L = 0  q = 0 (00) reset = 0 x = 1
170 output L = 0  q = 3 (11) reset = 0 x = 1
180 output L = 0  q = 2 (10) reset = 0 x = 1
190 output L = 1  q = 1 (01) reset = 0 x = 1
200 output L = 0  q = 0 (00) reset = 0 x = 1
```

L จะเป็น 1 ก็ต่อเมื่อ อยู่ใน state 01 และ
อินพุท x เป็น 1

โครงสร้าง Verilog