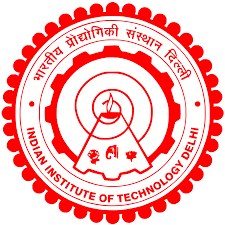
**INDIAN INSTITUTE OF TECHNOLOGY, DELHI**

****

**SESSION:2021-22**

**PROJECT REPORT**

**COURSE: IEC LABORATORY**

**TASK: DESIGN A MOD-5 SYNCHRONOUS COUNTER USING JK FLIP FLOP**

***SUBMITTED BY: RIYA CHORDIA***

***ENTRY NO: 2021EEN2024***

***MTECH PROGRAMME: INTEGRATED ELECTRONICS AND CIRCUITS***

***TARGETS ACHIEVED:***

* ***MOD-5 Synchronous counter is made using master-slave JK flip flop.***
* ***The counter counts from 0 to 4.***
* ***All layouts are made from scratch with a minimum height of 1.4 micrometre.***
* ***Width of MOD 5 counter layout is 80.5 micrometres***
* ***Area= (1.4\*80.5) micrometres***

**=112.7 micrometres**

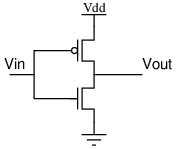
* **Timing information including rise time, fall time, propogation delay from low to high and high to low have been calculated for all the circuits and mentioned in the report.**
* **DRC, LVS and PEX analysis of all the circuits has been successfully done.**
* **Width of NMOS is kept 200nm and width of PMOS is kept 400nm.**
* **Clock frequency = 250MHz**
* **Schematics, simulations, layouts and post layout simulation of all the circuit blocks has been successfully done and are shown in this report.**

***TARGET REMAINING:***

* ***Setup time and hold time of sequential circuits.***

**INVERTER**

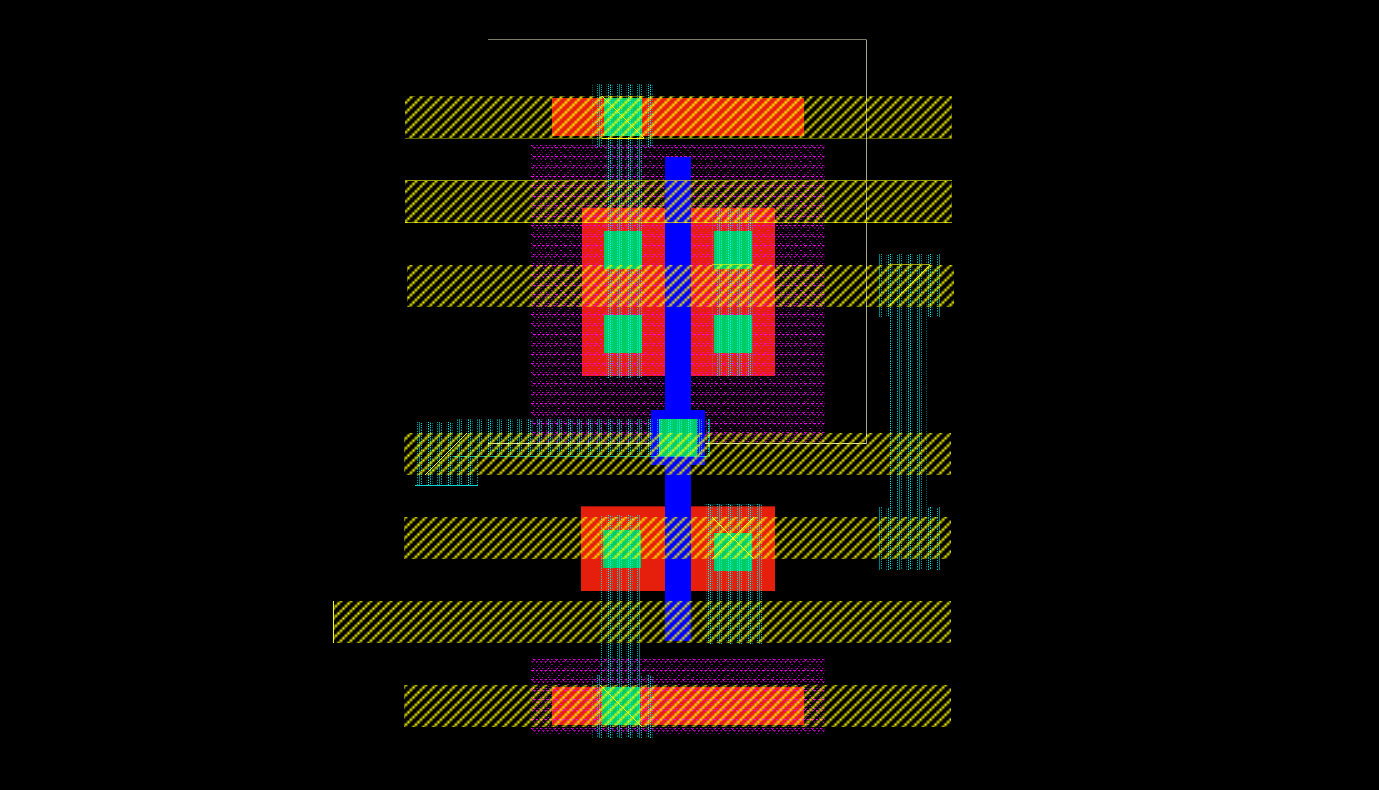
**Schematic Diagram:**

****

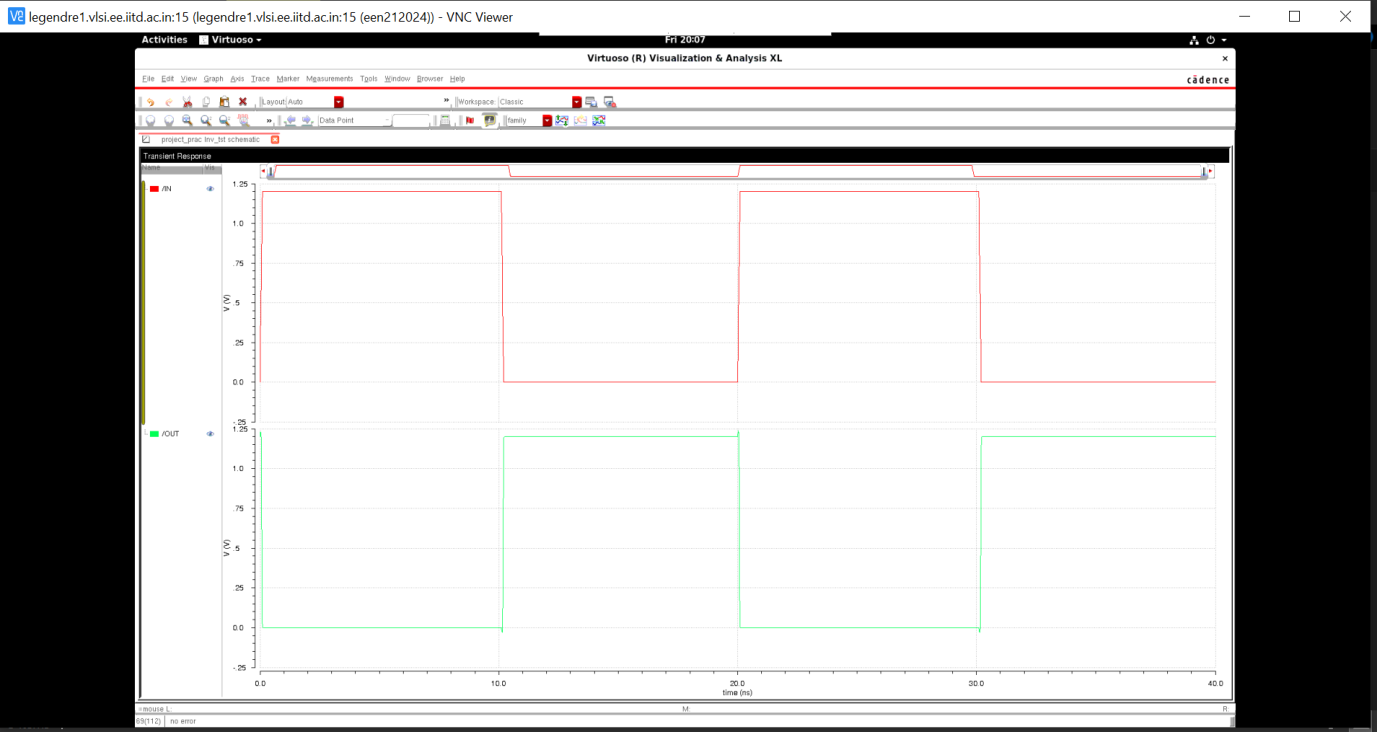
**Simulation:**

****

**Layout:**

****

**Post Layout Simulation:**

****

**TIMING INFORMATION:**

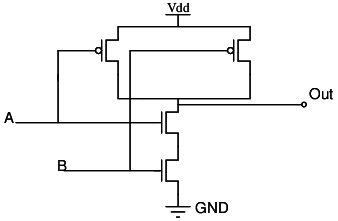
**RISE TIME: 13.47 E -21 s FALL TIME: 22.44p s**

**DELAY TIME: tpLH {low to high} and tpHL {high to low}**

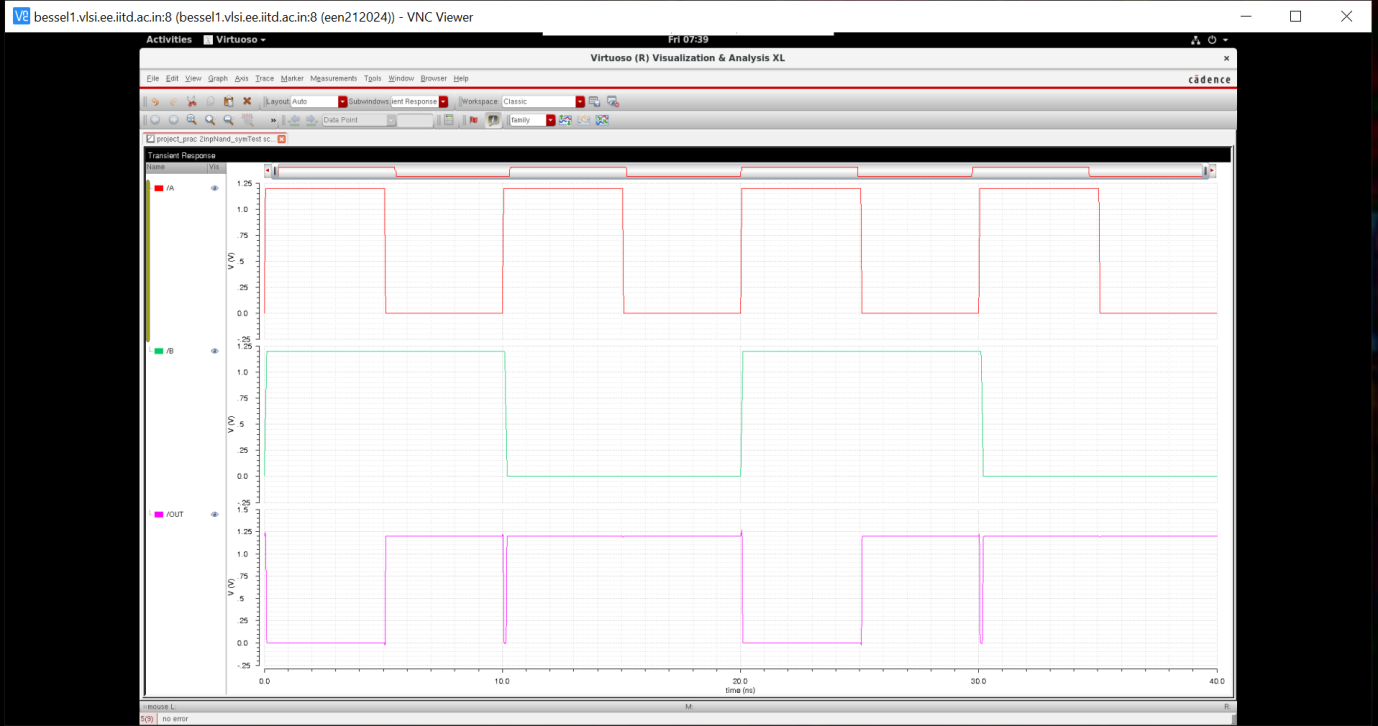
**TpLH: 16.78p s tpHL: 16.78p s**

**2 INPUT NAND GATE**

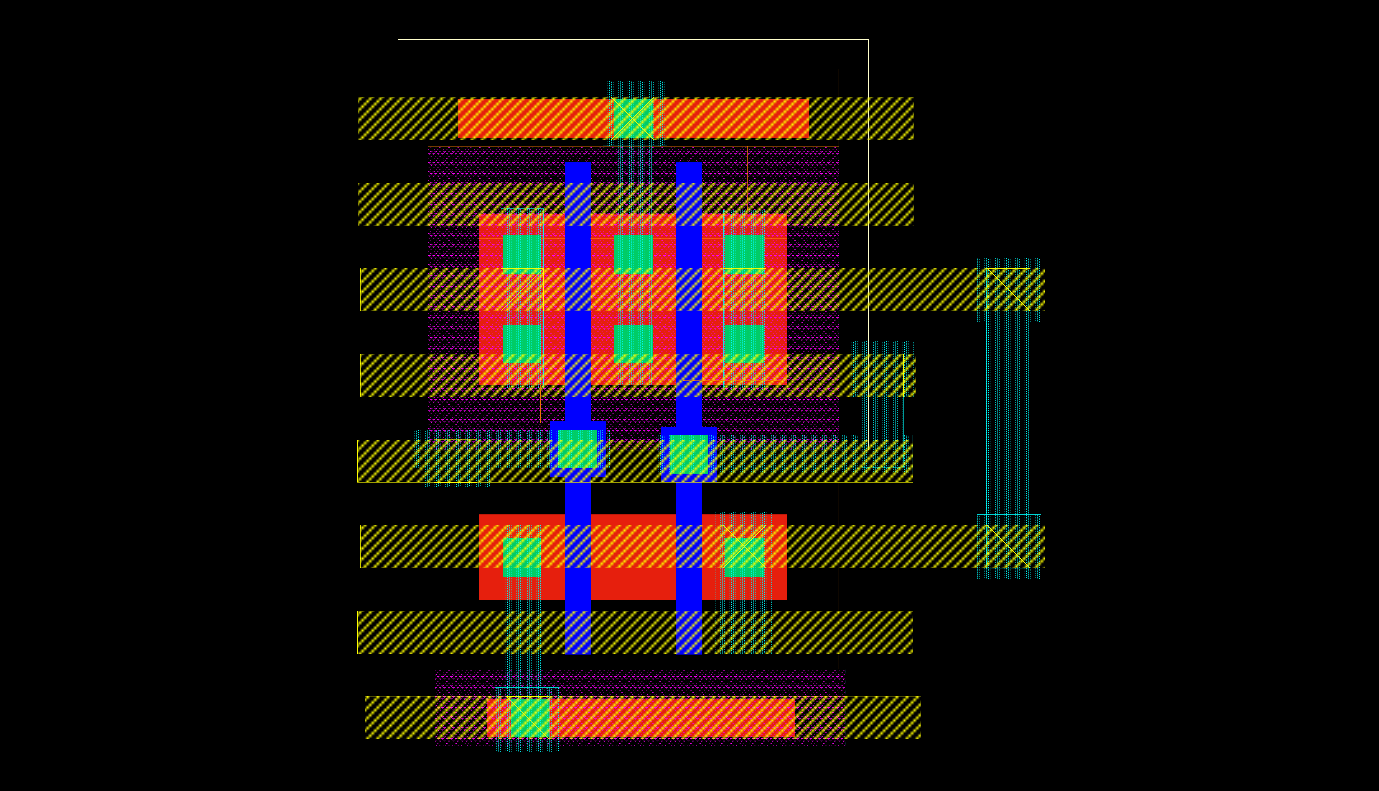
**Schematic Diagram:**

****

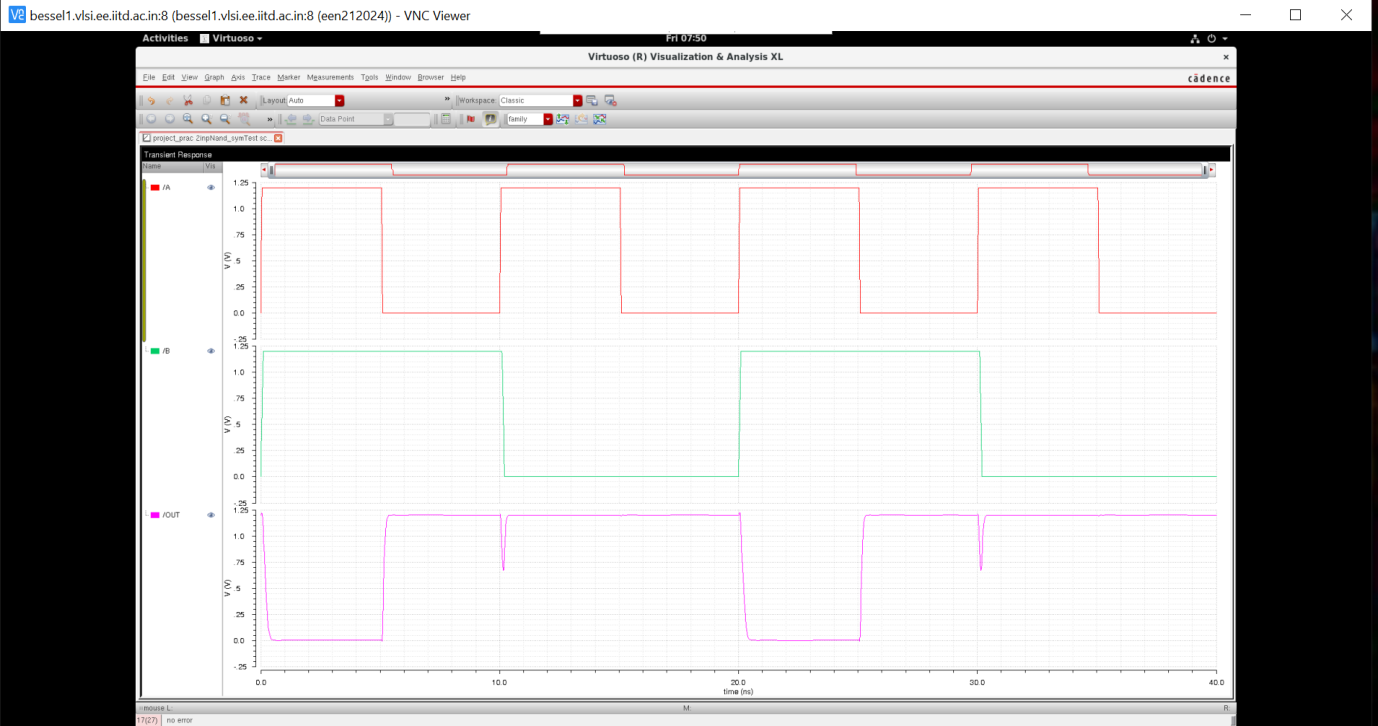
**Simulation:**

****

**Layout:**

****

**Post Layout Simulation:**

****

**TIMING INFORMATION:**

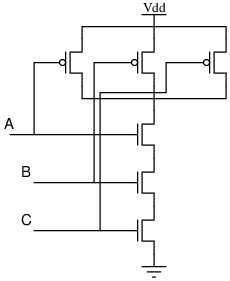
**RISE TIME: 196.8E-18 s FALL TIME: 23.83p s**

**DELAY TIME: tpLH {low to high} and TpHL {high to low}**

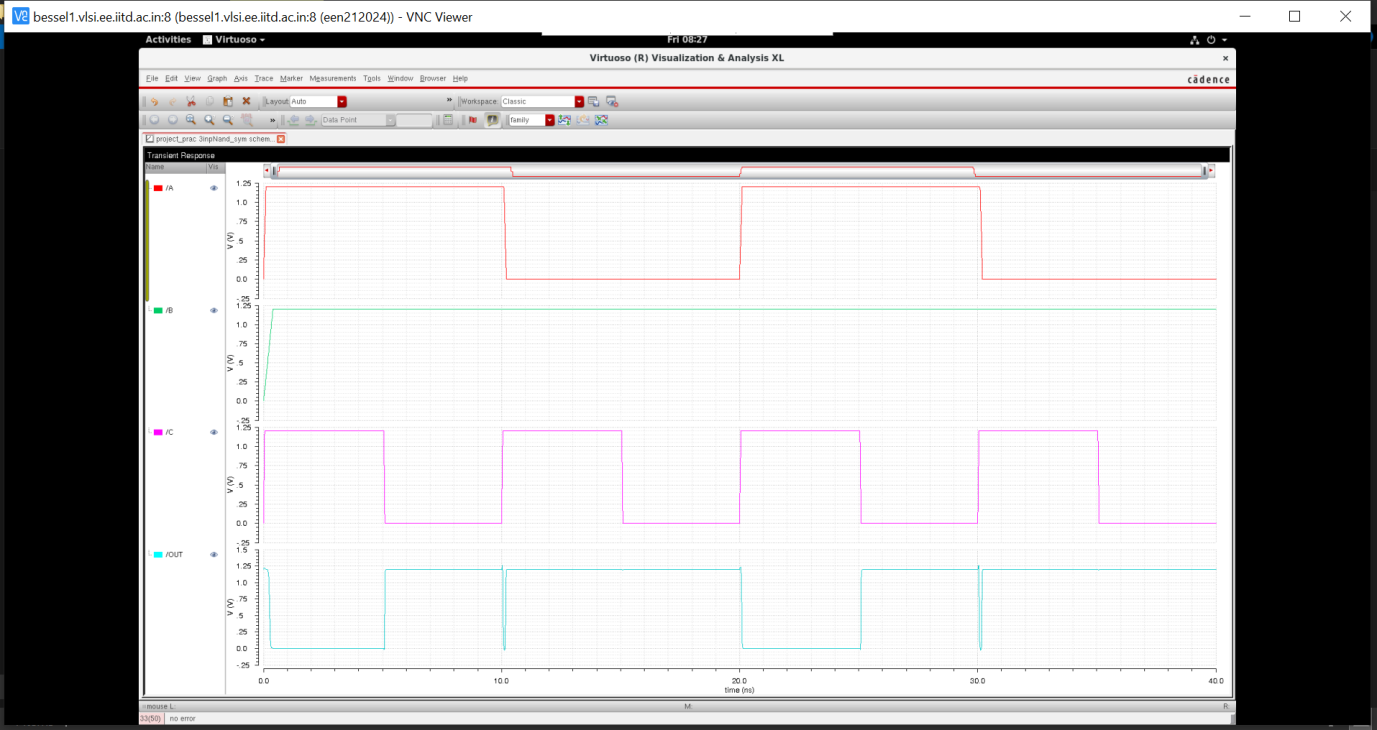
**TpLH: 5.096n s tpHL: 9.951n s**

**3 INPUT NAND GATE**

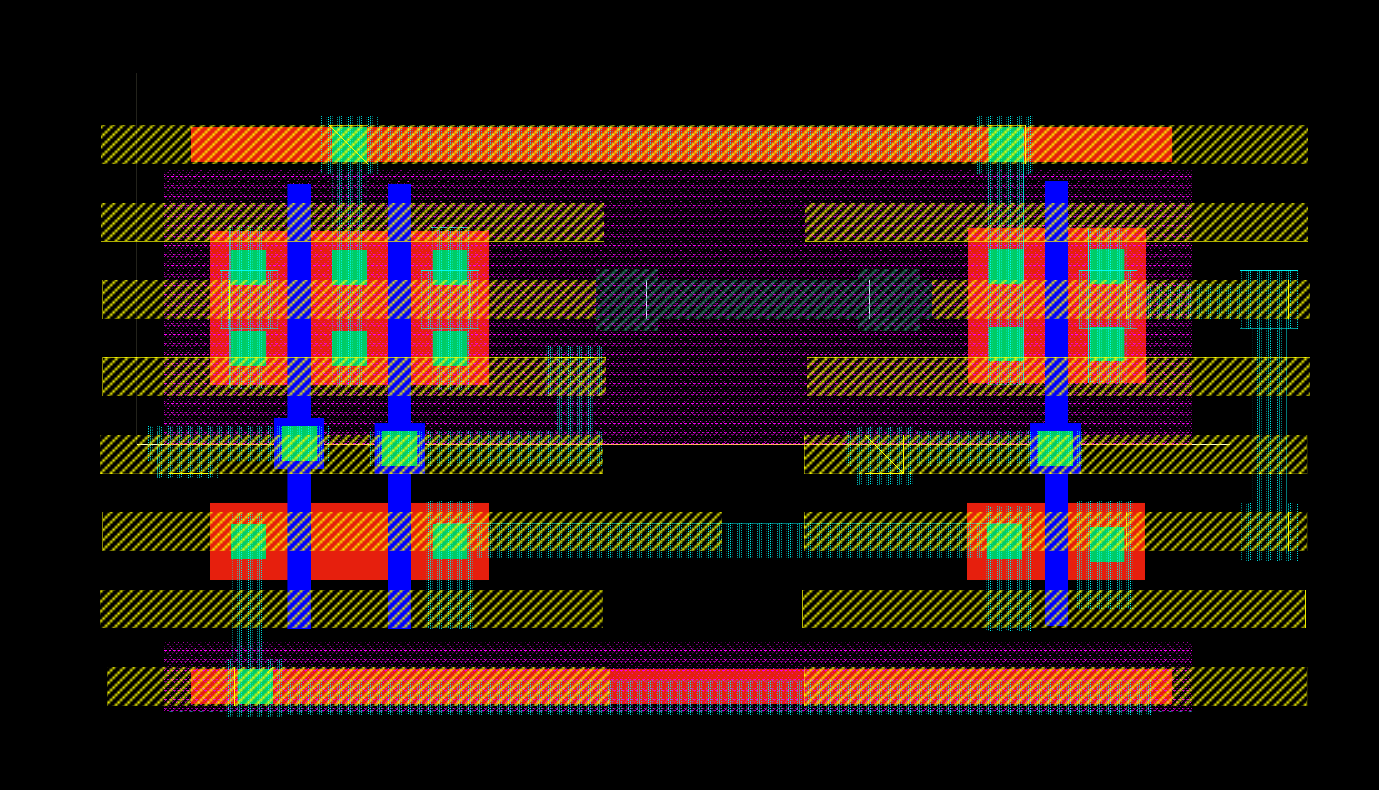
**Schematic Diagram:**

****

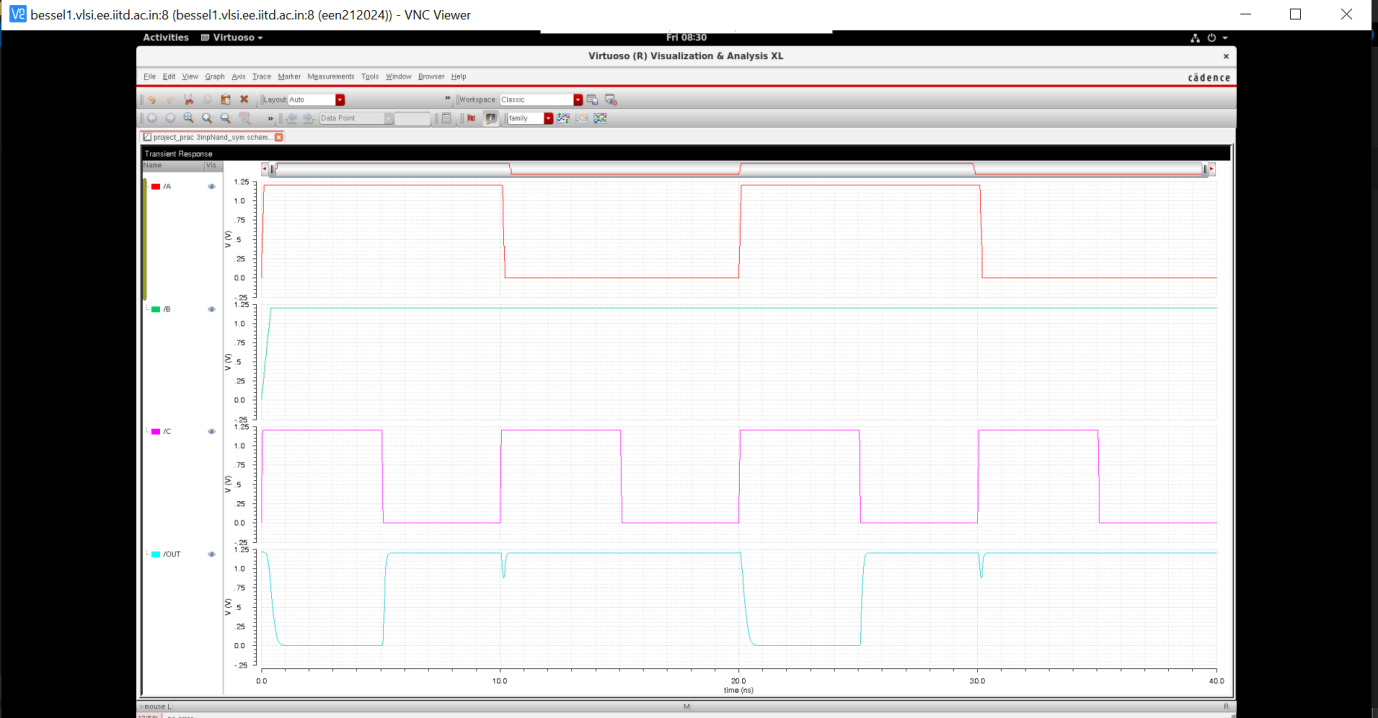
**Simulation:**

****

**Layout:**

****

**Post Layout Simulation:**

****

**TIMING INFORMATION:**

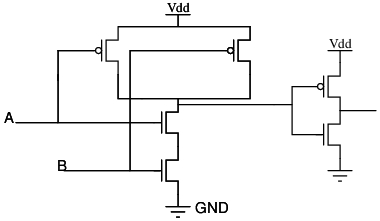
**RISE TIME: 354.3p s FALL TIME: 354.3p s**

**DELAY TIME: tpLH {low to high} and TpHL {high to low}**

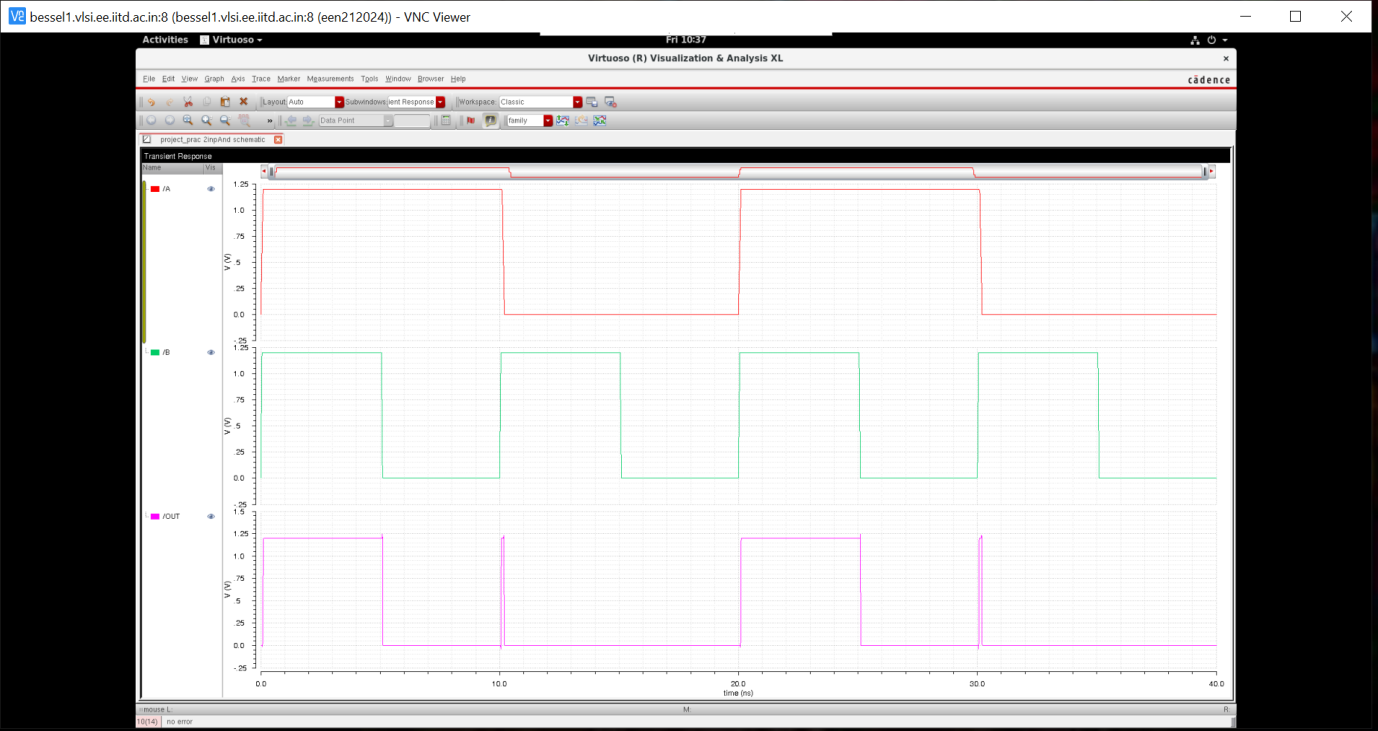
**TpLH: 20.08E-9 s tpHL: 9.583E-9 s**

**AND GATE**

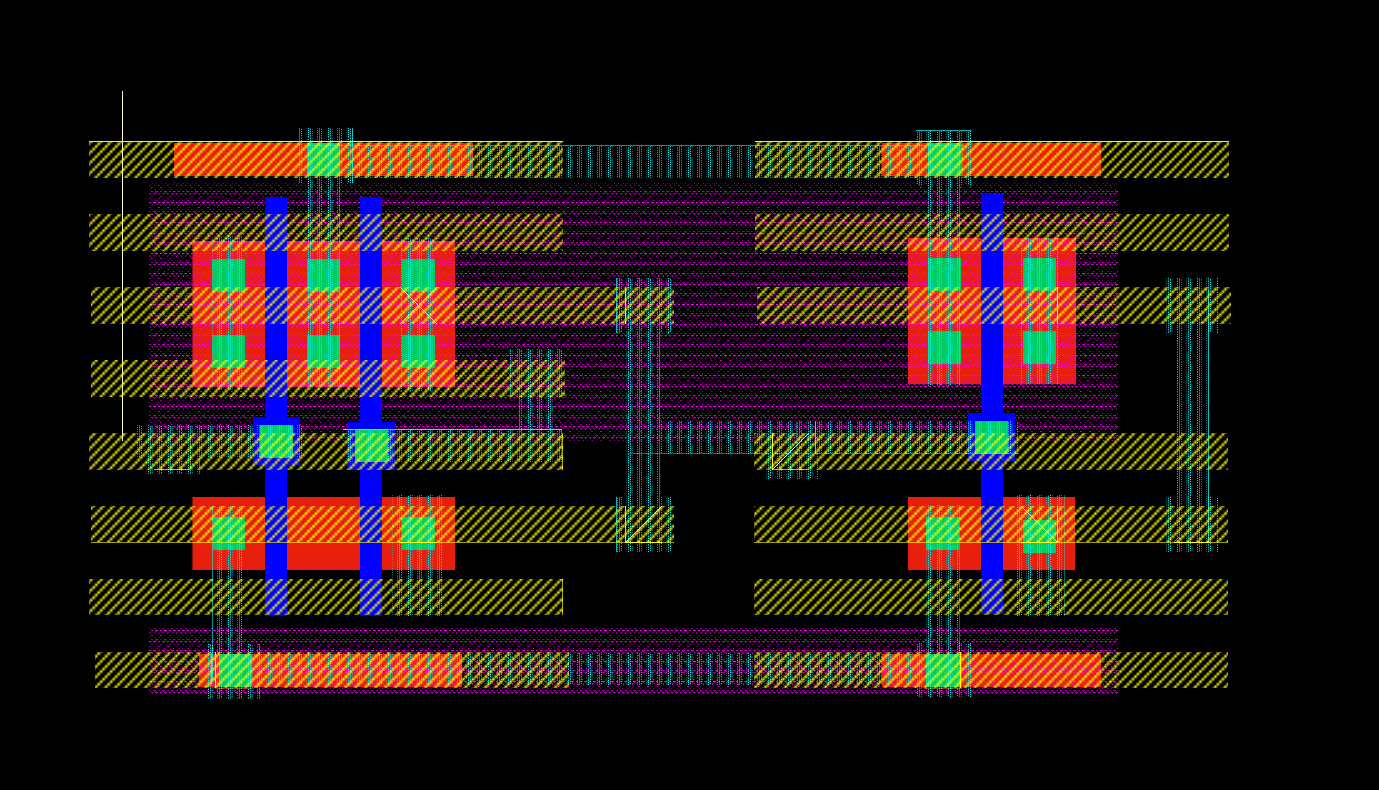
**Schematic Diagram:**

****

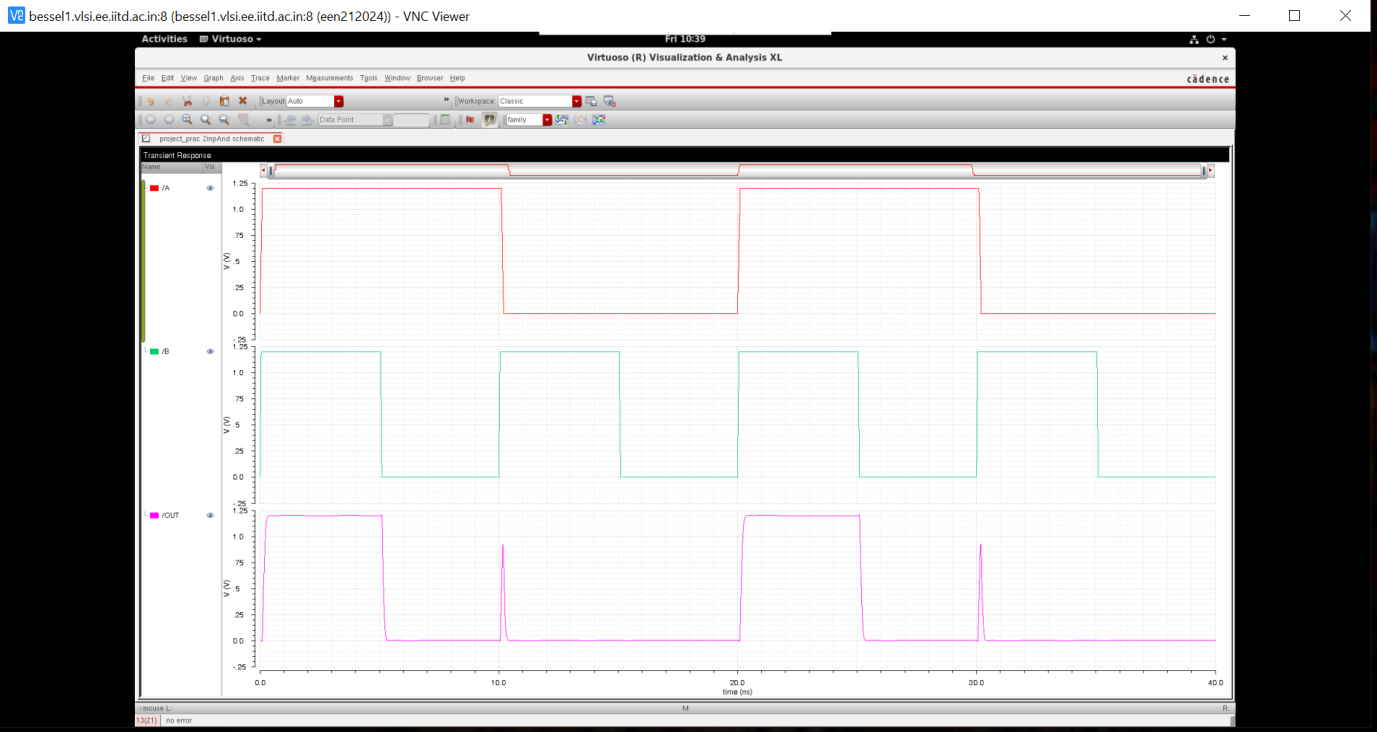
**Simulation:**

****

**Layout:**

****

**Post Layout Simulation:**

****

**TIMING INFORMATION:**

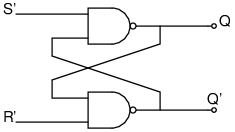
**RISE TIME: 2.049E -18 s FALL TIME: 123.3p s**

**DELAY TIME: tpLH {low to high} and TpHL {high to low}**

**TpLH: 5.049n s tpHL: 4.859n s**

**SR LATCH**

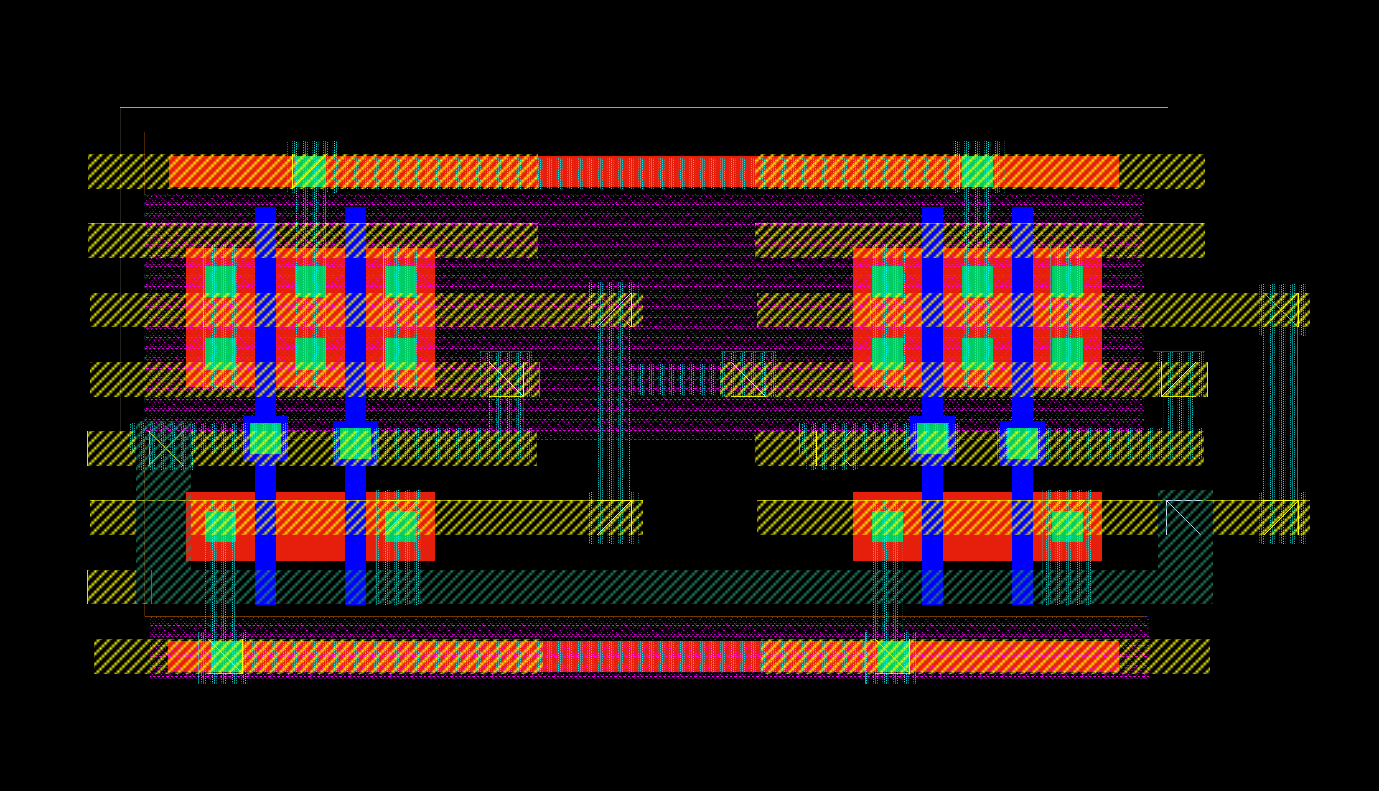
**Schematic Diagram:**

****

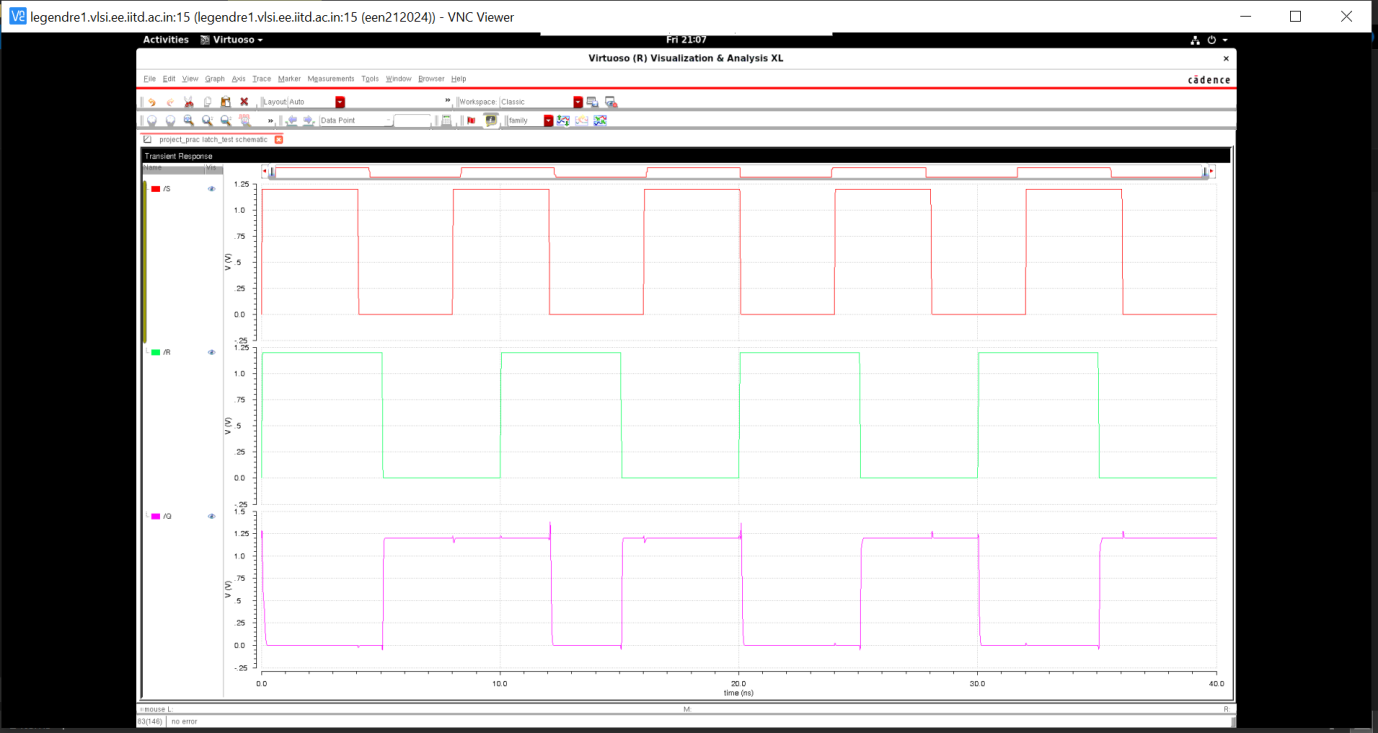
**Simulation:**

****

**Layout:**

****

**Post Layout Simulation:**

****

**TIMING:**

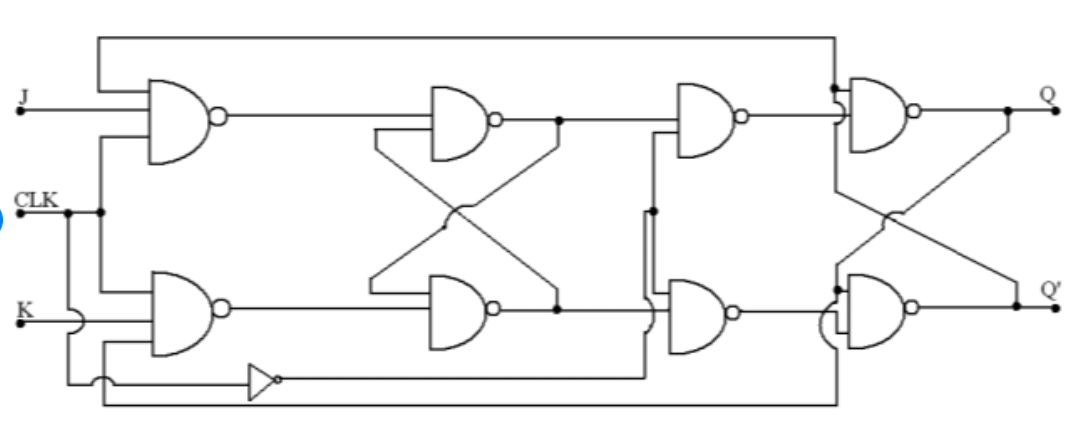
**RISE TIME: 218.3E -18 s FALL TIME: 124.3p s**

**DELAY TIME: tpLH {low to high} and TpHL {high to low}**

**TpLH: 6.78n s tpHL: 6.98n s**

**JK FLIP FLOP**

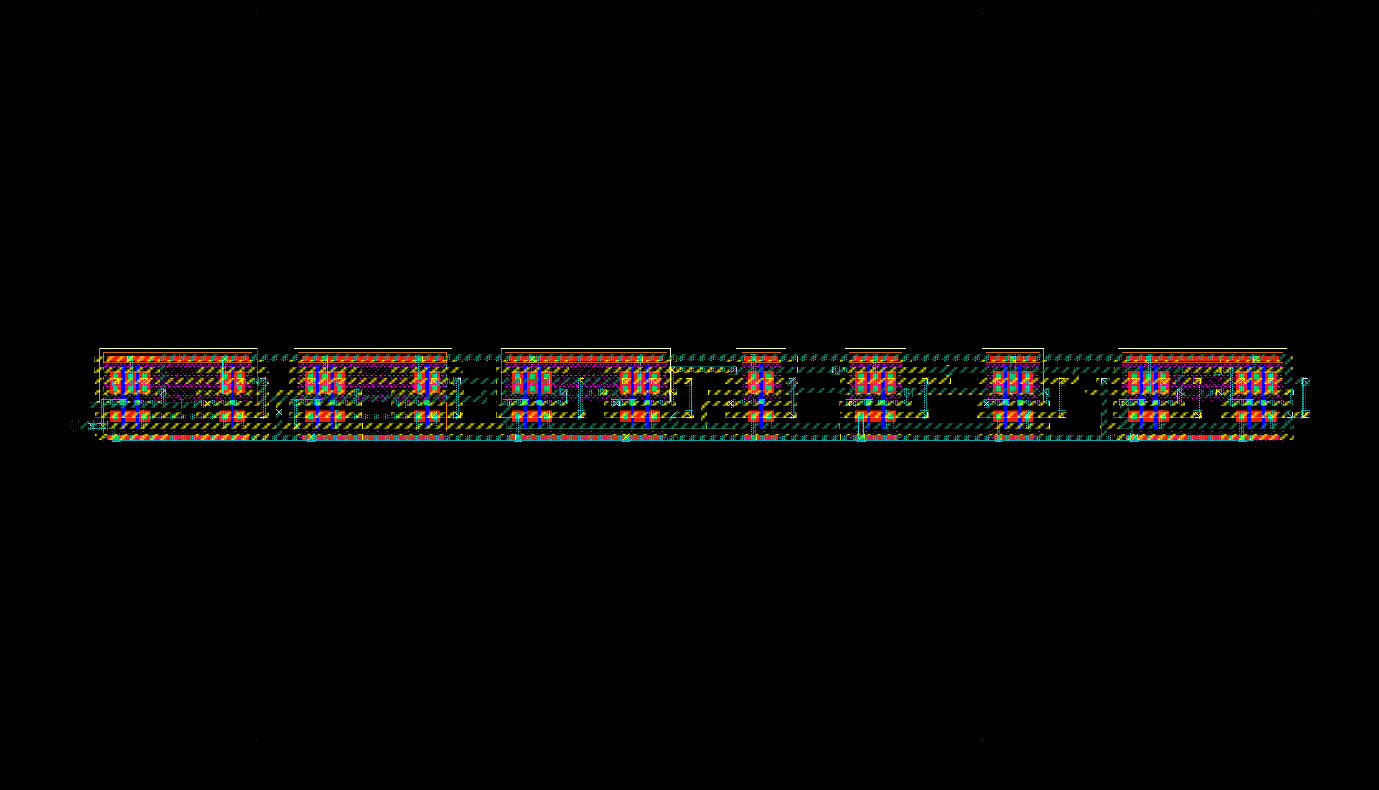
**Schematic Diagram:**

****

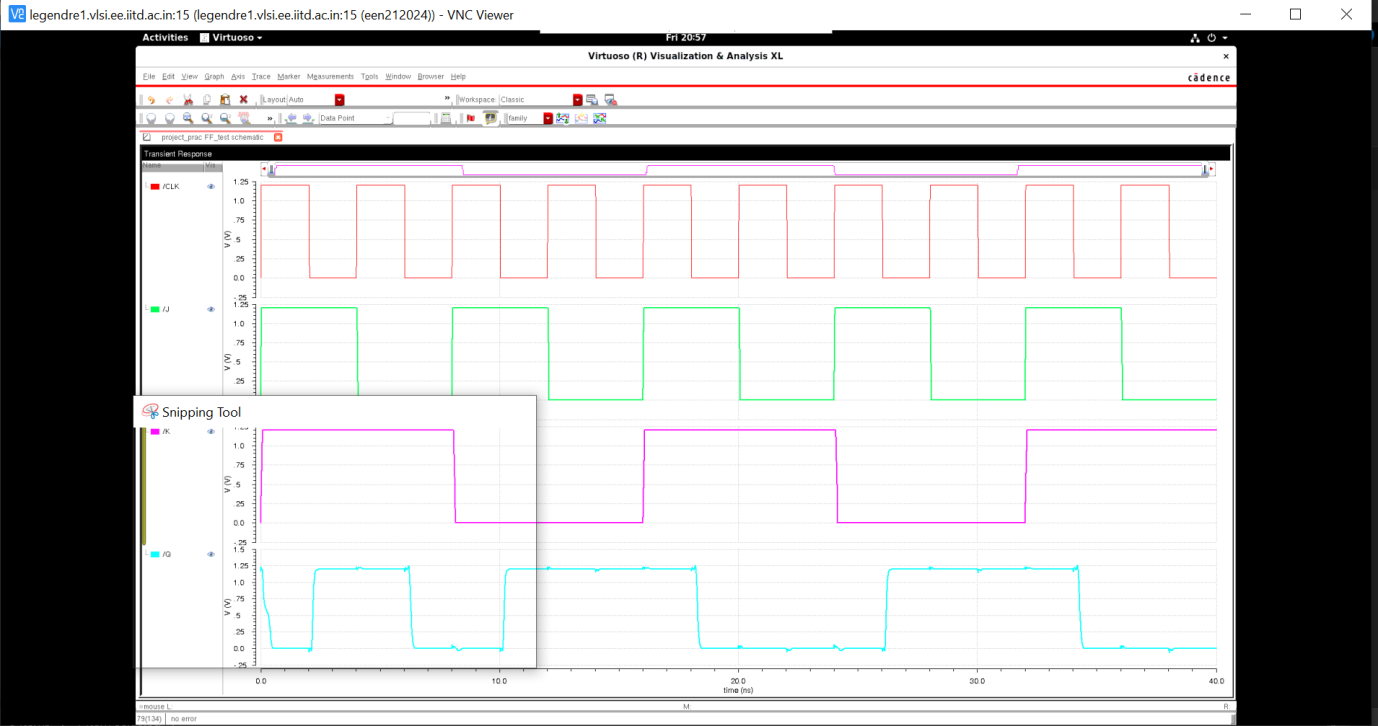
**Simulation:**

****

**Layout:**

****

**Post Layout Simulation:**

****

**TIMING INFORMATION:**

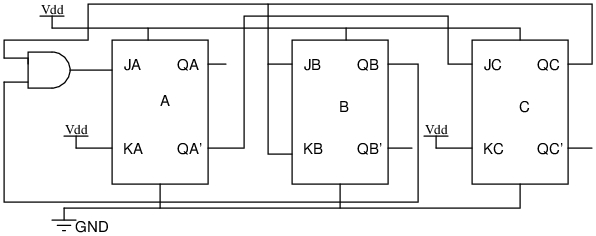
**RISE TIME: 330.2p s FALL TIME: 342.5p s**

**DELAY TIME: tpLH {low to high} and TpHL {high to low}**

**TpLH: 6.136n s tpHL: 7.087n s**

**COUNTER**

**Schematic Diagram:**

****

**Simulation:**

****

**Layout:**

****

**Post Layout Simulation:**

****

**TIMING INFORMATION(QA):**

**RISE TIME: 123.2p s FALL TIME: 121.5p s**

**DELAY TIME: tpLH {low to high} and TpHL {high to low}**

**TpLH: 6.285n s tpHL: 7.112n s**