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Entry No.: 2021EEN2024

IEC LAB ASSIGNMENT

PHYSICAL DESIGNING

MOD-5 COUNTER

(INNOVUS AND GENUS)

- All the steps have been performed and their resepective screenshots are attached in the report.
- Timing Reports (Setup and Hold time) are generated with zero violations.
- Power reports are being generated.
- DRC check, Geometry check and Connectivity check has been successfully done.
- Tcl and sdc files are shown in the report.
- Log files, command files, delays.sdf, counter.spef file and timing report obtained from genus have been added in the github folder.

Path of the files:

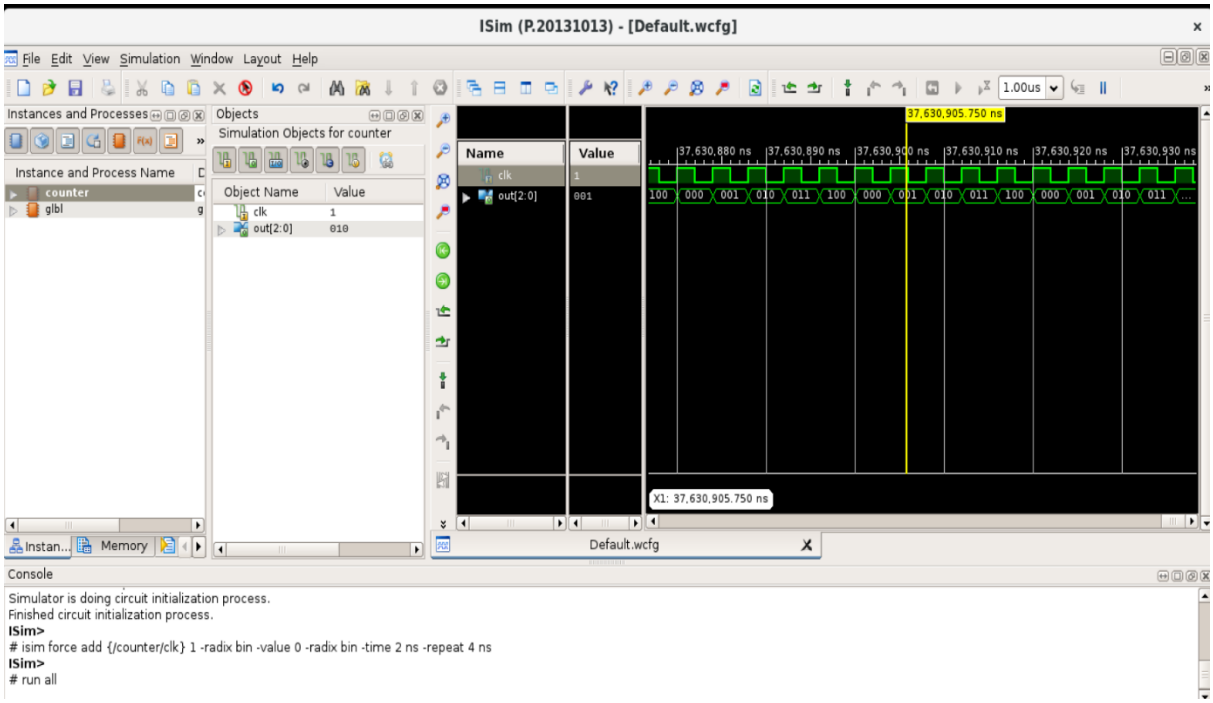
```
/afs/iitd.ac.in/user/e/ee/een212024/Physical/Labassignment/counterpd/
```

Verilog code: Counter.V

```
module counter(
 out      ,  // Output of the counter
 clk      // clock input
 );
 //----------Output Ports--------------
  output [2:0] out;
  //------------Input Ports--------------
  input clk;
  //------------Internal Variables--------
  reg [2:0] out;
  //-------------Code Starts Here-------
  always @(posedge clk)
 if (out<4)
  begin
   out <= out + 1;
  end
```

```
else
 begin
  out <= 2'b0 ;
 end
 endmodule
```

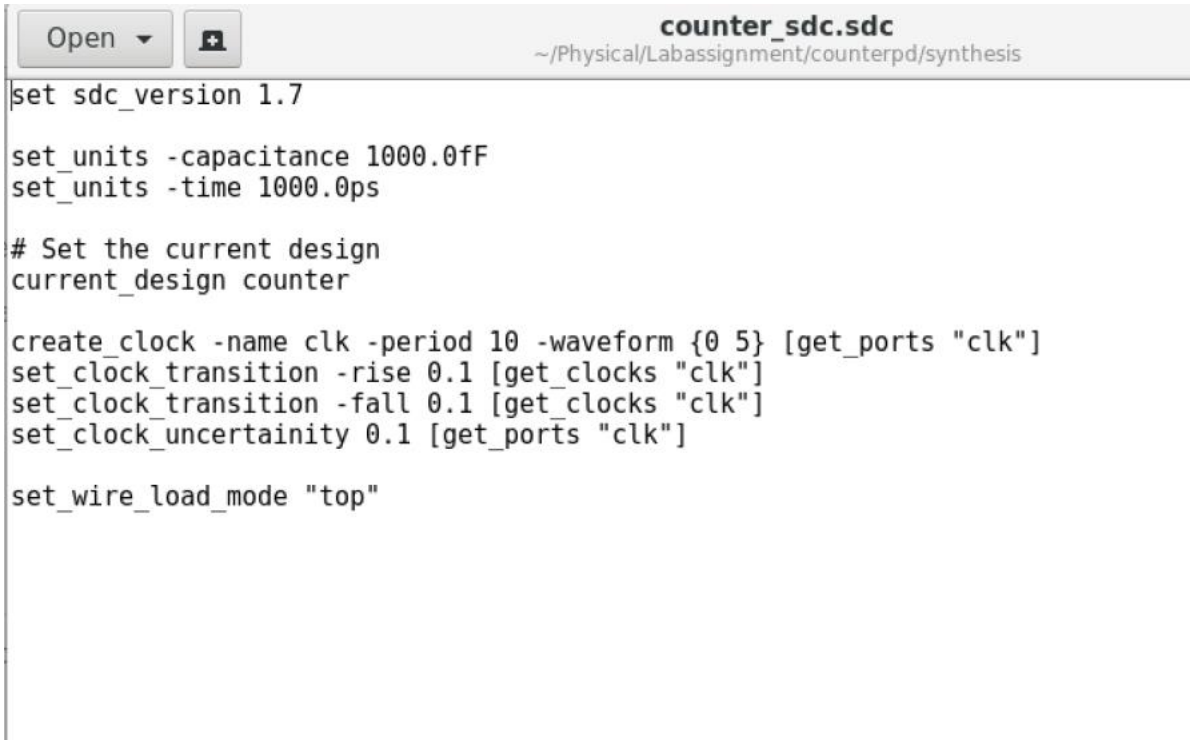
SIMULATION(ISE)



GENUS: Tool used for synthesis stage(converting RTL to a gate-level-netlist)

- Command to invoke the tools(file name:genuscmd1) have been added in the github folder.

SDC & TCL FILES:

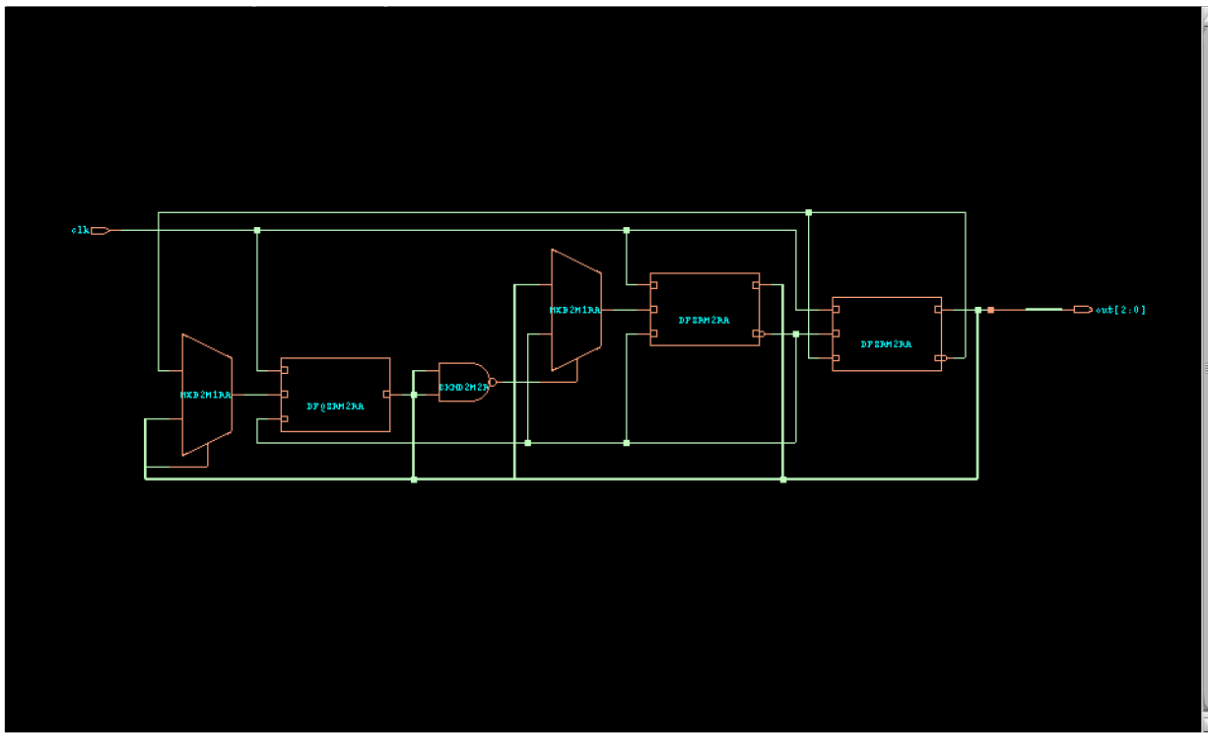


Open counter.tcl ~/Physical/Labassignment/counterpd/synthesis Save

counter_sdc.sdc | counter.tcl

```
set search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/
synopsys/ccs"
set_attribute lib_search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/
UMC65LLSC/synopsys/ccs"
set_attribute hdl_search_path "./rtl/"
set_attribute library "uk65lscllmvbbr_100c25_tc_ccs.lib"

read_hdl counter.v
elaborate
check_design -unresolved
read_sdc ./synthesis/counter_sdc.sdc
synthesize -to_mapped -effort medium
write_hdl > ./typical/counter_netlist.v
write_sdc > ./typical/counter.sdc
```

Loading genus and Generating Schematic:



Netlist Generated:

Open ▾ | counter_netlist.v | ~/Physical/Labassignment/counterpd/typical | Save

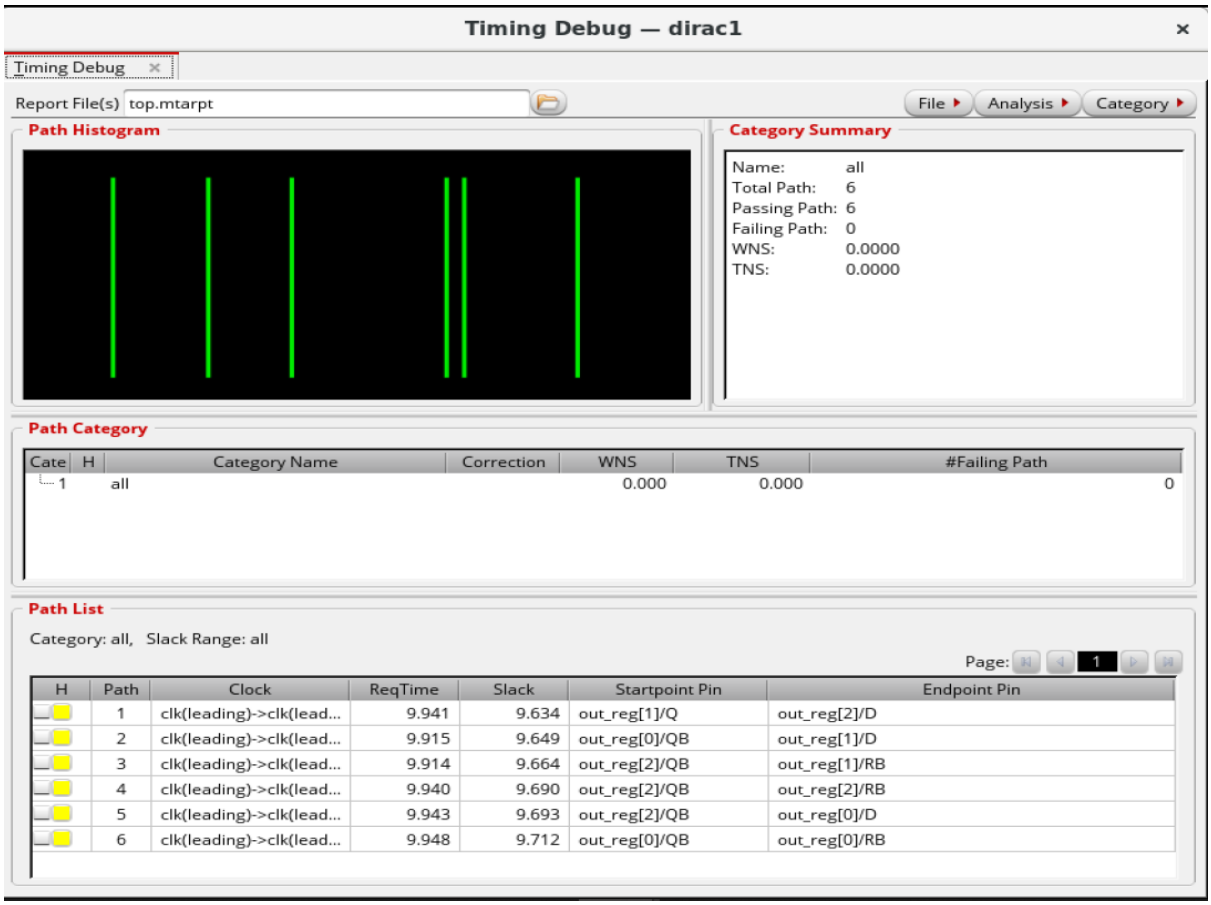
```
// Generated by Cadence Genus(TM) Synthesis Solution 19.12-s121_1
// Generated on: Oct 17 2021 09:49:55 IST (Oct 17 2021 04:19:55 UTC)

// Verification Directory fv/counter

module counter(out, clk);
  input clk;
  output [2:0] out;
  wire clk;
  wire [2:0] out;
  wire n_0, n_1, n_2, n_3, n_4;
  DFQZRM2RA \out_reg[1] (.CK (clk), .D (n_2), .RB (n_4), .Q (out[1]));
  MXB2M1RA g69(.A (out[2]), .B (n_4), .S (n_0), .Z (n_3));
  MXB2M1RA g71(.A (n_1), .B (out[0]), .S (out[1]), .Z (n_2));
  CKND2M2R g72(.A (out[0]), .B (out[1]), .Z (n_0));
  DFZRM2RA \out_reg[2] (.CK (clk), .D (n_3), .RB (n_4), .Q (out[2]),
       .QB (n_4));
  DFZRM2RA \out_reg[0] (.CK (clk), .D (n_4), .RB (n_1), .Q (out[0]),
       .QB (n_1));
endmodule
```

Sdc file generated:

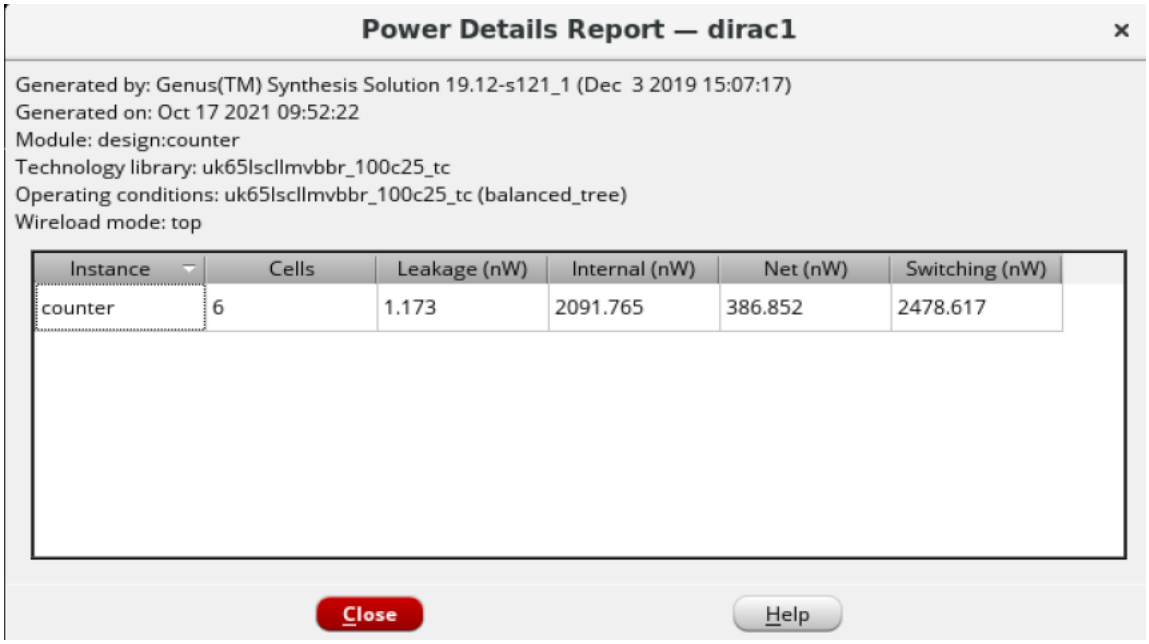
Open ▾ | counter.sdc | ~/Physical/Labassignment/counterpd/typical | Save | ≡

```
# ###############################################################

#  Created by Genus(TM) Synthesis Solution 19.12-s121_1 on Sun Oct 17 09:49:55 IST 2021

# ###############################################################

set sdc_version 2.0

set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design counter

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_wire_load_mode "top"
```

Generating Timing Reports (In genus) :

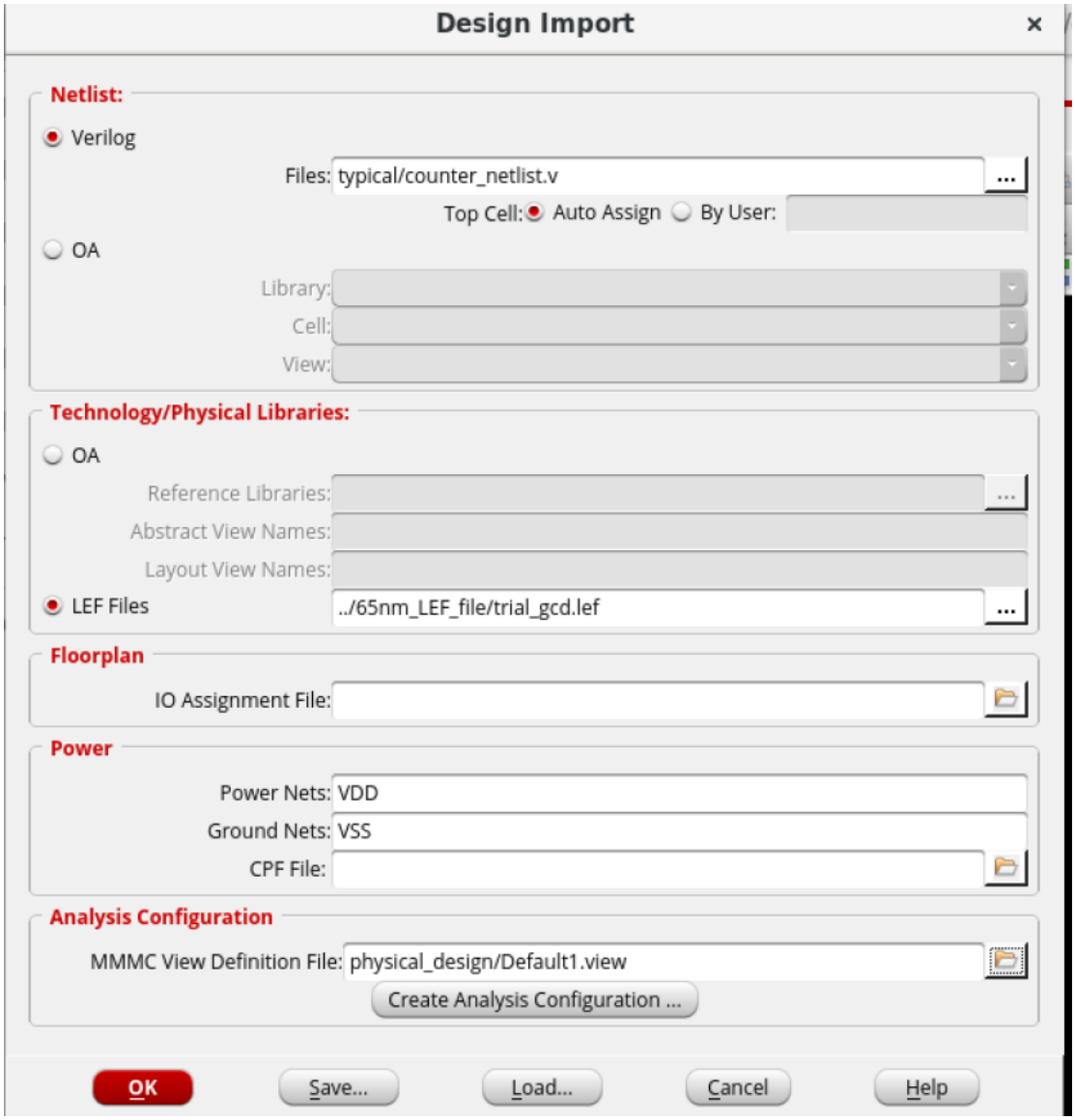


Generating Power Report:

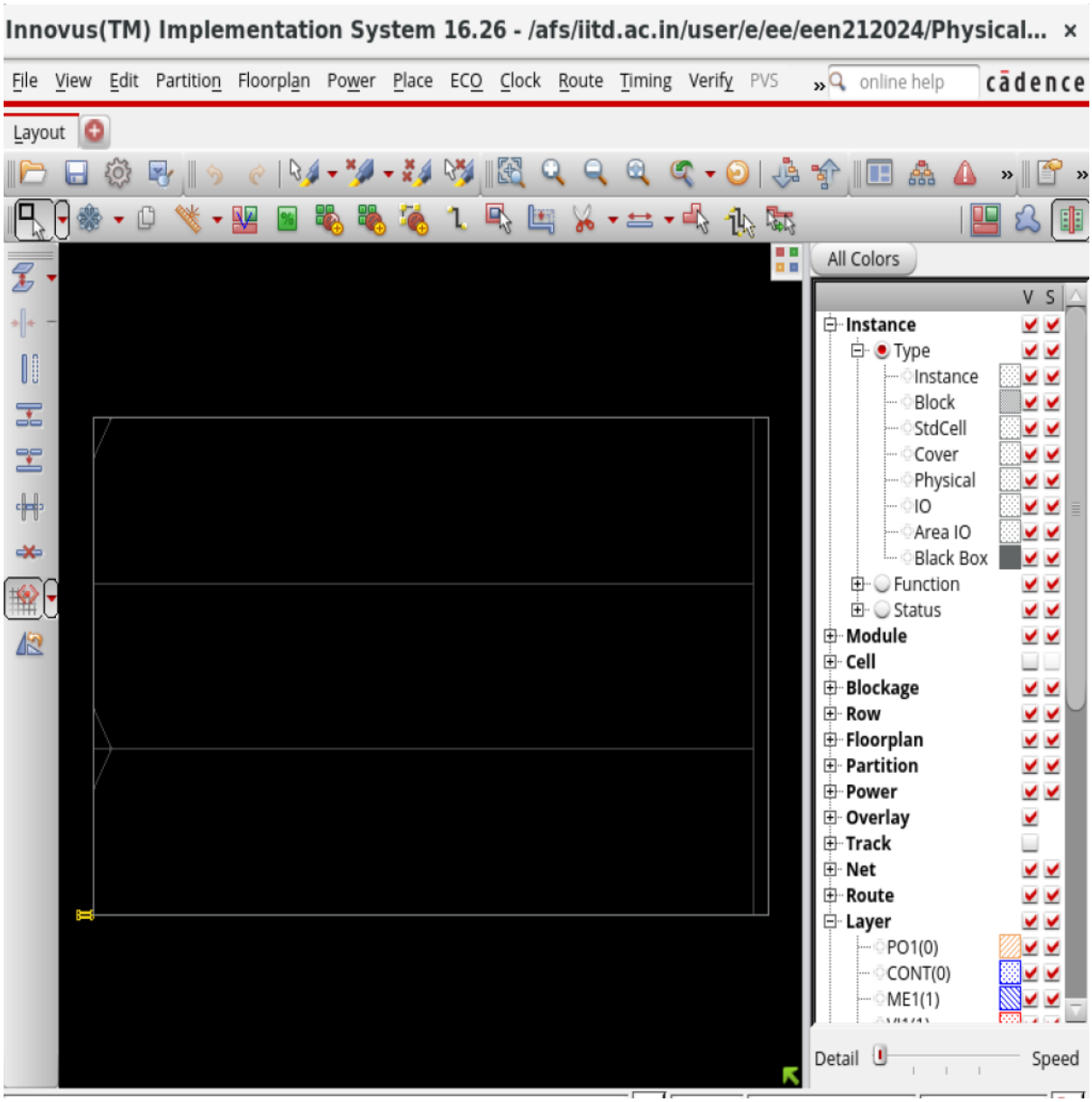


INNOVUS:

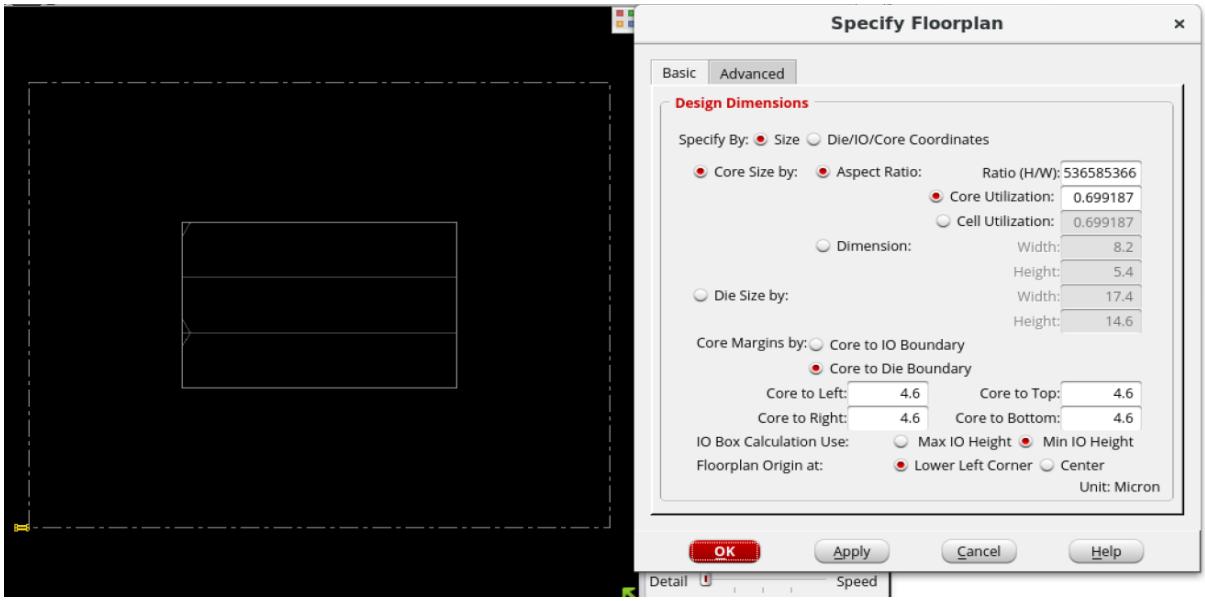
Importing Design:



Design Window:

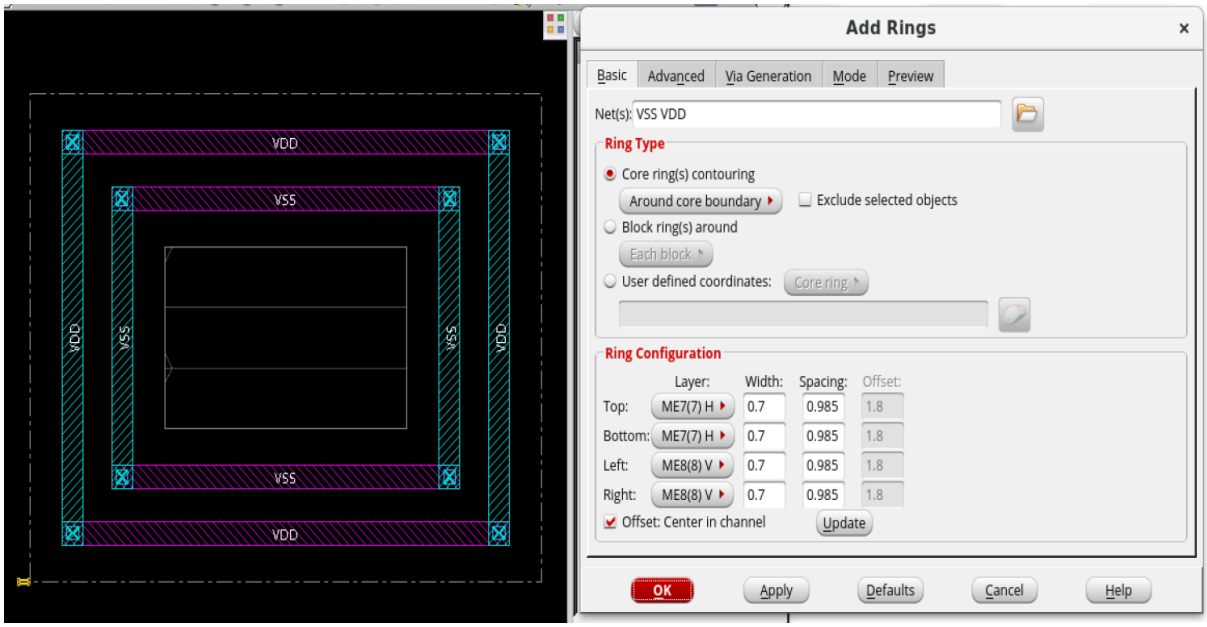


Floorplanning the design:

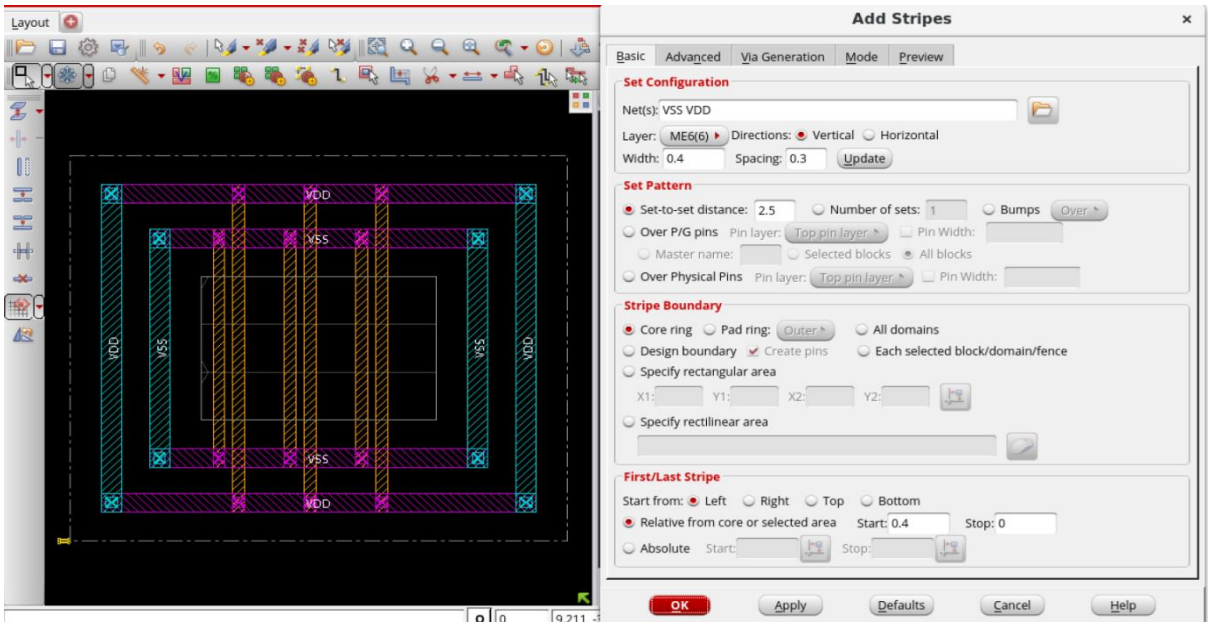


POWER PLANNING:

Adding Rings:

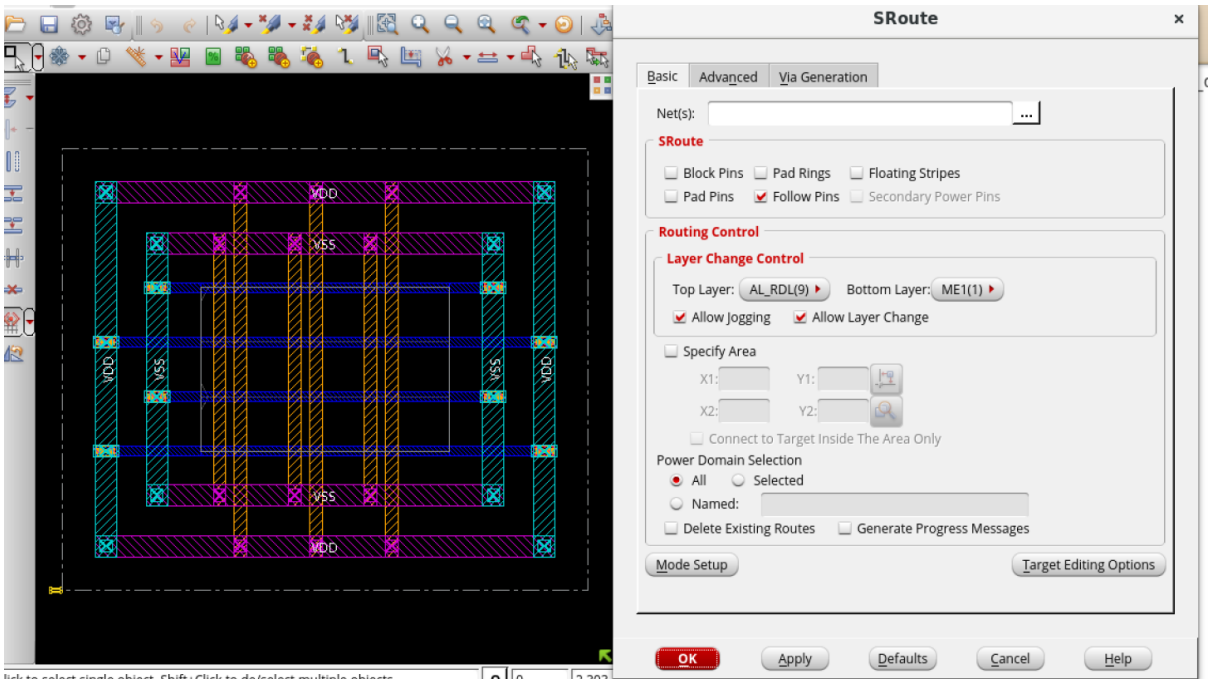


Adding Stripes:

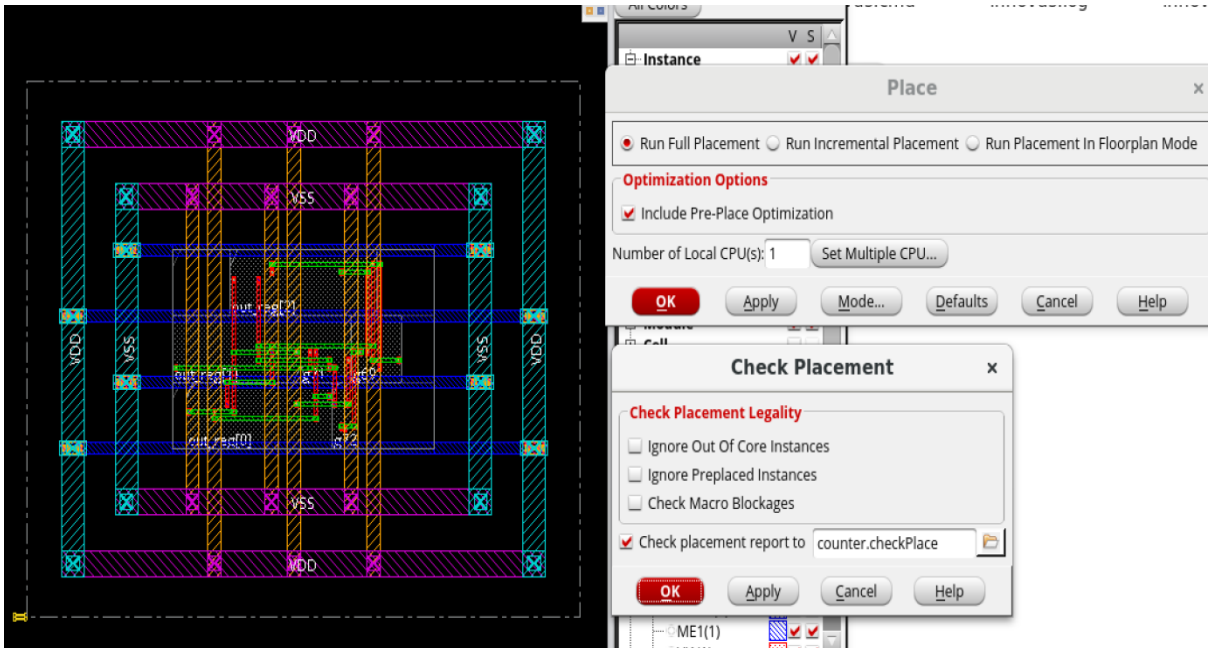


Creating power rails with special route:

```
globalNetConnect VDD -type pgpin -pin VDD -instanceBaseName *
globalNetConnect VSS -type pgpin -pin VSS -instanceBaseName *
```



Placing standard cell and placement check:



Pre-CTS (Timing Analysis):

Set-up time:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  9.267  |  9.267  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    6    |    6    |    0    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+-------------------+
|                |              Real             |       Total       |
|    DRVs        +------------------+------------+-------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)   |
+----------------+------------------+------------+-------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)        |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)        |
|   max_fanout   |      0 (0)       |     0      |      0 (0)        |
|   max_length   |      0 (0)       |     0      |      0 (0)        |
+----------------+------------------+------------+-------------------+

Density: 69.919%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.39 sec
Total Real time: 0.0 sec
Total Memory Usage: 2017.617188 Mbytes
innovus 3>
```

Open ▾ | counter_preCTS.slk — ~/Physical/Labassignment/counterpd/timingReports | Save | ≡ | ×

```
# Format: clock  timeReq  slackR/slackF  setupR/setupF  instName/pinName   # cycle(s)
clk(R)->clk(R)  9.844    9.267/*        0.156/*         out_reg[2]/D    1
clk(R)->clk(R)  9.791    9.300/*        0.209/*         out_reg[1]/D    1
clk(R)->clk(R)  9.788    9.329/*        0.212/*         out_reg[1]/RB    1
clk(R)->clk(R)  9.849    9.390/*        0.151/*         out_reg[2]/RB    1
clk(R)->clk(R)  9.855    9.396/*        0.145/*         out_reg[0]/D    1
clk(R)->clk(R)  9.868    9.438/*        0.132/*         out_reg[0]/RB    1
```

Hold time:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.099  |  0.099  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    6    |    6    |    0    |
+--------------------+---------+---------+---------+

Density: 69.919%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.83 sec
Total Real time: 1.0 sec
Total Memory Usage: 1992.414062 Mbytes
innovus 3>
```

Open | counter_preCTS_hold.slk — ~/Physical/Labassignment/counterpd/timingReports | Save

```
# Format: clock  timeReq  slackR/slackF  holdR/holdF  instName/pinName   # cycle(s)
clk(R)->clk(R)  0.027    */0.099        */-0.027       out_reg[0]/RB    1
clk(R)->clk(R)  0.028    */0.101        */-0.028       out_reg[1]/D     1
clk(R)->clk(R)  0.025    */0.106        */-0.025       out_reg[2]/D     1
clk(R)->clk(R)  0.025    */0.107        */-0.025       out_reg[1]/RB    1
clk(R)->clk(R)  0.024    */0.109        */-0.024       out_reg[2]/RB    1
clk(R)->clk(R)  0.024    */0.109        */-0.024       out_reg[0]/D     1
```

Clock Tree synthesis and Nano-routing:

Commands used:

create_ccopt_clock_tree_spec

ccopt_design

Post-CTS (Timing Report)

Setup time:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  9.284  |  9.284  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    6    |    6    |    0    |
+--------------------+---------+---------+---------+

+----------------+-----------------------------------+------------------+
|                |               Real                |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  | Worst Vio      |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |   0.000        |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000        |      0 (0)       |
|   max_fanout   |      0 (0)       |     0          |      0 (0)       |
|   max_length   |      0 (0)       |     0          |      0 (0)       |
+----------------+------------------+----------------+------------------+

Density: 69.919%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.68 sec
Total Real time: 1.0 sec
Total Memory Usage: 2060.84375 Mbytes
innovus 5>
```

Open | counter_postCTS.slk — ~/Physical/Labassignment/counterpd/timingReports | Save

```
# Format: clock  timeReq  slackR/slackF  setupR/setupF  instName/pinName   # cycle(s)
clk(R)->clk(R)  9.814    9.284/*         0.186/*         out_reg[2]/D    1
clk(R)->clk(R)  9.758    9.308/*         0.242/*         out_reg[1]/D    1
clk(R)->clk(R)  9.754    9.337/*         0.246/*         out_reg[1]/RB    1
clk(R)->clk(R)  9.817    9.400/*         0.183/*         out_reg[2]/RB    1
clk(R)->clk(R)  9.823    9.406/*         0.177/*         out_reg[0]/D    1
clk(R)->clk(R)  9.835    9.447/*         0.165/*         out_reg[0]/RB    1
```

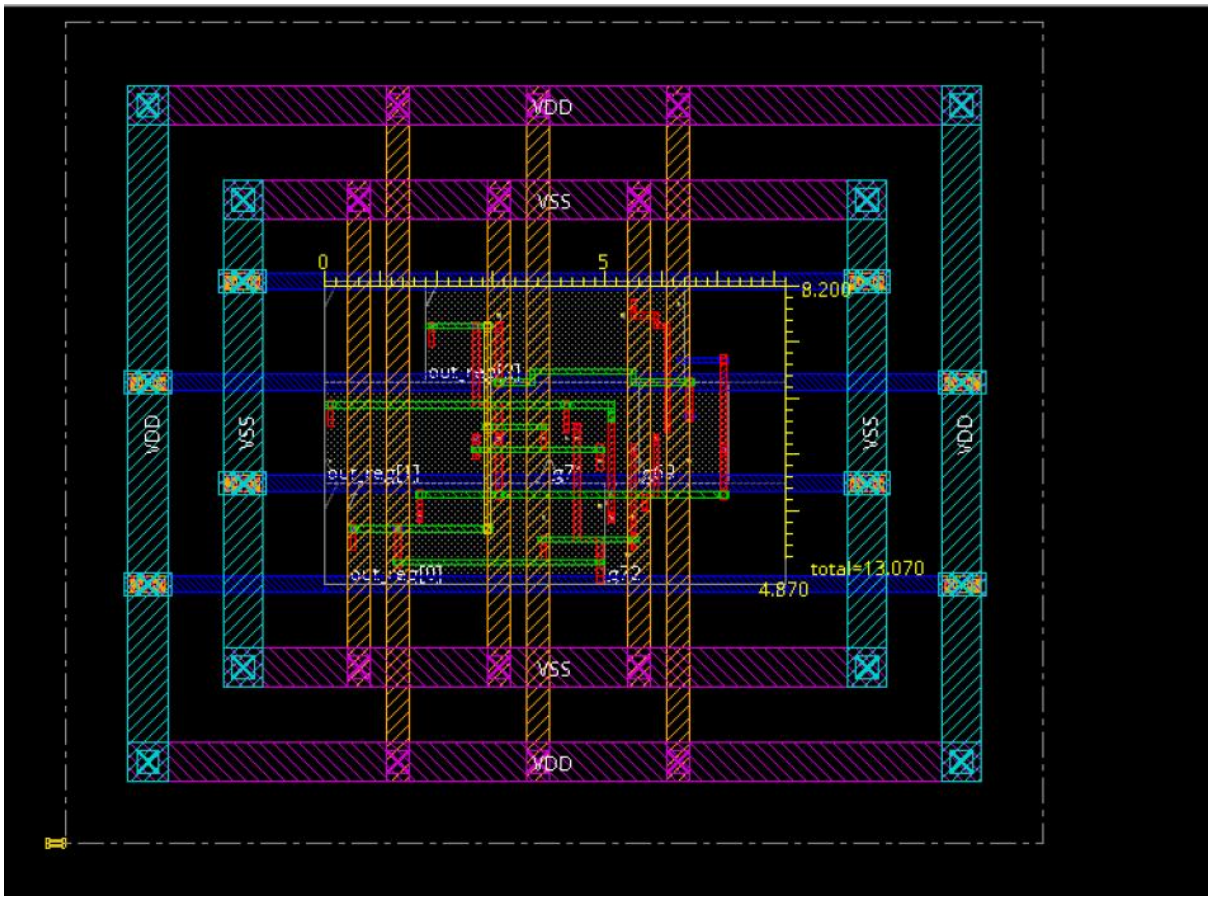
Hold time:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.096  |  0.096  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    6    |    6    |    0    |
+--------------------+---------+---------+---------+

Density: 69.919%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.98 sec
Total Real time: 1.0 sec
Total Memory Usage: 2042.695312 Mbytes
innovus 5>
```

Open | counter_postCTS_hold.slk ~/Physical/Labassignment/counterpd/timingReports | Save

```
# Format: clock  timeReq  slackR/slackF  holdR/holdF  instName/pinName   # cycle(s)
clk(R)->clk(R)  0.003    */0.096        */-0.003       out_reg[0]/RB    1
clk(R)->clk(R)  0.004    */0.098        */-0.004       out_reg[1]/D    1
clk(R)->clk(R)  0.002    */0.102        */-0.002       out_reg[2]/D    1
clk(R)->clk(R)  0.002    */0.104        */-0.002       out_reg[1]/RB    1
clk(R)->clk(R)  0.000    */0.105        */-0.000       out_reg[2]/RB    1
clk(R)->clk(R)  -0.000   */0.106        */0.000        out_reg[0]/D    1
```

Final Layout Generated:



Physical Verification:

DRC Check:

```
*** Starting Verify DRC (MEM: 2042.7) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 17.400 14.600} 1 of 1
 VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

Geometry Check:

```
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 2880
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 1.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.4  MEM: 106.6M)

innovus 5>
```

Connectivity Check:

```
VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Sun Oct 17 10:26:40 2021

Design Name: counter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (17.4000, 14.6000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sun Oct 17 10:26:40 2021
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)

innovus 5> 
```