INDIAN INSTITUTE OF TECHNOLOGY, DELHI

IEC LABORATORY-II

ELP832

ASSIGNMENT 1

PHYSICAL DESIGN FLOW OF ASYNCHRONOUS FIFO

(GENUS TOOL)

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PROBLEM STATEMENT:

Part 1:

Design Asynchronous FIFO

Read this paper. Then do PD(Physical Design) flow. Assume any clock frequency like (10MHz or 20MHz).

Task to be done in GENUS

- create clock definition
- generated clock definition
- Virtual clock
- input delay
- output delay
- max delay
- min delay
- max transition
- max capacitance
- max fanout
- clock latency
- clock uncertainty
- Multicycle Path
- False Path
- Half Cycle Path
- disable timing arcs
- case analysis

Results (Part 1)

- All the applicable commands were written in sdc (Synopsys Design Constraint) file.
- Following commands are not required in the sdc file of the asynchronous Fifo design:
  - Generated clock definition
  - Virtual clock
  - Max fanout
  - Half Cycle path
  - Disable timing arcs
  - Case analysis
- Remaining all are the applicable commands for our design.
- All commands of sdc files are successfully implemented in genus tool.

PART 2:

Sanity checks after performing above task

- Multidriven nets
- Floating pins
- Undriven input ports
- Unloaded outputs
- Unconstrained pins
- Pin mismatch counts between an instance and its reference
- Tristate buses with non-tristate drivers
- Wire loops across hierarchies
- If any unconstrained paths exist in the design then PNR tool will not optimize that path, so these checks are used to report unconstrained paths
- Checks whether the clock is reaching to all the clock pin of the flip-flop.
- Check if multiple clock are driving same registers
- Check unconstrained endpoints
- Port missing input/output delay.
- Port missing slew/load constraints.

Results (Part 2):

These sanity checks are the design and timing checks that are performed in the genus tool using commands:

- Check_design
- Check_timing

There were no design and timing errors found.

Path of the directory:

./een212024/Physical/Labassignment/fifo

- Sdc file and netlist files are being generated in the genus tools.
- .sdc, .tcl, generated.sdc, netlist.v, .log, .cmd , .sdef all files are uploaded separately in the submitted folder.
- Some screenshots have been attached in the report.

```
  Done Checking the design.
Statistics for commands executed by read_sdc:
 "all_outputs"              - successful      1 , failed      0 (runtime  0.00)
 "create_clock"             - successful      2 , failed      0 (runtime  0.00)
 "current_design"           - successful      1 , failed      0 (runtime  0.00)
 "get_clocks"               - successful     20 , failed      0 (runtime  0.00)
 "get_ports"                - successful      7 , failed      0 (runtime  0.00)
 "set_clock_latency"        - successful      2 , failed      0 (runtime  0.00)
 "set_clock_uncertainty"    - successful      1 , failed      0 (runtime  0.00)
 "set_false_path"           - successful      2 , failed      0 (runtime  0.00)
 "set_input_delay"          - successful      2 , failed      0 (runtime  0.00)
 "set_max_capacitance"      - successful      1 , failed      0 (runtime  0.00)
 "set_max_delay"            - successful      1 , failed      0 (runtime  0.00)
 "set_max_transition"       - successful      1 , failed      0 (runtime  0.00)
 "set_min_delay"            - successful      1 , failed      0 (runtime  0.00)
 "set_multicycle_path"      - successful      2 , failed      0 (runtime  0.00)
 "set_output_delay"         - successful      2 , failed      0 (runtime  0.00)
 "set_units"                - successful      2 , failed      0 (runtime  0.00)
 "set_wire_load_mode"       - successful      1 , failed      0 (runtime  0.00)
Total runtime 0.0
```

Fig.1 SDC commands successfully implemented in the genus tool

```
Lint summary
 Unconnected/logic driven clocks                                  0
 Sequential data pins driven by a clock signal                    0
 Sequential clock pins without clock waveform                     0
 Sequential clock pins with multiple clock waveforms              0
 Generated clocks without clock waveform                          0
 Generated clocks with incompatible options                       0
 Generated clocks with multi-master clock                         0
 Paths constrained with different clocks                          0
 Loop-breaking cells for combinational feedback                   0
 Nets with multiple drivers                                       0
 Timing exceptions with no effect                                 3
 Suspicious multi_cycle exceptions                                0
 Pins/ports with conflicting case constants                       0
 Inputs without clocked external delays                           0
 Outputs without clocked external delays                          0
 Inputs without external driver/transition                       12
 Outputs without external load                                   10
 Exceptions with invalid timing start-/endpoints                  0

                                                  Total:         25
```

Fig.2 Sanity Checks for the timing

```
        Check Design Report (c)
        -----------------------
 Summary
 -------

             Name                          Total
-------------------------------------------------
Unresolved References                          0
Empty Modules                                  0
Unloaded Port(s)                               0
Unloaded Sequential Pin(s)                     0
Unloaded Combinational Pin(s)                  0
Assigns                                        0
Undriven Port(s)                               0
Undriven Leaf Pin(s)                           0
Undriven hierarchical pin(s)                   0
Multidriven Port(s)                            0
Multidriven Leaf Pin(s)                        0
Multidriven hierarchical Pin(s)                0
Multidriven unloaded net(s)                    0
Constant Port(s)                               0
Constant Leaf Pin(s)                           0
Constant hierarchical Pin(s)                   0
Preserved leaf instance(s)                     0
Preserved hierarchical instance(s)             0
Feedthrough Modules(s)                         0
Libcells with no LEF cell                      0
Physical (LEF) cells with no libcell           0
Subdesigns with long module name               0
Physical only instance(s)                      0
Logical only instance(s)                     339


  Done Checking the design.
```

Fig.3 Sanity Checks for the design

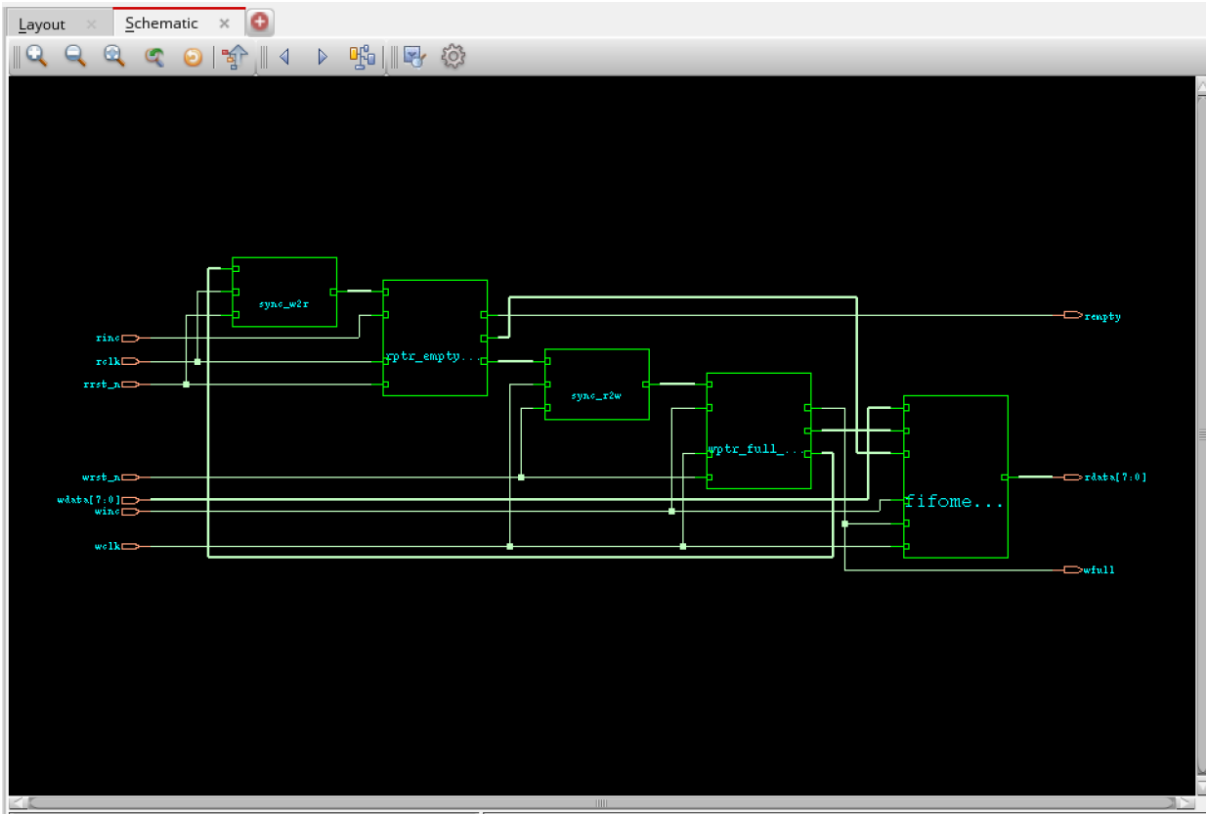

Fig.4 Generated schematic of Asynchronous FIFO

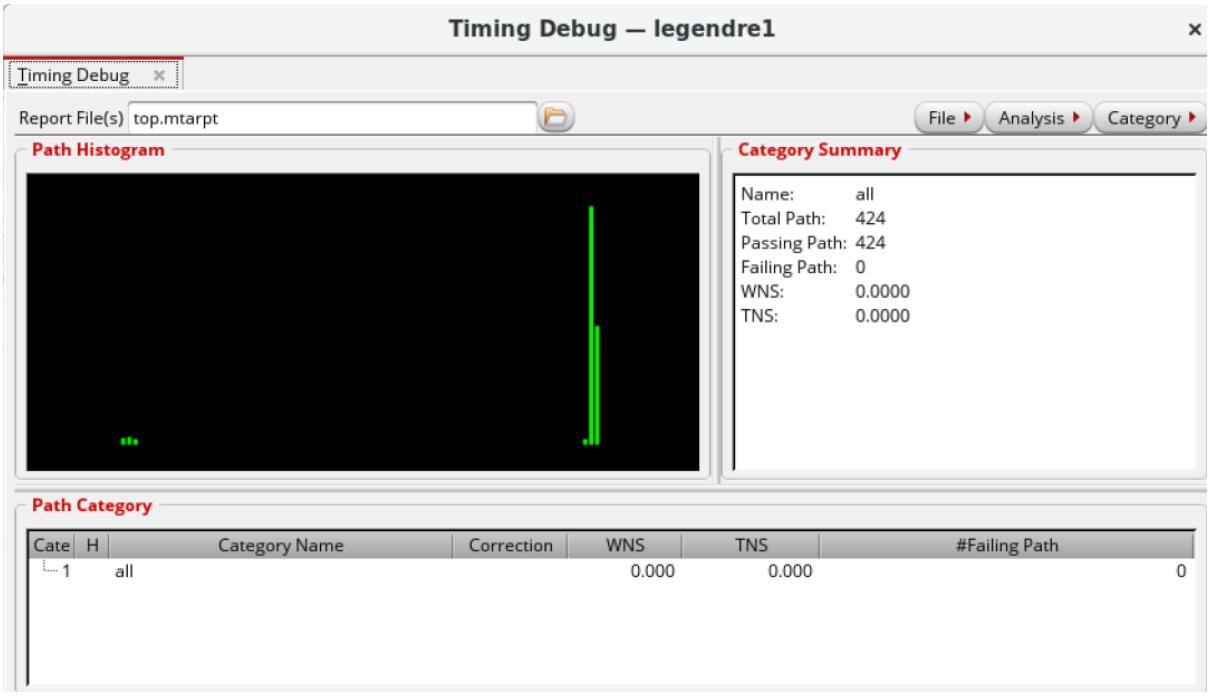

Fig.5 Debug Timing figure with zero failing paths