



United International University

Department of Computer Science and Engineering

EEE 2123: Electronics

Mid-Term Exam: Summer 2022 Time: 1 hour 45 minutes Marks: 30

There are four questions here. Answer all of them

1. Assume that a diode has a turn-on voltage of 2.1 V and a breakdown voltage of 4 V . The reverse saturation current and operating temperature of the diode are 10 nA and 25°C respectively.



Figure 1: Figure for Q-1

- (a) Fill up the following table based on the given information: [3]

Case	V_a	V_b	Biasing type	ON/OFF/Breakdown
1	10	5		
2	5	10		
3	-5	2		
4	-3	-5		

- (b) For Case 1, calculate the diode current with appropriate unit. [1]
- (c) What will be the effect on the turn on voltage and the reverse saturation current if the temperature is increased to 75°C ? [2]

2. Consider the following rectifier circuit where $I_{0,avg} = 5\text{ mA}$.

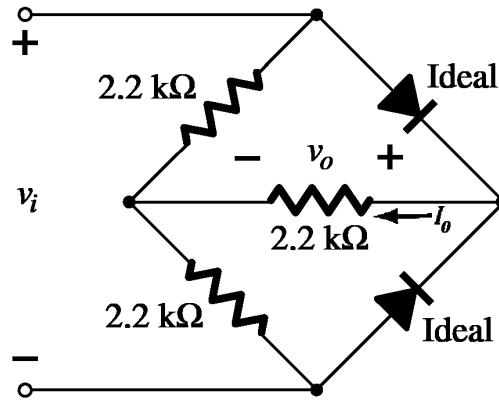


Figure 2: Circuit diagram for Q-2

- (a) Express v_0 in terms of v_i . [2]
- (b) Find the maximum value and average values of v_0 . Hints: Ohms law relates v_0 and i_0 . [2]
- (c) Sketch v_0 and v_i in the same plot mentioning peak values. [1]
- (d) Calculate PIV of any diode given in the above network. [1]

3. (a) Design the clipper and clamper circuit to produce the following output voltage (V_o) according to the given input voltage (V_i). Assume the diodes to be ideal. Hints: Try to achieve a signal with 3 V to -7 V peak values at the end of the clipper network. [5]

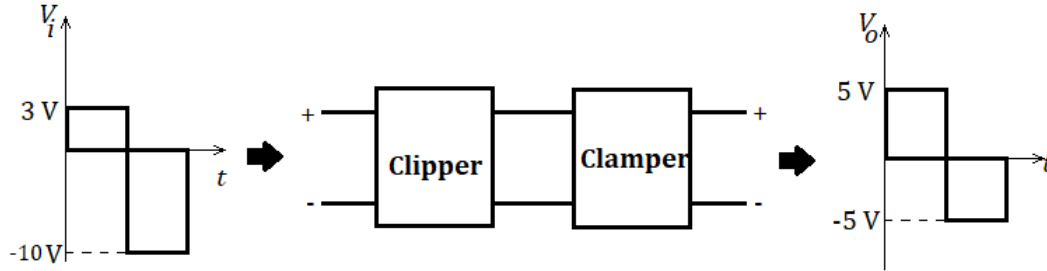


Figure 3: Circuit diagram for Q-3(a)

- (b) Sketch the output voltage of the following circuit assuming *GaAs* diode and properly mention the output voltage levels. The r.m.s (root mean square) value of the input voltage is 10 V. [4]

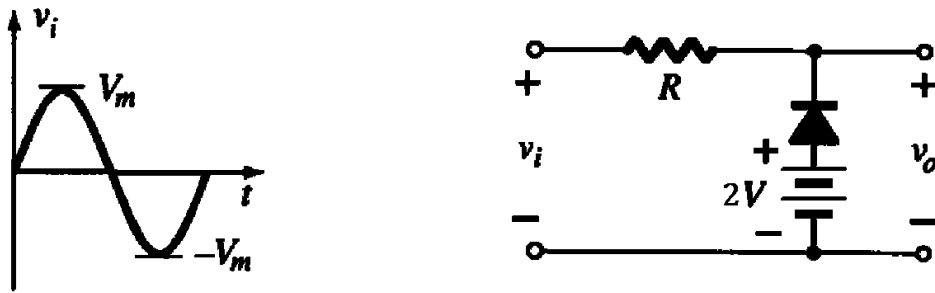


Figure 4: Circuit diagram for Q-3(b)

4. (a) Solve the following circuit to find the values of I_1, I_2, I_3, I_4, I_0 and V_0 . [6]

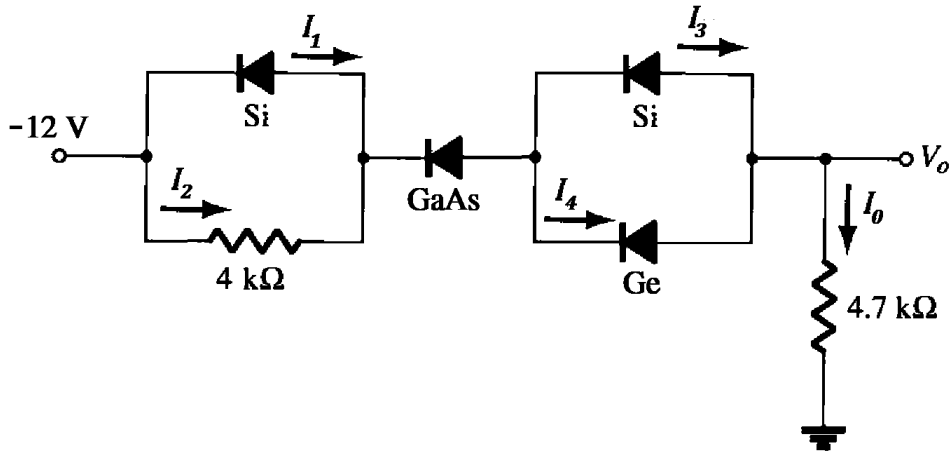


Figure 5: Circuit diagram for Q-4(a)

Question-4 continued....

(b) Find the values of I_1 , I_2 , I_0 and V_0 in the following network.

[3]

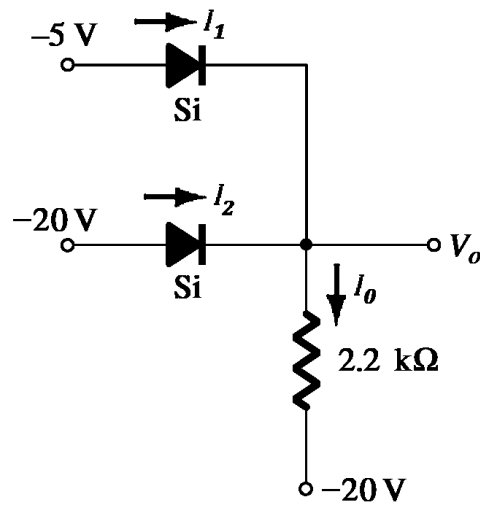


Figure 6: Circuit diagram for Q-4(b)