United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Final Exam :: Trimester: Fall 2022

Course Code: EEE 2123, Course Title: Electronics

Total Marks: 40 Duration: **2 hours**

There are FIVE questions. Answer all the questions. Marks are indicated in the right margin.

1. a) A student at UIU found a circuit in the Electronics lab which has a very interesting characteristic. Whenever he applied any DC voltages to the input of this circuit, he found zero voltage at the output. Also, when he applied any non-DC voltages to the input, he found non zero voltage at the output. He did not understand why this was happening and went to you. Now, you have to explain him by designing such circuit. **[2]**

   b) Mr. Anik wants to calculate the average value of four different inputs. But he couldn't implement such calculation system in circuit as he was busy over his office work at UIU. Now, design such circuit to help Mr. Anik. **[3]**

2. a) Explain why the current in MOSFET becomes constant at the saturation region. **[2]**

   b) A MOSFET has the following gate voltage and source voltage, $V_G = 0, V_S = -1V$. If the threshold voltage of this MOSFET is 2V, then the source current of this MOSFET was found zero. Explain why the source current of this MOSFET is zero? Also, determine the maximum threshold voltage of this MOSFET for which the source current becomes non-zero for the same gate and source voltage. **[2+1]**

3. a) A MOSFET is connected in the following configuration shown in **Figure 1.**

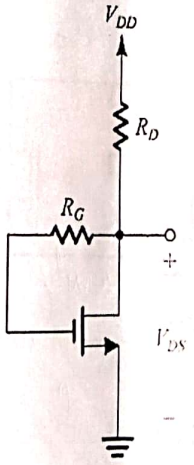

Figure 1

If $V_{DD} = 5V, R_G = 100M\Omega, R_D = 2K\Omega, V_{DS} = 2.5V, k_n'\left(\frac{W}{L}\right) = 1mA/V^2$, then determine the operating region of this MOSFET and drain current, I_D. **[6]**

b) A MOSFET is connected in the following configuration shown in **Figure 2.**

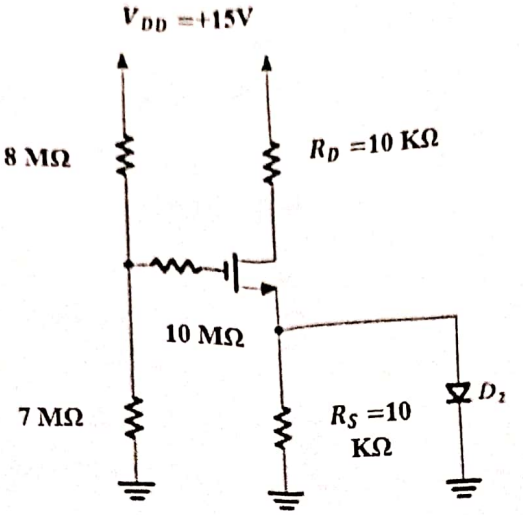

Figure 2.

The MOSFET has the following characteristics, $k_n'\left(\frac{W}{L}\right) = \frac{2.5mA}{V^2}, V_t = 0.75V$. Now, if the diode connected in the above circuit is a silicon diode, then determine the Gate current, Drain current, source current, I_{R_S} and I_{D_2} of the MOSFET. [7]

4. (a) From the pull-up network from **Figure 3.**, design the pull-down (NMOS) network to complete the CMOS implementation. Also determine the logic function from this circuit. **[2+1]**

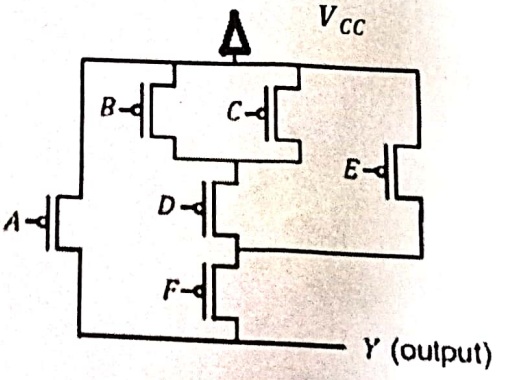

Figure 3.

(b) Implement the following logic function in single stage CMOS technology. **[3]**

$$f = ((a+b)\bar{c} + de)\bar{f}$$

5. (a) For the circuit in **Figure 4.**, it is required to determine the value of the voltage that results in the transistor operating at the edge of saturation. The transistor β is specified to be 50. **[5]**

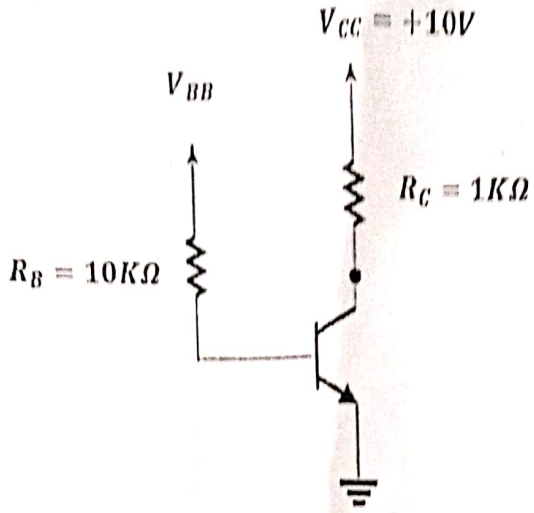

Figure 4.

(b) From the circuit in **Figure 5.**, determine the values of $V_C, V_E, V_B, I_C, I_B, and\ I_E$. Assume that $R_B = 10K\Omega$. **[6]**

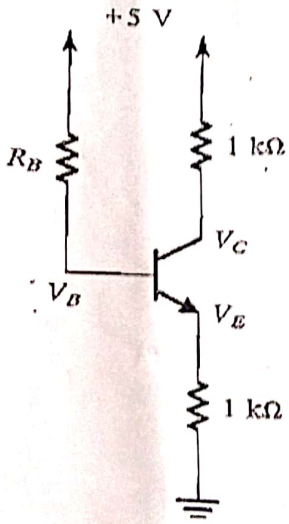

Figure 5.