



**United International University
Department of Computer Science and Engineering**

EEE 2123: Electronics

Final-Exam: Spring 2022 Time: 2 hours Marks: 40

There are five questions here. Answer all of them

1. (a) Why is MOSFET called a voltage-controlled device? [3]
 (b) What will be the effect on an n-channel MOSFET if the p-substrate becomes highly doped? [2]
2. (a) For the circuit shown below, determine the values of I_D and V_{DS} . Also, find the operating region of the transistor. For the NMOS, $V_{tn} = 1 \text{ V}$ and $k'_n(W/L) = 0.5 \text{ mA/V}^2$. [5]

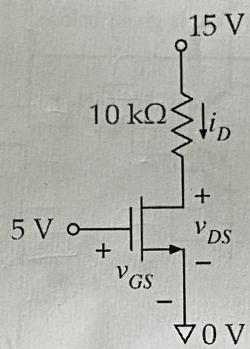


Figure 1: Circuit diagram for Q-2(a)

- (b) It is required to design the following circuit to establish a dc drain current of 0.5 mA. The transistor is specified to have $V_t = 1 \text{ V}$, $W/L=150/40$ and $k'_n=1 \text{ mA/V}^2$. For simplicity, consider that both R_D and R_S are of the same value. [5]

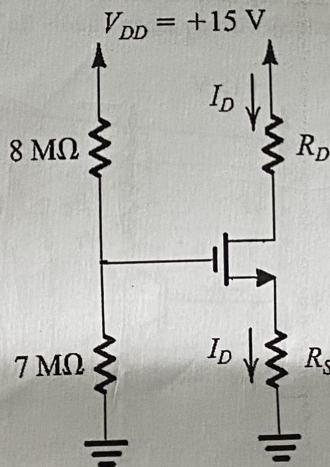


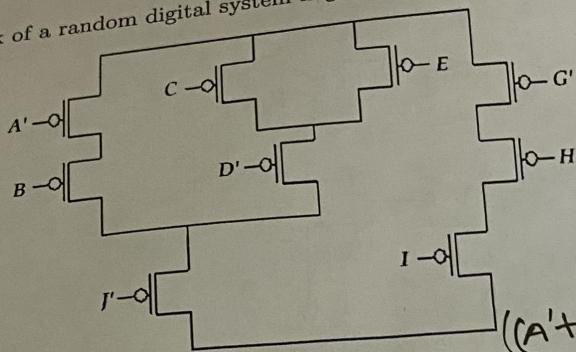
Figure 2: Circuit diagram for Q-2(b)

Question-2 continued....

- (c) Consider the following cases for operating an NMOS transistor with threshold voltage of 1 V. Now complete the following table. Here, all values are given in volt unit. [5]

Serial No.	V_S	V_G	V_D	V_{GS}	V_{OV}	V_{DS}	Operating Region
1	1.5	2.5	4	1.0	?	?	?
2	0	?	?	?	1.0	?	edge of saturation
3	2.0	3.0	2.0	?	?	?	?
4	-2.0	0	2.0	?	?	?	?

3. The PMOS network of a random digital system is given below:



$$(A'+B)(C'E+D') + G + H + I$$

Figure 3: PMOS network for Q-3 \Rightarrow

Draw the corresponding NMOS network using the concept of CMOS technology and mention the expression of the output function f in complementary form. [4]

4. (a) Find the values of I' , I'' , I_B , V_E and R_E so that the BJT in the following figure operates in the saturation mode (deep in saturation) with $\beta_{forced}=1.5$. [5]

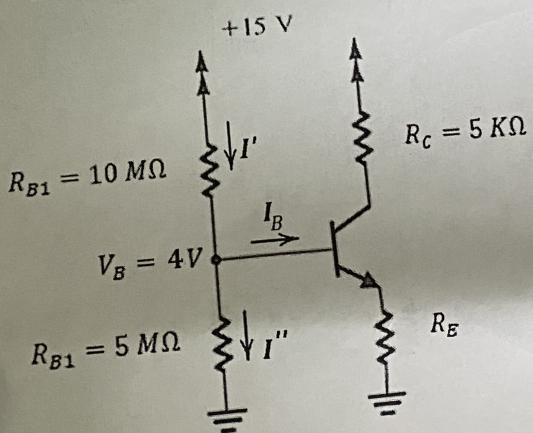


Figure 4: Circuit diagram for Q-4(a)

Question-4 continued....

(b) Find all node voltages and mention the values of a and b

- (b) Find all node voltages and branch currents in the following circuit assuming $V_{CE}=2$ V. Also, [5]
mention the values of α and β .

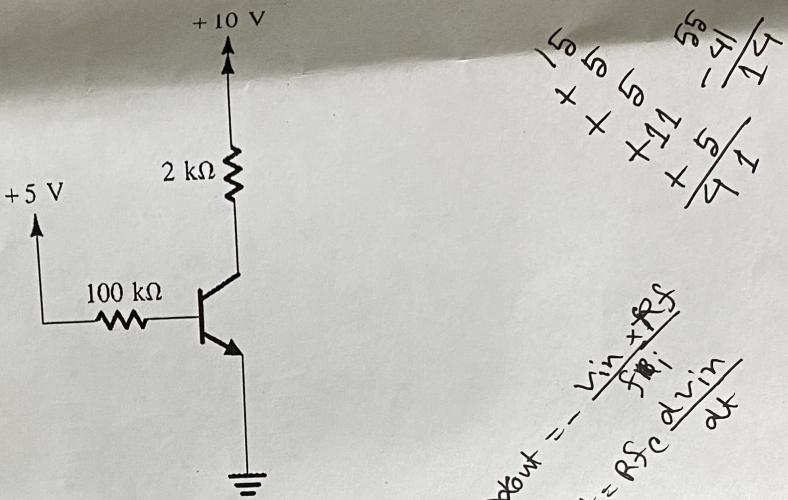


Figure 5: Circuit diagram for Q-4(b)

5. Design an amplifier circuit that can generate the following outputs:

(a) $v_0 = -5 \frac{dv_i}{dt} + 10v_i$
(b) $v_0 = -15v_1 - 20v_2$ (here, v_1 and v_2 are two different inputs)

Clearly mention the values of all circuit parameters. Assume that the feedback resistor is $10 \text{ k}\Omega$ in [6]
all cases.

