United International University
Department of Computer Science and Engineering

EEE 2123: Electronics

Final-Exam: Summer 2022 Time: 2 hours Marks: 40

There are five questions here. Answer all of them

1. (a) Implement the following logic function in single stage and draw the corresponding circuit diagram: [4]

$$f = (\overline{a}b\overline{c} + d)e + g\overline{h}$$

(b) Draw the PMOS network corresponds to the following circuit. Also, find out the corresponding logic expression. [3]

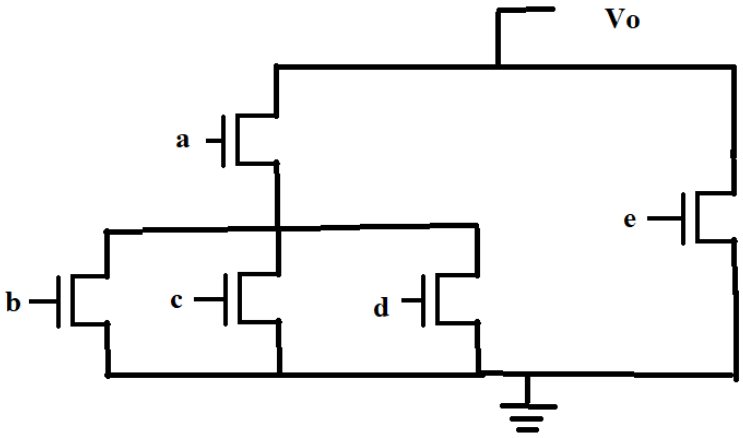

Figure 1: NMOS network for Q-1(b)

2. (a) The MOSFET in the following figure has $V_t = 0.5V$, $k'_n = 400\mu A/V^2$. Find the required values of W/L and R when $v_I = V_{DD} = +1.8V$, $r_{DS} = 50\Omega$, and $V_o = 50mV$. [6]

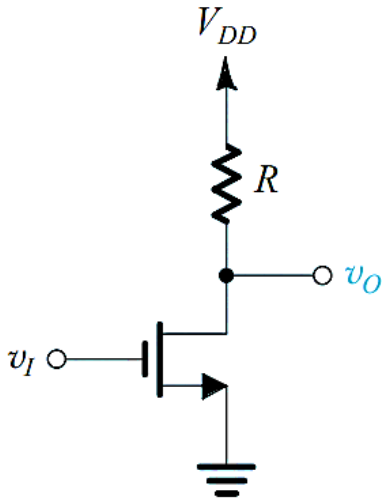

Figure 2: Circuit diagram for Q-2(a)

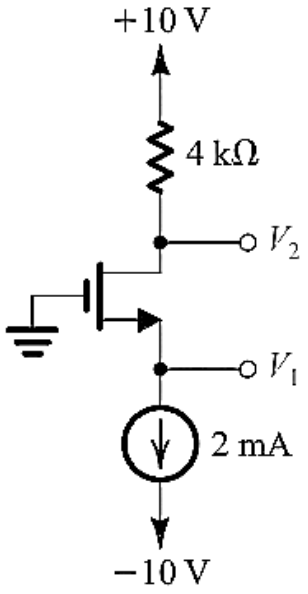

Figure 3: Circuit diagram for Q-2(b)

(b) Find out the operating region of the MOSFET shown in Figure 3. [5]

3. (a) Find all node voltages and branch currents in the following circuit assuming operation at the edge of saturation. Also, mention the values of α and β. [6]

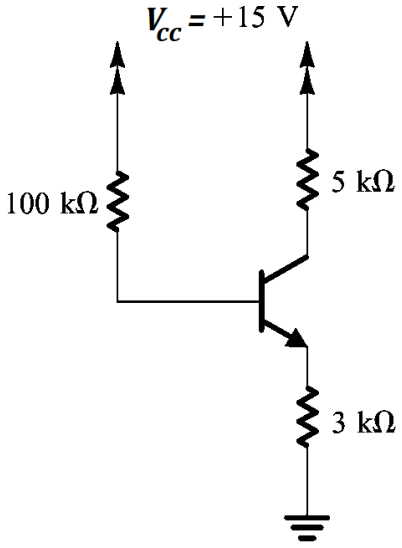

Figure 4: Circuit diagram for Q-3(a)

(b) A bipolar device whose emitter terminal is connected to a -5 V supply is operating at active region with $\beta = 100$. A voltage of 0.8 V is obtained across base-emitter junction for 3 mA emitter current. What should be voltage at base terminal if the current through collector becomes 1.5mA. [4]

4. (a) Draw the $i \sim v$ curve of an n-channel MOSFET whose $V_G = V_S = -10V$. [3]

   (b) Why is BJT called a bipolar device? [2]

5. Design an op-amp circuit that can generate the following outputs:

   (a) $v_0 = -5\dfrac{dv_i}{dt} + 10v_i$ using difference amplifier [3]

   (b) $v_0 = -15v_i + 10\displaystyle\int v_i dt - \frac{1}{2}\frac{dv_i}{dt}$ [4]

   Clearly mention the values of all circuit parameters. Assume the feedback resistor in all cases to be 1 $k\Omega$.