**RANJITH MADDI**

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# Professional experience

**3+ Years of experience in,**

* Digital Design, Micro-Architecture, RTL coding/Integration, Simulation, Timing closures FPGA design.
* Experience of working on many industry standard protocols and interfaces like SPI, I2C, knowledge on UART, Pcie.
* Complete design cycle for FPGA based systems including RTL coding/Integration, Verification and Synthesis and STA.
* Worked on Xilinx FPGAs, having basic knowledge of device architectures.
* Having knowledge on CDC design technique for FPGA design.
* Expertise in developing Designs with **Verilog** andgood in **VHDL** programming.
* Have sound knowledge in FPGA/ASIC Design Flow.
* Worked with various tools – **Xilinx ISE and VIVADO**, ModelSim and QuestaSim.
* Worked on **Xilinx Chip scope analyzer and ILA analyzer.**
* Worked on code coverage.
* Basic knowledge on TCL.
* Hands on experience in **Tanner toolsV.13.O** for Physical design.
* Sportive team player, motivates the team members to excellence, understands the value and importance of delegating work and responsibilities.
* Strong communication, analytical, debugging and presentation skills.

# Experience

* Working as Engineer at **eInfochips LTD**, Ahmedabad, from 14th August 2017 to till date.
* Worked as RTL designer at **Trylogic soft solutions**, Hyderabad, from 19th December 2014 to 30thth July 2017.

# Educational Qualification

* **M.Tech** in**VLSI DESIGN** from VAAGDEVI COLLEGE OF ENGINEERING, WARANGAL, JNTUH, TELANGANA in 2015 and aggregated with **75%.**
* **B.Tech** in **Electronics and Communication** fromTCEK, KARIMNAGAR, JNTUH, TELANGANA in 2013 and aggregated with **75%**.

# Technical Skills

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| Hardware Description Language | Verilog ,VHDL |
| Simulation Tools | ModelSim, QuestaSim |
| Synthesis & Implementation | Xilinx ISE, PlanAhead and Xilinx-Vivado |
| FPGA debug | Xilinx Chip Scope Analyzer, ILA debug Analyzer |
| Protocol Knowledge | I2C,SPI,UART |
| Hardware implementation | Xilinx Kintex 7, Spartan 6, Nexys video Aritix, BASYS 3(Spartan 3E) |
| Operating systems | Windows, LINUX |

# Project details

# Project #1

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| Project | Oscilloscope demo board FPGA design |
| Technology | Verilog, Xilinx Vivado, Artix 7 nexys video |
| Role | Team Member |
| Team Size | 3 |
| **Duration** | 3 Months |
| Synopsis  This Project represents the transmission of the prbs high speed data signals with distortions. In this project, generating the high speed signals with different high frequencies (625Mbps, 1.25Gbps, 2.5Gbps, 5Gbps) and adding the different types of distortions to the high speed signals, displaying those signals with oscilloscope.  Responsibilities involved   * Understand the PRBS high speed signal generation with Transceivers (GTP). * Micro-architecture design and RTL of Frame decoding, i2c slave, binary to bcd conversion blocks and GTP transmitter configuration, XDC file creation, hardware validation with demo board. * Debug and bug fix issues which were found during the hardware validation with ILA. * Run the synthesis with Xilinx vivado and simulation in questasim. | |
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# Project #2

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| Project | PRBS data transmission through the Transceiver. |
| Technology | Xilinx Vivado, Verilog |
| Role | Team Member |
| Team Size | 2 |
| Duration | 1 Month |
| Synopsis  The Functionality of design is to transmit PRBS’s output through transceiver with the speed of 1Gbps.The design include PRBS7, PRBS9, PRBS11 and PRBS15. Selection of PRBS done through external configuration via SPI.    Responsibilities involved   * Understand the PRBS generation, SPI slave. * Micro-architecture design and RTL of Frame decoding, RAM, PRBS 7, PRBS 11, SPI slave and GTP transmitter configuration. * Integrated all blocks and IP. * Run the synthesis and created the test bench for simulation for the top design. | |
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# Project #3

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| Project | Video Test Pattern Generator |
| Technology | Xilinx Vivado, Verilog, Video, Kintex 7 |
| Role | Team Member |
| Team Size | 2 |
| Duration | 2 |
| Synopsis  This project involves to display with different types of video test pattern generators, in this we have generated eight different video test patterns (horizontal lines, vertical lines, red, green, blue etc...) . Replaced the customized video test pattern generator in the place of existing test pattern generator in the example design.  Responsibilities involved   * Understand digital image specifications, test pattern generations. * Micro architecture and RTL for four test patterns (horizontal lines, cross lines on white display, display red and green colures). * Understand the existing example design and internal blocks. * Integration of different VTPG related ip’s. * Hardware validation. | |

# Project #4

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| Project | **Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic** |
| Technology | Verilog Xilinx ISE 14.4, Modelsim, Xilinx power estimator, Spartan 3 |
| Role | Team Member |
| Team Size | 1 |
| Duration | 3 Months |
| Synopsis  Hardware acceleration has been proved an extremely promising implementation strategy for the digital signal processing (DSP) domain. We differentiate from previous works on flexible accelerators by enabling computations to be aggressively performed with carry-save (CS) formatted data.  Responsibilities involved   * Understand the DSP blocks and FCU. * Understand the different algorithm (DADDA, Wallace tree). * Micro architecture of top design block and RTL for top module all internal blocks like partial product generation and reduction, carry save arithmetic blocks. * Run the synthesis, compared the utilization report with existing block report and created Verilog test bench for simulation. * Created UCF file for hardware validation. * Debug the output signals with chip scope debugger to check the output. * Power analysis with the Xilinx power estimator. | |

# Project #5

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| Project | **News Paper Vending Machine controller** |
| Technology | Verilog , Xilinx ISE 14.4 and Modelsim |
| Role | Team Member |
| Team Size | 1 |
| Duration | 2 Months |
| Synopsis  NEWS Paper vending machines are used to dispense small different NEWS Papers when a coin is inserted. FPGA based vending machine give fast response and uses less power than the microcontroller based vending machine. This vending machine supports four products and two coins. The vending machine accepts coins as inputs in any sequence and delivers products when required amount is deposited and gives back the change if entered amount is greater than the price of product. It also supports cancel feature means a user can with draw the request any time and entered money will be returned back without any NEWS Paper.  Responsibilities involved   * Understand the Finite state machines. * Designed FSM for top level design and RTL for the top block. * Checked the synthesis report. * Designed a simple Verilog test bench for top block, checked for the simulation for all possible states. | |

# Project #6

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| Project | **Title: Implementation of I2C Master Bus Controller** |
| Technology | Verilog, Xilinx ISE, ModelSim |
| Role | Team Member |
| Team Size | 2 |
| Duration | 2 Months |
| Synopsis  This implements serial data communication using I2C (Inter-Integrated Circuit) master bus controller. The I2C master bus controller used to transmit the data from master to slave.  **Responsibilities involved**   * Understanding the protocol and data format. * Design and verification of i2c protocol. * Creating efficient FSM for the design of i2c Protocol. * Architect the design and described the functionality using Verilog HDL. * Verifying the protocol with single master single slave environment. | |

**Declaration:**

I hereby declare that the information furnished above is true to the best of my knowledge and belief.

Date:

Place: RANJITH MADDI