Name: - BRAHMBHATT YOGESH ARVINDBHAI
Phone: - **7041747984**
Email: - yogesh.barot444@gmail.com

Objective:

Intend to build a career with leading corporate of hi-tech environment with committed and dedicated people, which will help me to explore myself fully and realize potential. To secure an innovative position in the field of electrical and to make the optimum use of my strength and capabilities to get the best result.

Educational Qualifications:

Sr. No.	Degree/Certificate	Institution/Board	Marks obtained	Year
1	SSC	GSEB	76.77%	**2011**
2	HSC	GSHEB	52.66%	**2013**
3	BE-EE	GITS/GTU	7.08 CGPA	**2017**

Academic Projects:

Project Name: A New cascaded Multilevel five level Inverter Topology with reduced number of switches & sources.

Platform: Power Electronics and Embedded System

Duration: final year

Project Description: -

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. The voltage source inverters produce an output voltage or a current with levels either 0 or +ve or-ve V dc. They are known as two-level inverters. Multilevel inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages. Multilevel inverter has advantage like minimum harmonic distortion. Multi-level inverters are emerging as the new breed of power converter options for high power applications. They typically synthesize the stair –case voltage waveform (from several dc sources) which has reduced harmonic content.

For a multilevel inverter, switching angles at fundamental frequency are obtained by solving the selective harmonic elimination equations by using Fourier analysis in such a way that the fundamental voltage is obtained as desired and certain lower order harmonics are eliminated and higher order harmonics eliminated using high pass filter. As these equations are nonlinear transcendental in nature and solution of equation can be obtained by applying iterative numerical techniques

In this project mainly focused on the design and implementation of new topology in a single phase five level cascaded H-bridge multilevel inverter H_5 topology by using only a five switches and two DC power source. The main objective of this project is to increase number of levels with a low number of switches and sources at the output without adding any complexity to the power circuit. The main

merit of the new topology is to reduce the lower total harmonic distortion, lower electromagnetic interference generation and high output voltage. In this paper, firing angle of switches in manner single phase five level cascaded H-bridge multilevel inverter H_5 topology are calculated in such manner to reduce lower order harmonics by increasing level as well as using less number of switches. The single phase five level cascaded H-bridge multilevel inverter H_5 topology are implemented using IRF 840 mosfets and ATmega32 microcontroller.

Technical Skills

Microprocessor/controller	8085, Atmega 16/32 microcontroller
PCB Designing	Proteus,
Circuit Designing	Multisim, Proteus,
Microcontroller simulator	Keil, AVR Studio,
Mathematical Software	Matlab, Psim
Programming Languages	C language,Assembly language

- Power system planning and designing
- Testing and commissioning of electrical equipment
- Good in installing switchgear and protection
- All kind of domestic and commercial electrical equipment installation
- Control panel and PLC system wiring diagram solving
- All type of mechanical machine maintenance

Personal Profile:

- Gender : Male
- Date of Birth : 17 / 10 / 1993
- Address : 48, Rushikunj society Behind giriraj society , bayad.
- Languages Known : Gujarati, Hindi, English
- Hobbies : Travelling, Bike riding , Innovation
- Strength : Loyal to my work, Leadership, Never Give Up, Quick learner ability to work under pressure

Declaration:

I am sincere in all my endeavours and have a good co-ordination skill to work in a team. I hereby declare that the information furnished above is true to the best of my knowledge.

Yours faithfully,

YOGESH BRAHMBHATT