Dhirubhai Ambani
Institute of Information and Communication Technology

KHYATI NAGRANI

M.Tech, Information and Communication Technology specialized in VLSI and Embedded systems
8849267189,202111031@daiict.ac

EDUCATION

Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT)
CPI:8.08
Aug 2021 – Present Gandhinagar, Gujarat

BTech in Electronics and communication from Gujarat Technological University
CPI:7.99
Aug 2016 – May 2020 Gandhinagar, Gujarat

Kendriya Vidyalaya (SAC),XII (CBSE)
Percentage:83.6 %
2015 – 2016 Ahmedabad, Gujarat

Kendriya Vidyalaya (SAC),X (CBSE)
Percentage: 89.3%
2013 – 2014 Ahmedabad, Gujarat

SKILLS

Area(s) of Interest : Digital design (RTL to GDSII)

Programming Languages : Verilog,VHDL,C

Tools and Technologies :LTSpice,Keil MDK,Xilinx ISE,Quartus lite

POSITIONS OF RESPONSIBILITY

SPC Member
Active member of student placcement cell at DAIICT
Jan 2022 – Nov2022

SPC Member
Active member of student placcement cell at GEC Gn
Jan 2017 – Dec 2018

Head Volunteer
Workshop related to soft skills
Aug 2016

INTERESTS

- Story Writing
- Listening to Podcasts
- Reading about Mythology

PROJECTS

Neural Network Architectures for Integrated Circuits :
July 2022 - Present

- Thesis work that focuses on the architectural design and implementation of neural networks (NNs) for integrated circuit design. The architecture consists of the adder, multiplier, and rectified linear unit (ReLU) blocks. Three architectures (i) single-in single-out (SISO), (ii) multiple-in single-out (MISO), and (iii) multiple-in multiple-out (MIMO) are developed. In NNs, weight values are required, fed from a manually generated memory. The weight values were prepared by training the NNs model on software. Finally, the SISO, MISO, and MIMO neural-networks were taped out.
- **Guide:** Prof. Tapas Kumar Maiti

Digital Data Simulator and Data Formatter:
June 2019 - May 2020

- Industrial project done at ISRO. Digital data simulator is FPGA based programmable data pattern generator,which is able to generate different test data patterns. Data Formatter receives data from cameras and sends formatted data to Acquisition PC for storing and further analysing. During development and testing of Data Formatter, Data Simulator is used.
- **Guide:**K.J Shah and Soumen Garai (Sci/Eng at ISRO),Prof JK Bhavsar

ACHIEVEMENTS

- Received 2nd Rank In Mock parliament held at LD college of engineering