Open-Source Tools for FPGAs

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***Abstract*—The open-source FPGA ecosystem has taken a lot of significant steps and is now capable of offering some really cost-effective and flexible alternatives to proprietary FPGA development tools. Applications like Yosys, Nextpnr, Project IceStorm, and SymbiFlow make it very easy for developers, researchers, and hobbyists to experiment with FPGAs without the heavy costs and rigidity of proprietary solutions. Unfortunately, most open-source FPGA tools face lean support for VHDL and advanced timing optimization issues, among other drawbacks. Still, the improvement of these open-source tools remains community-driven. Supported by organizations like the FOSSi Foundation, these tools offer a collaborative platform that promotes innovation and accessibility in FPGA development. As advancements in language support, machine learning integration, and verification capabilities progress, open-source tools are becoming increasingly competitive with proprietary solutions, paving the way for an inclusive future in reconfigurable hardware.**

***Index Terms*—Open-source FPGA, Yosys, Nextpnr, Project IceStorm, SymbiFlow, VHDL, Verilog, FOSSi Foundation, FPGA design tools, machine learning integration, formal verification, FPGA ecosystem, flexible design tools.**

I. Introduction

Field-Programmable Gate Arrays are programmable, versatile, and powerful semiconductor devices that can be programmed after manufacturing to implement certain functionality specifications. A distinct feature that separates FPGAs from ASICs is the capability of reprogrammability; this allows for iterative design and even adaptation after deployment. The latter characteristic singularly makes FPGAs one of the foundational elements in applications, literally from consumer electronics to space exploration [1] .

FPGAs are impossible to overestimate in their importance among modern technologies. Just two decades ago, due to immense demand for high-speed data processing and adaptability, FPGAs have carved out places in quite a few fields: telecommunications, automotive systems, artificial intelligence, and so on. They allow for the acceleration of machine learning models, support 5G infrastructure, and also realize custom protocols in real-time systems. It is these properties of reconfigurability which render FPGAs quite useful both for prototyping as well as for production where design changes abound, since developers can afterward optimize performance or even add new functionality without a complete remake of the hardware [2].

Traditionally, the development of FPGA-based systems was done using proprietary vendors' tools provided by major FPGA vendors like Xilinx and Intel. While these are feature-rich, they are closed source, very expensive, and generally come with limiting licenses that strongly inhibit access to source code and flexibility in innovative ways. Proprietary tools, such as Xilinx's Vivado or Intel's Quartus Prime, do not give much insight into how things are compiled, synthesized, and routed, thus acting like black boxes where very little can be optimized from the user side. They also tend to make developers stick with particular ecosystems, which decreases portability and collaboration between projects requiring different FPGA platforms [3]. Finally, proprietary tool limitations gave way to open-source FPGA tools. Open-source activities open their innards and let collaboration in, further enabling a developer to enhance and shape the tools to their needs. Events related to open-source FPGA tools reduce costs and democratize access to FPGA technology, enabling educational institutions and hobbyists alike to experiment with FPGAs with no costly licenses. These advantages make the open-source tool exceptionally attractive for researchers and startups by pushing the development of the community-driven approach right into barrier-free FPGA design [4].

This paper will examine the structure and importance of key open-source FPGA tools, including Yosys, Nextpnr, Project IceStorm, SymbiFlow, VTR, and F4PGA, along with the HDL languages they support. The following section will address the challenges and limitations faced by some of these tools. Next, a comparison with proprietary tools will highlight differences in features and functionality. Finally, the paper will explore future directions and potential innovations in open-source FPGA development.

II. What is FPGA tooling?

FPGA tooling encompasses all the software and frameworks needed during the whole development flow of FPGAs, from the very beginning of a design to the generation of a program bitstream. As shown in Fig. 1, FPGA tooling follows several steps: designing, verification, synthesis, place and route, and finally generating the program bitstream that configures the hardware of an FPGA. Each of these steps serves a purpose: design describes the circuit, verification checks for correctness, synthesis generates the logical gates to implement that design,

place and route determines how the gates will be laid out on the FPGA, and the program bitstream is the resultant output actually downloaded to the hardware.

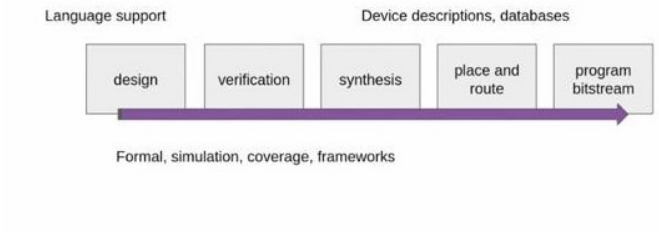

Fig. 1. FPGAs Tooling

Tooling also involves formal verification, simulation, coverage analysis, and various development frameworks, which become necessary in making the design reliable and efficient. This is significantly supported by language support, providing familiar environments to developers for coding their designs, device descriptions, and databases that are necessary for mapping high-level designs to specific FPGA hardware. Without these tools, configuration and optimization of FPGAs would be a very time-consuming and error-prone process [5].

The FPGAs tools have considerably evolved since the very first days of this technology. Early tools were very basic, providing little capability to design and implement a product. As applications in FPGAs increased with complexity, vendors developed proprietary advanced tools that contained advanced features such as high-level synthesis, debugging, and optimization. These vendor-provided tools remained restrictive, limiting the exposure and flexibility needed for the larger community of developers. Open-source FPGA tools have indeed come of age. For instance, open-source tools like Yosys for synthesis, Nextpnr for place and route, and Project Trellis for device support are redefining the developers' interaction with FPGAs, opening up more collaboration spaces. These tools come to the front because of their adaptability, the ability to work across various FPGA platforms, and their potential for innovation without constraints from proprietary ecosystems alone. [6]

III. Open-source FPGA tool-chains

The open-source movement has had a profound impact on both hardware and software development. On the software level, open-source has completely changed the way we think of collaboration, with open-source repositories like GitHub hosting literally thousands of projects that anyone can help contribute to. In the hardware world, the open-source movement has taken much, much longer, mostly because of some very real difficulties and associated costs with developing hardware. On the other hand, OpenCores, RISC-V, and the open-source FPGA ecosystem do try to shut that gap by making a philosophy against sharing knowledge to reduce costs. Free and open-source FPGA tools constitute a part of a greater movement towards having no friction in the process of hardware development. They give access to basic toolchains that one needs when working with FPGAs without having any financial or licensing constraints tied to proprietary tools. Such a movement is democratizing not only FPGA development but innovating, too, by allowing users to deeply understand and customize the tools for their needs [7]. The result of this movement has been the creation of complete FPGA toolchains that remain at parity with proprietary offerings. These toolchains consist of a set of free and open-source tools that serve every stage in the FPGA design process, from design entry to bitstream generation. Common core tools found within the open-source toolchains include Yosys, Nextpnr, Project IceStorm, SymbiFlow, Verilog to Routing, VTR, and F4PGA. Each one of these tools plays a designed role within the toolchain, adding its unique capabilities to the process of development.

1) **Yosys** is one of the pioneering open-source synthesis tools capable of translating high-level hardware descriptions, mainly in Verilog, to gate-level netlists. The output from this translation is a low-level circuit representation that may be further processed by place-and-route tools, thereby completing the implementation on the FPGA architecture. The most characteristic feature of Yosys is its flexibility and modularity, allowing easy extension and customization. Its modular design allows adding new passes and transformations to the tool with minimal effort. In this way, it could adapt to different synthesis flows on various FPGA architectures, so far. Yosys natively supports Verilog synthesis and provides partial support for VHDL using external plugins. Key features include comprehensive scripting capabilities, native support for formal verification, and easy integration with open-source simulators like Verilator. Together with a placer and router such as Nextpnr, Yosys allows designers to reach the best customization and functionality of open-sourced hardware design by providing a complete synthesis and implementation flow. [4], [6]
   For Yosys, a typical flow from synthesis can be conceptualized in Fig. 2. Initially, a VHDL design file (design.vhd) undergoes conversion to Verilog format (design.v) using a tool like vasy. This Verilog file then enters Yosys with an input script (design.tcl) that directs the synthesis process. Yosys outputs a BLIF (Berkeley Logic Interchange Format) netlist (design.blif), which represents the gate-level circuit. This netlist can then be converted to a VHDL structural Alliance netlist (design.vst) through blif2vst, ready for further steps in FPGA design. This flow highlights Yosys's interoperability with multiple file formats and tools, enabling efficient conversion and synthesis across different hardware description languages and FPGA architectures [11].

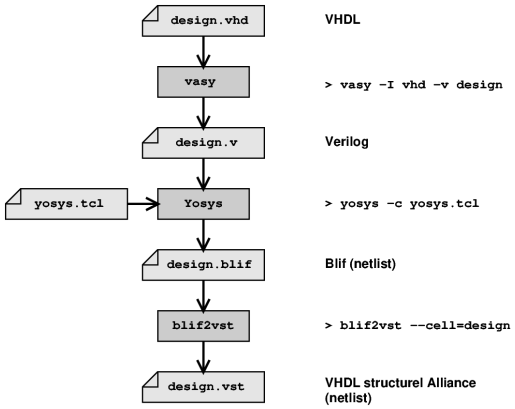

Fig. 2. Yosys's synthesis flow

2) **Nextpnr** is an open-source place-and-route tool that has the capability to run the mapping logic from the netlist onto physical resources from FPGAs. It supports a number of FPGA architectures, including Lattice iCE40, ECP5, and Xilinx Series-7, by means of a flexible architecture database format. This makes it easier to adapt to new FPGA families since most changes required for new architecture support are already implemented in the code. Distinctive features in nextpnr are the integration of various backend databases, whereby Project Trellis allows efficient design porting between different FPGA devices. Further, nextpnr provides an elaborative and customizable routing algorithm to fine-tune different FPGA families, making developers do their work for a wide range of applications [4], [6].Graphical User Interface: Fig. 3 further extends this functionality by providing a graphical representation of the routing process and allows designers to experiment and optimize their designs interactively. This scalability and flexibility has made nextpnr a favorite choice across the board, from the tiny Lattice iCE40 designs all the way to the larger, more complex Xilinx-based applications [12].

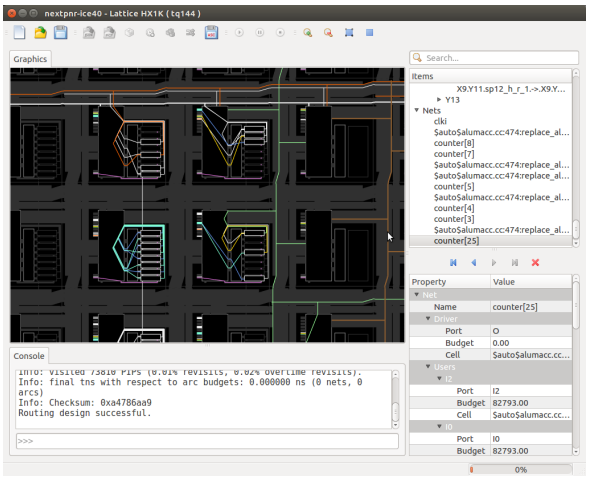

Fig. 3. GUI Nextpnr

3) **Project IceStorm** is an open-source toolchain developed mainly to target the Lattice iCE40 series of FPGAs. It provides a complete toolchain for such devices, including bitstream generation. In short, Project IceStorm enables developers to have full control over design and programming by providing an open-source counterpart of proprietary Lattice tools. The major components are: Yosys synthesizer, nextpnr performing place-and-route, and IcePack does the packing of designs into bitstreams. Once generated, these bitstreams are programmed to the FPGA using IceProg. Such openness and accessibility make Project IceStorm a very compelling choice for educational and research projects, demonstrating the benefits of using open-source tools and offering insight and flexibility not possible with a vendor-provided solution. Its broad approach has made it a hit with developers who prefer the control and visibility provided by open-source tooling. [4], [6]
4) **SymbiFlow** is one such open-source FPGA toolchain that intends to support multiple FPGA families from various vendors, including Xilinx and Lattice. By combining several state-of-the-art open-source tools, such as Yosys for synthesis, nextpnr for place-and-route, and Project Trellis for Xilinx Series-7, SymbiFlow intends to create a general-purpose toolchain that can work seamlessly across various FPGA ecosystems. SymbiFlow basically develops one general-purpose toolchain that evades the need for vendor-specific tools, thereby helping developers stay away from vendor lock-in. Due to the device-specific abstract in its modular architecture, it works with various families of FPGAs without having to switch out toolchains. This level of flexibility and broad device support makes SymbiFlow an interesting option for anyone requiring interoperability across a diverse range of FPGA platforms due to its wide solution space that meets open-source requirements and cross-platform development with minimal friction [4], [6]. Fig. 4 effectively demonstrates how these tools interact within the SymbiFlow ecosystem to offer a streamlined FPGA development process [13].

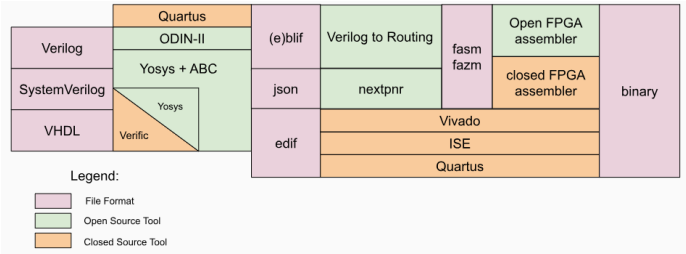

Fig. 4. SymbiFlow Toolchain Components

5) **Verilog to Routing VTR** is an open-source framework that is widely used both in academia and research while approaching the study and exploration of new FPGA architectures and their related CAD flows [5]. VTR

is providing a full CAD flow from Verilog synthesis through to routing and supports many different architectural models, thus allowing researchers to experiment with new FPGA structures and algorithms. The general VTR CAD flow, as illustrated in Fig. 5, includes the following stages: elaboration, synthesis, technology mapping, packing, placement, routing, and timing and area estimation that allow the end-to-end design flow from a Verilog circuit to an optimized FPGA layout. It starts with a Verilog circuit that is elaborated using the Odin II; this result then goes through synthesis and technology mapping using ABC. Its successive steps, in order, of packing, placement, and routing are controlled by VPR, which is driven by an FPGA architecture description file. The last step in this sequence would be timing and area estimation, upon which quality of results would depend. This flexibility and openness of VTR have provided a key vehicle that advances the state of the art in next-generation FPGA design flows and allows both architectural and CAD strategies to take quick leads through deep explorations possible in FPGA design. [14]

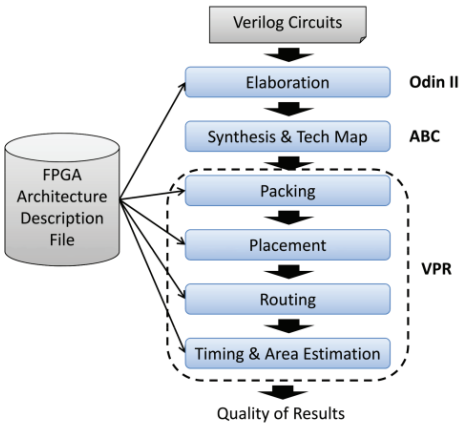

Fig. 5. VTR CAD Flow

6) **F4PGA**, formerly known as SymbiFlow, is an open-source FPGA development platform; it encapsulates many different tools and projects within one toolchain. In Fig. 6, it may be seen that F4PGA provides architecture definitions from such projects as Project X-Ray, Project U-Ray, QuickLogic DB, and Project IceStorm so that many platforms of FPGAs can be supported. These architecture definitions are packaged and stored in Google Cloud Storage (GCS) buckets that can be accessed from F4PGA examples and from CI tests, among other components. This modular and framework-oriented approach allows developers to integrate new tools and libraries seamlessly supporting synthesis, place-and-route, and bitstream generation. The model's adaptability and community-driven development make F4PGA flexible towards various FPGA platforms that are targeted by developers, hence encouraging more and more growth in the open-source FPGA community [15].

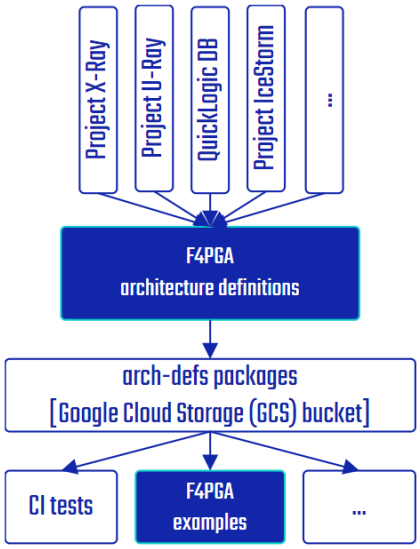

Fig. 6. F4PGA Architecture Overview

IV. Comparison with Proprietary Tools

The rise of open-source FPGA tools has prompted comparisons with proprietary tools like Xilinx's Vivado and Intel's Quartus Prime. Such comparisons typically address a handful of key criteria: performance, flexibility, usability, community support, and cost. Each one of these factors shows different strong and weak points for the open-source and proprietary approaches, respectively, as shown in Fig. 7.

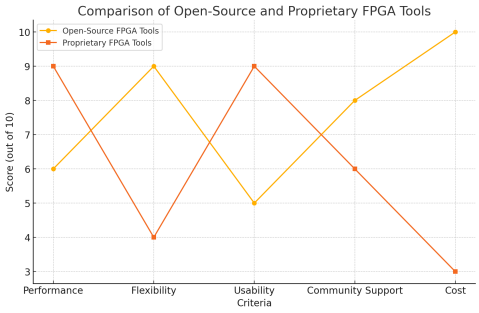

Fig. 7. Comparison Overview

Proprietary tools usually have an edge in performance: they provide very optimized designs, advanced timing closure support, and sophisticated optimization algorithms. All these capabilities enable proprietary tools to generate timing-accurate bitstreams with high efficiency in synthesis and place-and-route. Open-source tools differ in their performance. The latter ones might be less effective since, with limited access to specific routing algorithms, their capabilities related to timing and area optimization can hardly compete with proprietary tools [4], [5].This is usually in the name of flexibility. Open-source tools are more adaptable since they support multiple

vendors, meaning that their developers can work across various platforms. On top of this, their open-source nature means that it is possible for them to be changed and extended to suit custom architectures. Proprietary tools normally operate within vendor-specific ecosystems, with limited compatibility with alternative devices and architectures. This rigidity forms a barrier for developers who plan to or would like to work in multi-vendor setups or test customized architectures. Usability is another area in which proprietary tools are naturally very good. They often boast user-friendly graphical interfaces and integrated debugging and simulation tools that even newcomers among FPGA developers can use. Open-source tools are mostly command-line driven and might require technical manual setup. Of course, some open-source tools already provide GUI support like nextpnr. [4], [6].

On community support, open-source tools have solid communities supporting them. Active development is found on systems such as GitHub. There is extensive documentation, and contributors very often make resources available for learning and troubleshooting. Formal technical support tends to be limited to the community itself. In turn, proprietary tools enjoy official support from the vendors, full-featured documentation, and technical teams that can be helpful for developers in finding reliable assistance and swift solutions. [3], [7]

Ultimately, another very important differential factor is cost. The open-source tool is free and open-source-to-use, making them a very attractive option for projects that have tight budgets and educational institutions. That, in turn, permits smaller teams, independent developers, and educational programs access to resources for FPGA development without significant costs. Proprietary tools provide high licensing fees that may be extremely prohibitive for smaller organizations and/or independent developers without any corporate backing. [3], [7]

V. VHDL AND VERILOG SUPPORT

HDLs are essential of FPGA development, and two popular vehicles by which a designer describes the behavior and structure of digital circuits remain VHDL and Verilog. Both languages have strengths and applications; Verilog is generally more popular in the United States and for commercial applications, while VHDL enjoys widespread usage in Europe and for aerospace and defense projects. This has made supporting these HDLs a critical focus area for developers to extend the usability and adoption of open-sourced FPGA tools.

Verilog is a popular HDL because of the ease and efficiency with which digital logic can be described. The open-source FPGA tools have heavily invested in supporting Verilog-based synthesis flows. Yosys, the cornerstone of the open-source toolchain, natively supports Verilog for synthesis and a number of optimization passes on it. Such strong support for Verilog has been instrumental in paving the way for opensource tools for the vast amount of developers who already know the language. The main highlights of the support of Verilog in open-source tools are as follows:

- *Wide Language Coverage:* There is extensive language coverage whereby most of the Verilog-2001 standard constructs have been handled by Yosys, although work is still on the way for further enhancements for subsets of SystemVerilog . [4], [6]
- *Integration with Simulators:* Yosys is well integrated with full-featured, freely available Verilog simulators such as Verilator and Icarus Verilog, which are used very frequently for the purpose of Verilog design verification.
- *Optimizations:* Yosys provides a number of passes that optimize the Verilog designs for logic minimization and resource sharing, helping to enhance the results of synthesis.

VHDL is a strongly typed language that demands stringent design. For this reason, it remains a favorite in industries that require very high-reliability systems. Open-source tool support for VHDL is partly an area under development.It provides:

- *GHDL Integration:* Yosys is integrated with GHDL, an open-source VHDL simulator, allowing for the synthesis of VHDL designs. GHDL supports the full VHDL-93 standard and partial support for newer standards, such as VHDL-2008 [4], [6].
- *Mixed-Language Designs:* By using Yosys and GHDL together, mixed-language designs can be synthesized, allowing Verilog and VHDL modules to operate side by side. This is essential for legacy systems or projects with components written in both HDLs [4], [7].
- *Ongoing Development:* Although VHDL support in Yosys is less mature compared to Verilog, it is continuously and rapidly improving, thanks to ongoing community development efforts to enhance compatibility and add additional VHDL features to the synthesis and verification flow [6].

The following Fig.8 shows Comparison of Verilog and VHDL Support in Open-Source FPGA Tools. Verilog enjoys broader support, while VHDL is gradually gaining traction through GHDL integration.

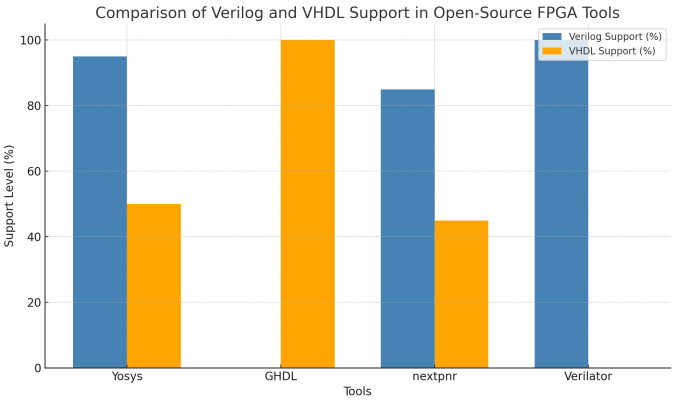

Fig. 8. Comparison of Verilog and VHDL

Open-source FPGA tools are now under heavy development and continuously add more VHDL support; indeed, thanks to

growing contributions from community members and industrial demands. For instance, one of the most important efforts is getting Yosys integrated with GHDL, in some sense, and an already fully functional VHDL synthesis flow is available. As maturity and new features are added to GHDL, an open-source toolchain will also have near-parity in VHDL support in relation to a proprietary tool. This is a very real reason for increased VHDL functionality, and the driving force behind this comes from the industrial requests from industries such as aerospace, defense, and telecommunication, where, due to set design principles, there is a standard usage of VHDL. Also, many universities in Europe teach digital design using VHDL, and most of them require easy-to-access tools that at least support the language for educational purposes. Support for VHDL is also required for projects dealing with legacy codebases or existing IP cores in VHDL . While open-source FPGA development focused on supporting Verilog first, the continued improvement of VHDL support is extending its reach to be more suitable for use in industries or users whose design workflow requires the use of both Verilog and VHDL to develop FPGAs.

VI. Challenges and Limitations

Despite the many advantages provided by the open-source FPGA toolchains, a number of issues and limitations still remain to be fixed in order to encourage wider adoption, especially within commercial workflows. The first usually would have to do with the disparity in supporting languages. While Verilog support in tools like Yosys has grown quite extensive and well-developed, VHDL support lagged. This is quite a barrier for industries and projects reliant on VHDL, as it has been one of the most widely used languages in industries like aerospace, defense, and telecommunications—not to mention that legacy codebases or existing IP cores are usually written in VHDL [8]. While this integration with GHDL has allowed a way to synthesize VHDL designs, the maturity level is still far from the comprehensive support that was found in proprietary tools. Hence, open-source tools still fall short for projects requiring VHDL.

The second most critical limitation is the gap in timing closure and optimization. The proprietary tools, such as Xilinx's Vivado and Intel Quartus, feature advanced algorithms in timing analysis and optimization that make it possible for the designers to arrive at strict performance requirements for high-end systems. They rely on multiple years of development and vendor-specific know-how, which allows them to offer state-of-the-art timing and power optimization that simply cannot be replicated using the open-source options today. While the open-source community is actually working in this direction, the development of such functionality takes a lot of time and expertise, along with knowledge of FPGA hardware details, which in most cases is not publicly shared. This puts the open-source FPGA tools at a disadvantage in competing applications where exact timing and power optimization matter, especially in commercial and high-performance applications [9].

In spite of the technical limitations, there exist many obstacles to the adoption and integration of open-source FPGA tools within commercial workflows. The leading challenge is that no official vendor supports it. Proprietary tools get extensive support and backing from FPGA manufacturers like Xilinx and Intel, but open-source tools are left on their own without any direct contact with the vendors. For developers working with open-source tools, community-driven support will be their only resort, and this support has become intermittent, with hardly any assurance of issues that are complex getting resolved in time. A significant headache for projects requiring fast troubleshooting or extensive debugging resources is indeed a fact that open-source tools rely on the community for support, thus limiting their feasibility in large-scale projects where speed is a factor. The documentation and learning curve for open-source FPGA tools are cumbersome. Though the open source community has done a lot to clean things up, still proprietary tools have slick, detailed user guides and tutorials combined with technical support. For companies investing in proprietary tools, this is an added benefit: these resources can reduce the learning curve and enable faster onboarding of new members. While open-source projects might be rich in community-driven documentation, it may be disjointed and without cohesion and clarity, which a vendor-provided one could supply, hence getting new users up to speed quickly and effectively remains a challenge. [8], [9]

VII. Future directions and innovations for open-source tools

The future indeed seems bright for open-source FPGA tools, basing their success on the collaborative effort of the community, increased interest from industry, and rapid technological advancement. These tools will evolve further as new contributors grow out of academia, hobbyist communities, and industry, meaning that the gap compared with proprietary solutions will continue to decrease. One important trend in this development is the improvement in the support of languages, especially VHDL and SystemVerilog. Improving support for these languages will make open-source tools more attractive for industries where established workflows rely on these languages. This could widen their application and appeal. Indeed, there are several efforts already to enhance VHDL support, such as the work currently being carried out on integrating GHDL with Yosys. Similarly, an extension of SystemVerilog support may provide a number of new opportunities for its adoption, as shown in Fig. 9 [8], [9]. Another exciting trend in the development of open-source FPGA tools is the push for advanced optimization algorithms. These community-driven efforts would advance the sophistication of the algorithms for timing closure, routing, and power optimization that would close part of the gap to proprietary tools like Vivado and Quartus. This, in turn, means that once these features are more developed, it would be possible for developers in high-performance applications to use open-source tools more successfully and have optimized designs without having to rely on proprietary software [8].

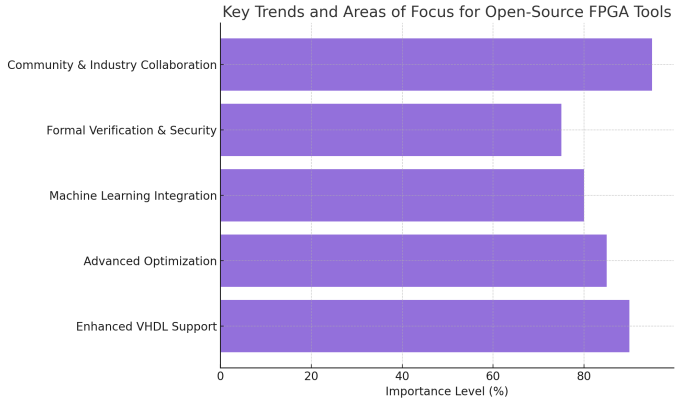

Fig. 9. Key trends and areas for the future development

There are a number of other innovative approaches under exploration to further improve open-source FPGA tools, whereby machine learning takes the leading role. In this regard, several researchers have tried to utilize machine learning algorithms for enhancement and efficiency in both FPGA synthesis and place-and-route processes. Applications of machine learning to such tasks may promise to bring design quality and compilation times well within the range of making open-source tools highly attractive for complicated design projects. If successful, such steps indeed promise a quantum leap and can match or even excel in capabilities compared to certain proprietary tools. Other focus areas are formal verification and security, since FPGA designs keep on growing in complexity. It becomes very important to make sure that designs are correct and secure, particularly in safety-critical applications. More advanced formal verification capabilities are foreseen to be integrated into open-source FPGA tooling, empowering designers to find and mitigate a wide range of potential issues much earlier on in the design cycle. Such improvements would allow not only a better design reliability but also would bring the opensource tools in step with industry standards concerning the security and robustness of the developed products, further supporting their adoption in regulated industries [[10].

The open-source FPGA community is alive and growing thanks to the contributions coming from academia, hobbyists, and companies believing in the potentiality of open-source hardware. SymbiFlow, now called F4PGA, collaborations and the FOSSi Foundation is one of the key drivers in very active pushes of the effort of development and standardization that eventually will set up a much more coherent ecosystem of open-source FPGA utilities. There is also an industrial support contribution that is growing, for example, Google, to this end, including the OpenHW Group by providing resources and expertise to further develop these tools. This convergence of community and industry support creates a strong foundation for the growth of open-source FPGA tools in the future and allows them to evolve to appeal to a wide range of user classes. As these efforts progress, open-source FPGA tools hold the potential to change the face of FPGA development by offering a realistic alternative to proprietary solutions and democratizing access to advanced digital design capabilities. [9], [10]

VIII. Conclusion

The open-source FPGA ecosystem has grown a lot and offers openness and flexibility that is not provided by proprietary FPGA development tools. The most important tools that have made FPGA design cheaper and more community-driven include Yosys, Nextpnr, Project IceStorm, and SymbiFlow. While open-source tools generally lag behind their commercial equivalents in a number of ways, such as limited VHDL support and primitive timing optimization, they offer valuable options for universities and individual developers and research projects. These tools certainly enable collaboration and innovation, sustained by active communities and organizations such as the FOSSi Foundation. While proprietary tools are still leading in many optimizations and some vendor-specific features, open-source FPGA tooling keeps evolving, with promising steps regarding language support, machine learning integration, and verification techniques. This progress points toward a future where FPGA technology is accessible to more people, enabling more exploration and innovation without the limitations of costly, closed ecosystems.

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IX. DECLARATION OF ORIGINALITY

I hereby declare that I myself have written this paper, and that I have not used any external sources other than those mentioned. Anything borrowed from a different source, whether phraseology or idea, is duly acknowledged. I further declare that this paper has not previously been submitted for any course or examination, in this form or in a similar version.

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