RESET SW1

27pF C1
Y1
4.000MHz
C2 27pF
R2 1KΩ

C3
47µF

R1 27K
R3 1KΩ
R4 1KΩ
R5 1KΩ

AK1
100nF

MC6809

U2
74HC138

U3
74HC04

U4
74HC154

IO_B-F
J11

IO_3-7
J10

Y2
C5
U5
65C51N
C4
AK5
100nF

USB
J18
J15
UART $C604

J13
GND
J12
+5V

HM6264
$0000-$1FFF

HM6264
$2000-$3FFF

HM6264
$4000-$5FFF

HM6264
$6000-$7FFF

HM6264
$8000-$9FFF

HM6264
$A000-$BFFF

2764
$E000-$FFFF

GND
J9
+5V

U10
AK10
100nF

U11
AK11
100nF

U12
AK12
100nF

U13
AK13
100nF

U14
AK14
100nF

U15
AK15
100nF

R12 1KΩ
R13 4KΩ

U16
AK16
100nF

U22
PTM $C408
MC6840
AK22
100nF

U20
ACIA $C006
MC6850
AK20
100nF

U21
ACIA $C206
MC6850
AK21
100nF

ACIA $C206
J1
J2
ACIA $C006
J16
USB
J17
USB

U28
MC6821
PIA PA $D00C
PIA PB $D00C
PIA $D00C
AK28
100nF
J4
J5

U29
MC6821
PIA PA $D20C
PIA PB $D20C
PIA $D20C
AK29
100nF
J6
J7

U30
MC6821
PIA PA $D40C
PIA PB $D40C
PIA $D40C
AK30
100nF
J8

J14
DataBus

CPU X-3

Rev: 2
Issue: 2024-12-29
Title: CPU X-3
Design: Roger Landén