REPORT

Design of Reconfigurable LFSR for VLSI IC Testing in FPGA

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Introduction

Linear Feedback Shift Registers (LFSRs) are widely used in VLSI testing, especially for generating pseudo-random sequences. This project involves designing a reconfigurable LFSR, which can be used for both ASIC and FPGA-based VLSI IC testing. The reconfigurable LFSR provides flexibility in selecting different tap configurations, allowing it to generate different pseudo-random sequences as needed for various test patterns.

LFSR

- A Linear Feedback Shift Register (LFSR) is a type of digital circuit used to generate sequences of binary numbers.
- It is widely utilized in various applications, including cryptography, error detection and correction, random number generation, and digital signal processing.
- LFSRs are known for their simplicity and efficiency in generating pseudo-random sequences.

Working of a LFSR

- An LFSR consists of a shift register and a feedback mechanism. The shift register is made up of flip-flops, each holding a bit of data.
- On each clock cycle, the bits in the register are shifted one position to the right (or left), with the most significant bit (MSB) being filled by the output of the feedback logic.
- The feedback logic typically involves XOR (exclusive OR) operations on selected bits of the register, referred to as "taps."
- The positions of these taps are determined by a characteristic polynomial, which defines the sequence generated by the LFSR.

Objectives

- Design a reconfigurable LFSR with customizable tap positions.
- Implement the LFSR in FPGA environment.
- Validate the design through simulation and synthesis.

Standard LFSR

- A **standard LFSR (Linear Feedback Shift Register)** is a digital circuit with a fixed configuration where the taps (specific bit positions used for feedback) and the polynomial are predetermined during design.
- This configuration determines the sequence of bits generated by the LFSR, which remains consistent every time the circuit is reset.
- Due to its simplicity, a standard LFSR is easy to implement and is commonly used in applications where a known and consistent sequence is required, such as in error detection (e.g., CRC) or pseudo-random number generation.

Reconfigurable LFSR

- A **reconfigurable LFSR** allows for the dynamic selection of taps and possibly even the seed value during operation, providing the flexibility to generate different sequences based on changing requirements.
- This added flexibility comes with increased complexity, as additional logic is needed to handle the reconfiguration.
- Reconfigurable LFSRs are particularly useful in environments like VLSI testing for ASICs and FPGAs, where the ability to adapt the sequence for different testing scenarios or fault conditions is crucial.

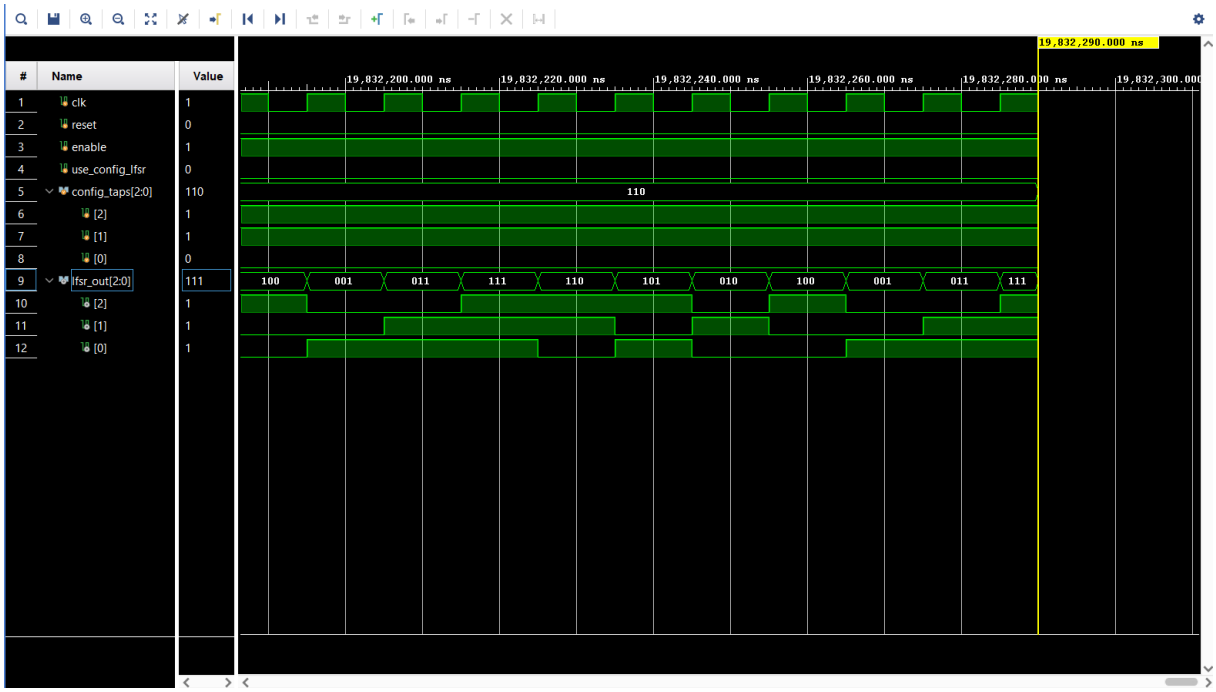
Observations

Simulation in FPGA Environment

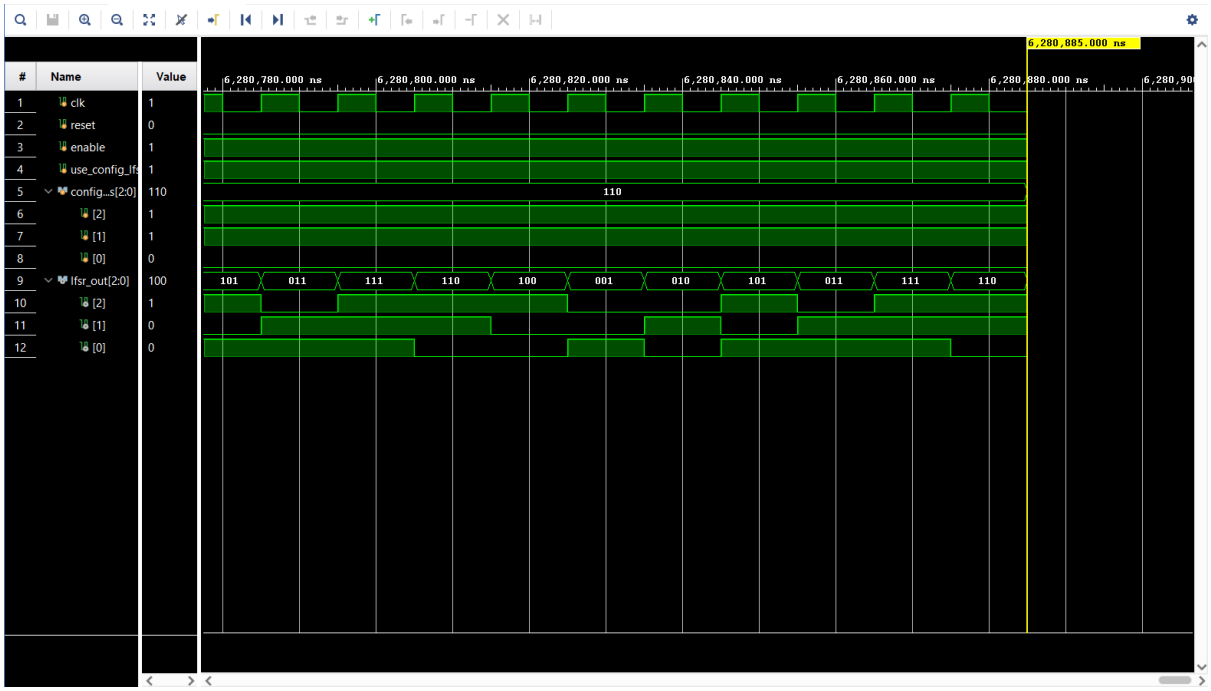
- The LFSR generated a pseudo-random sequence as expected.
- It works as a standard LFSR when the value of “use_config_lfsr” is 0 and it works as a reconfigurable LFSR when the value if “use_config_lfsr” is 1.
- Different tap configurations produced different sequences, demonstrating the reconfigurability.
- The timing constraints were met, with a clock period of 10 ns.

Result

- **Standard LFSR**



❖ **Reconfigurable LFSR**



Conclusion

- The reconfigurable LFSR was successfully designed and implemented in the FPGA environment.
- The design demonstrated flexibility through reconfigurable tap positions and was verified through extensive simulation and synthesis.
- The project highlights the trade-offs between FPGA and ASIC implementations in terms of performance, area, and power.