# OKI semiconductor

# MSM2128RS

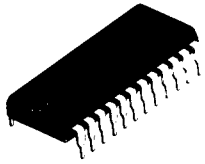
## 2 KW x 8 BIT STATIC RAM

## GENERAL DESCRIPTION

The OKI MSM2128 is a 16384 bits static Random Access Memory organized as 2048 words by 8 bits using Advanced N-channel Silicon Gate MOS technology. It uses fully static circuitry throughout and no clocks or refresh are required. The reduced standby power dissipation is automatically performed by CS control. Single +5 V Power supply. All inputs and outputs are directly TTL compatible. Common data I/O using three-state outputs. The 24 pin package is pin compatible with standard 16 K UV Erasable Programmable ROM.

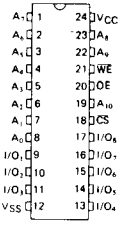
## FEATURES

- Single power supply
- External clock and refresh operation not required
- Access time
  - MSM2128-12RS . . . 120ns (max)
  - MSM2128-15RS . . . 150ns (max)
  - MSM2128-20RS . . . 200ns (max)
- Low power dissipation
  - during operation . . . MSM2128-15RS/20RS
  - . . . 550 mW (max)
  - . . . MSM2128-12RS
  - . . . 660 mW (max)
  - during standby . . . 110 mW (max)
- TTL compatible I/O
- Three-state I/O
- Common data I/O capability
- Power down mode using chip select signal
- Convertibility of pins used in 16KEPROM MSM2716



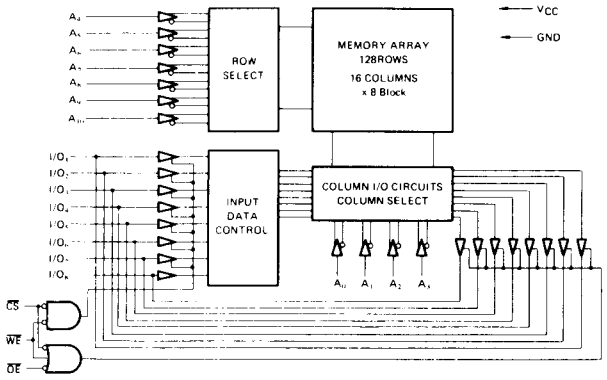
## PIN CONFIGURATION

(Top View)




$A_0 \sim A_{10}$: Address Inputs
$I/O_1 \sim I/O_8$: Data Input/Output
$V_{CC}$: Power (5V)
$V_{SS}$: Ground
$\overline{WE}$: Write Enable
$\overline{CS}$: Chip Select
$\overline{OE}$: Output Enable

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit | Conditions |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.5 to 7 | V | Respect to $V_{SS}$ |
| Input Voltage | $V_{IN}$ | −0.5 to 7 | V | |
| Operating Temperature | Topr | 0 to 70 | °C | |
| Storage Temperature | $T_{stg}$ | −55 to 150 | °C | |
| Power Dissipation | $P_D$ | 1.0 | W | |

## DC AND OPERATING CHARACTERISTICS

($T_a$ = 0°C to + 70°C, $V_{CC}$ = 5V ±10%, unless otherwise notes.)

| Parameter | Symbol | 2128-12RS | | | 2128-15/20RS | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Input Load Current | $I_{LI}$ | −10 | | 10 | −10 | | 10 | μA | $V_{CC}$ = Max.<br>$V_{IN}$ = GND to $V_{CC}$ |
| Output Leakage Current | $I_{LO}$ | −10 | | 10 | −10 | | 10 | μA | $\overline{CS}$ = $\overline{OE}$ = $V_{IH}$,<br>$V_{CC}$ = Max.<br>$V_{out}$ = GND to $V_{CC}$ |
| Operating Current | $I_{CC}$ | | | 120 | | | 100 | mA | $V_{CC}$ = Max. $\overline{CS}$ = $V_{IL}$<br>I I/O = 0 mA $t_{cyc}$ = Min. |
| Standby Current | $I_{SB}$ | | | 15 | | | 15 | mA | $V_{CC}$ = Min. to Max.<br>$\overline{CS}$ = $V_{IH}$ |
| Peak Power-on Current | $I_{SBP}$ | | | 20 | | | 20 | mA | $V_{CC}$ = GND to $V_{CC}$ = Min.<br>$\overline{CS}$ = Lower of $V_{CC}$ or $V_{IH}$ |
| Input Voltage | $V_{IH}$ | 2 | 5 | 6 | 2 | 5 | 6 | V | Respect to Vss |
| | $V_{IL}$ | −0.5 | 0 | 0.8 | −0.5 | 0 | 0.8 | V | |
| Output Voltage | $V_{OH}$ | 2.4 | | $V_{CC}$ | 2.4 | | $V_{CC}$ | V | $I_{OH}$ = −1.0 mA |
| | $V_{OL}$ | | | 0.4 | | | 0.4 | V | $I_{OL}$ = 2.1 mA |

**Notes 1.** Typical limits are at $V_{CC}$ = 5V, $T_a$ = 25°C, and specified loading.

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## AC CHARACTERISTICS

($T_a$ = 0°C to + 70°C, $V_{CC}$ = 5V ± 10%, unless otherwise noted.)

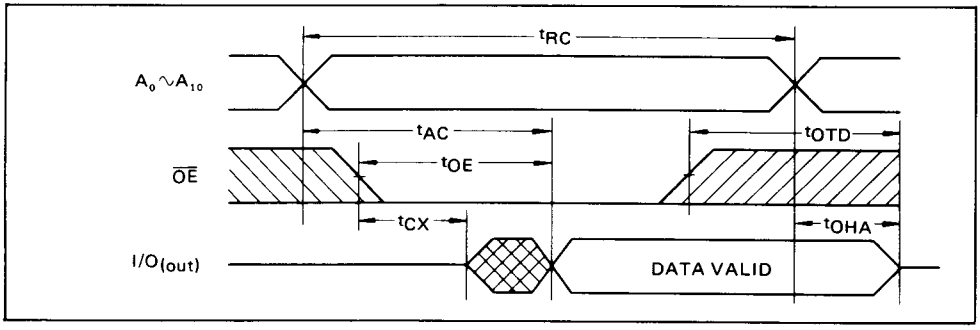
## AC TEST CONDITIONS

| Parameter | Conditions |
|---|---|
| Input High Level | 2.0V |
| Input Low Level | 0.8V |
| Input Rise and Fall Times | 10 ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | $C_L$ = 100 pF, 1TTL Gate |

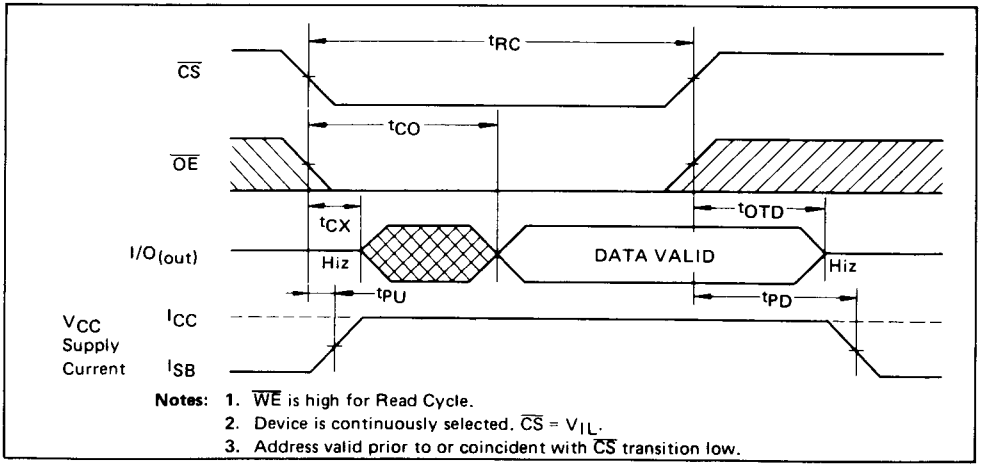
## READ CYCLE [1]

| Parameter | Symbol | 2128-12RS | | 2128-15RS | | 2128-20RS | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Read Cycle Time | $t_{RC}$ | 120 | | 150 | | 200 | | ns | |
| Address Access Time | $t_{AC}$ | | 120 | | 150 | | 200 | ns | |
| Output Enable to Output Delay | $t_{OE}$ | | 50 | | 60 | | 70 | ns | |
| Chip Select Access Time | $t_{CO}$ | | 120 | | 150 | | 200 | ns | |
| Chip Selection to Output in Low Z | $t_{CX}$[2] | 10 | | 10 | | 10 | | ns | |
| Chip Selection to Output in High Z | $t_{OTD}$[3] | 0 | 40 | 0 | 50 | 0 | 60 | ns | |
| Output Hold from Address Time | $t_{OHA}$ | 10 | | 10 | | 10 | | ns | |
| Chip Select to Power Up Time | $t_{PU}$ | 0 | | 0 | | 0 | | ns | |
| Chip Select to Power Down Time | $t_{PD}$ | | 50 | | 60 | | 80 | ns | |

## READ CYCLE NO. 1 [8] [9]




## READ CYCLE NO. 2 [8] [10]



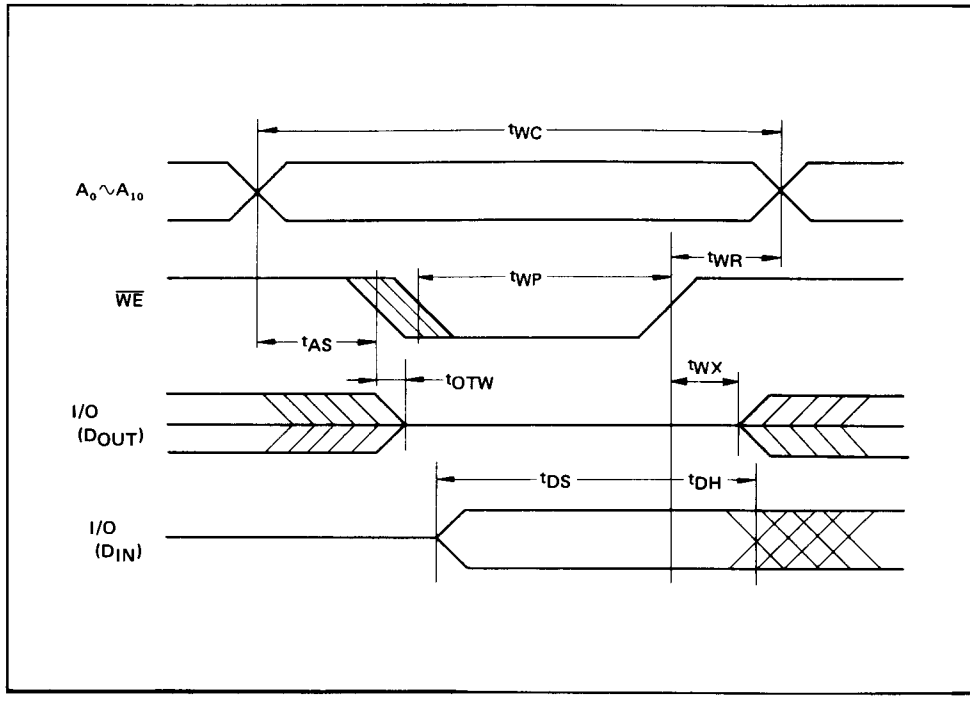

**Notes:** 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = $V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

## WRITE CYCLE (4)(5)

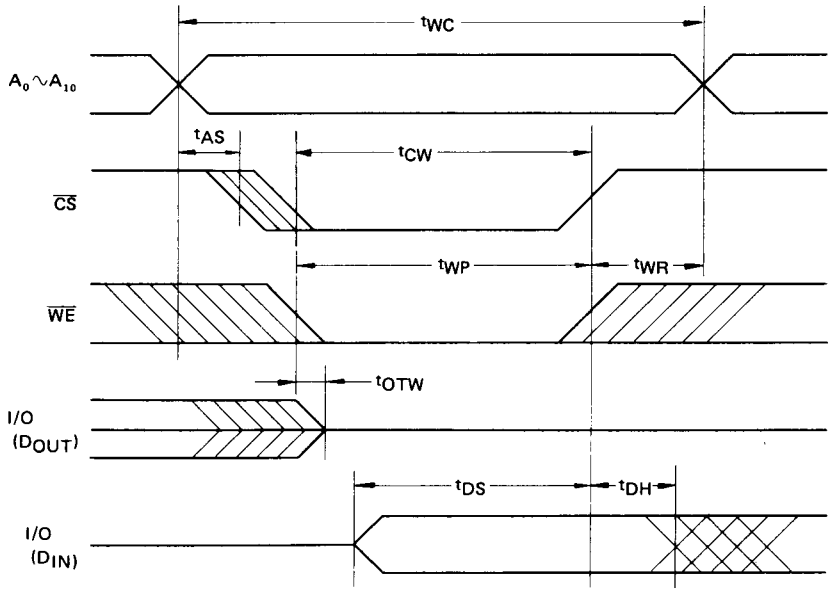
| Parameter | Symbol | 2128-12RS | | 2128-15RS | | 2128-20RS | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Write Cycle Time | $t_{WC}$ | 120 | | 150 | | 200 | | ns | |
| Chip Selection to End of Write | $t_{CW}$ | 90 | | 120 | | 150 | | ns | |
| Address Setup Time | $t_{AS}$ | 20 | | 20 | | 20 | | ns | |
| Write Pulse Width | $t_{WP}$ | 60 | | 80 | | 100 | | ns | |
| Write Recovery Time | $t_{WR}$(6) | 10 | | 10 | | 10 | | ns | |
| Data Valid to End of Write | $t_{DS}$(6) | 50 | | 70 | | 90 | | ns | |
| Data Hold Time | $t_{DH}$(6) | 10 | | 15 | | 15 | | ns | |
| Write Enabled to Output in High Z | $t_{OTW}$(7) | 0 | 40 | 0 | 50 | 0 | 60 | ns | |
| Output Active from End of White | $t_{WX}$ | 5 | | 5 | | 5 | | ns | |

**Notes**
1. A read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. $t_{CX}$ is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. $t_{OTD}$ is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
5. $\overline{OE}$ may be allowed in a Write Cycle both high and low.
6. $t_{WR}$, $t_{DS}$, and $t_{DH}$ are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
7. $t_{OTW}$ is specified by the time when DATA OUT is floating, not defined by output level.

## WRITE CYCLE NO. 1(11)(13)



## WRITE CYCLE NO. 2[12][13]




**Notes** 1. $\overline{WE}$ control mode
2. $\overline{CS}$ control mode
3. When I/O pins are Data output mode, don't force inverse signal to these pins.

## FUNCTION TRUTH TABLE

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Mode | Output | Power |
|---|---|---|---|---|---|
| H | X | X | Not Selected | High Z | Standby |
| L | L | X | Write | High Z | Active |
| L | H | L | Read | $D_{OUT}$ | Active |
| L | H | H | Not Selected | High Z | Active |

## CAPACITANCE

($T_a$ = 25°C, f = 1 MHz)

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Input/Output Capacitance | $C_{I/O}$ | | 8 | pF | $V_{I/O}$ = 0V |
| Input Capacitance | $C_{IN}$ | | 6 | pF | $V_{IN}$ = 0V |

Note: This parameter is periodically sampled and not 100% tested.