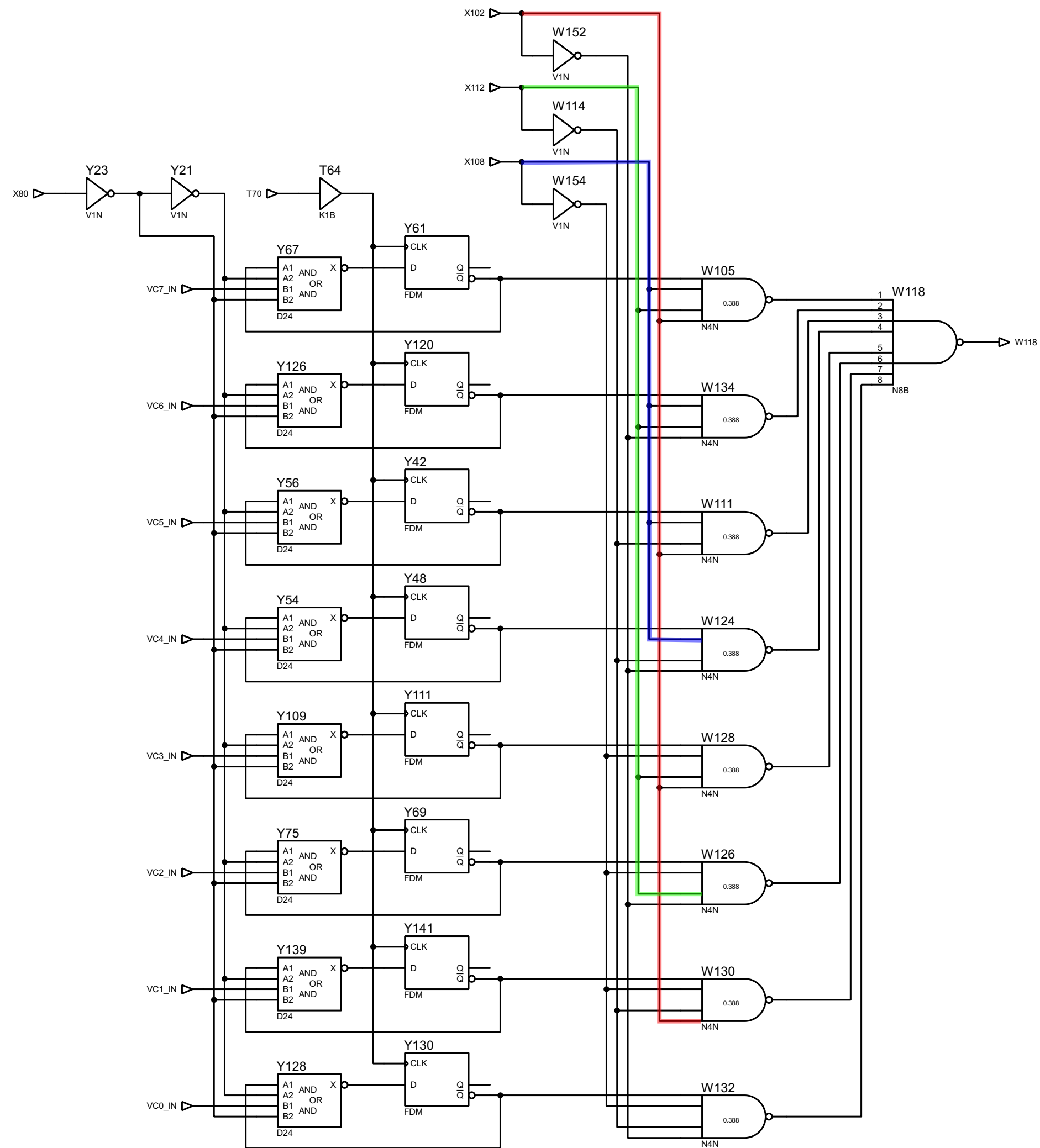
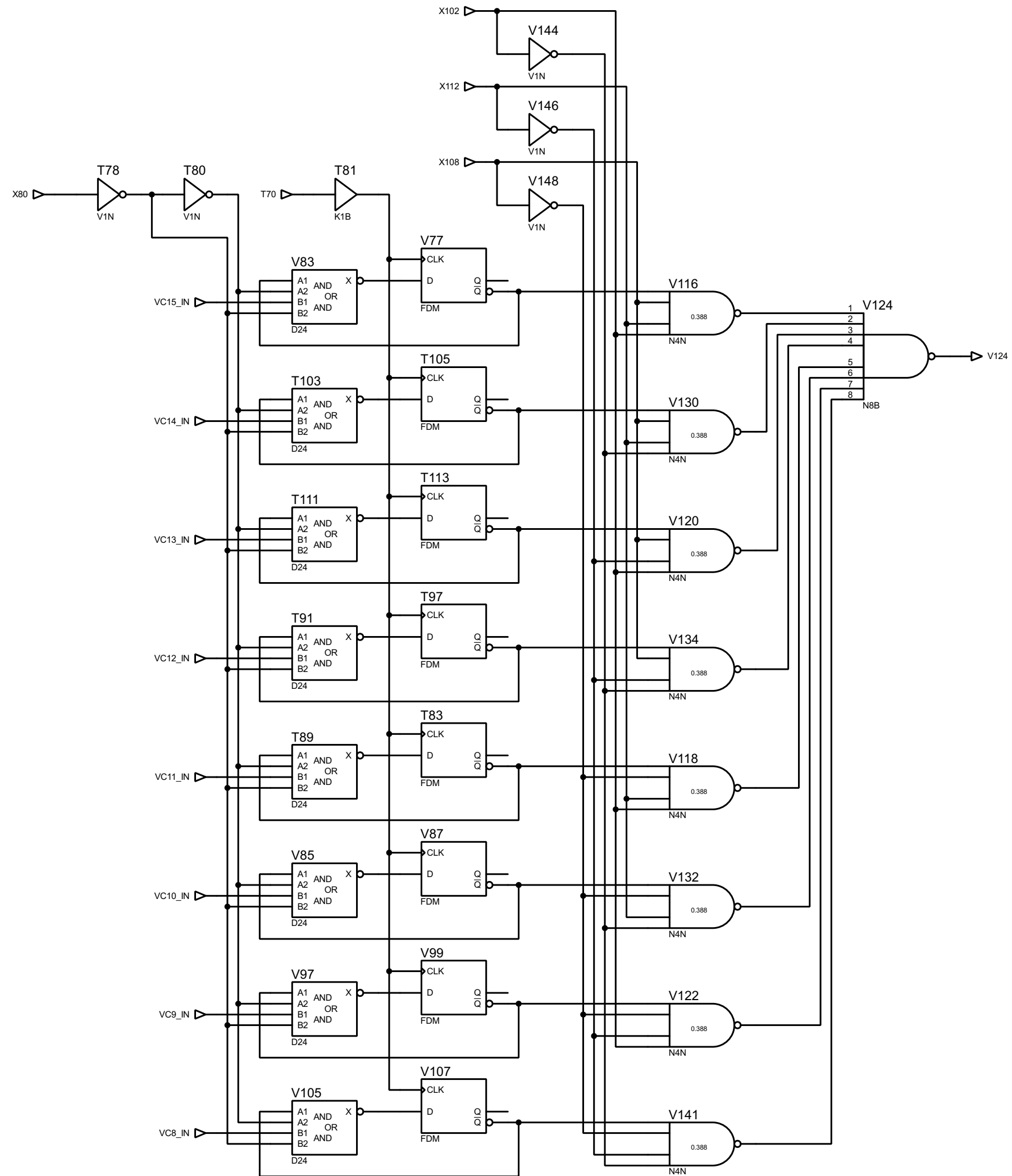
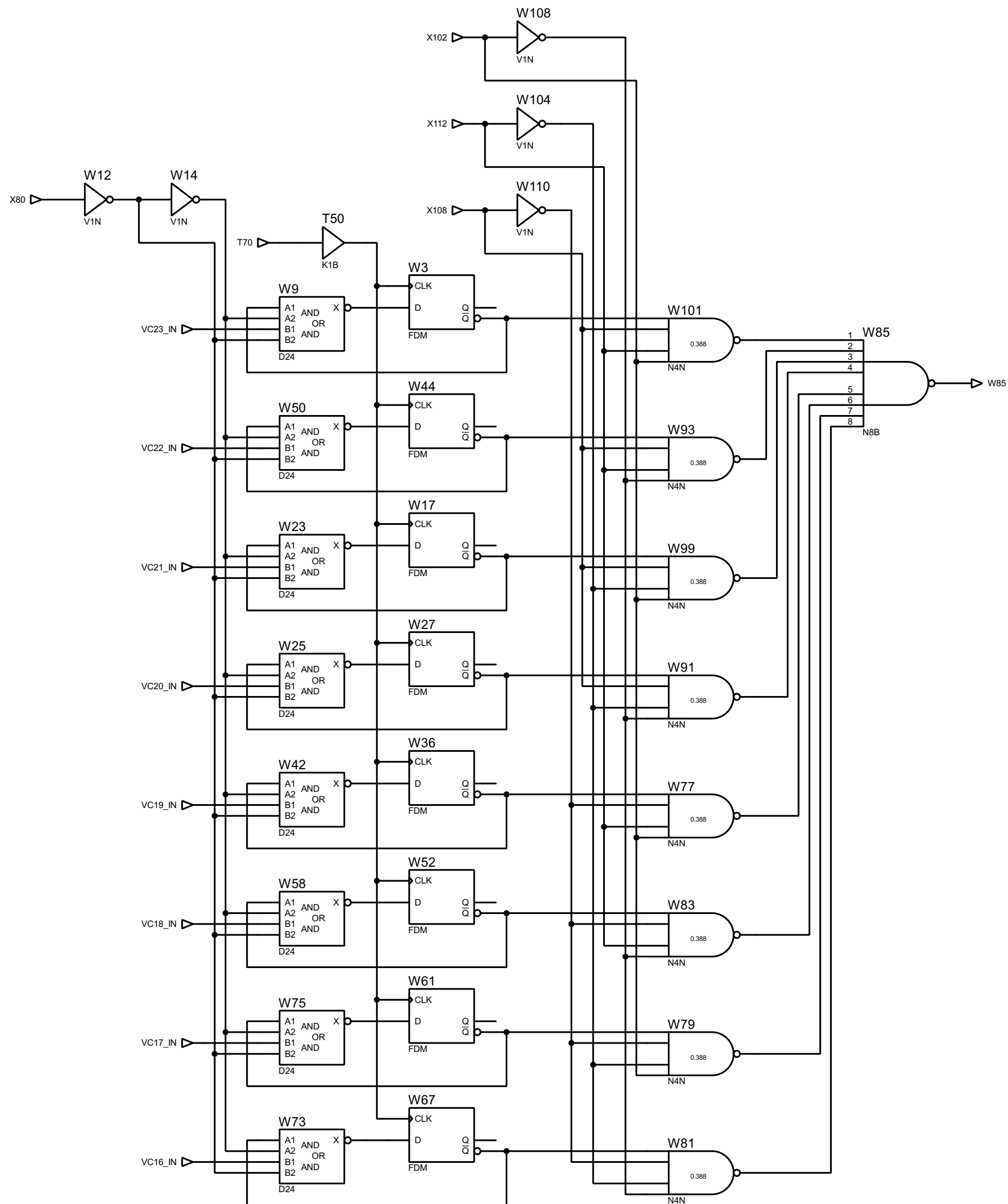


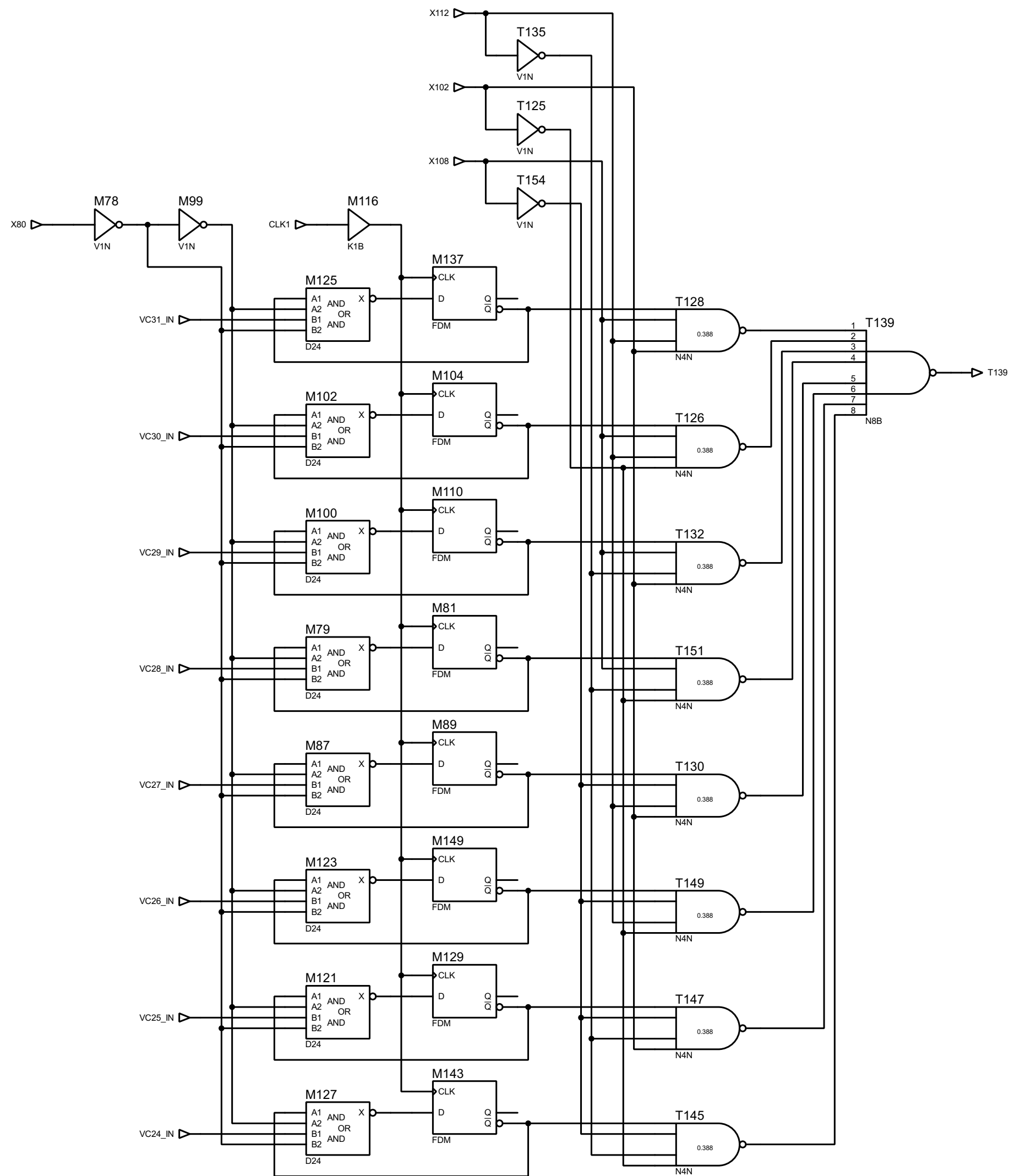
COL0 -> DSBA ???

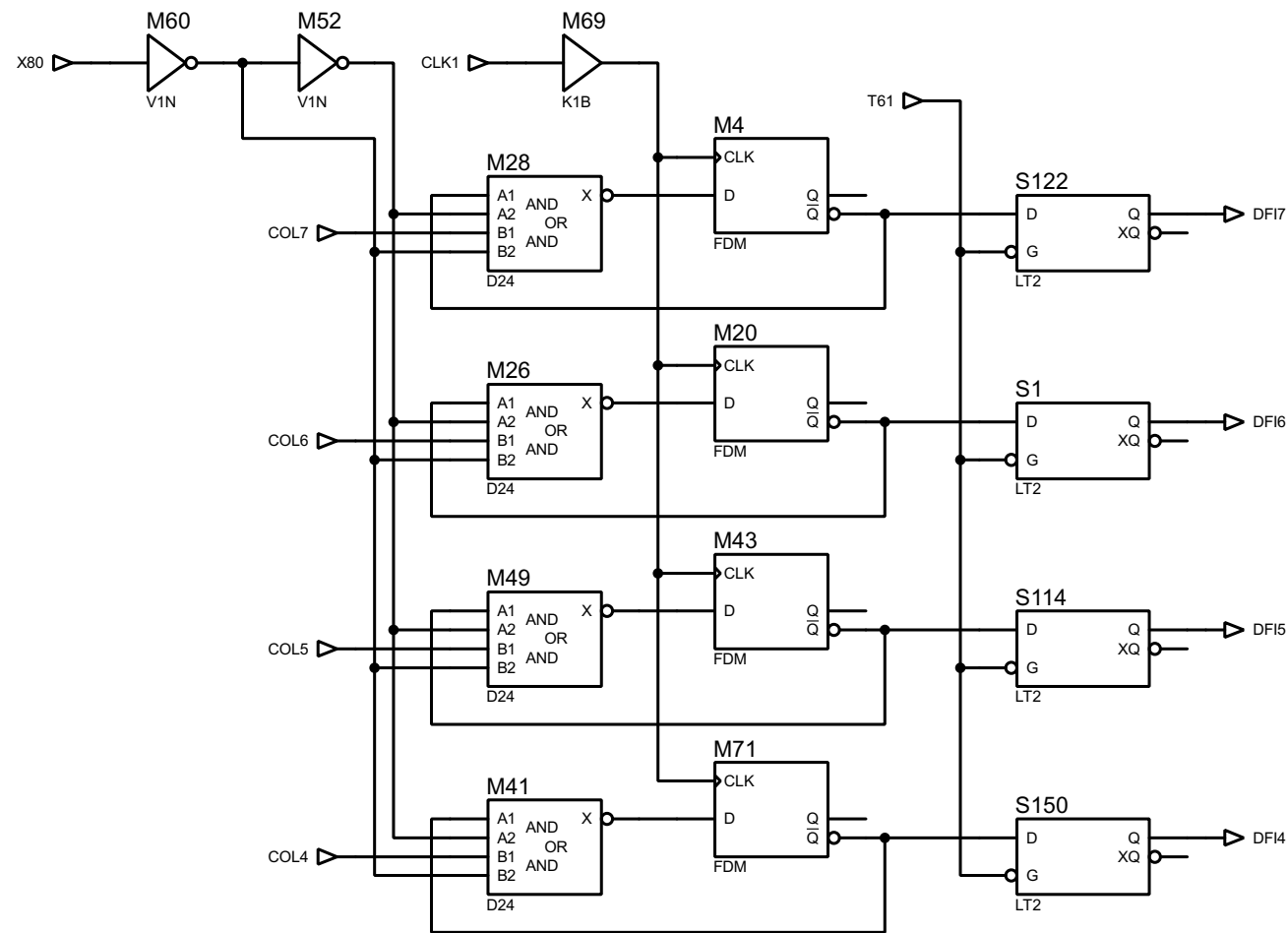












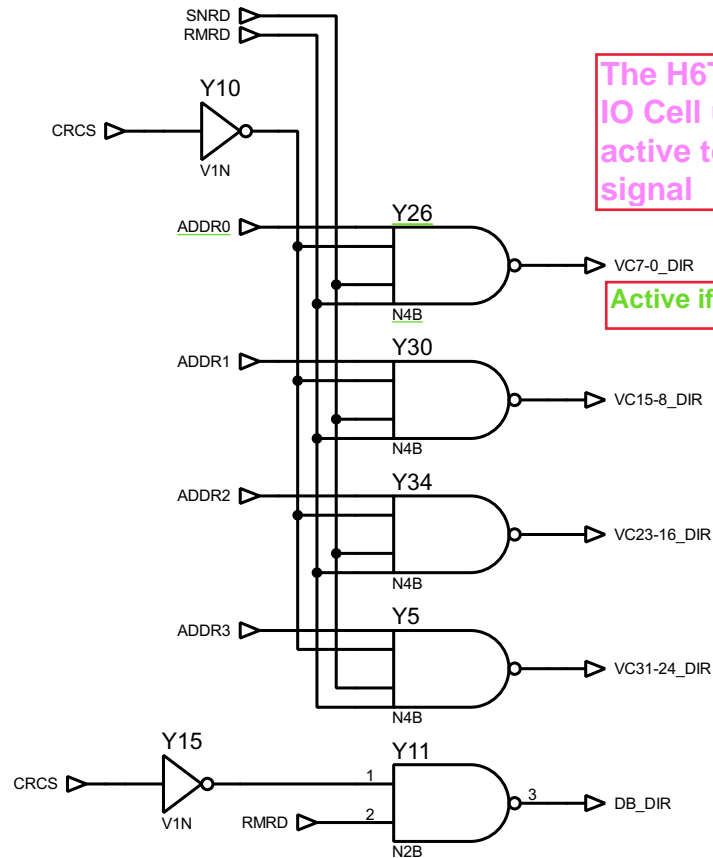
SNRD=1 W to 051962  
SNRD=0 R from 051962  
RMRD = 1 read VC ROM data into DB  
(select VC byte using AB[1:0])  
RMRD = 0 DON'T READ FROM ROM  
CRCS = 0 ACTIVE -> I/O ACTIVITY  
BETWEEN CPU AND 051962/051961  
CRCS = 1 INACTIVE -> DISCONNECTED  
FROM CPU BUS

ADDR0	RMRD	SNRD	~CRCS	VC7-0_DIR
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
...	...	...	...	...
1	1	1	1	0 ACTIVE

ADDR0=1  
RMRD=1  
SNRD=1 W  
CRCS=1 NO ACTIVE

VC7-0\_DIR = 1 ROM SPACE -> 051962 VC (NORMAL USE)  
VC7-0\_DIR = 0 051962 -> ROM SPACE (DEV & TESTING)

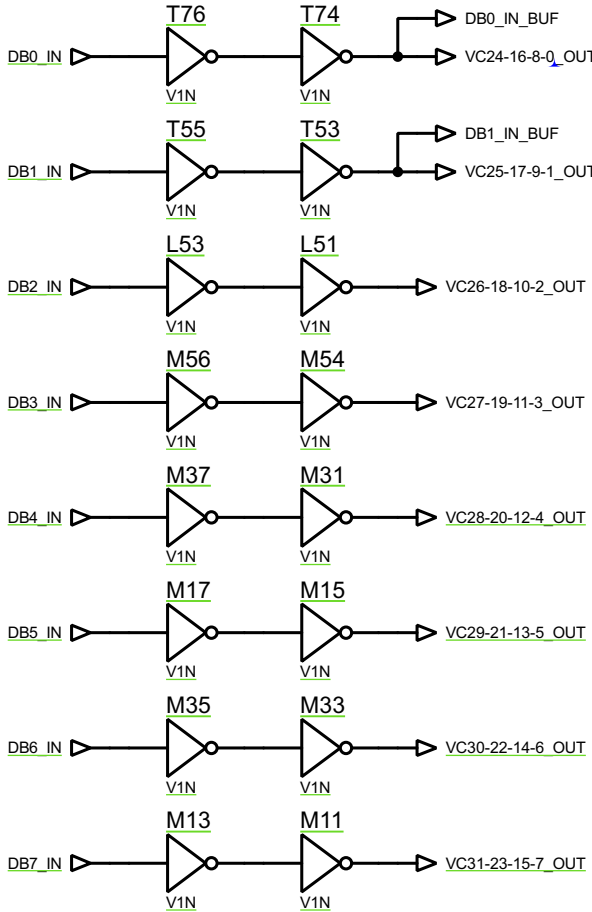
VC15-8\_DIR ADDR1=1  
VC23-16\_DIR ADDR2=1  
VC31-24\_DIR ADDR3=1



The H6T Tristate  
IO Cell uses OEn  
active to low  
signal

Active if VC7-0\_DIR=0

CRCS	RMRD	DB_DIR ~(CRCS & RMRD)
0	0	1
0	1	1
1	0	1
1	1	0 ACTIVE



DB\_IN -> VC\_BYTE\_OUT VC31-24\_OUT  
VC23-16\_OUT  
VC15-8\_OUT  
VC7-0\_OUT

