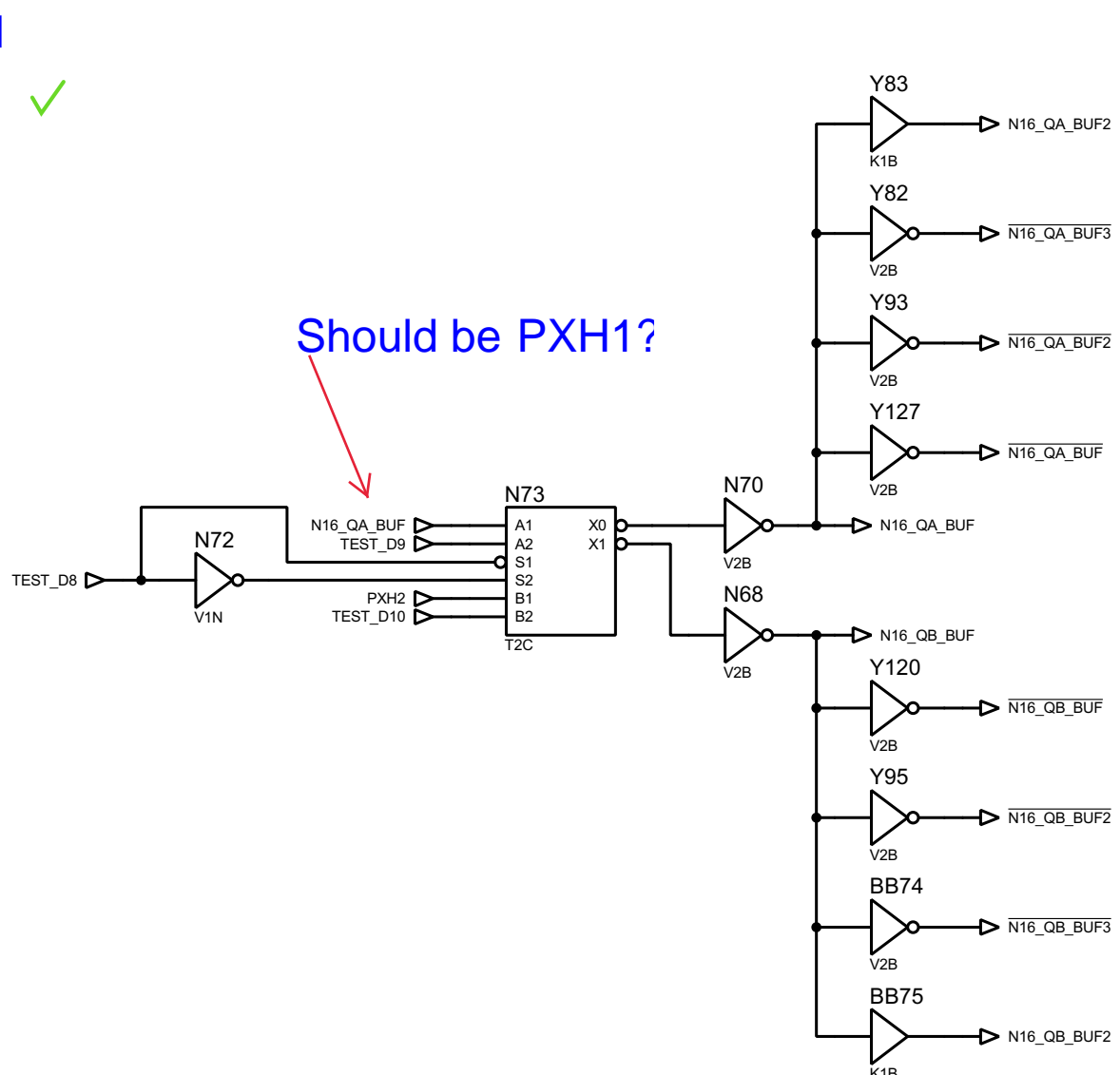


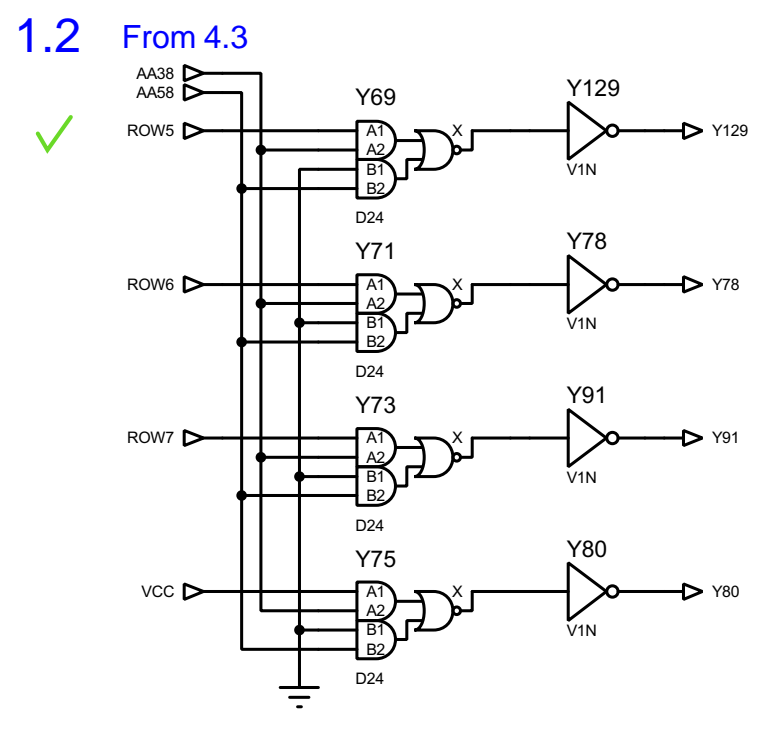
```

VRAM Address (1 word per address)
FEDC BA98 7654 3210
0000 00xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 1101 xxxx xxxx Layer C scroll
0000 1101 xxxx xxxx A X scroll
0001 00xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 1100 xxxx xxxx B Y scroll
0001 1101 xxxx xxxx B X scroll
0001 1101 xxxx xxxx X tilemaps X
          xx xxx X Tilemaps Y

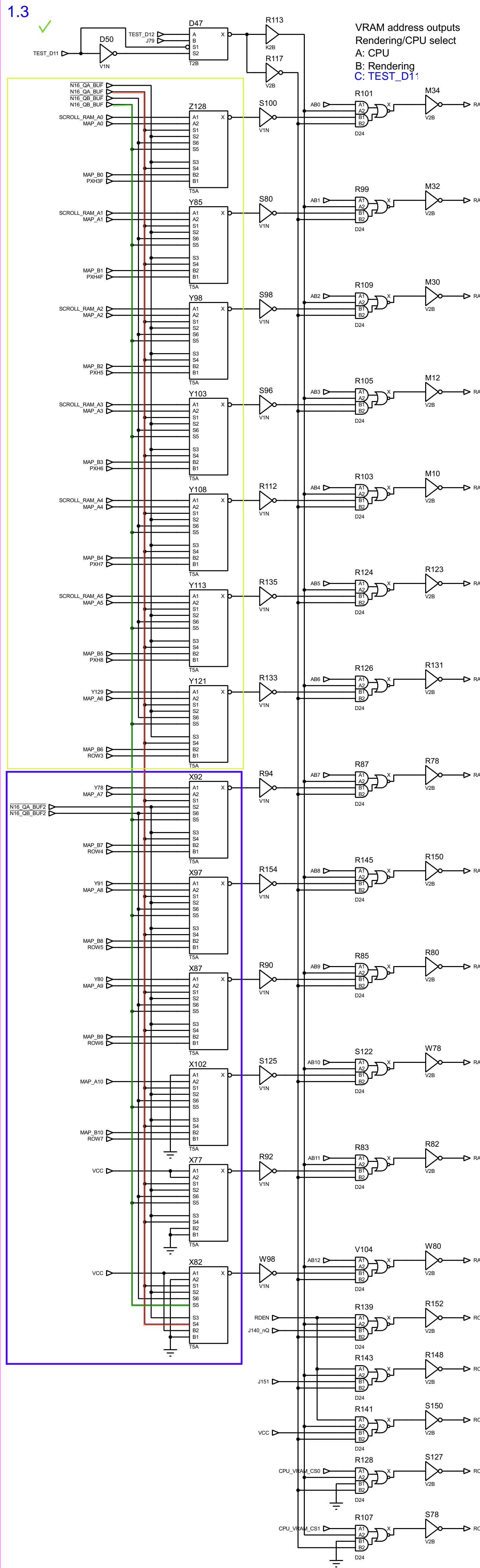
```

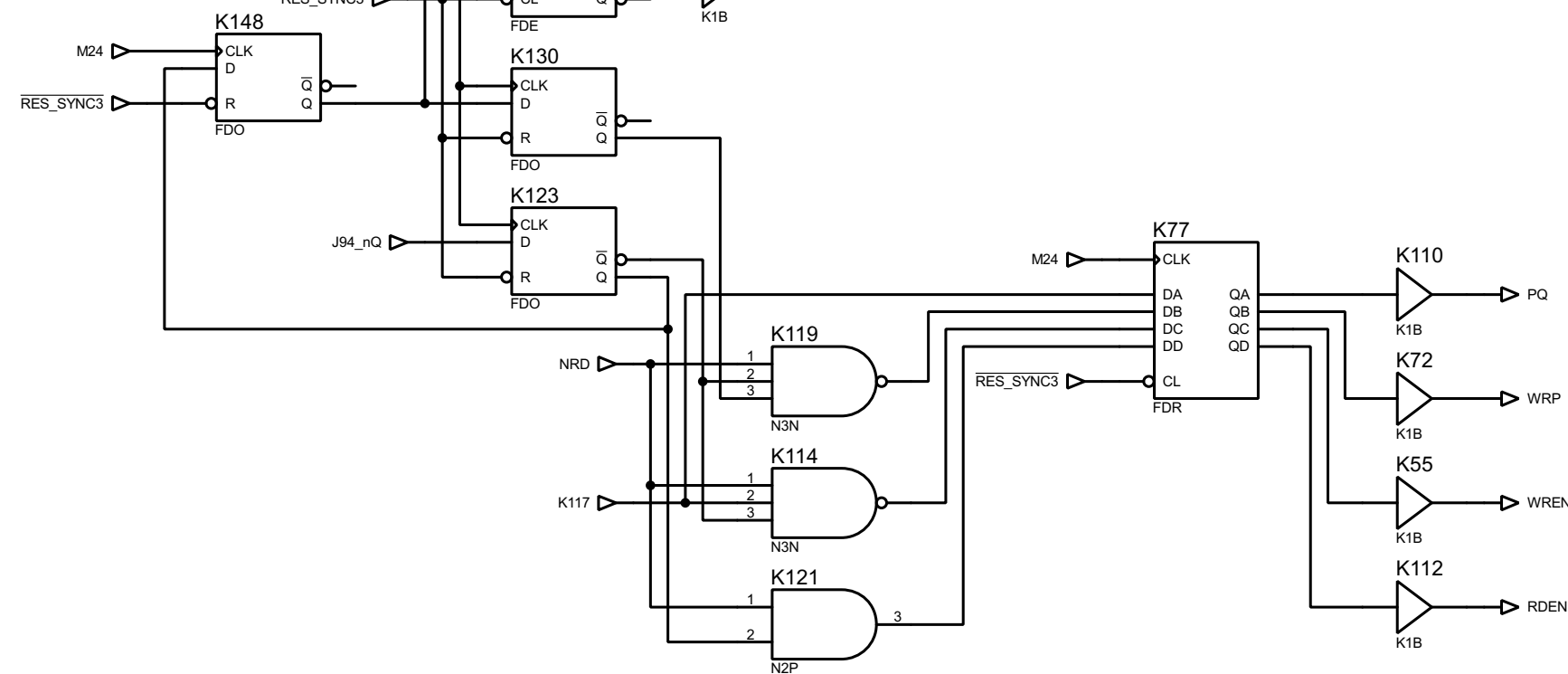
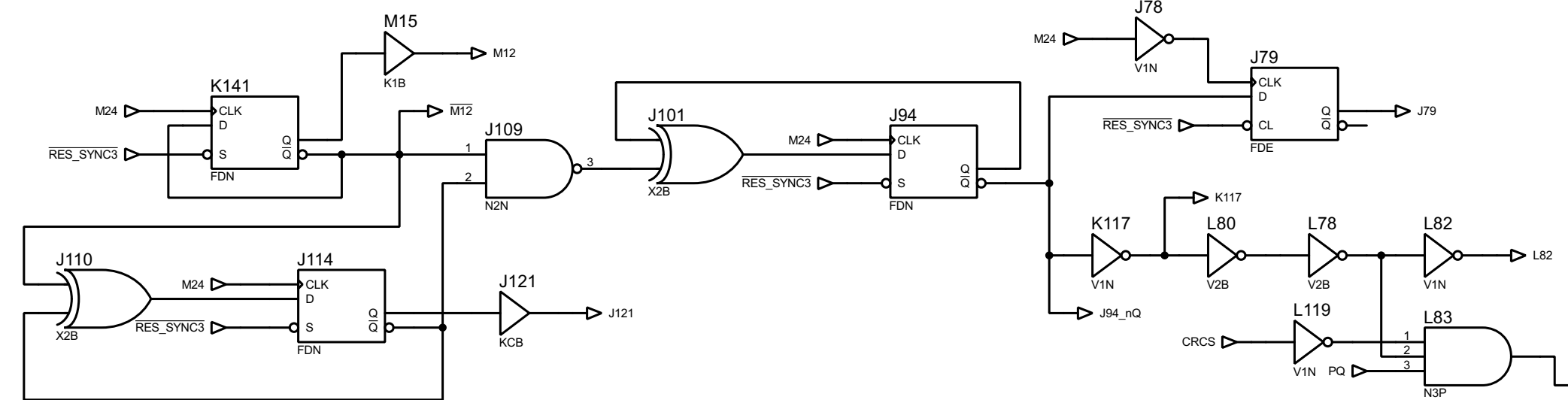


## TEST\_D13 Addresses Selector



Selection can be simplified using AA38 (and AA38n) only  
AA58 always selects 1'b0.

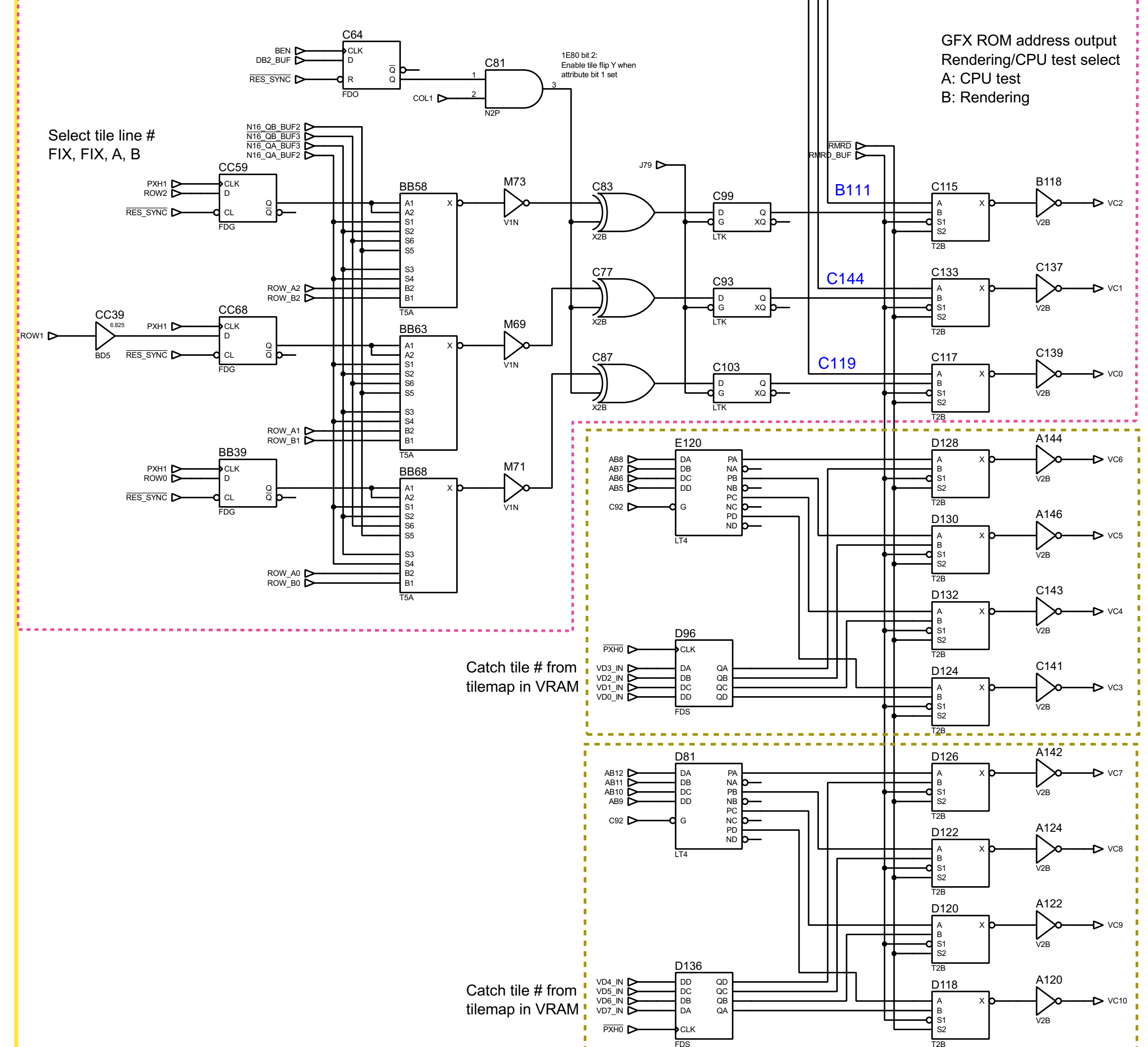




## TIMING SIGNALS

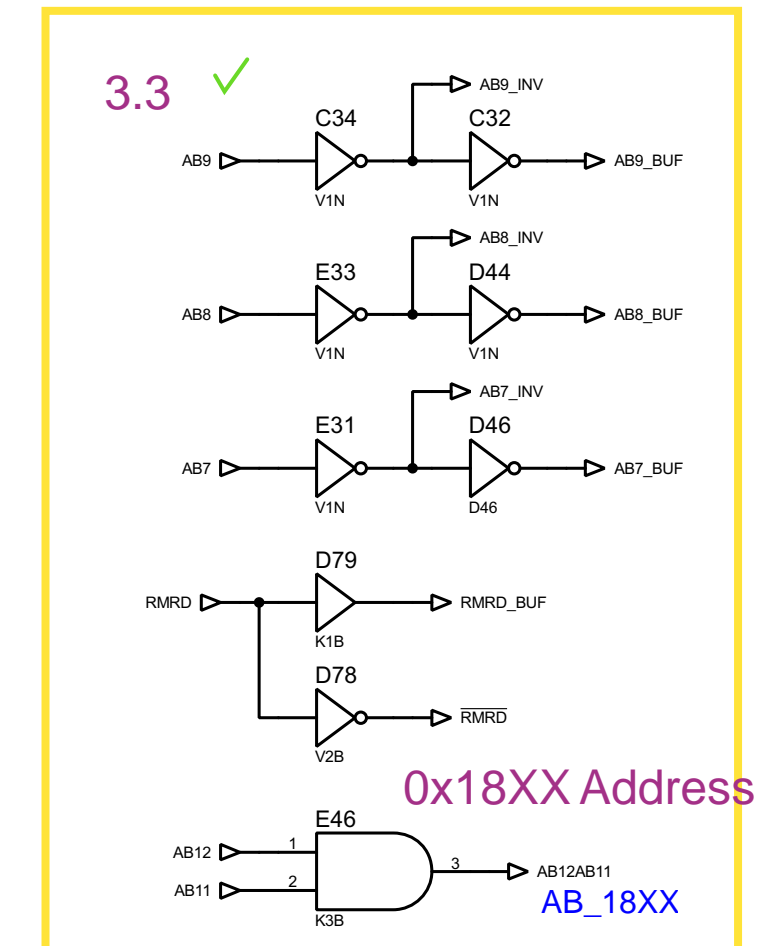
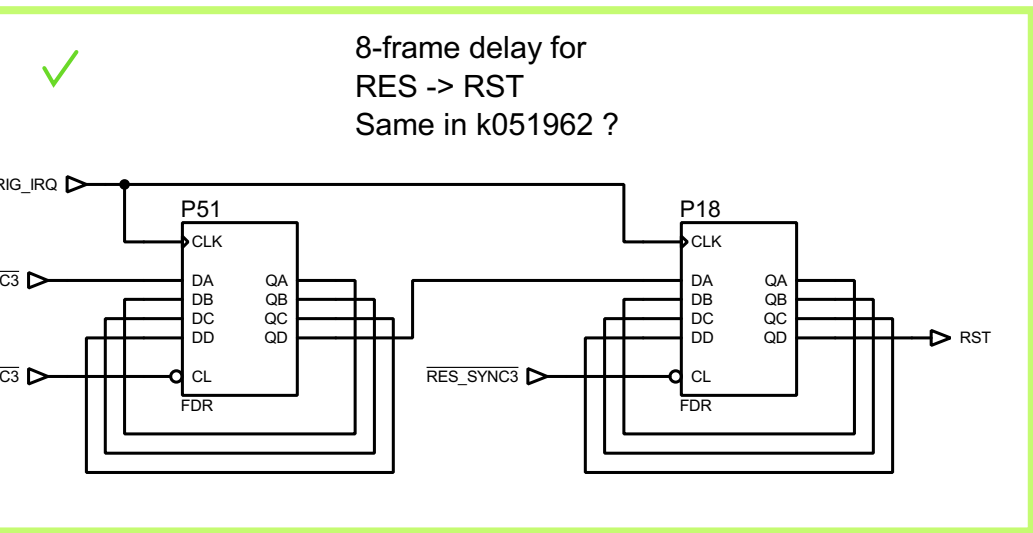


SKIP because AB[1:0] used to select byte



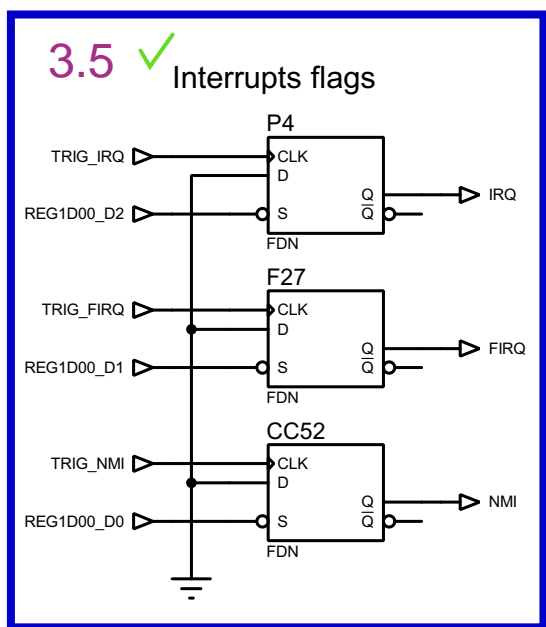
### 3.1 ✓

The diagram shows a circuit for a 3-bit counter. It consists of three main components: an N122 flip-flop, an M74 3-to-8 decoder, and an H12 3-input OR gate. The N122 flip-flop has inputs M04 (CLK), V02 (D), and RES (CL), and a feedback input FDE. Its output Q is connected to the M74 decoder's input K2B. The M74 decoder has three outputs: RES\_SYNC3, RES\_SYNC, and RES\_SYNC2. The H12 OR gate has three inputs: RES\_SYNC3, RES\_SYNC, and RES\_SYNC2. The output of the H12 OR gate is connected to the RES input of the N122 flip-flop, forming a feedback loop.

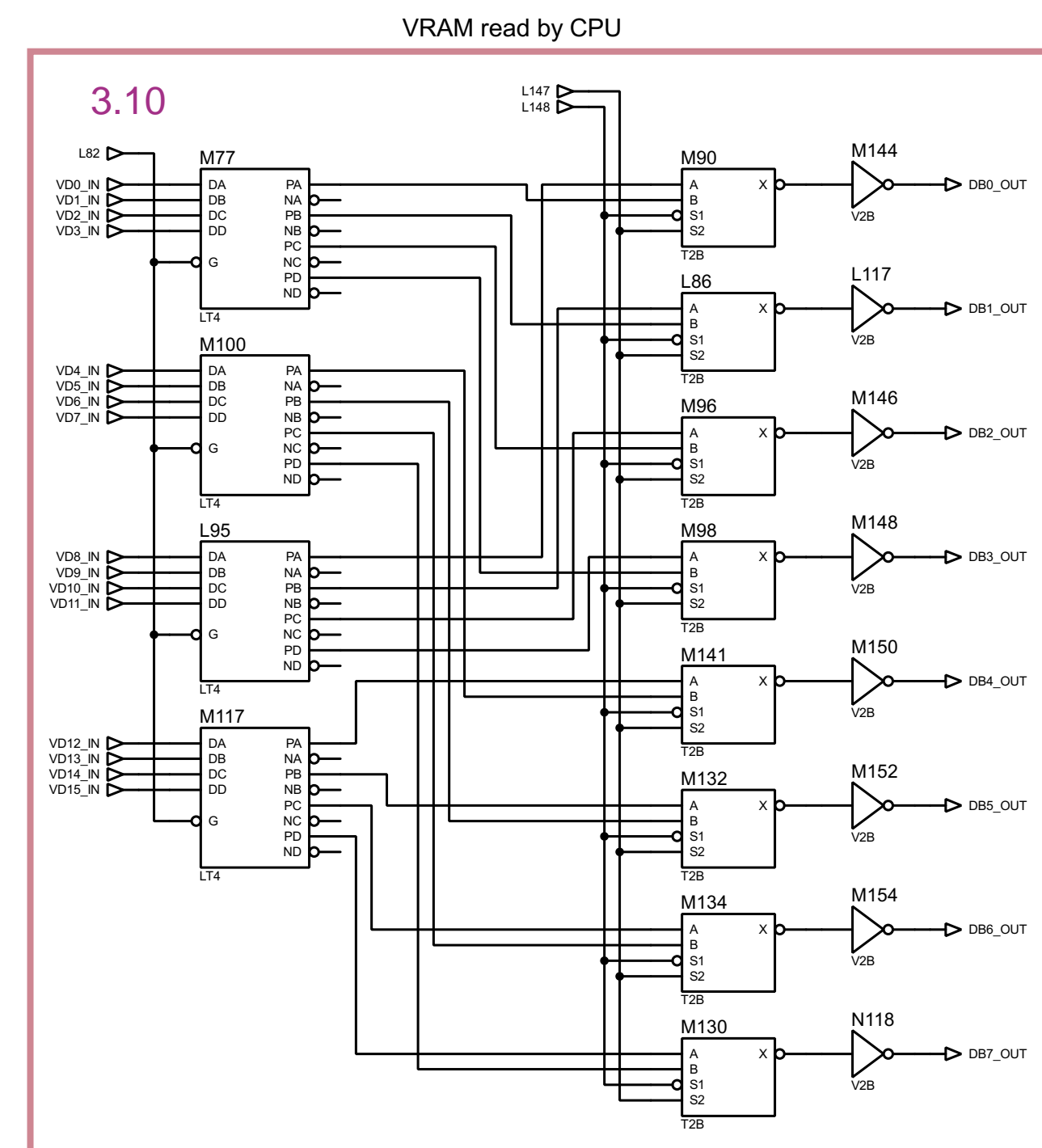
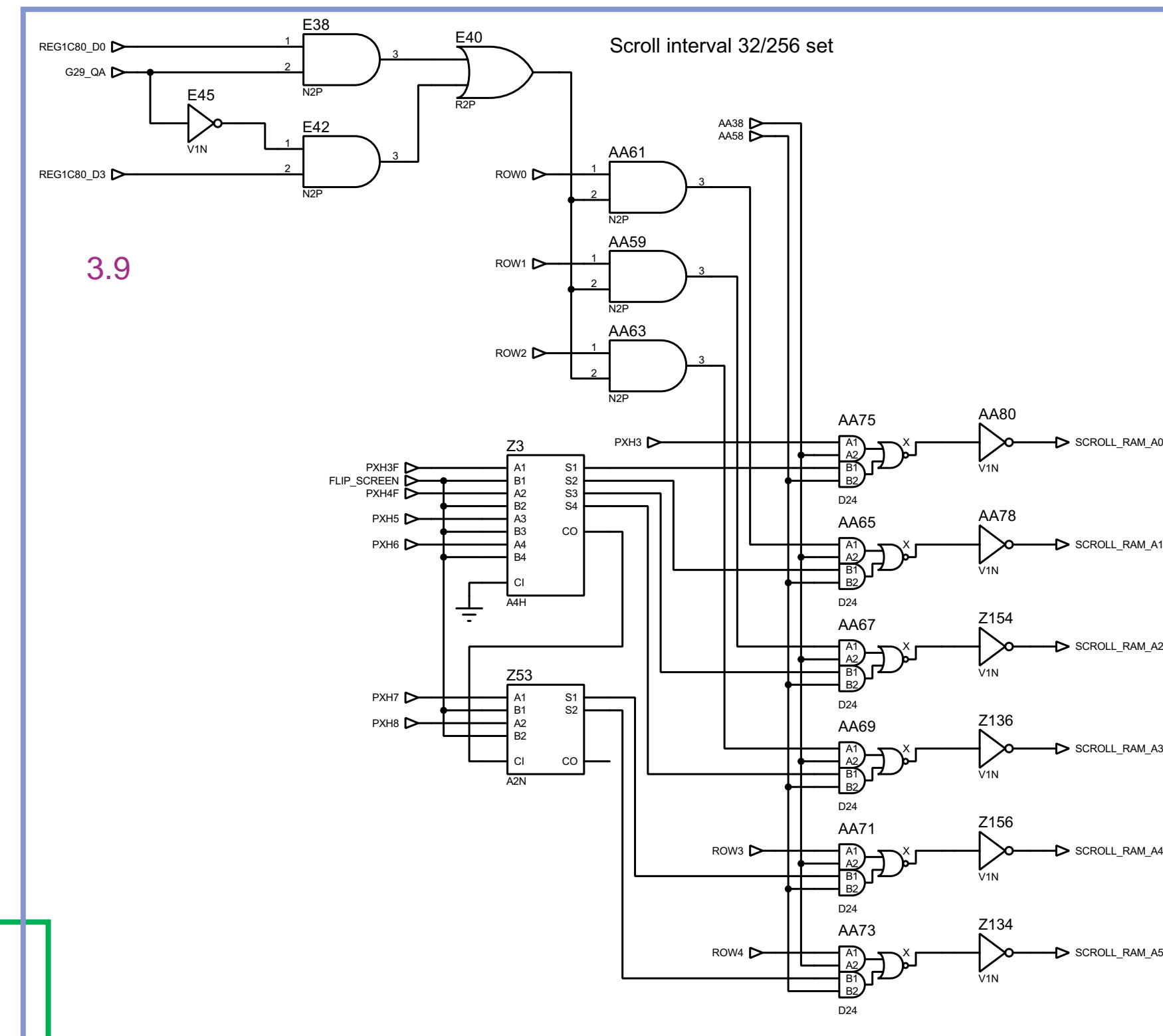
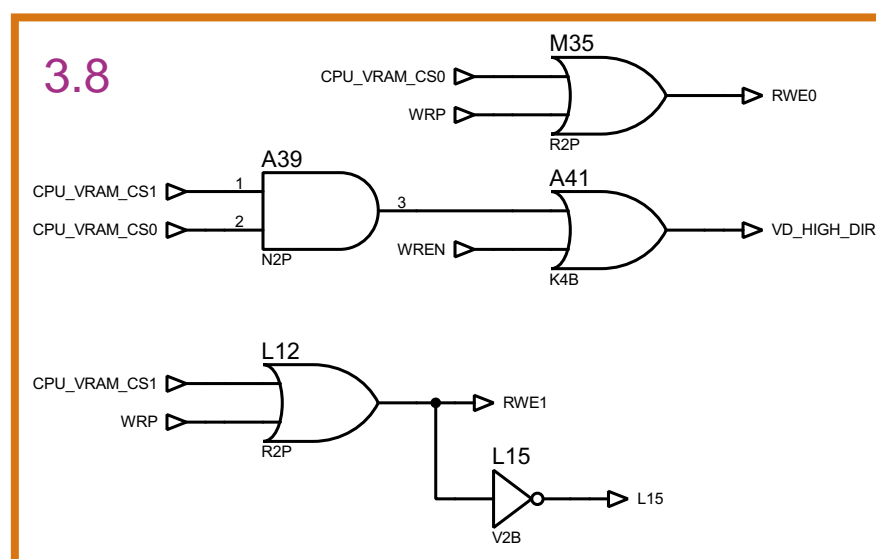
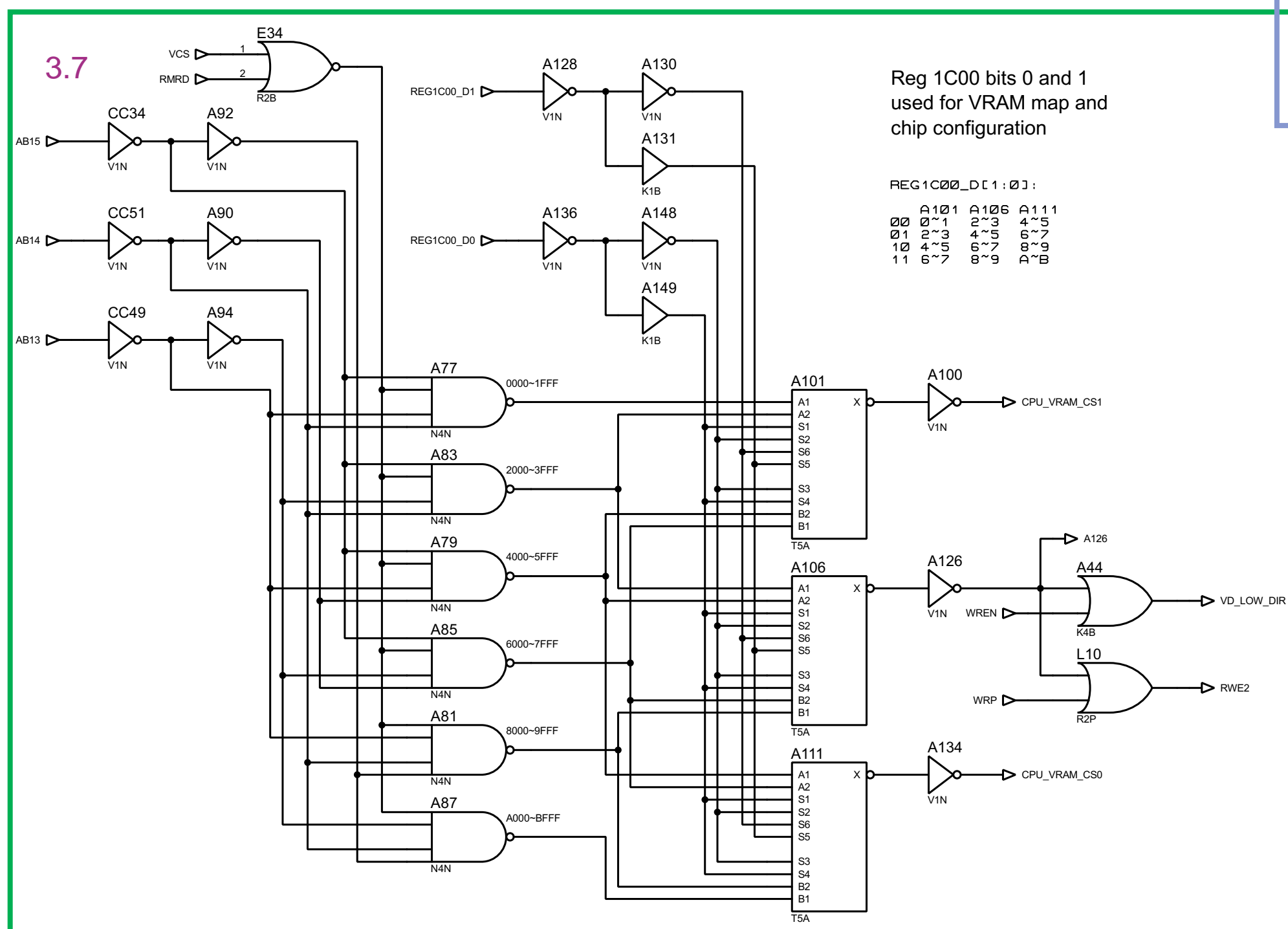
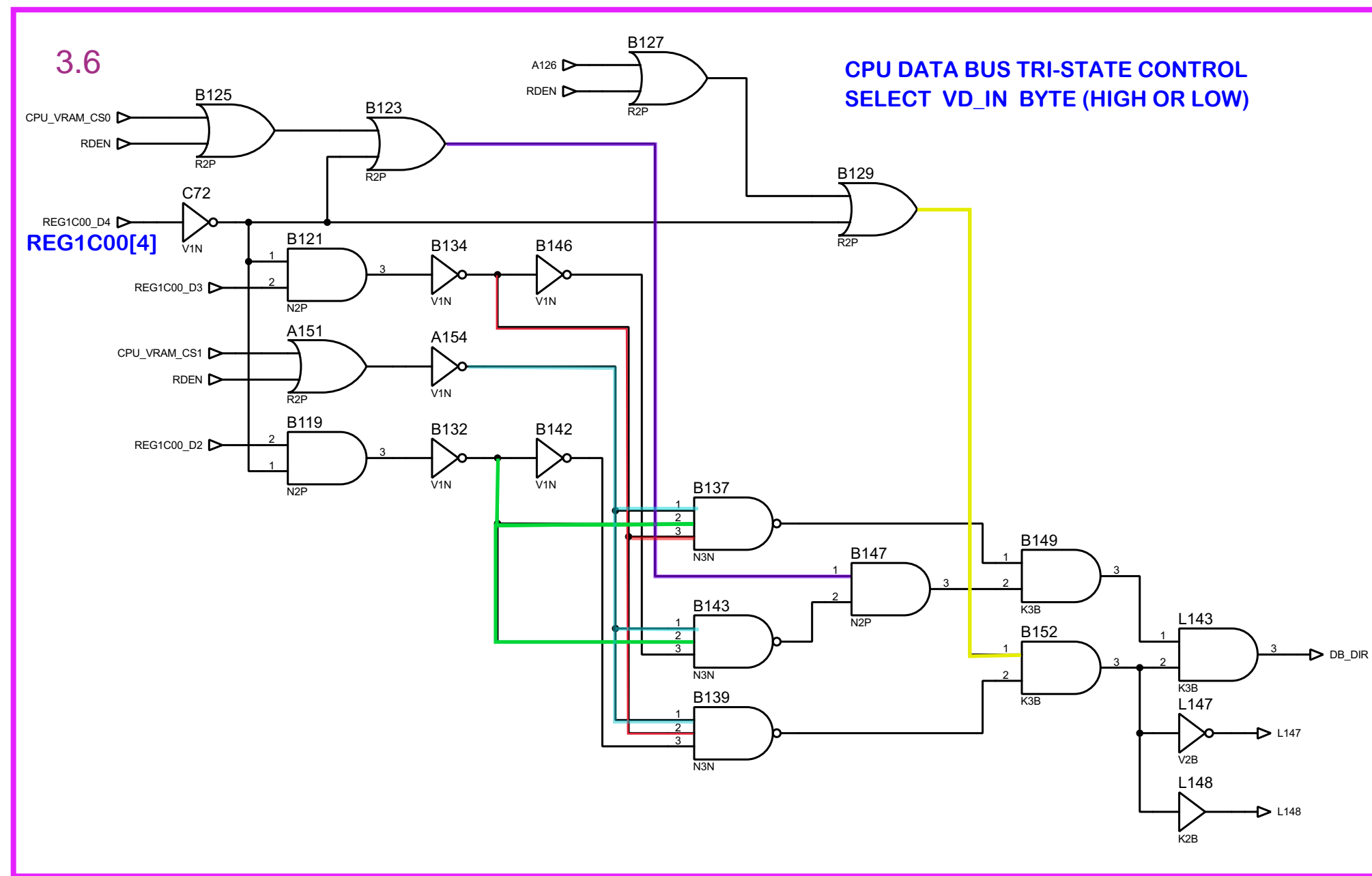


### 3.4 ✓

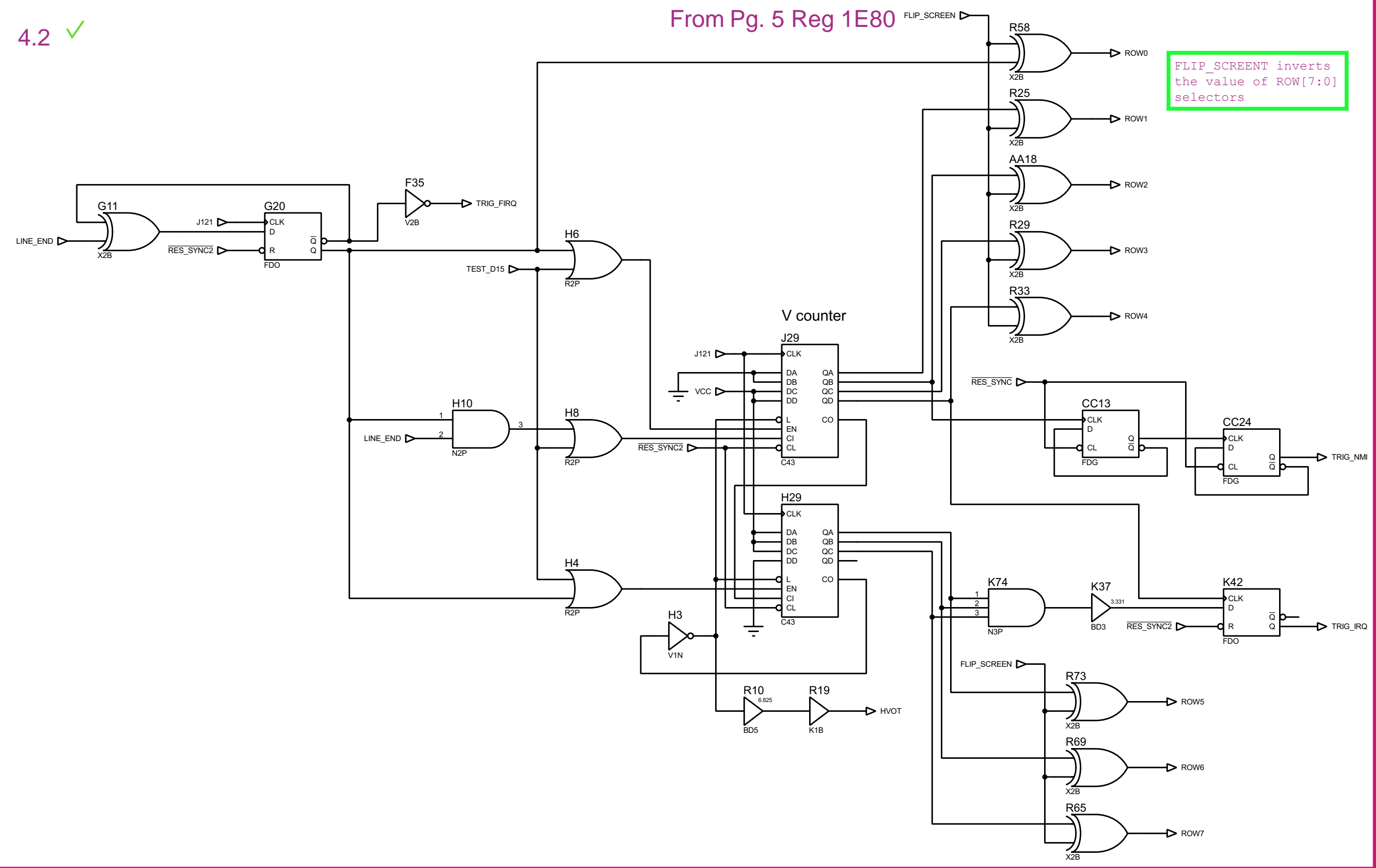
The diagram illustrates a 10-bit bus system. It consists of 10 input signals (DB0\_IN to DB7\_IN) and 10 output signals (DB0\_BUF to DB7\_BUF). Each input signal is connected to a buffer (N135 to N103) and an inverter (K2B). The output of each buffer is connected to the input of the corresponding inverter, and the output of each inverter is connected to the output signal. The buffers are labeled N135, N80, N132, N77, N83, N97, N100, and N103. The inverters are labeled K2B.



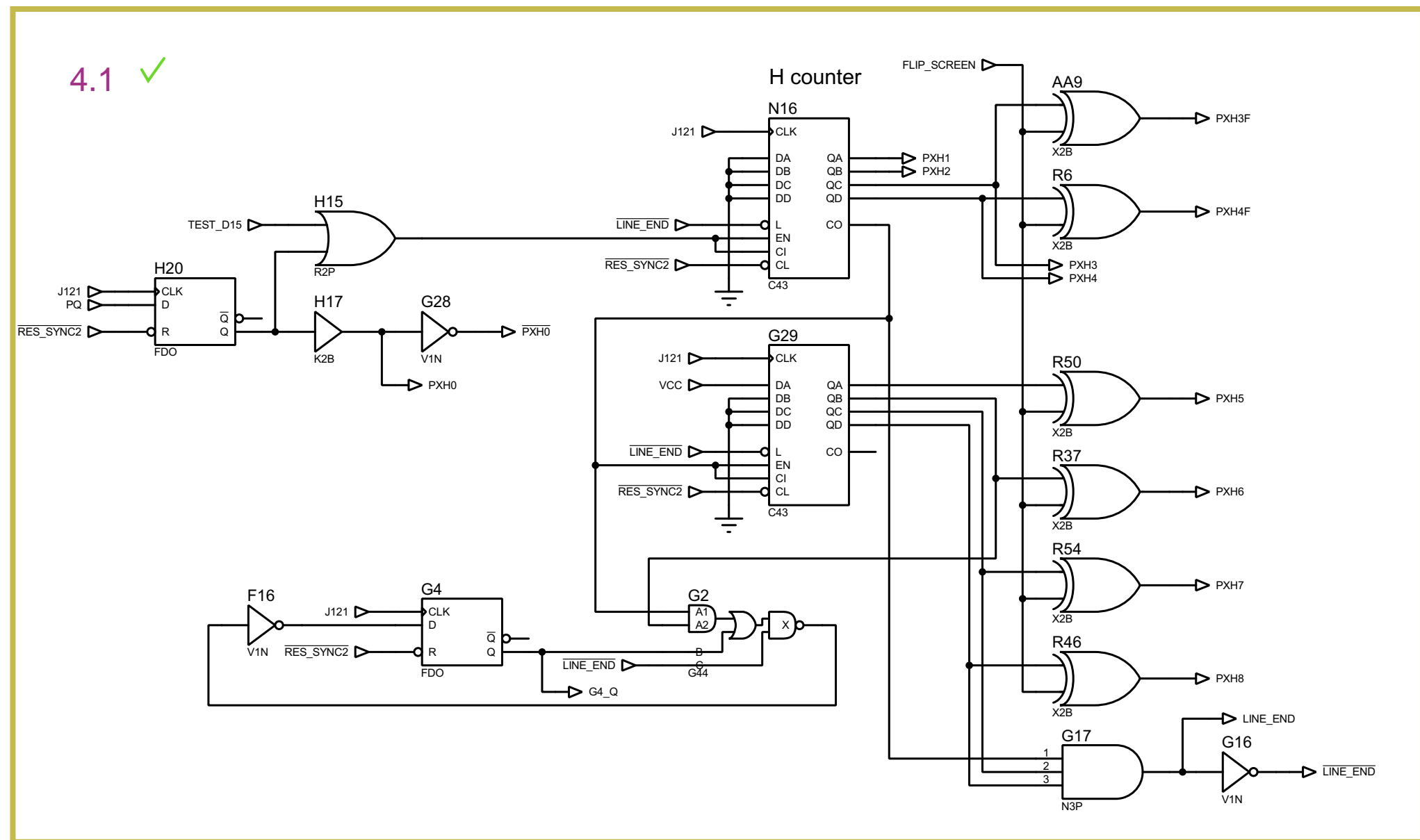
```
wire [7:0] DB_BUF
```



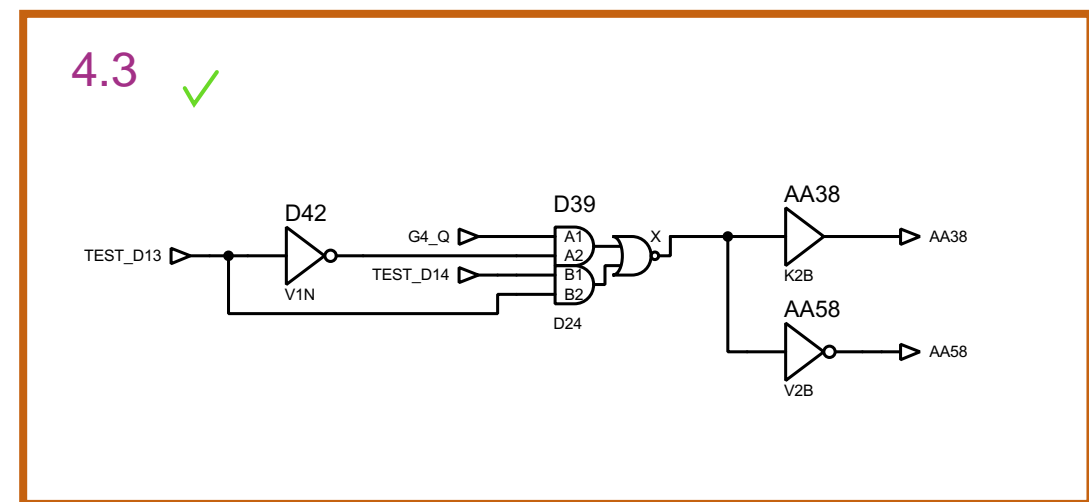
4.2 ✓



4.1 ✓

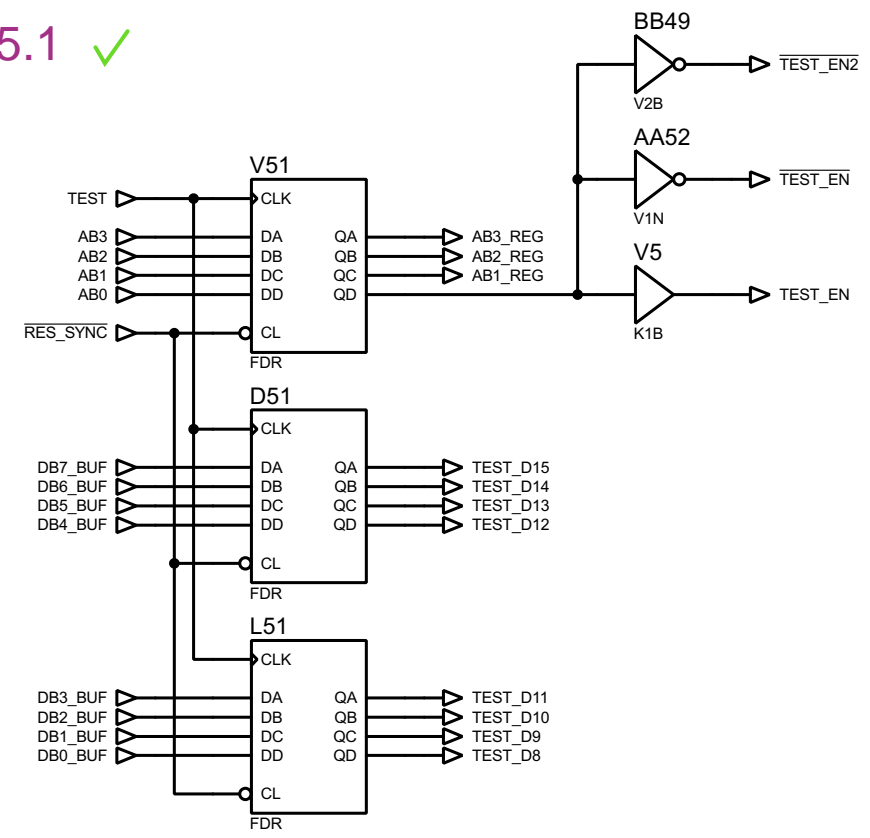


4.3 ✓

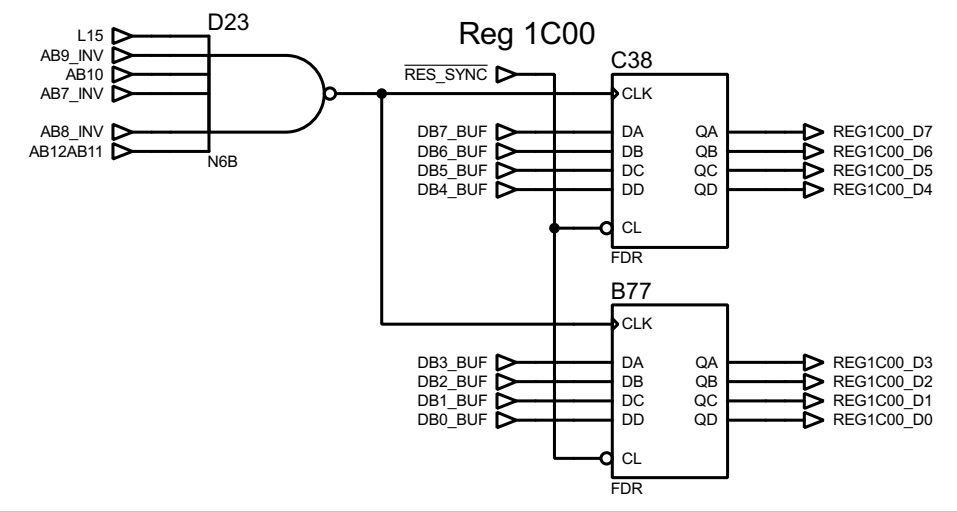




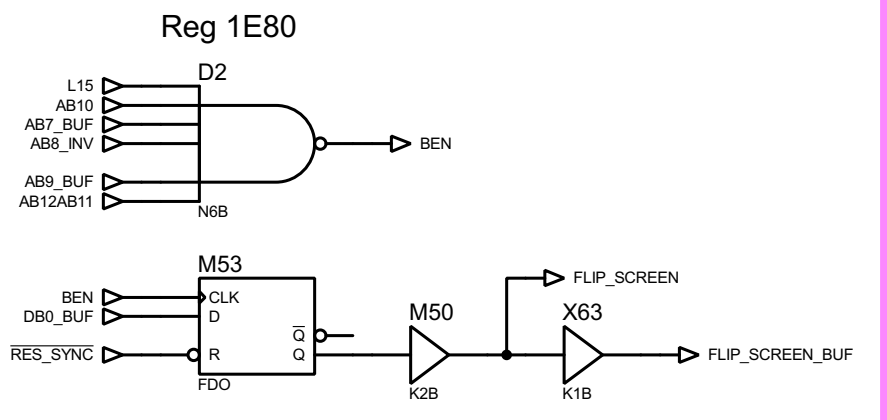
5.1 ✓



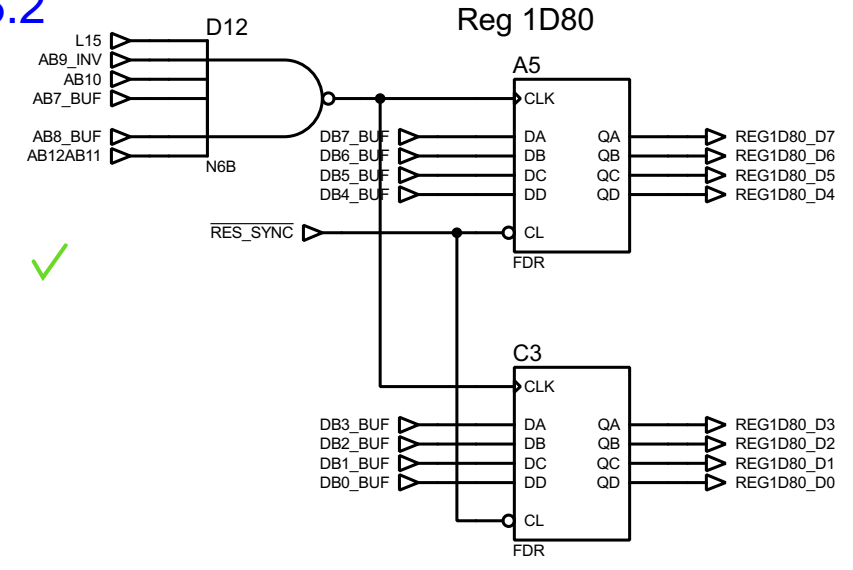
5.4 ✓



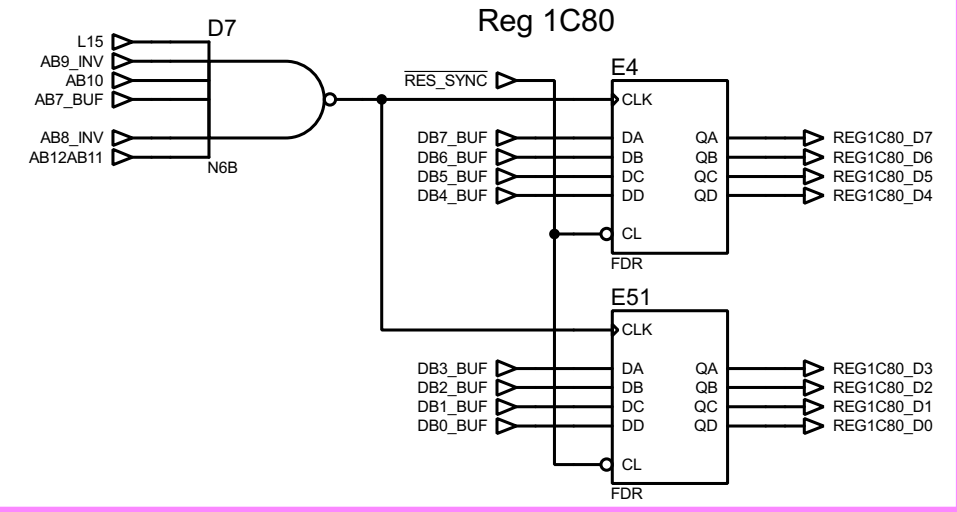
5.7 ✓



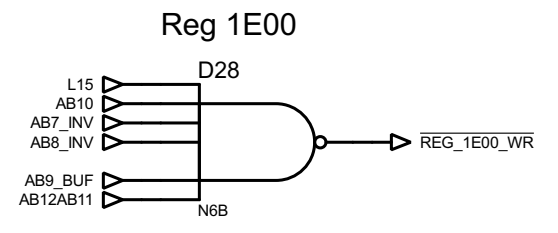
5.2 ✓



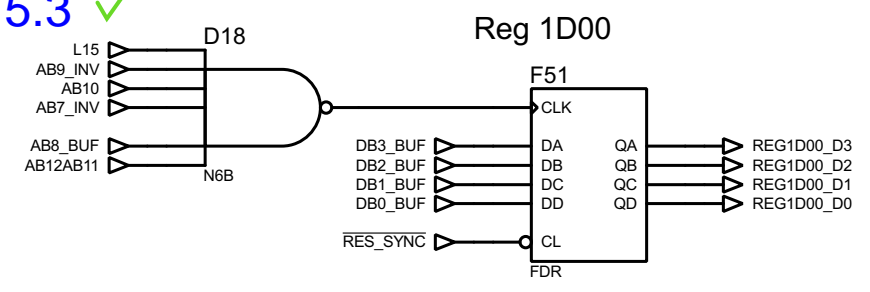
5.5 ✓



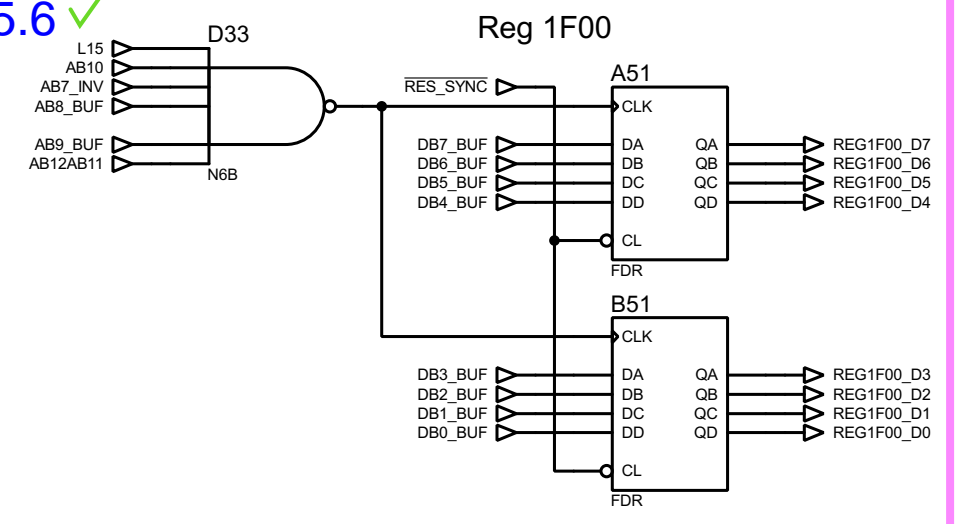
5.8 ✓



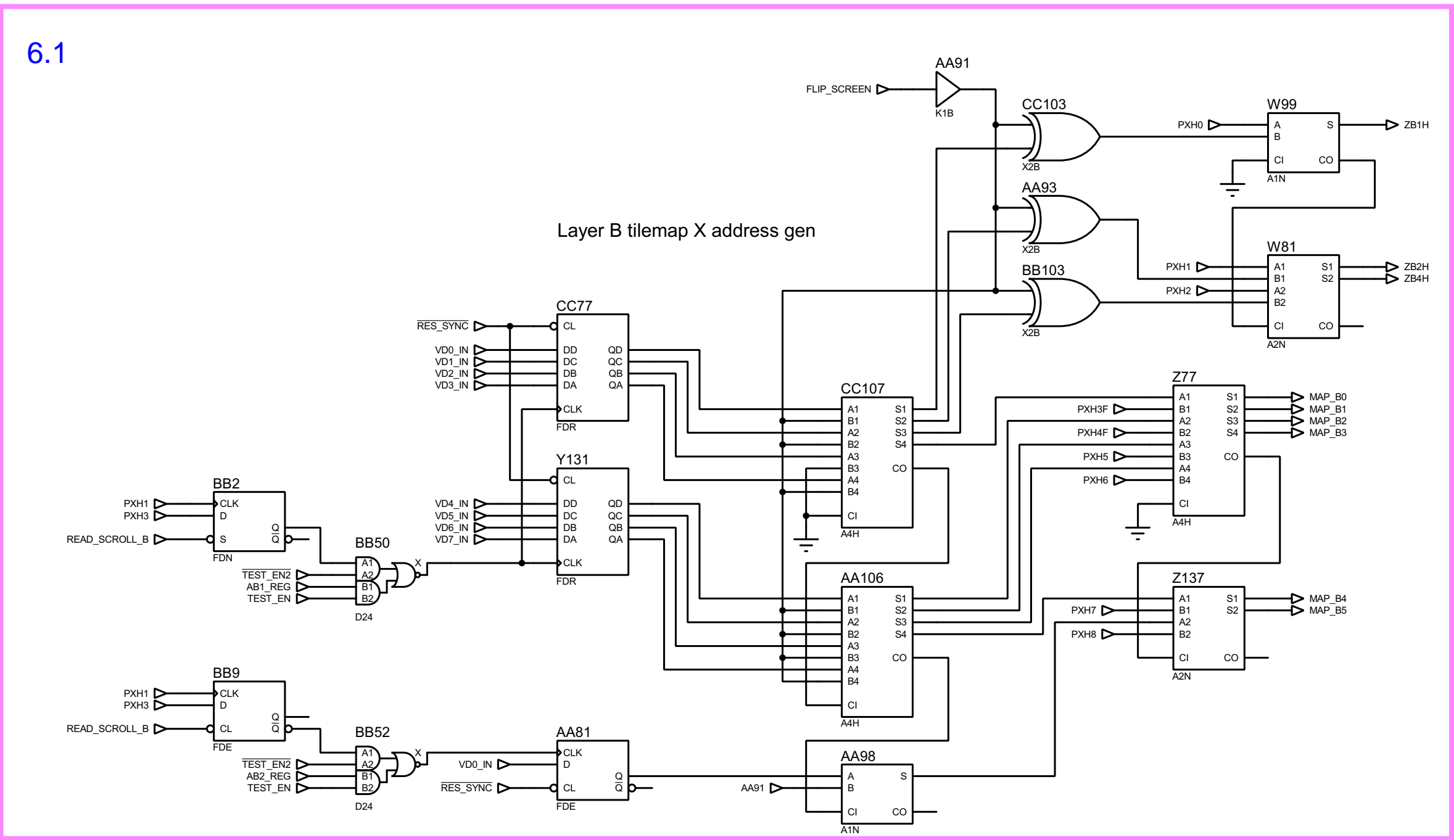
5.3 ✓



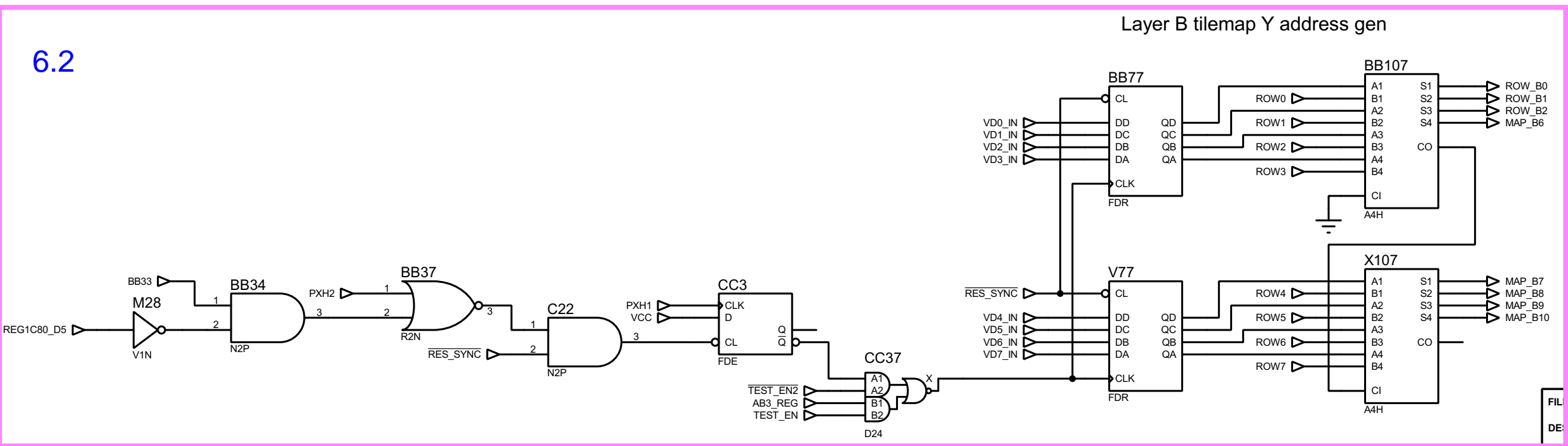
5.6 ✓



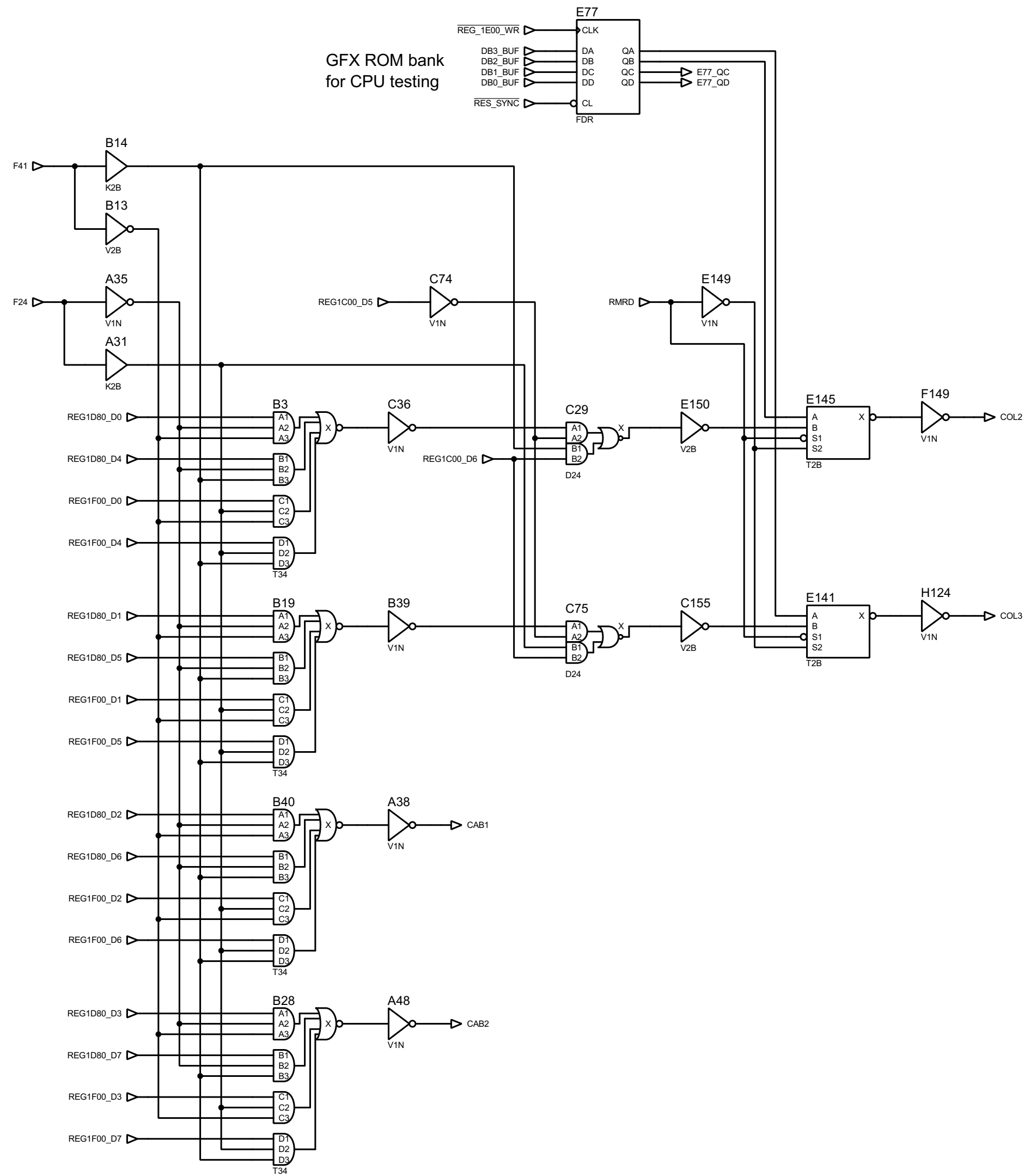
6.1



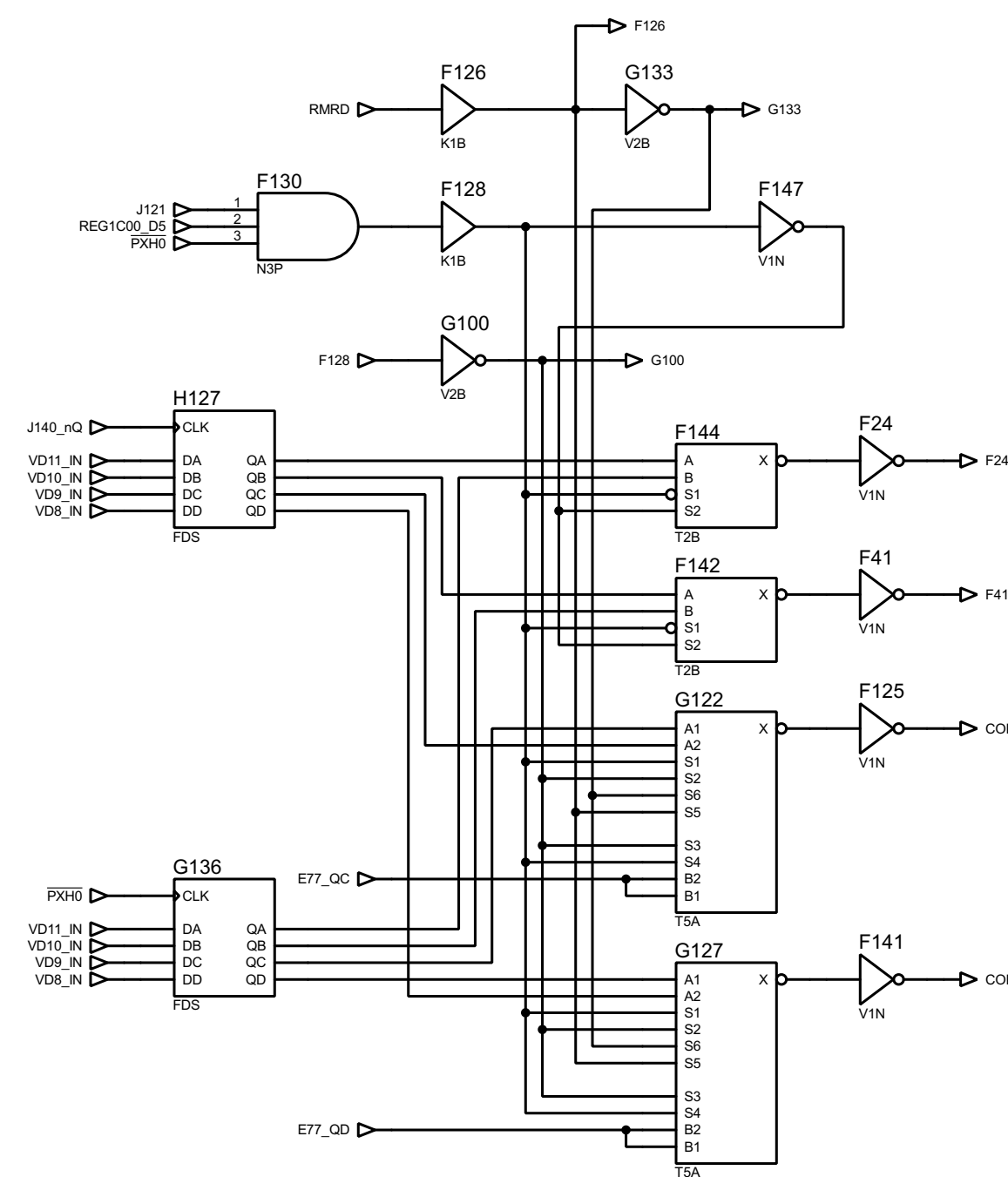
6.2



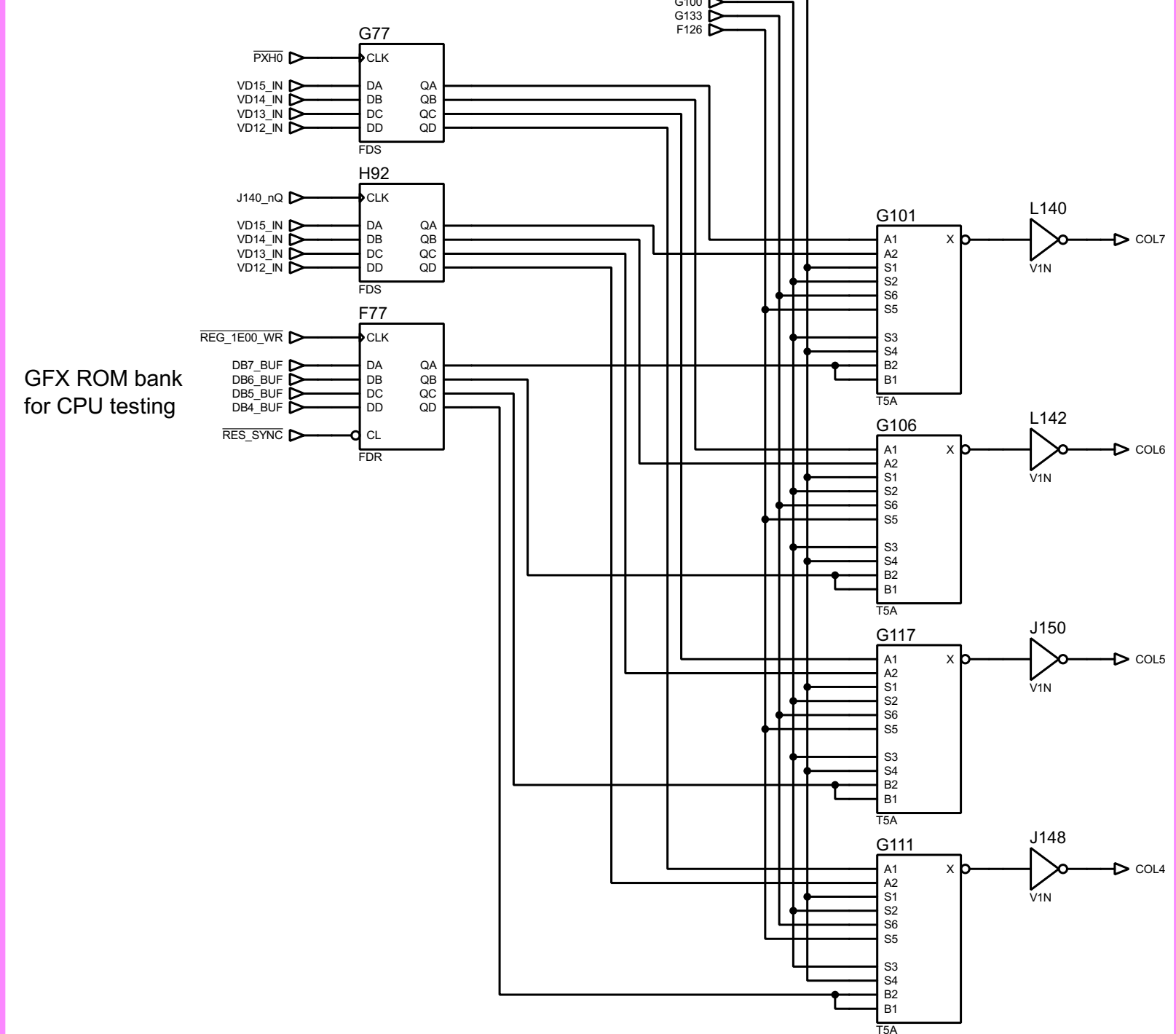
## 7.1



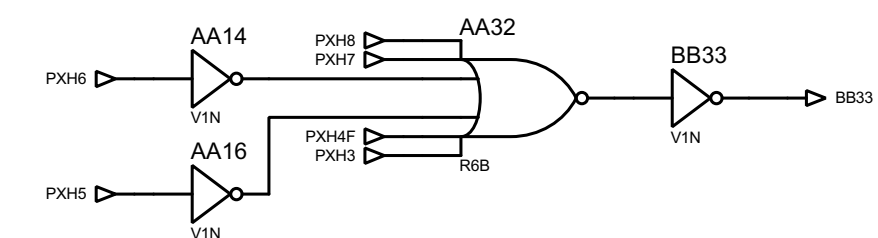
## 7.2



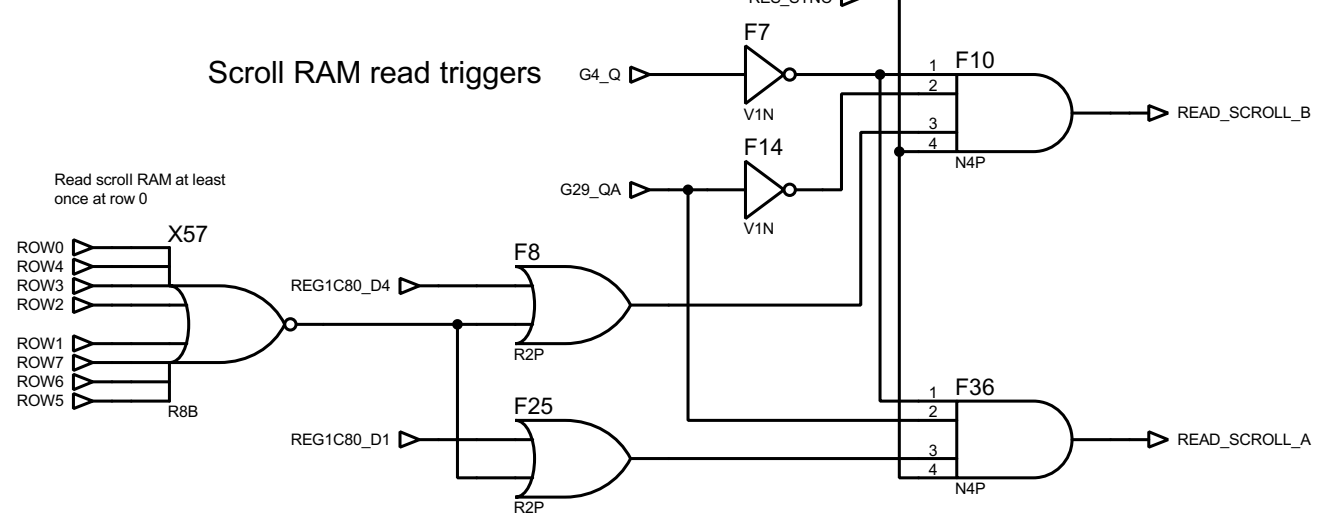
## 7.3



## 7.4

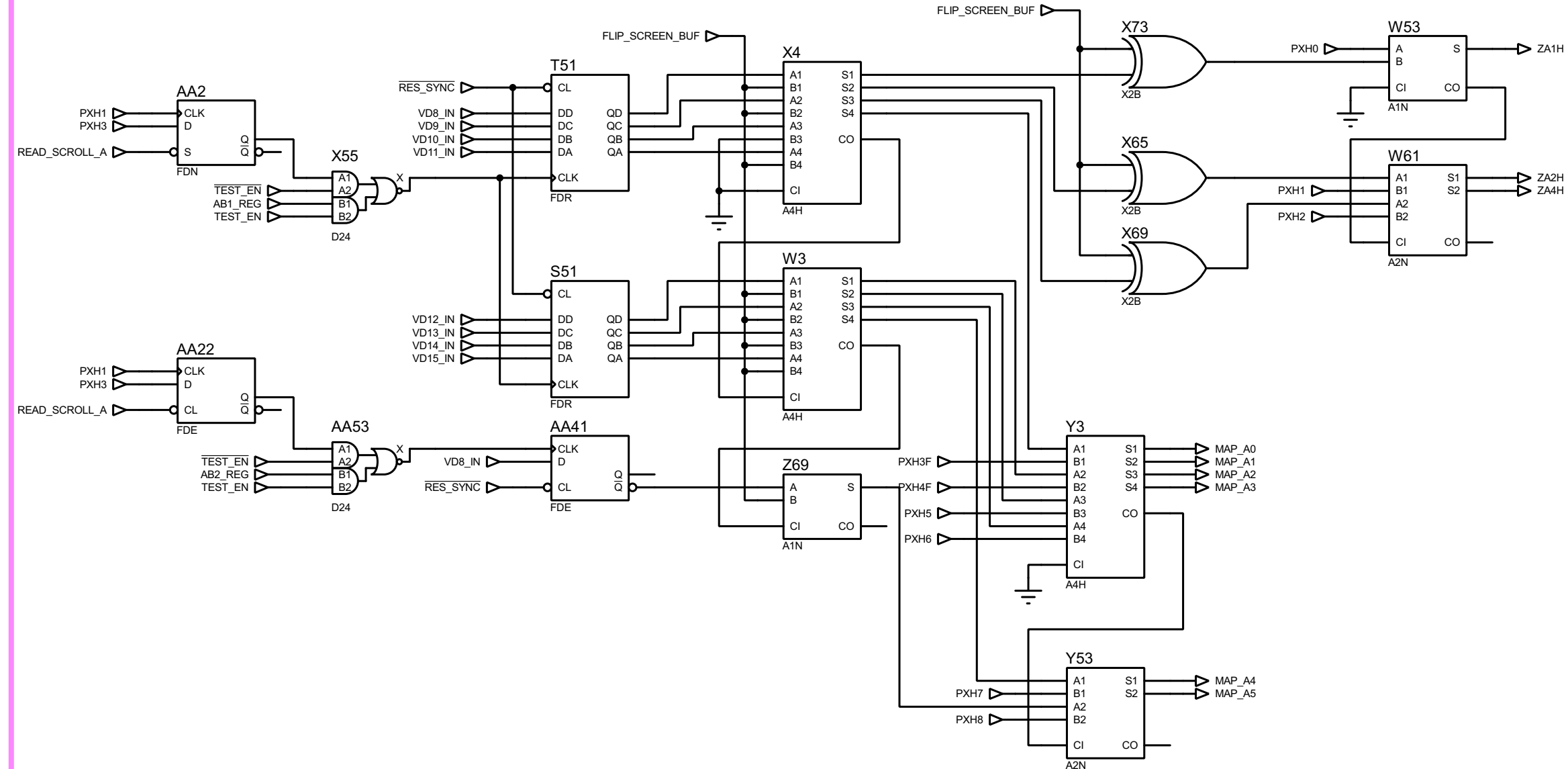


## 7.5



## 8.1

### Layer A tilemap X address gen



## 8.2

### Layer A tilemap Y address gen

