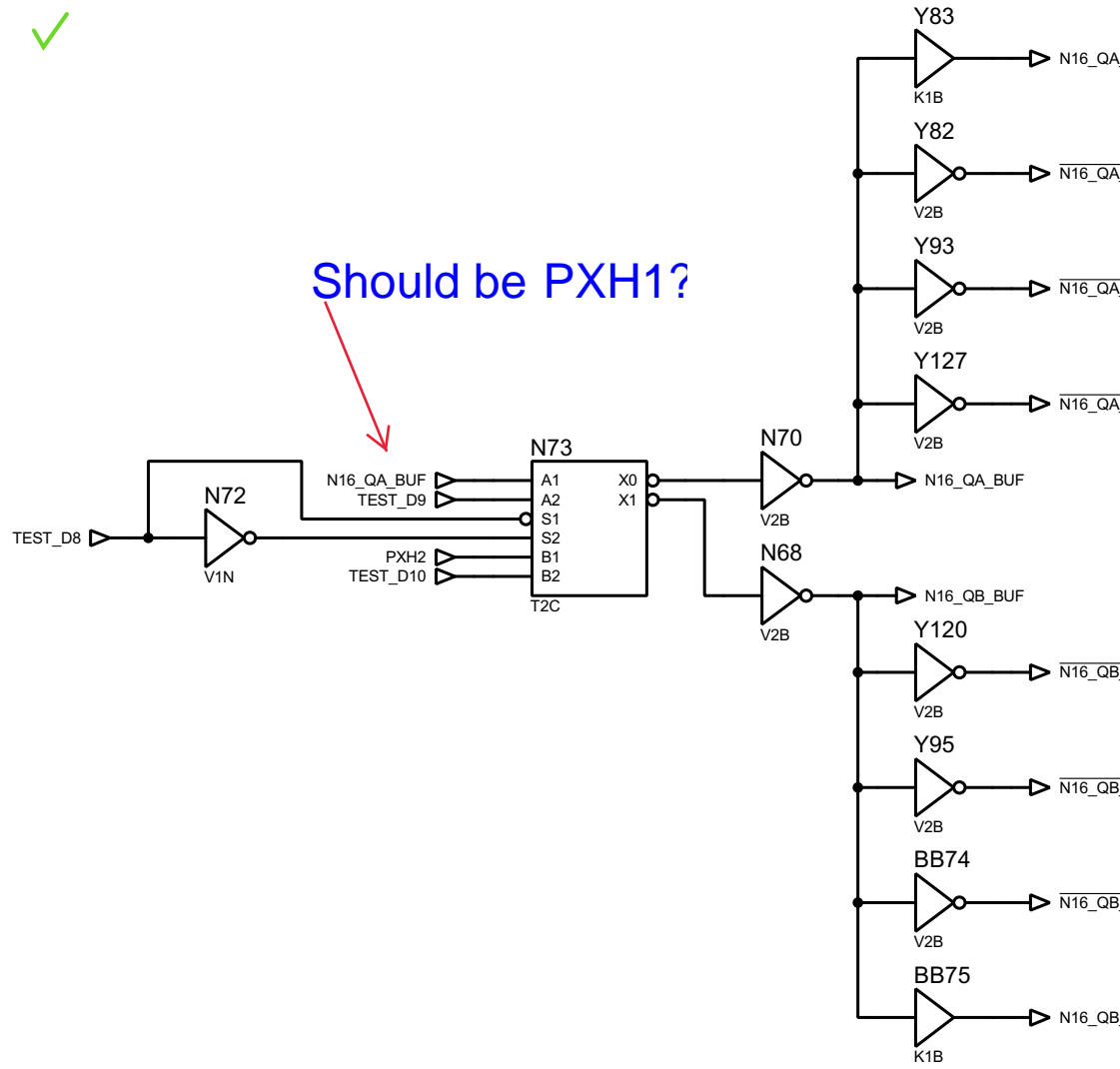
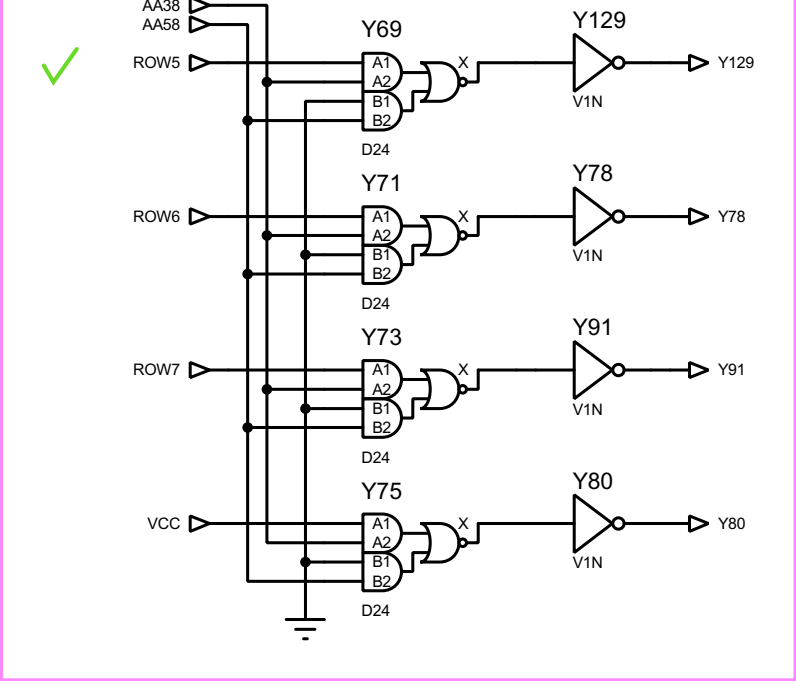


```
VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 00xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 1100 xxxx xxxx A Y scroll
0000 1101 xxxx xxxx A X scroll
0001 00xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 1100 xxxx xxxx B Y scroll
0001 1101 xxxx xxxx B X scroll
          x xxxx x Tilemaps X
xx xxx  Tilemaps Y
```



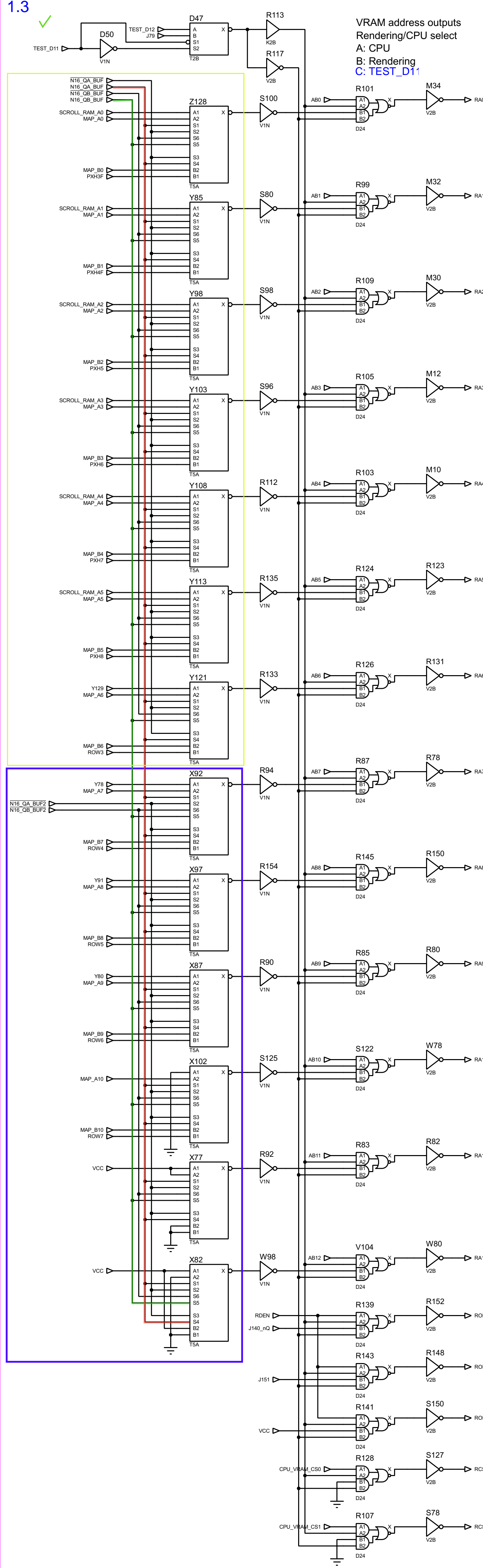
TEST_D13 Addresses Selector

1.2 From 4.3



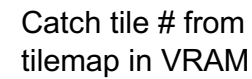
Selection can be simplified using AA38 (and AA38n) only, AA58 always selects 1'b0.

1.3



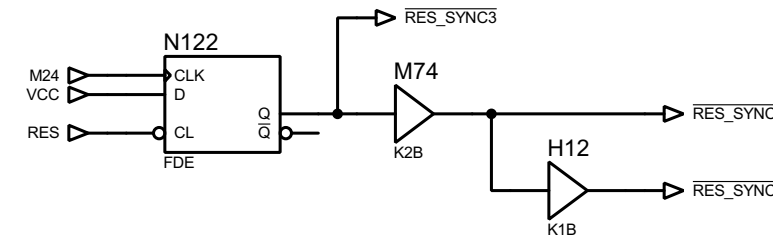


SKIP because AB[1:0] used to select byte



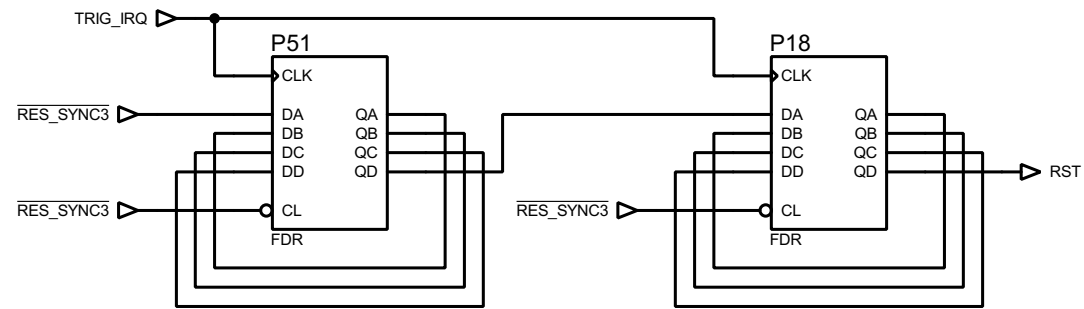
RES_SYNC signals generator

3.1 ✓

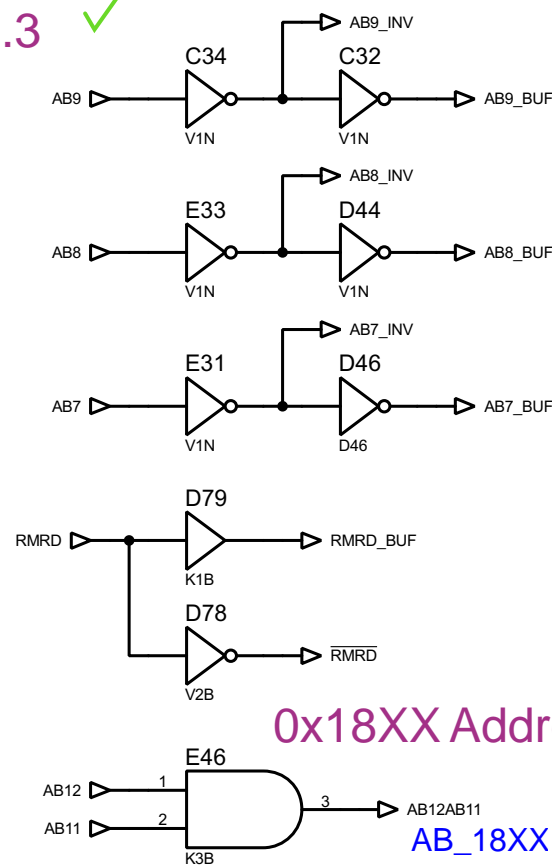


3.2 ✓

8-frame delay for
RES -> RST
Same in k051962 ?



3.3 ✓

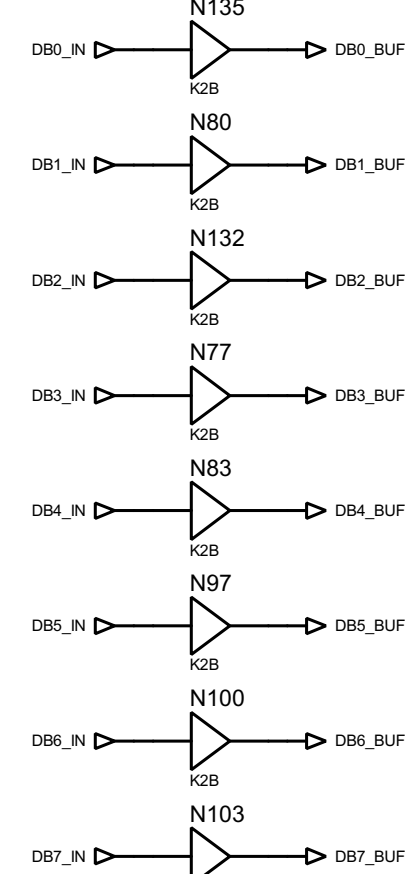


0x18XX Address

AB_18XX

180c-1833: Layer A Y Scroll

3.4 ✓



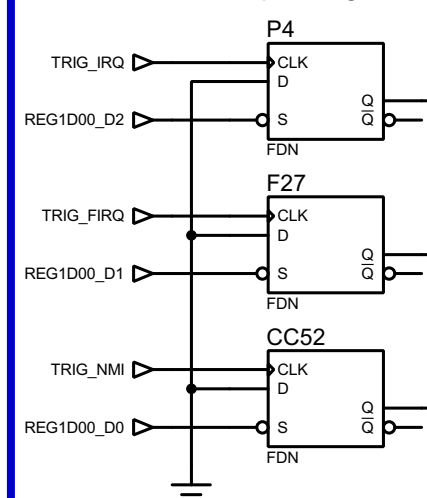
wire [7:0] DB_IN

wire [7:0] DB_BUF

VD_IN
DB_IN
DB_OUT
DB_BUF

3.5 ✓

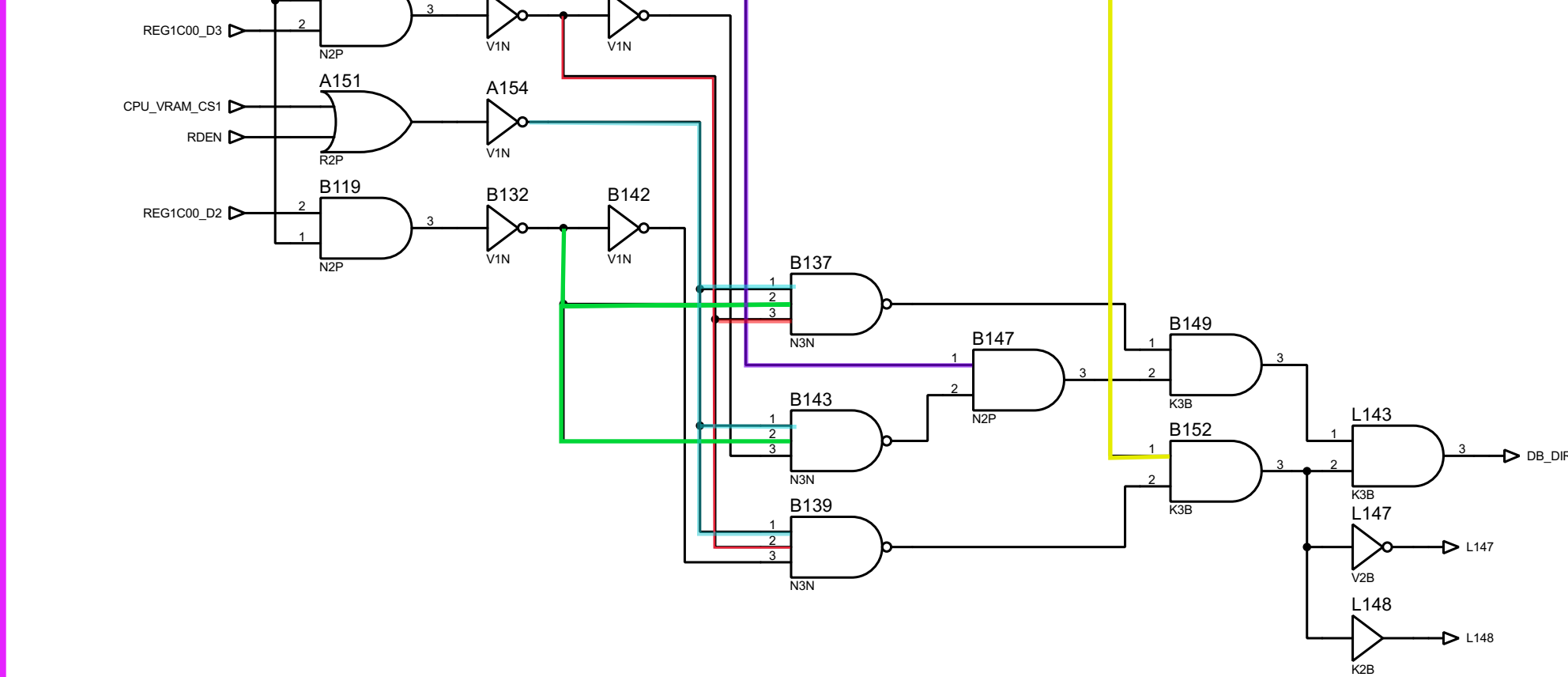
Interrupts flags



3.6 ✓

CPU DATA BUS TRI-STATE CONTROL
SELECT VD_IN BYTE (HIGH OR LOW)

REG1C00[4]



VRAM CONFIG AND CS/RW CONTROL

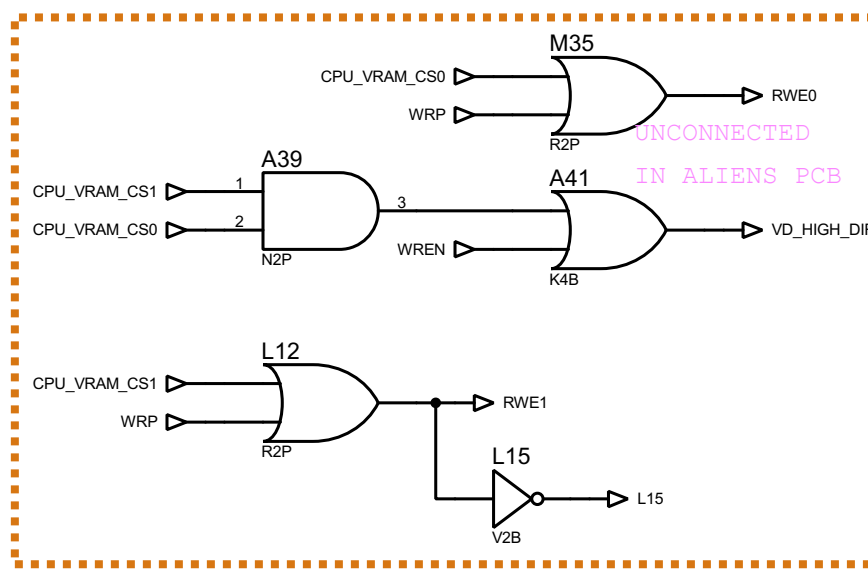
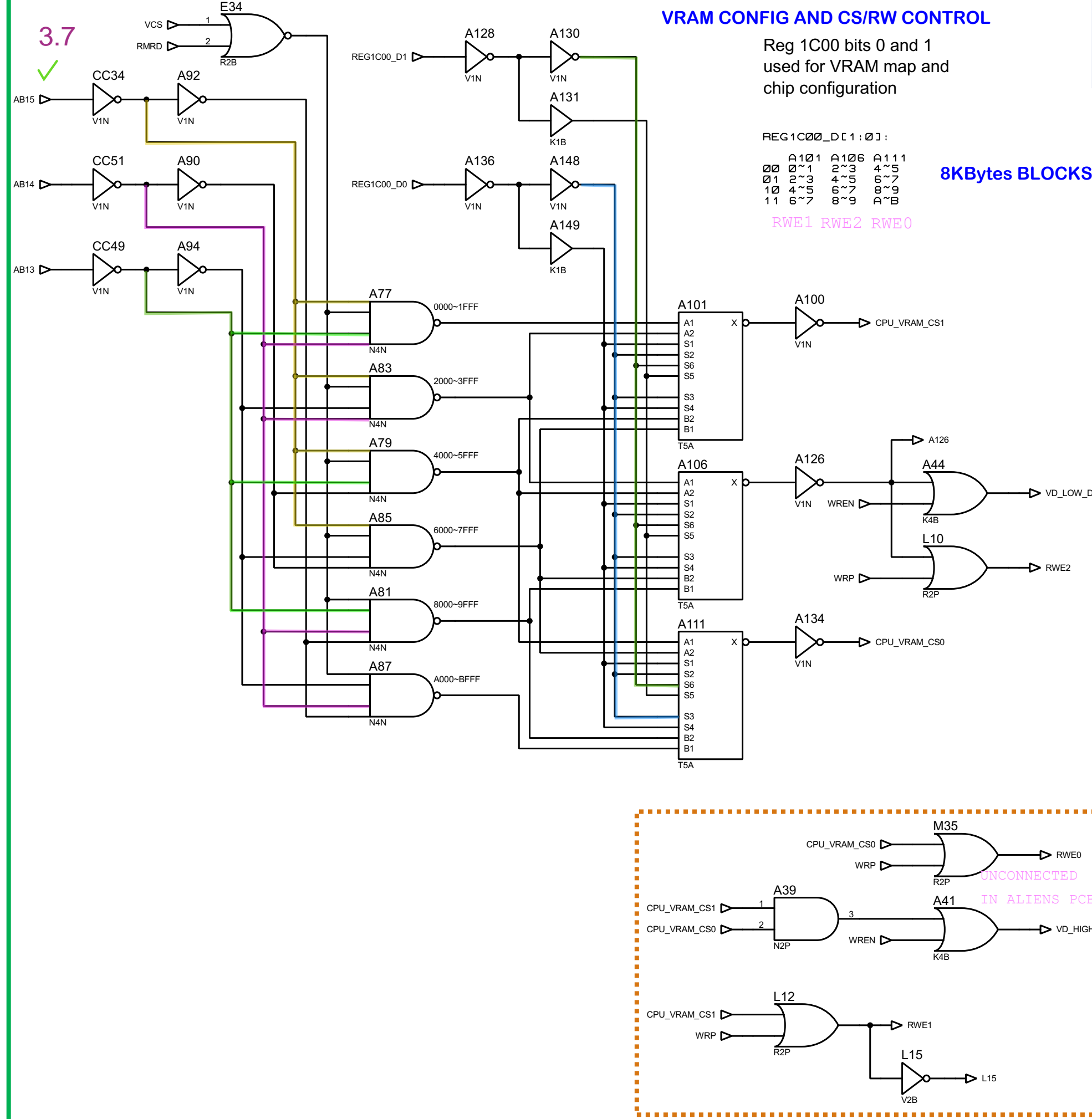
Reg 1C00 bits 0 and 1
used for VRAM map and
chip configuration

REG1C00_D0[1:0] :

00 0~1 2~3 4~5 6~7
01 2~3 4~5 6~7 8~9 A~B
10 4~5 6~7 8~9 A~B
11 6~7 8~9 A~B

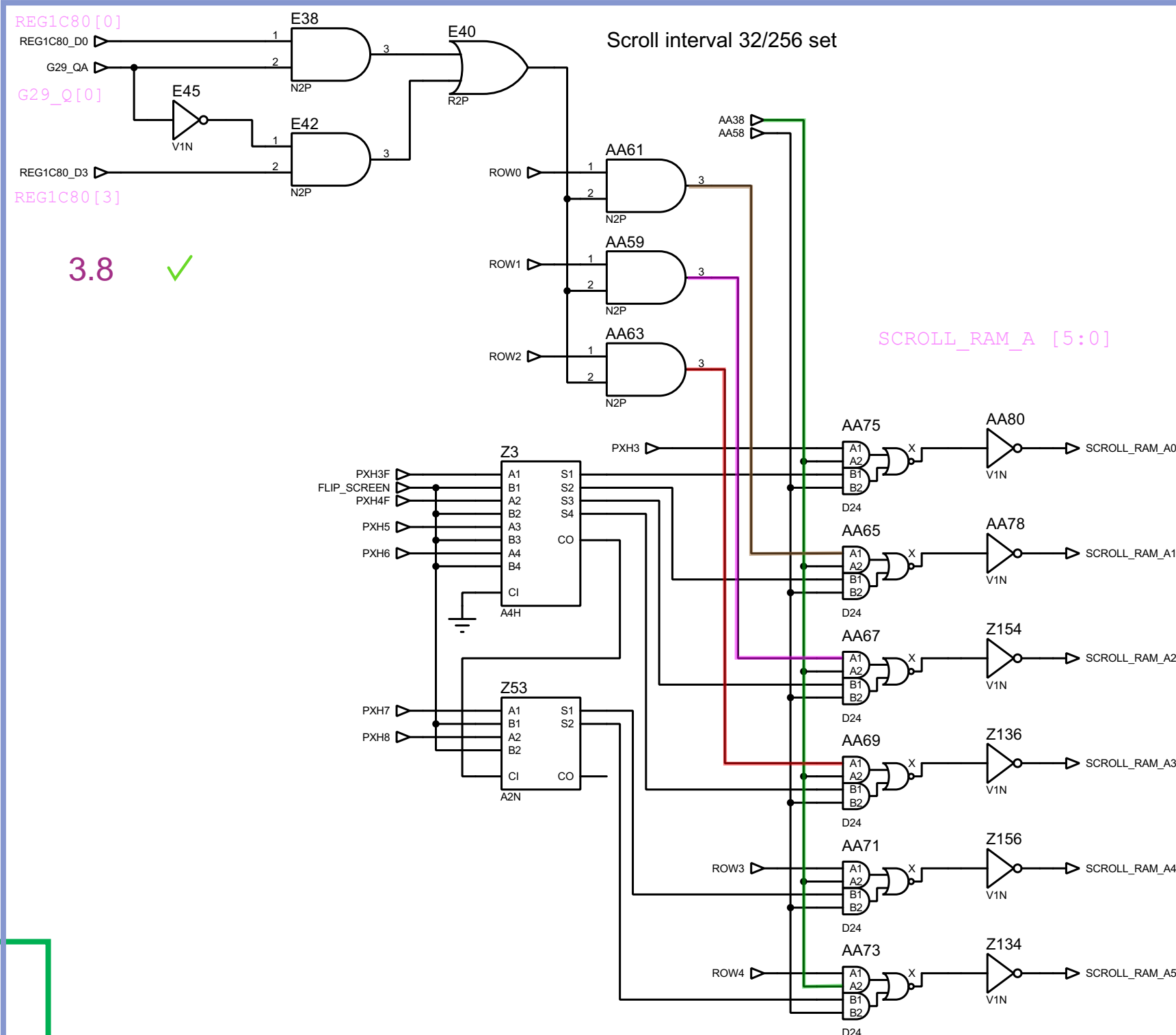
8KBytes BLOCKS

RWE1 RWE2 RWE0



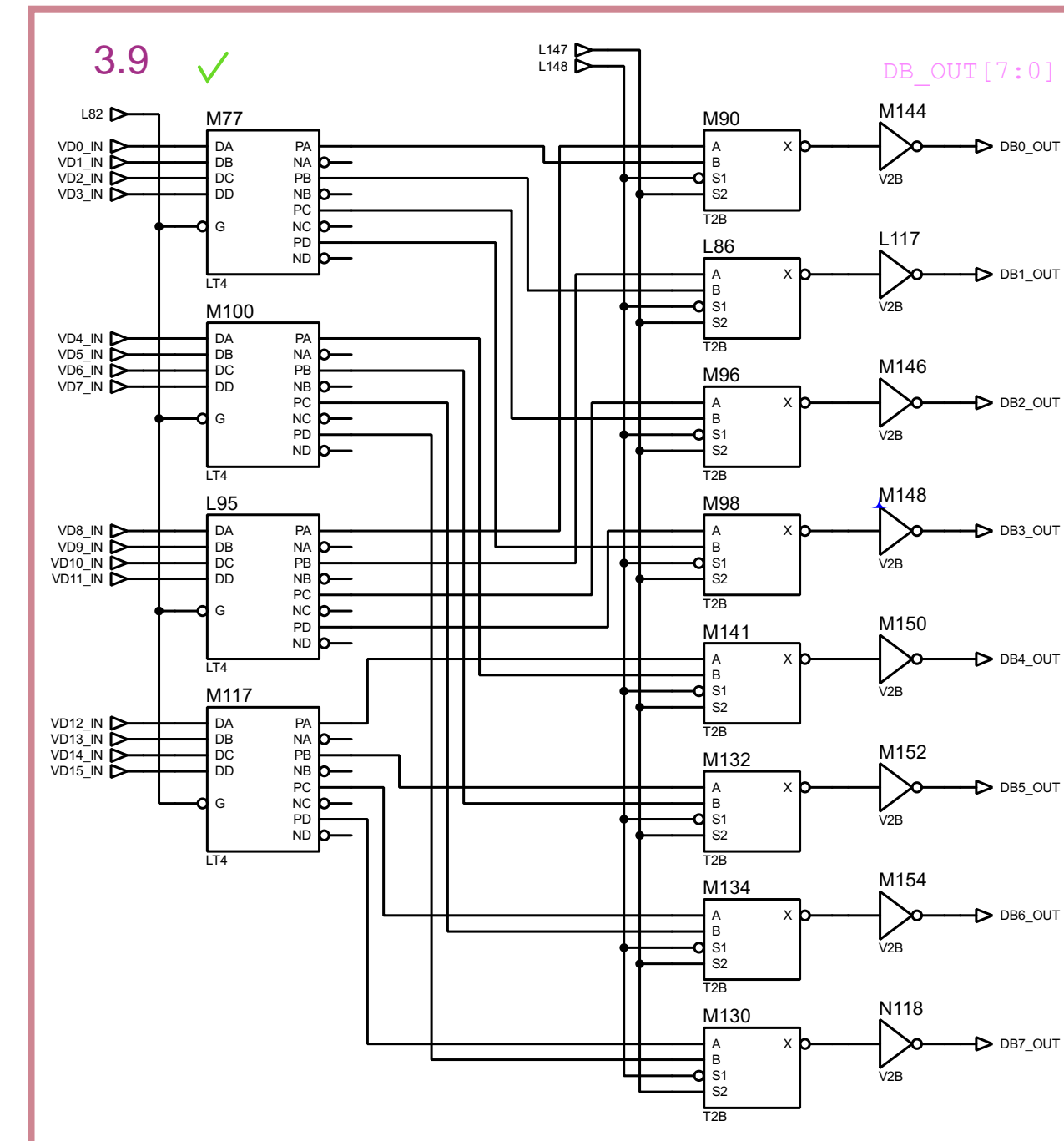
3.8 ✓

Scroll interval 32/256 set



SCROLL_RAM_A [5:0]

VRAM read by CPU



FILE NAME: k052109.pdsprj

DESIGN TITLE: Konami 052109

CPU STUFF

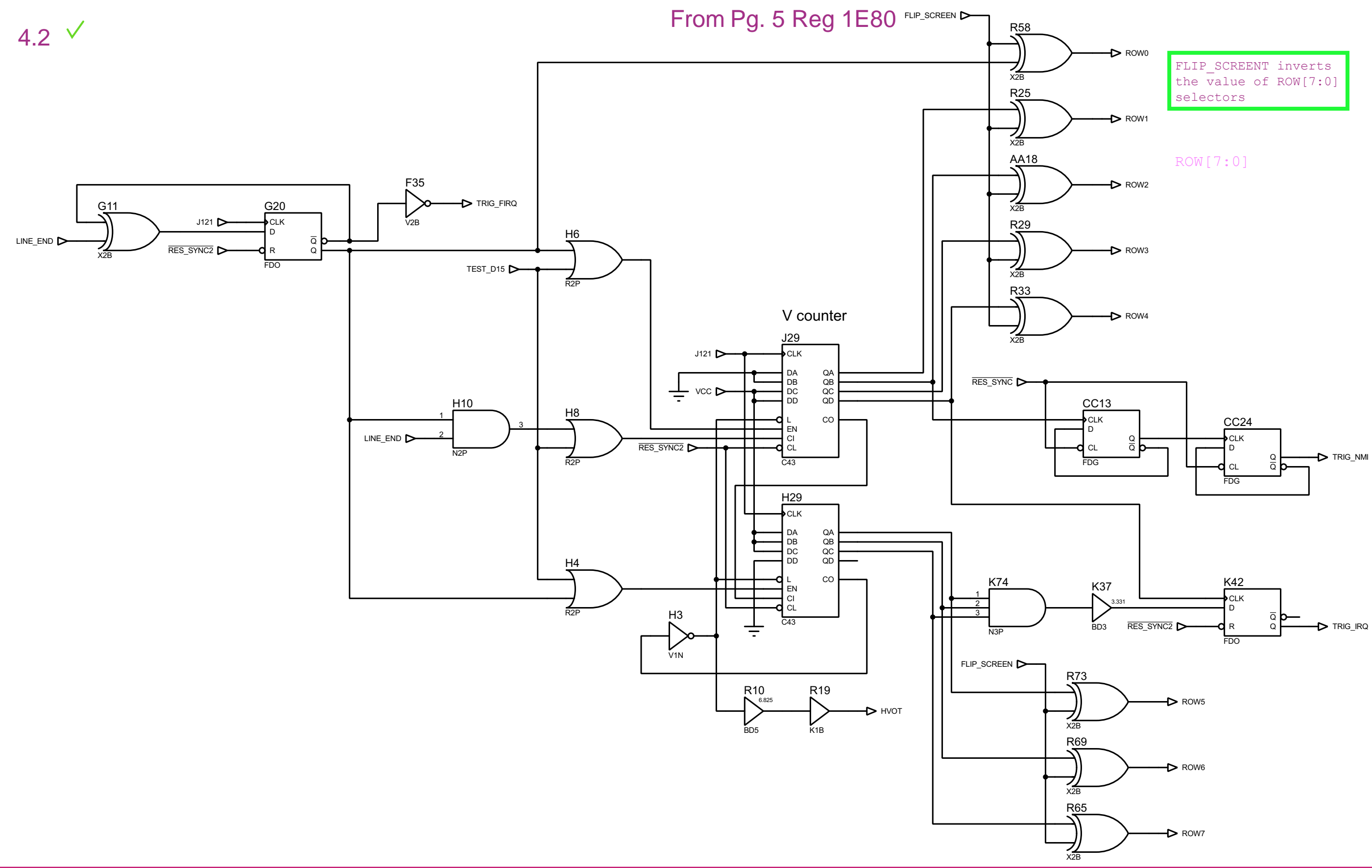
BY: Sean Gonsalves

REV: A

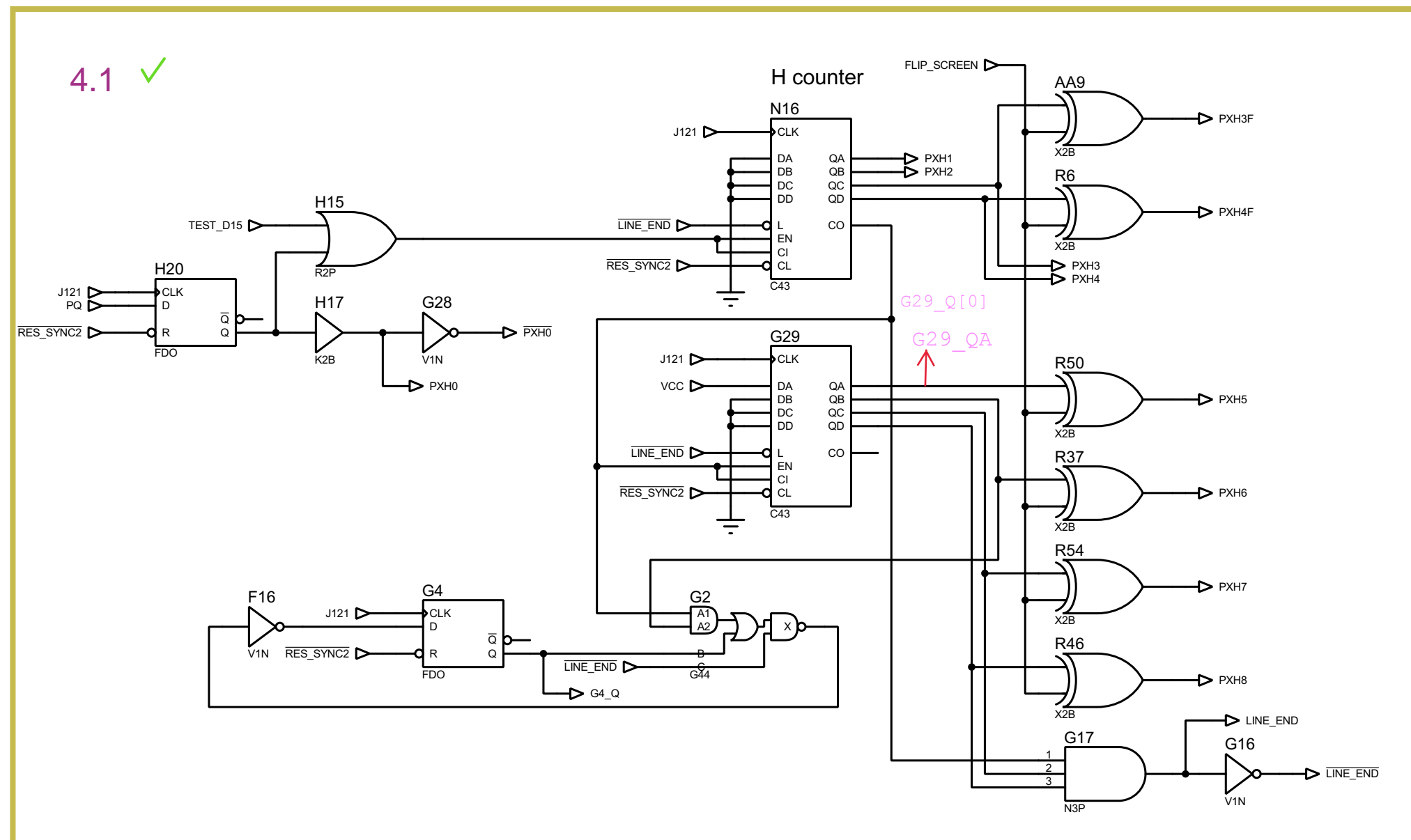
DATE: 22/06/2021

PAGE: 3 of 8

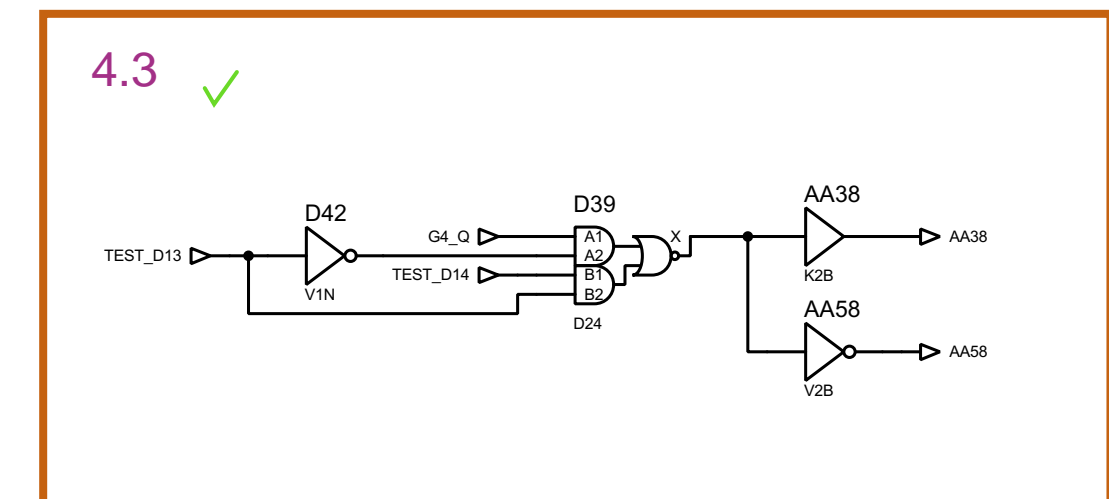
4.2 ✓



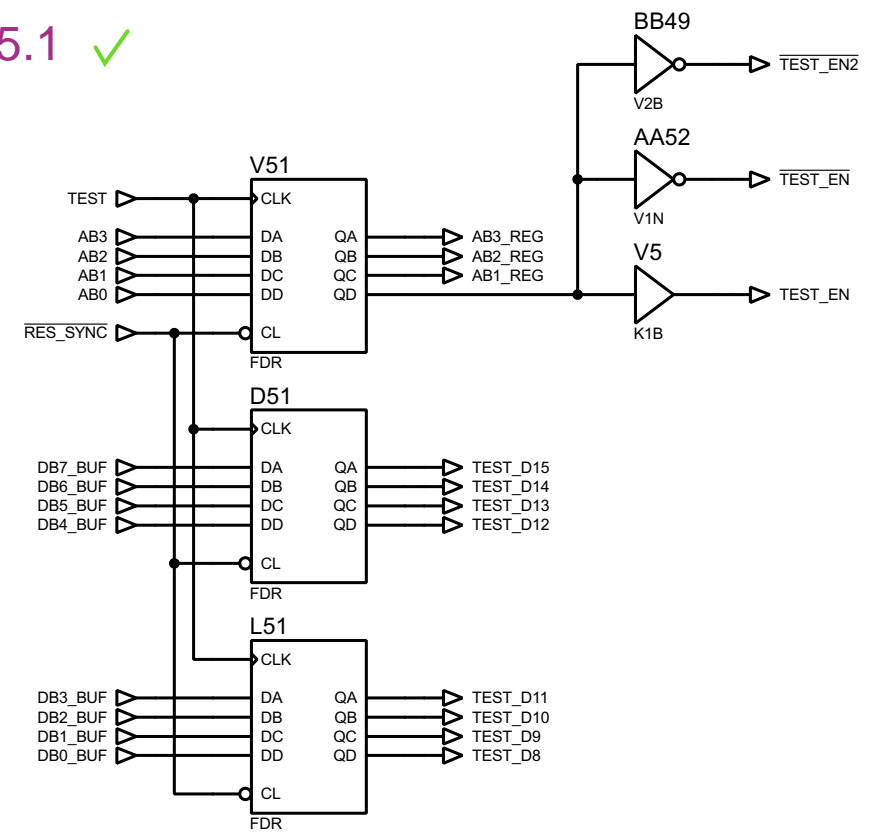
4.1 ✓



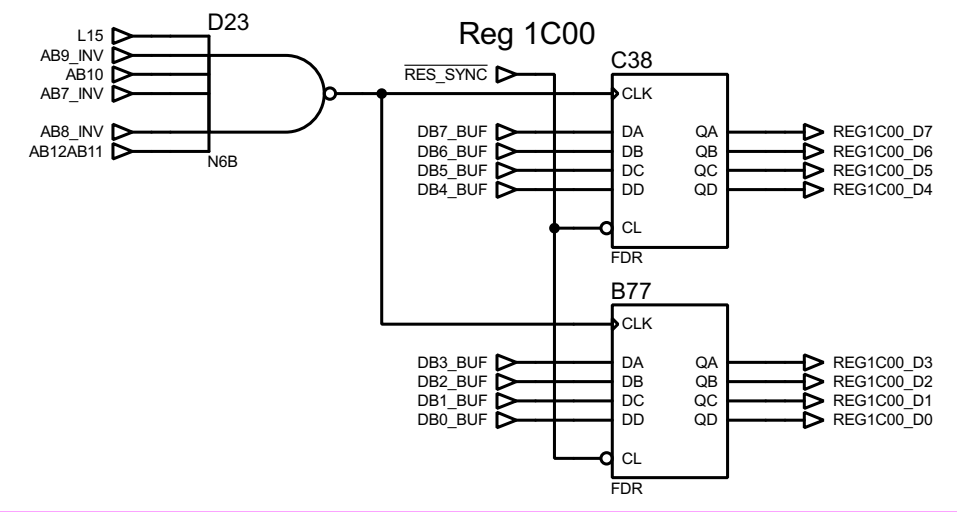
4.3 ✓



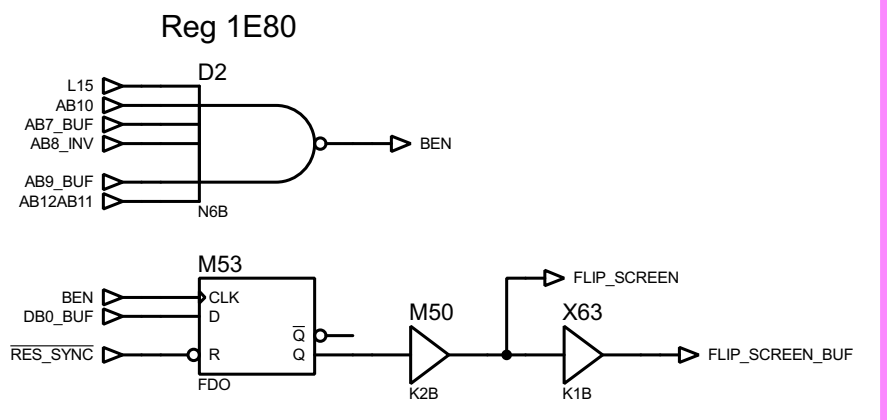
5.1 ✓



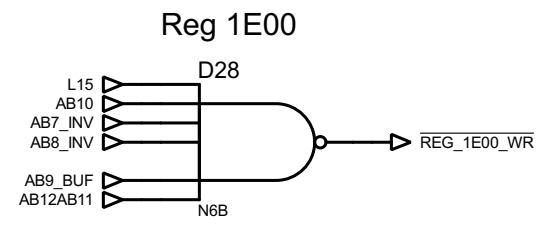
5.4 ✓



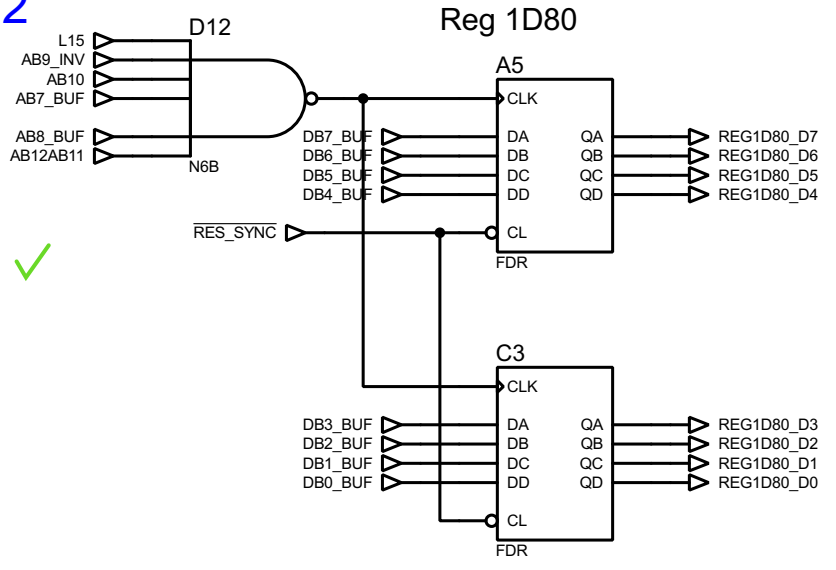
5.7 ✓



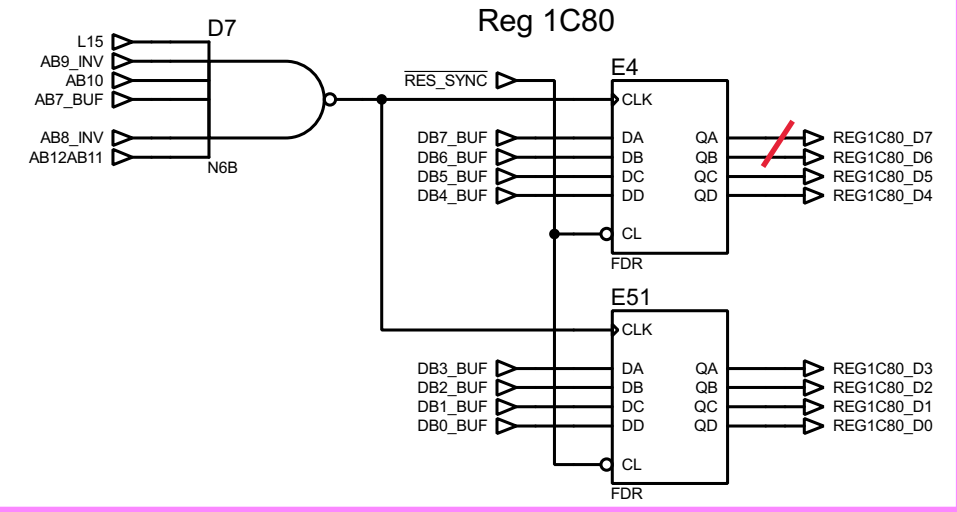
5.8 ✓



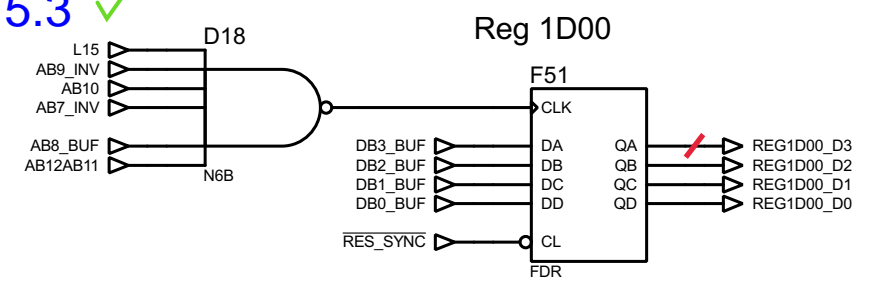
5.2 ✓



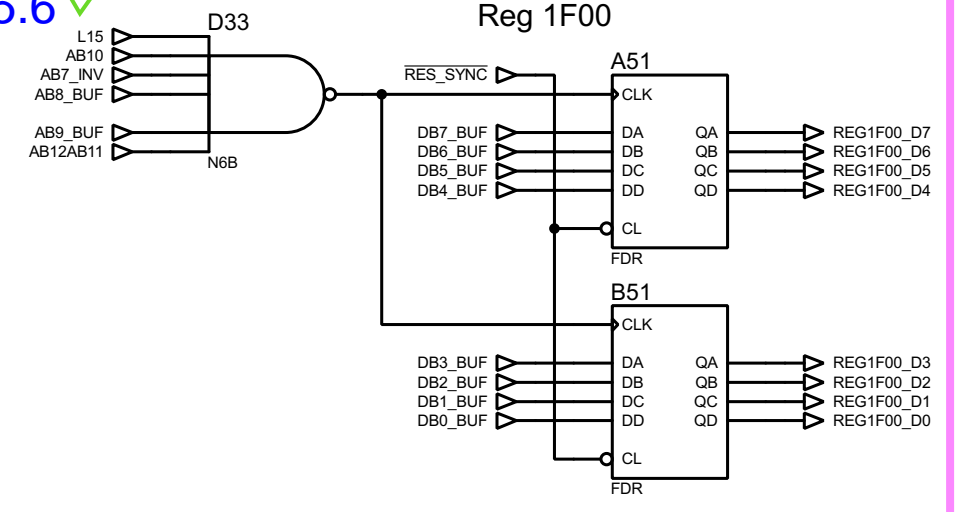
5.5 ✓



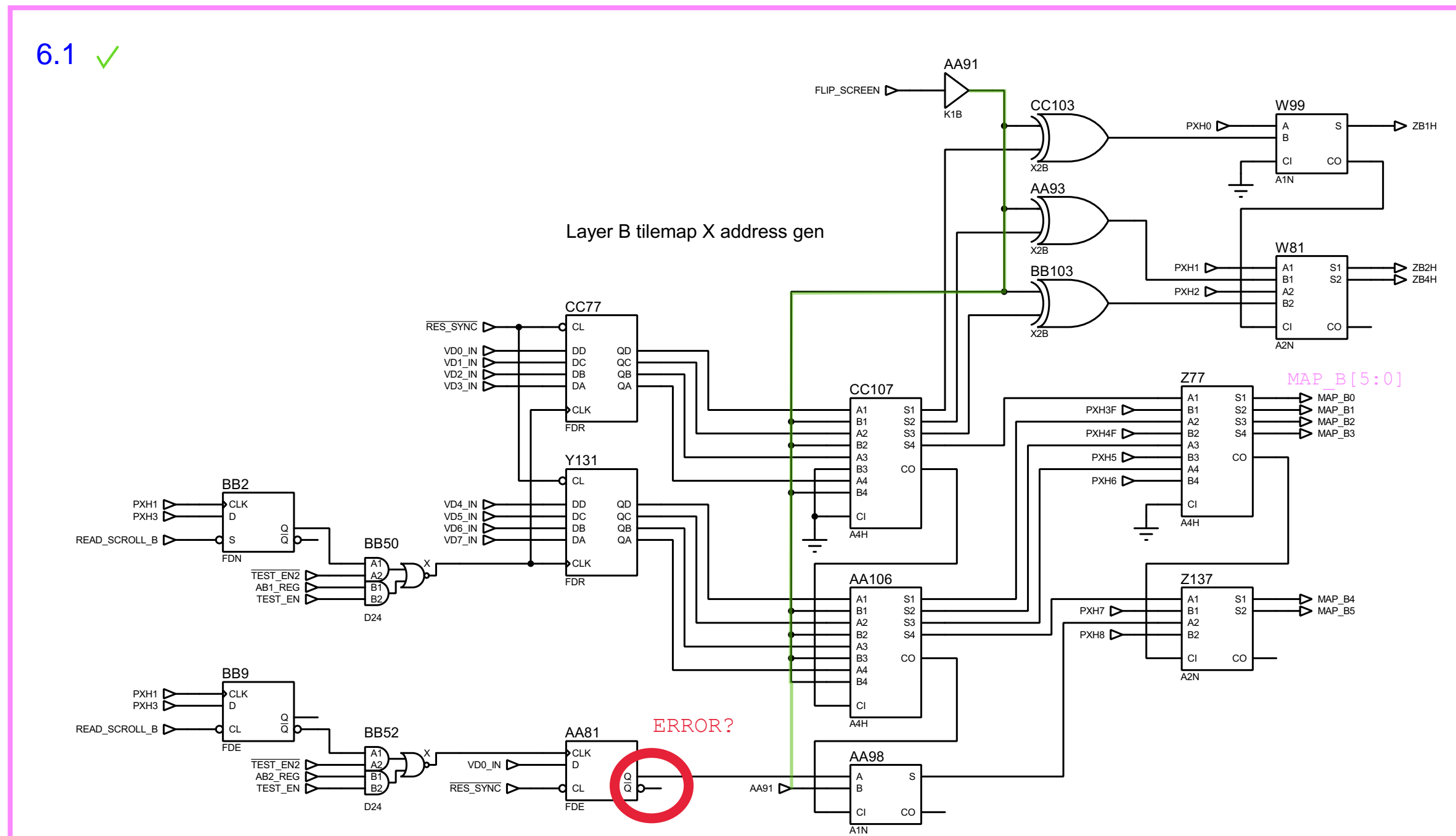
5.3 ✓



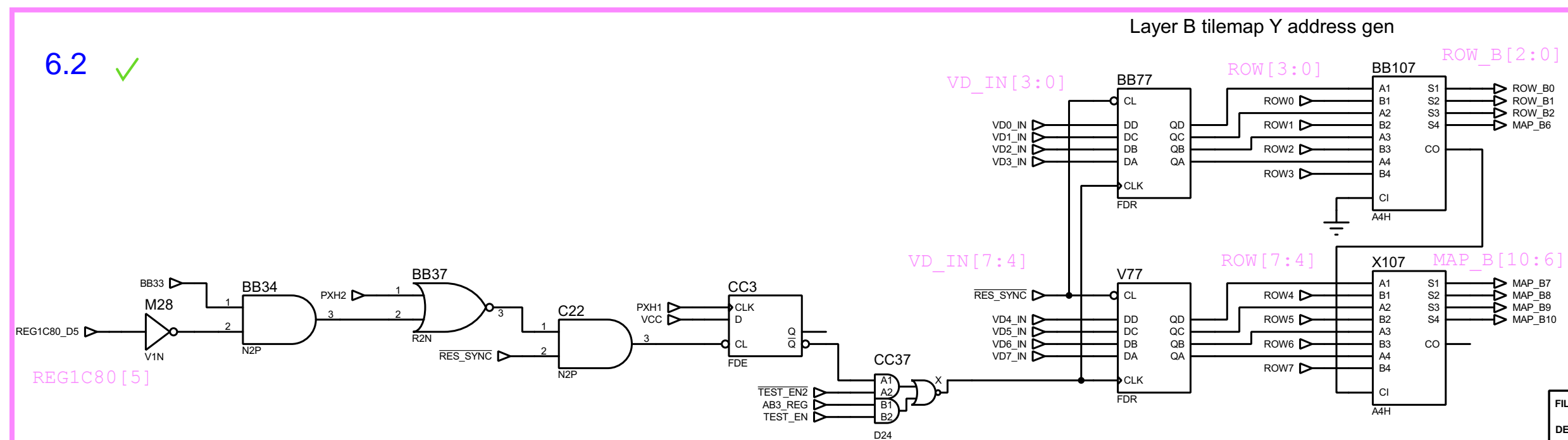
5.6 ✓



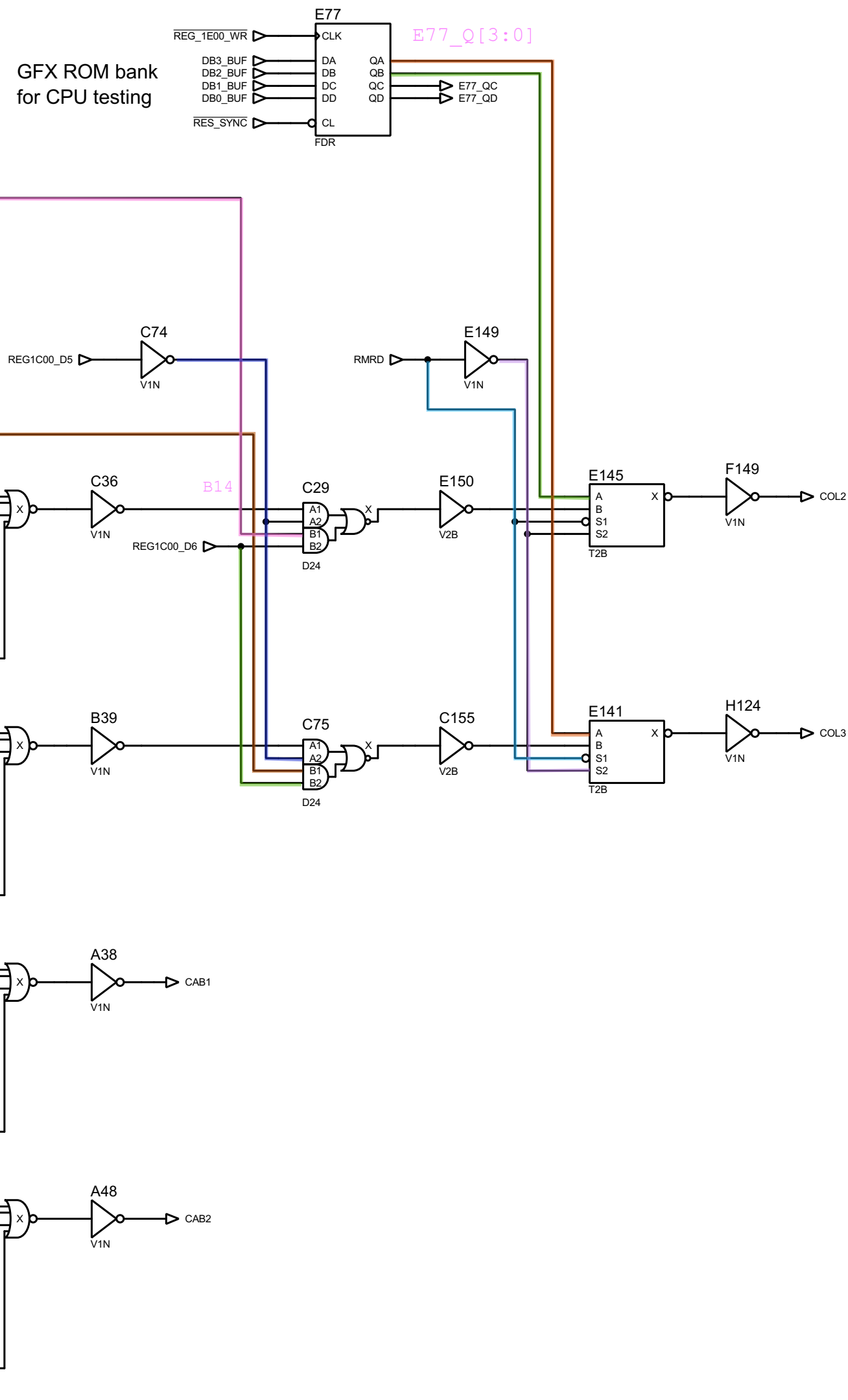
6.1 ✓



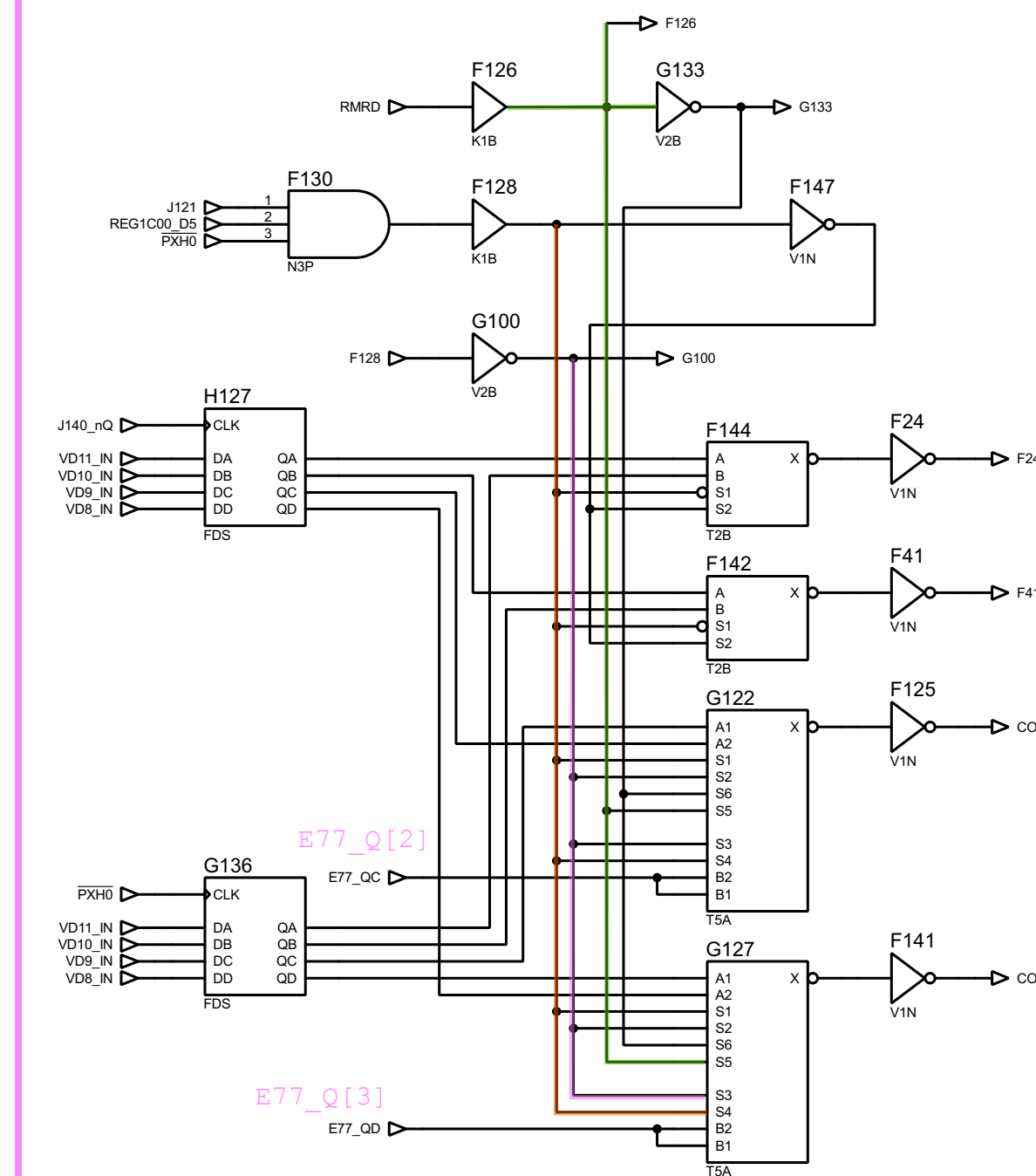
6.2 ✓



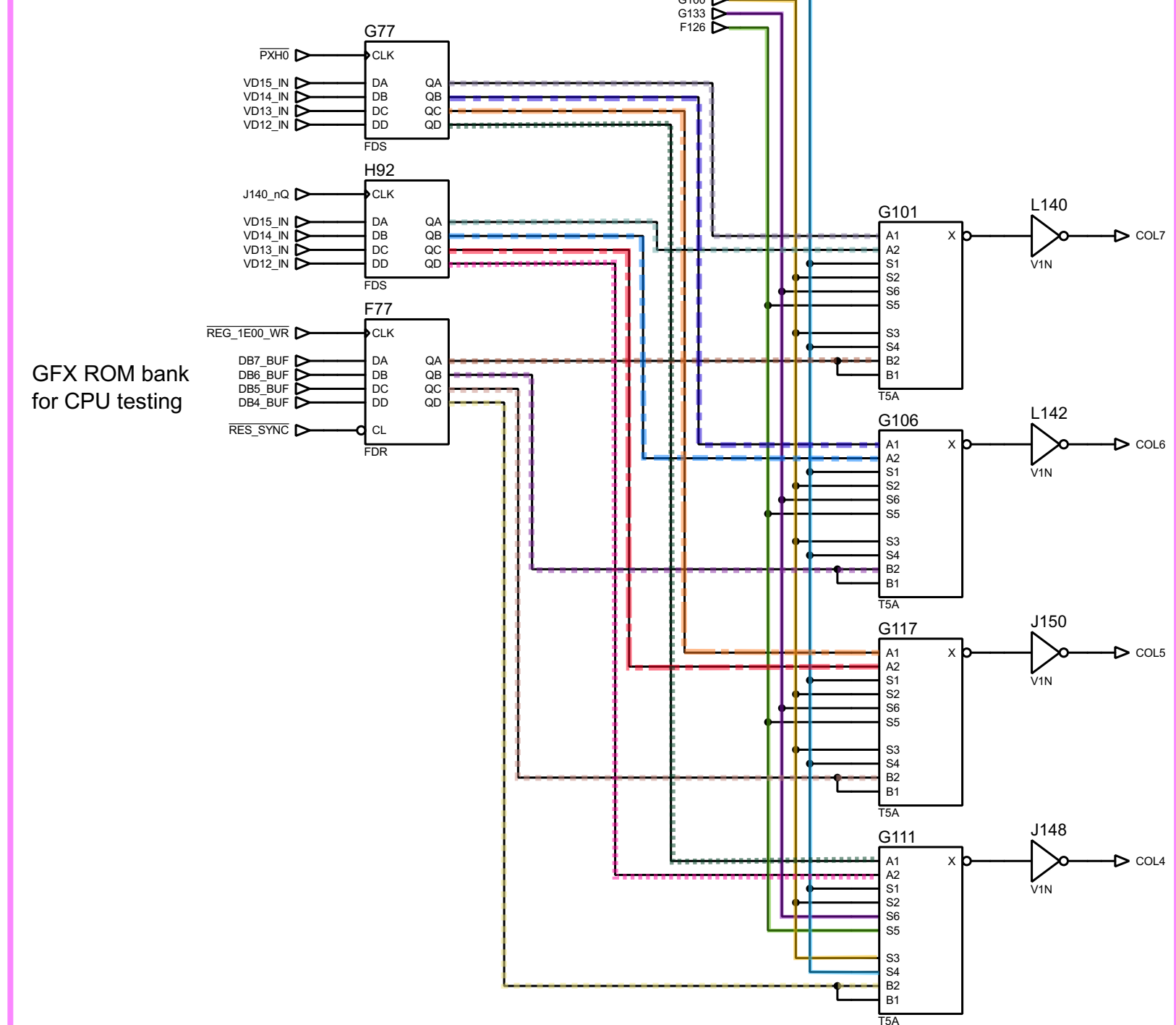
7.2



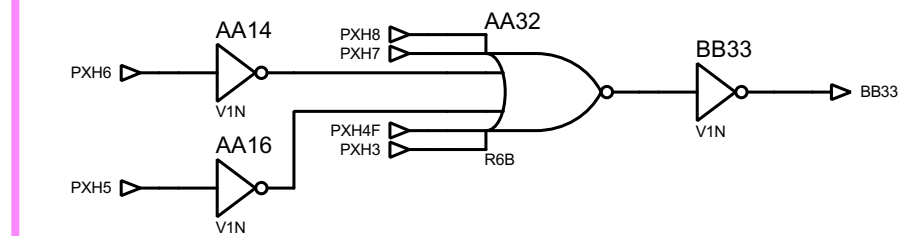
7.1



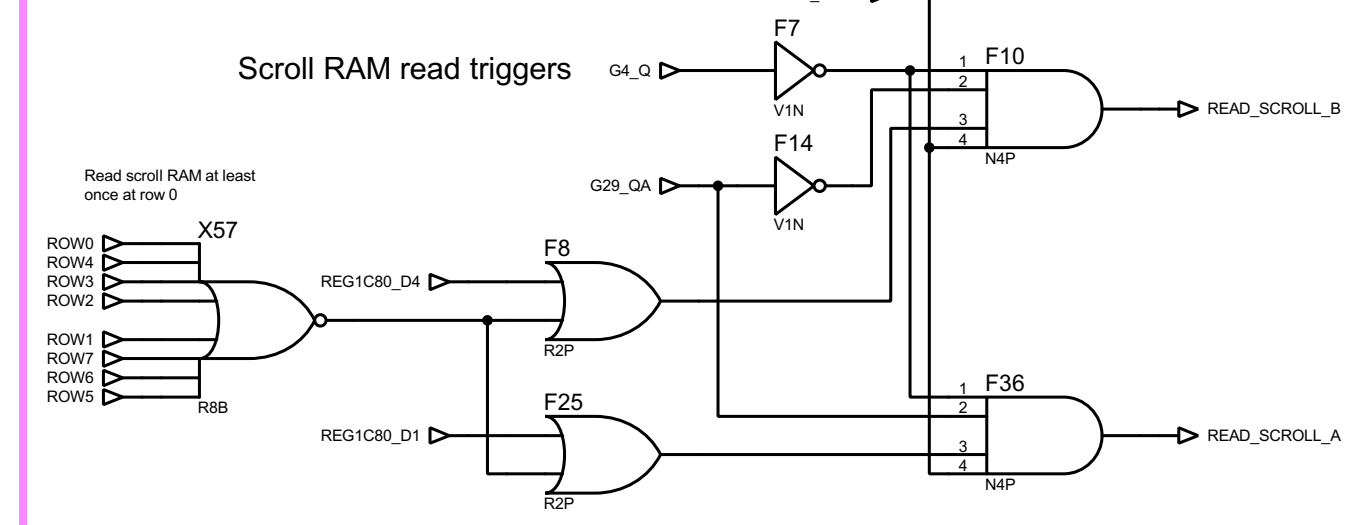
7.3



7.4

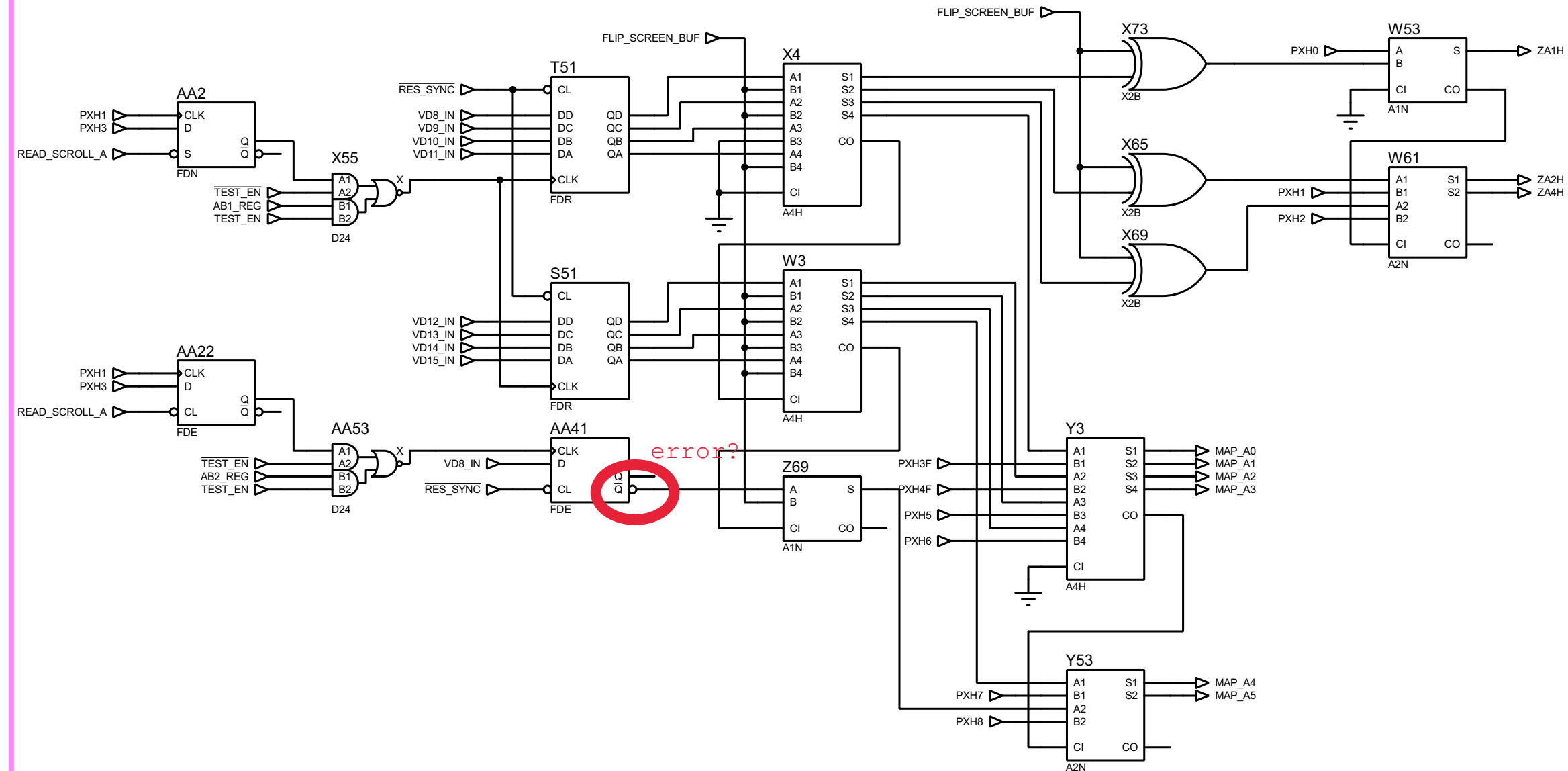


7.5



8.1 ✓

Layer A tilemap X address gen



8.2 ✓

Layer A tilemap Y address gen

