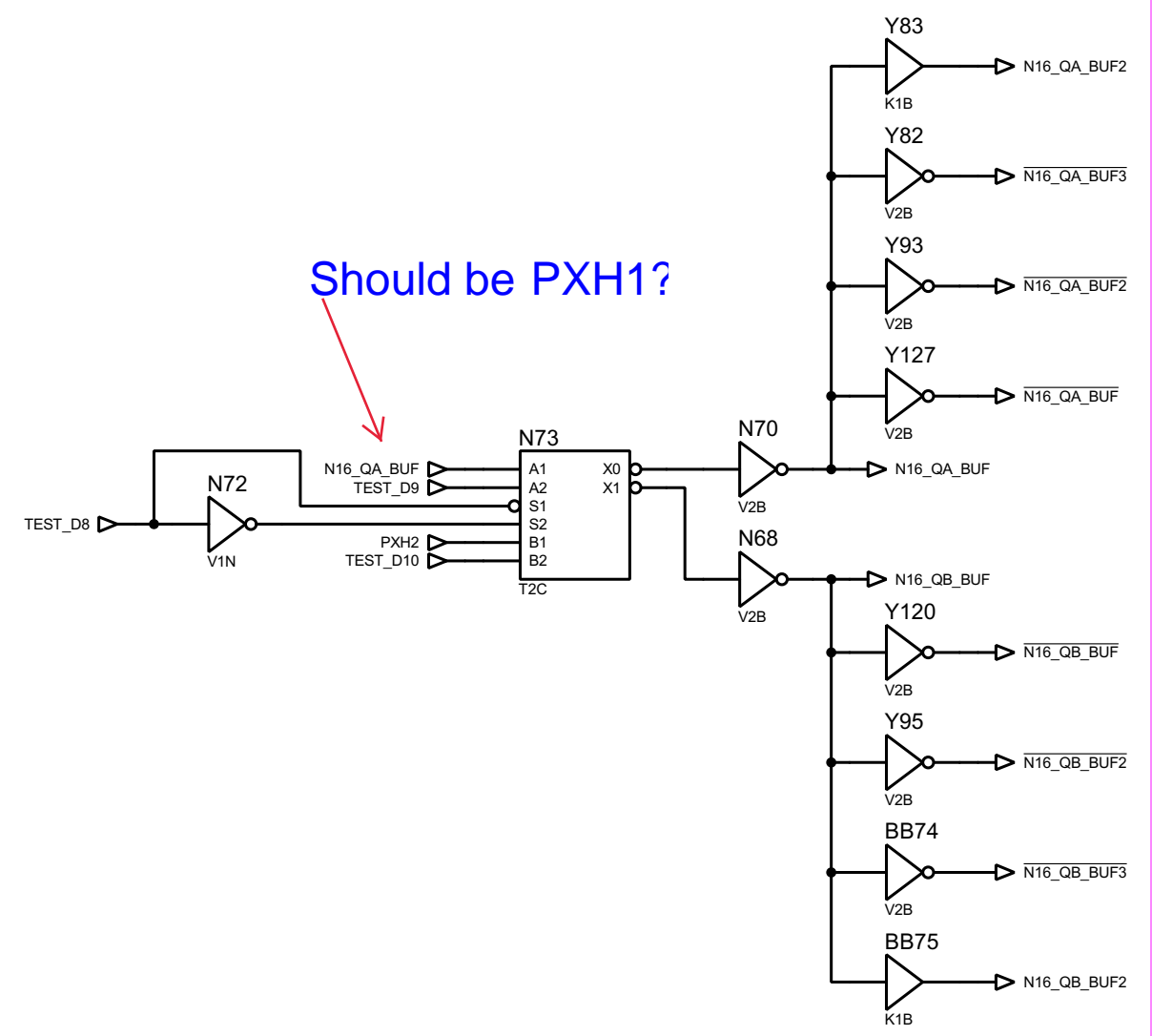


```

VRAM      address (1 word per address)
FEDC      BA98      7654      3210
0000      01xx      xxxx      xxxx      Layer FIX tilemap
0001      01xx      xxxx      xxxx      Layer A tilemap
0002      10xx      xxxx      xxxx      Layer B tilemap
0003      0000      0000      0000      Layer C tilemap
0004      0000      0000      0000      Layer D tilemap
0005      0000      11xx      xxxx      A X scroll
0006      0001      00xx      xxxx      Layer FIX codes
0007      0001      01xx      xxxx      Layer A codes
0008      0001      10xx      xxxx      Layer B codes
0009      0001      1100      0000      Layer C codes
0010      0001      1101      xxxx      B X scroll
0011      0001      1101      0000      x xxxx x Tilemaps X
0012      0001      1101      0000      xx xxx Tilemaps Y

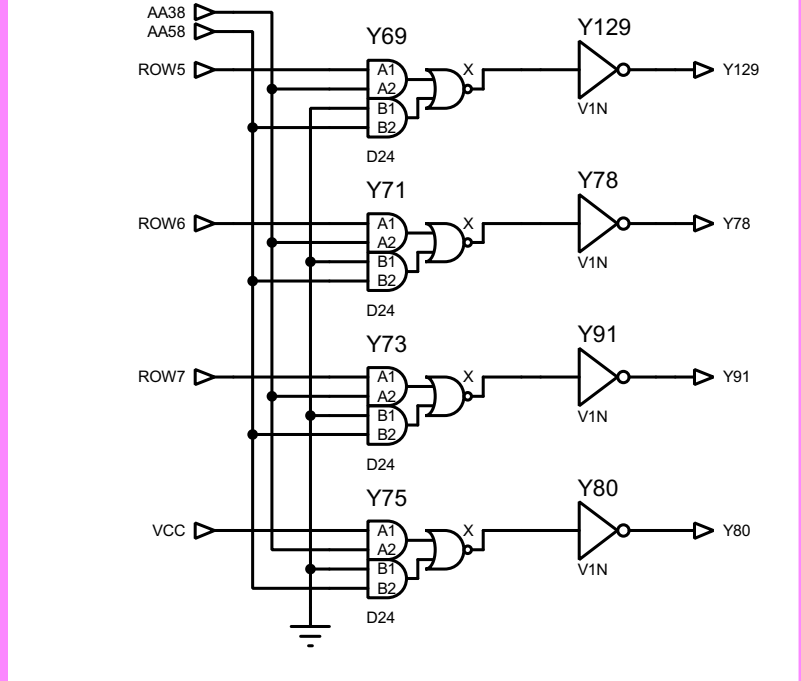
```

1.1



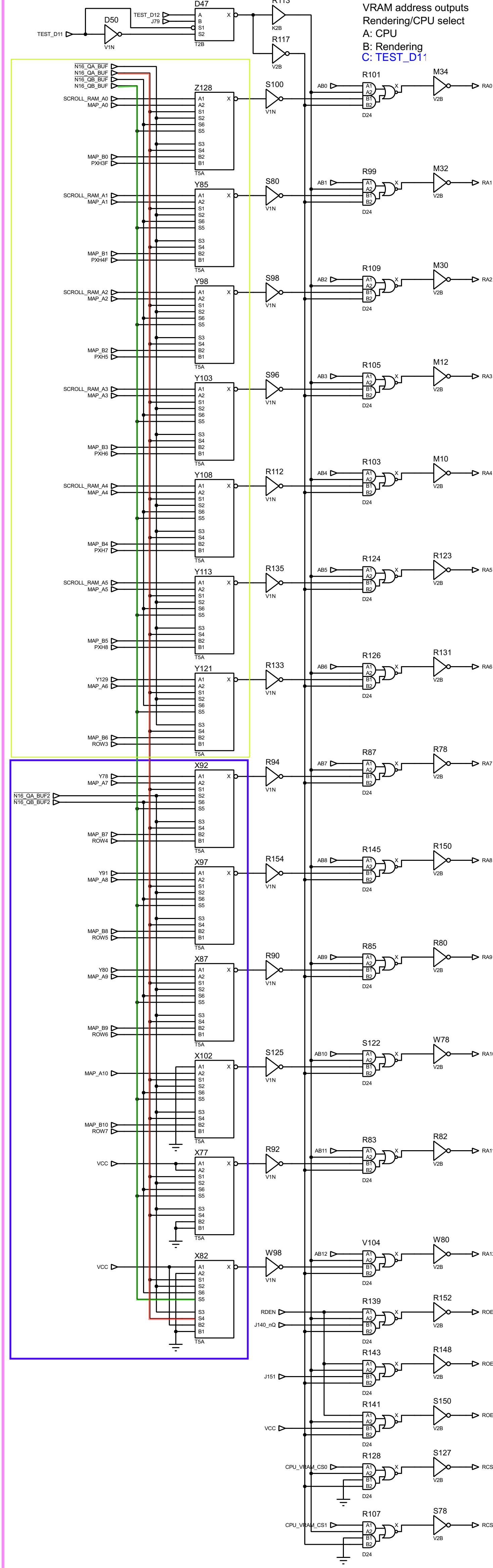
TEST_D13 Addresses Selector

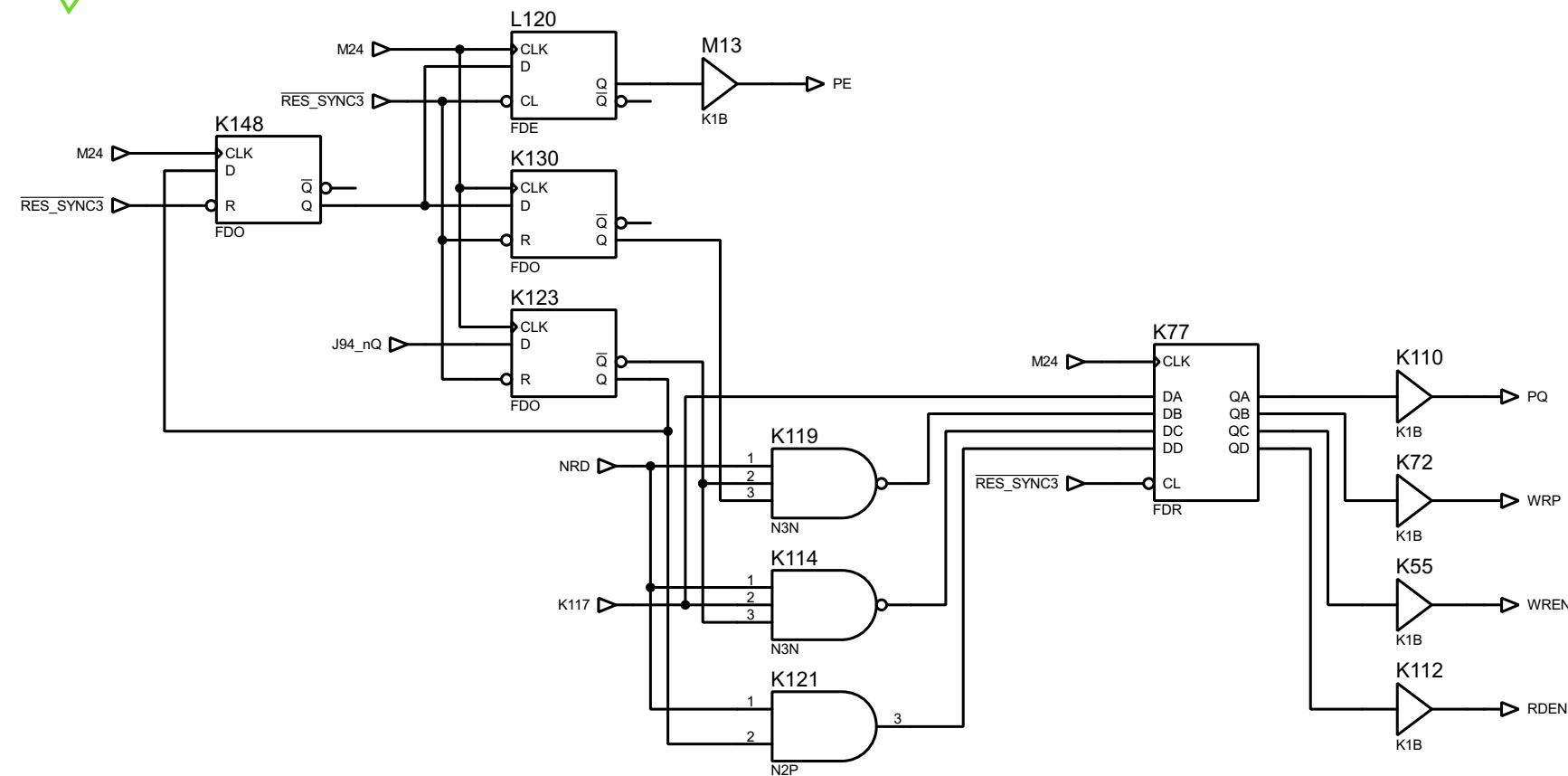
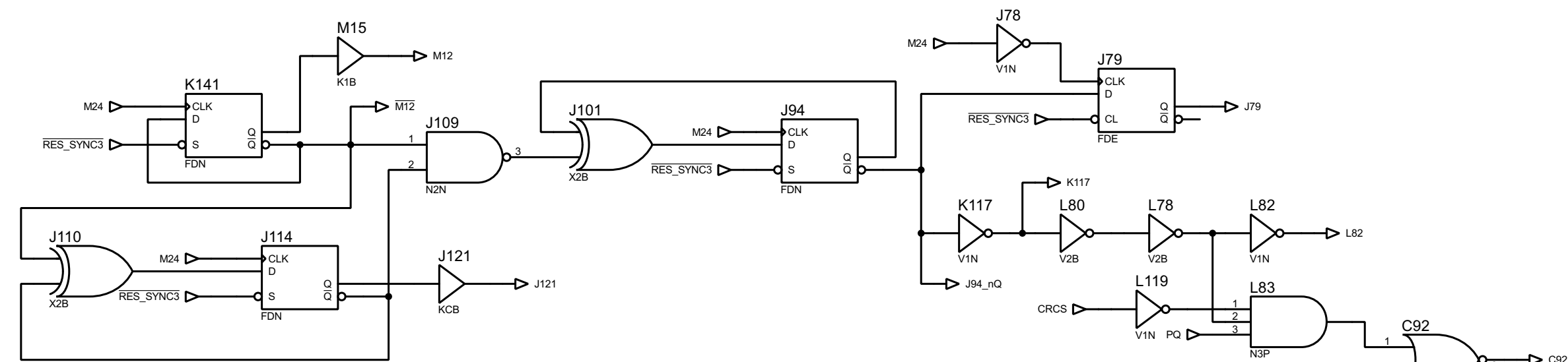
1.2 From 4.3



Selection can be simplified using AA38 (and AA38n) only, AA58 always selects 1'b0.

1.3

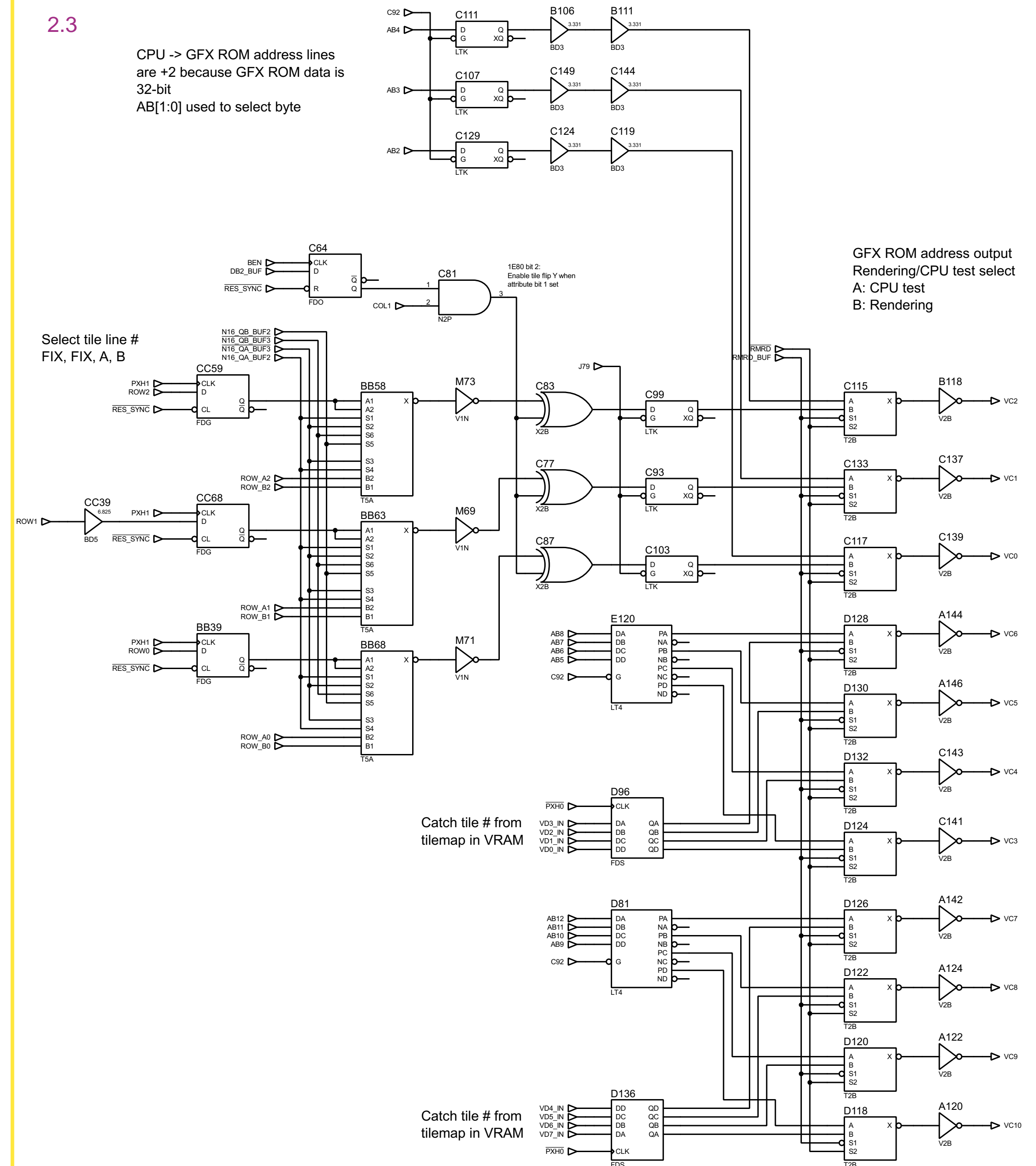




TIMING SIGNALS

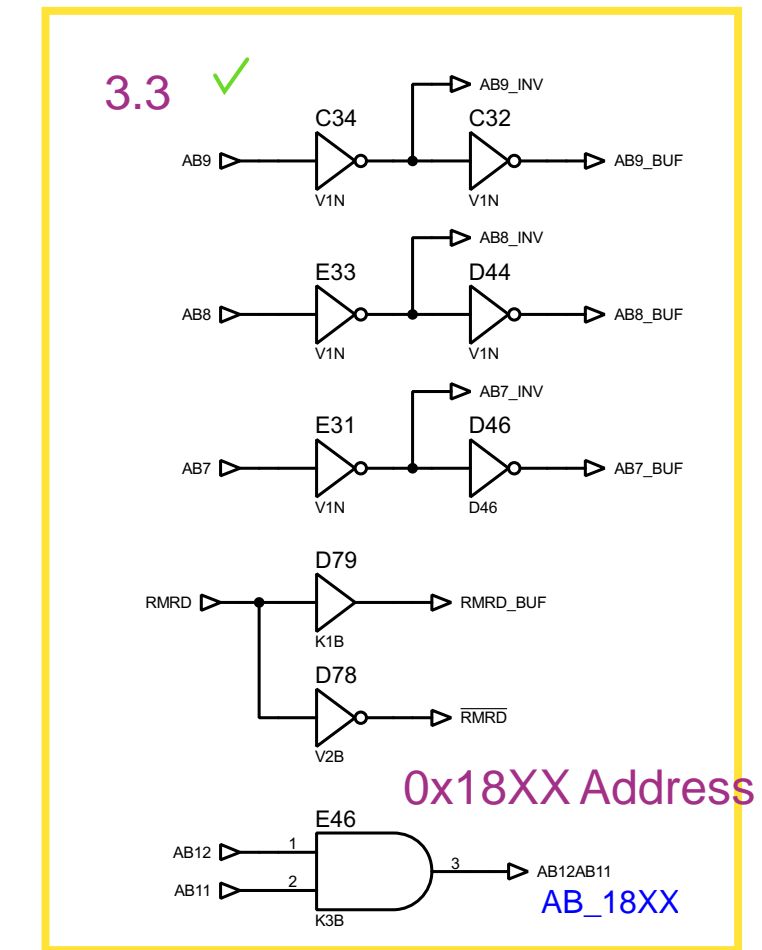
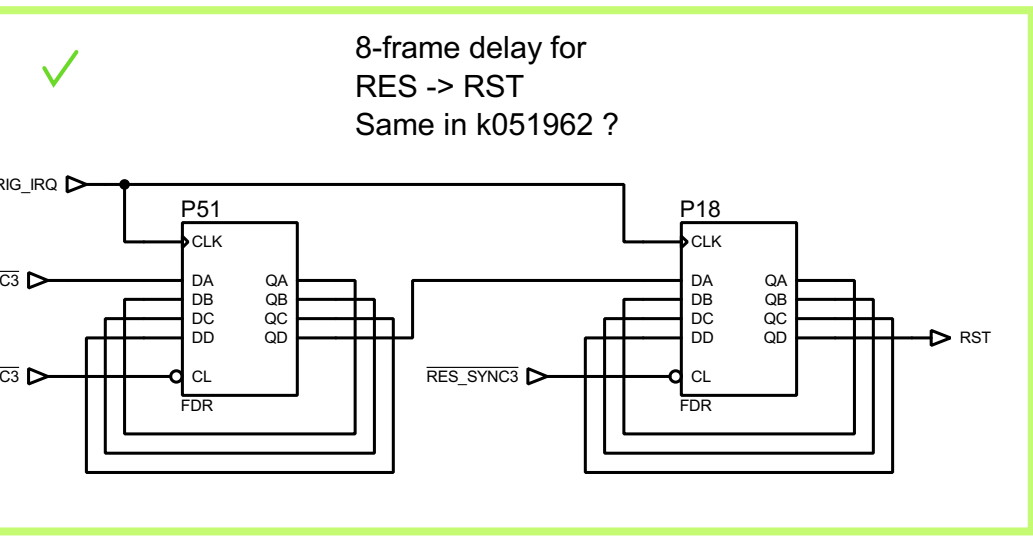
2.3

CPU -> GFX ROM address lines
are +2 because GFX ROM data is
32-bit
AB[1:0] used to select byte



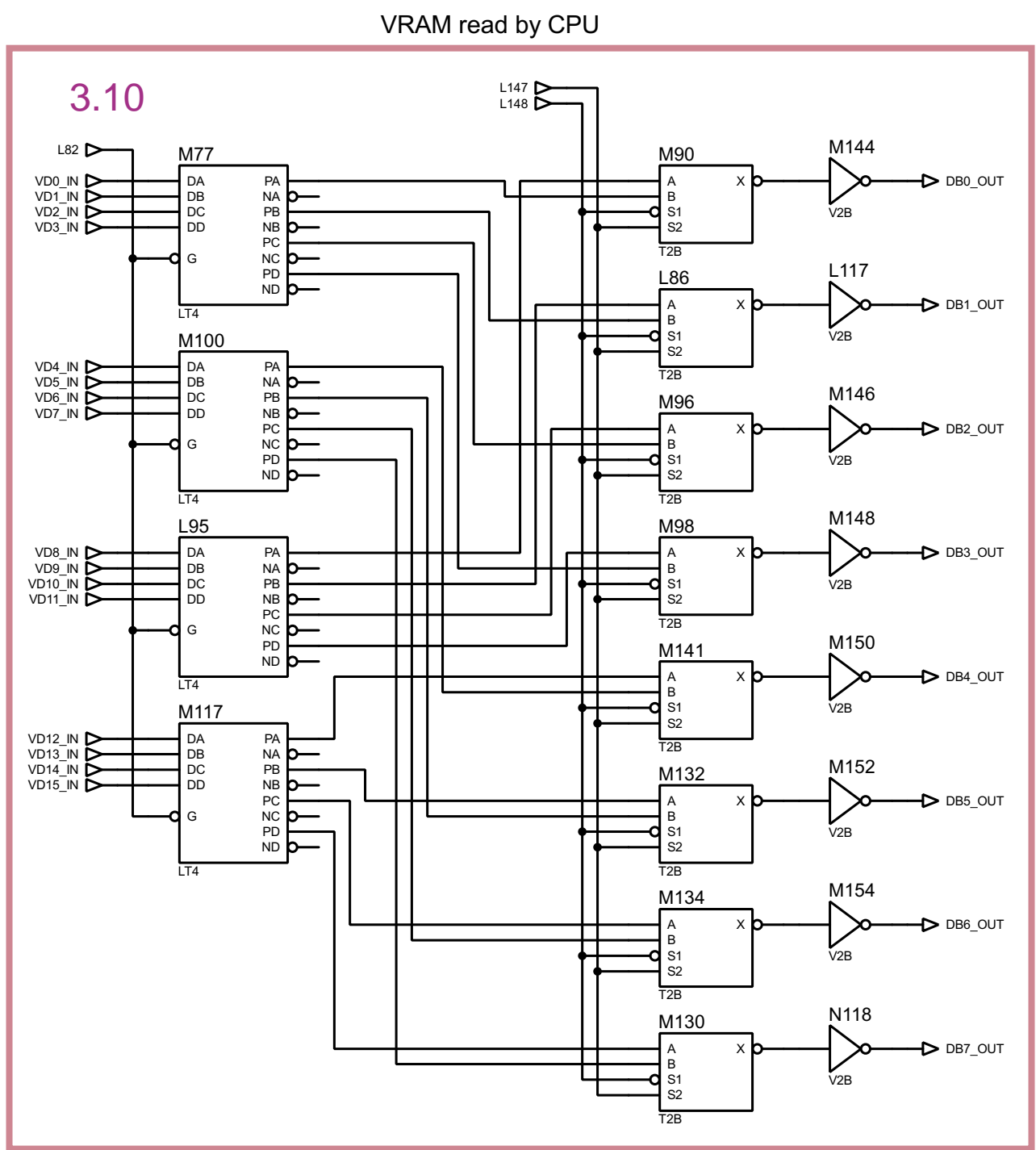
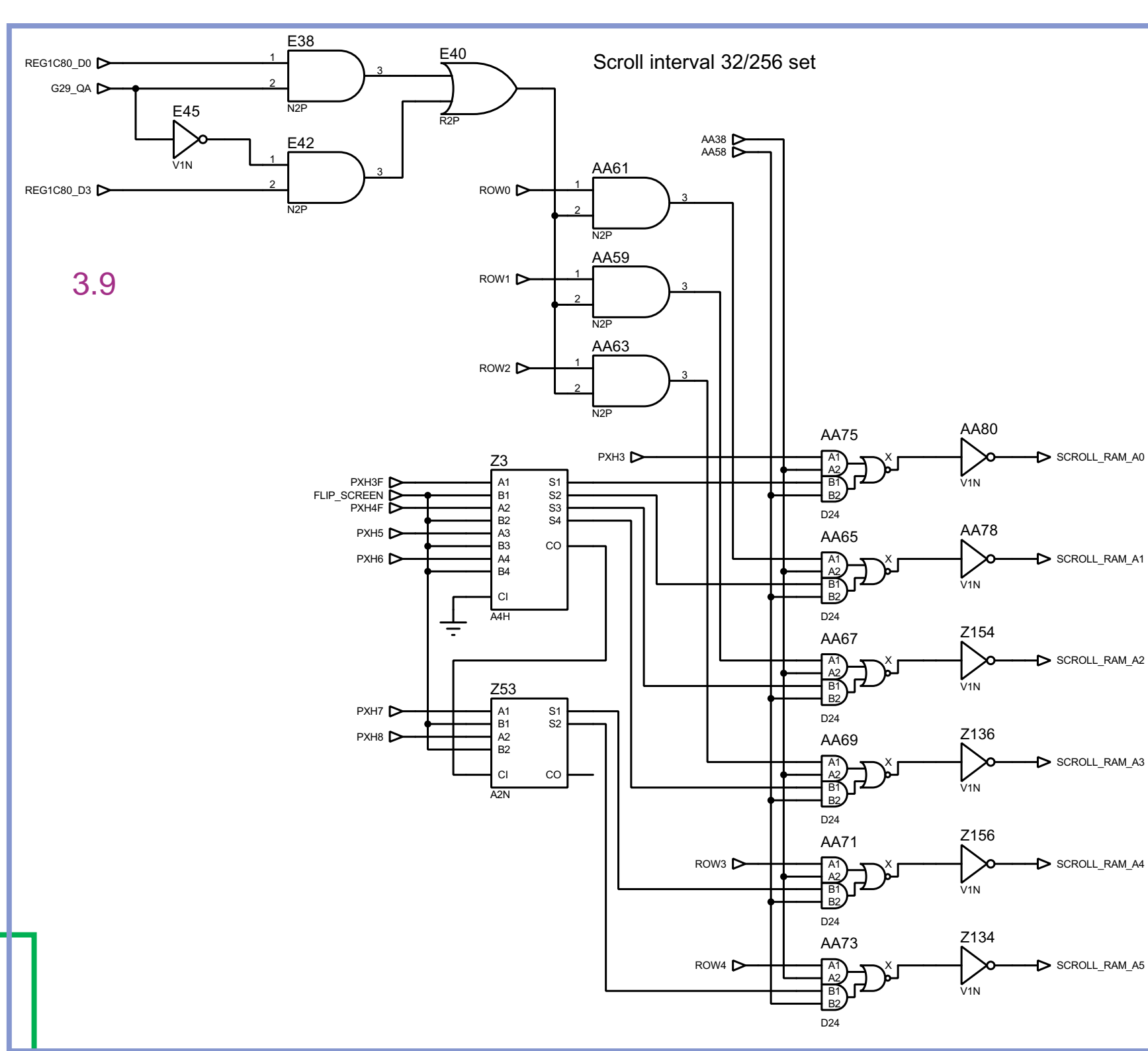
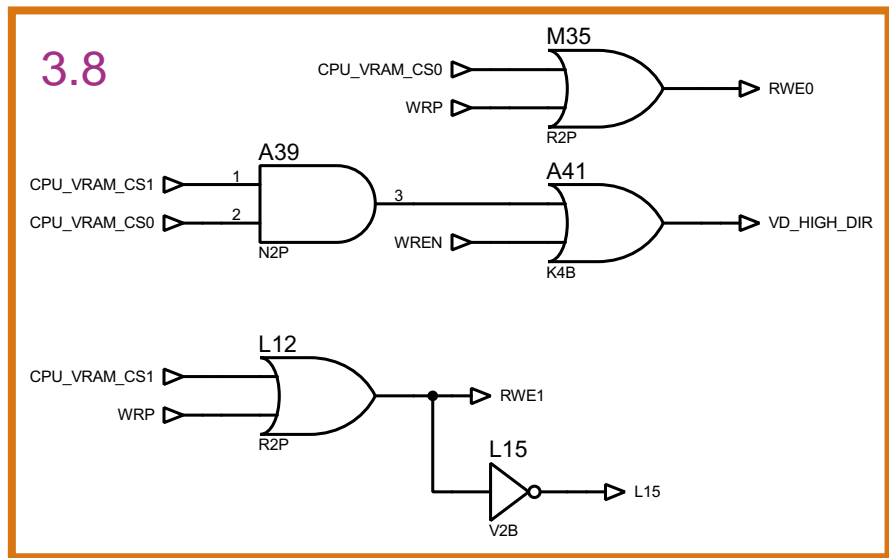
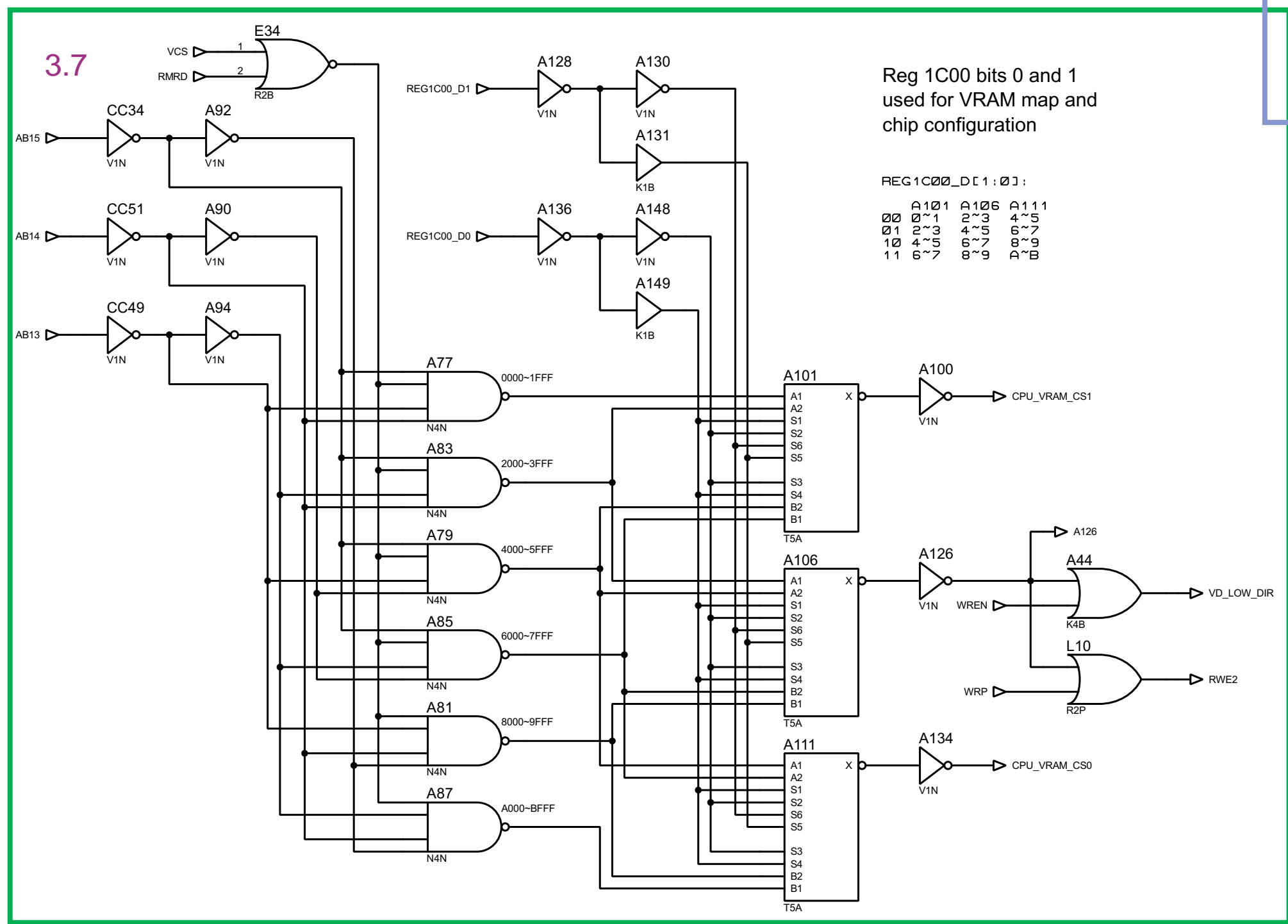
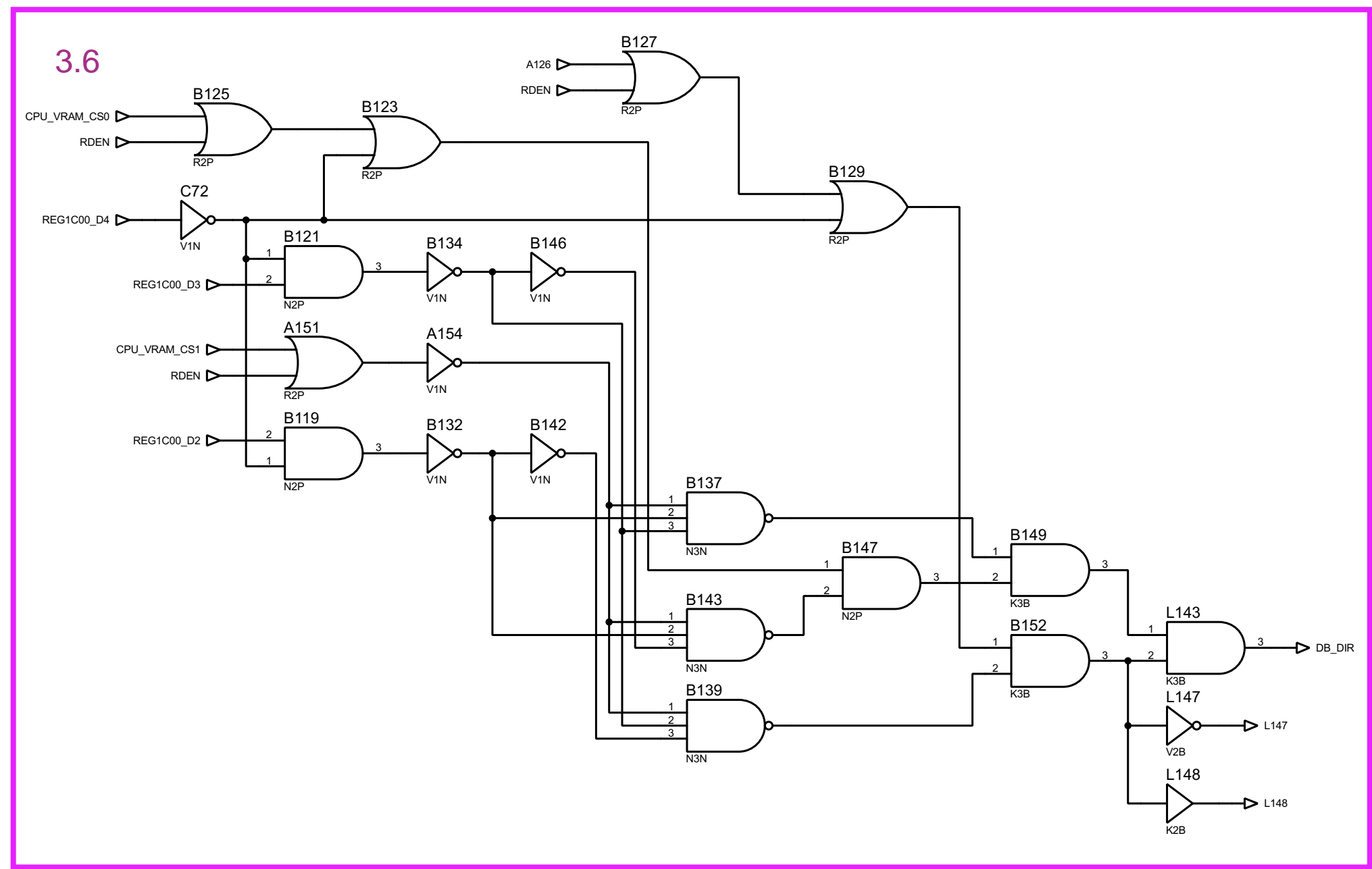
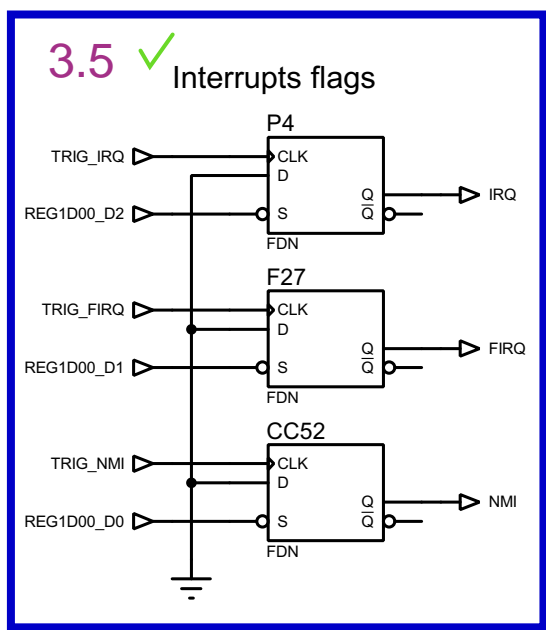
3.1 ✓

The diagram shows a circuit for a 3-bit counter. It consists of three main components: an N122 flip-flop, an M74 3-to-8 decoder, and an H12 3-input OR gate. The N122 flip-flop has inputs M04 (CLK), V02 (D), and RES (CL), and outputs Q and FDE. The M74 decoder has a 3-bit input (Q, Q-bar, and FDE) and eight outputs, one of which is RES_SYNC3. The H12 OR gate has three inputs (Q, Q-bar, and FDE) and two outputs, RES_SYNC and RES_SYNC2.



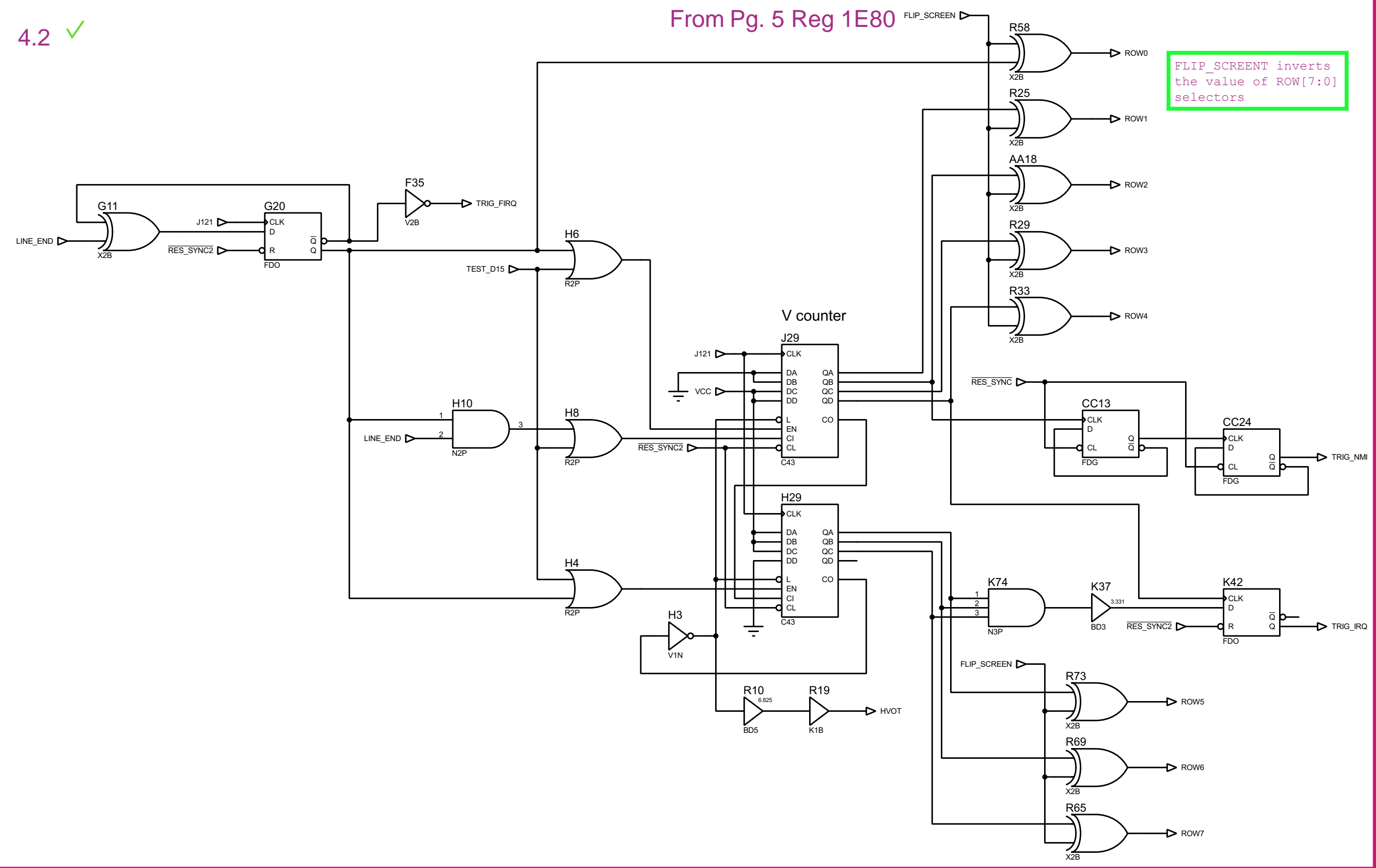
3.4 ✓

The diagram illustrates a 10-bit bus system. It consists of 10 inverters, each labeled with a component number (N135, N80, N132, N77, N83, N97, N100, N103) and a 4-bit bus identifier (K2B). Each inverter has an input labeled 'DBx_IN' and an output labeled 'DBx_BUF', where 'x' ranges from 0 to 9. The inputs are connected to the outputs of the previous stage, forming a chain of inverters. The outputs are labeled DB0_BUF, DB1_BUF, DB2_BUF, DB3_BUF, DB4_BUF, DB5_BUF, DB6_BUF, and DB7_BUF. The diagram shows the internal structure of the bus system, including the inverters and the bus identifiers.

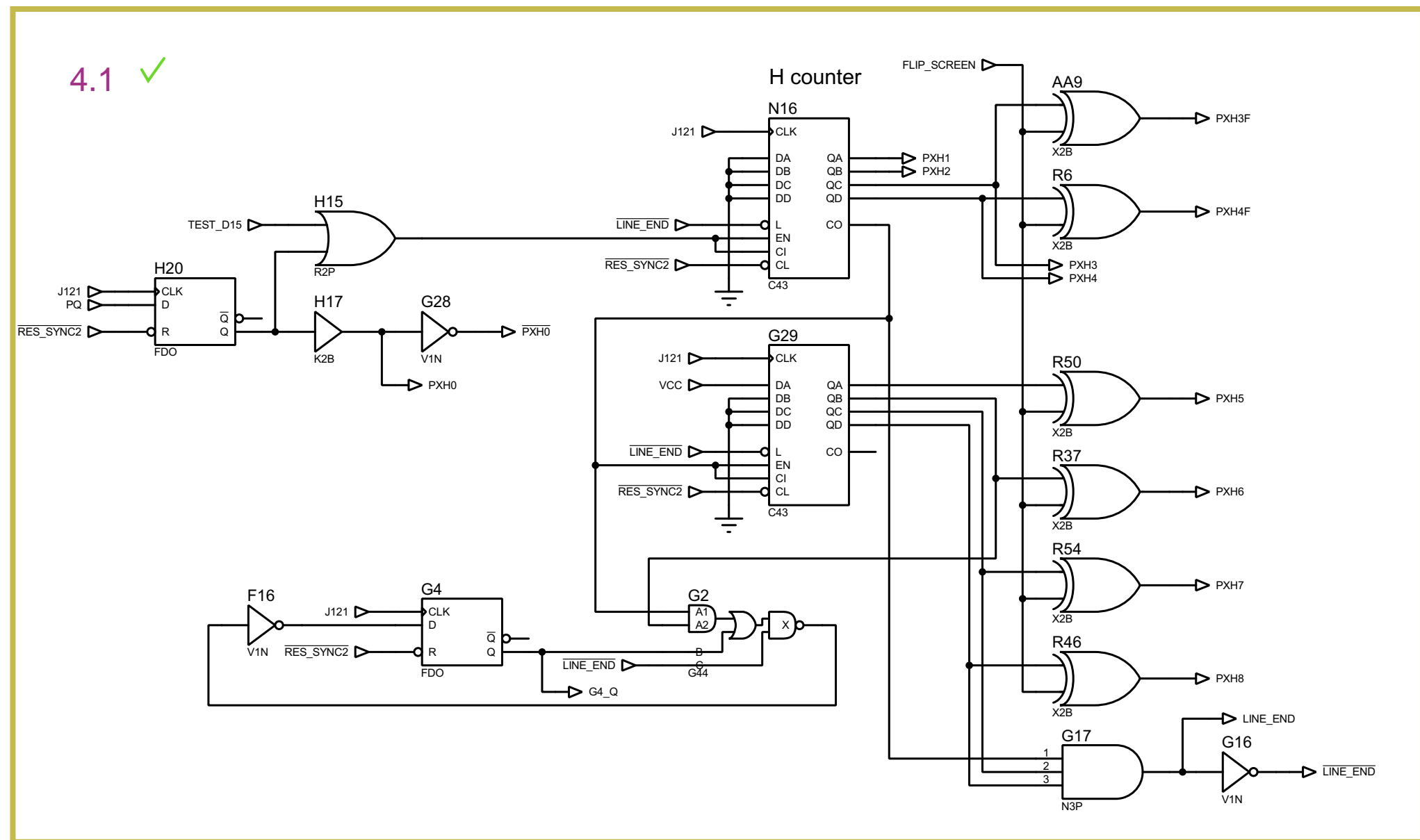


```
wire [7:0] DB_BUF
```

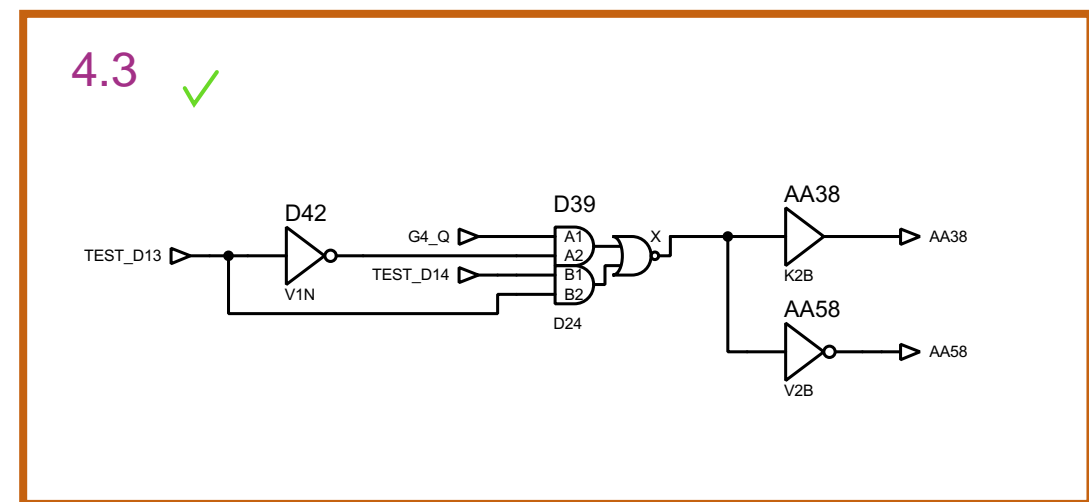
4.2 ✓



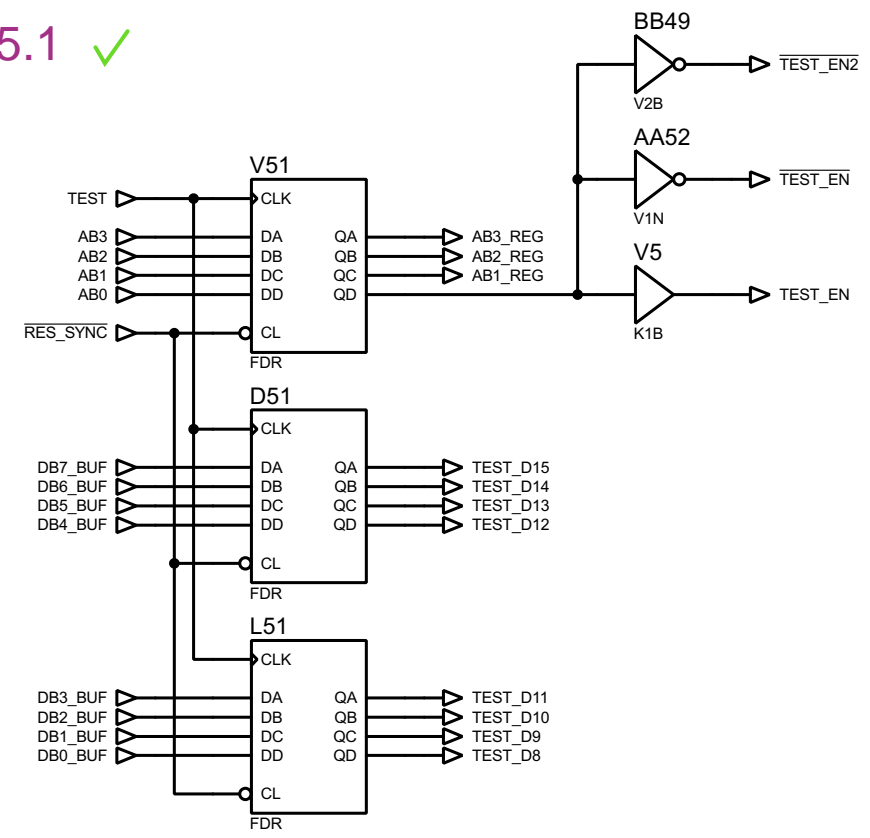
4.1 ✓



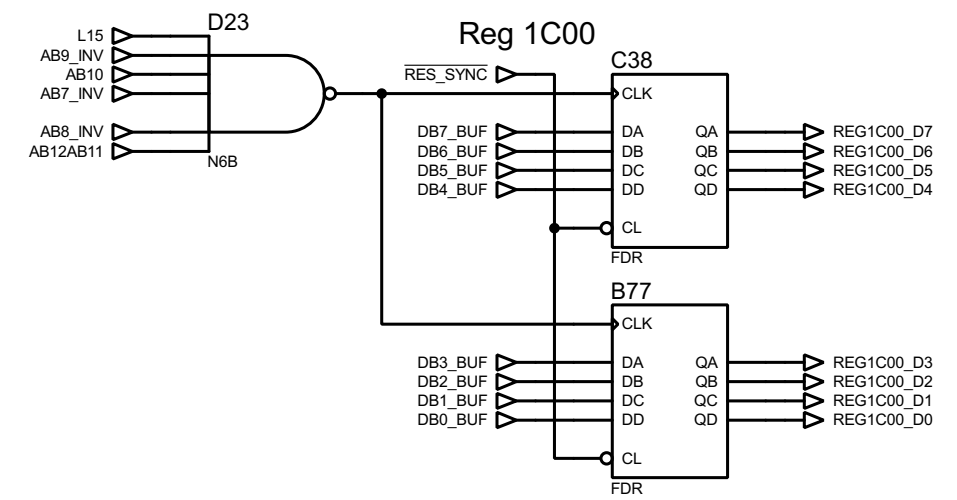
4.3 ✓



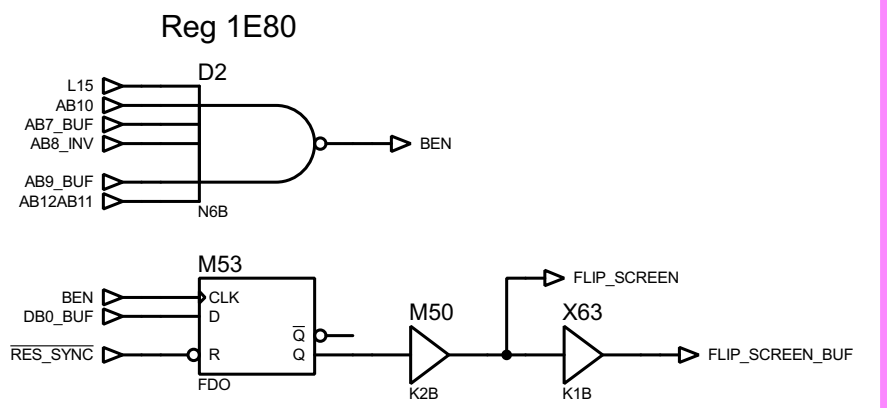
5.1 ✓



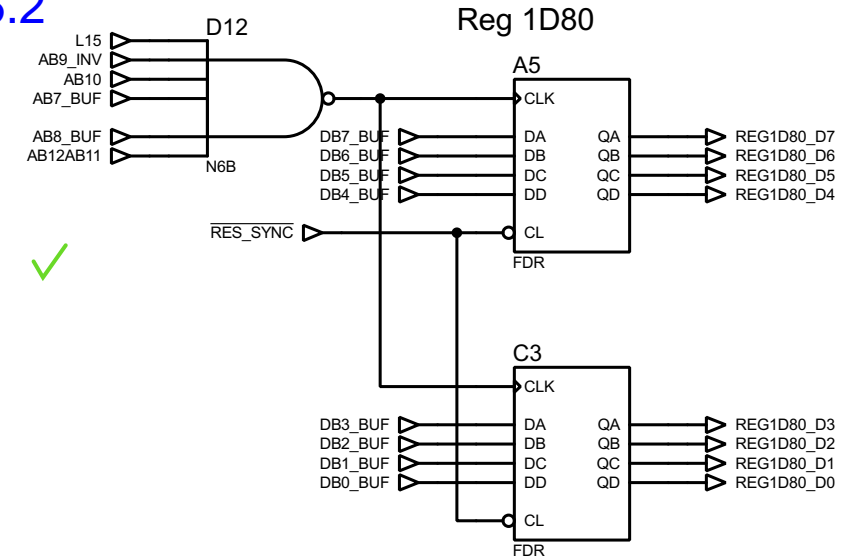
5.4 ✓



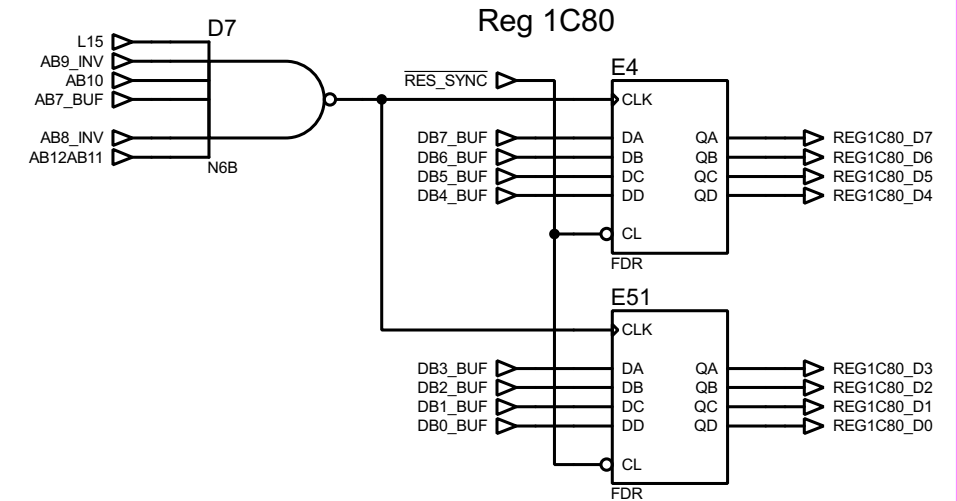
5.7 ✓



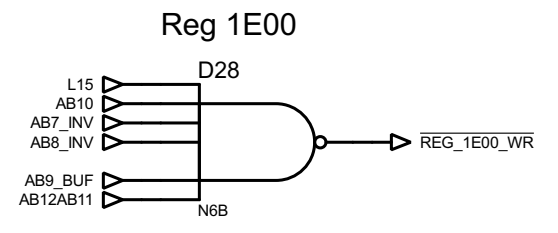
5.2 ✓



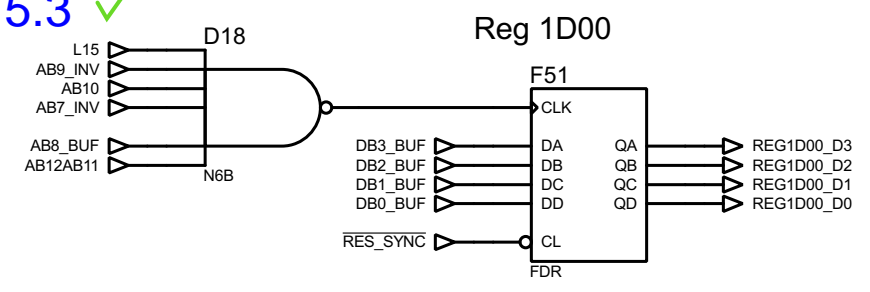
5.5 ✓



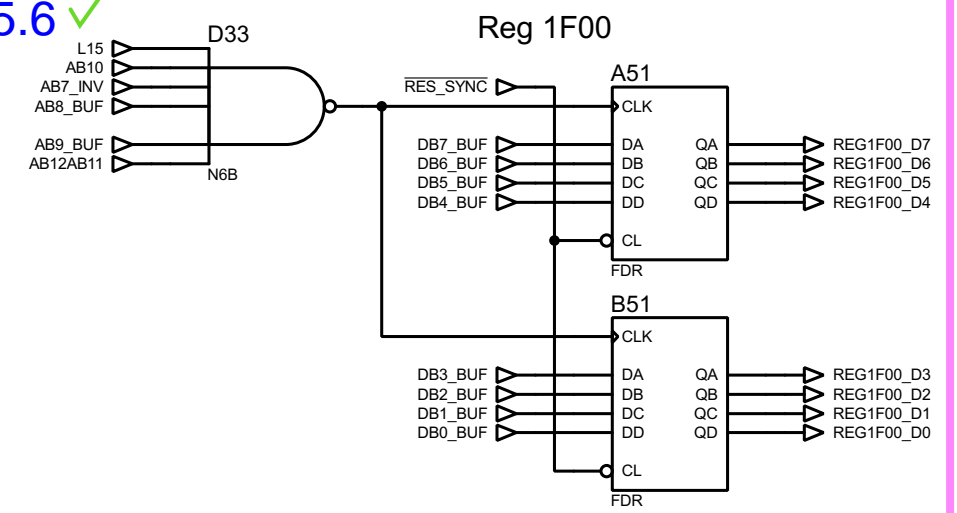
5.8 ✓



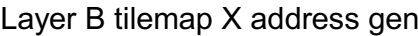
5.3 ✓



5.6 ✓



6.1



6.2



The diagram illustrates the internal logic of the GFX ROM bank for CPU testing. It features a 4-to-1 multiplexer (E77) that selects between four 8-bit ROM banks (DB3_BUF, DB2_BUF, DB1_BUF, DB0_BUF) based on the REG_TE00_WR signal. The selected data is then routed through various logic gates (AND, OR, NOT) and registers (REG1C00_D5, REG1C00_D6) to produce the final output signals (COL2, COL3).

Key components and signals include:

- Inputs:** REG_TE00_WR, DB3_BUF, DB2_BUF, DB1_BUF, DB0_BUF, RES_SYNC, F41, F24, REG1D80_D0, REG1D80_D4, REG1F00_D0, REG1F00_D4, REG1D80_D1, REG1D80_D5, REG1F00_D1, REG1F00_D5, REG1D80_D2, REG1D80_D6, REG1F00_D2, REG1F00_D6, REG1D80_D3, REG1D80_D7, REG1F00_D3, REG1F00_D7.
- Logic Gates:** AND gates (B3, B19, B40, B28), OR gates (C36, C29, C75, C155), NOT gates (A35, A31, C74, E149, E150, E145, E141, H124).
- Registers:** REG1C00_D5, REG1C00_D6.
- Outputs:** COL2, COL3.

7.2

7.3

GFX ROM bank for CPU testing

7.4

7.5

Scroll RAM read triggers

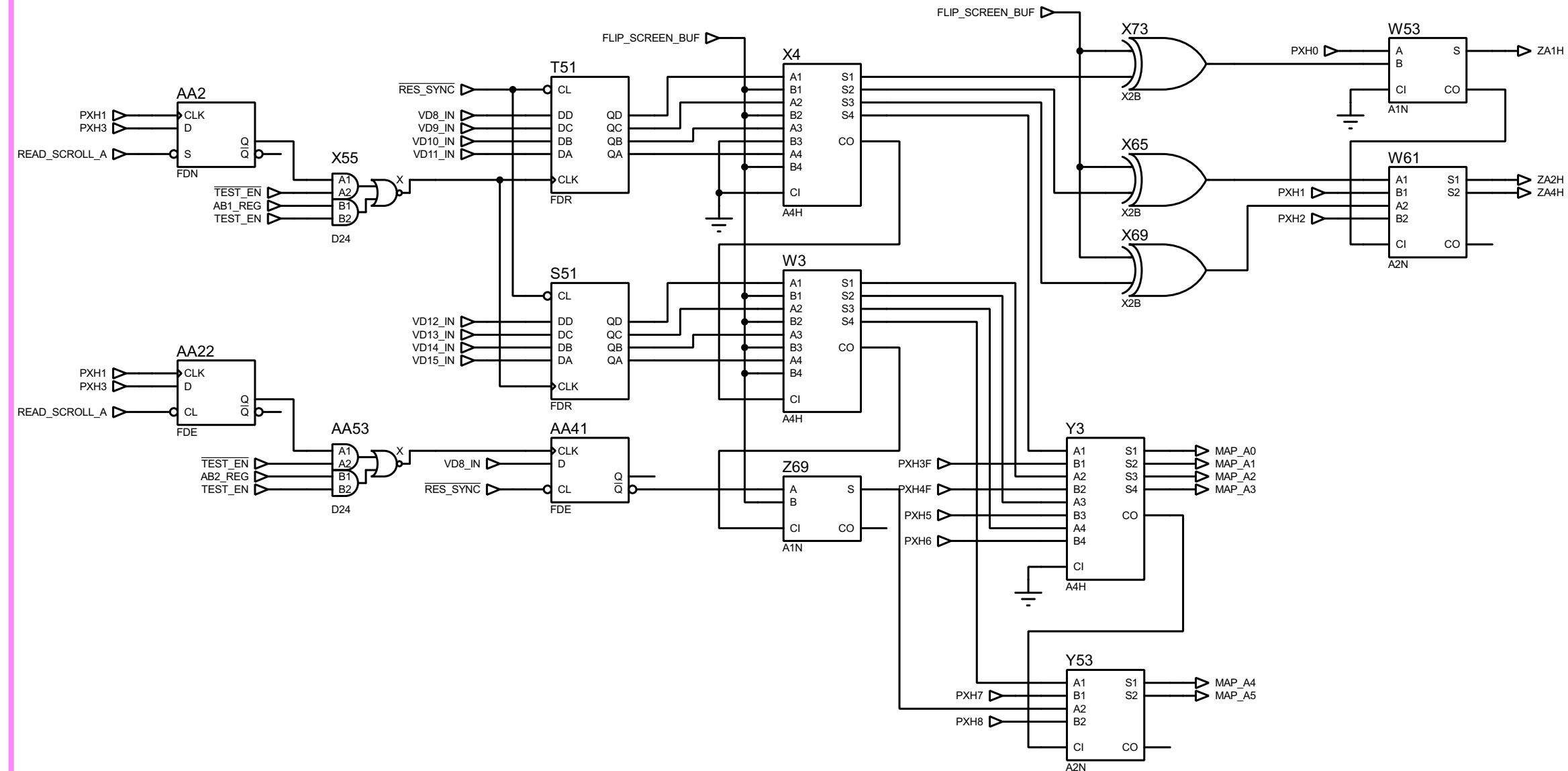
Read scroll RAM at least once at row 0

```

graph LR
    ROW0[ROW0] --> X57
    ROW4[ROW4] --> X57
    ROW3[ROW3] --> X57
    ROW2[ROW2] --> X57
    ROW1[ROW1] --> X57
    ROW7[ROW7] --> X57
    ROW6[ROW6] --> X57
    ROW5[ROW5] --> X57
    X57 --> REG1C80_D4
    REG1C80_D4 --> F8
    REG1C80_D4 --> F25
    R2P[R2P] --> F8
    R2P[R2P] --> F25
    F8 --> F10
    F8 --> F36
    F25 --> F10
    F25 --> F36
    G4_O[G4_O] --> F10
    G4_O[G4_O] --> F36
    G29_QA[G29_QA] --> F10
    G29_QA[G29_QA] --> F36
    RES_SYNC[RES_SYNC] --> F10
    RES_SYNC[RES_SYNC] --> F36
    N4P[N4P] --> F10
    N4P[N4P] --> F36
    F10 --> READ_SCROLL_B
    F36 --> READ_SCROLL_A
  
```

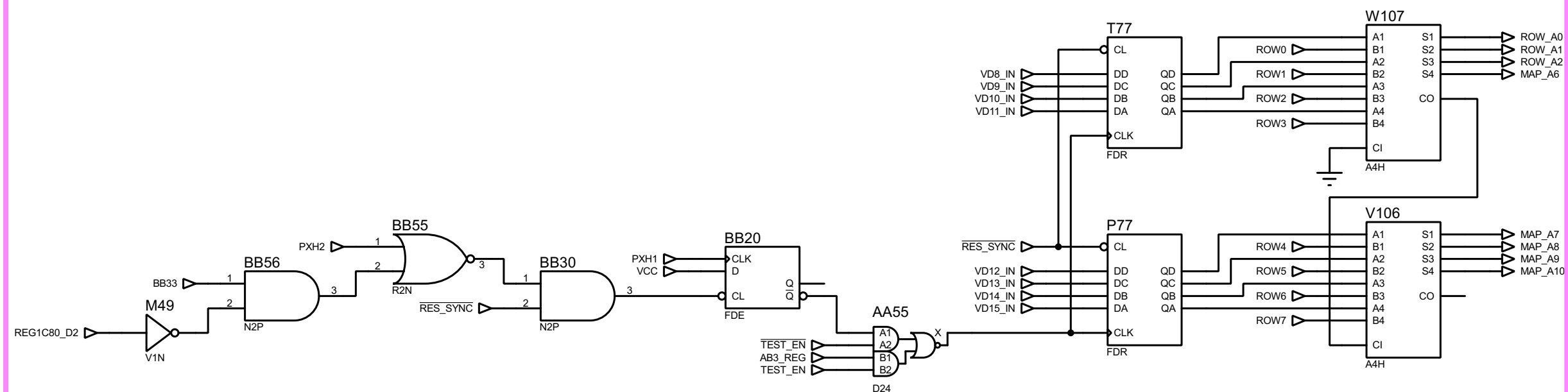
8.1

Layer A tilemap X address gen



8.2

Layer A tilemap Y address gen



FILE NAME: k052109.pdsprj

DESIGN TITLE: Konami 052109
LAYER A SCROLL

BY: Sean Gonsalves

REV: A

DATE:

22/06/2021

PAGE:

8 of 8