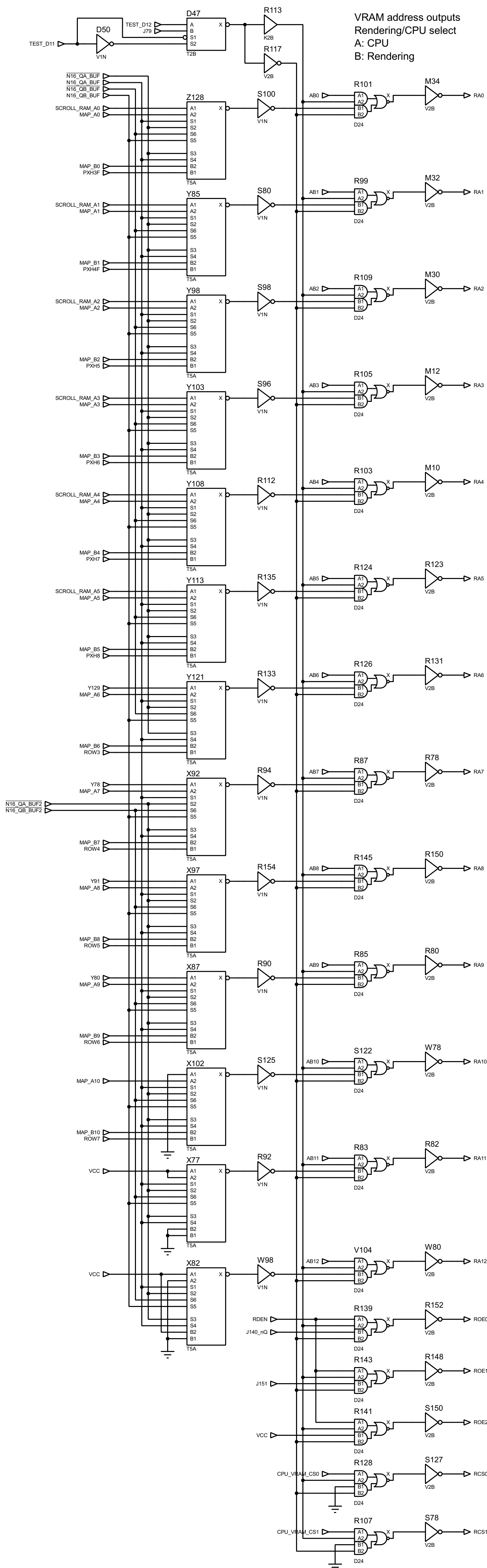
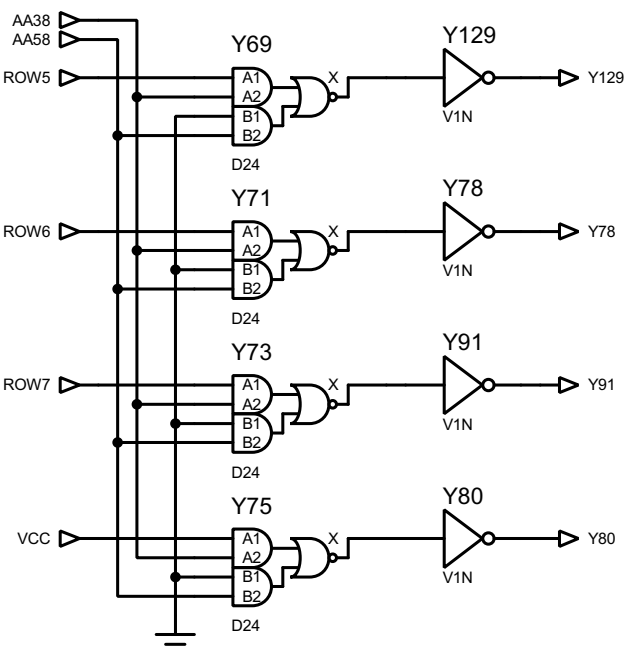
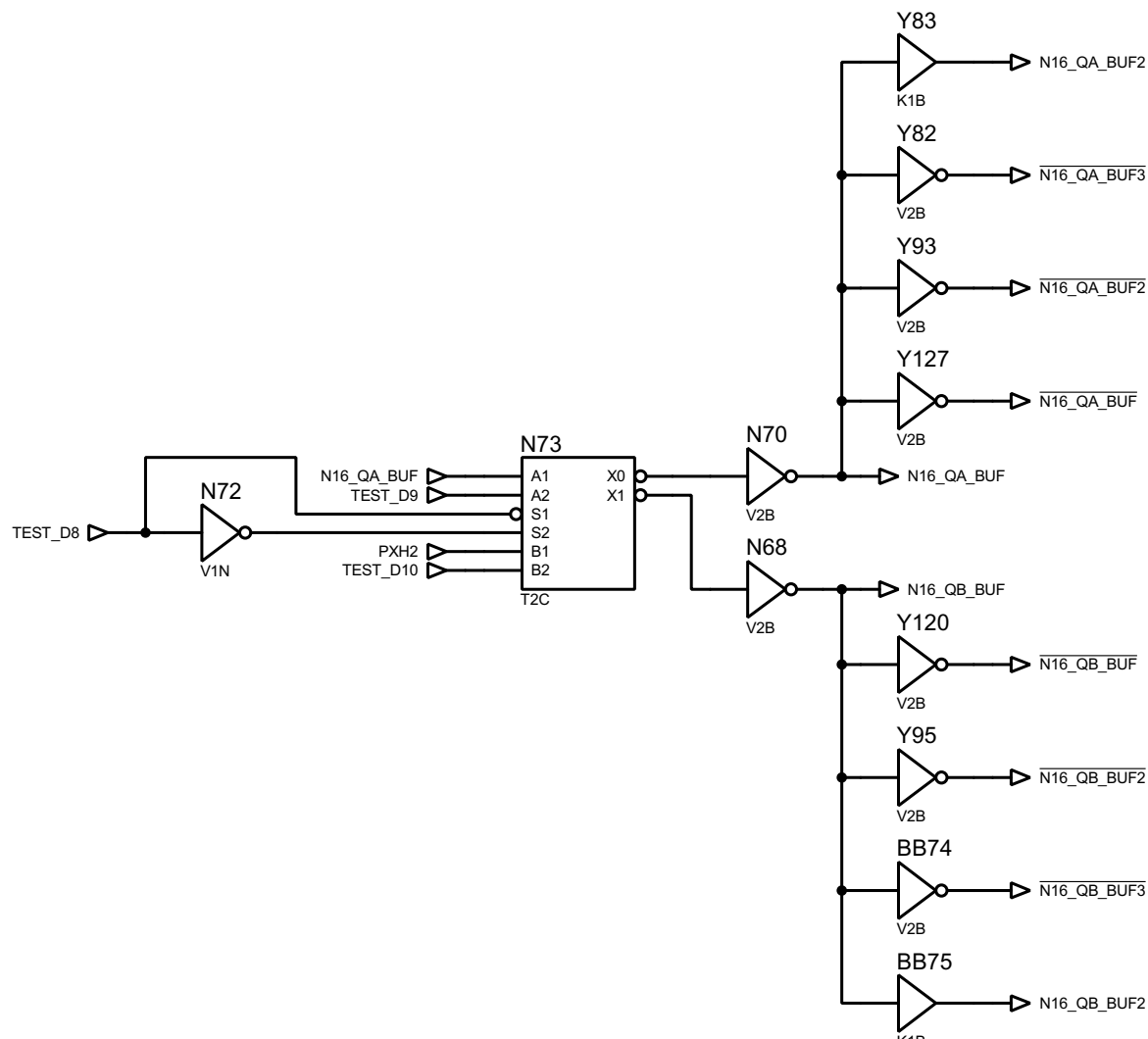
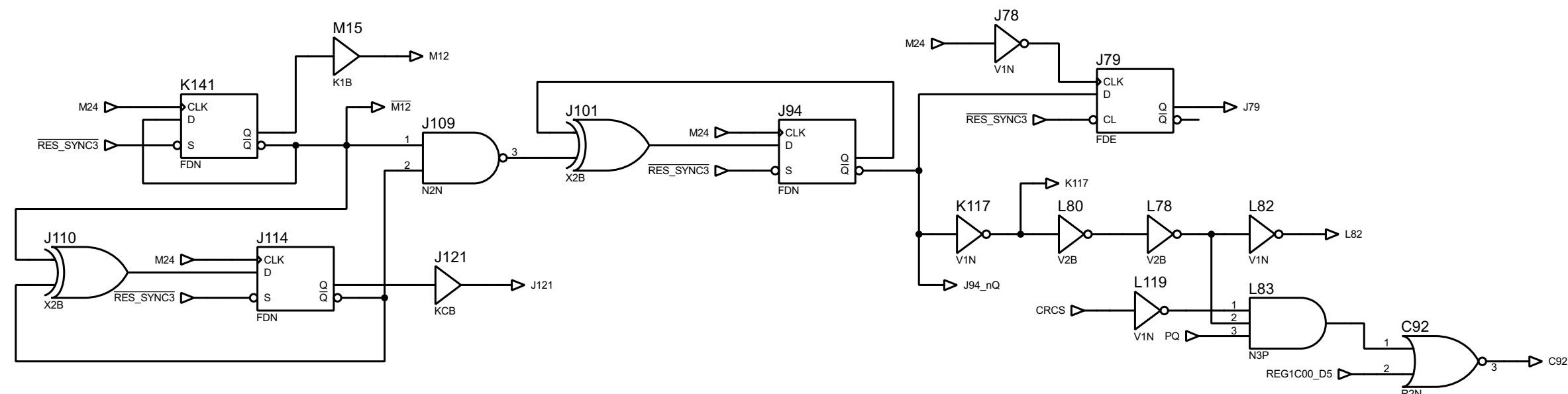
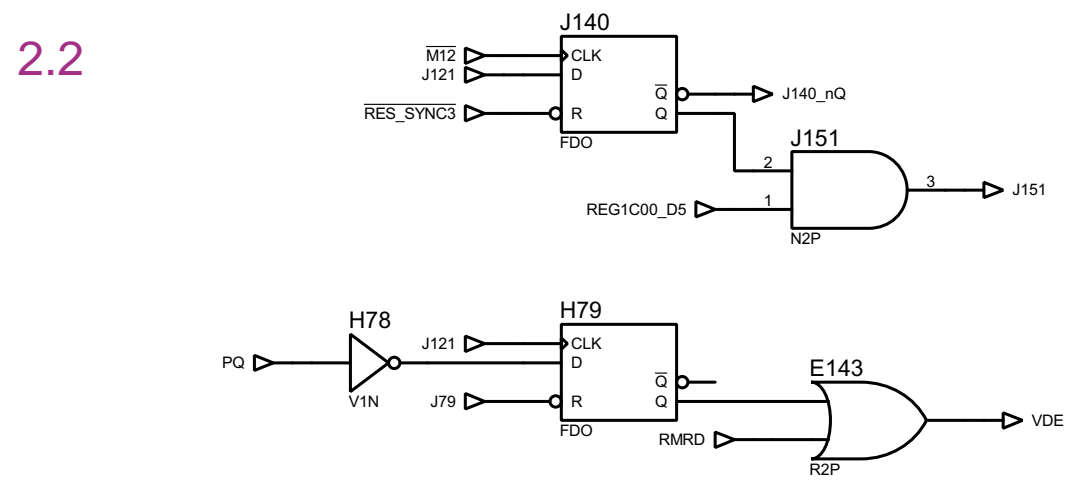


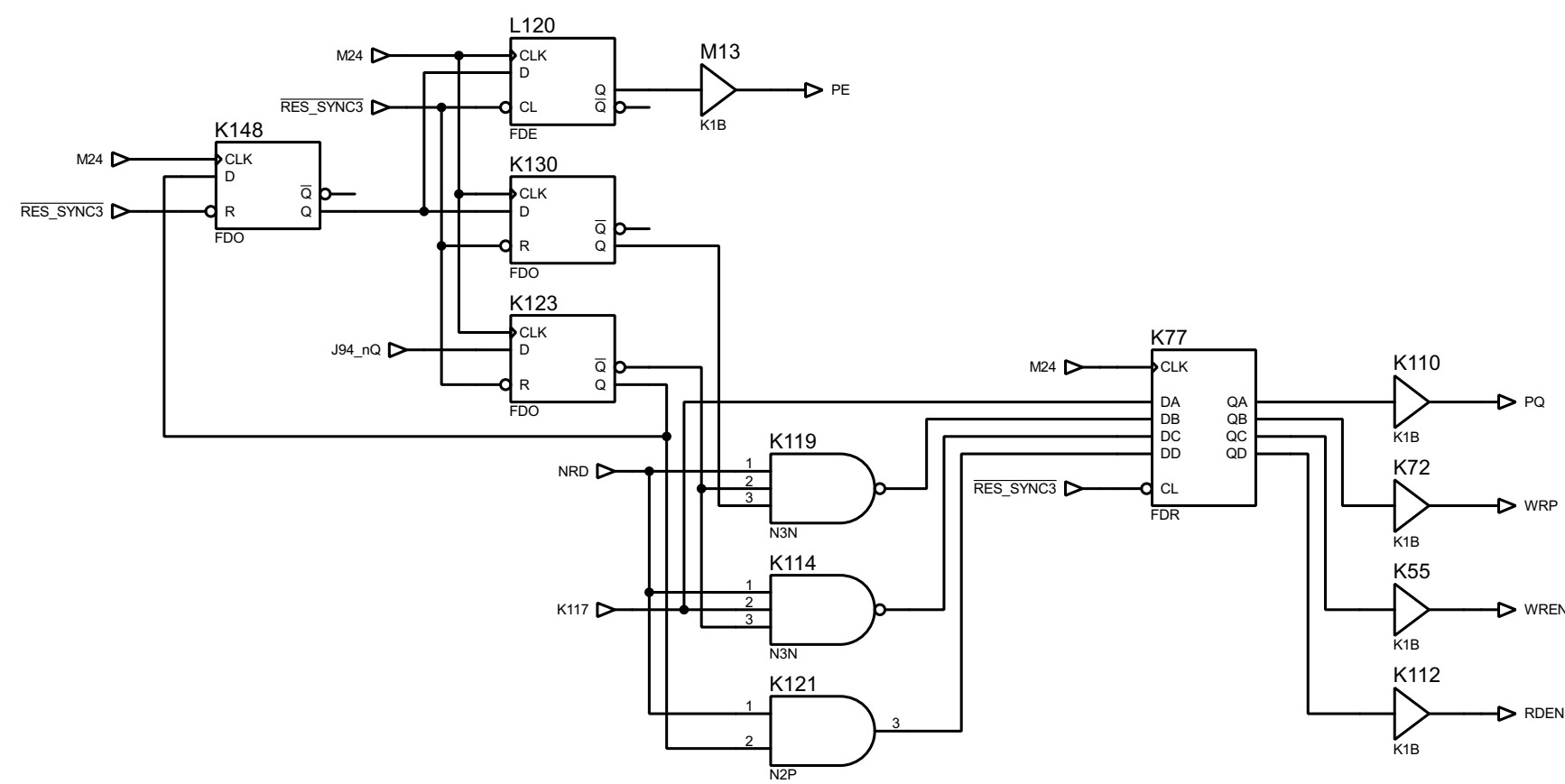
VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 00xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 1100 xxxx xxxx A Y scroll
0000 1101 xxxx xxxx A X scroll
0001 00xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 1100 xxxx xxxx B Y scroll
0001 1101 xxxx xxxx B X scroll
0001 1110 xxxx xxxx X Tilemaps X
0001 1111 xxxx xxxx Y Tilemaps Y
xx xxx Tilemaps Y



2.2



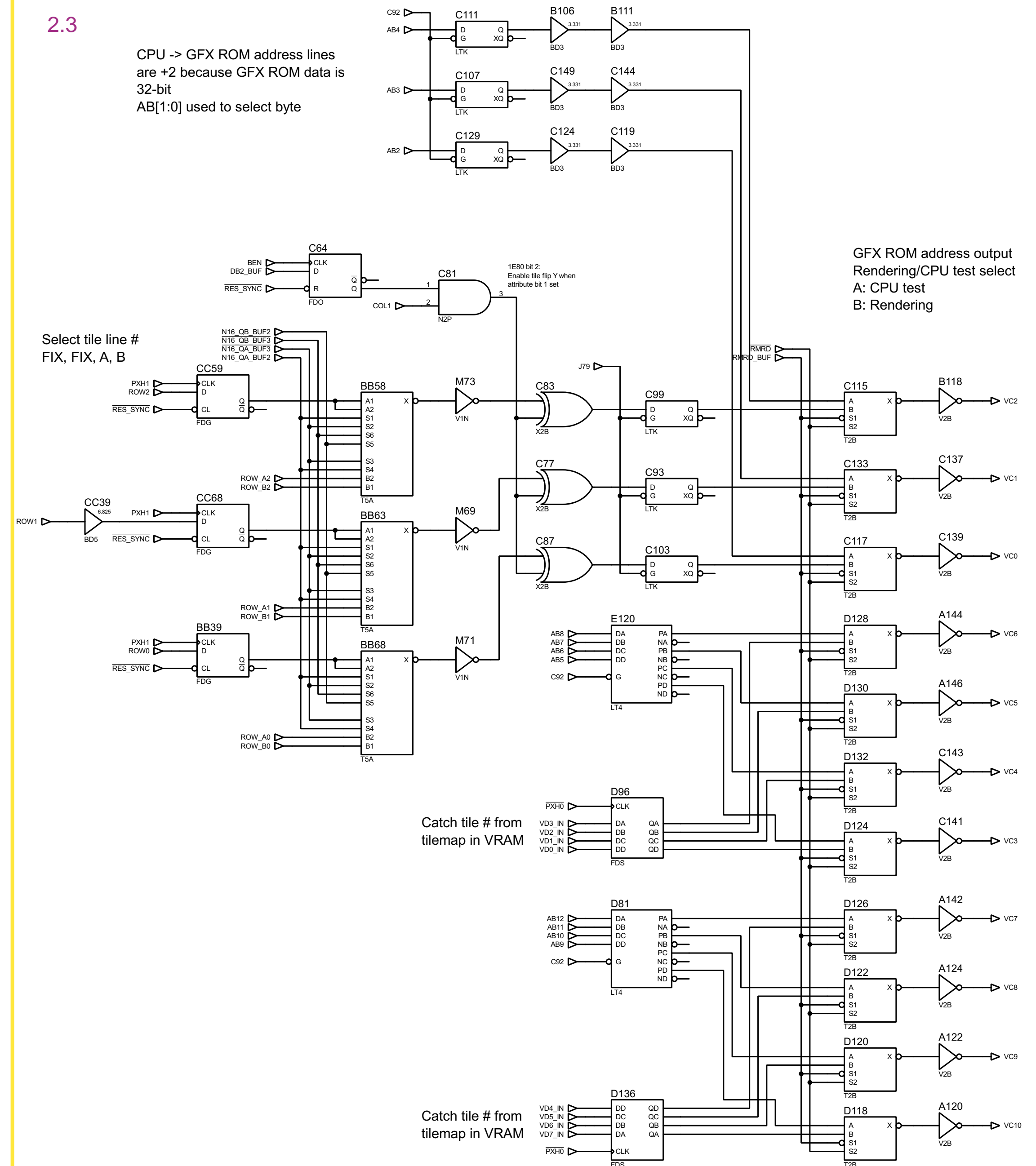
2.1



TIMING SIGNALS

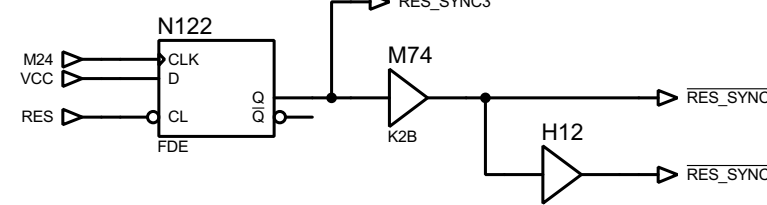
2.3

CPU -> GFX ROM address lines
are +2 because GFX ROM data is
32-bit
AB[1:0] used to select byte



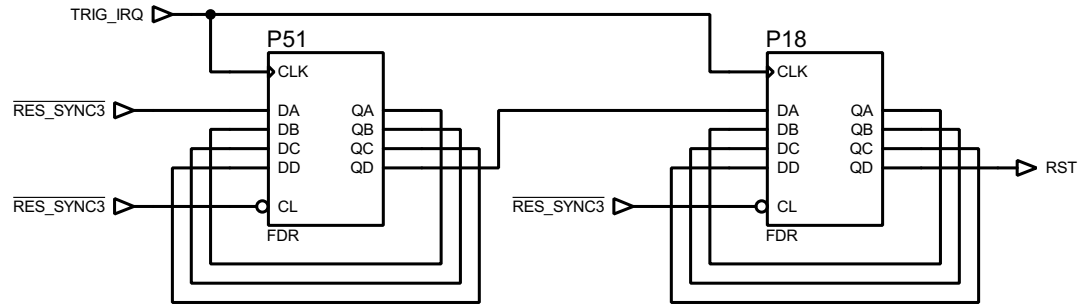
RES_SYNC signals generator

3.1

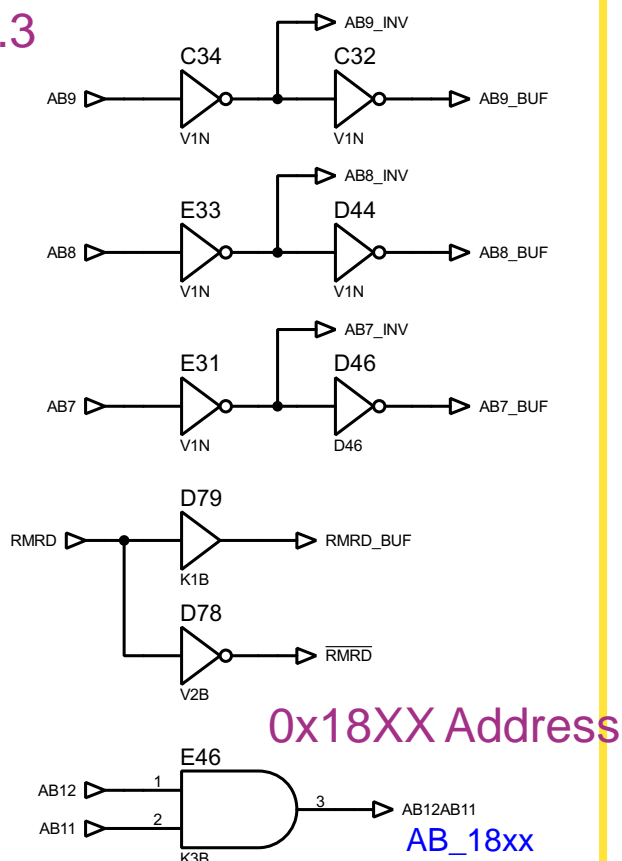


3.2

8-frame delay for
RES -> RST
Same in k051962 ?

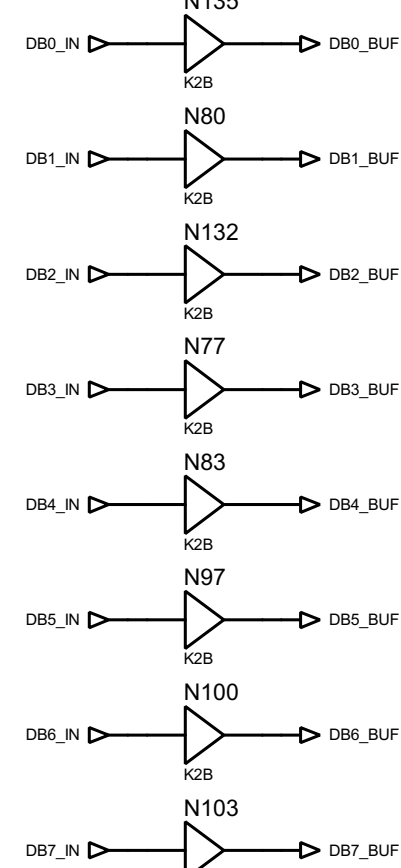


3.3



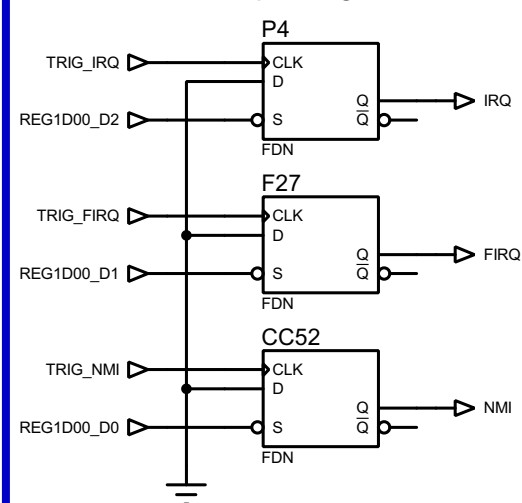
180c-1833: Layer A Y Scroll

3.4

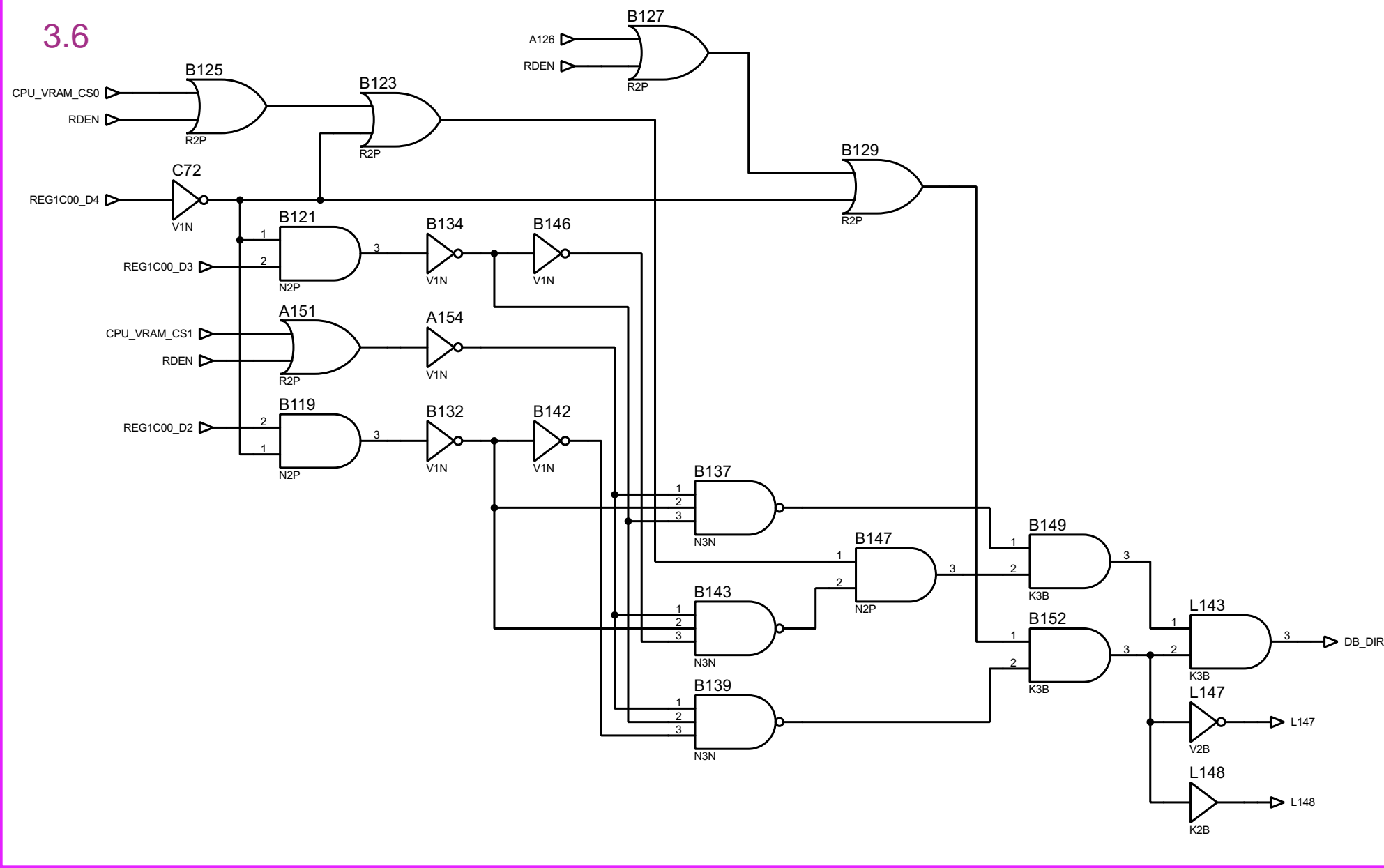


3.5

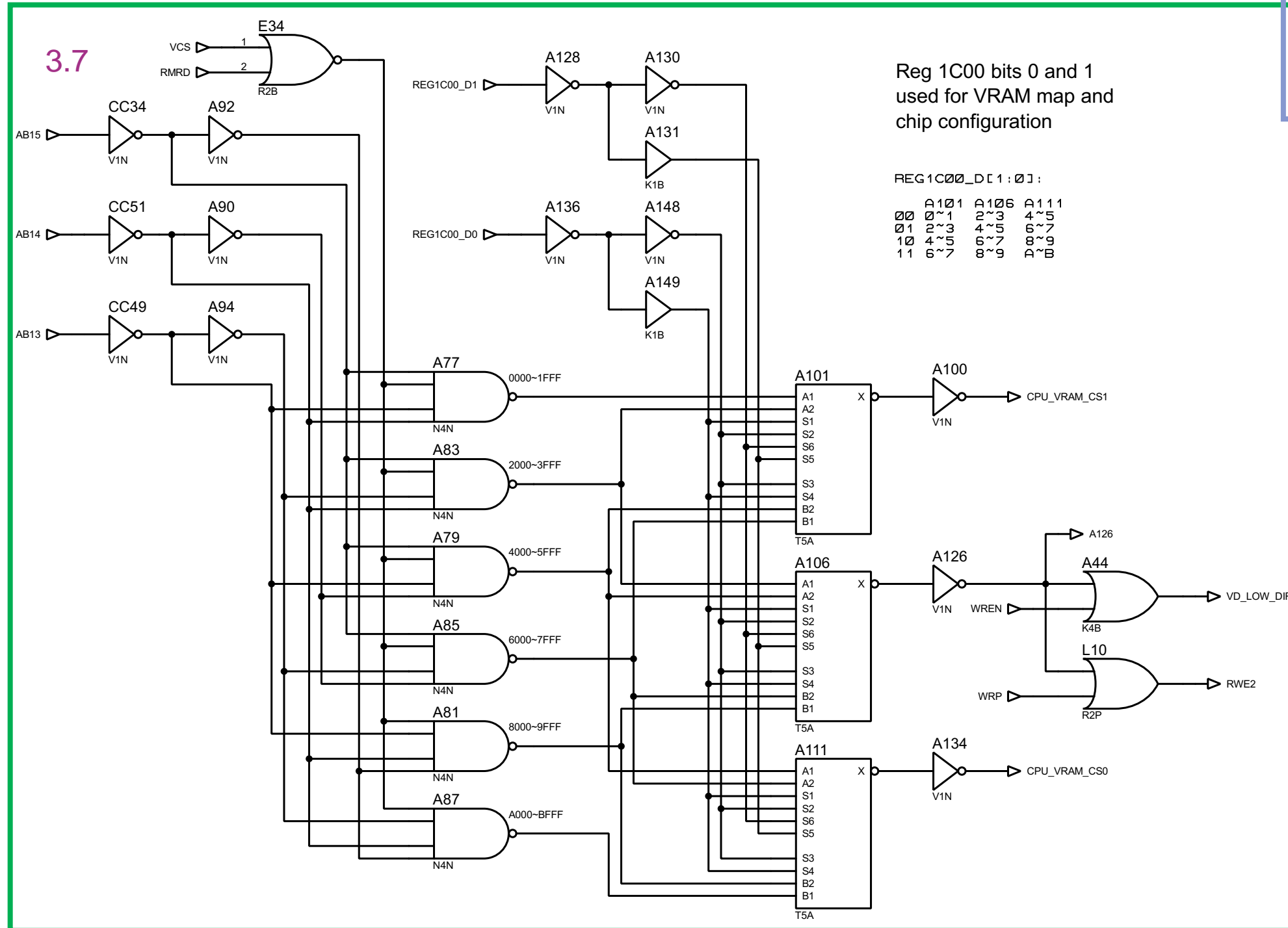
Interrupts flags



3.6



3.7

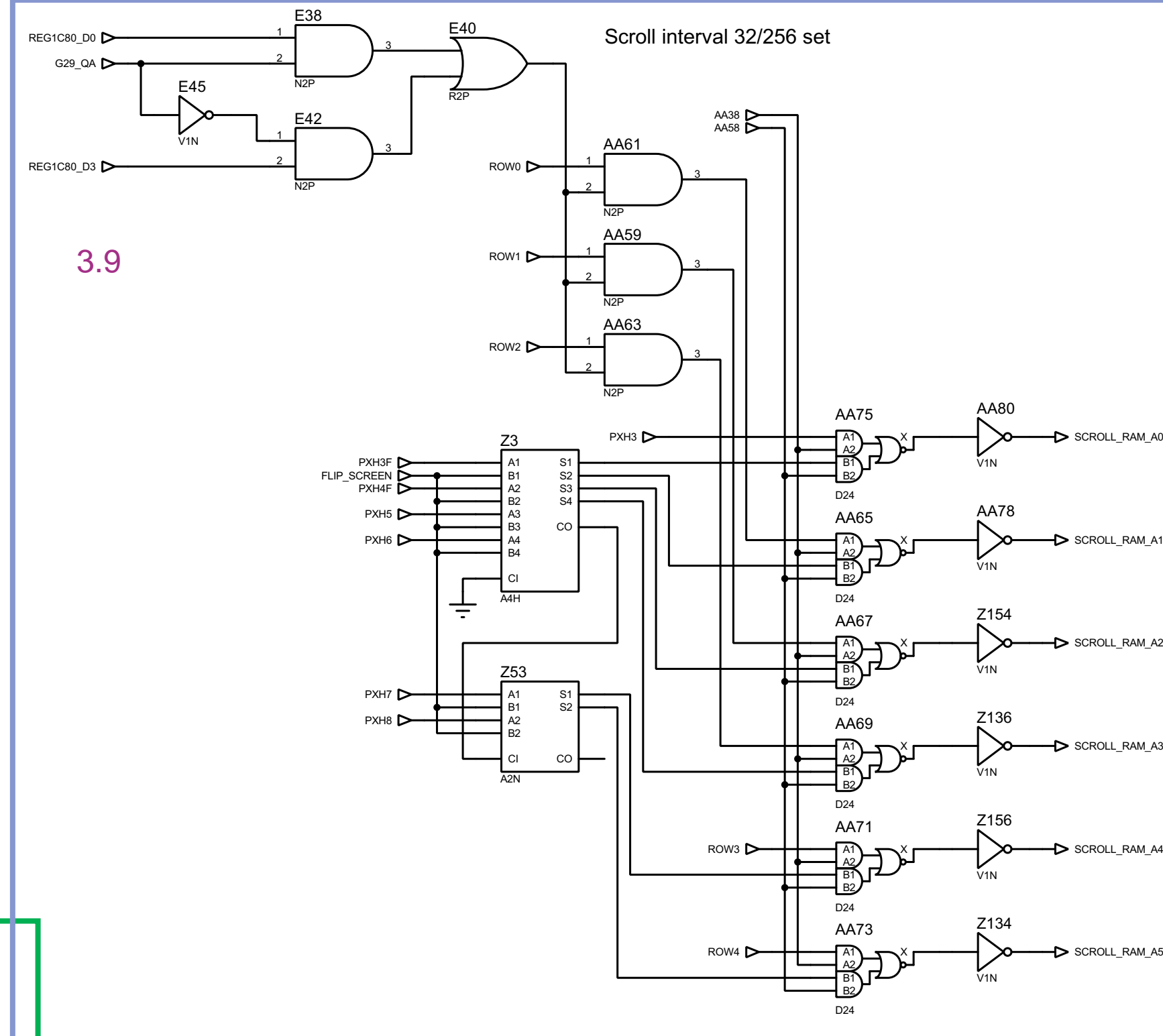


Reg 1C00 bits 0 and 1
used for VRAM map and
chip configuration

REG1C00_D[1:0] :

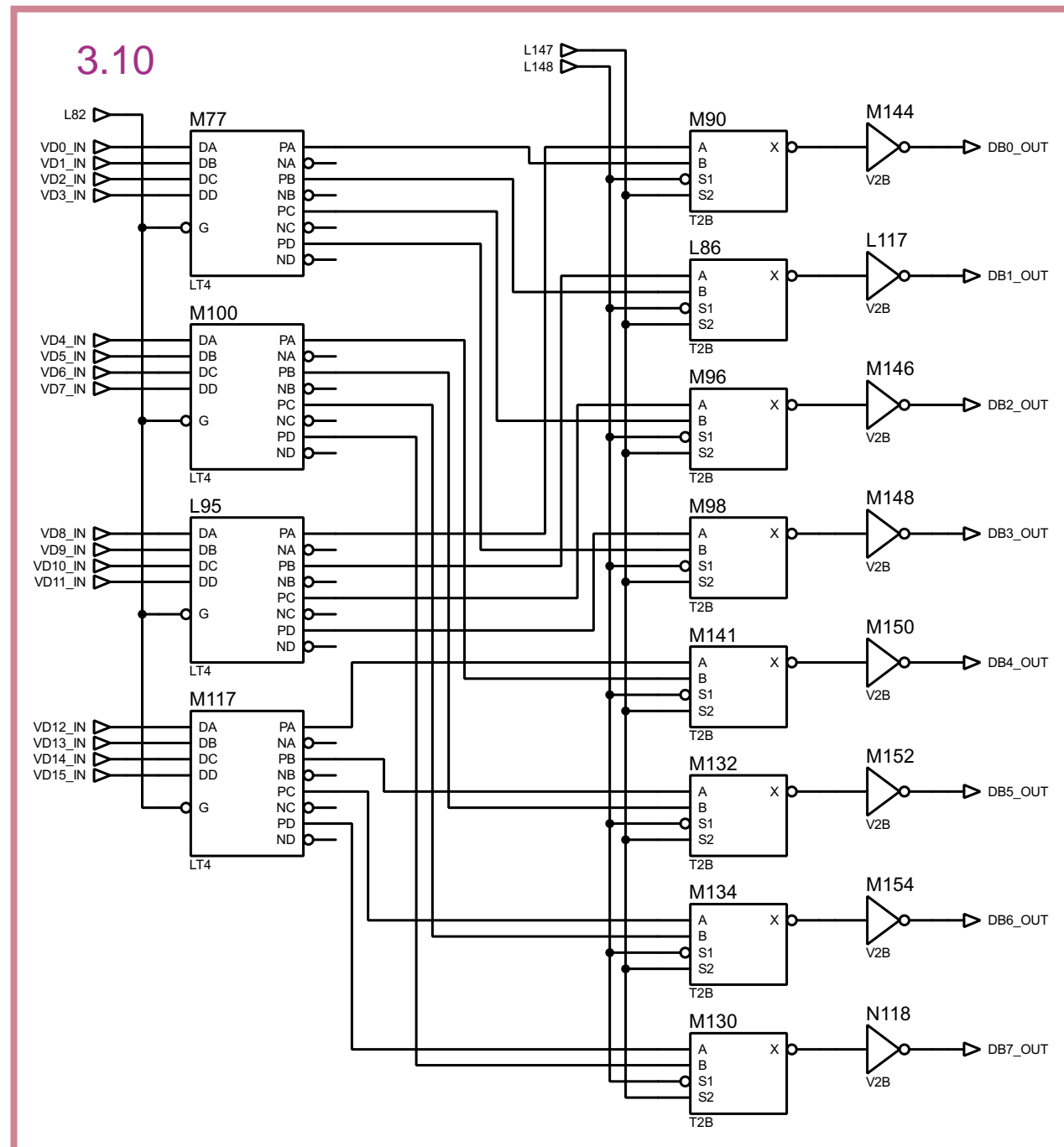
00	0~1	2~3	4~5
01	2~3	4~5	6~7
10	4~5	6~7	8~9
11	6~7	8~9	A~B

3.9

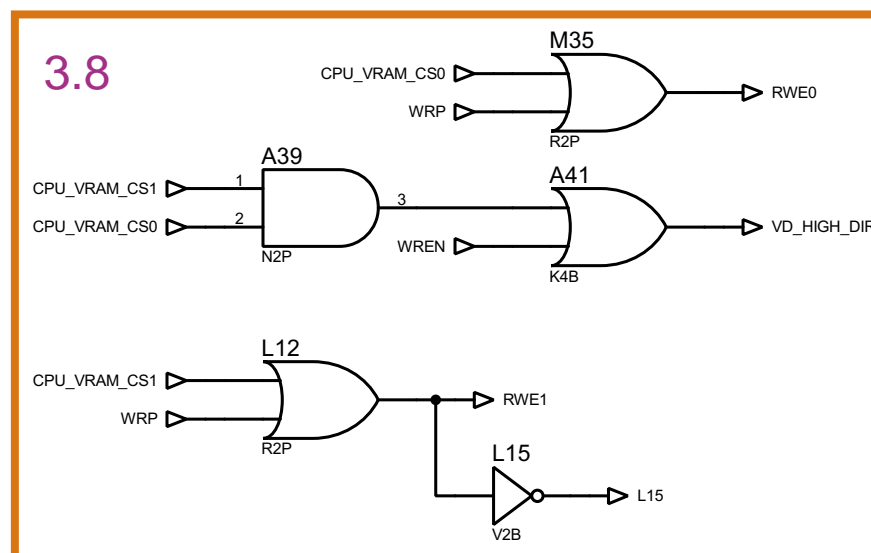


VRAM read by CPU

3.10



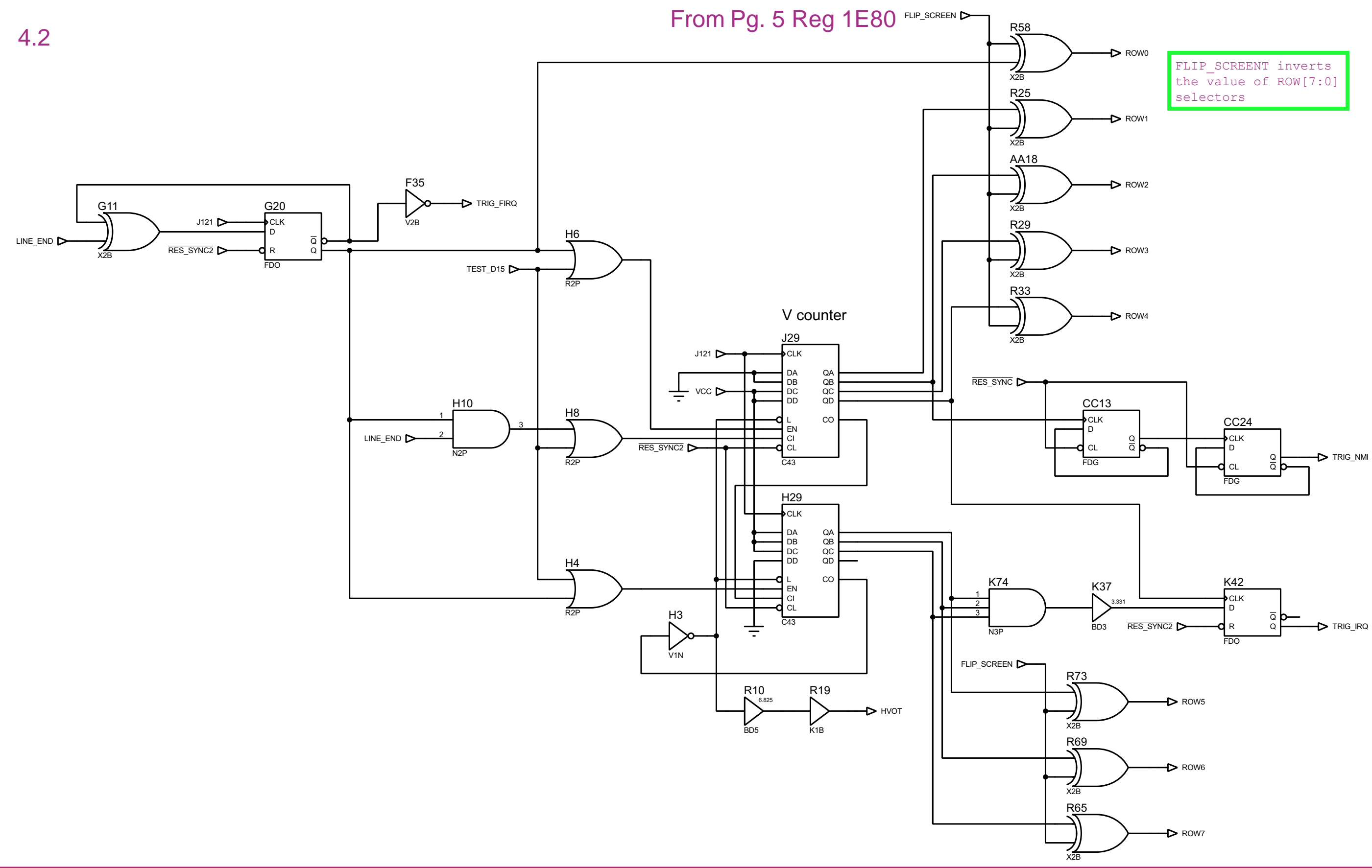
3.8



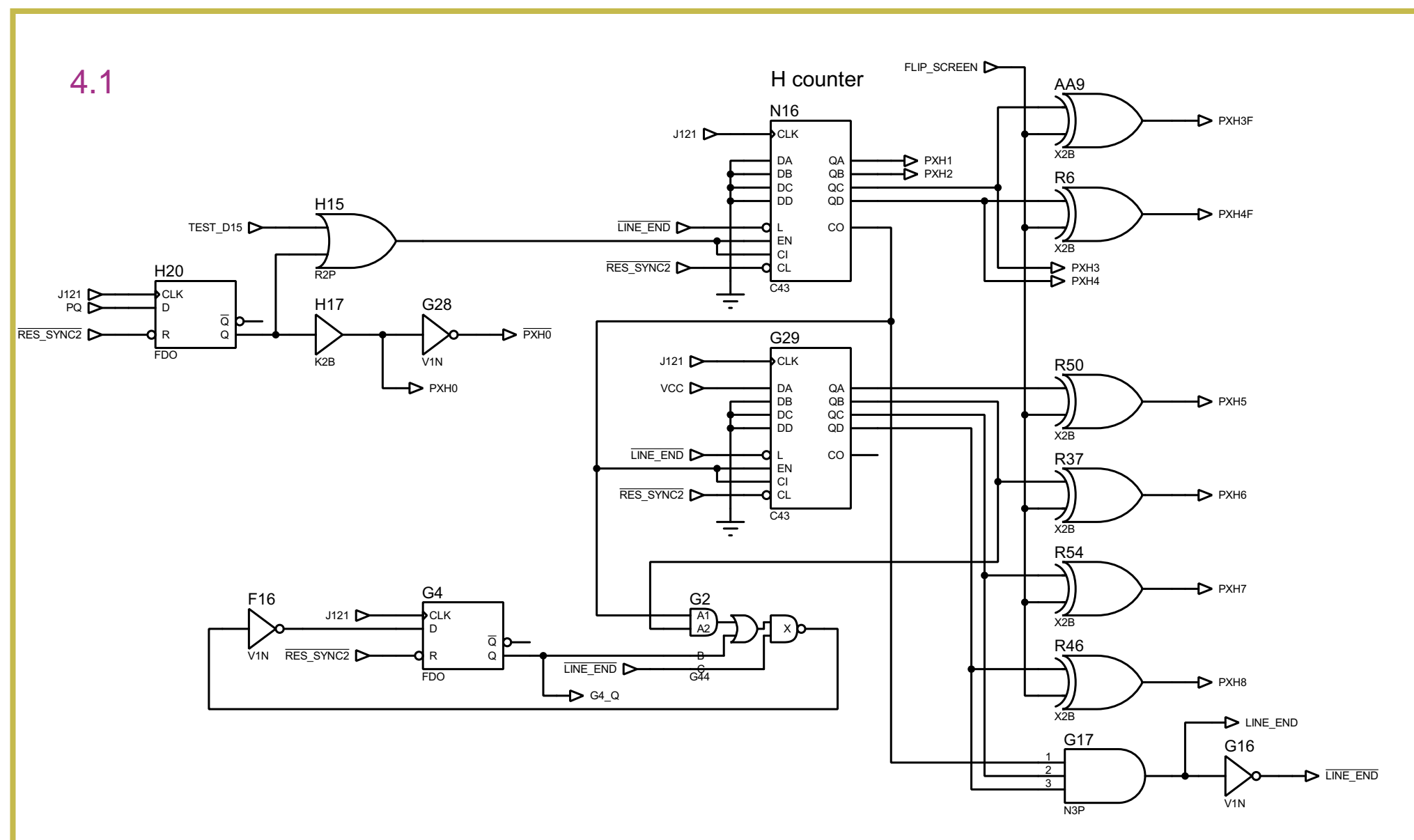
wire [7:0] DB_IN

wire [7:0] DB_BUF

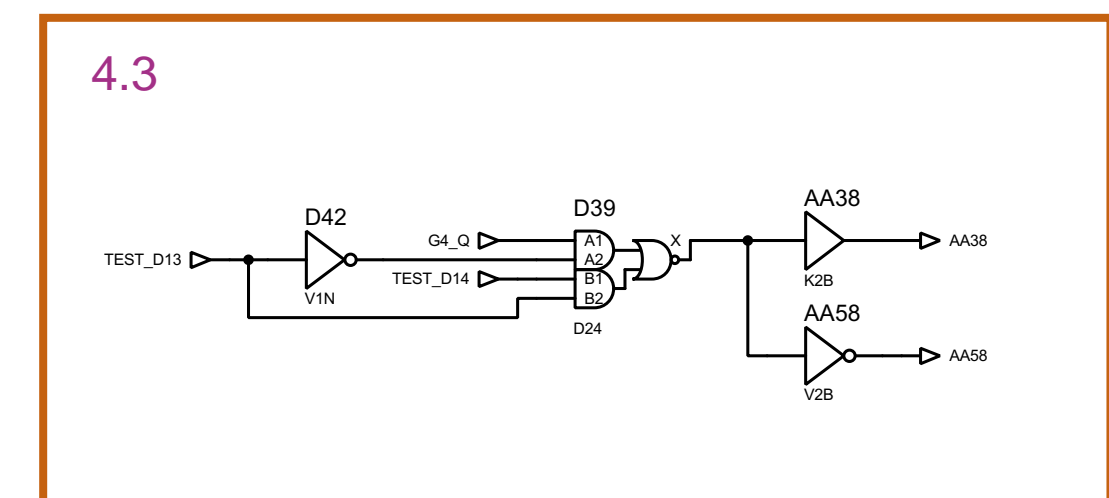
4.2



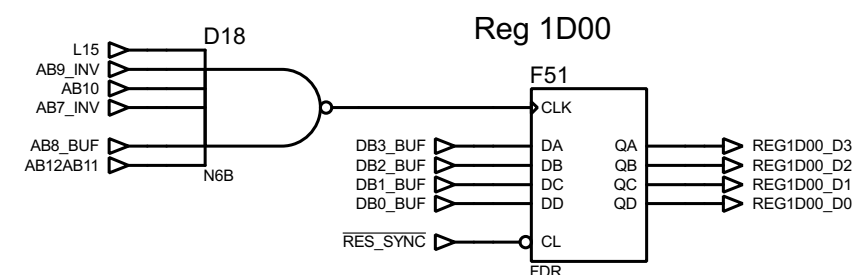
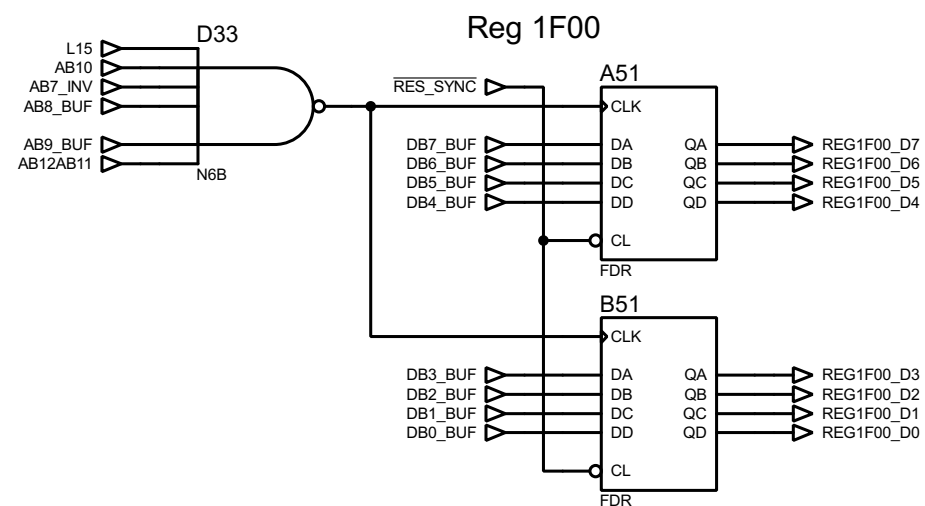
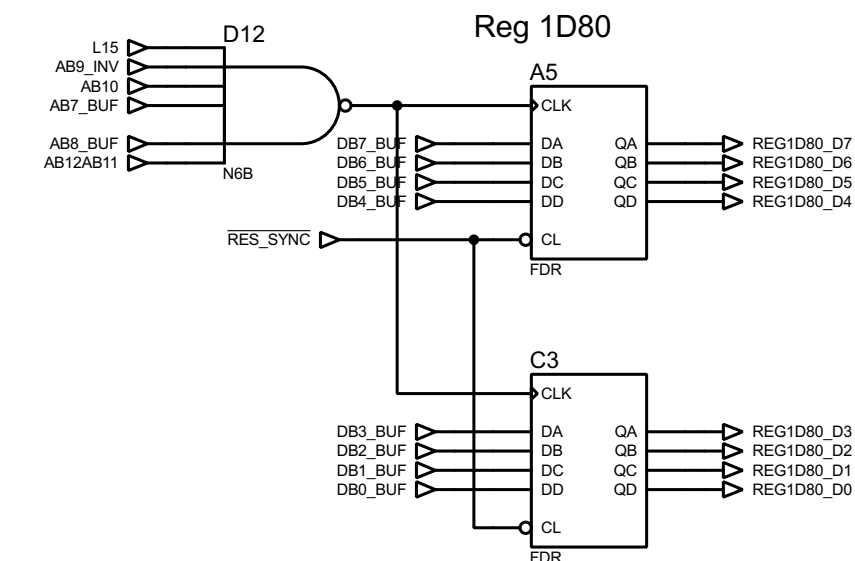
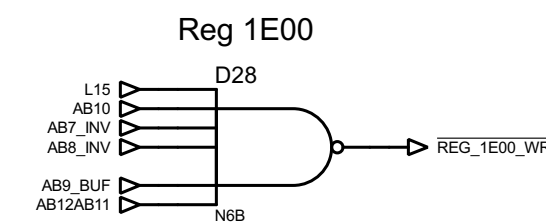
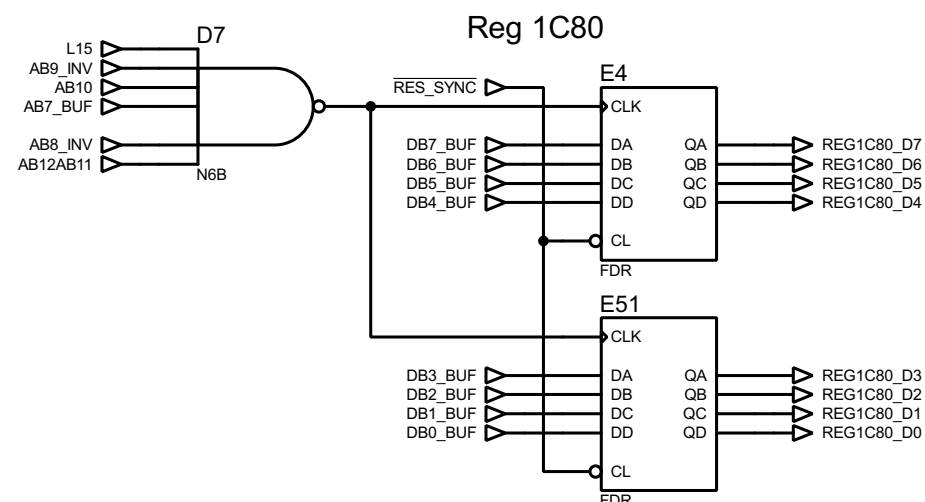
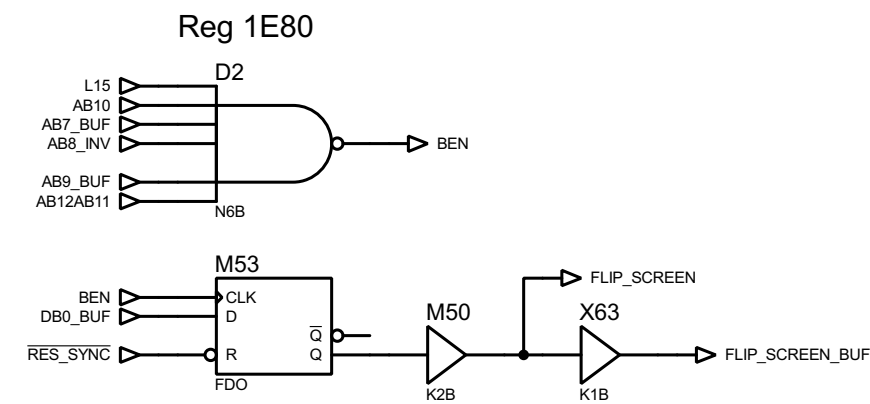
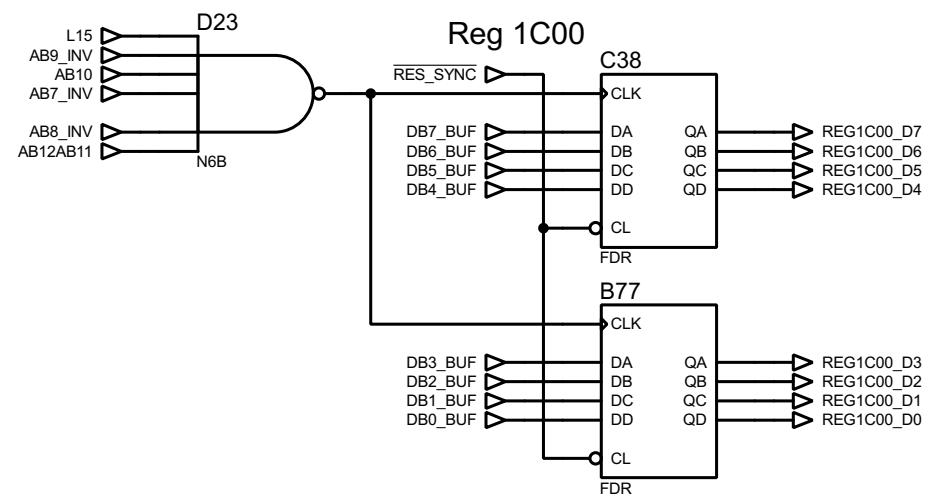
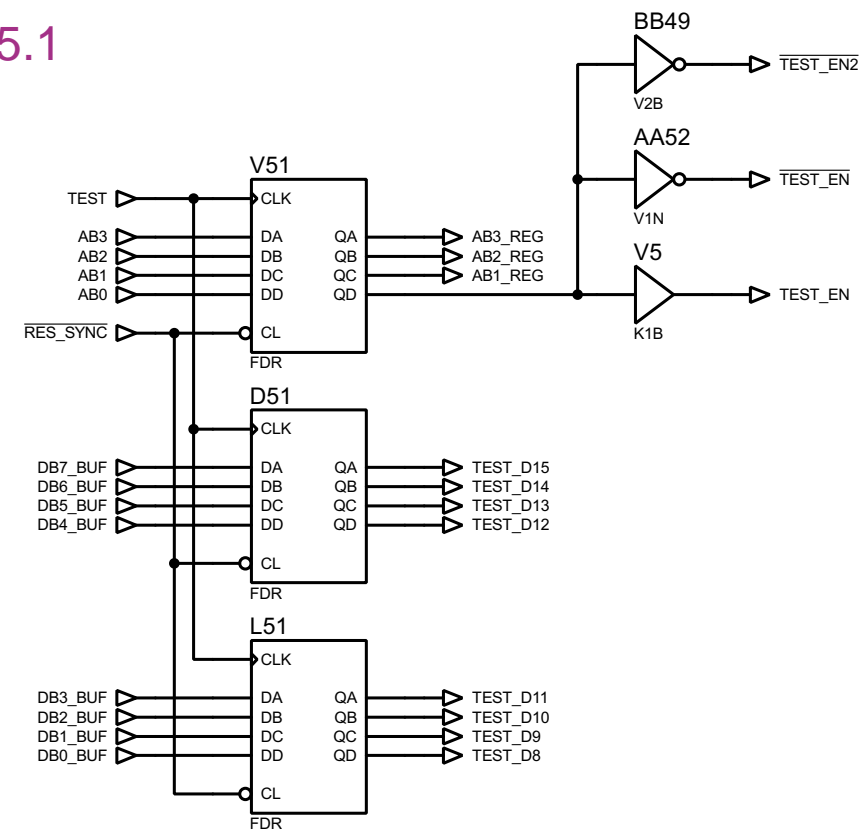
4.1

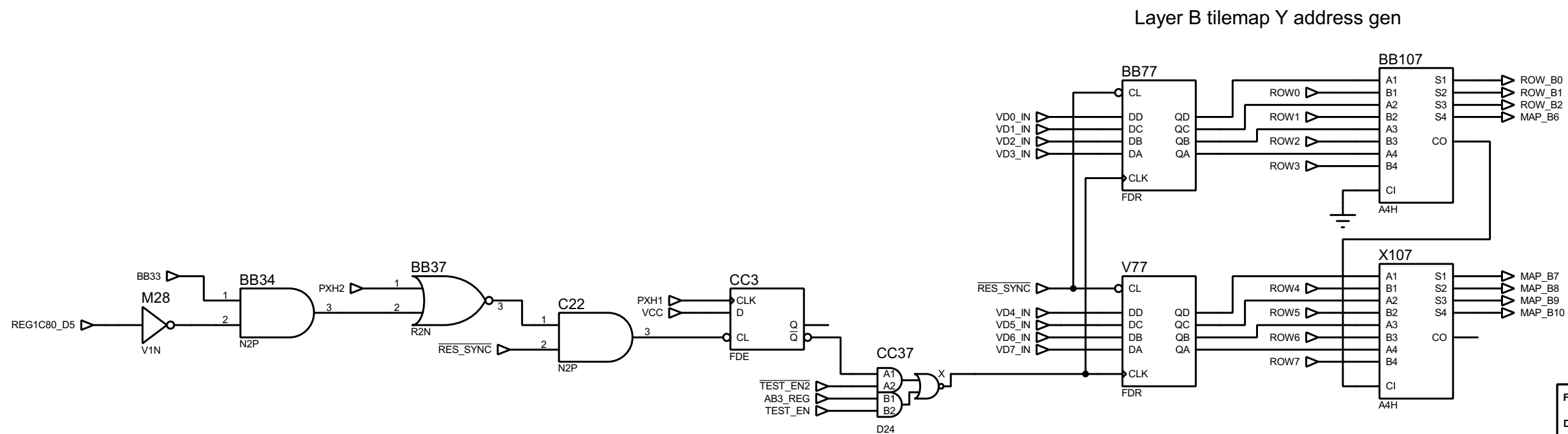
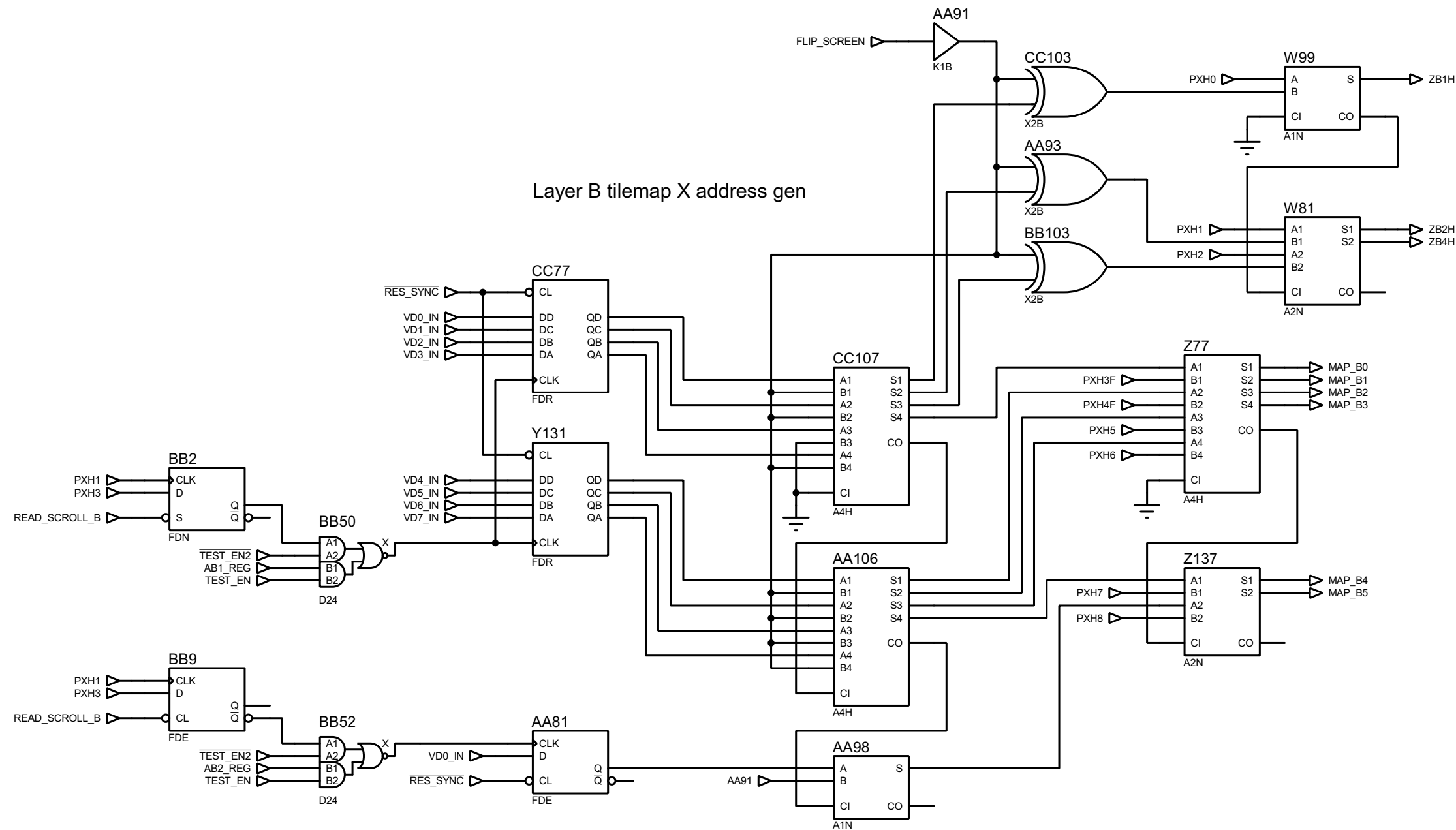


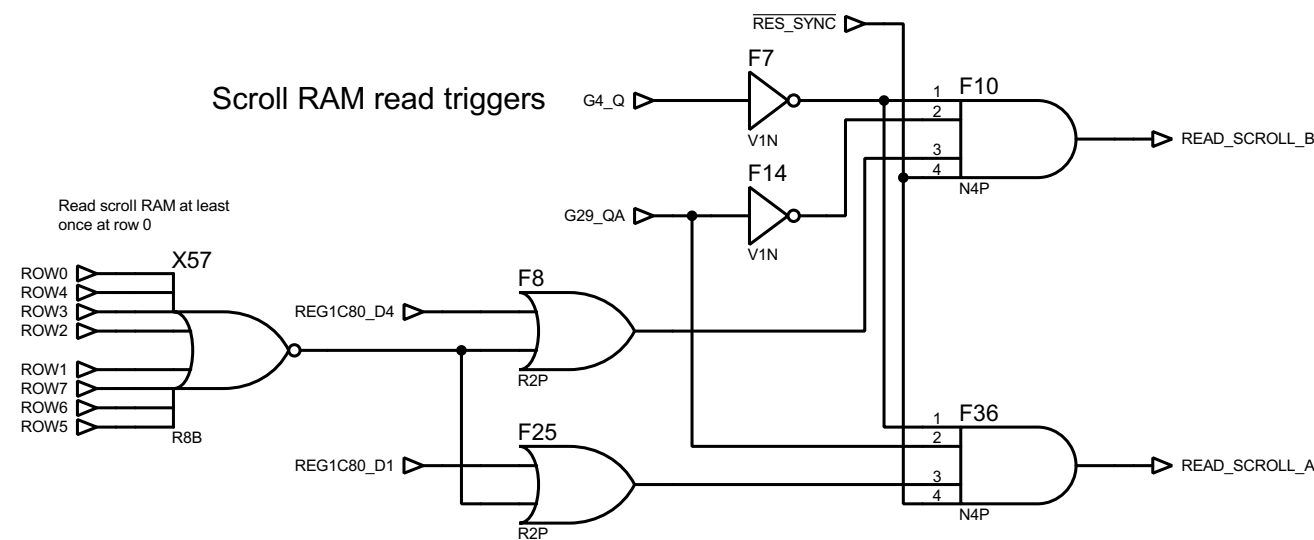
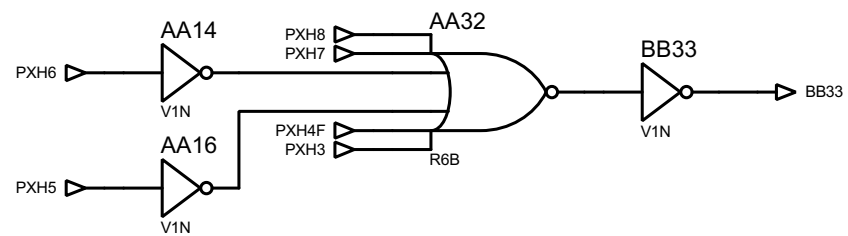
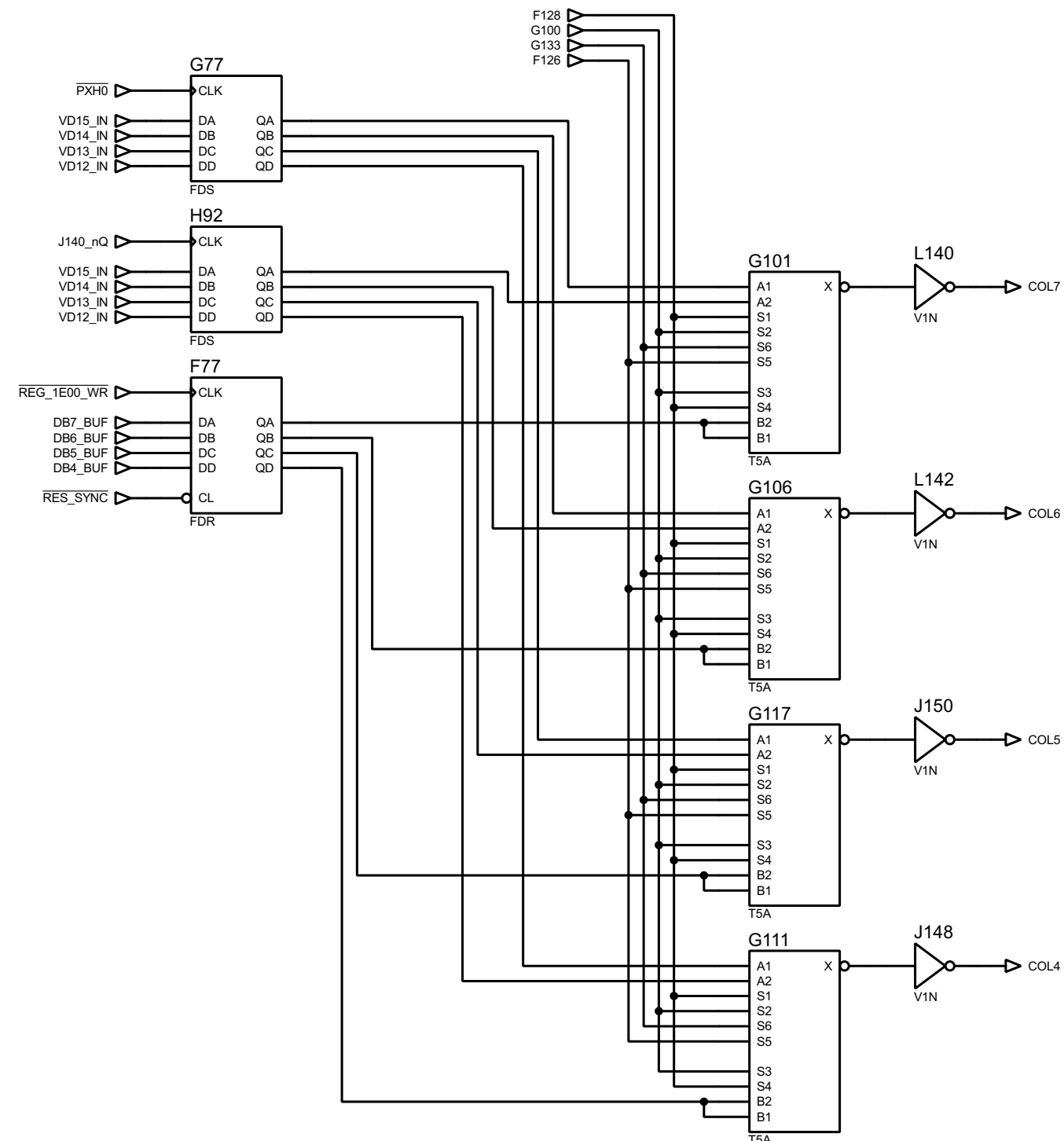
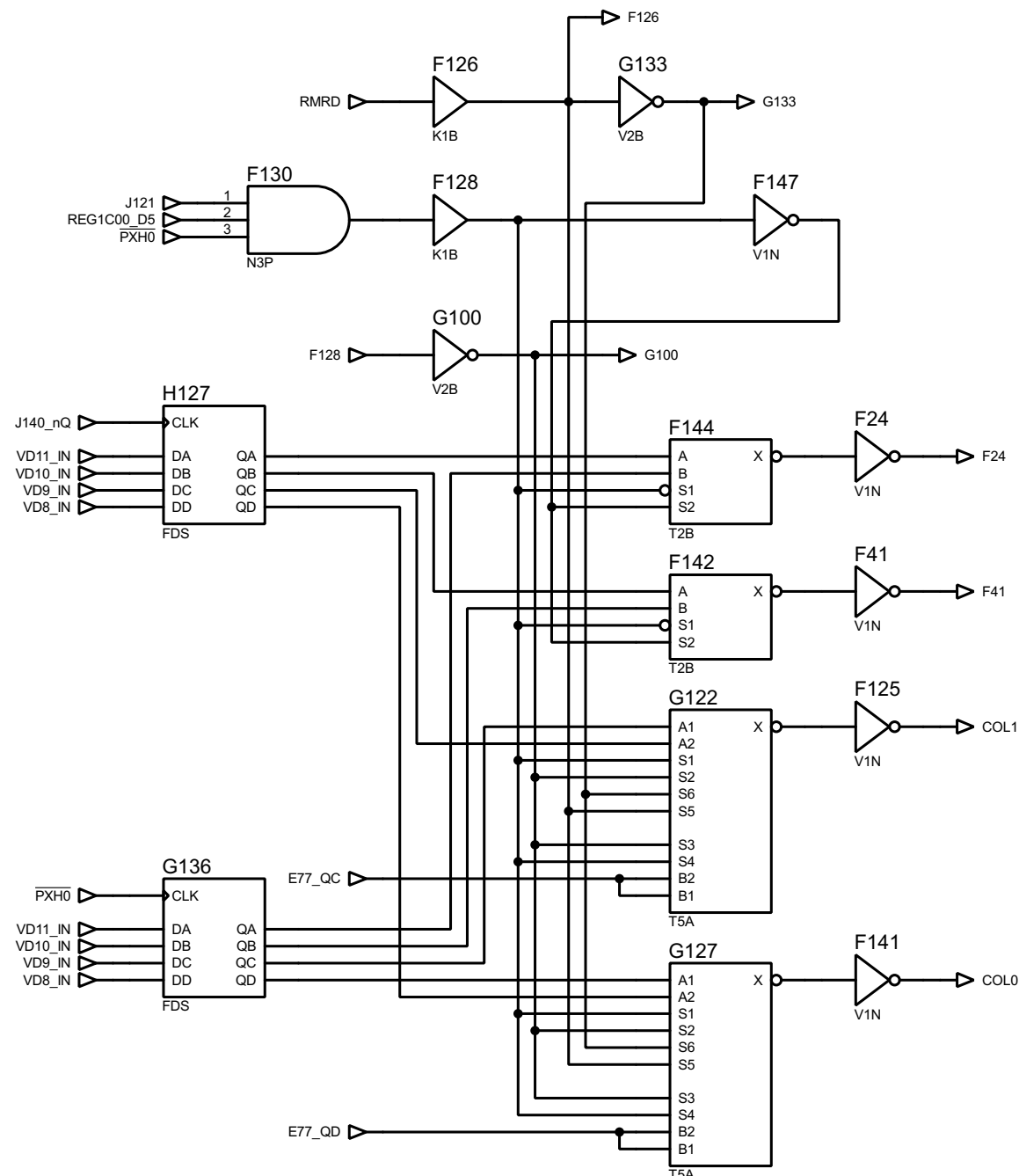
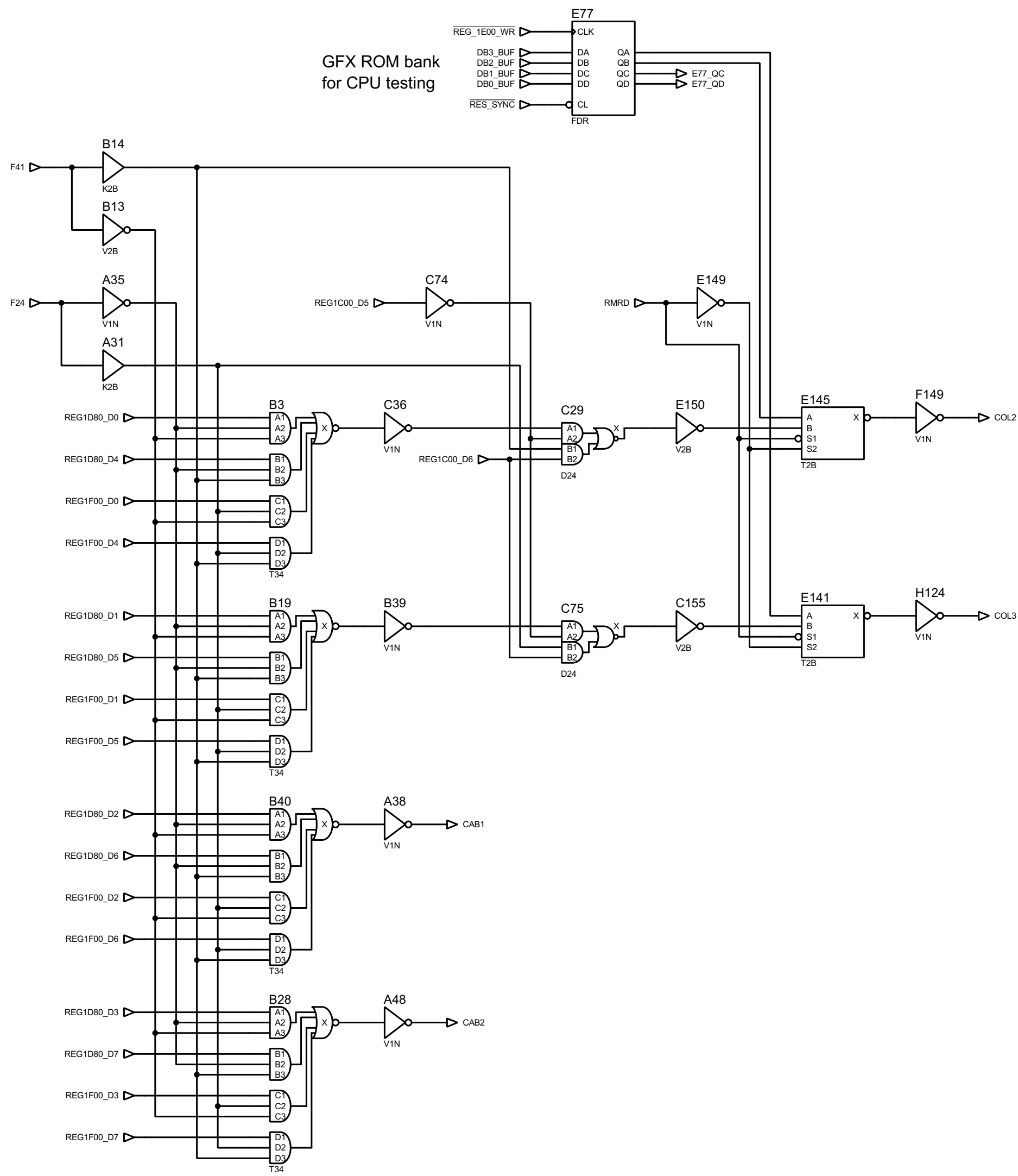
4.3



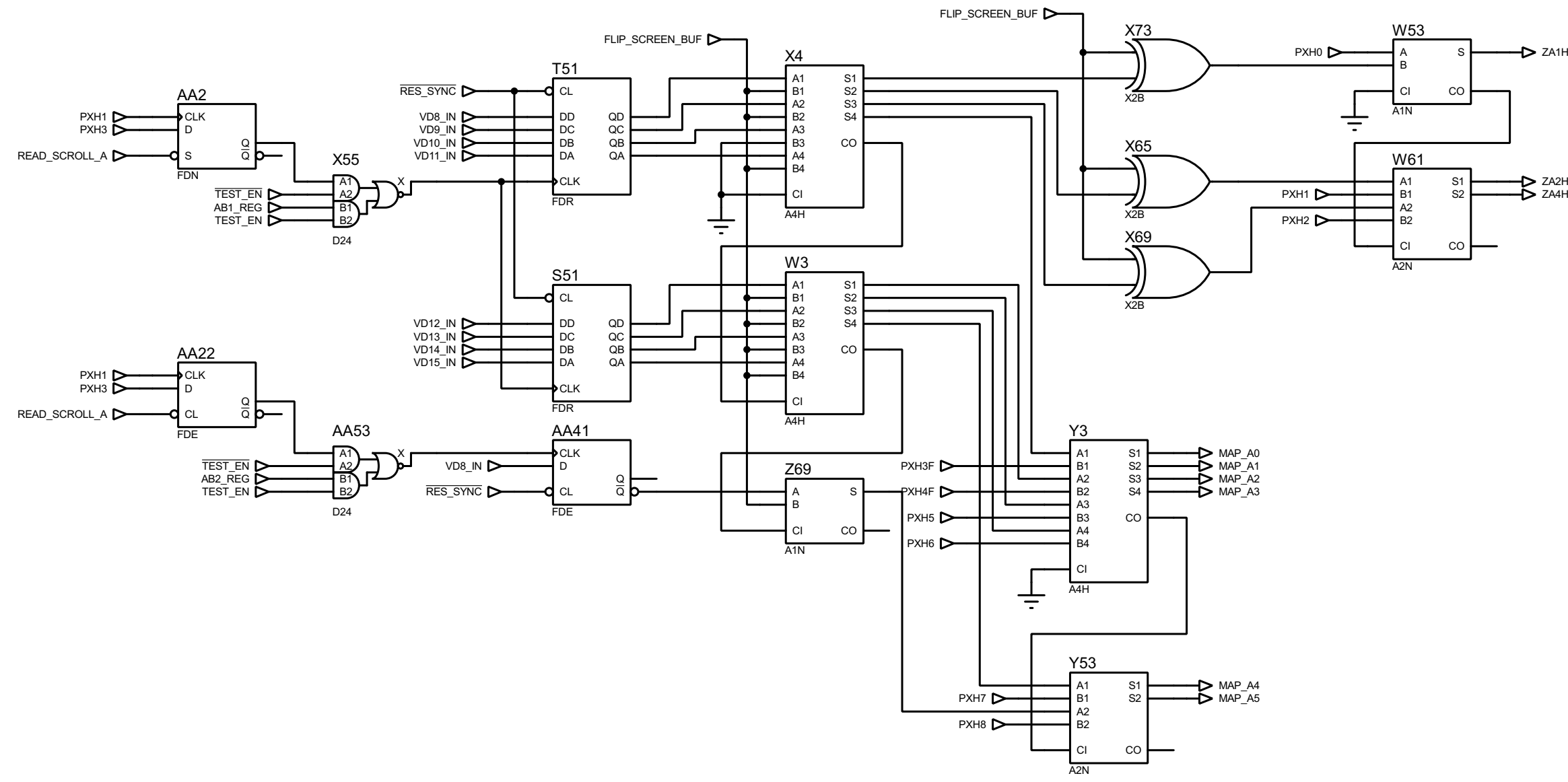
5.1







Layer A tilemap X address gen



Layer A tilemap Y address gen

