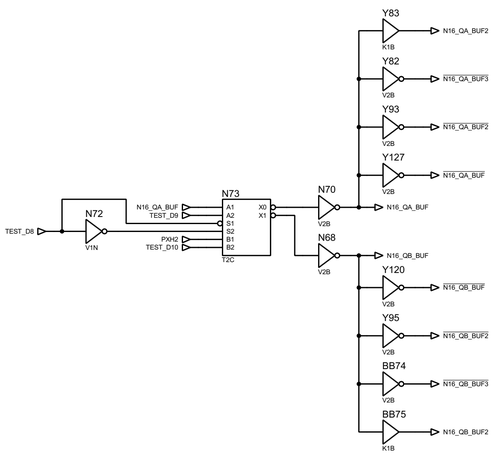
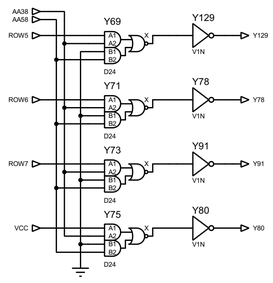
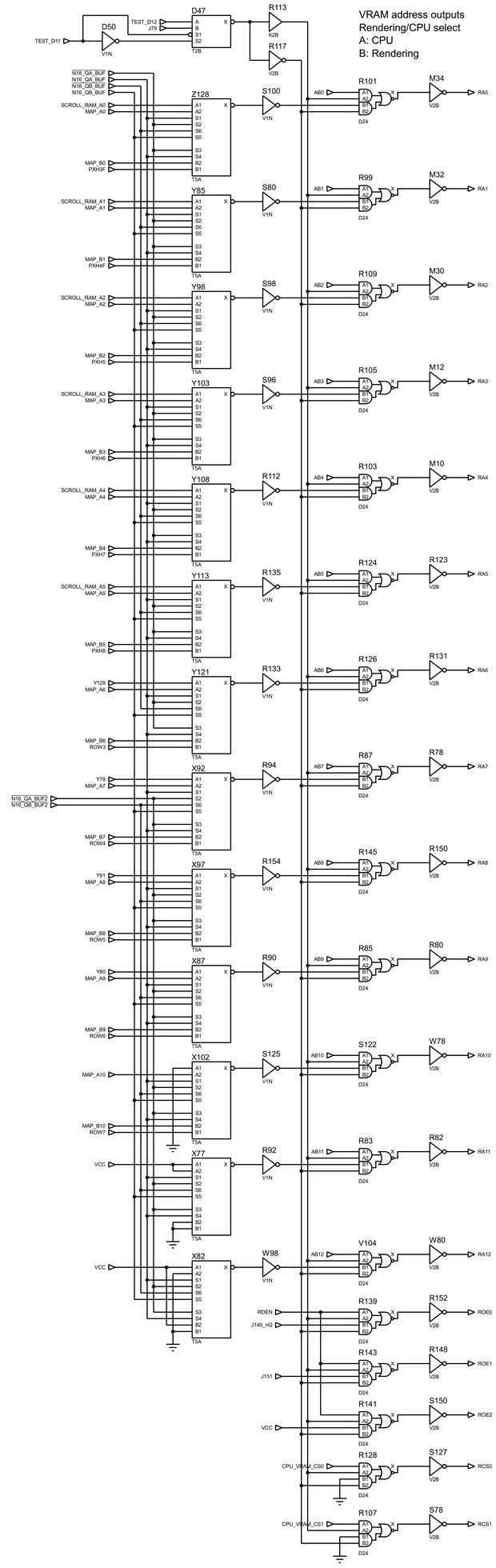
```
VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 00xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 1100 xxxx xxxx A Y scroll
0000 1101 xxxx xxxx A X scroll
0001 00xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 1100 xxxx xxxx B Y scroll
0001 1101 xxxx xxxx B X scroll
             x xxxx x Tilemaps X
          xx xxx      Tilemaps Y
```

VRAM address outputs
Rendering/CPU select
A: CPU
B: Rendering







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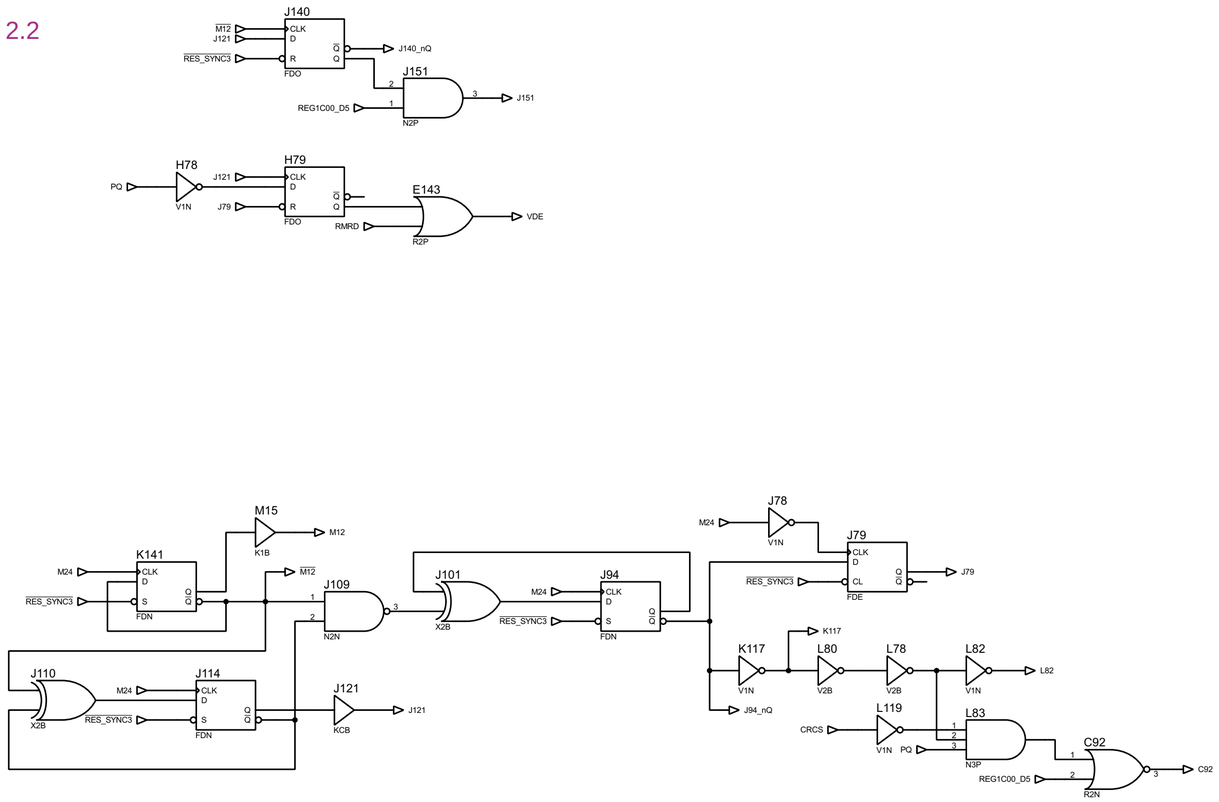
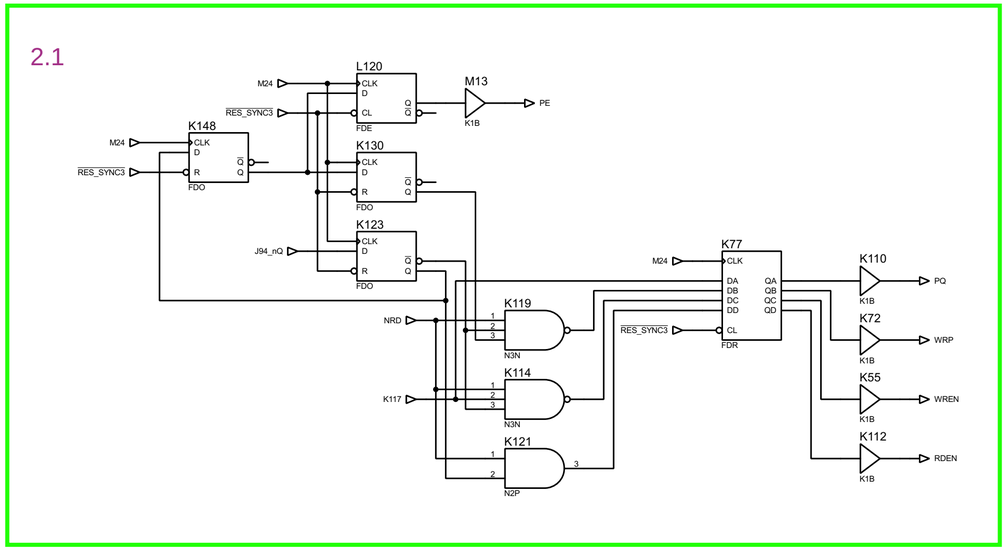
DESIGN TITLE: **Konami 052109** VRAM ADDRESS		PAGE: **1 of 8**
BY: **Sean Gonsalves**	REV: **A**	

2.2



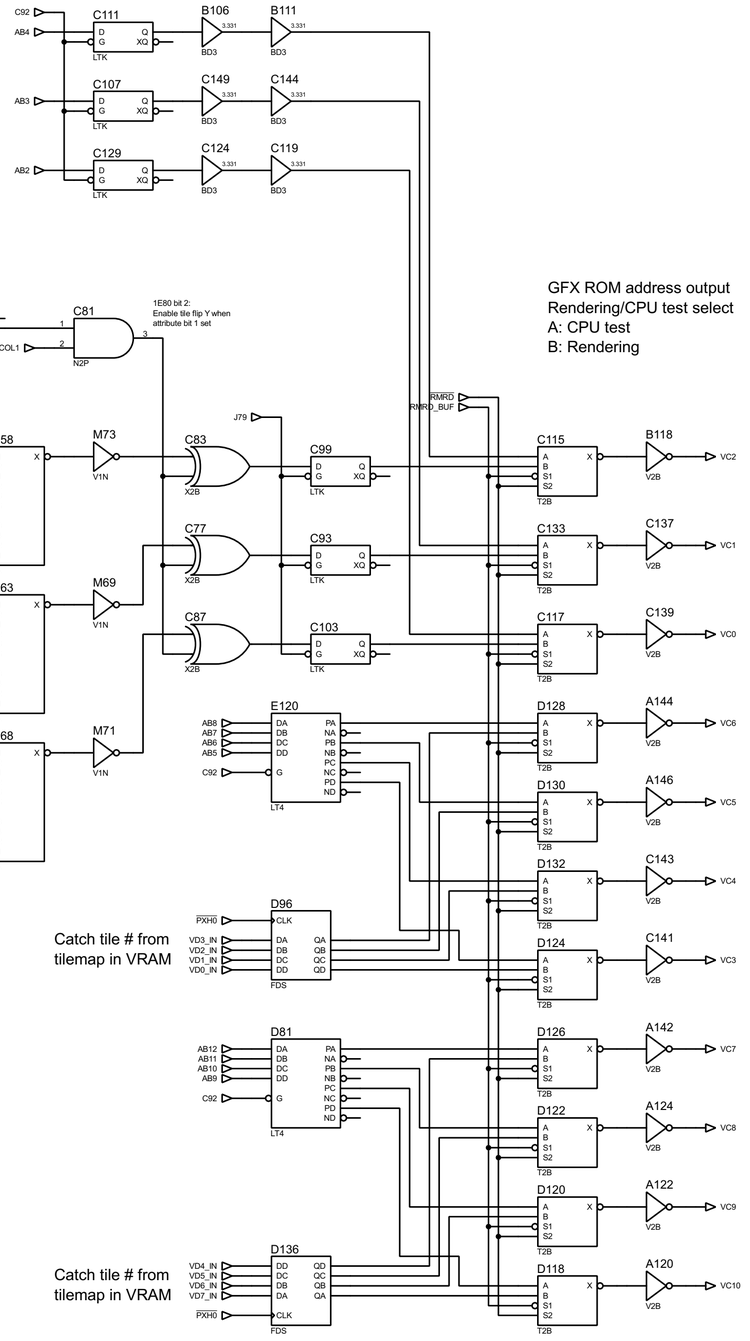
2.1



TIMING SIGNALS

2.3

CPU -> GFX ROM address lines
are +2 because GFX ROM data is
32-bit
AB[1:0] used to select byte



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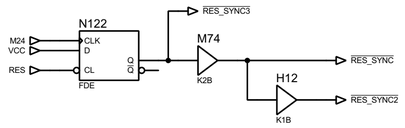
DESIGN TITLE: Konami 052109 GFX ROM ADDRESS		PAGE: 2 of 8
BY: Sean Gonsalves	REV: A	

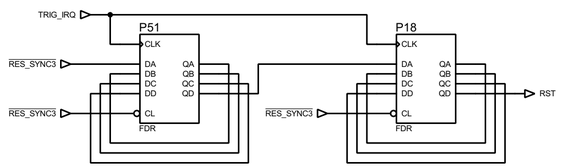
RES_SYNC signals generator

3.1

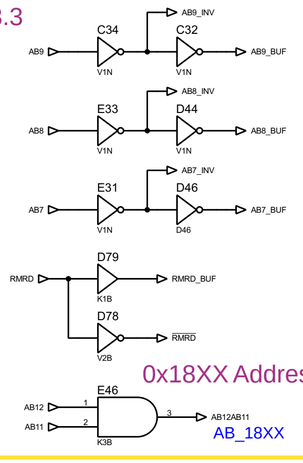


3.2

8-frame delay for
RES -> RST
Same in k051962 ?



3.3

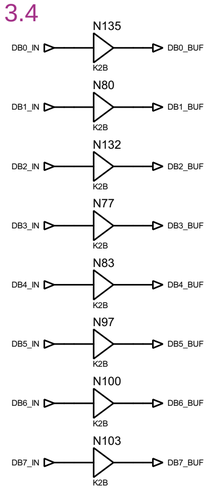


0x18XX Address

AB_18XX

180c-1833: Layer A Y Scroll

3.4

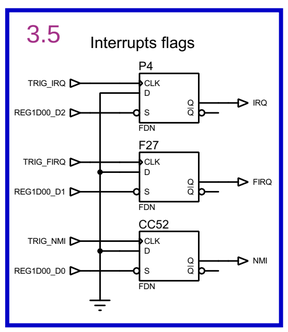


wire [7:0] DB_IN

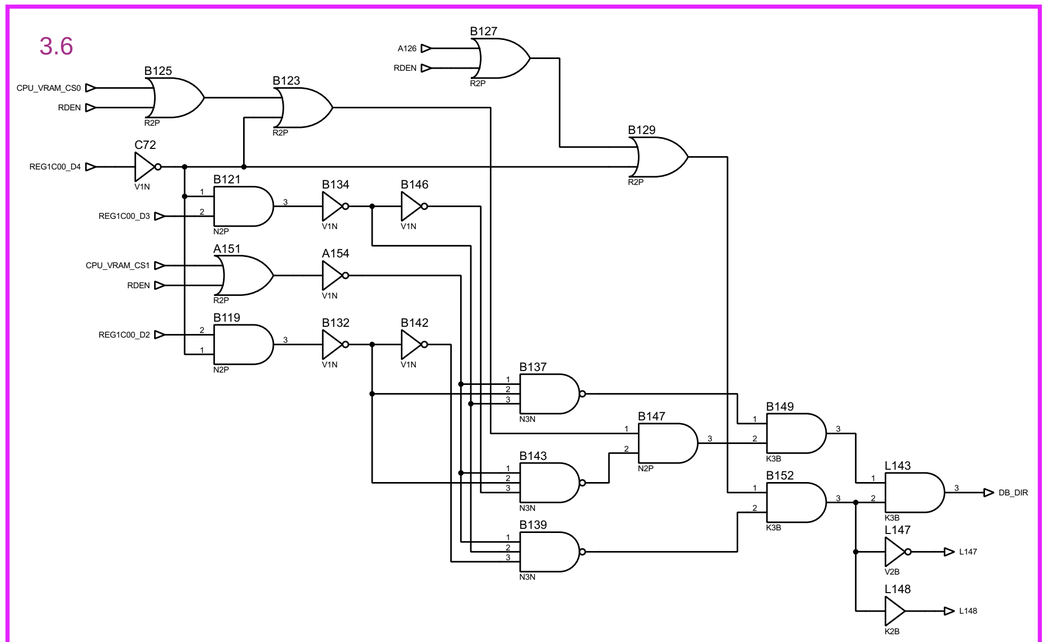
wire [7:0] DB_BUF

3.5

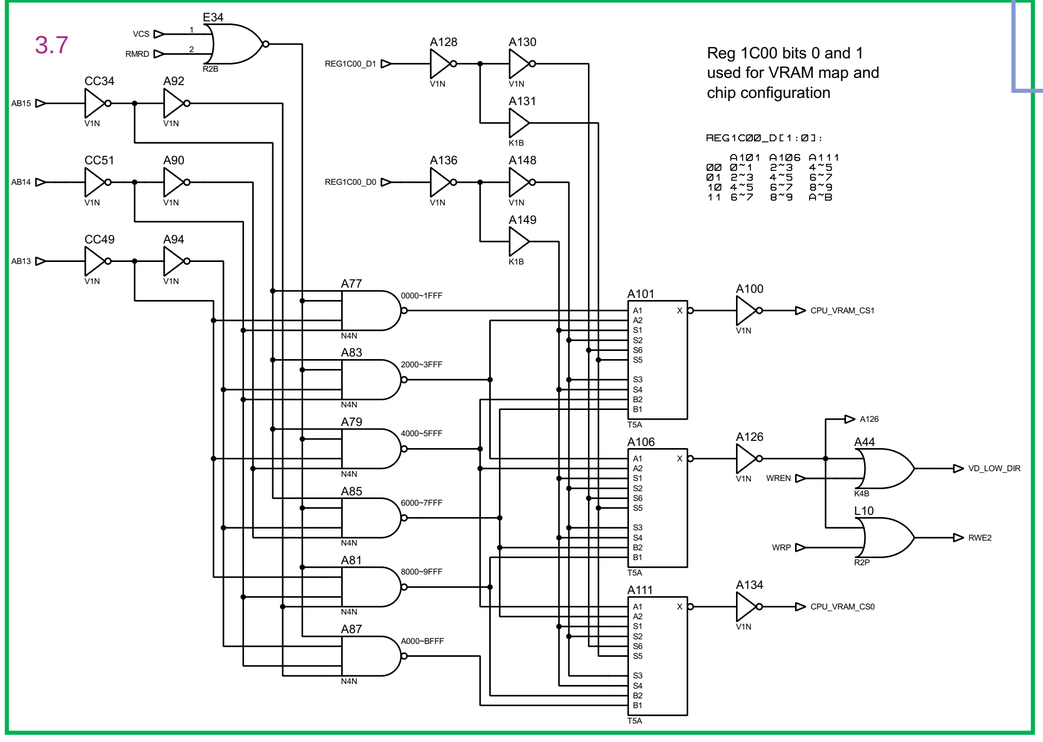
Interrupts flags



3.6



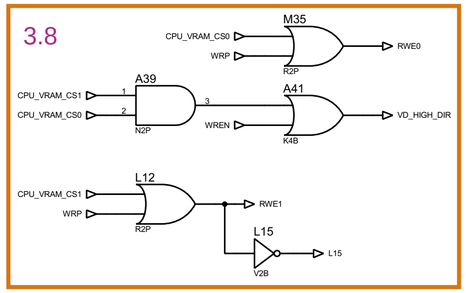
3.7



Reg 1C00 bits 0 and 1
used for VRAM map and
chip configuration

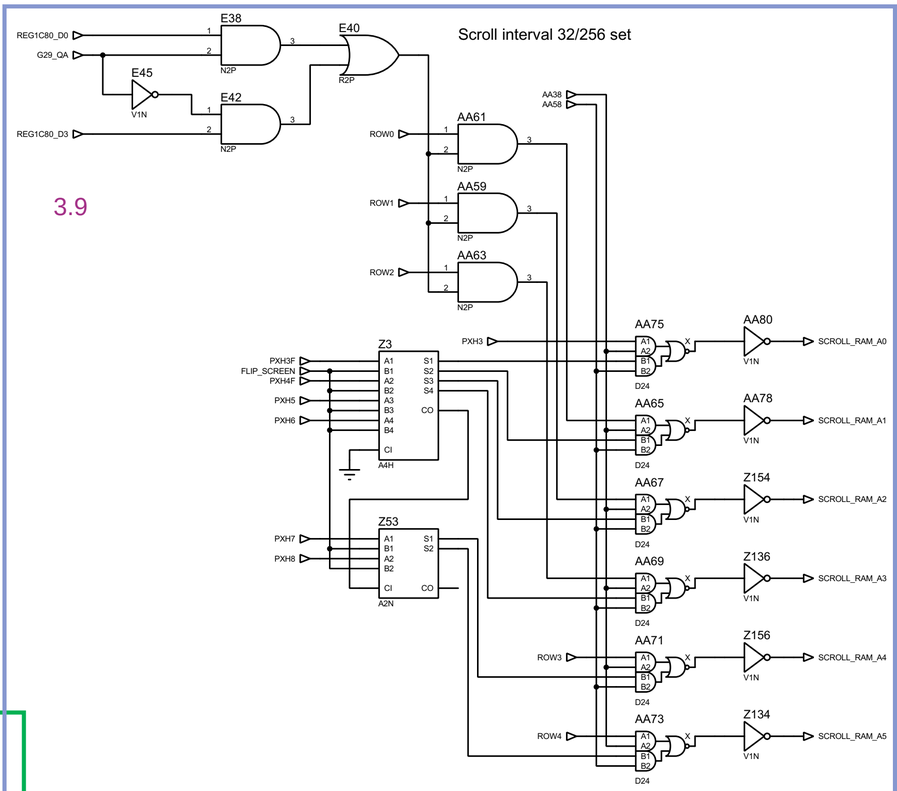
```
REG1C00_D[1:0]:

   A101 A106 A111
00  0~1  2~3  4~5
01  2~3  4~5  6~7
10  4~5  6~7  8~9
11  6~7  8~9  A~B
```

3.8



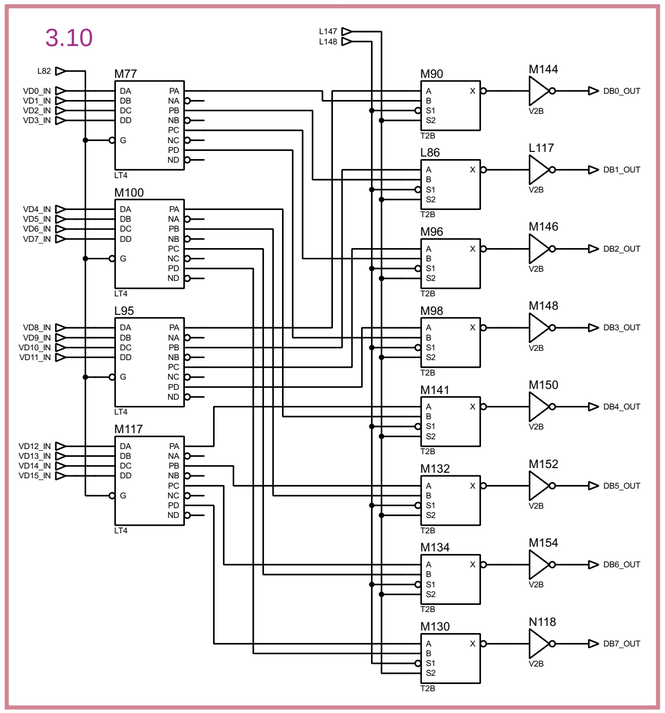
3.9

Scroll interval 32/256 set



VRAM read by CPU

3.10



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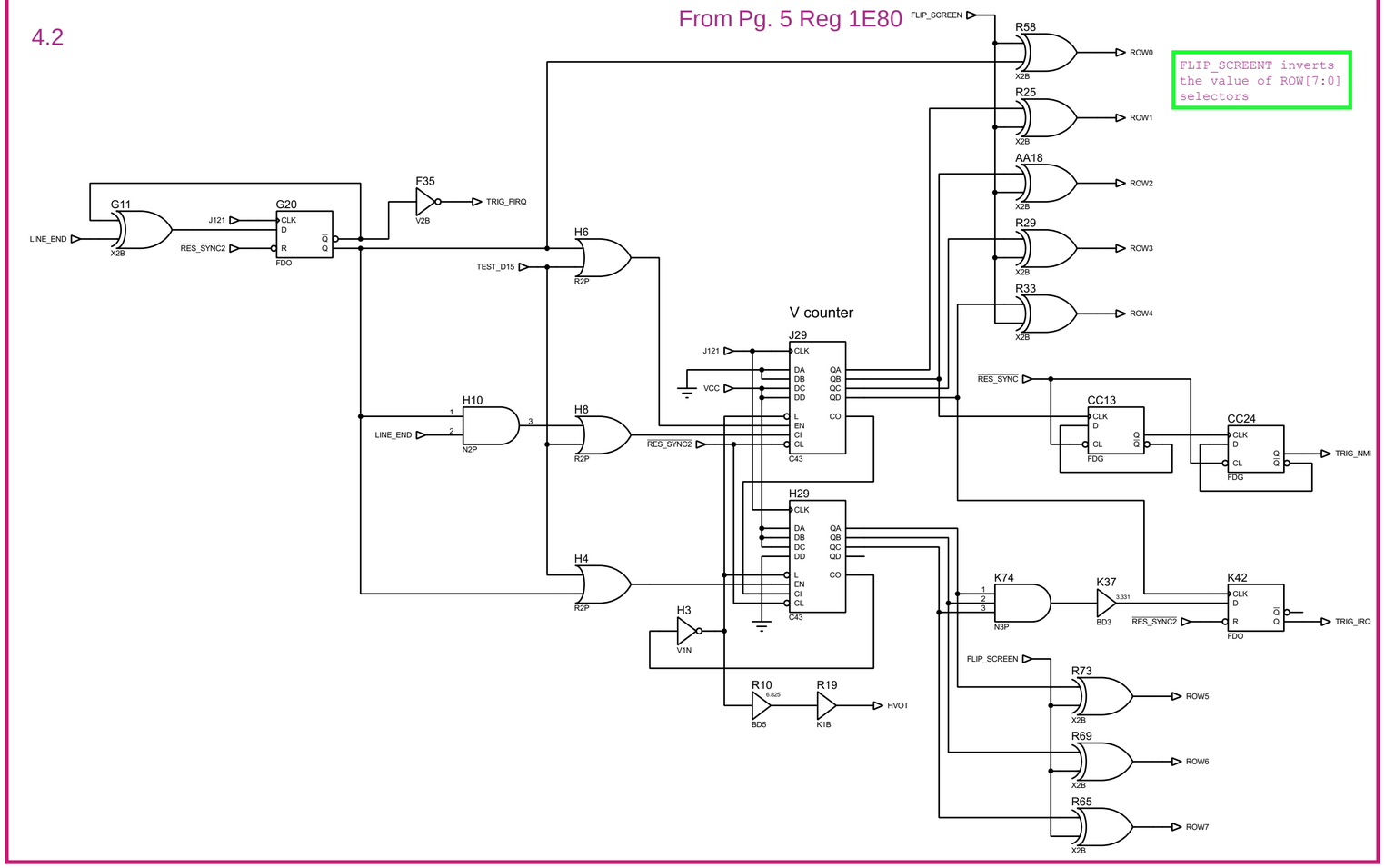
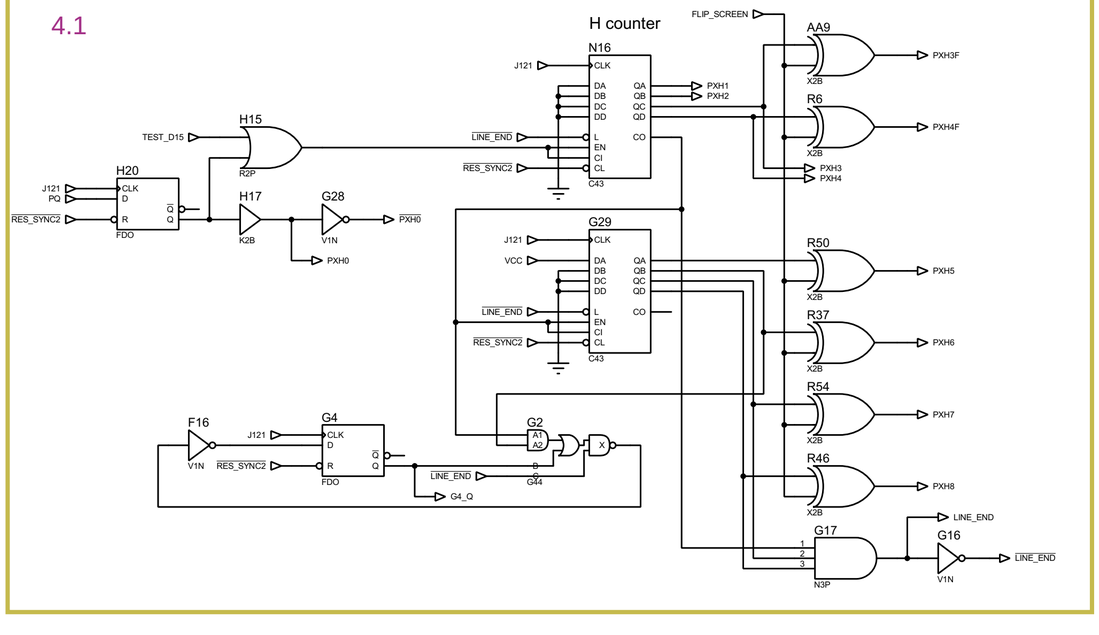
DESIGN TITLE: **Konami 052109** CPU STUFF	PAGE: **3 of 8**
BY: **Sean Gonsalves** REV: **A**	

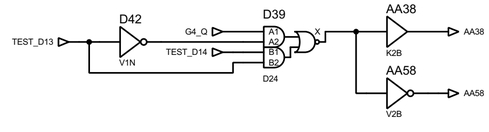
4.2



4.1

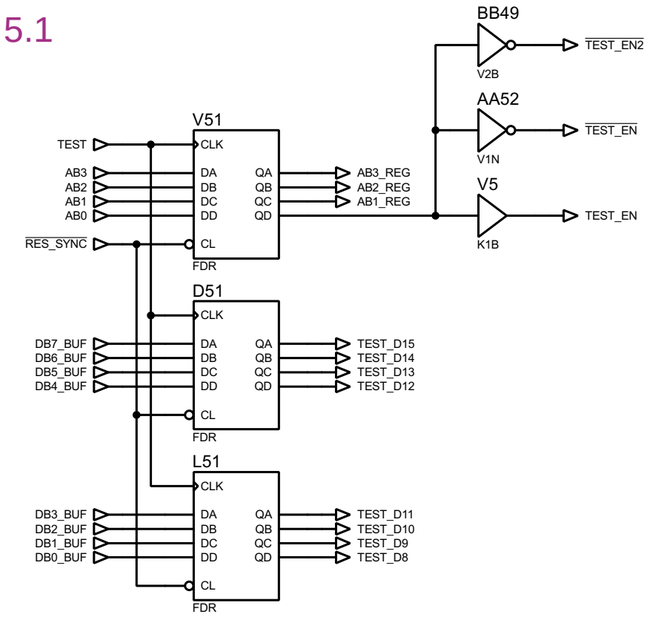


4.3

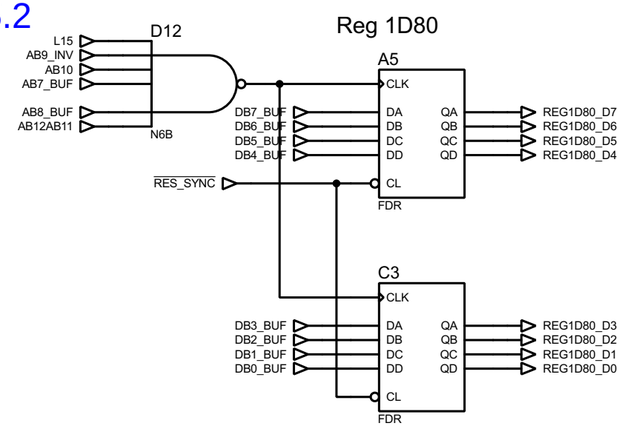


FILE NAME: k052109.pdsprj		DATE: 22/06/2021
DESIGN TITLE: Konami 052109 H/V COUNTERS		PAGE: 4 of 8
BY: Sean Gonsalves	REV: A	

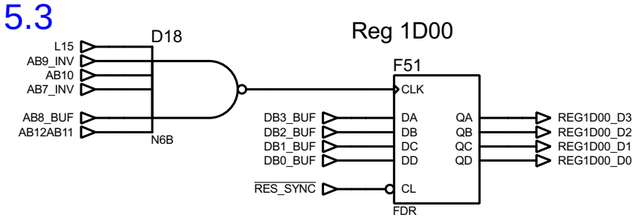
5.1



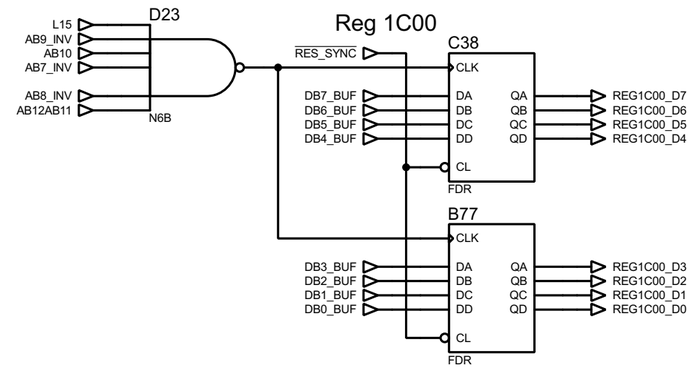
5.2



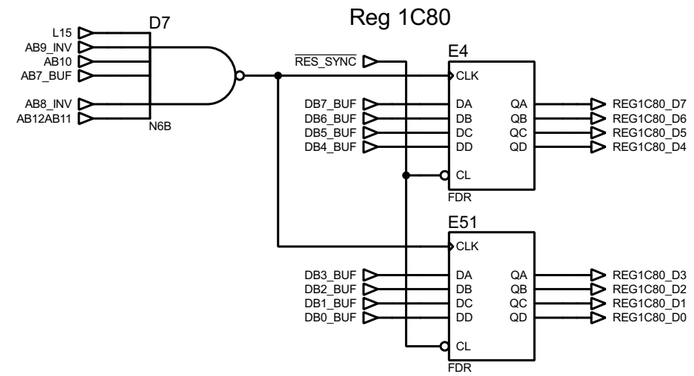
5.3



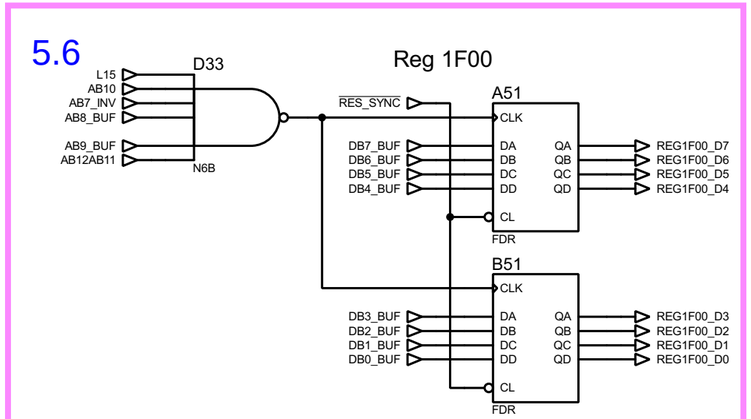
5.4



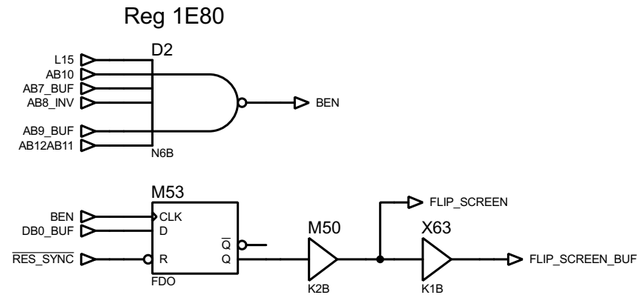
5.5



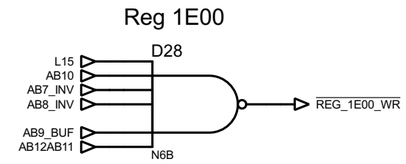
5.6



5.7



5.8



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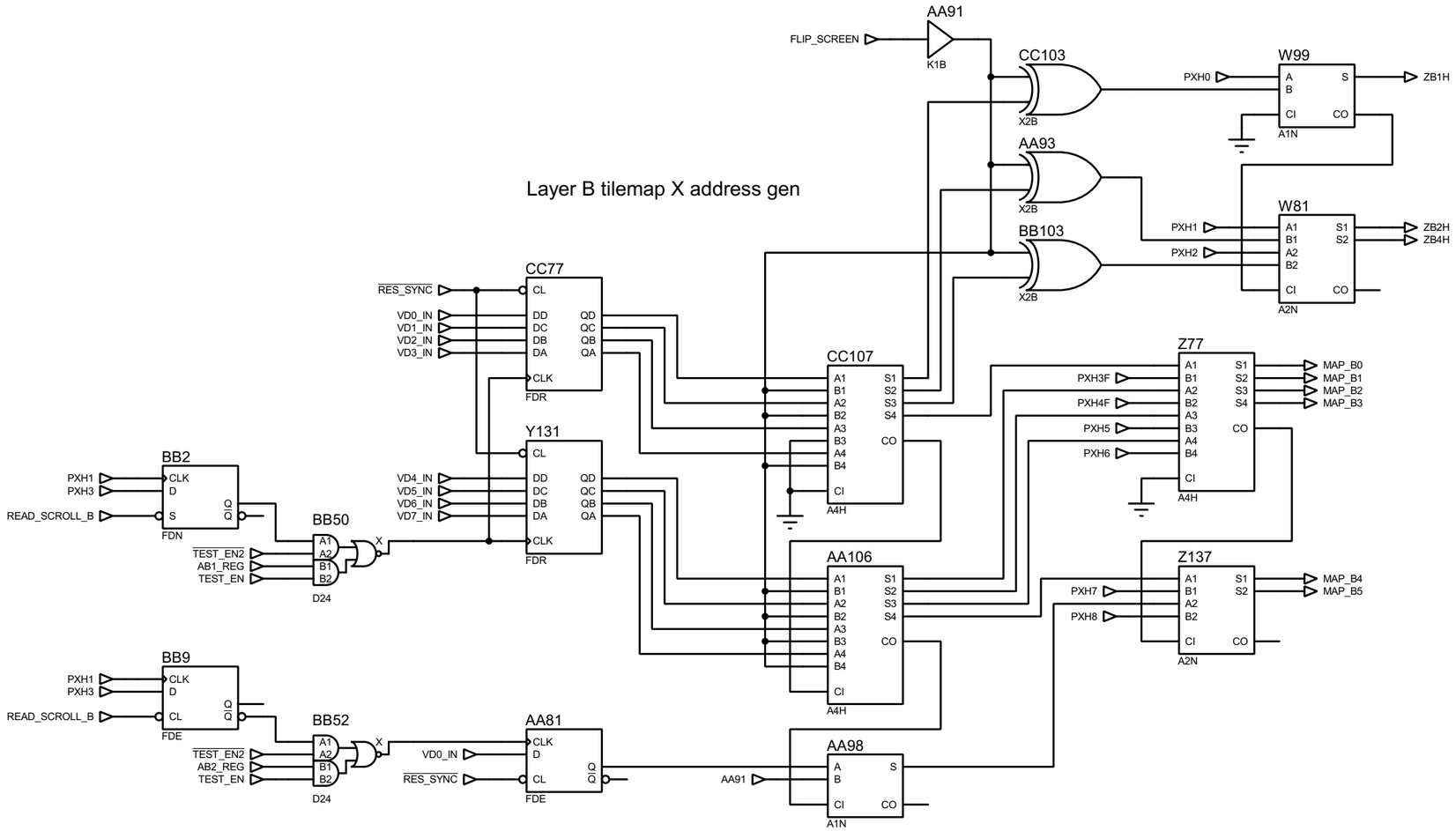
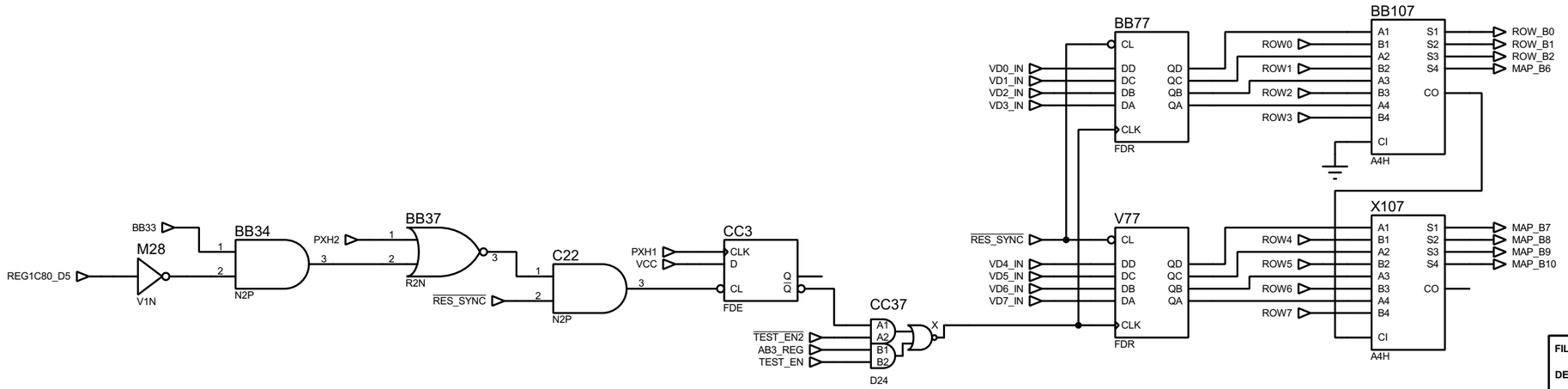
DESIGN TITLE: **Konami 052109** REGISTERS		PAGE: **5 of 8**
BY: **Sean Gonsalves**	REV: **A**	

Layer B tilemap X address gen



Layer B tilemap Y address gen



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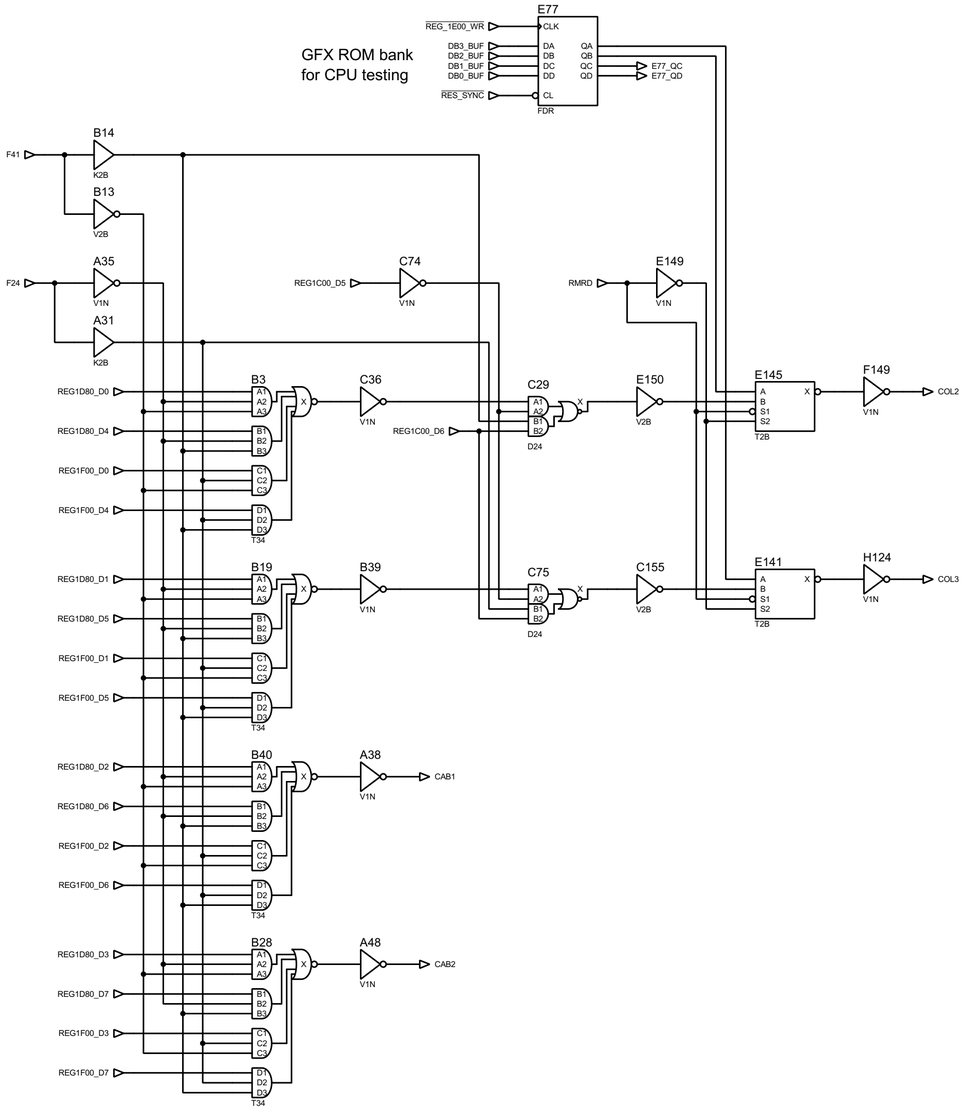
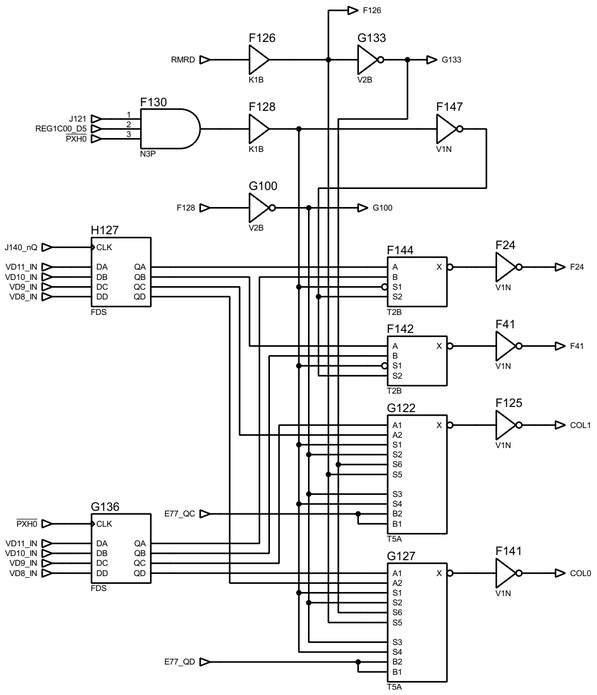
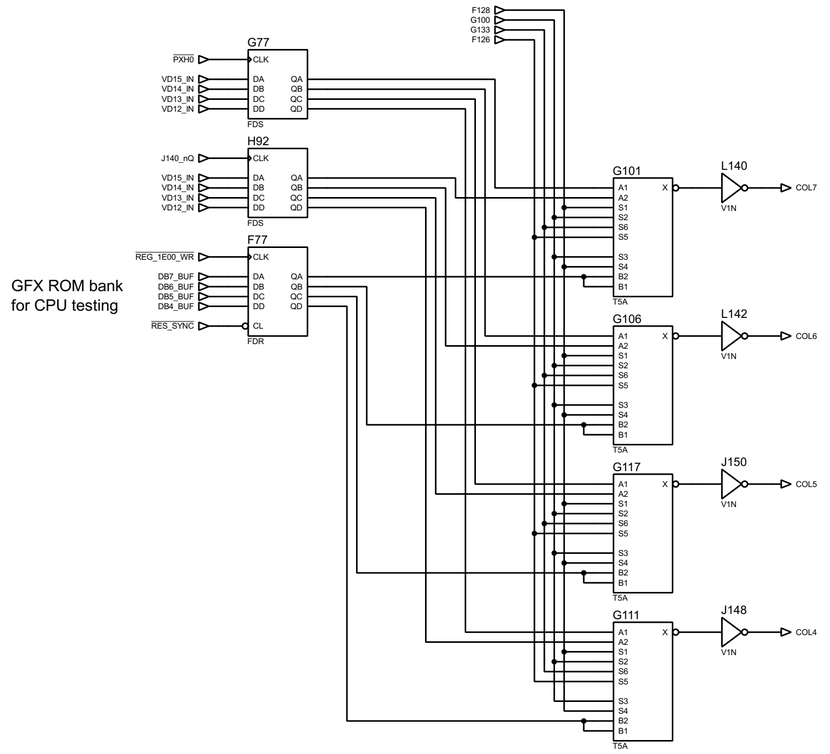
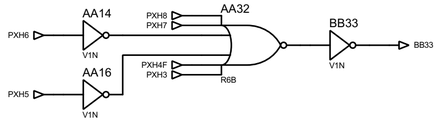
DESIGN TITLE: **Konami 052109** LAYER B SCROLL		PAGE:	**6 of 8**
BY: **Sean Gonsalves**	REV: **A**		

GFX ROM bank
for CPU testing

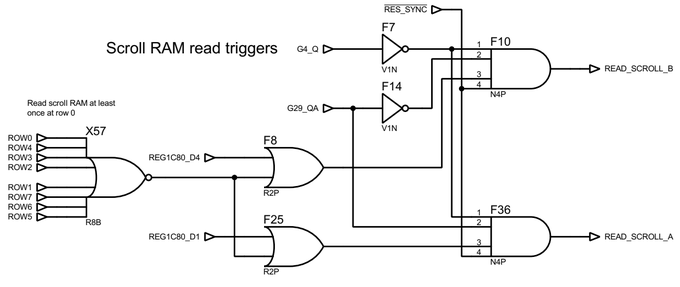






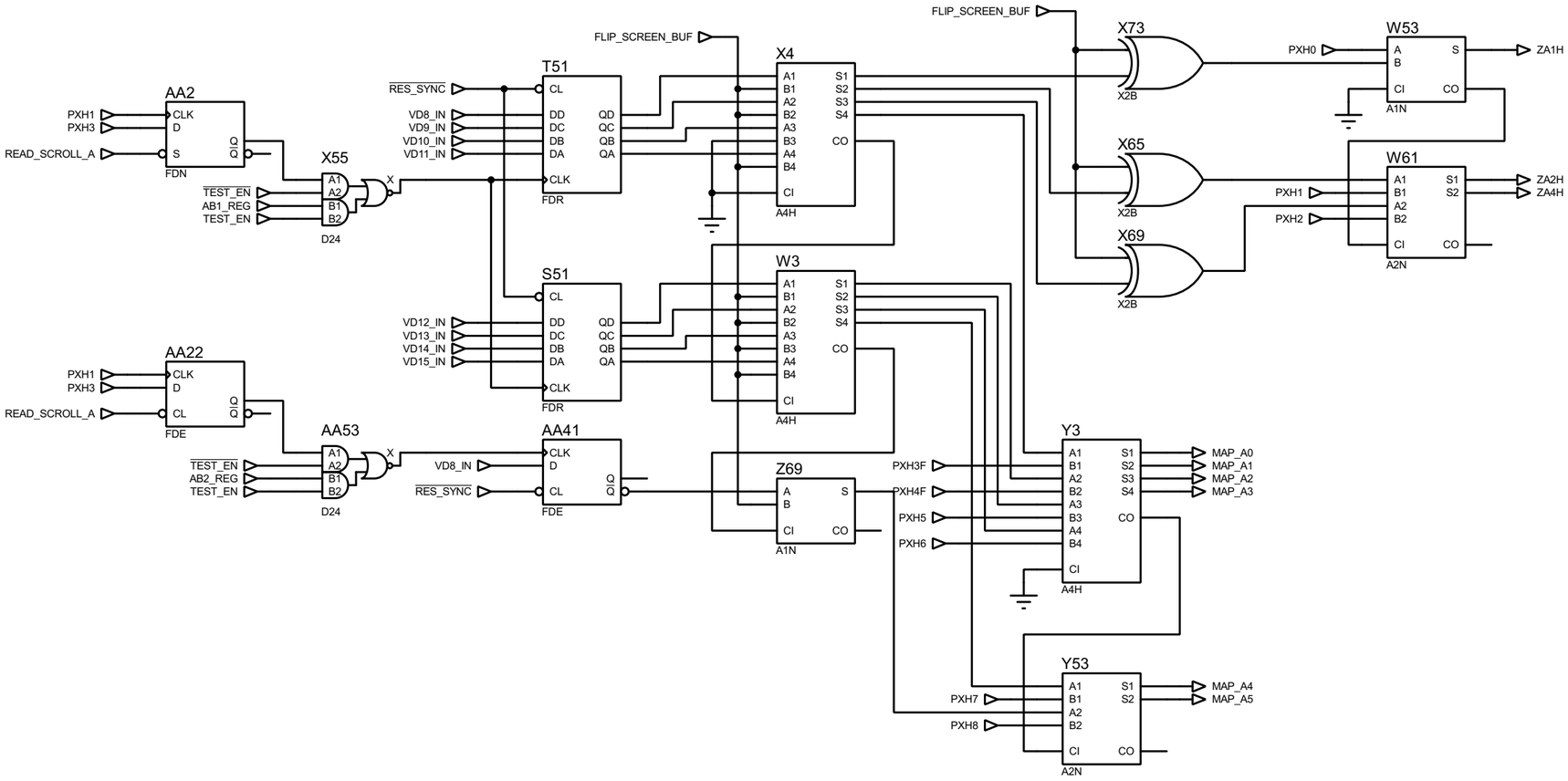


Scroll RAM read triggers

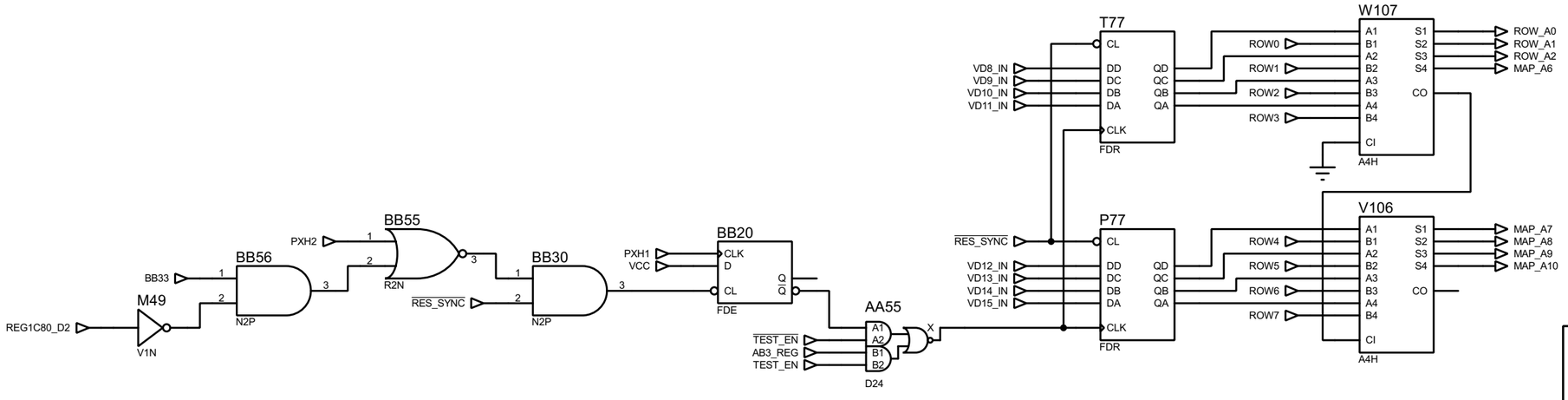


FILE NAME: **k052109.pdsprj**		DATE: **22/06/2021**
DESIGN TITLE: **Konami 052109** COL OUTPUTS		PAGE: **7 of 8**
BY: **Sean Gonsalves**	REV: **A**	

Layer A tilemap X address gen



Layer A tilemap Y address gen



FILE NAME: **k052109.pdsprj**			DATE: **22/06/2021**
DESIGN TITLE: **Konami 052109** LAYER A SCROLL			PAGE: **8 of 8**
BY: **Sean Gonsalves**	REV: **A**		