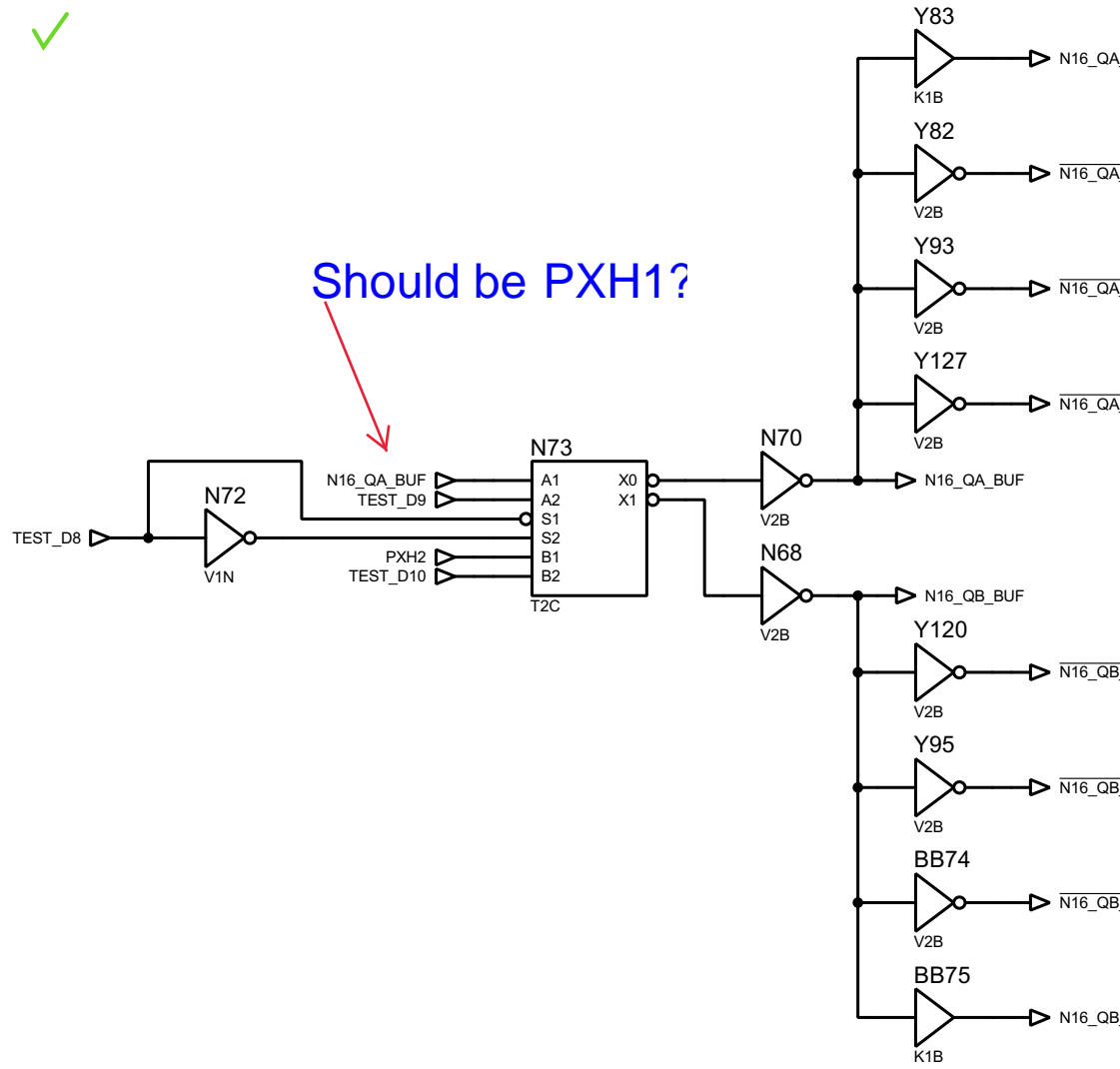
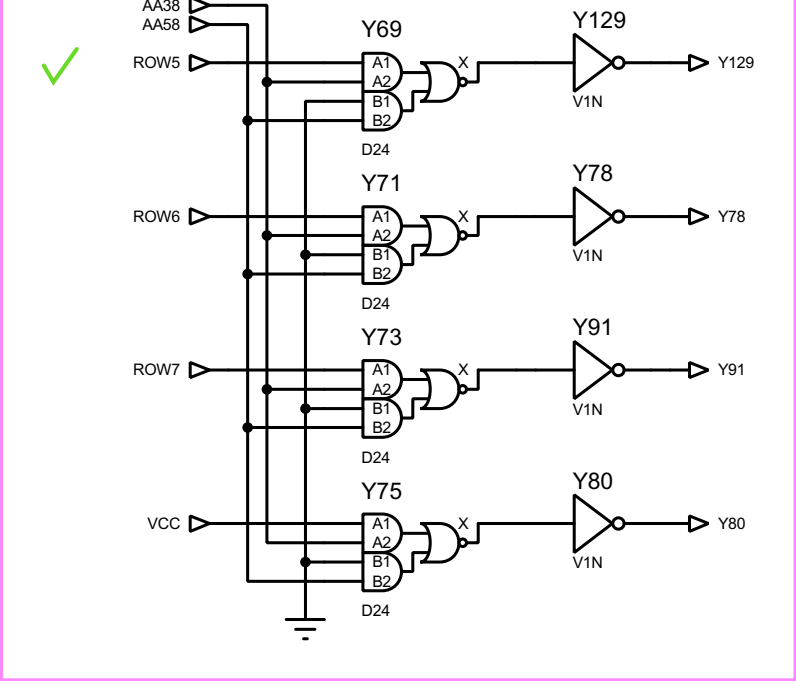


```
VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 00xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 1100 xxxx xxxx A Y scroll
0000 1101 xxxx xxxx A X scroll
0001 00xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 1100 xxxx xxxx B Y scroll
0001 1101 xxxx xxxx B X scroll
          x xxxx x Tilemaps X
xx xxx  Tilemaps Y
```



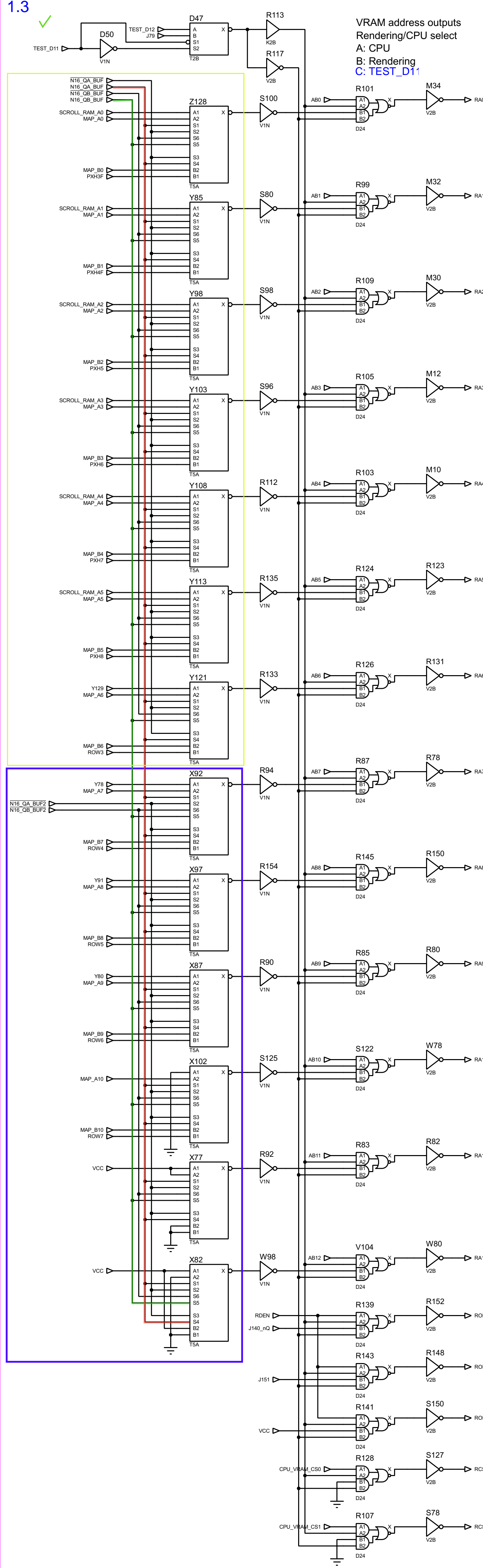
TEST_D13 Addresses Selector

1.2 From 4.3

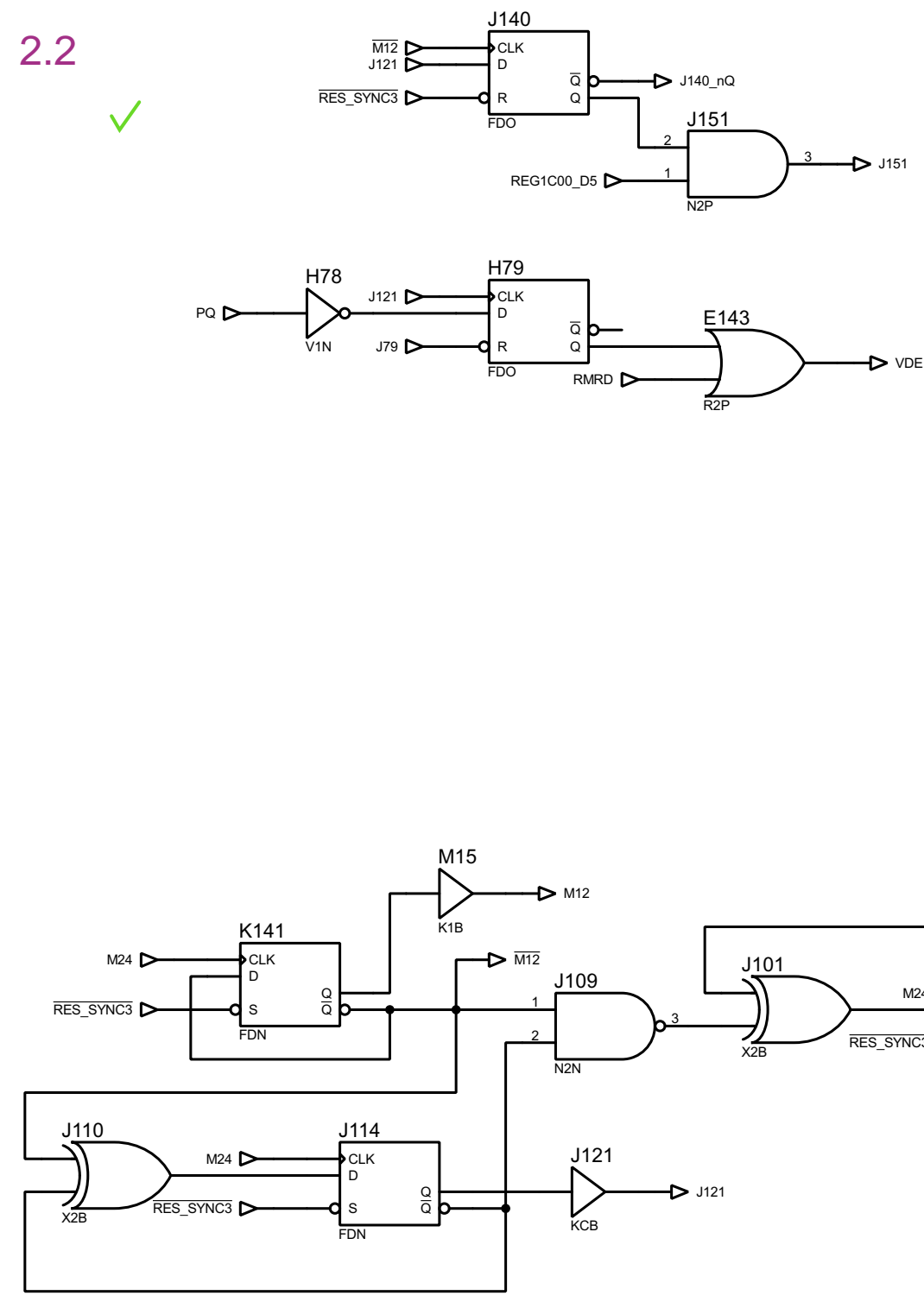


Selection can be simplified using AA38 (and AA38n) only, AA58 always selects 1'b0.

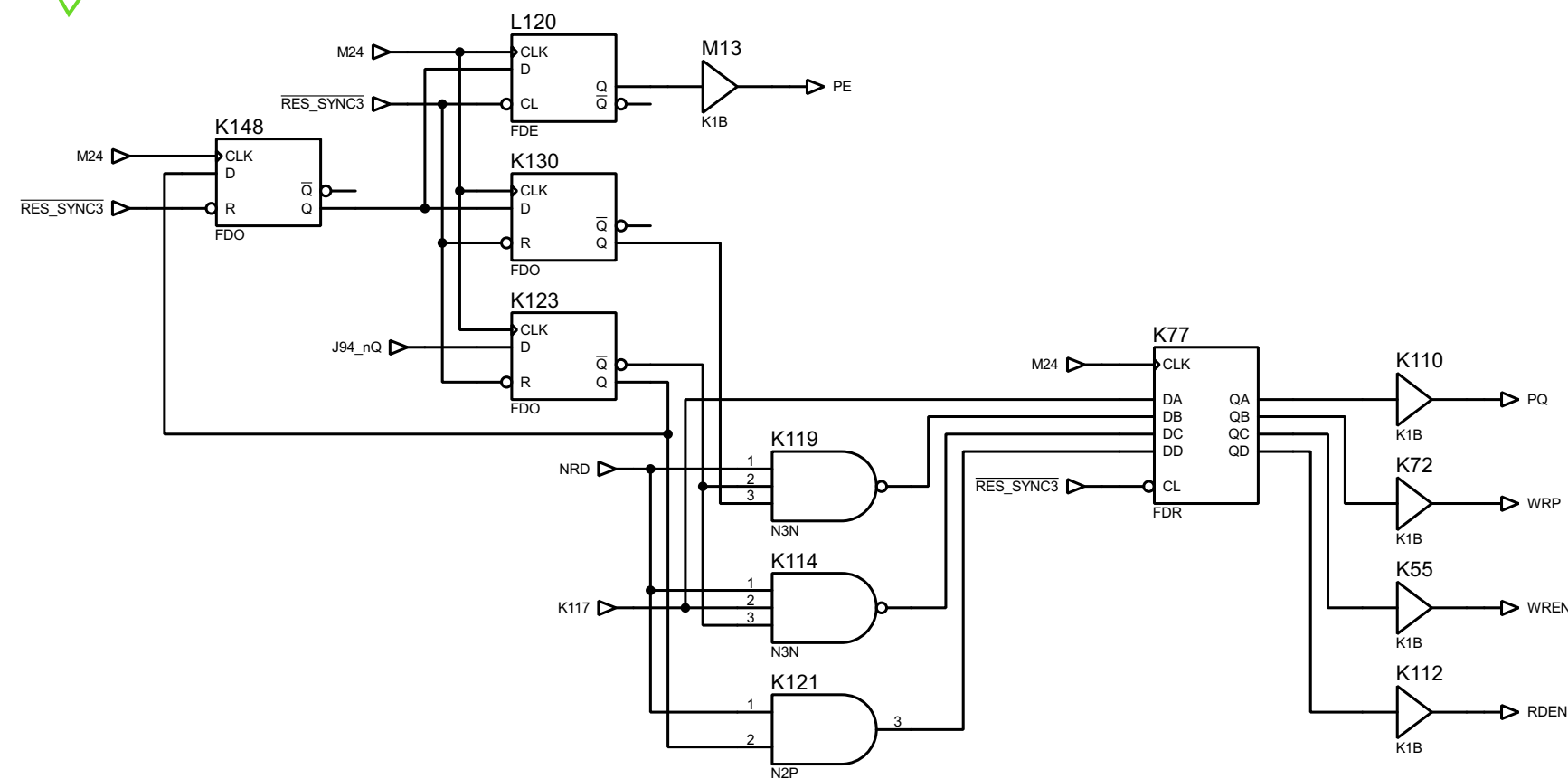
1.3



2.2



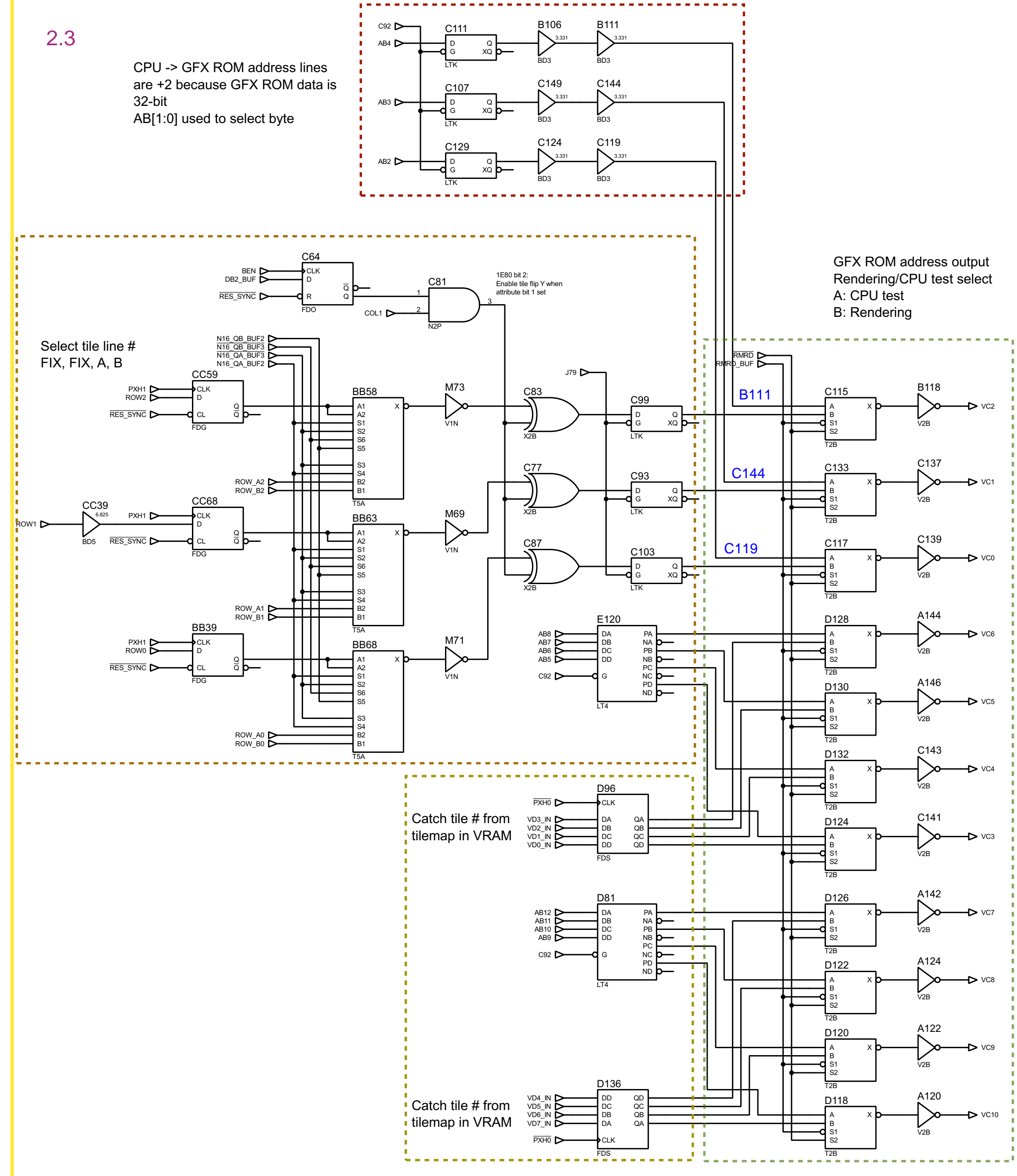
2.1



TIMING SIGNALS

2.3

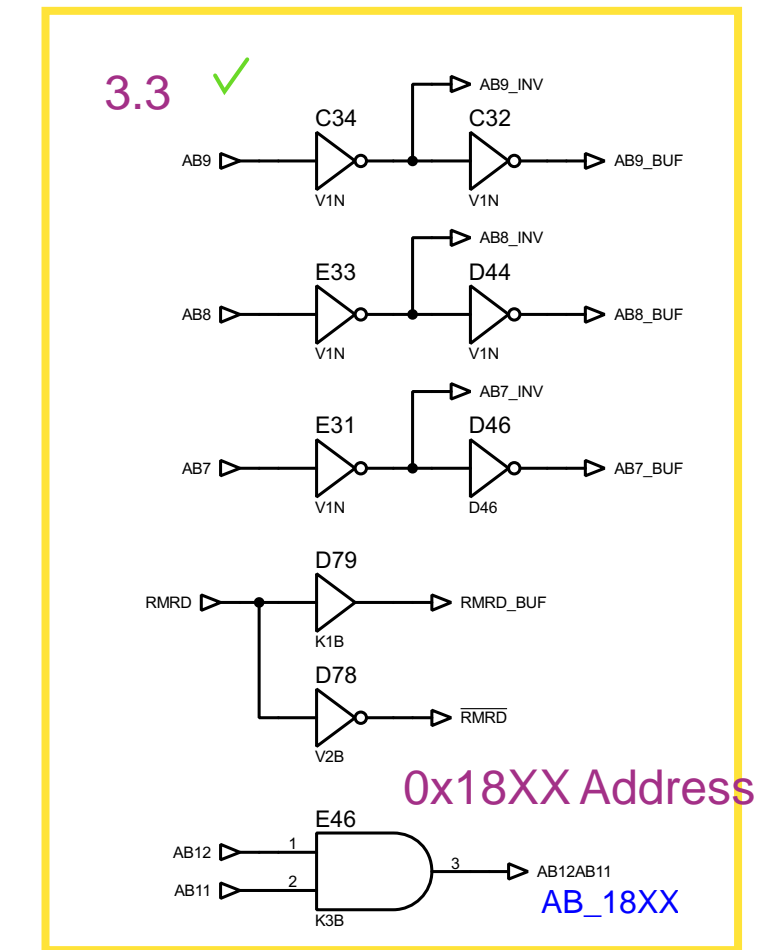
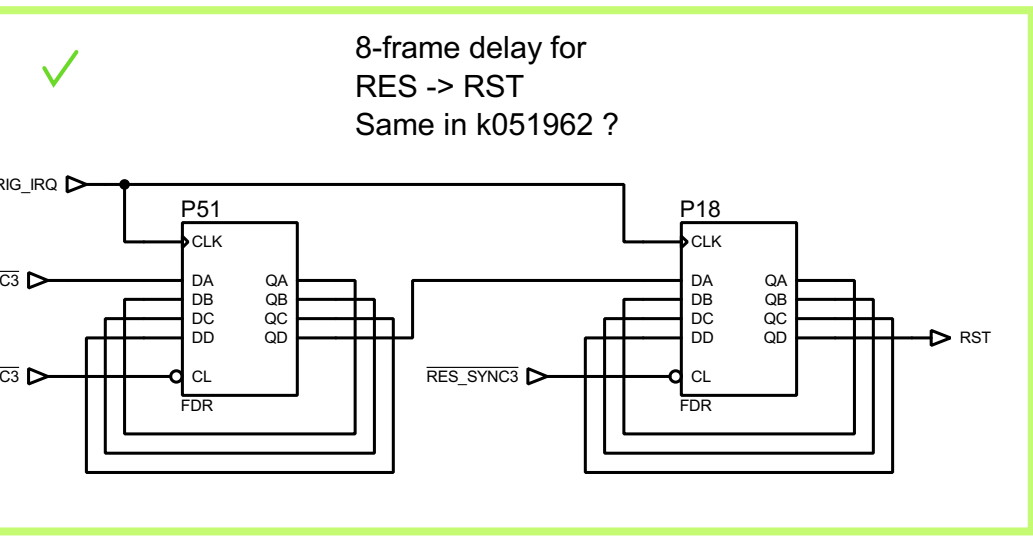
CPU -> GFX ROM address lines
are +2 because GFX ROM data is
32-bit
AB[1:0] used to select byte



GFX ROM address output
Rendering/CPU test select
A: CPU test
B: Rendering

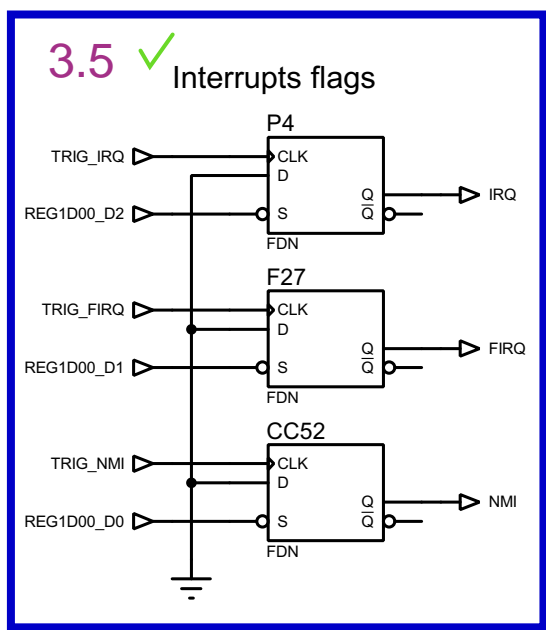
3.1 ✓

The diagram shows a circuit for a 3-bit counter. It starts with an N122 flip-flop. The flip-flop has four inputs: M04 (CLK), V02 (D), RES (CL), and FDE. The output Q is connected to the M74 multiplexer's input 0. The M74 multiplexer has two inputs (0 and 1) and one output. The output of the M74 is connected to the H12 comparator's input 0. The H12 comparator has two inputs (0 and 1) and one output. The output of the H12 is connected to the H1B comparator's input 0. The H1B comparator has two inputs (0 and 1) and one output. The output of the H1B is connected to the RES_SYNC2 output. The output of the H12 is connected to the RES_SYNC output. The output of the M74 is also connected to the RES_SYNC3 output.

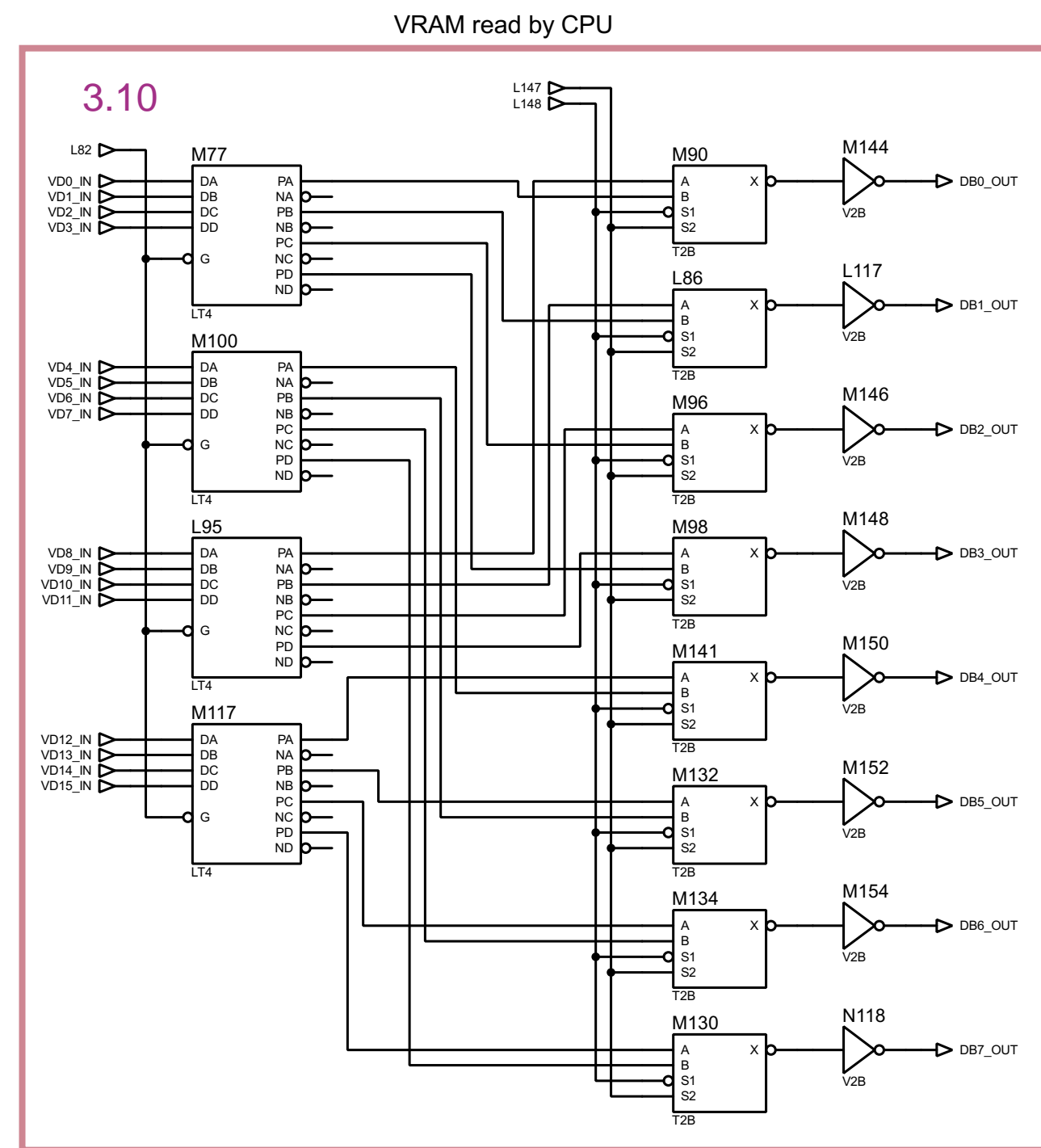
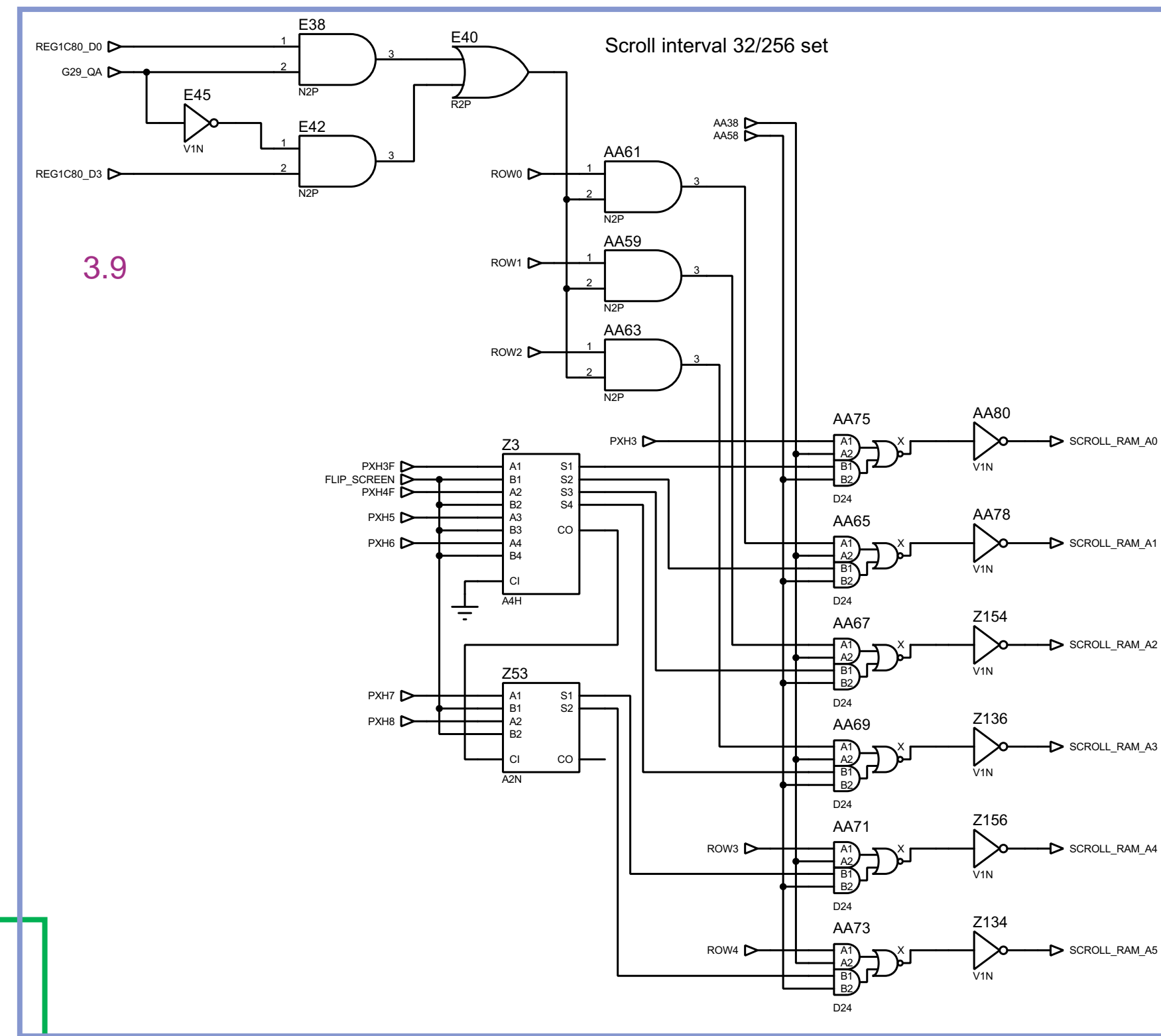
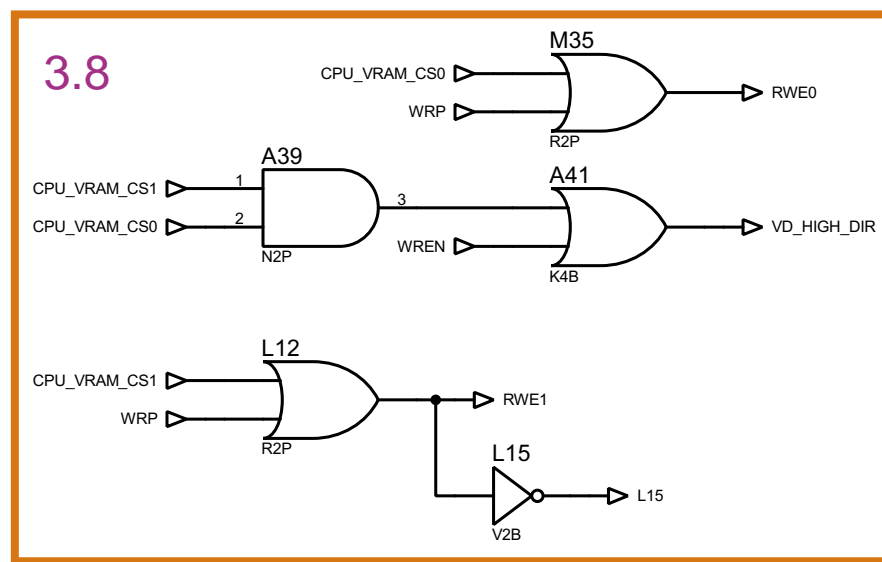
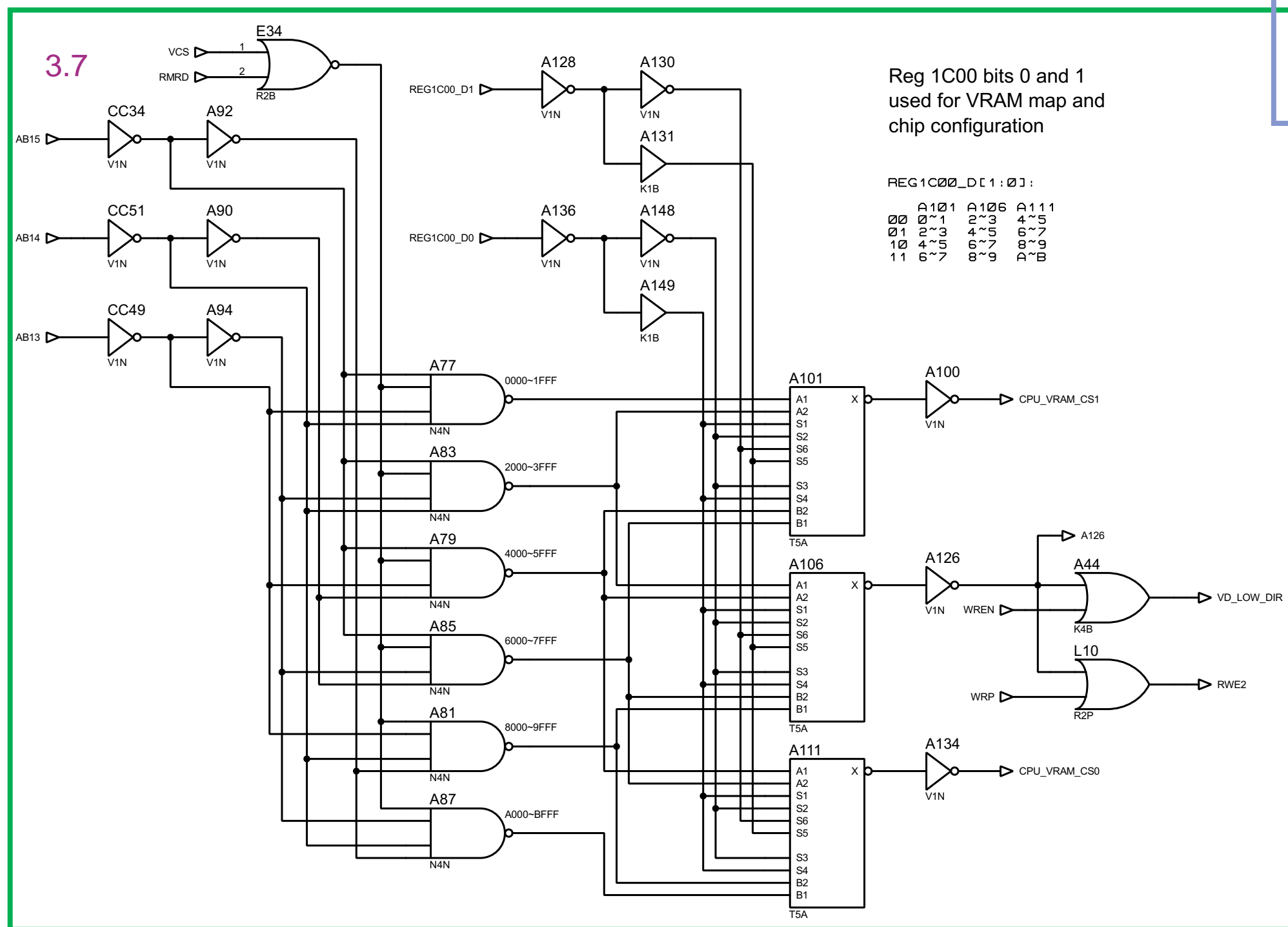
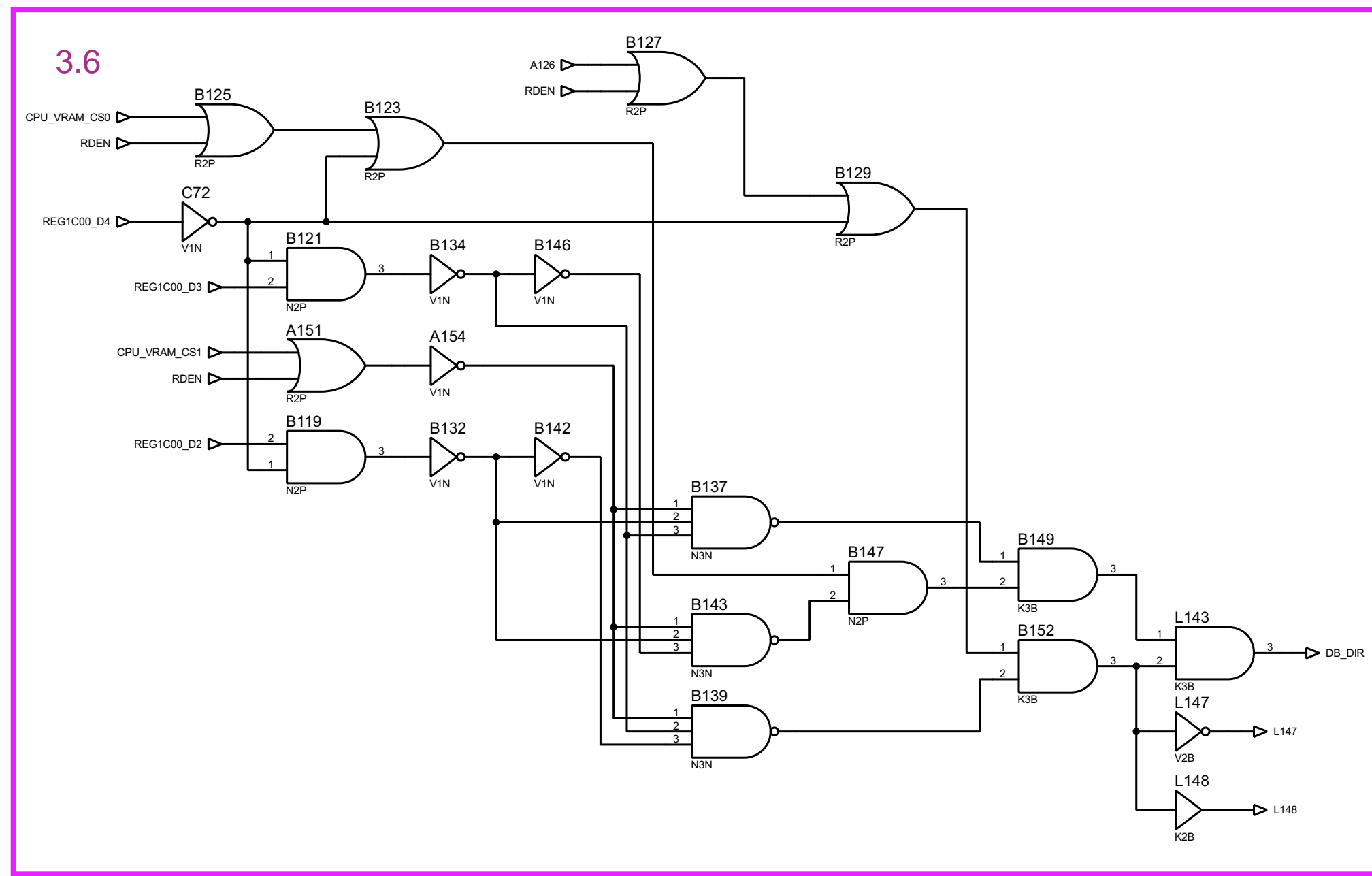


3.4 ✓

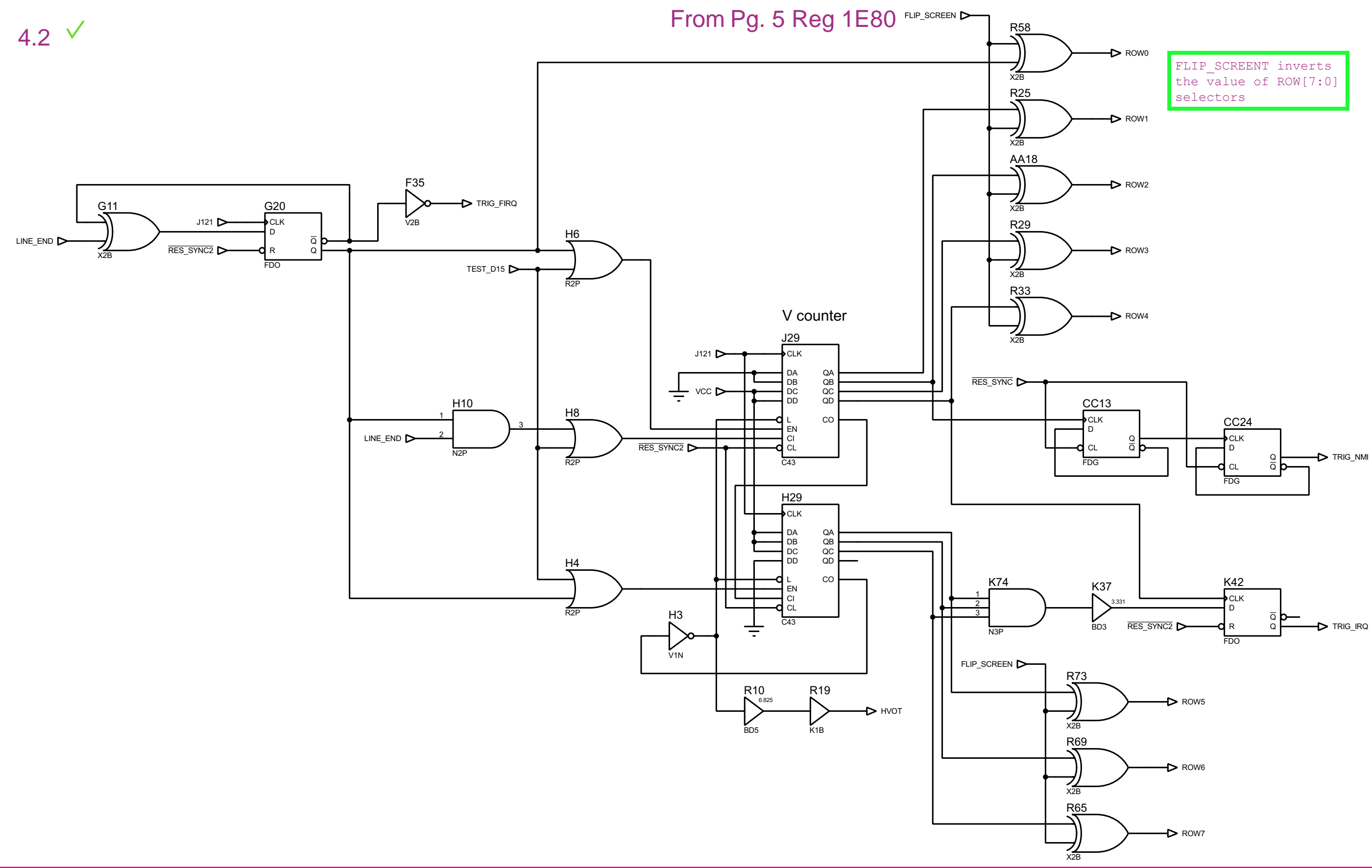
The diagram illustrates a 10-bit bus system. It consists of 10 input signals (DB0_IN to DB7_IN) and 10 output signals (DB0_BUF to DB7_BUF). Each input signal is connected to a buffer (N135 to N103) and an inverter (K2B). The output of each buffer is connected to the input of the corresponding inverter, and the output of each inverter is connected to the output signal. The buffers are labeled N135, N80, N132, N77, N83, N97, N100, and N103. The inverters are labeled K2B.



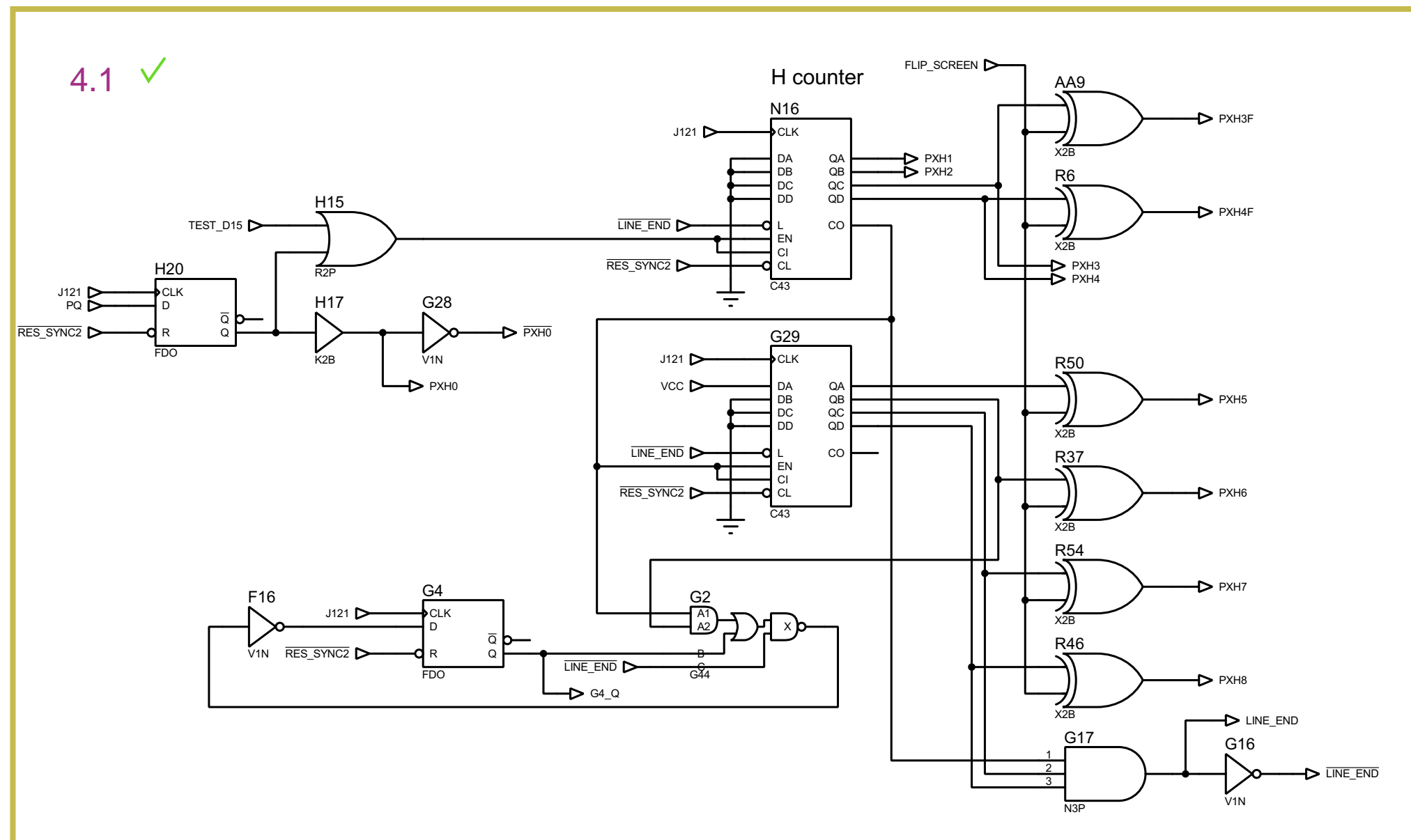
```
wire [7:0] DB_BUF
```



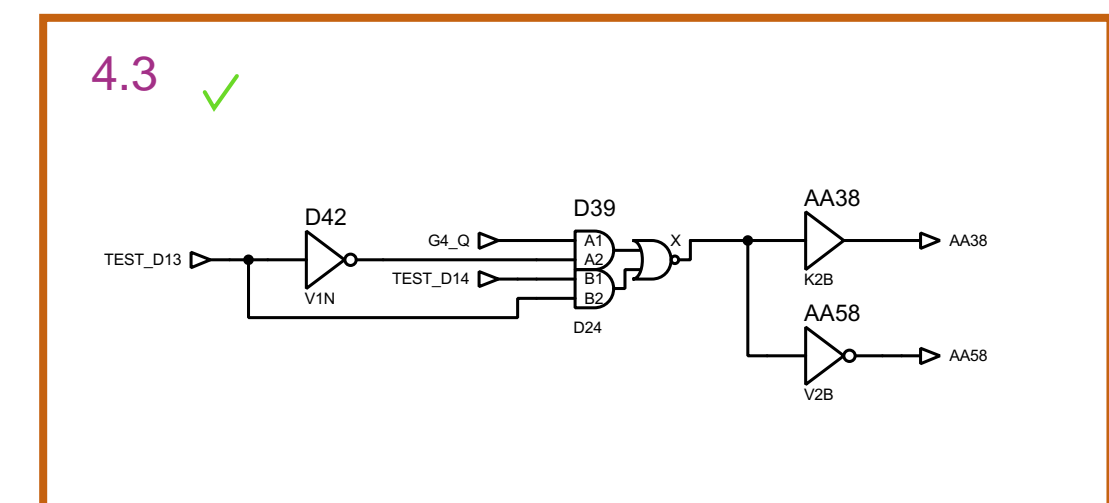
4.2 ✓



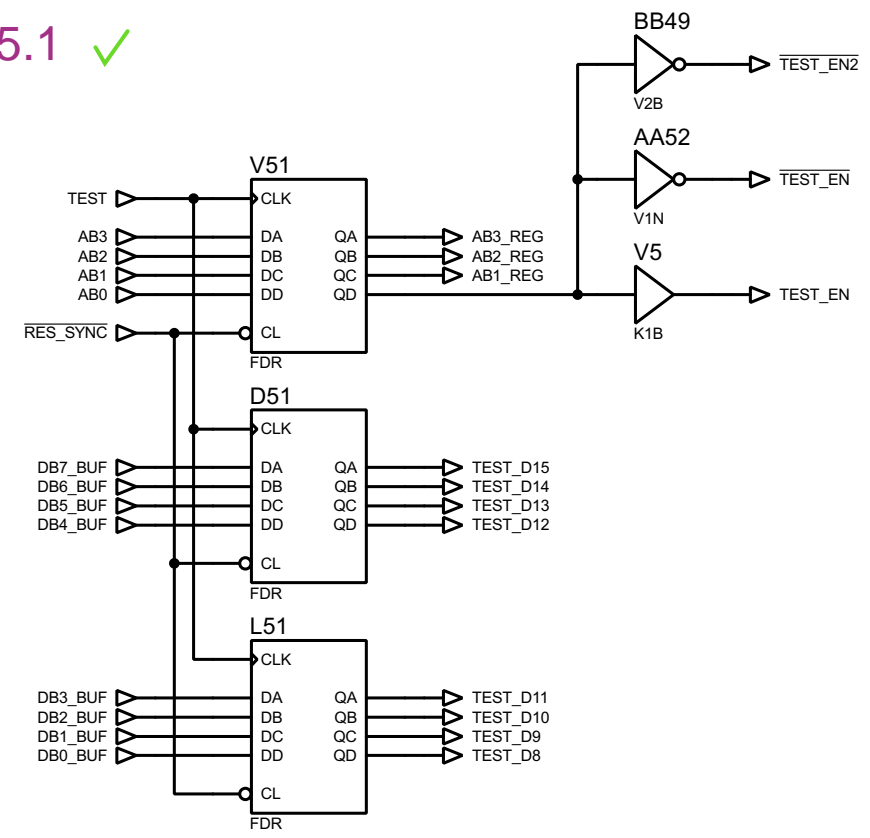
4.1 ✓



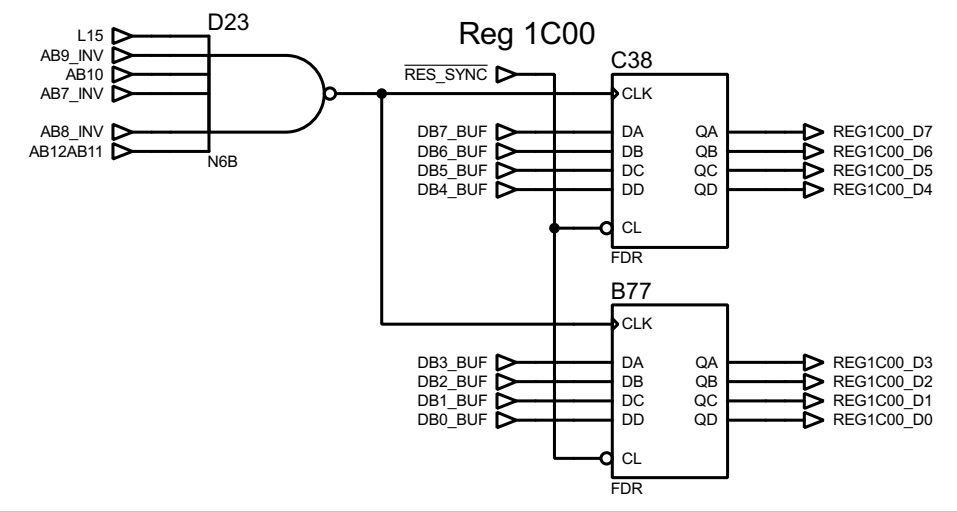
4.3 ✓



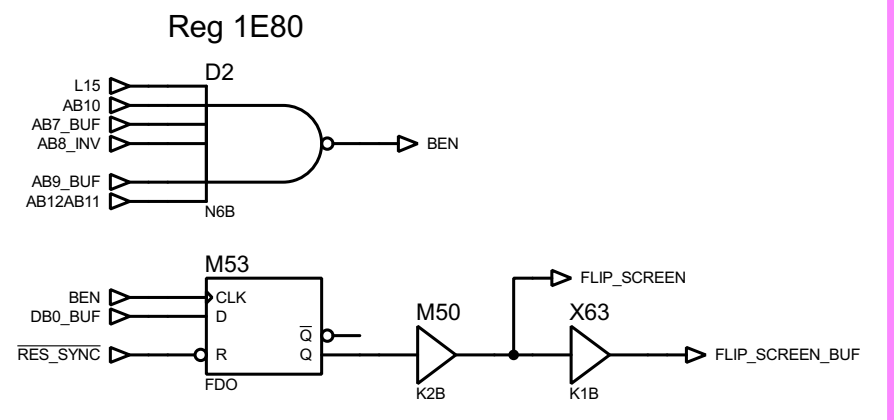
5.1 ✓



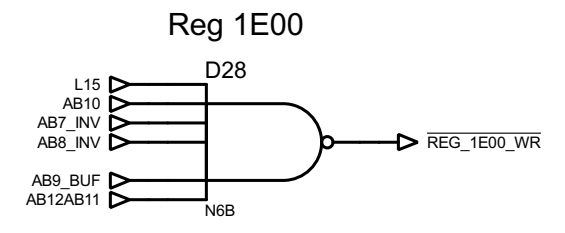
5.4 ✓



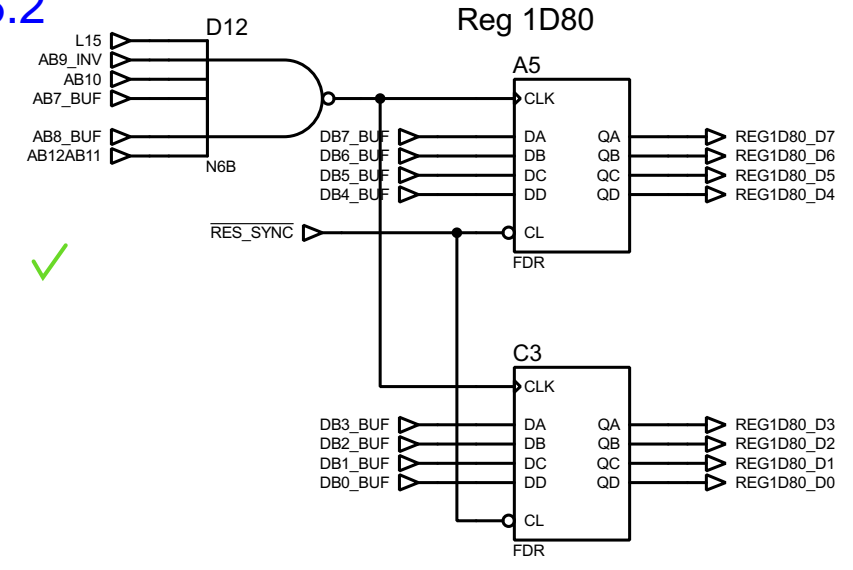
5.7 ✓



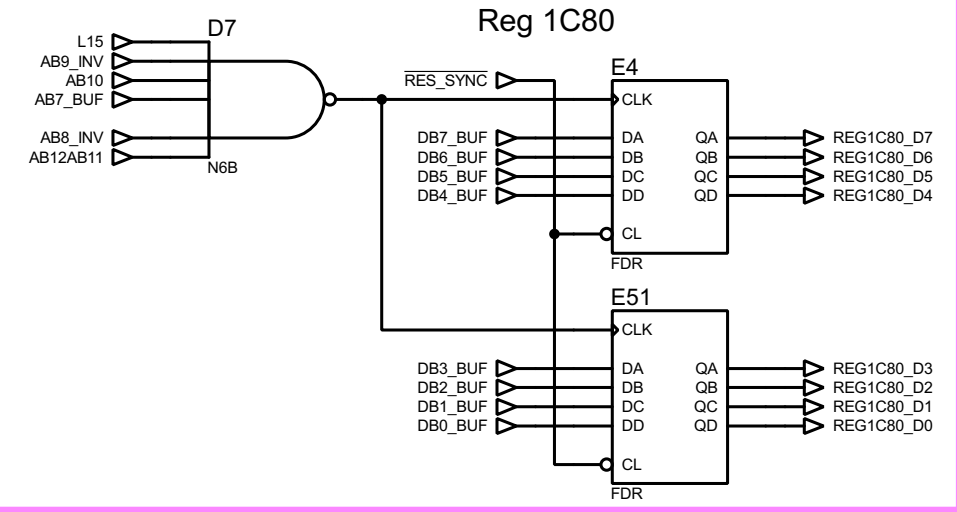
5.8 ✓



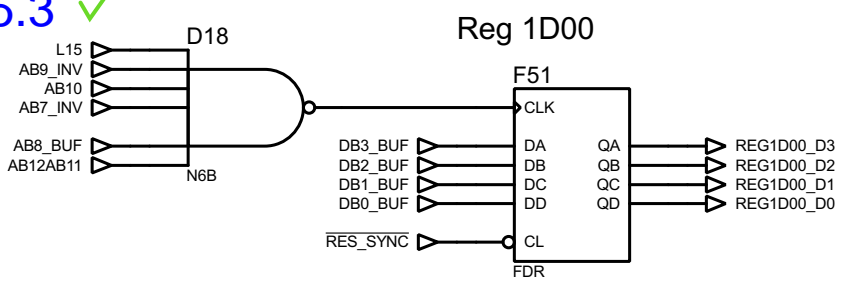
5.2 ✓



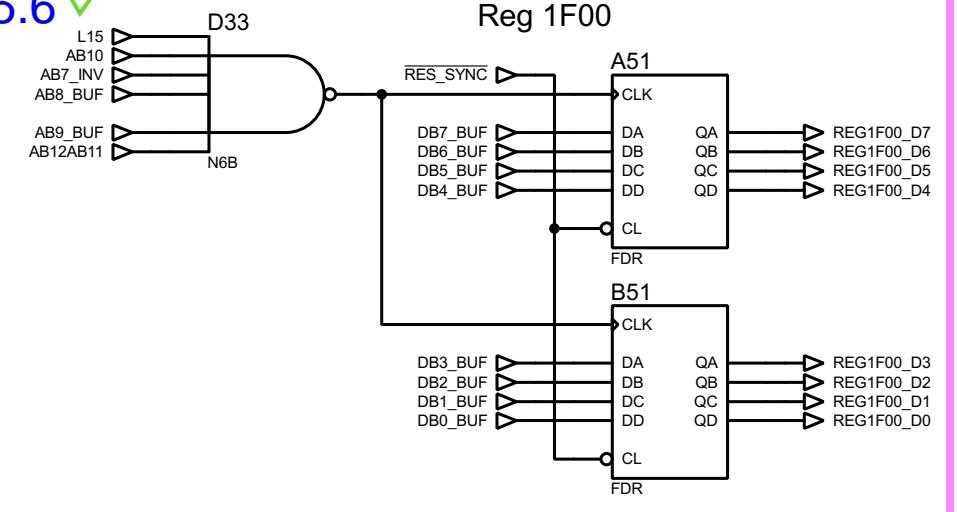
5.5 ✓



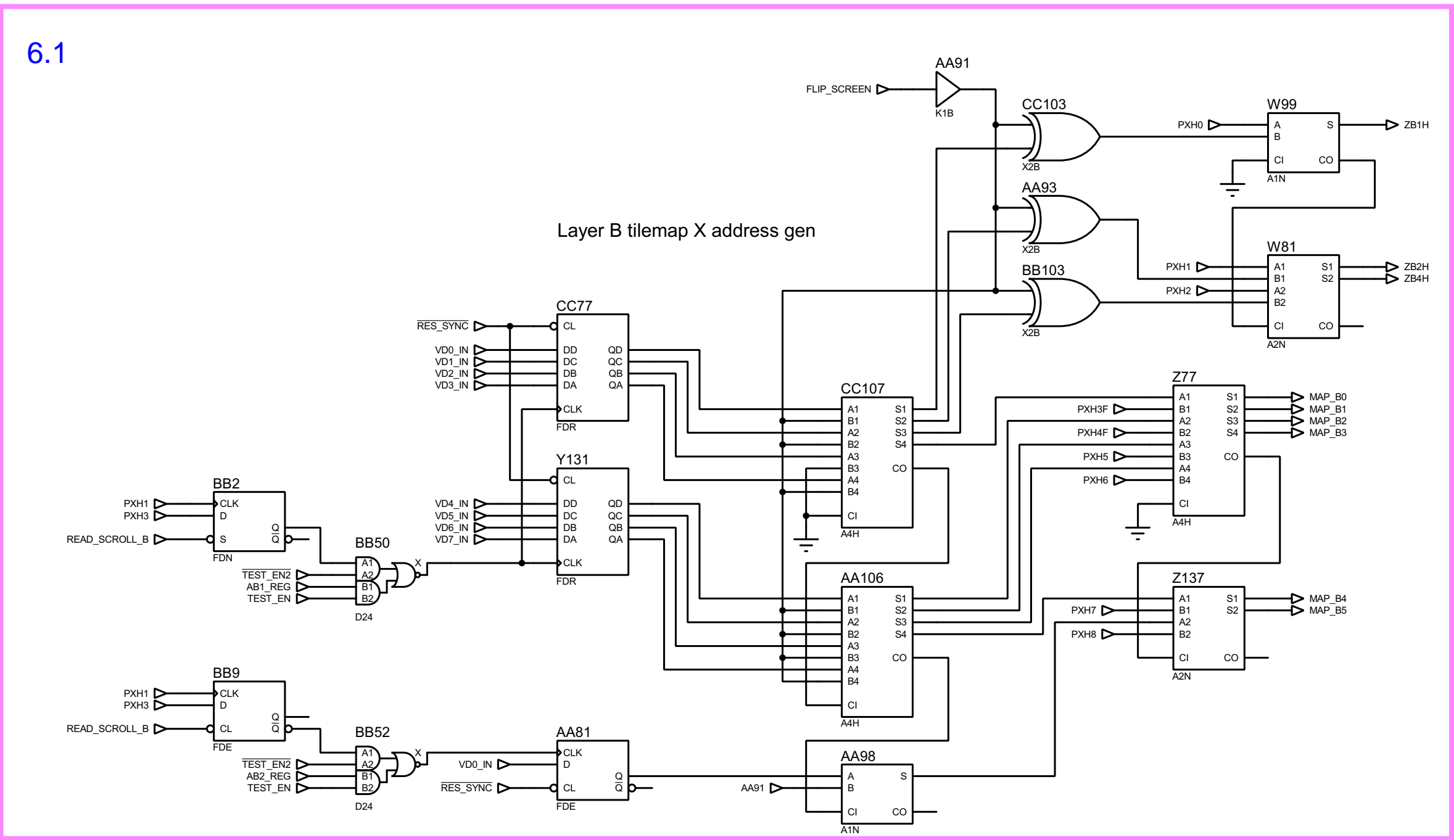
5.3 ✓



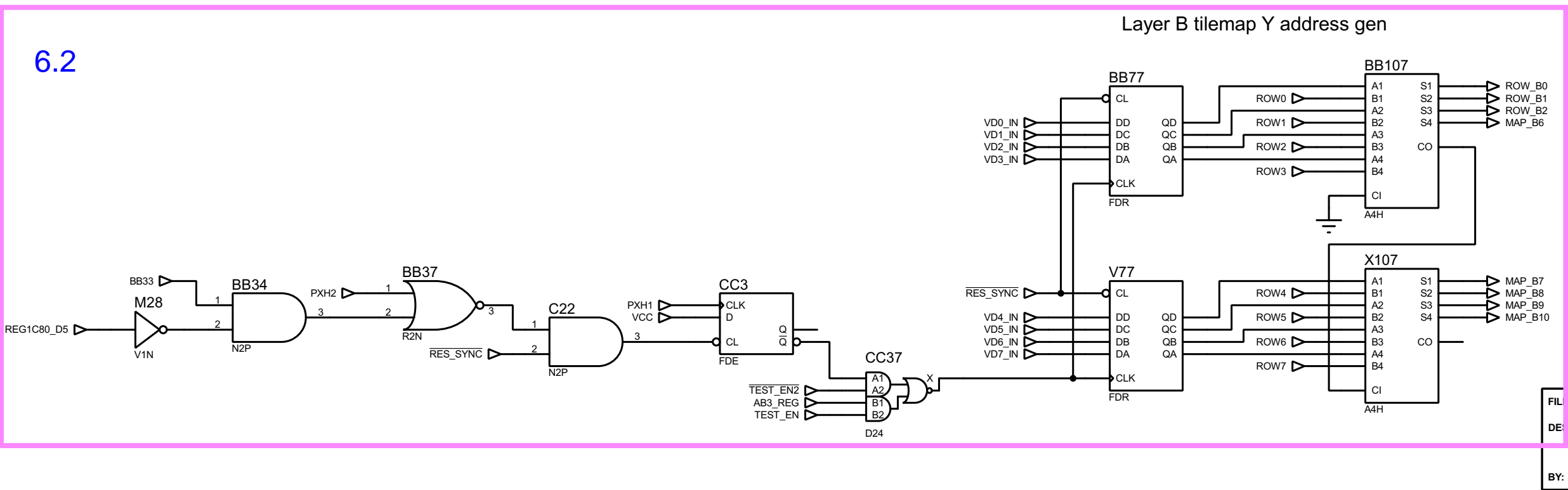
5.6 ✓



6.1



6.2



The diagram illustrates the logic for the GFX ROM bank during CPU testing. It features a 4-to-1 multiplexer (E77) that selects between four 8-bit ROM banks (DB3_BUF, DB2_BUF, DB1_BUF, DB0_BUF) based on the REG_TE00_WR signal. The selected data is then routed through various logic gates (AND, OR, NOT) and registers (REG1C00_D5, REG1C00_D6) to produce the final output signals (COL2, COL3). The diagram also shows the internal structure of the ROM banks, including the 4-to-1 multiplexers (B3, B19, B40, B28) and the 8-to-1 multiplexers (C36, C29, C75, C155) that combine the data from the ROM banks.

7.2

7.3

Logic diagram for the GFX ROM bank for CPU testing. The diagram shows four 3-to-8 decoders (G77, H92, F77, and G101/G106/G117/G111) connected to various inputs. The outputs of these decoders are connected to four multiplexers (L140, L142, J150, J148) which produce COL7, COL6, COL5, and COL4 respectively. The inputs to the decoders include PXH0, VD15_IN, VD14_IN, VD13_IN, VD12_IN, J140_nQ, REG_TEQ_WR, DB7_BUF, DB6_BUF, DB5_BUF, DB4_BUF, RES_SYNC, and F128, G100, G133, F126.

7.4

7.5

Scroll RAM read triggers

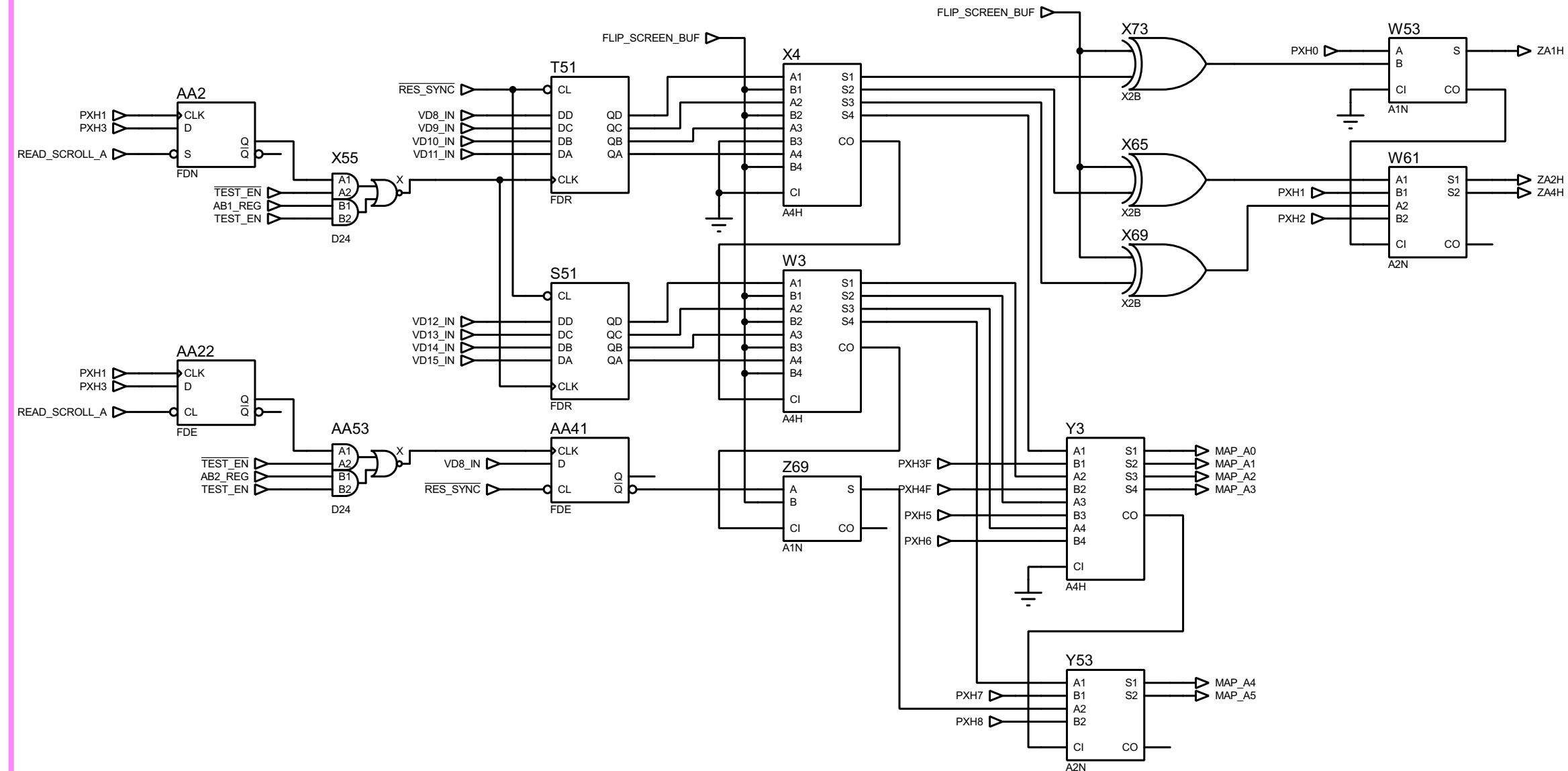
Read scroll RAM at least once at row 0

```

graph LR
    ROW0[ROW0] --> X57
    ROW4[ROW4] --> X57
    ROW3[ROW3] --> X57
    ROW2[ROW2] --> X57
    ROW1[ROW1] --> X57
    ROW7[ROW7] --> X57
    ROW6[ROW6] --> X57
    ROW5[ROW5] --> X57
    X57 --> REG1C80_D4
    REG1C80_D4 --> F8
    REG1C80_D1 --> F25
    R2P[R2P] --> F8
    R2P --> F25
    F8 --> F10
    F8 --> F36
    F25 --> F10
    F25 --> F36
    G4_O[G4_O] --> F10
    G4_O --> F36
    G29_QA[G29_QA] --> F10
    G29_QA --> F36
    RES_SYNC[RES_SYNC] --> F10
    RES_SYNC --> F36
    N4P[N4P] --> F10
    N4P --> F36
    F10 --> READ_SCROLL_B
    F36 --> READ_SCROLL_A
  
```

8.1

Layer A tilemap X address gen



8.2

Layer A tilemap Y address gen

