

3.1

The diagram shows the first stage of a 3-bit counter. It consists of an N122 flip-flop, an M74 K2B inverter, and an H12 K1B inverter. The flip-flop's clock (CLK) is connected to M04, its data input (D) to V02, and its clear input (CL) to RES. The flip-flop's output (Q) is connected to the input of the M74 inverter. The M74 inverter's output is connected to the input of the H12 inverter. The H12 inverter has two outputs: RES_SYNC and RES_SYNC2. The output of the M74 inverter is also labeled RES_SYNC3.

3.2

8-frame delay for
RES -> RST
Same in k051962 ?

The diagram illustrates a circuit for achieving an 8-frame delay between the RES (Reset Enable) signal and the RST (Reset) signal. It consists of two P18 flip-flops, labeled P51 and P18, connected in series. The TRIG_IRQ signal is connected to the CLK input of P51. The RES_SYNC3 signal is connected to the CL input of P51. The Q output of P51 is connected to the CLK input of P18. The RES_SYNC3 signal is also connected to the CL input of P18. The Q output of P18 is connected to the RST signal. The FDR (Feedback) inputs of both flip-flops are connected to their respective Q outputs. The diagram shows that the RST signal is delayed by 8 frames relative to the RES signal.

3.3

Logic diagram for the 0x18XX Address decoder. The diagram shows the following components and connections:

- Input **AB9** is connected to inverter **C34** (V1N).
- Output of **C34** is connected to inverter **C32** (V1N).
- Output of **C32** is labeled **AB9_INV**.
- Input **AB8** is connected to inverter **E33** (V1N).
- Output of **E33** is connected to inverter **D44** (V1N).
- Output of **D44** is labeled **AB8_INV**.
- Input **AB7** is connected to inverter **E31** (V1N).
- Output of **E31** is connected to inverter **D46** (D46).
- Output of **D46** is labeled **AB7_INV**.
- Input **RMRD** is connected to inverter **D79** (K1B).
- Output of **D79** is labeled **RMRD_BUF**.
- Input **RMRD** is also connected to inverter **D78** (V2B).
- Output of **D78** is labeled **RMRD**.
- Inputs **AB12** (pin 1) and **AB11** (pin 2) are connected to the inputs of NAND gate **E46** (K3B).
- Output of **E46** (pin 3) is labeled **AB12AB11**.

0x18XX Address

3.4

Diagram illustrating the bit-slice configurations for the 74181 ALU, showing the input (DBn_IN), output (DBn_BUF), and carry input/output (K2B) for each slice:

- N135: DB0_IN, K2B, DB0_BUF
- N80: DB1_IN, K2B, DB1_BUF
- N132: DB2_IN, K2B, DB2_BUF
- N77: DB3_IN, K2B, DB3_BUF
- N83: DB4_IN, K2B, DB4_BUF
- N97: DB5_IN, K2B, DB5_BUF
- N100: DB6_IN, K2B, DB6_BUF
- N103: DB7_IN, K2B, DB7_BUF

3.5 Interrupts flags

The diagram illustrates the connection of interrupt flags to the P4, F27, and CC52 modules. The P4 module has inputs TRIG_IRQ, REG1D00_D2, and FDN, and output IRQ. The F27 module has inputs TRIG_FIRQ, REG1D00_D1, and FDN, and output FIRQ. The CC52 module has inputs TRIG_NMI, REG1D00_D0, and FDN, and output NMI. All three modules are connected to a common ground line.

3.6

The logic diagram for Figure 3-6, titled "CPU_VRAM_CS0 and CPU_VRAM_CS1", illustrates a complex digital circuit. The inputs are CPU_VRAM_CS0, CPU_VRAM_CS1, REG1C00_D0, REG1C00_D1, REG1C00_D2, REG1C00_D4, A126, and R2P. The circuit consists of several logic gates and inverters, labeled B125, B123, B127, B129, B121, A151, B119, B134, A154, B132, B142, B137, B143, B139, B147, B149, B152, L143, L147, and L148. The output is DB_DIR. The circuit is organized into several stages, with inputs being processed through various gates and inverters to produce the final output. The diagram is a detailed representation of the hardware logic for the CPU_VRAM_CS0 and CPU_VRAM_CS1 signals.

3.7

Reg 1C00 bits 0 and 1 used for VRAM map and chip configuration

REG1C00_D[1:0]:

	A101	A106	A111
00	0~1	2~3	4~5
01	2~3	4~5	6~7
10	4~5	6~7	8~9
11	6~7	8~9	A~B

3.8

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graph LR
    CPU_VRAM_CS1_1[CPU_VRAM_CS1] -- 1 --> A39
    CPU_VRAM_CS0_1[CPU_VRAM_CS0] -- 2 --> A39
    A39 -- 3 --> A41
    WREN --> A41
    K4B --> A41
    A41 --> VD_HIGH_DIR
    CPU_VRAM_CS1_2[CPU_VRAM_CS1] --> L12
    WRP --> L12
    L12 -- R2P --> RWE1
    L12 --> L15
    L15 -- V2B --> V2B
  
```

3.9

Scroll interval 32/256 set

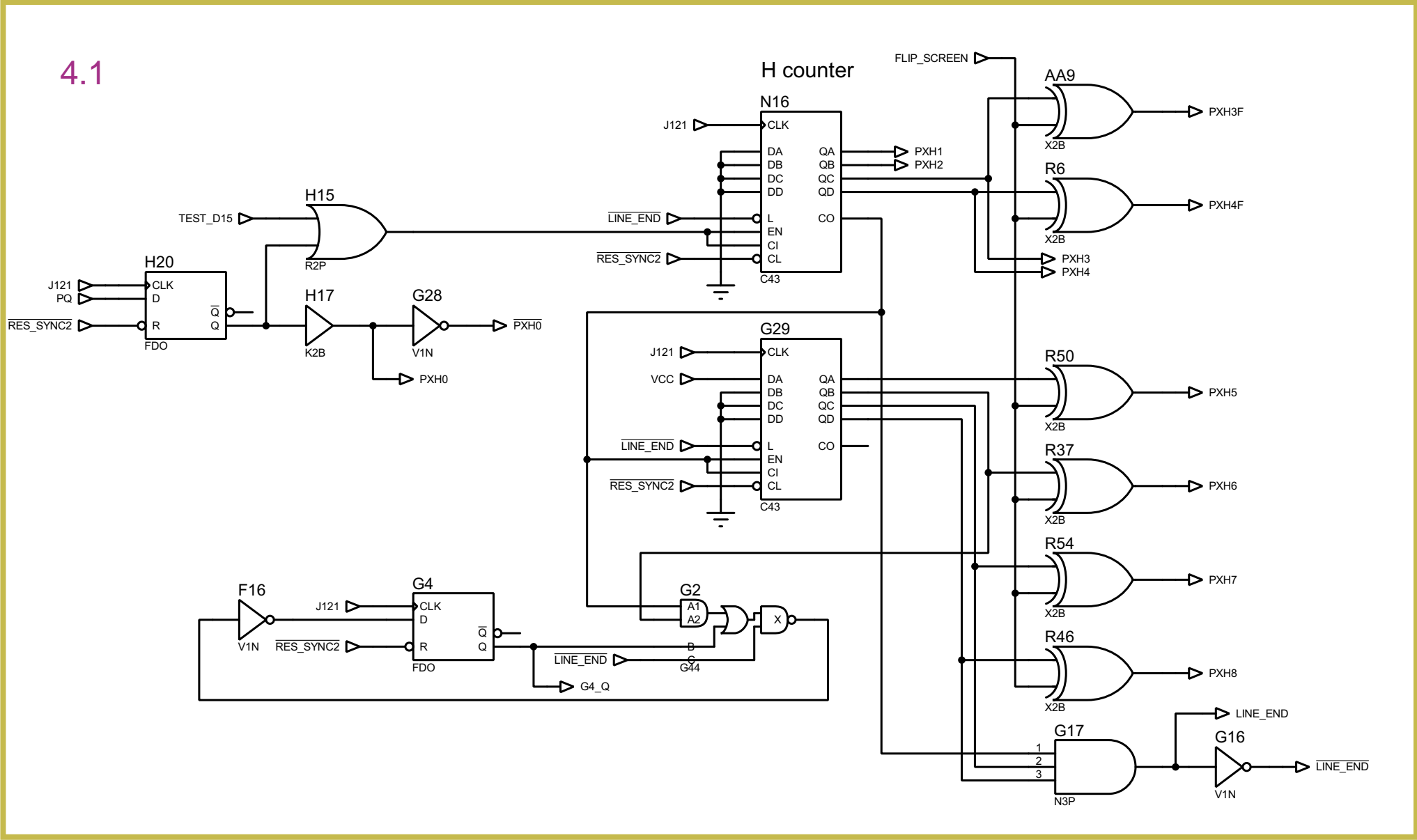
REG1C80_D0
G29_OA
E38
N2P
E40
R2P
E42
V1N
REG1C80_D3
AA61
ROW0
AA59
ROW1
AA63
ROW2
PXH3F
FLIP_SCREEN
PXH4F
PXH5
PXH6
Z3
A1
B1
A2
B2
A3
B3
A4
B4
Cl
A4H
S1
S2
S3
S4
CO
PXH7
PXH8
Z53
A1
B1
A2
B2
Cl
A2N
S1
S2
CO
AA75
A1
A2
B1
B2
D24
X
AA80
V1N
SCROLL_RAM_A0
AA65
A1
A2
B1
B2
D24
X
AA78
V1N
SCROLL_RAM_A1
AA67
A1
A2
B1
B2
D24
X
Z154
V1N
SCROLL_RAM_A2
AA69
A1
A2
B1
B2
D24
X
Z136
V1N
SCROLL_RAM_A3
AA71
A1
A2
B1
B2
D24
X
Z156
V1N
SCROLL_RAM_A4
AA73
A1
A2
B1
B2
D24
X
Z134
V1N
SCROLL_RAM_A5
ROW3
ROW4

3.10

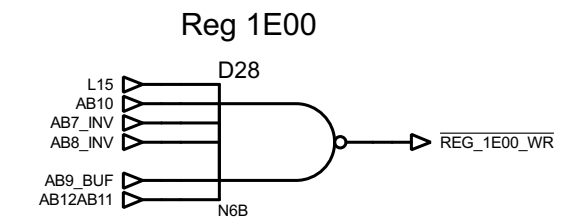
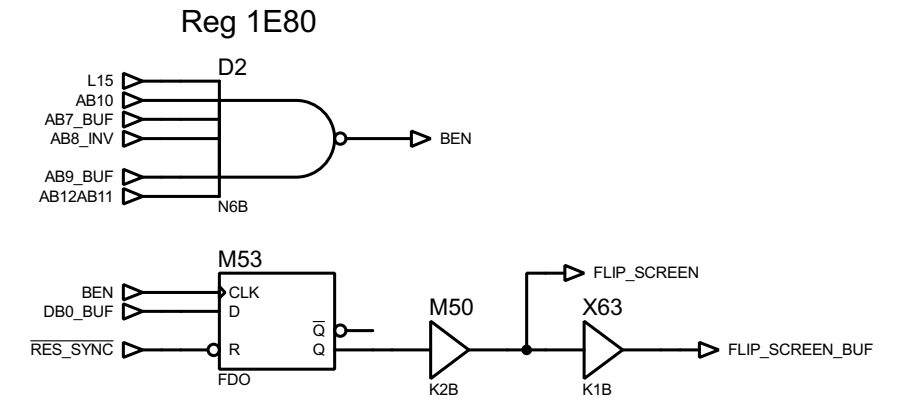
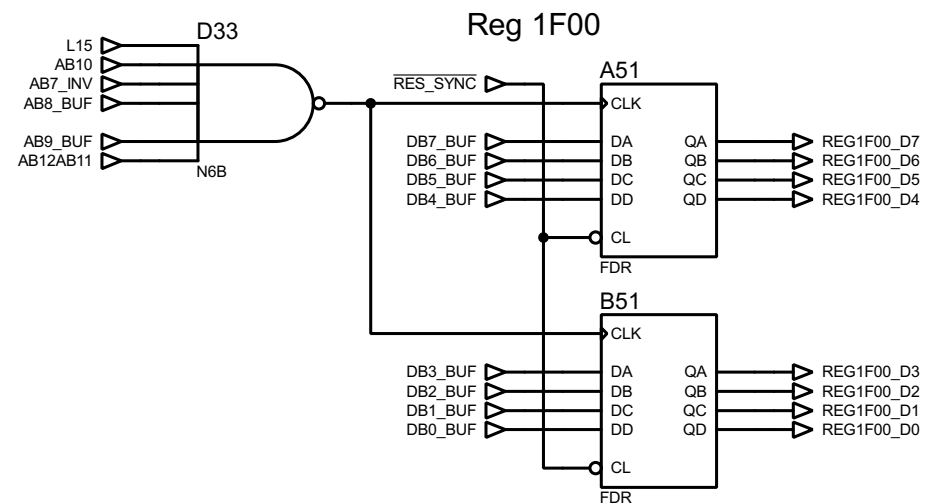
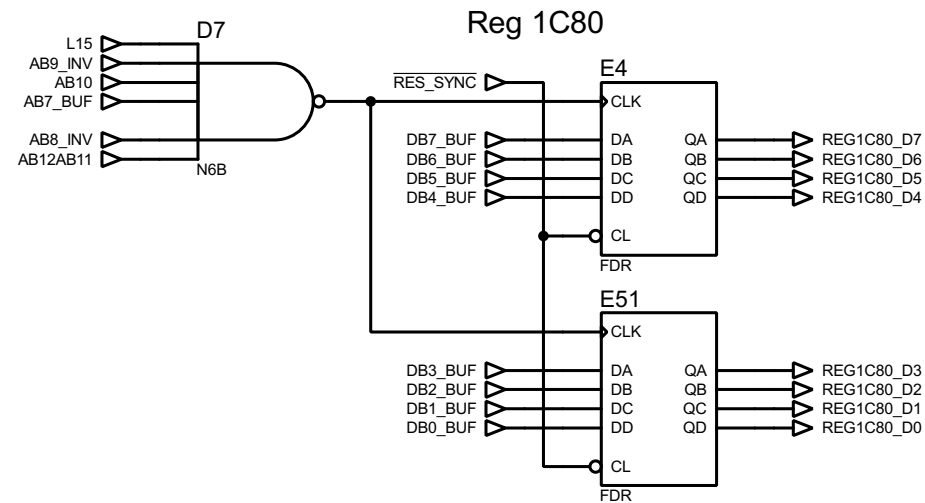
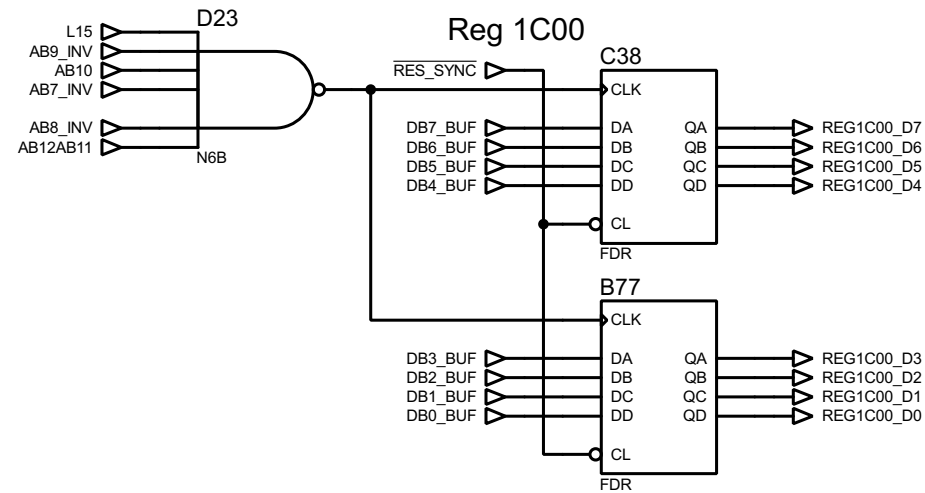
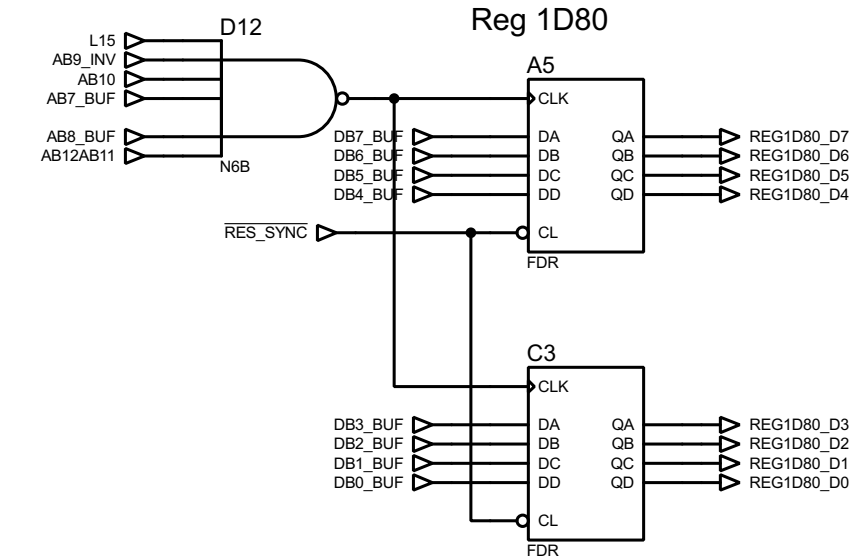
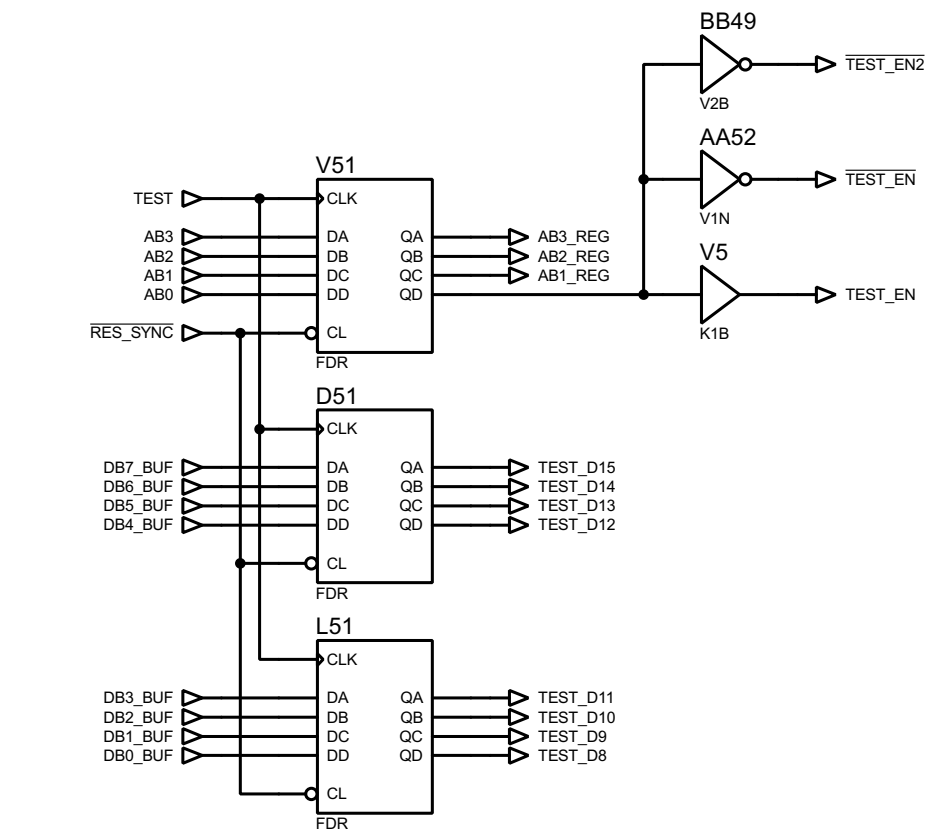
The diagram illustrates an 8-bit parallel adder using four 74181 ALU chips (M77, M100, L95, M117) and two 74182 carry look-ahead chips (L147, L148). The ALU chips are configured to perform 8-bit parallel addition. The carry look-ahead chips generate carry signals (V2B) for each stage. The final output is DB7_OUT.

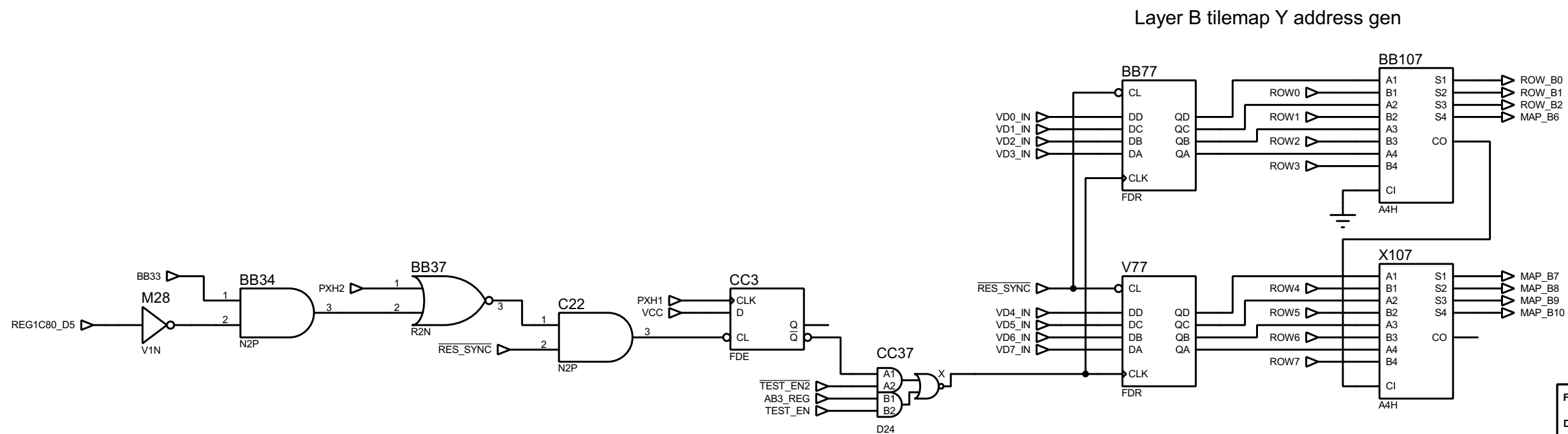
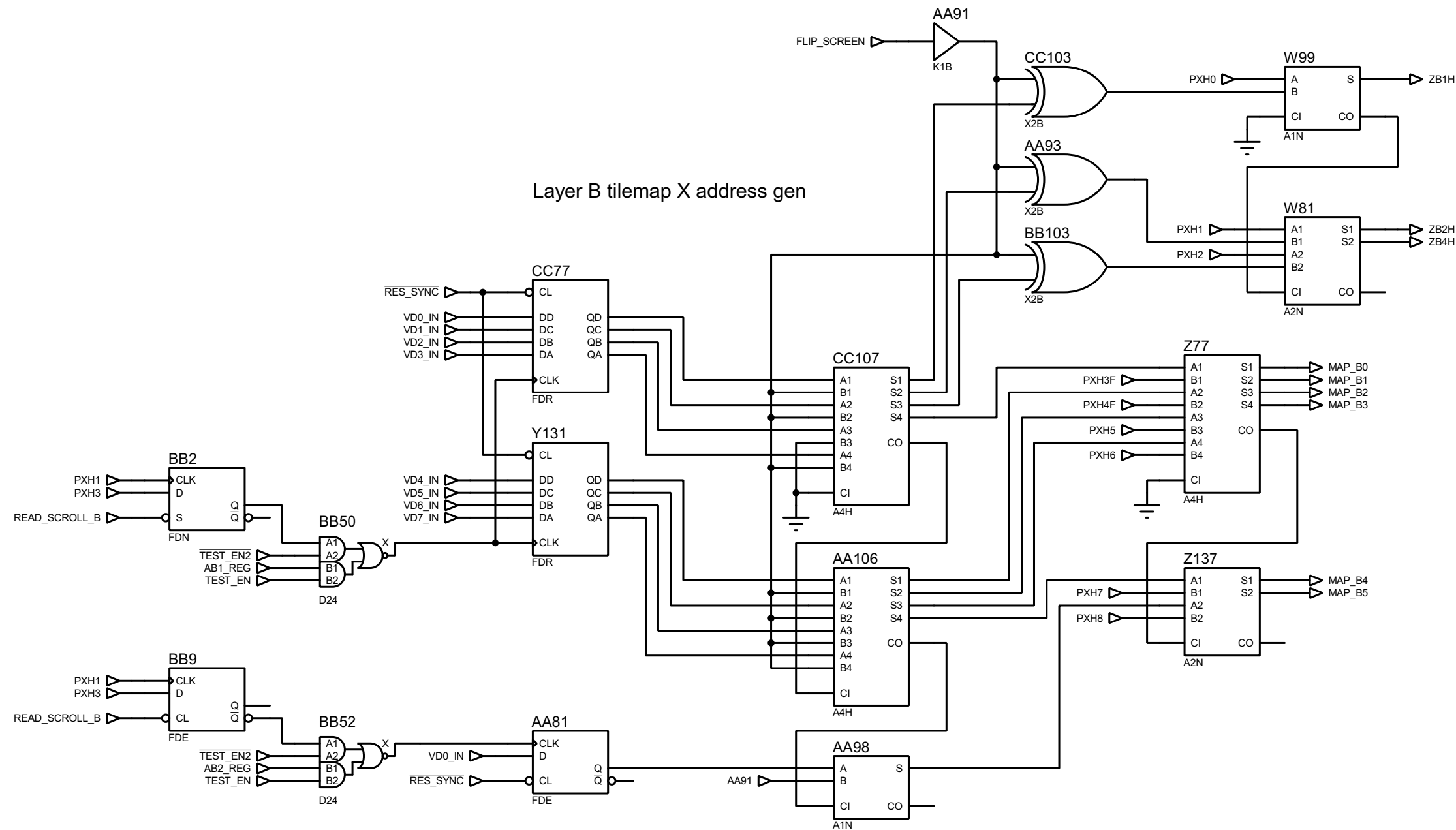
4.2

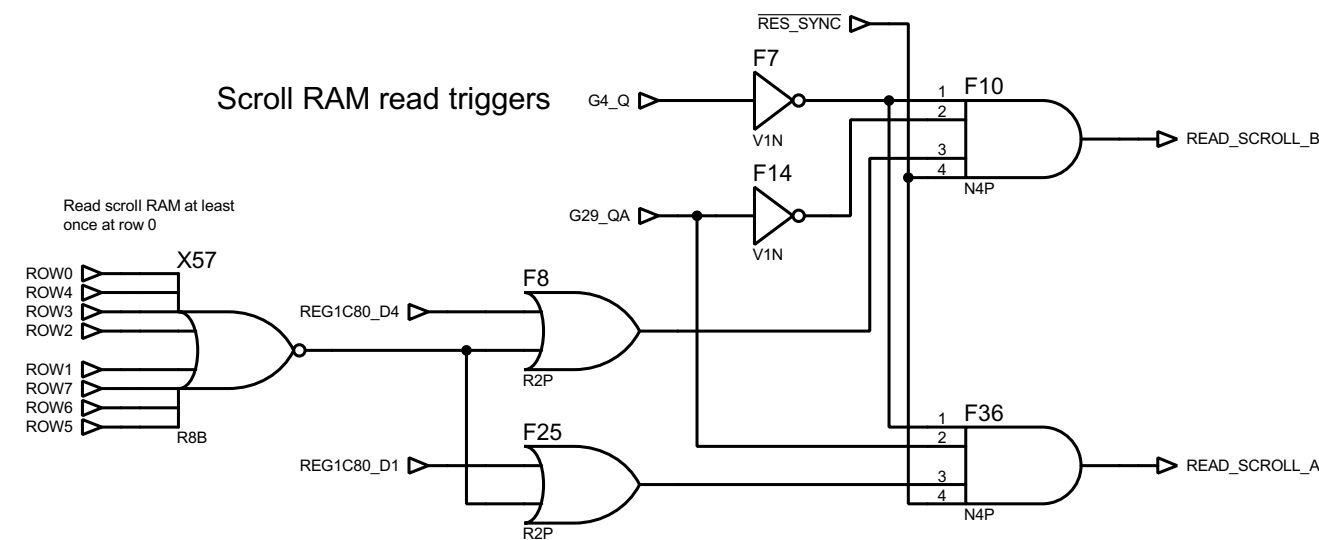
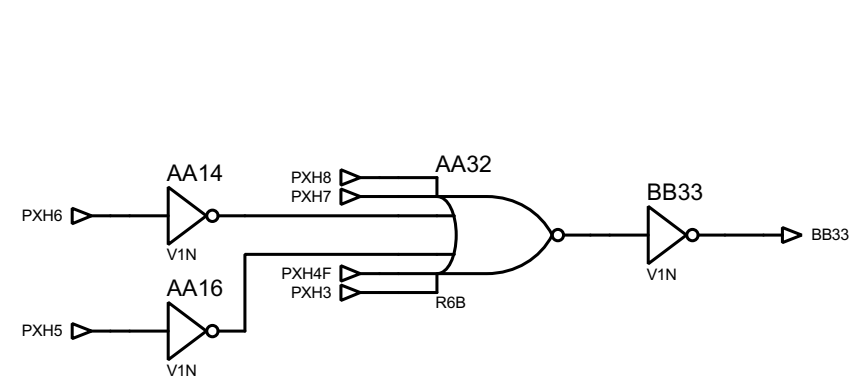
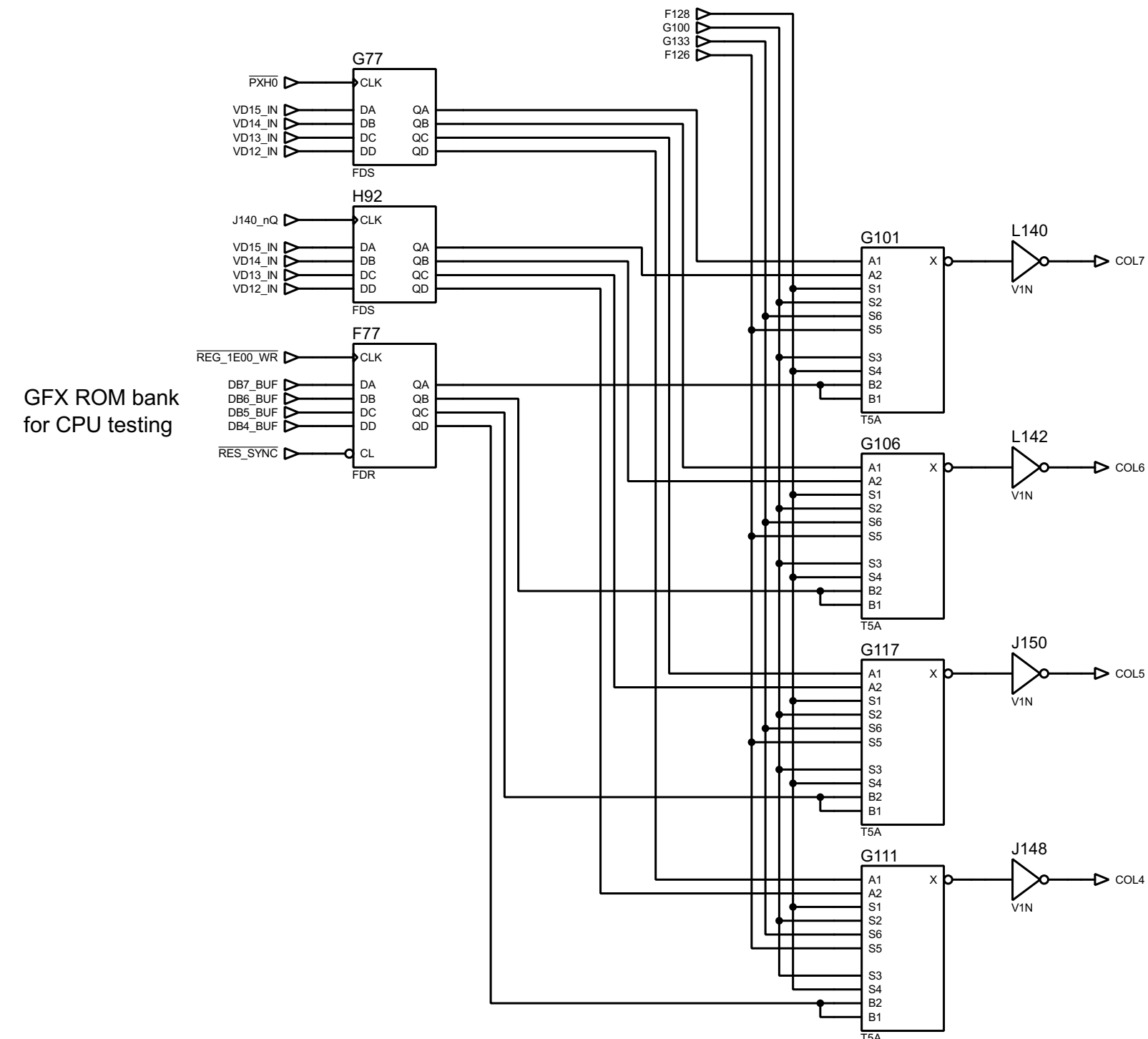
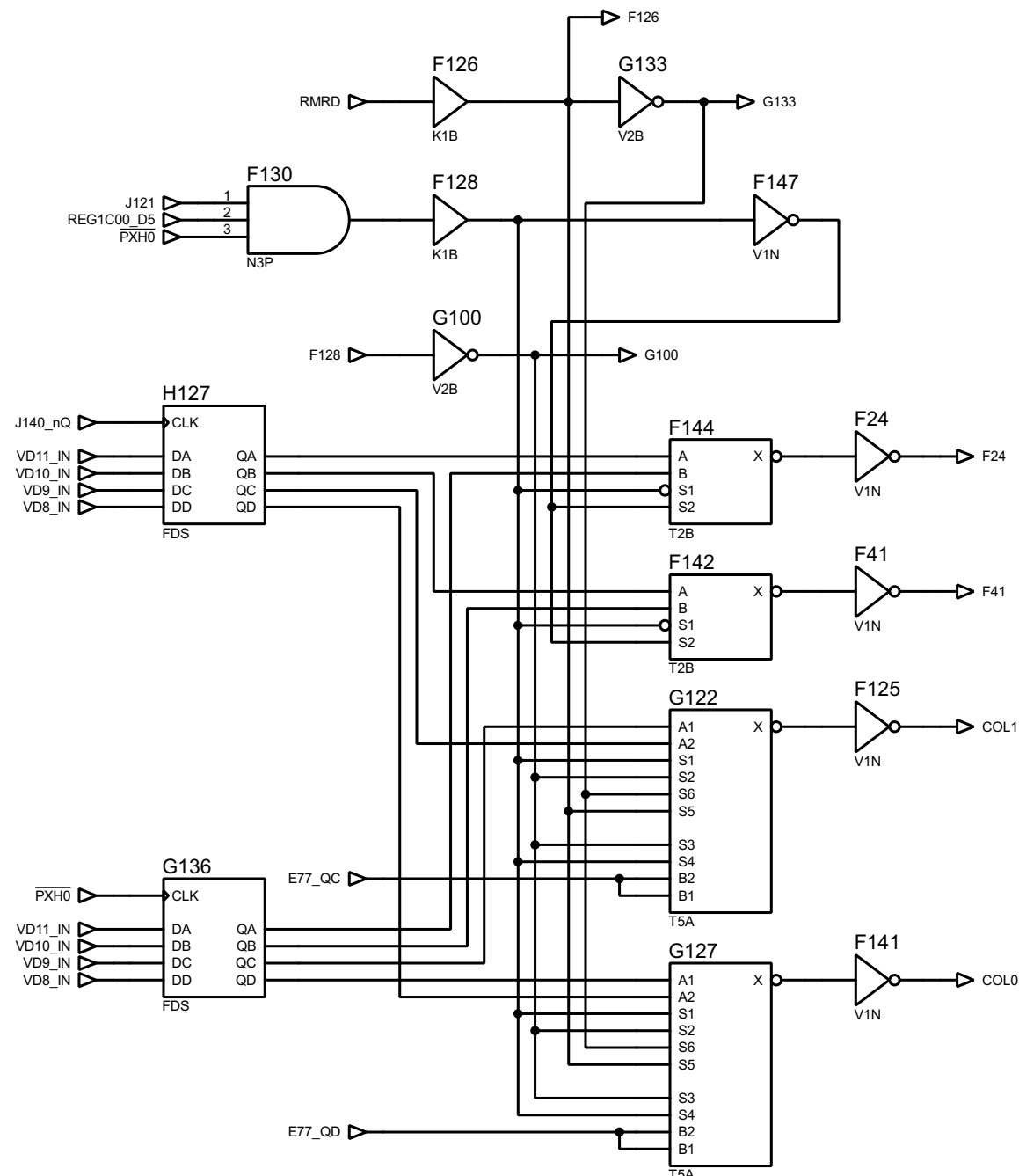
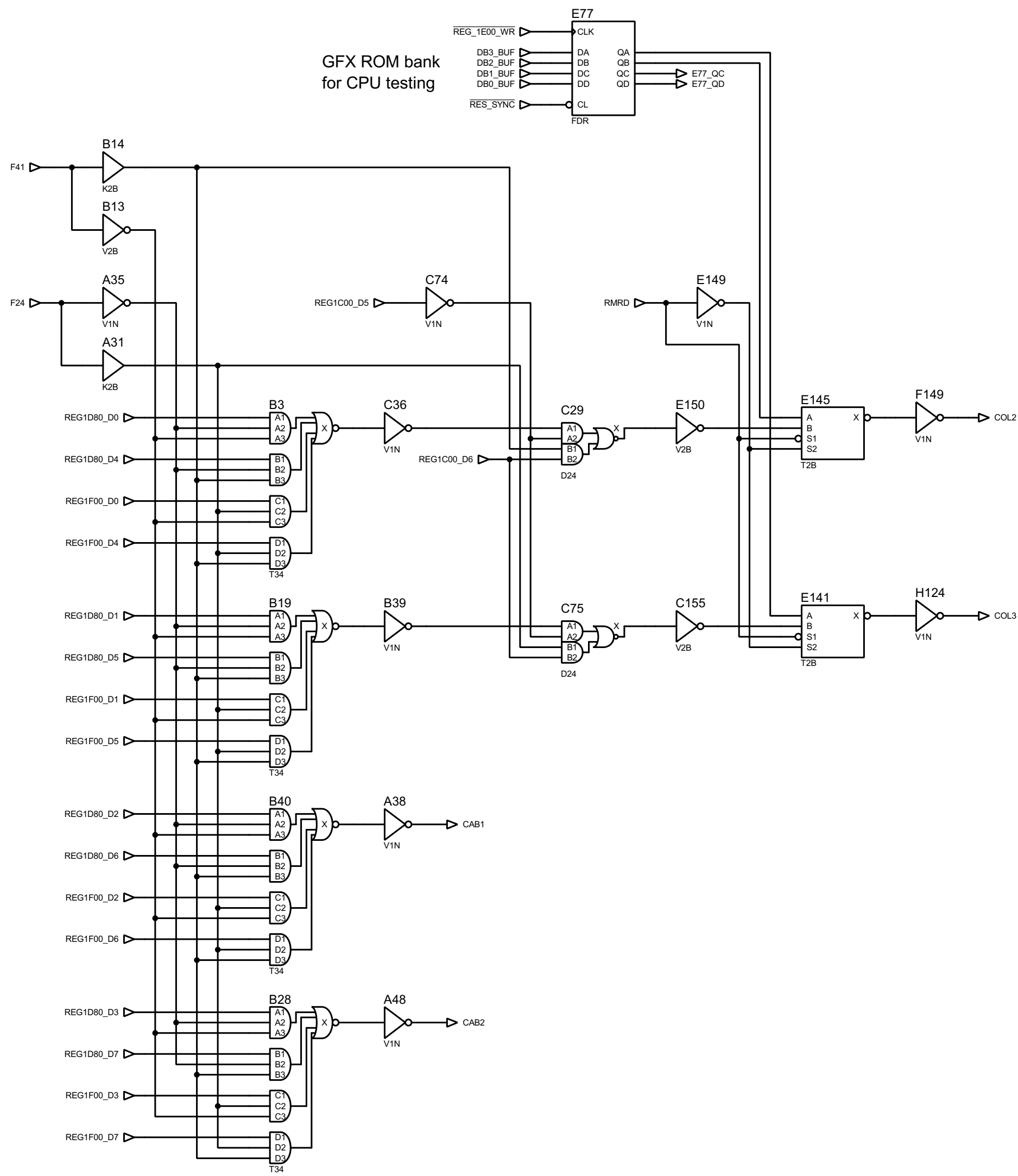
The diagram illustrates the logic for the V counter and row drivers. The V counter (J29) is a 4-bit counter with inputs CLK, DA, DB, DC, DD, L, EN, CI, CL, and CO. Its outputs QA, QB, QC, and QD are connected to row drivers (R58, R25, AA18, R29, R33, R73, R69, R65) and a row driver enable signal (RES_SYNC). The counter also controls a row driver enable signal (RES_SYNC2) and a row driver enable signal (RES_SYNC). The counter's outputs are connected to row drivers (R58, R25, AA18, R29, R33, R73, R69, R65) and a row driver enable signal (RES_SYNC). The counter also controls a row driver enable signal (RES_SYNC2) and a row driver enable signal (RES_SYNC).



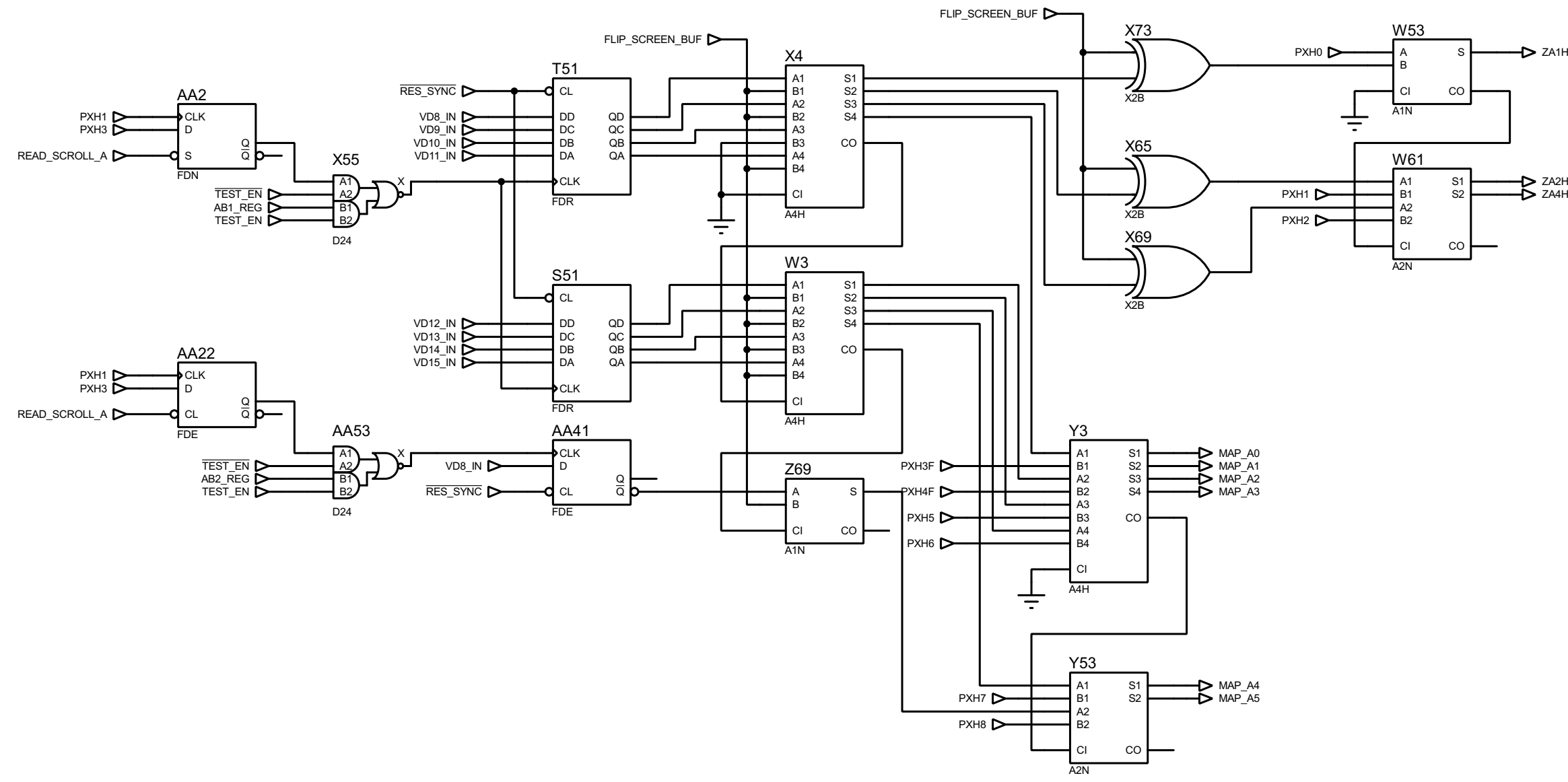
4.3







Layer A tilemap X address gen



Layer A tilemap Y address gen

