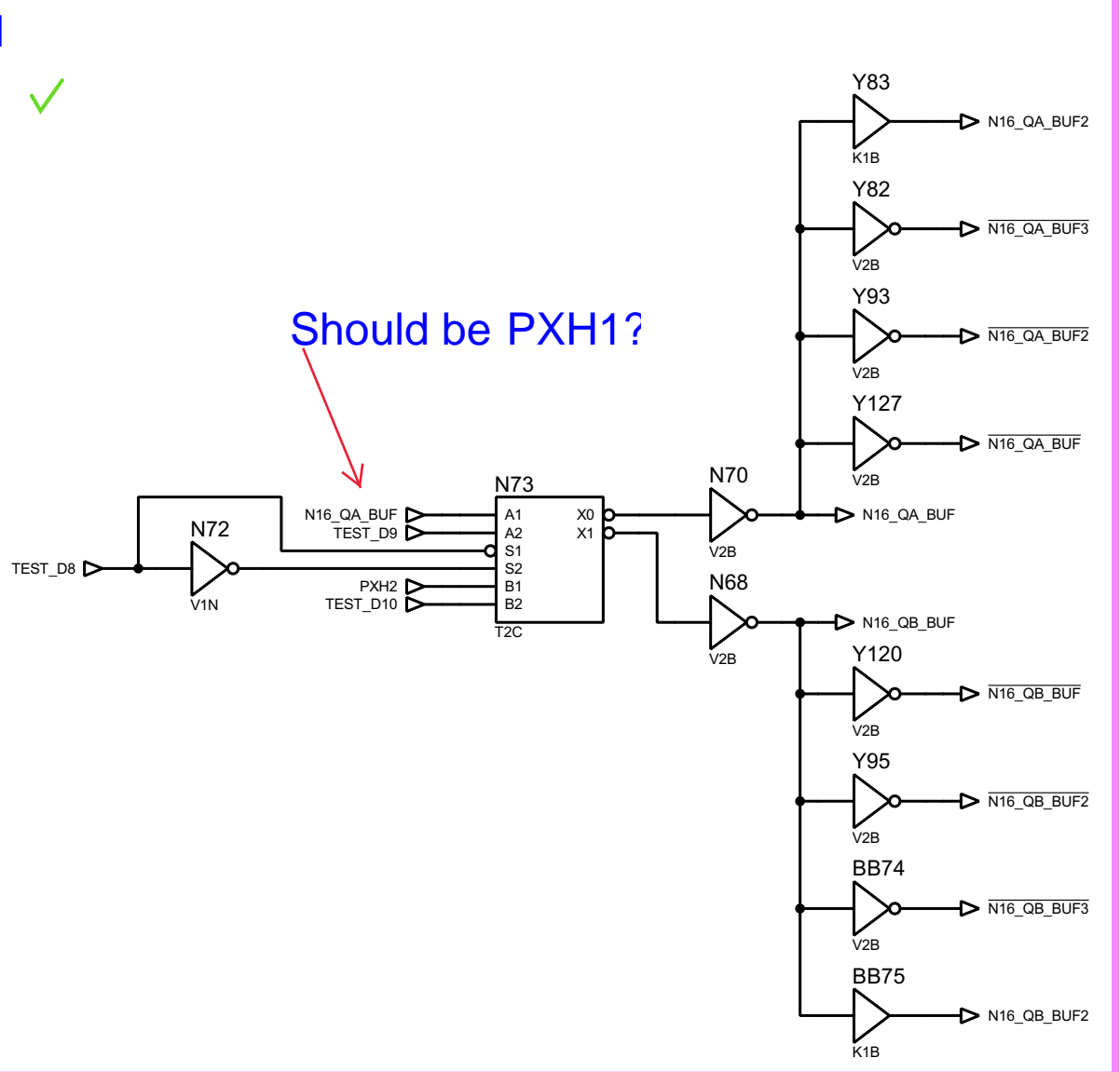


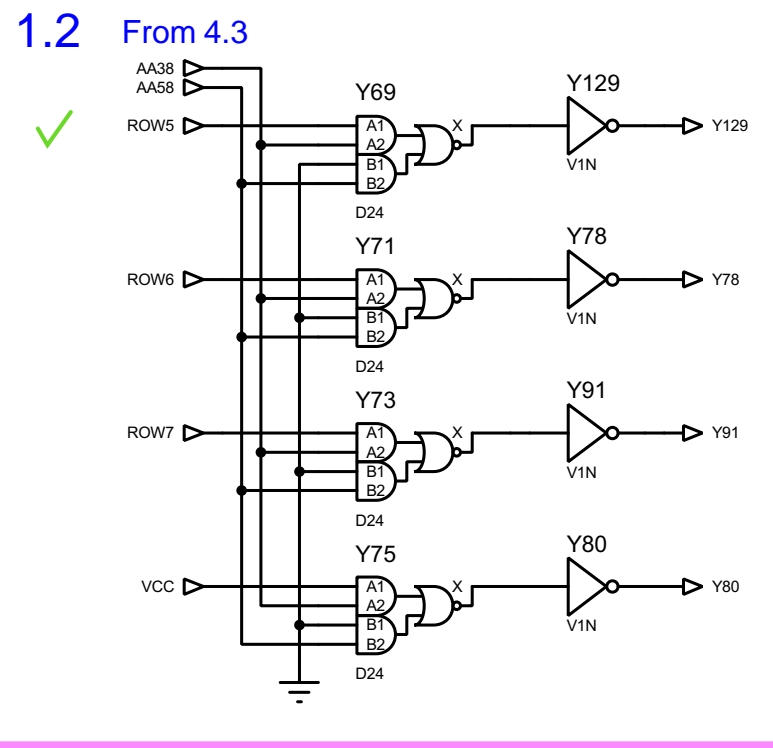
```

VRAM Address (1 word per address)
FEDC BA98 7654 3210
0000 00xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 11xx xxxx xxxx Layer C tilemap
0000 1101 xxxx xxxx A X scroll
0001 00xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 1100 xxxx xxxx B Y scroll
0001 1101 x xxxx X tilemaps X
          xx xxx Tilemaps Y

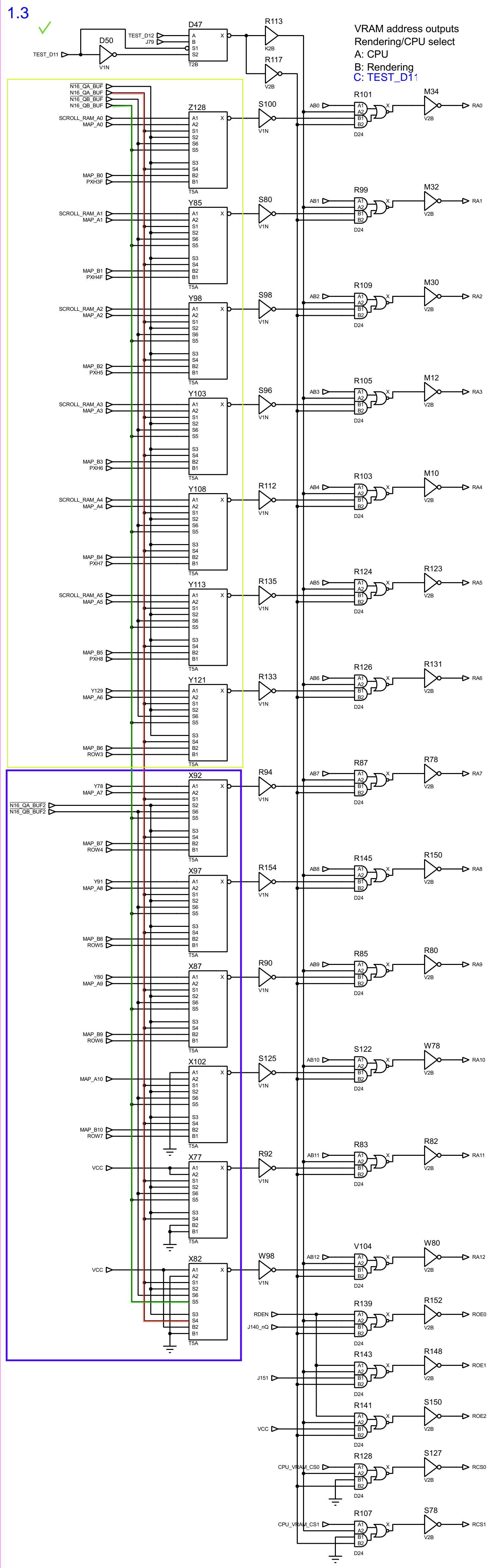
```

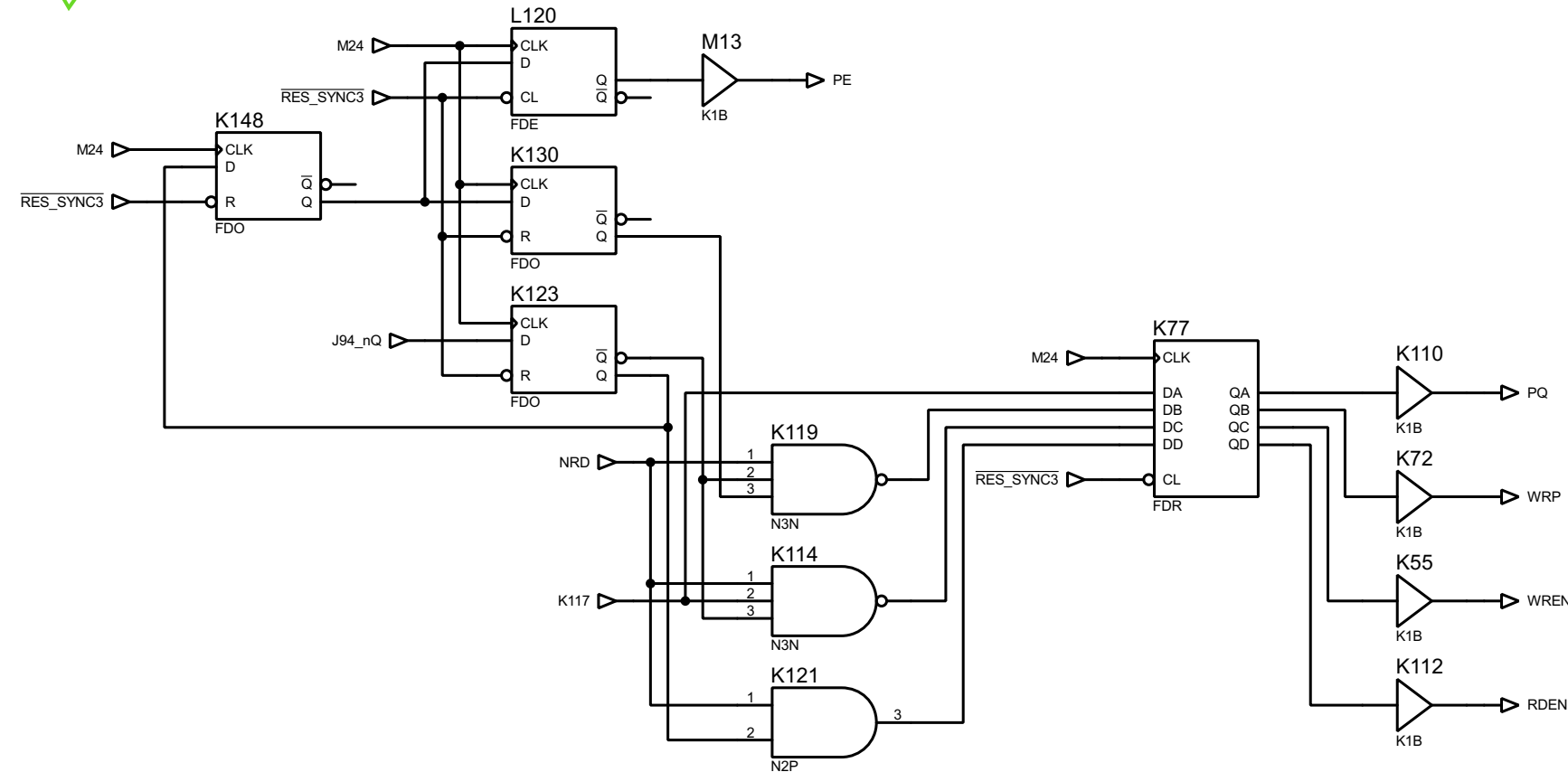
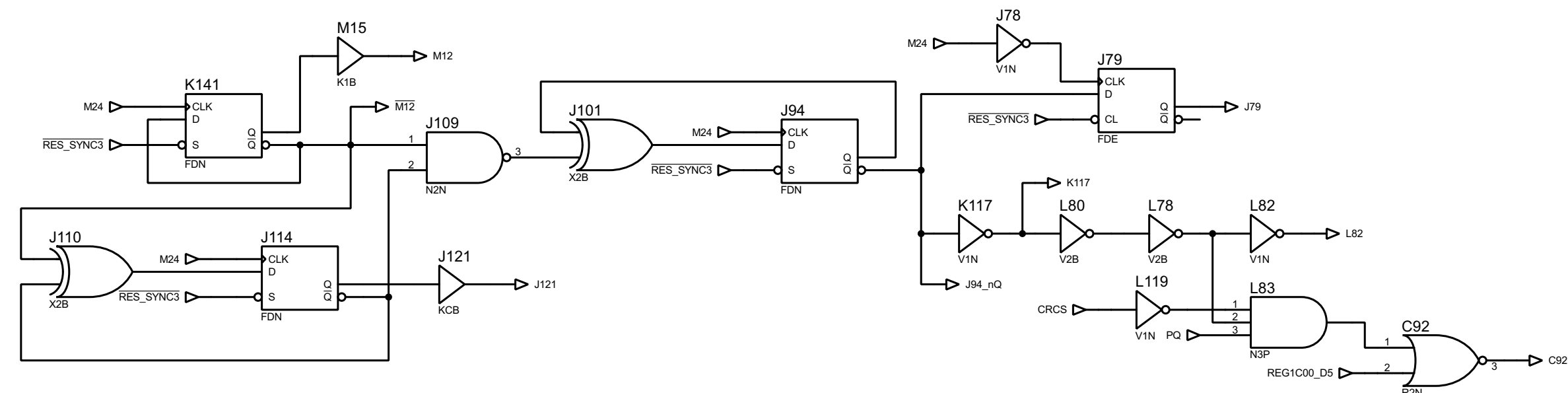


## TEST\_D13 Addresses Selector



Selection can be simplified using AA38 (and AA38n) only  
AA58 always selects 1'b0.

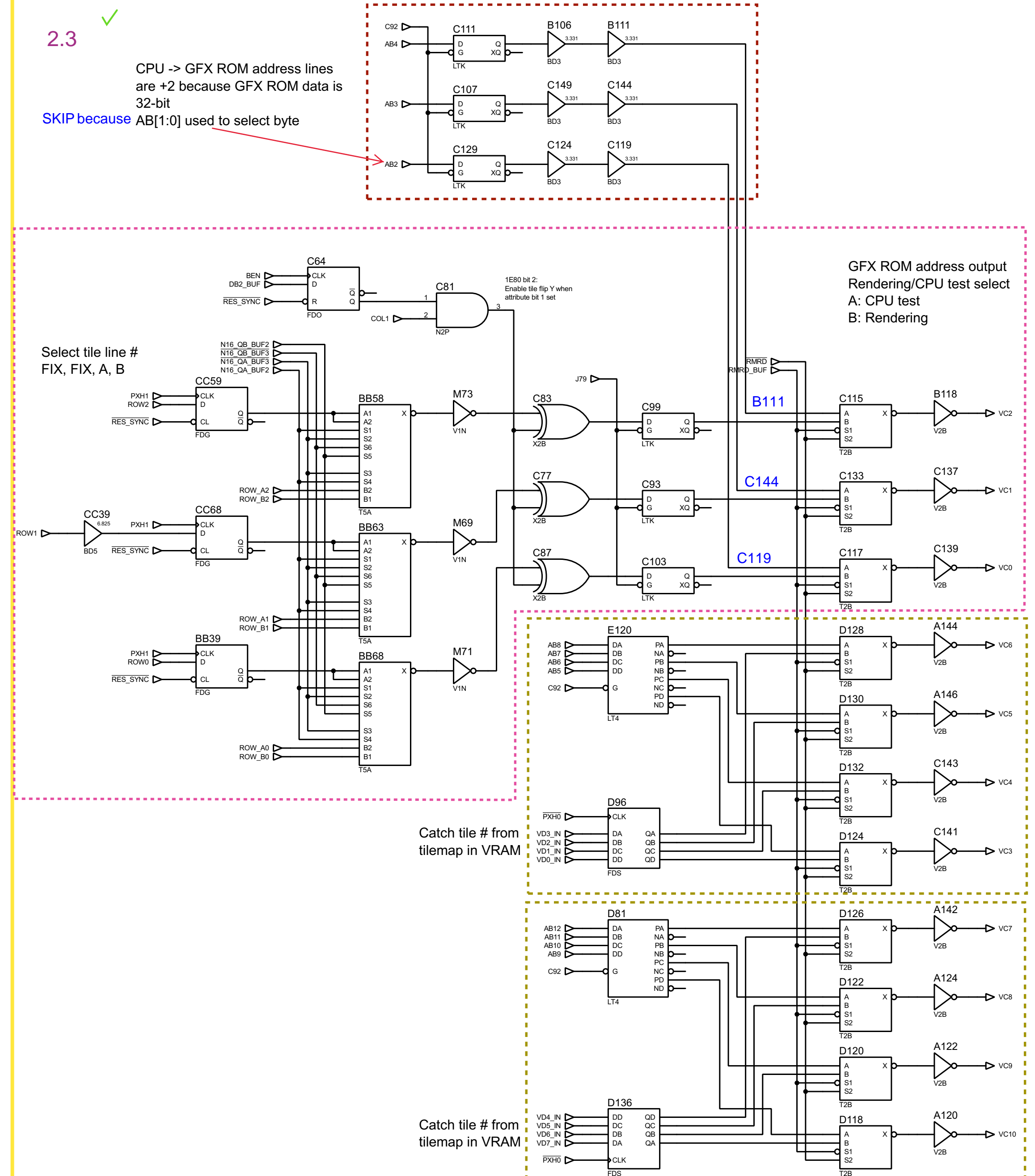




FILE NAME: <b>k052109.pdsprj</b>	DATE: <b>22/06/2021</b>
DESIGN TITLE: <b>Konami 052109 GFX ROM ADDRESS</b>	PAGE: <b>2 of 8</b>
BY: Sean Gonsalves	REV: A

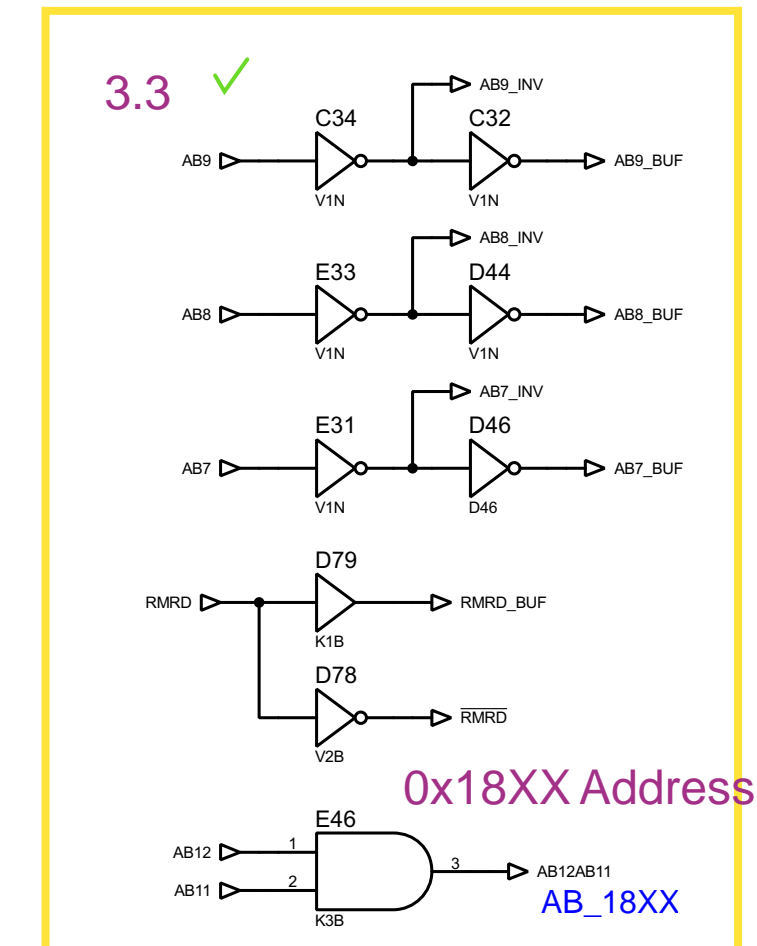
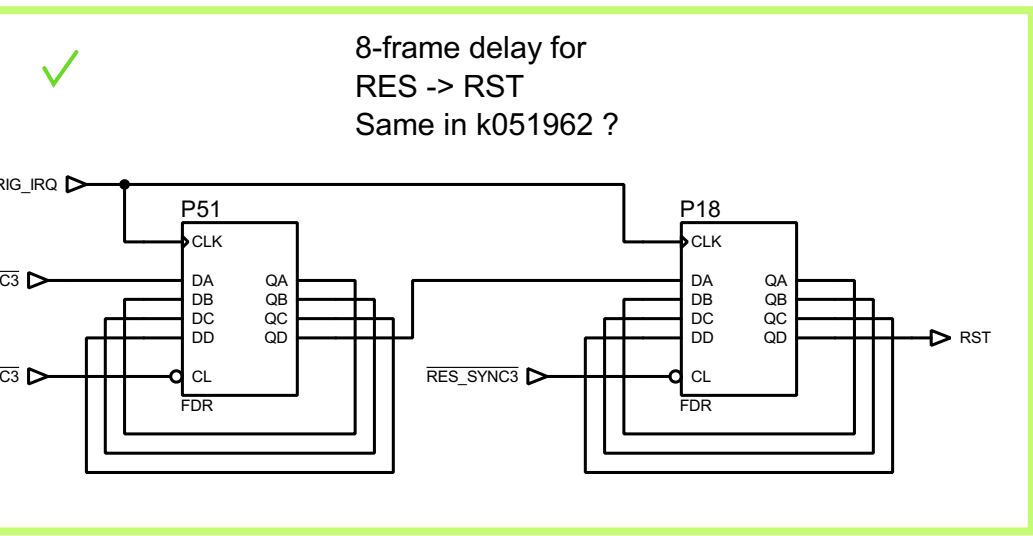


SKIP because AB[1:0] used to select byte



### 3.1 ✓

The diagram shows a circuit for a 3-bit counter. It consists of three main components: an N122 flip-flop, an M74 3-to-8 decoder, and an H12 3-input OR gate. The N122 flip-flop has inputs M04 (CLK), V02 (D), and RES (CL), and a feedback input FDE. Its output Q is connected to the M74 decoder's input K2B. The M74 decoder has three outputs: RES\_SYNC3, RES\_SYNC, and RES\_SYNC2. The H12 OR gate has three inputs connected to these three outputs, and its output is labeled RES\_SYNC2.

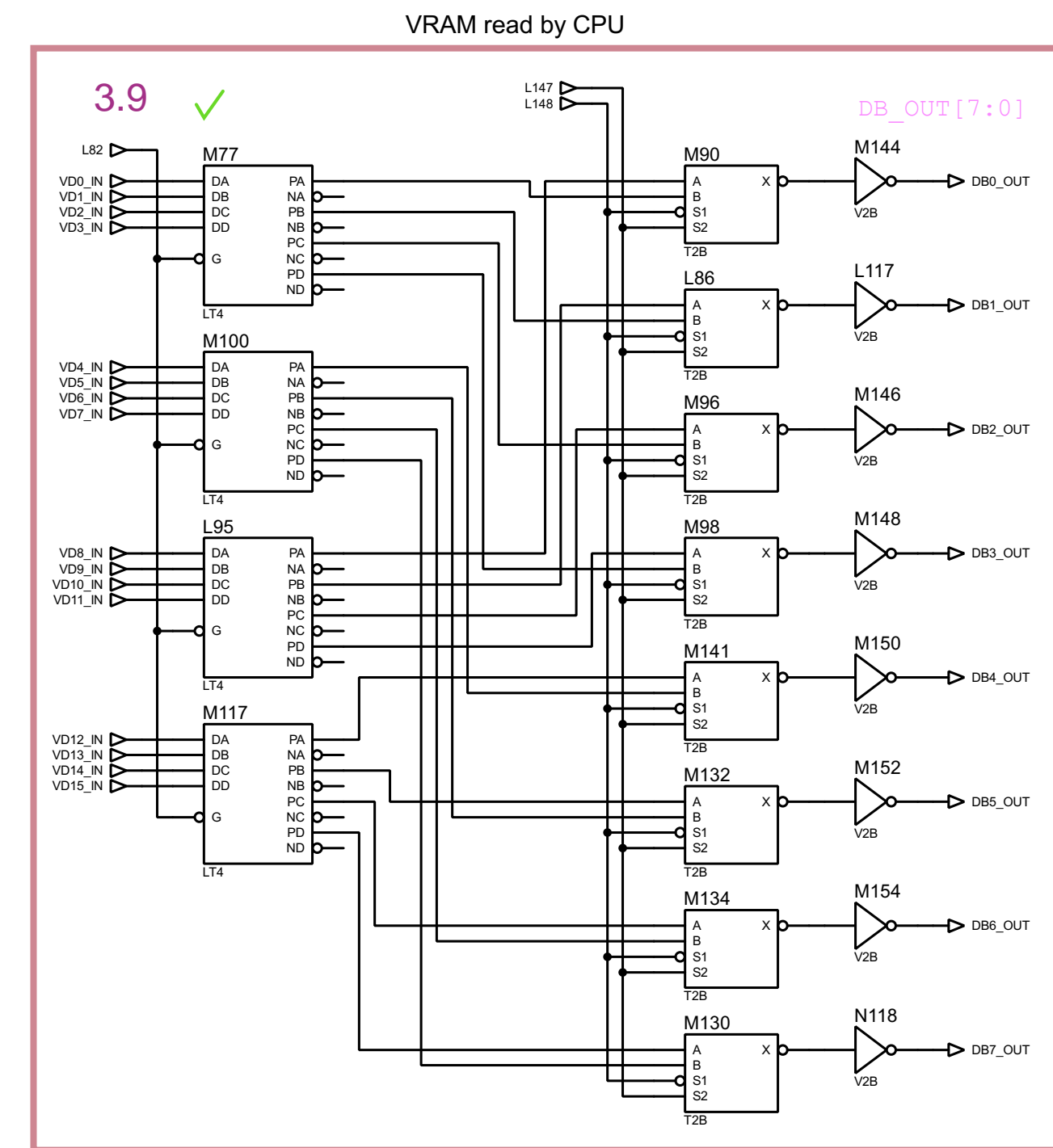
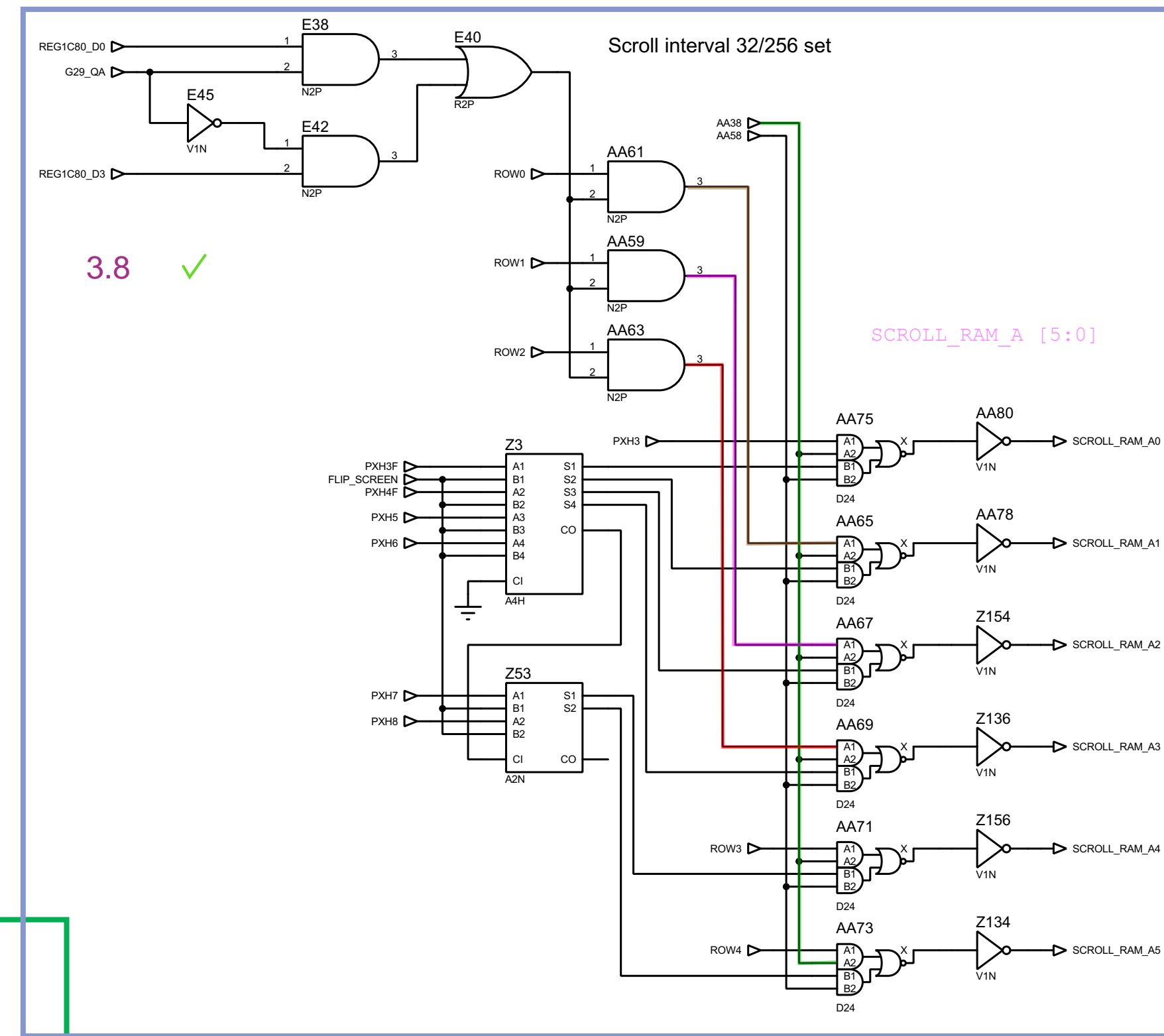
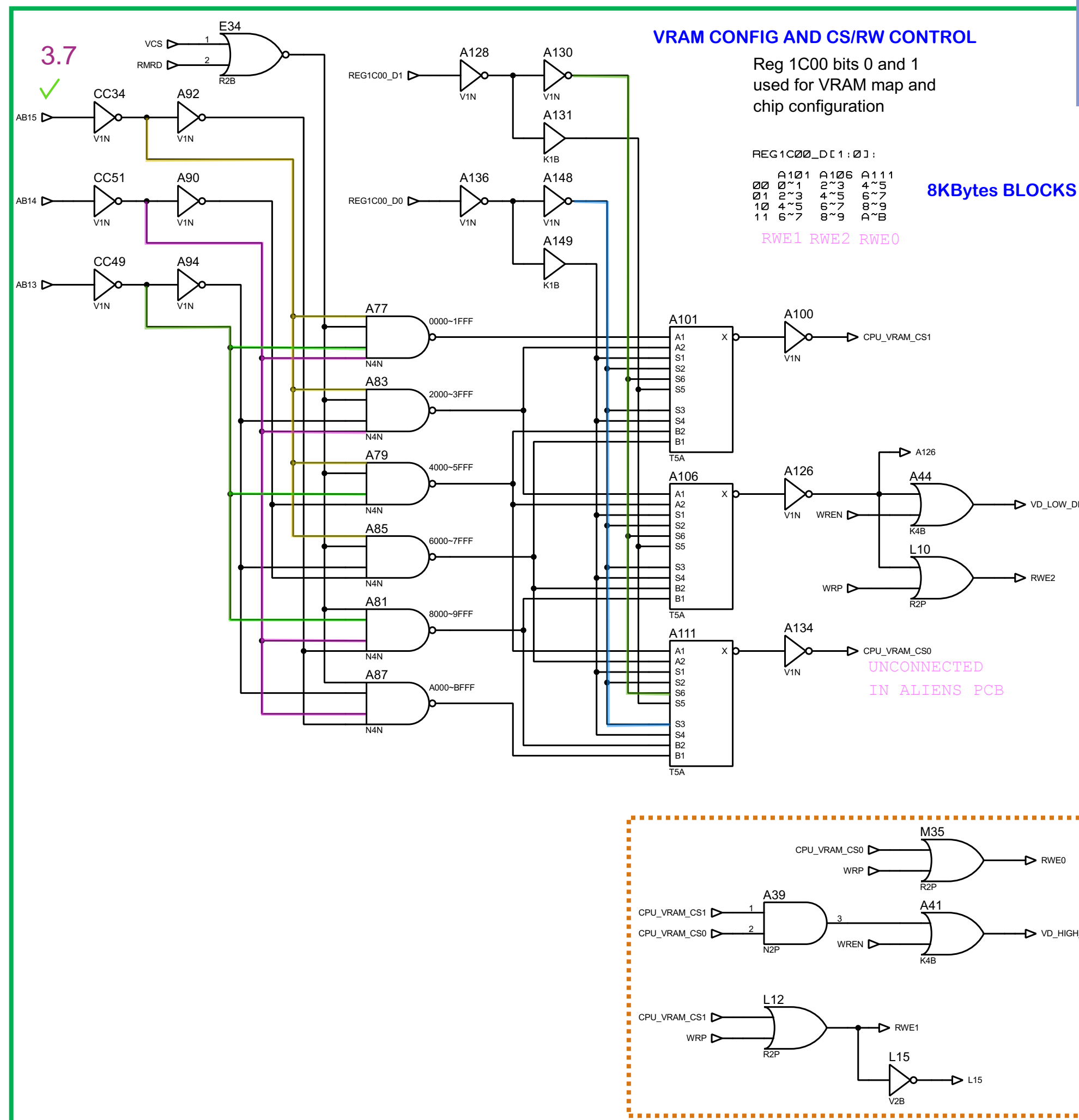
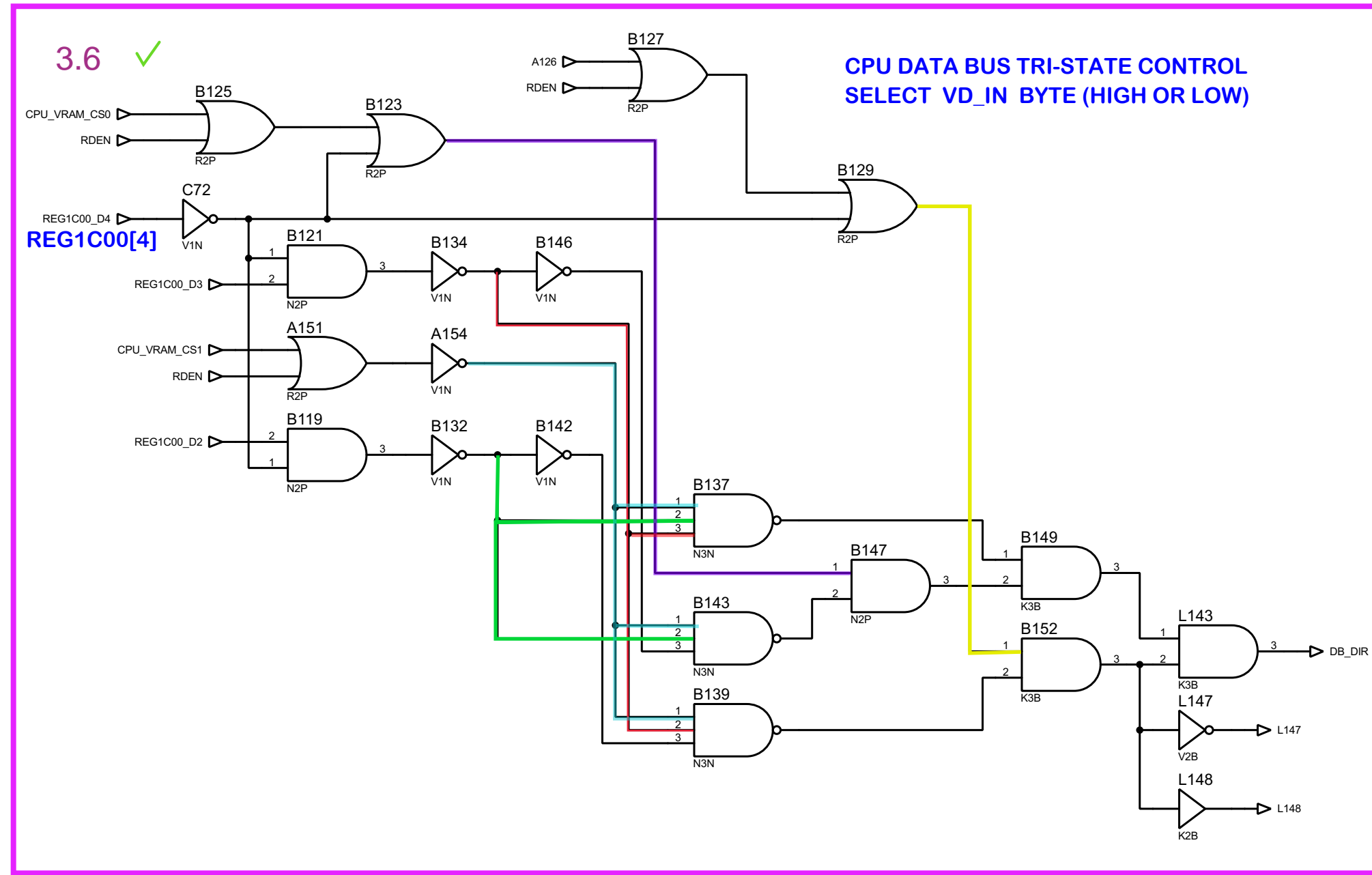


### 3.4 ✓

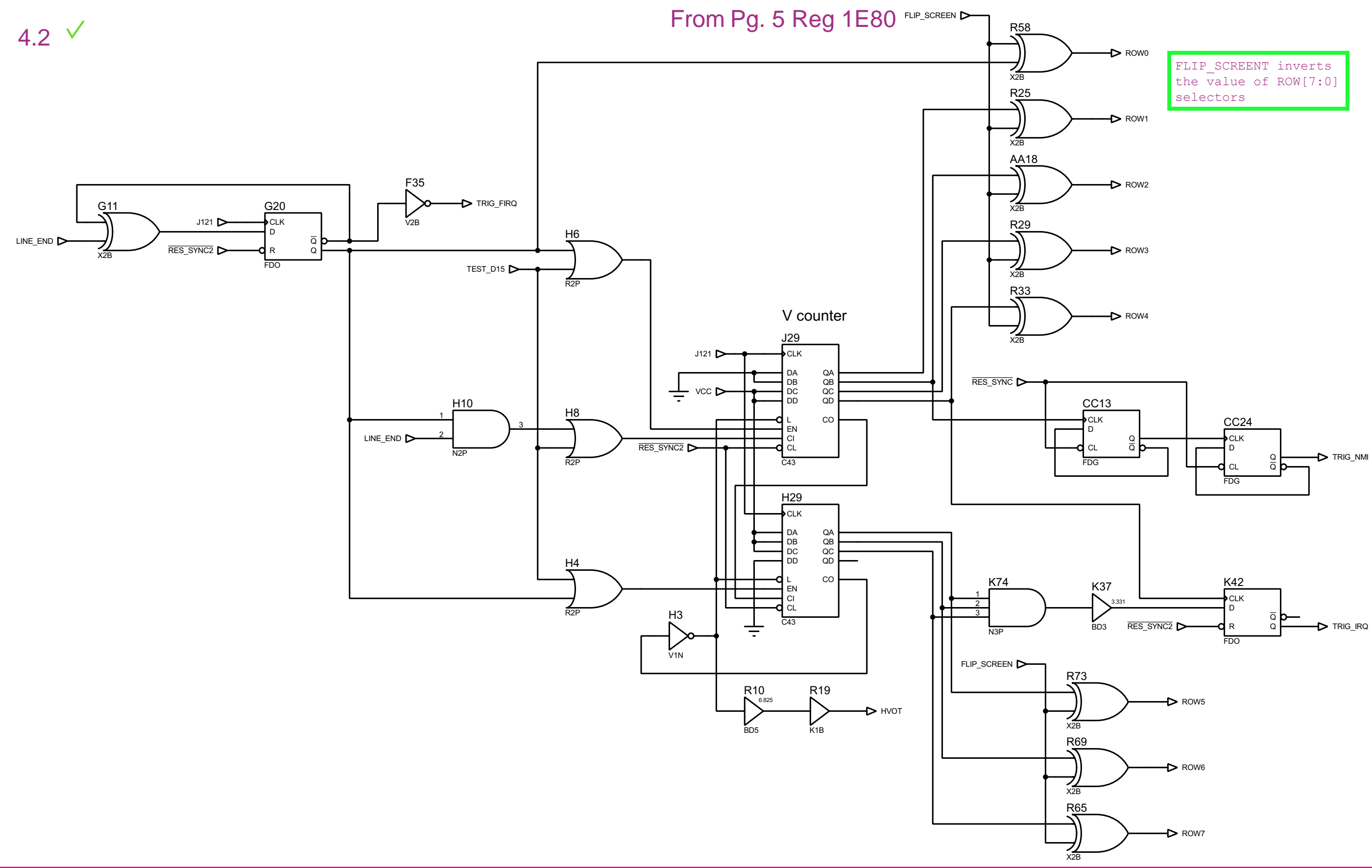
The diagram illustrates a set of 8 input buffers (DB0\_IN to DB7\_IN) connected to 8 output buffers (DB0\_BUF to DB7\_BUF) via inverters (N135, N80, N132, N77, N83, N97, N100, N103). Each inverter is labeled K2B.

```
wire [7:0] DB_BUF
```

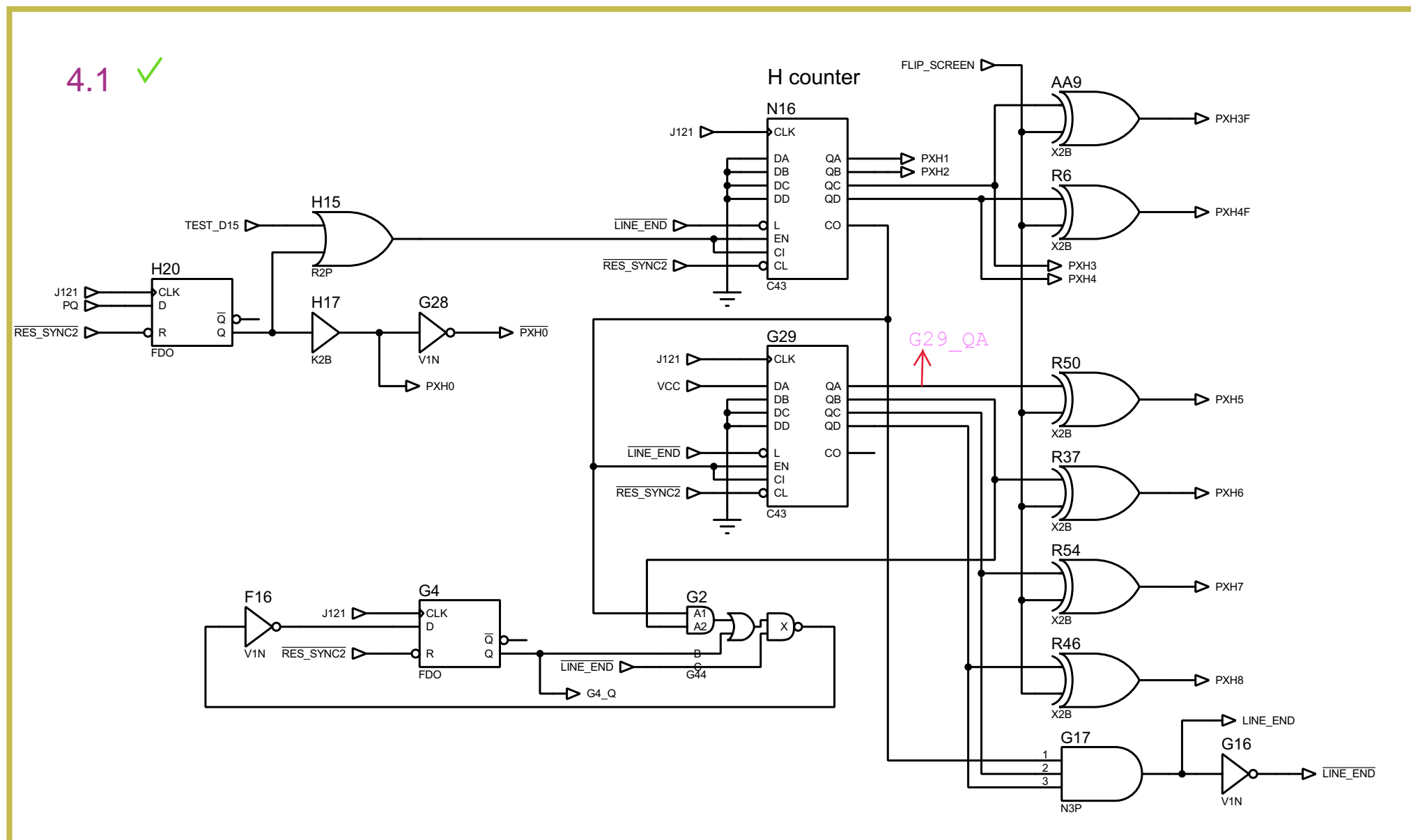
### 3.5 ✓ Interrupts flags



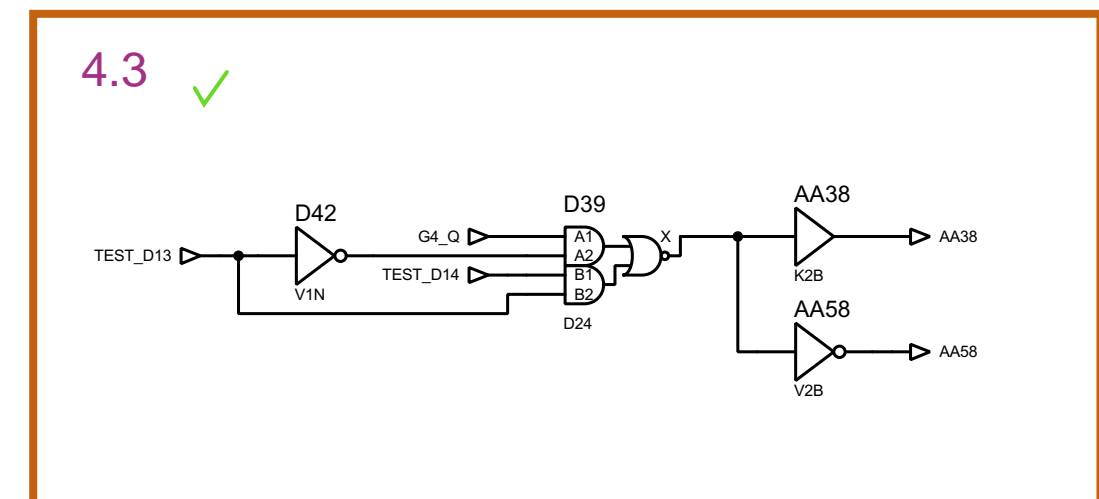
4.2 ✓



4.1 ✓

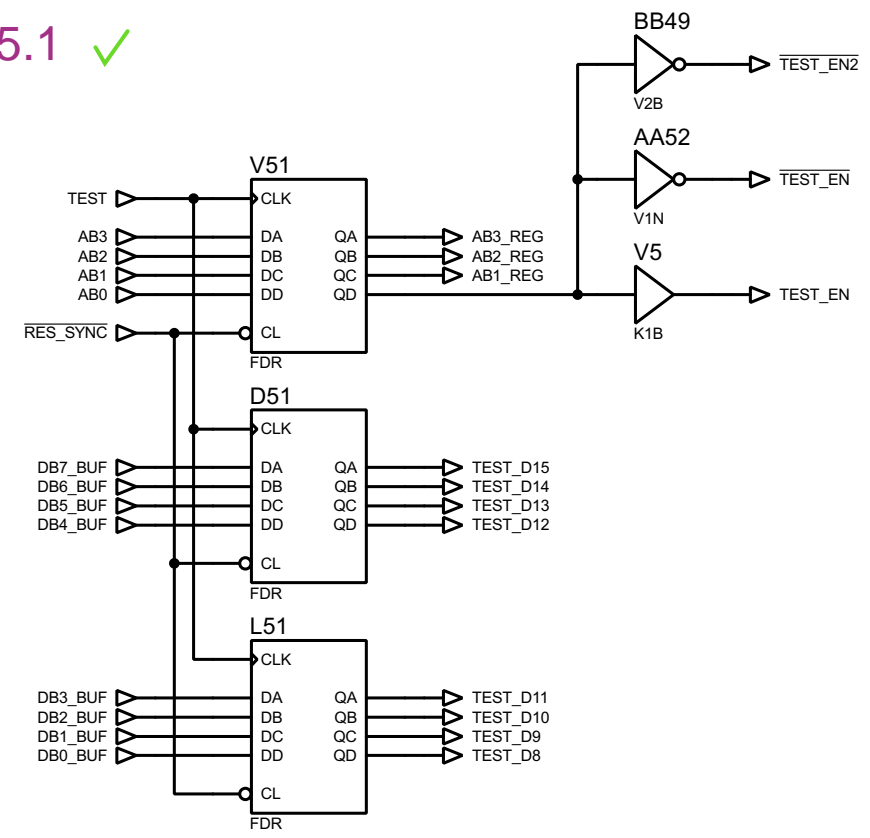


4.3 ✓

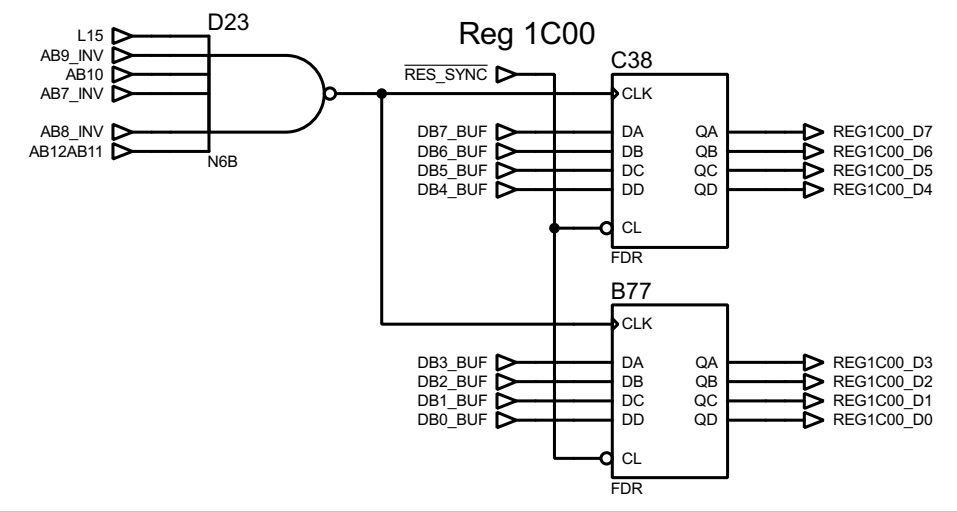




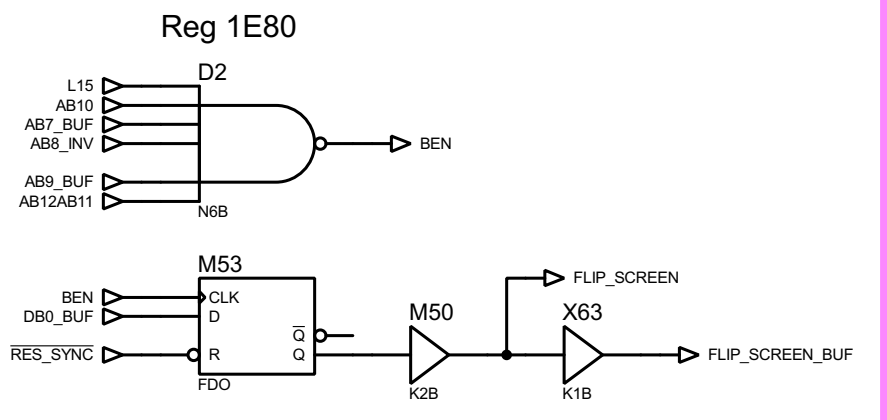
5.1 ✓



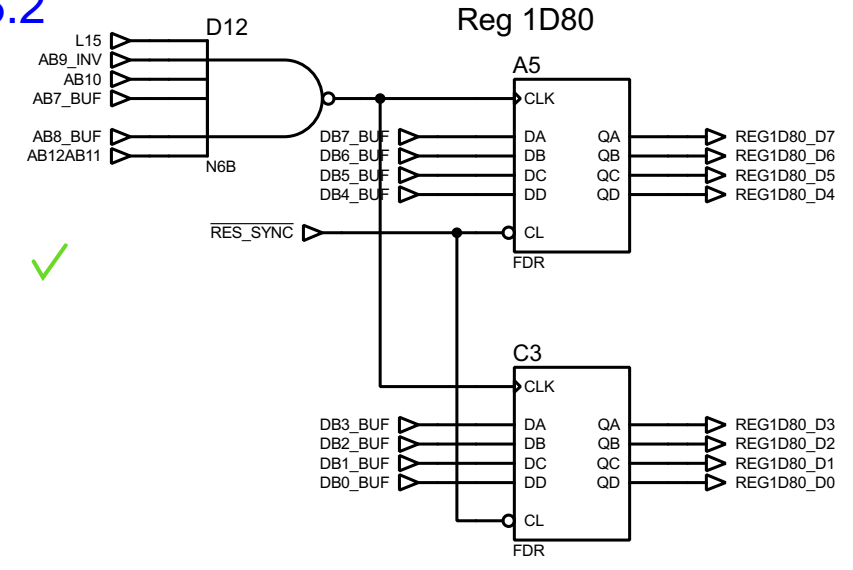
5.4 ✓



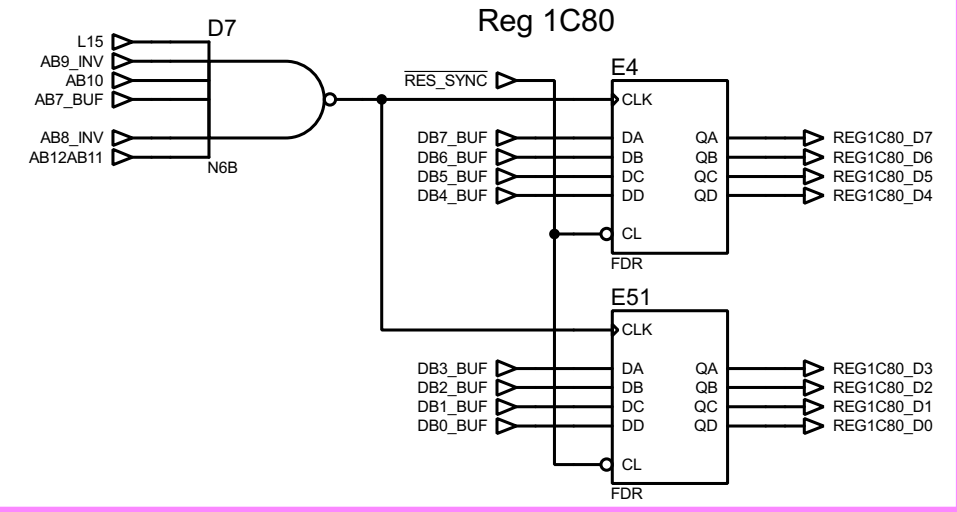
5.7 ✓



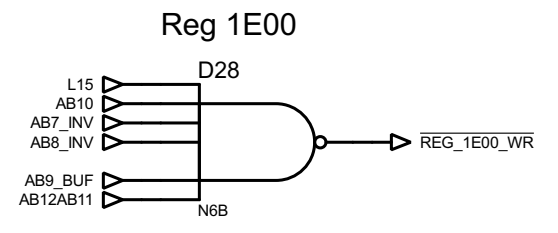
5.2 ✓



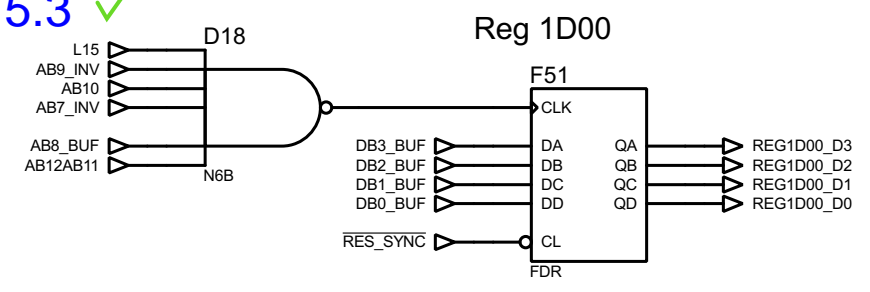
5.5 ✓



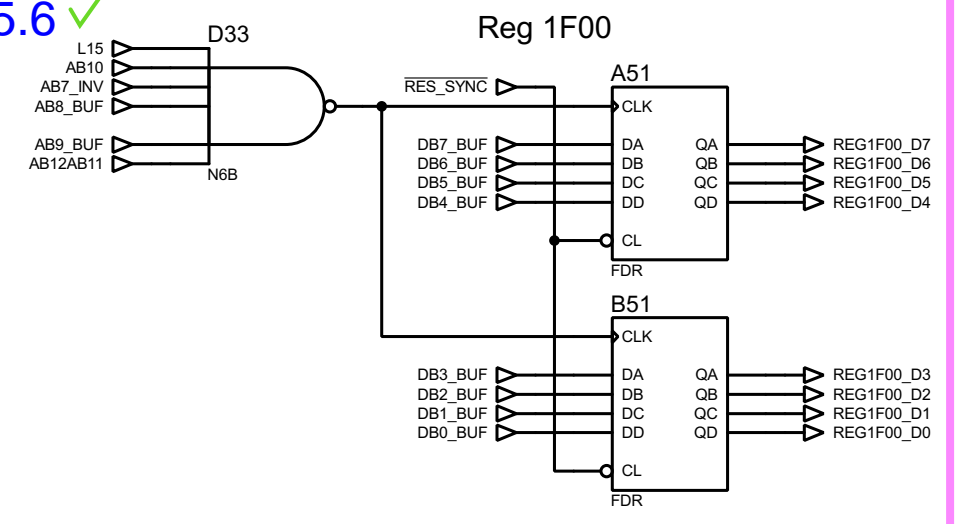
5.8 ✓



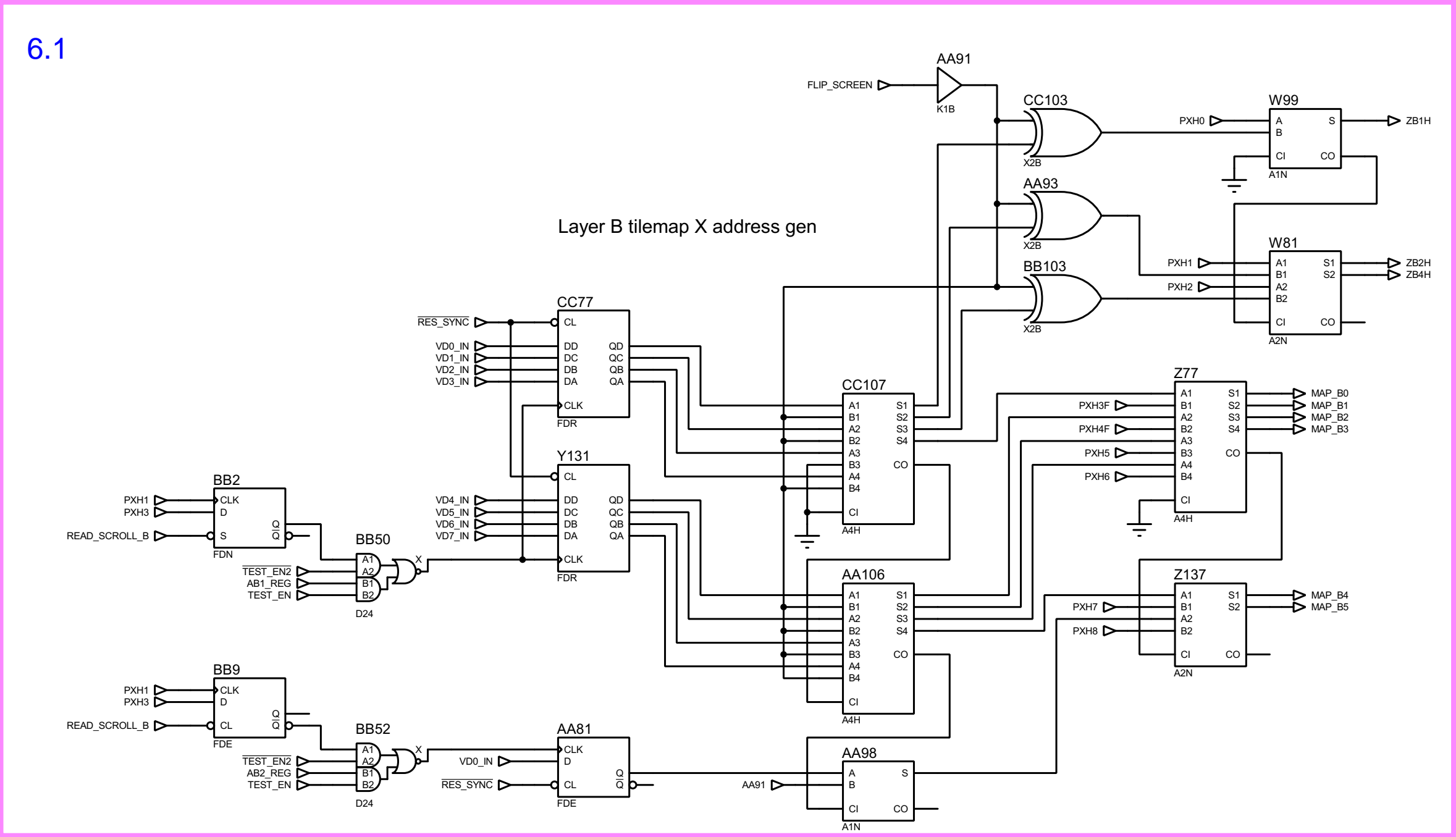
5.3 ✓



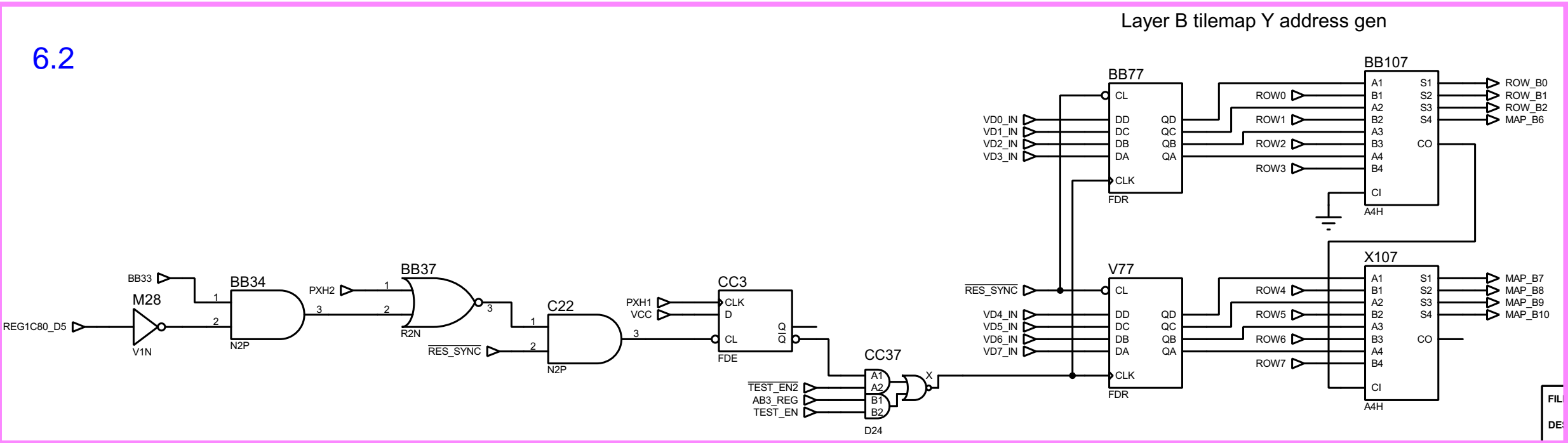
5.6 ✓



6.1



6.2



The diagram illustrates the logic for the GFX ROM bank during CPU testing. It features a 4-to-1 multiplexer (E77) that selects between four 8-bit ROM banks (DB3\_BUF, DB2\_BUF, DB1\_BUF, DB0\_BUF) based on the REG\_TE00\_WR signal. The selected data is then routed through various logic gates (AND, OR, NOT) and registers (REG1C00\_D5, REG1C00\_D6) to produce the final output signals (COL2, COL3).

**Key Components and Signals:**

- Inputs:** REG\_TE00\_WR, DB3\_BUF, DB2\_BUF, DB1\_BUF, DB0\_BUF, REG\_SYNC, REG1C00\_D5, REG1C00\_D6, REG1F00\_D0, REG1F00\_D4, REG1D80\_D0, REG1D80\_D4, REG1F00\_D1, REG1D80\_D1, REG1F00\_D2, REG1D80\_D2, REG1F00\_D3, REG1D80\_D3, REG1F00\_D6, REG1D80\_D6, REG1F00\_D7, REG1D80\_D7.
- Logic Gates:** AND gates (B3, B19, B40, B28), OR gates (C36, C29, C75, C155), NOT gates (A35, A31, C74, E149, F149, H124).
- Registers:** REG1C00\_D5, REG1C00\_D6, REG1F00\_D0, REG1F00\_D4, REG1D80\_D0, REG1D80\_D4, REG1F00\_D1, REG1D80\_D1, REG1F00\_D2, REG1D80\_D2, REG1F00\_D3, REG1D80\_D3, REG1F00\_D6, REG1D80\_D6, REG1F00\_D7, REG1D80\_D7.
- Outputs:** COL2, COL3.

## 7.2

### 7.3

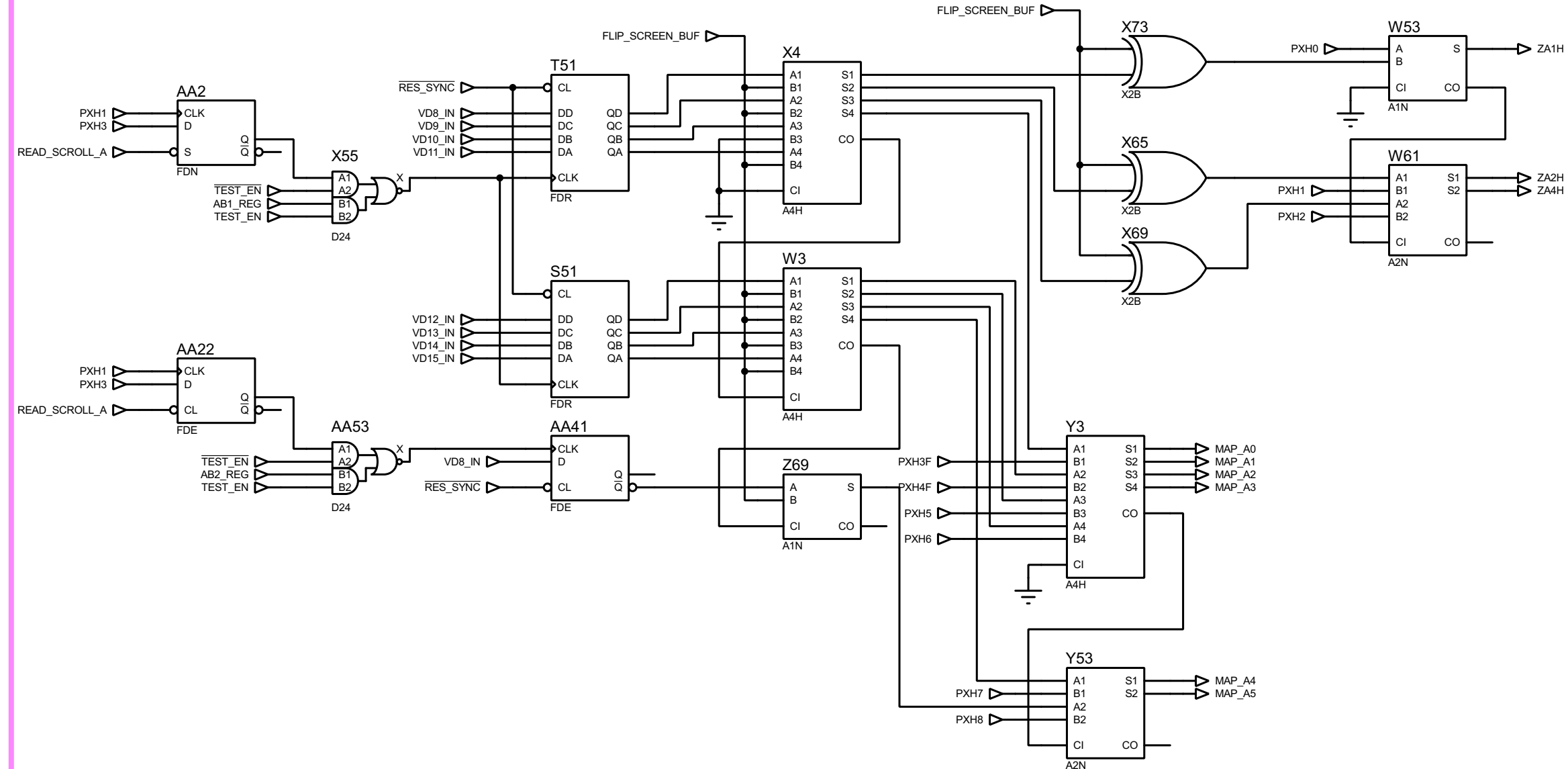
GFX ROM bank for CPU testing

## 7.4

## 7.5

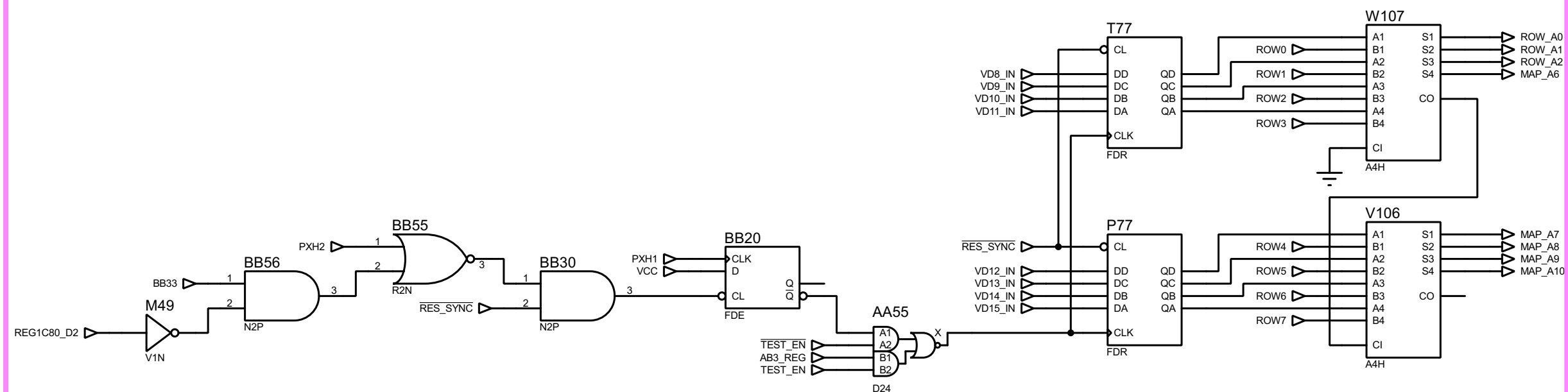
## 8.1

### Layer A tilemap X address gen



## 8.2

### Layer A tilemap Y address gen



FILE NAME: k052109.pdsprj

DESIGN TITLE: Konami 052109  
LAYER A SCROLL

BY: Sean Gonsalves

REV: A

DATE: 22/06/2021

PAGE: 8 of 8