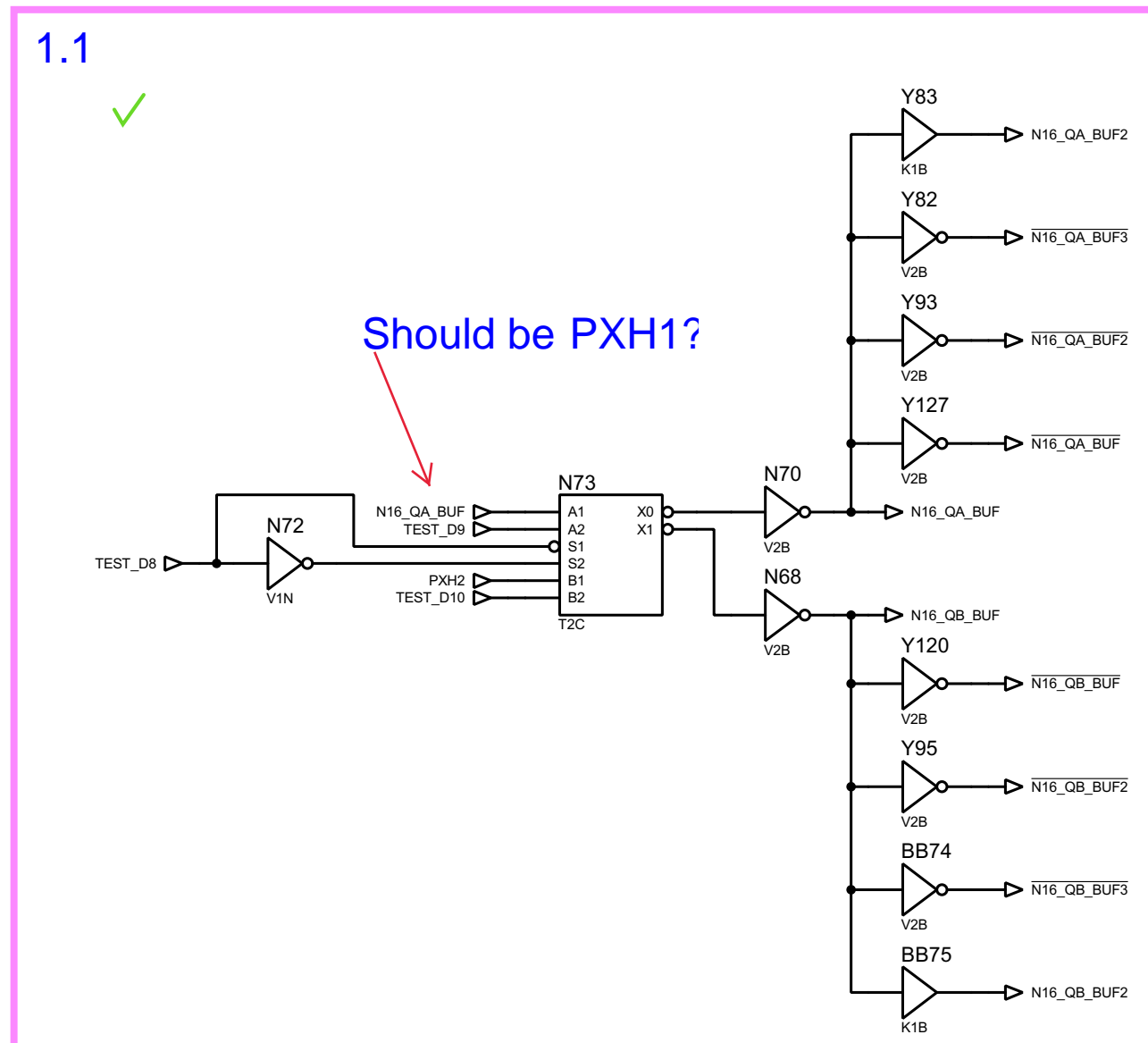


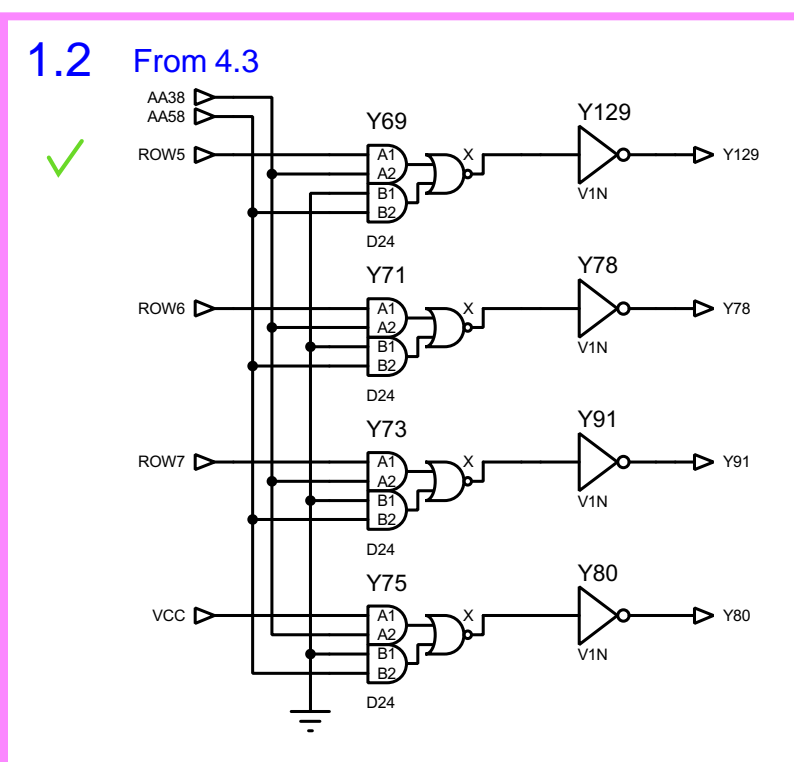
```

VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 01xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 110x xxxx xxxx A y scroll
0000 110x xxxx xxxx B y scroll
0000 01xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 110x xxxx xxxx B y scroll
0001 110x xxxx xxxx B x scroll
0001 1101 x xxxx x Tilemaps X
          xxx x Tilemaps Y

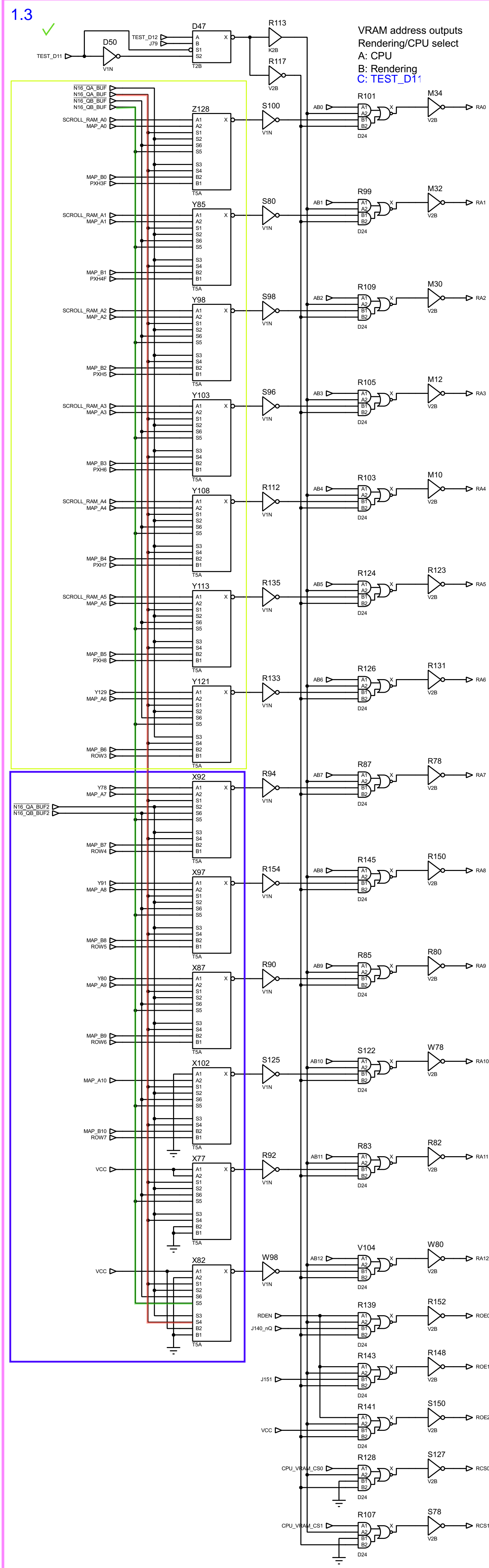
```

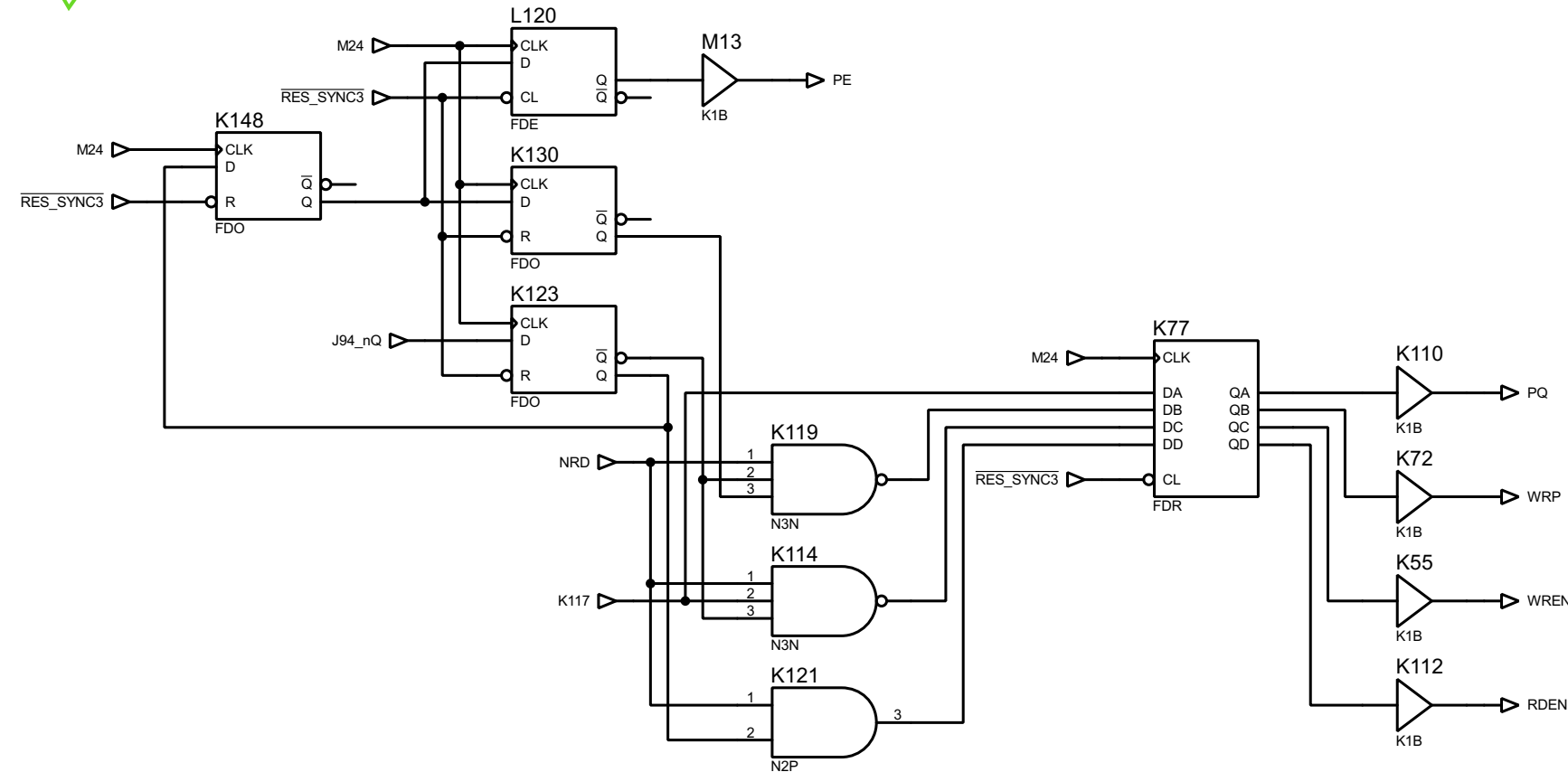
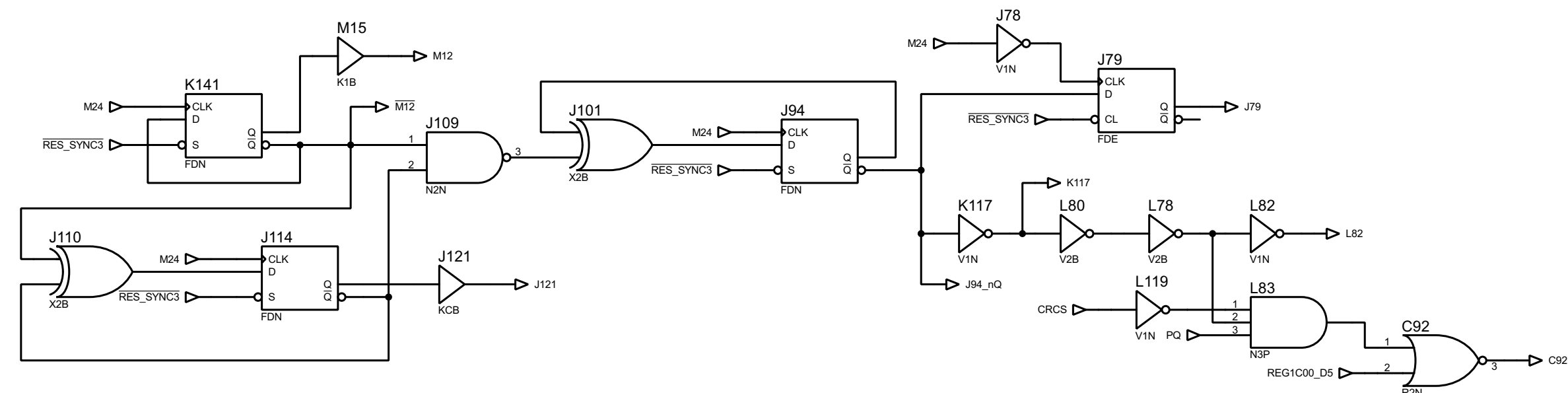


### TEST\_D13 Addresses Selector



Selection can be simplified using AA38 (and AA38n) only, AA58 always selects 1'b0.

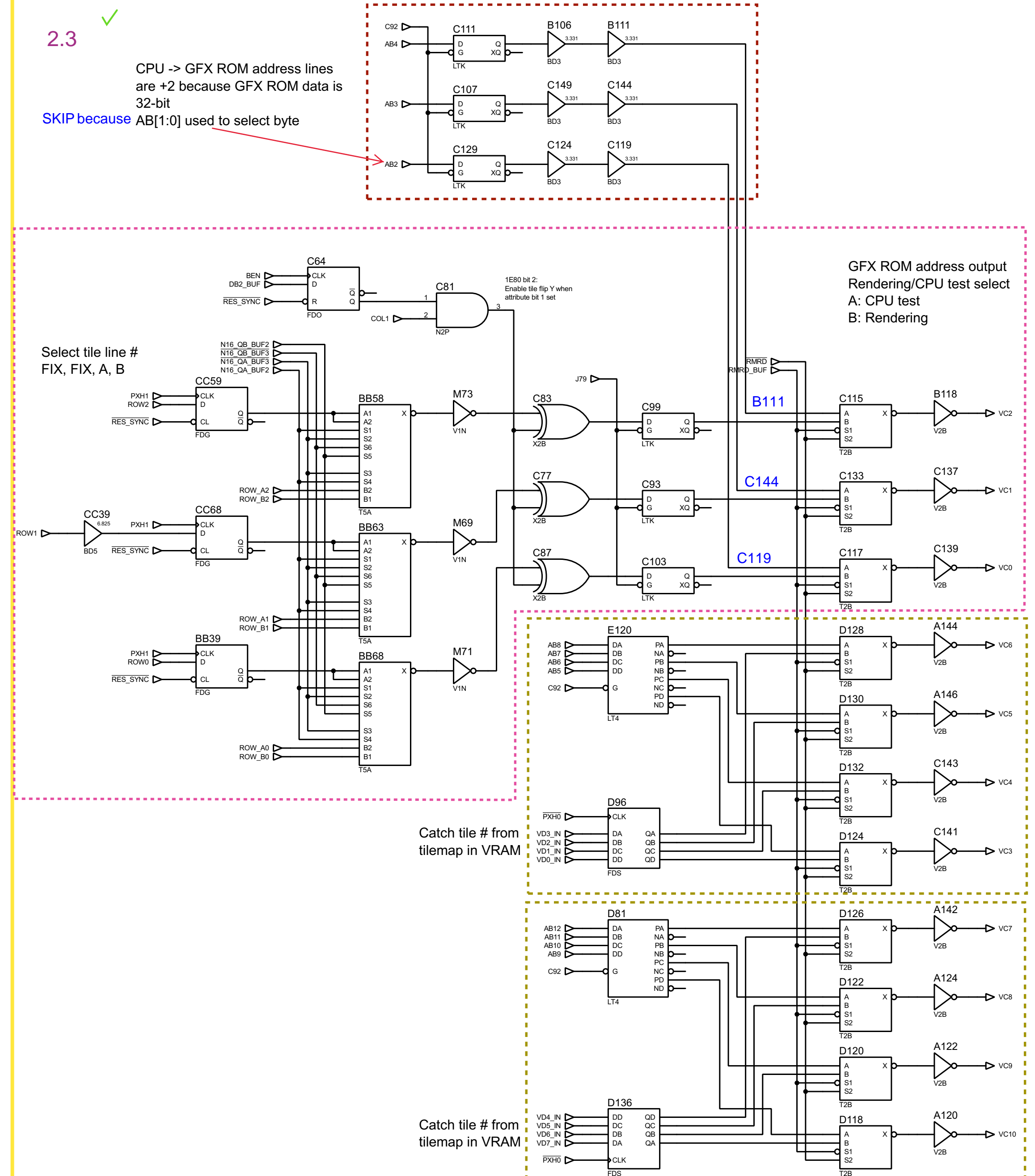




FILE NAME: <b>k052109.pdsprj</b>	DATE: <b>22/06/2021</b>
DESIGN TITLE: <b>Konami 052109 GFX ROM ADDRESS</b>	PAGE: <b>2 of 8</b>
BY: Sean Gonsalves	REV: A

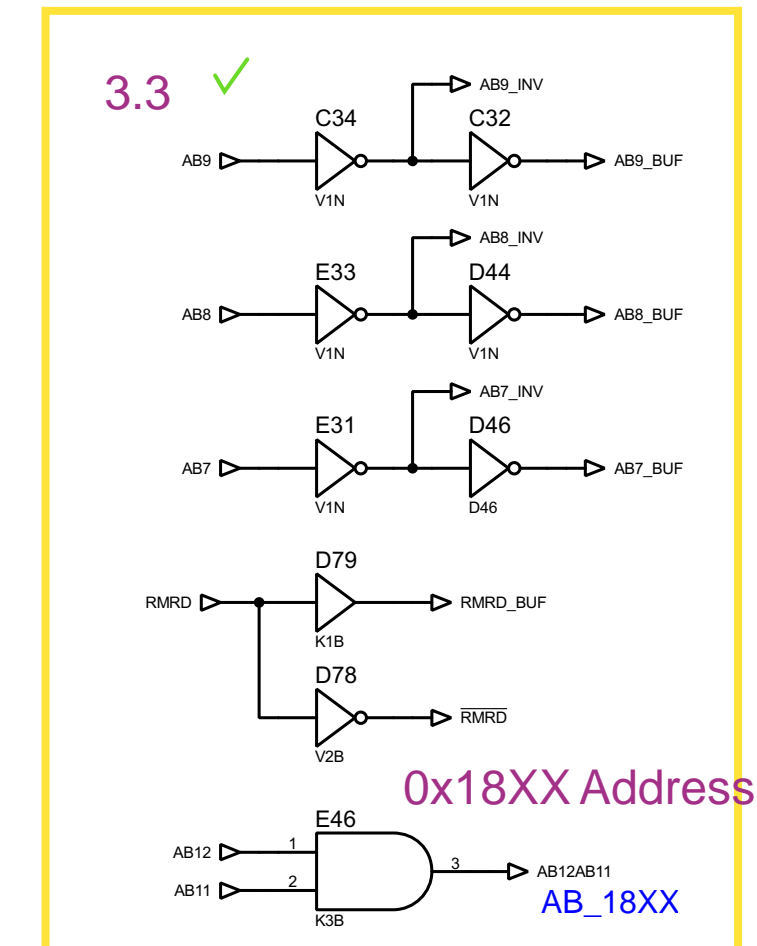
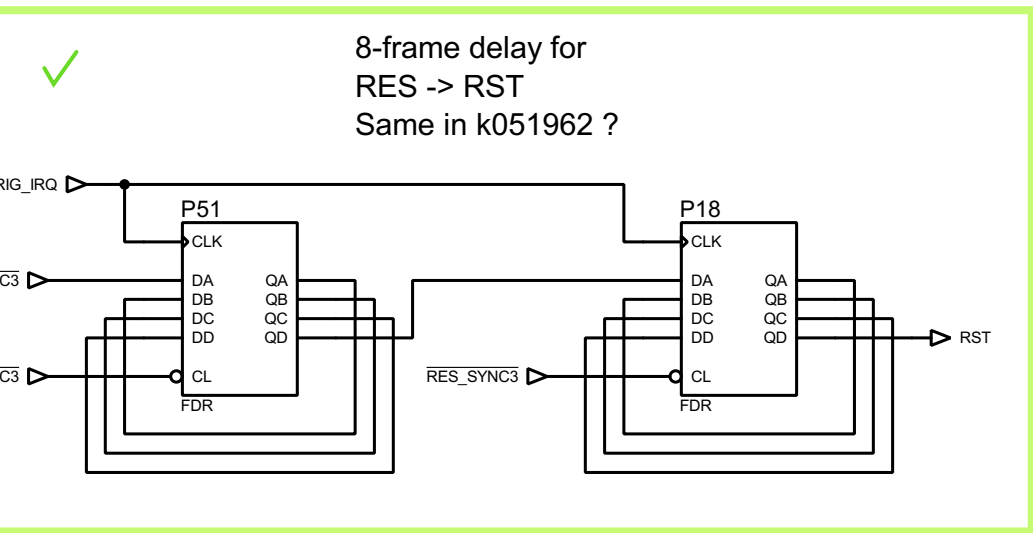


SKIP because AB[1:0] used to select byte



### 3.1 ✓

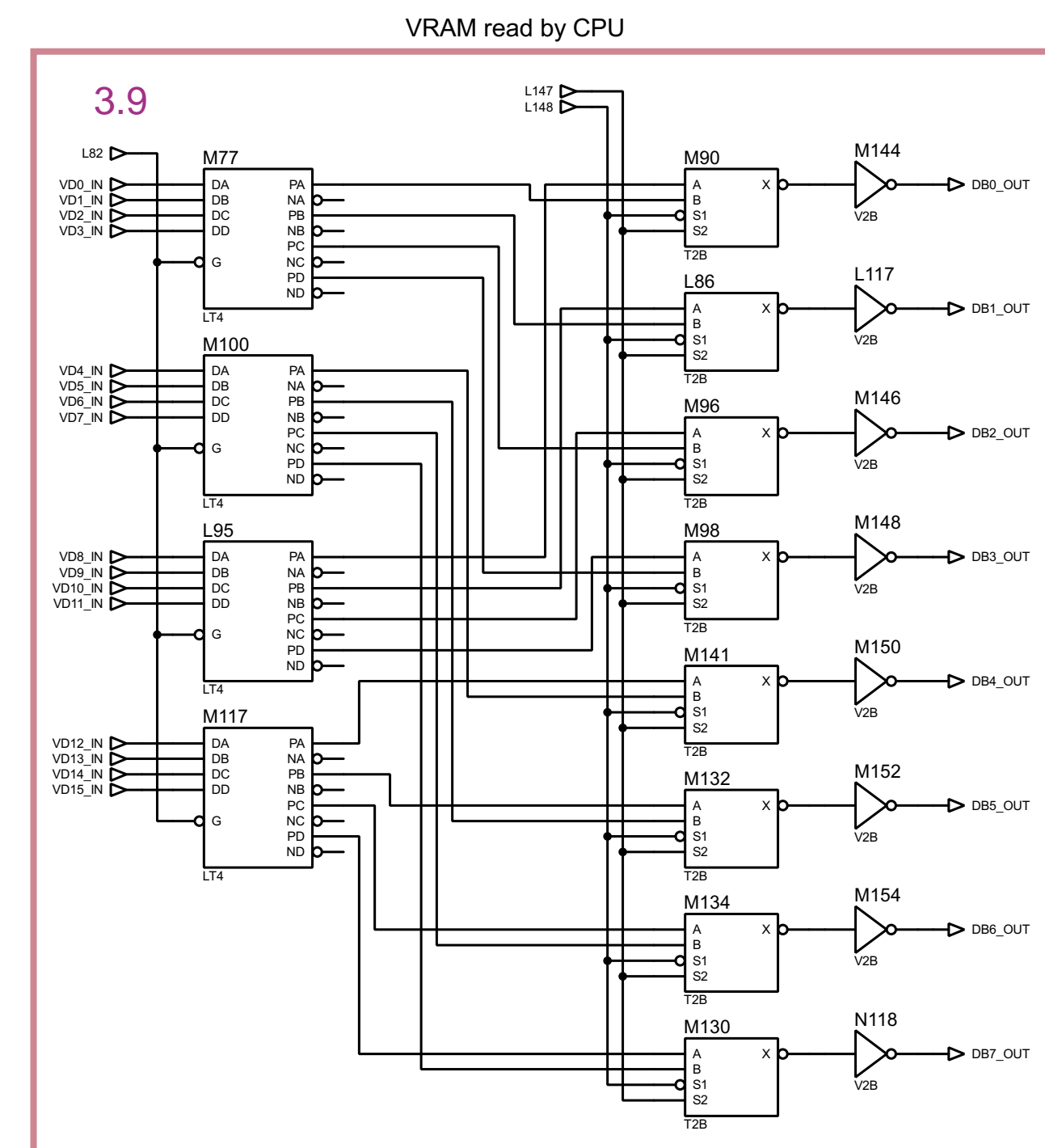
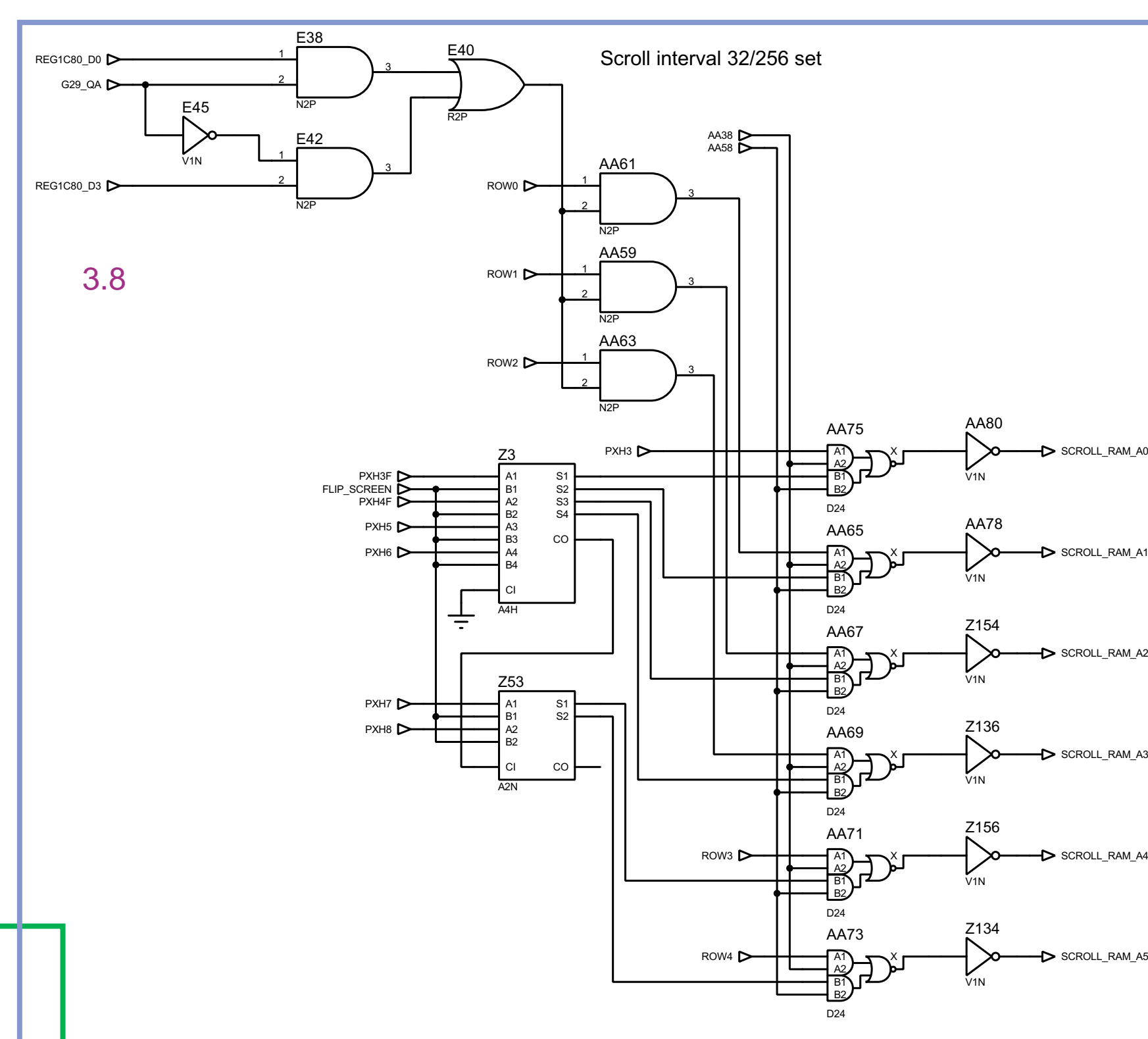
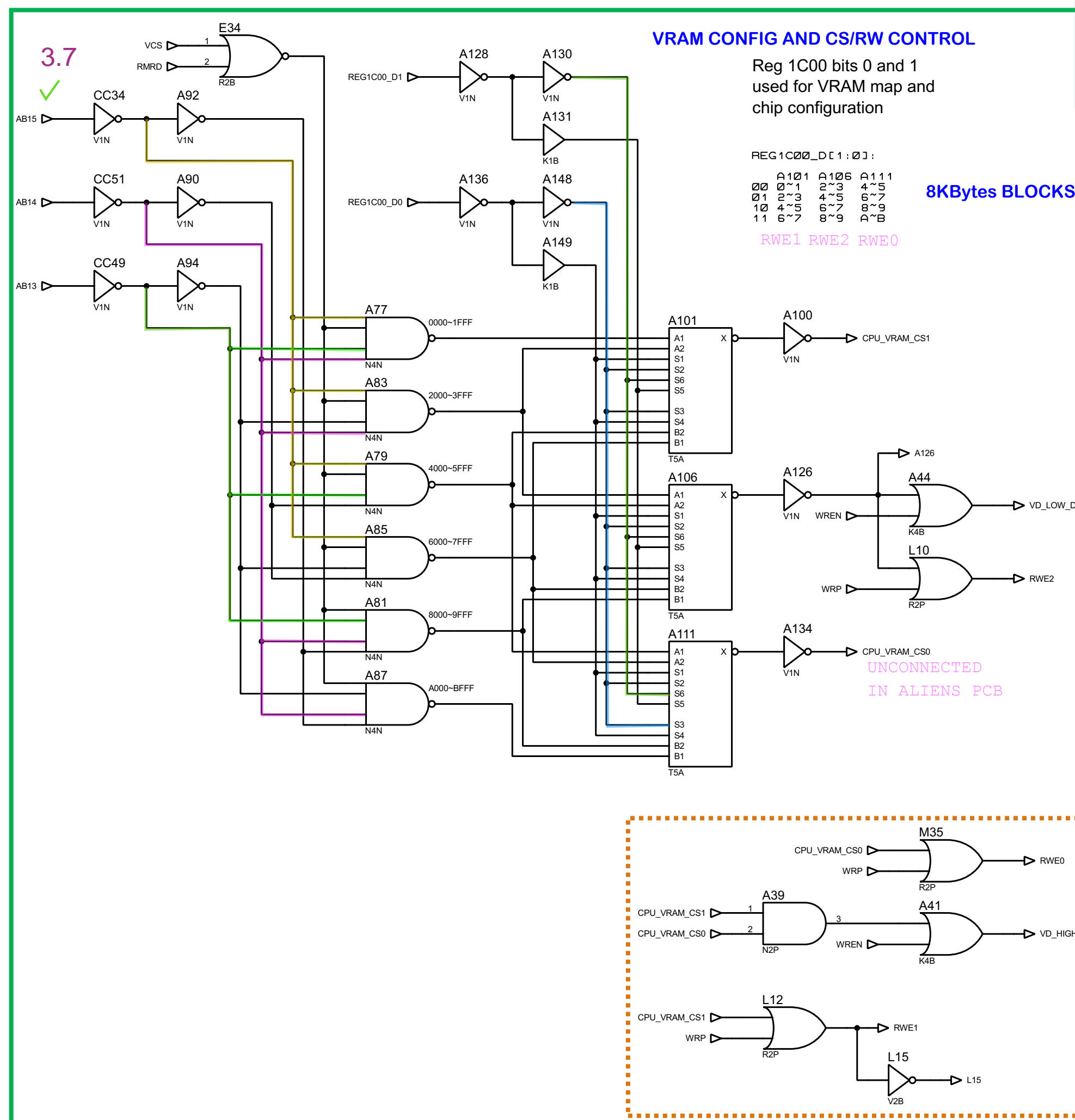
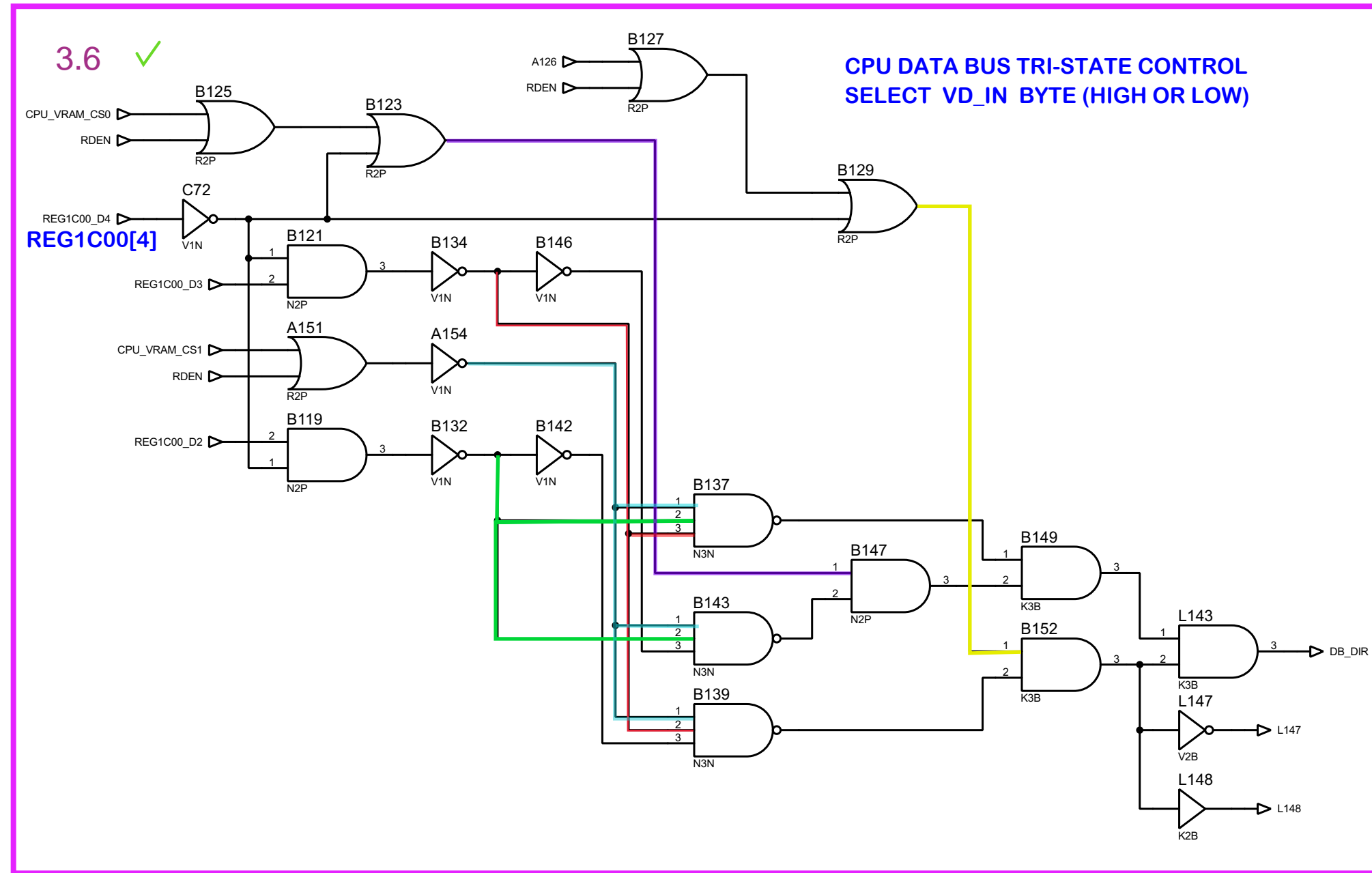
The diagram shows a circuit for a 3-bit counter. It starts with an N122 flip-flop. The flip-flop has four inputs: M04 (CLK), V02 (D), RES (CL), and FDE. The output Q is connected to the M74 multiplexer's input 0. The M74 multiplexer has two inputs (0 and 1) and one output. The output of the M74 is connected to the H12 comparator's input 0. The H12 comparator has two inputs (0 and 1) and one output. The output of the H12 is connected to the H1B comparator's input 0. The H1B comparator has two inputs (0 and 1) and one output. The output of the H1B is connected to the RES\_SYNC2 signal. The output of the H12 is connected to the RES\_SYNC signal. The output of the M74 is also connected to the RES\_SYNC3 signal.



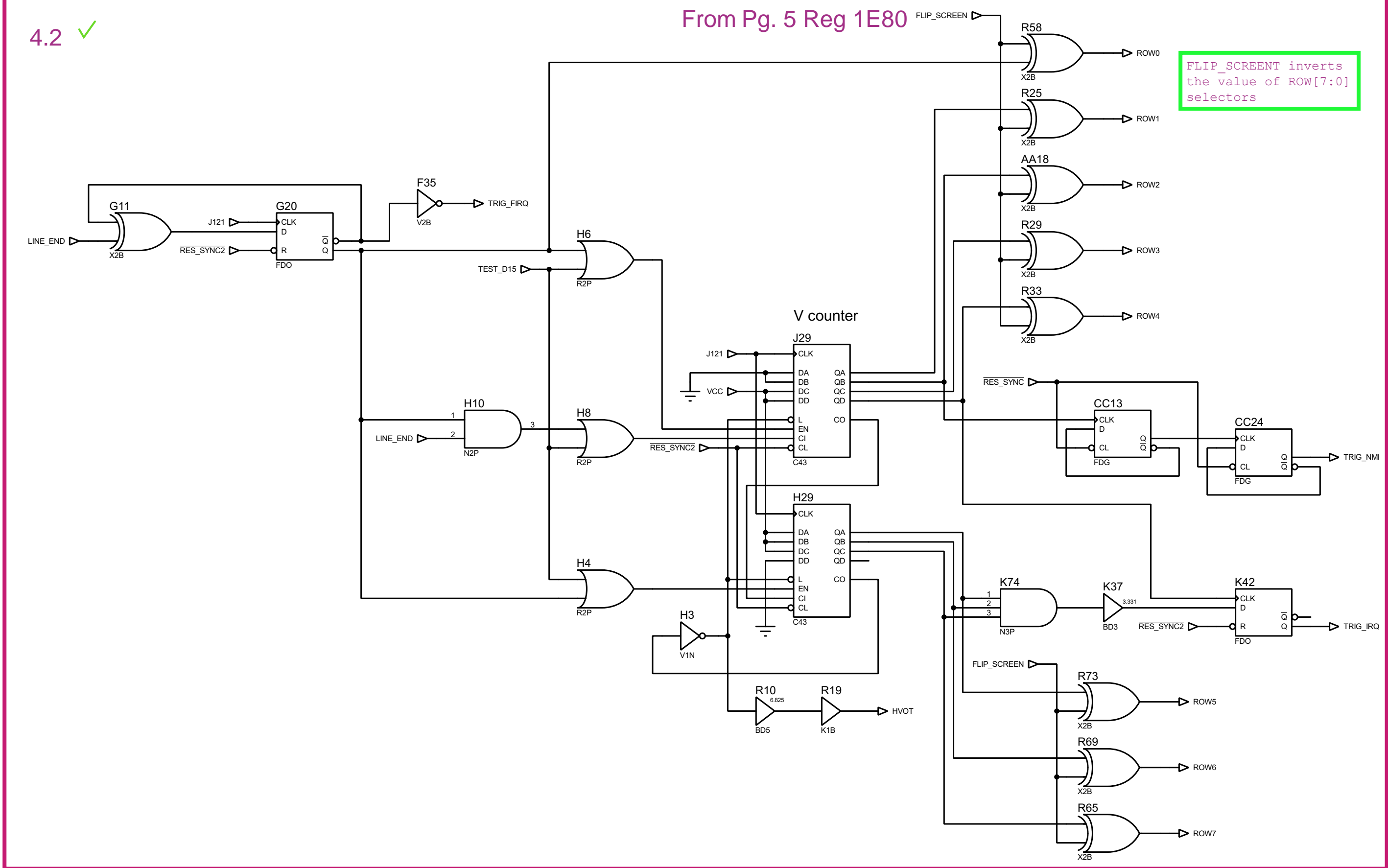
### 3.4 ✓

The diagram illustrates a 10-bit bus system. It consists of 10 buffers (N135, N80, N132, N77, N83, N97, N100, N103) and 10 inverters (K2B). Each input signal (DB0\_IN to DB7\_IN) is connected to a buffer and an inverter. The buffer output is connected to the inverter input, and the inverter output is connected to the buffer input, forming a loop. The output of each buffer is labeled DBx\_BUF.

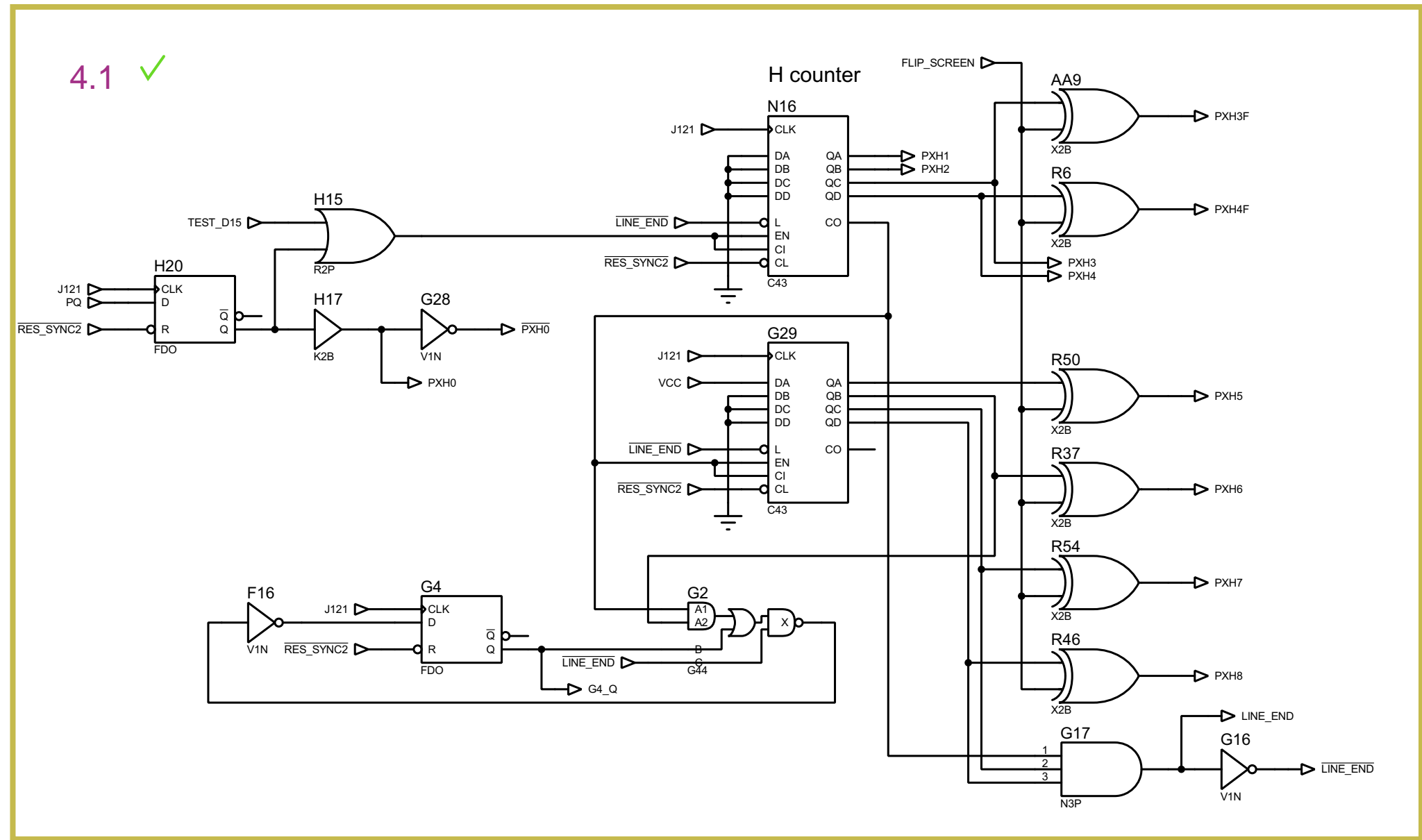
```
wire [7:0] DB_BUF
```



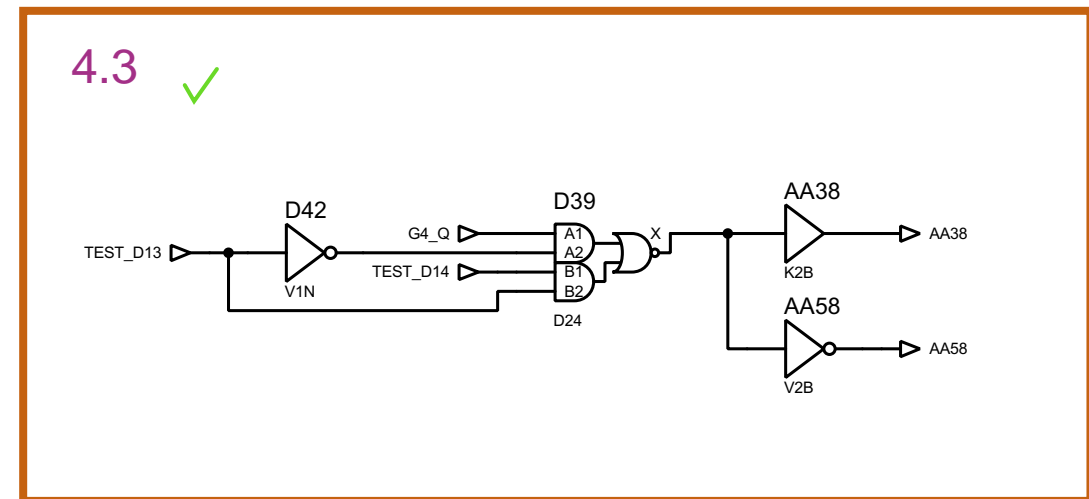
4.2 ✓



4.1 ✓

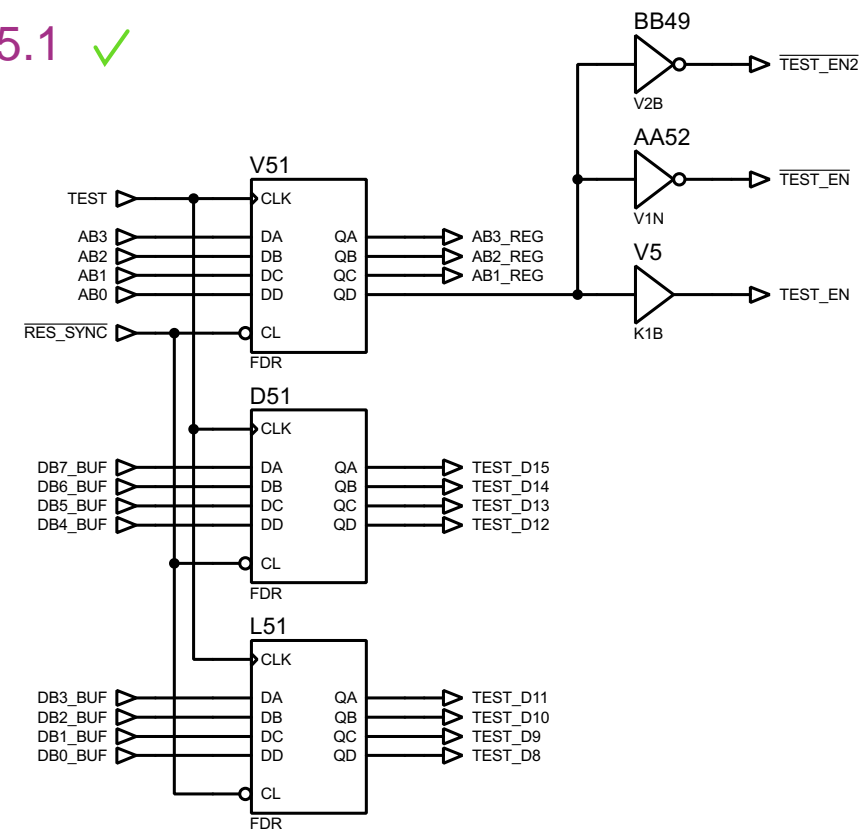


4.3 ✓

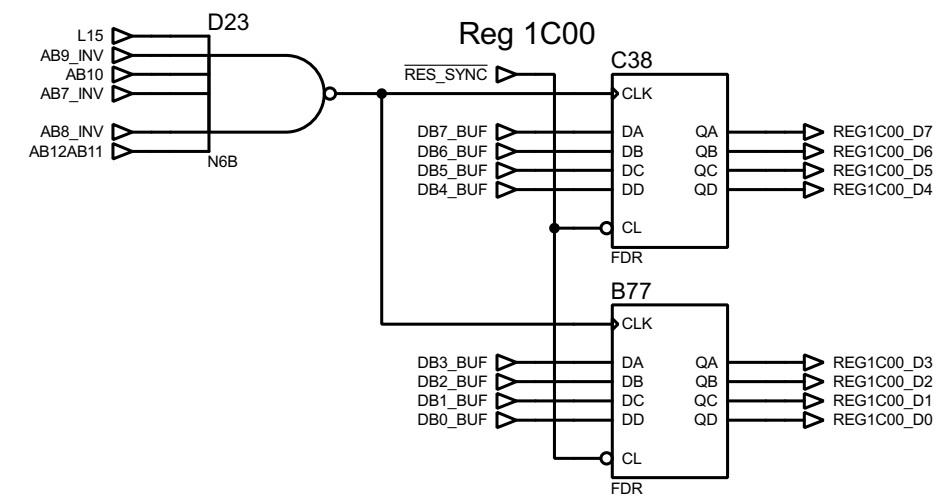




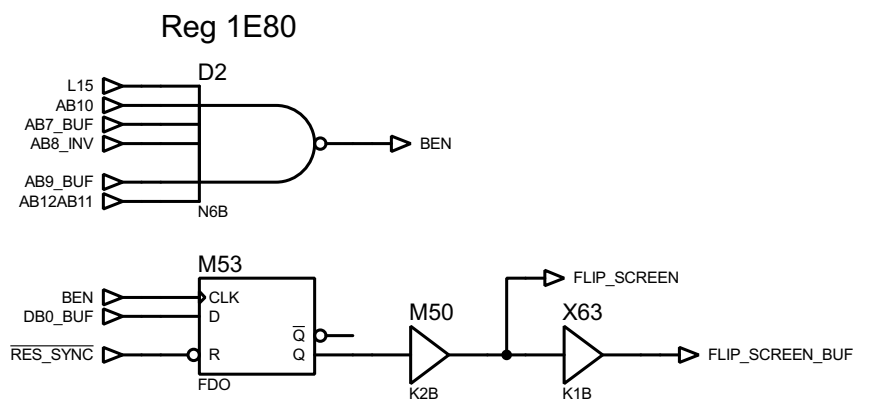
5.1 ✓



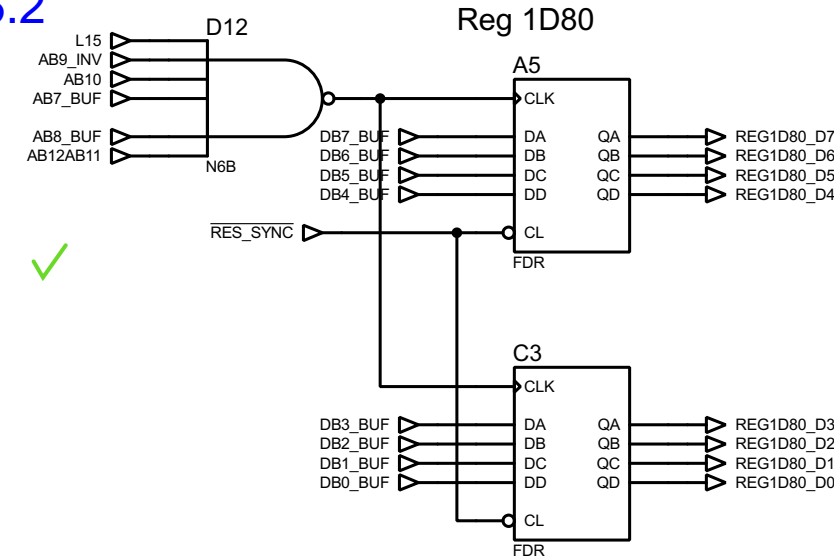
5.4 ✓



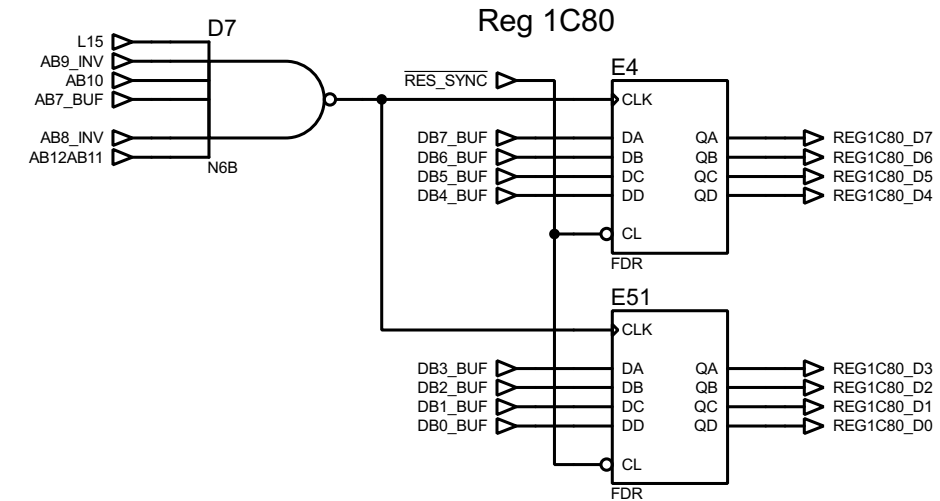
5.7 ✓



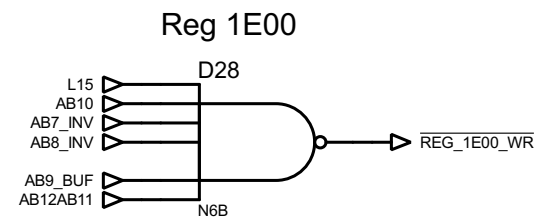
5.2 ✓



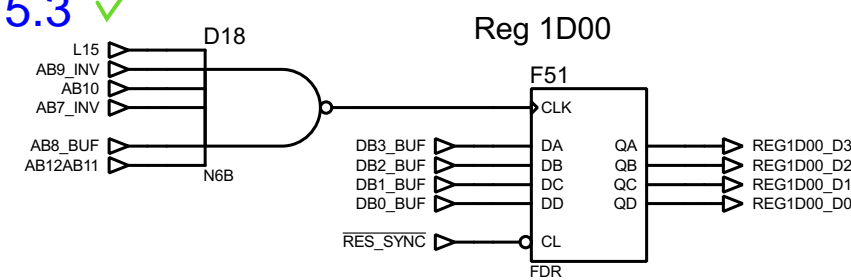
5.5 ✓



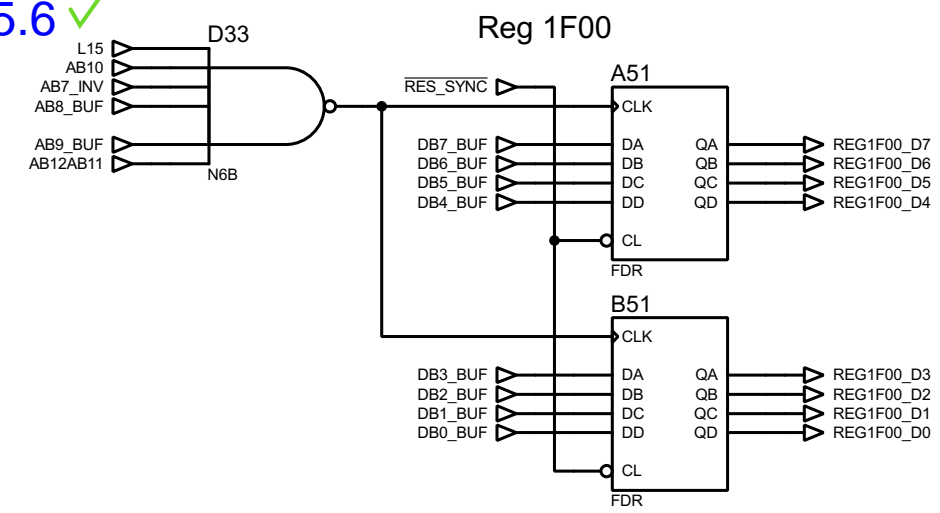
5.8 ✓



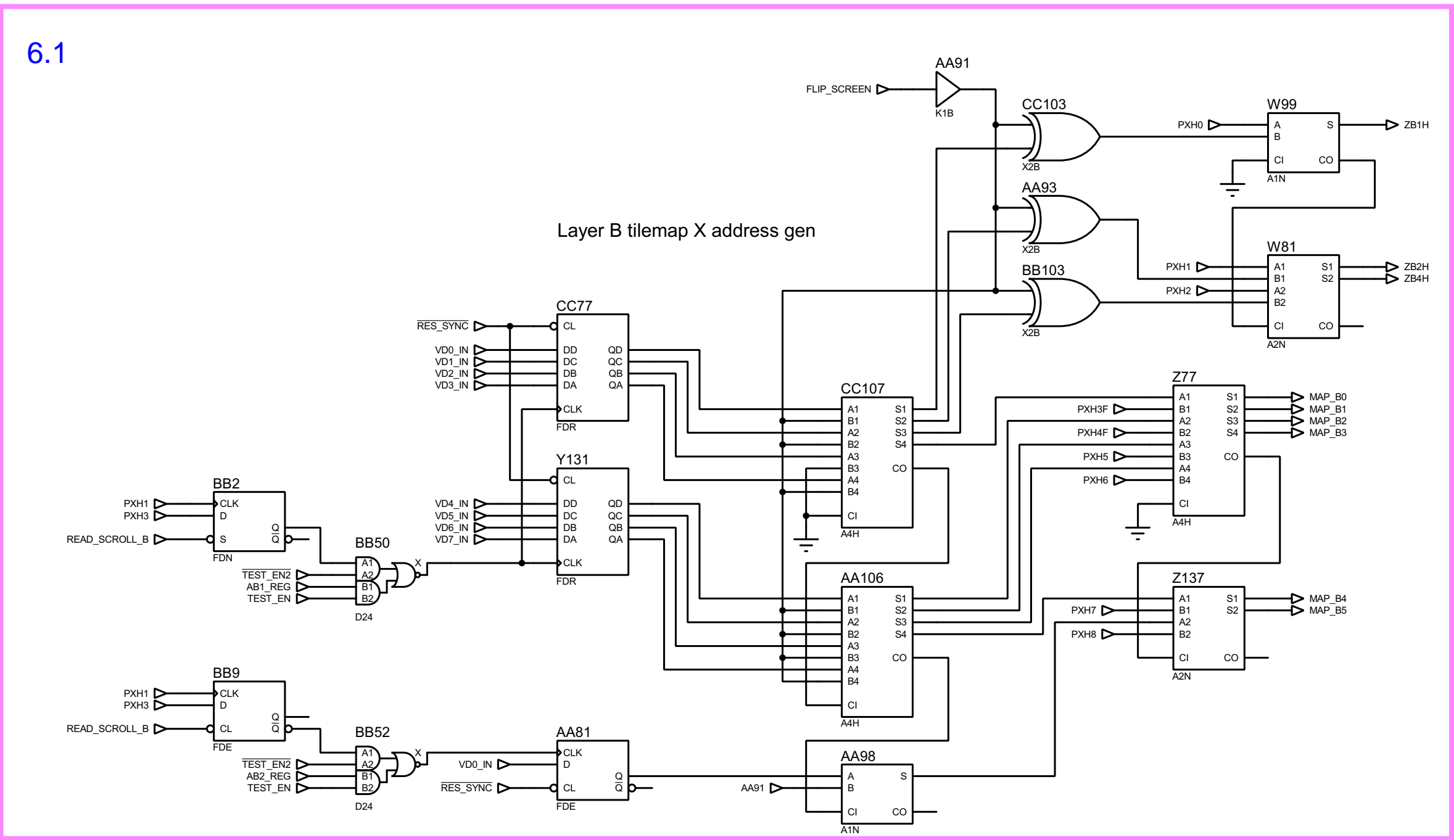
5.3 ✓



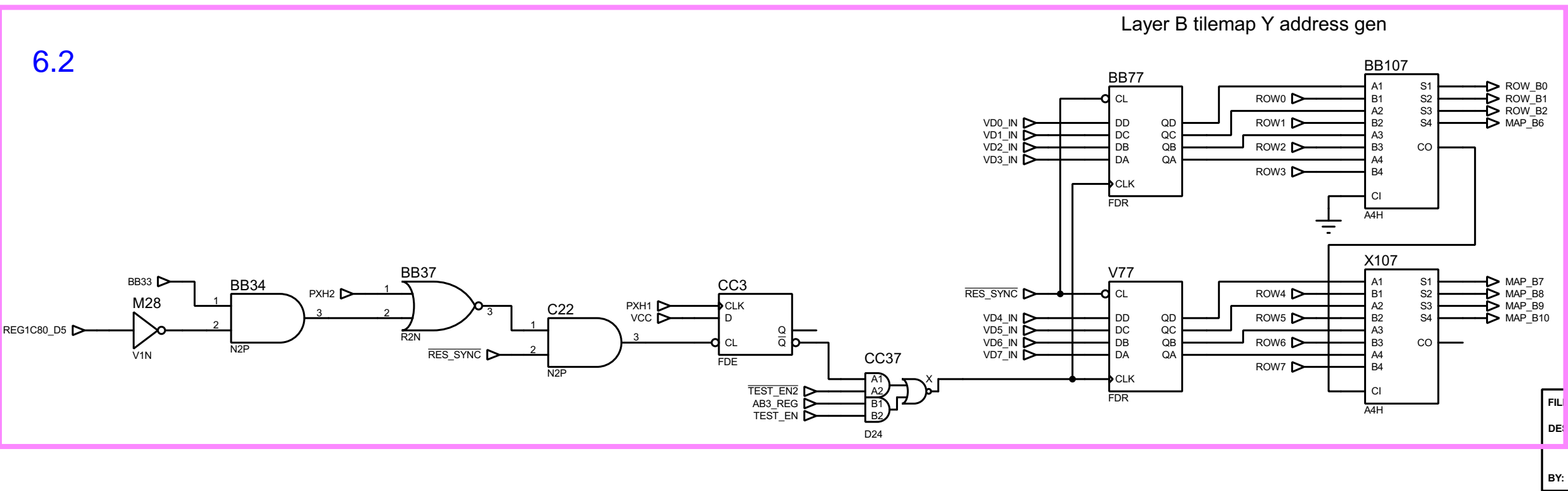
5.6 ✓



6.1



6.2



The diagram illustrates the internal logic of the GFX ROM bank for CPU testing. It features a 4-to-1 multiplexer (E77) that selects between four 8-bit ROM banks (DB3\_BUF, DB2\_BUF, DB1\_BUF, DB0\_BUF) based on the REG1E00\_WR signal. The selected data is then routed through various logic gates (AND, OR, NOT) and registers (REG1C00\_D5, REG1C00\_D6) to produce the final output signals (COL2, COL3). The diagram also shows the internal structure of the ROM banks, which are organized into four groups of four 8-bit words each, labeled REG1D80\_D0 through REG1F00\_D7.

## 7.2

### 7.3

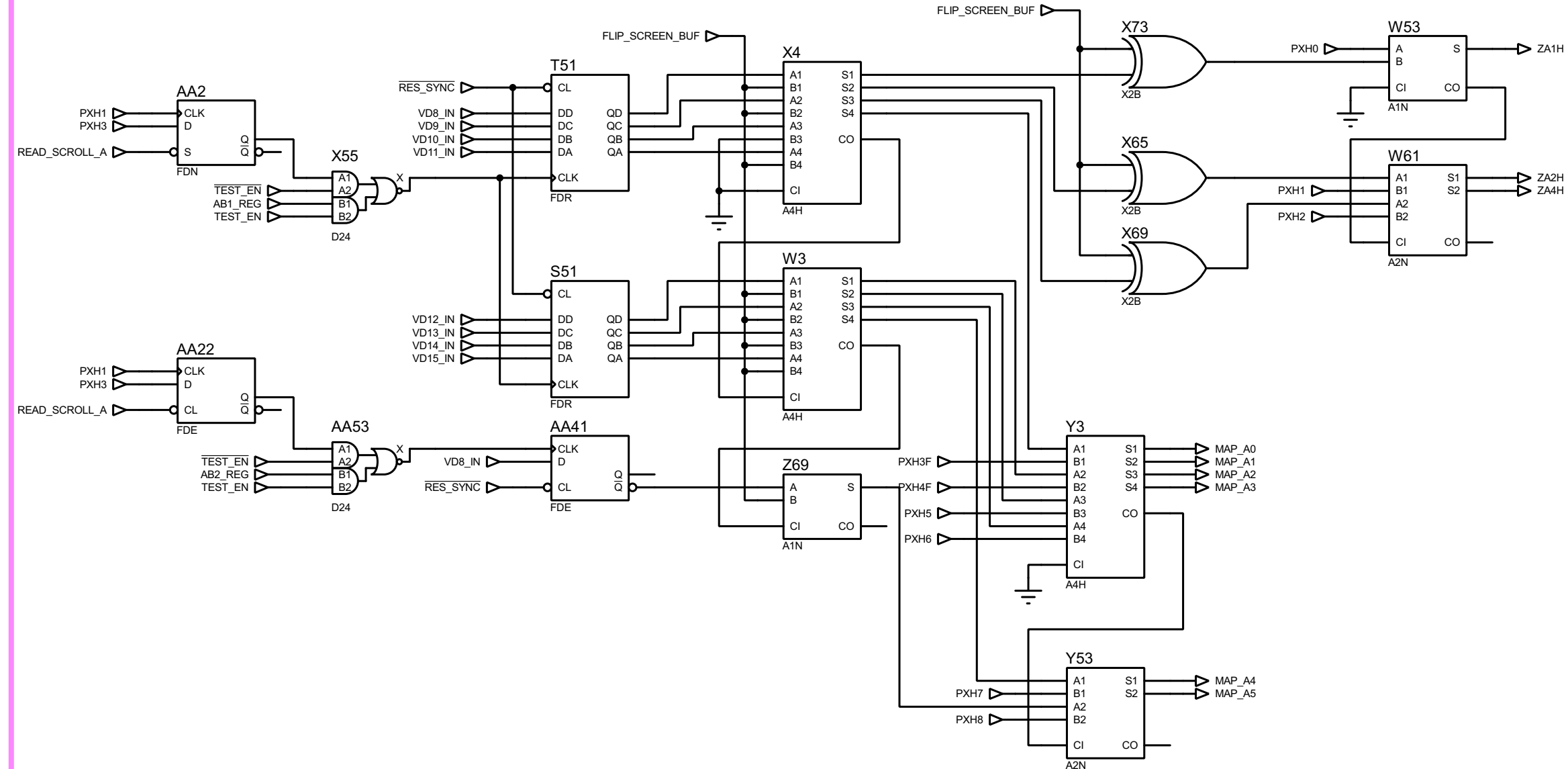
GFX ROM bank for CPU testing

## 7.4

## 7.5

## 8.1

### Layer A tilemap X address gen



## 8.2

### Layer A tilemap Y address gen

