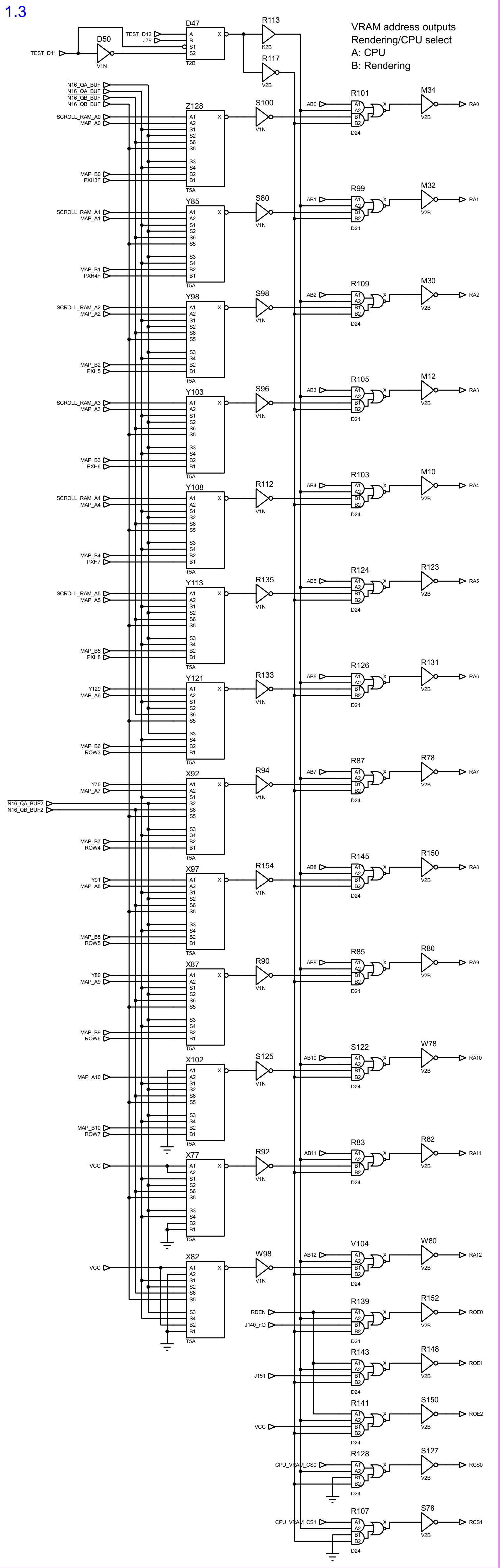
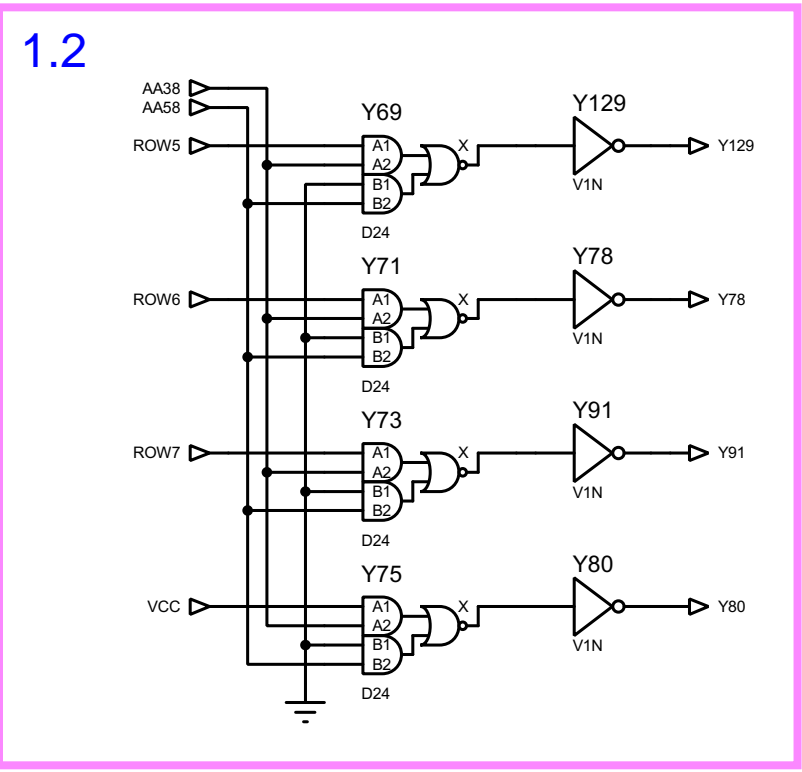
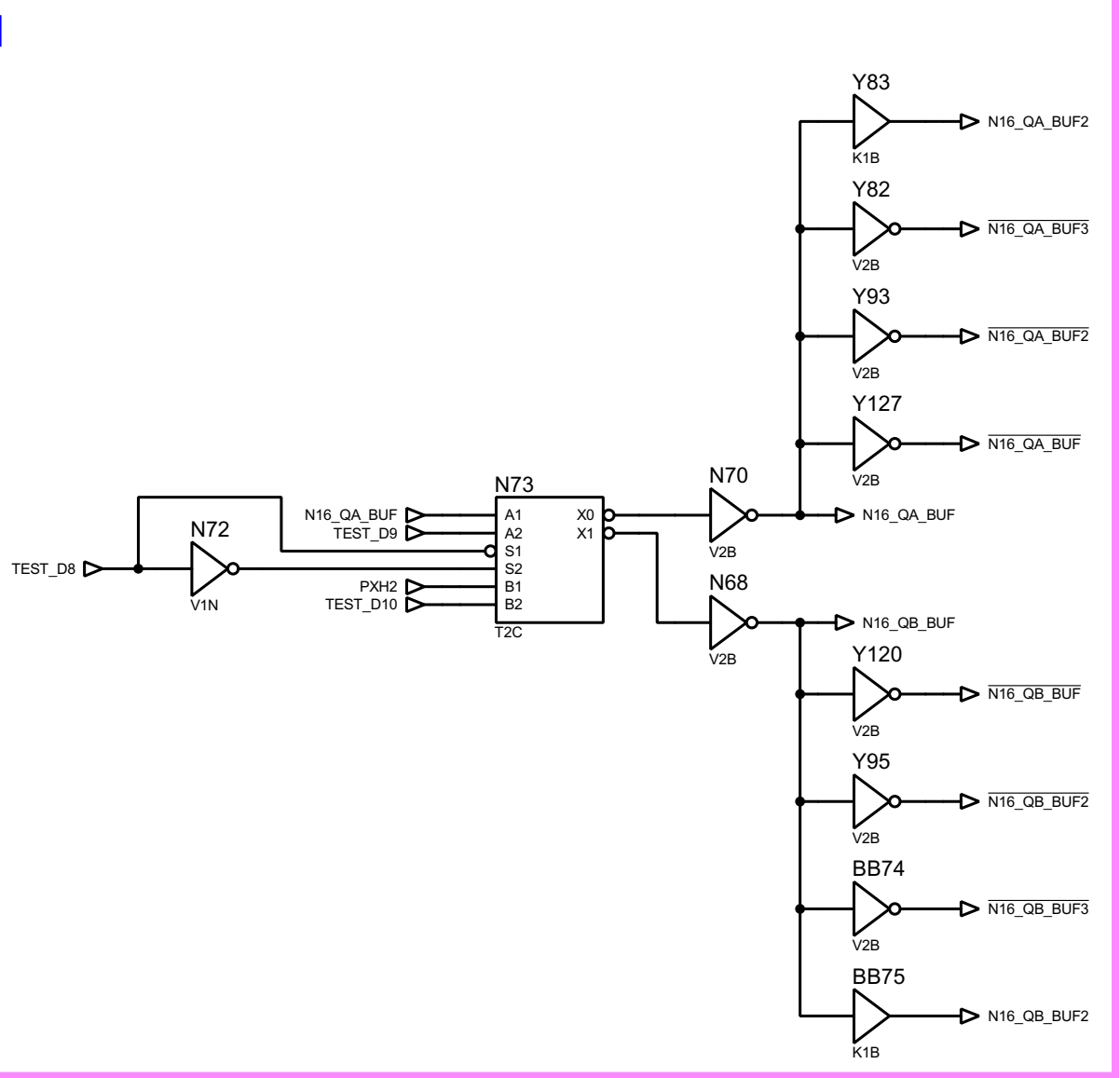
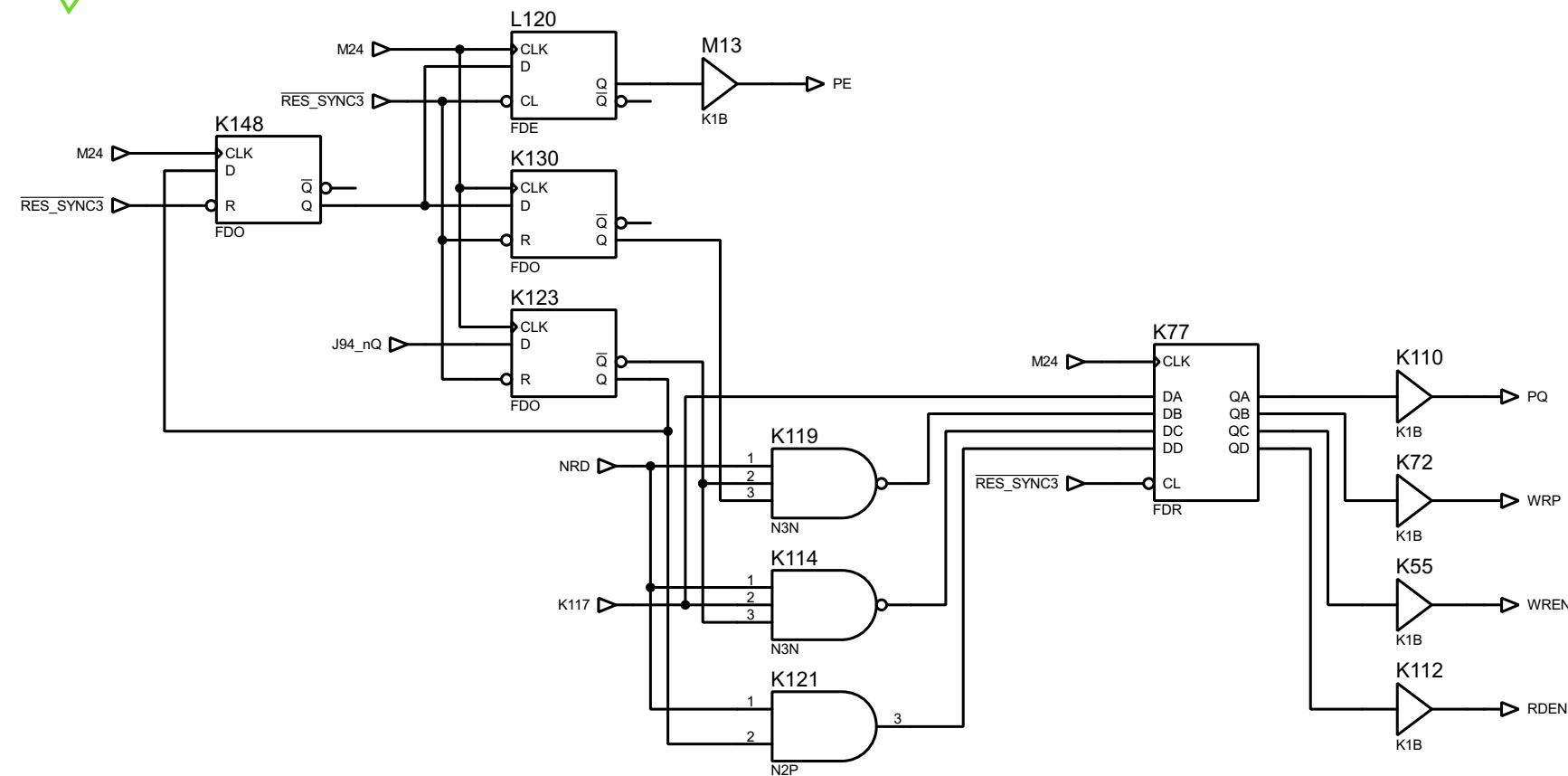
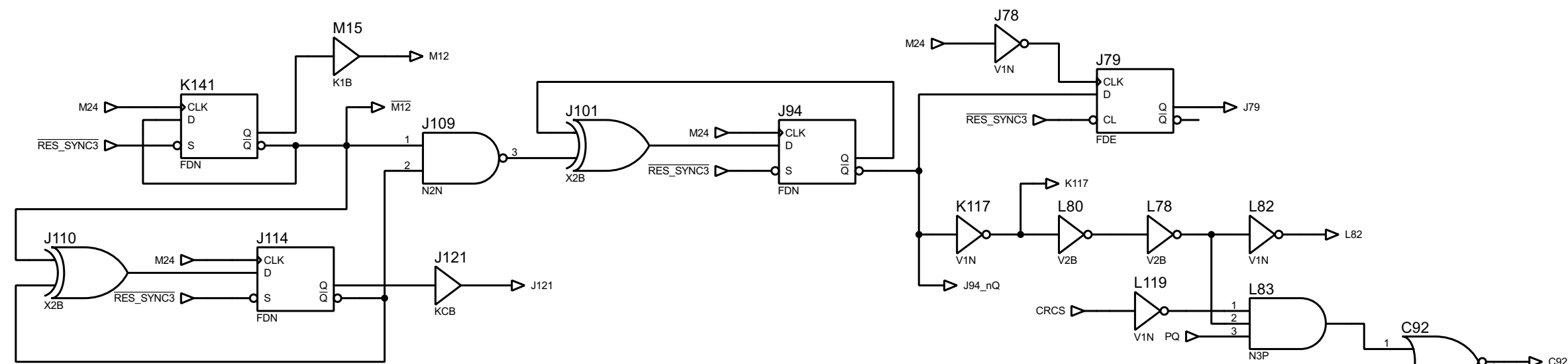


```

VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 00xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 1100 xxxx xxxx A Y scroll
0000 1101 xxxx xxxx B X scroll
0001 00xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 1100 xxxx xxxx B Y scroll
0001 1101 xxxx xxxx B X scroll
          x xxxx x Tilemaps X
xx xxxx Tilemaps Y

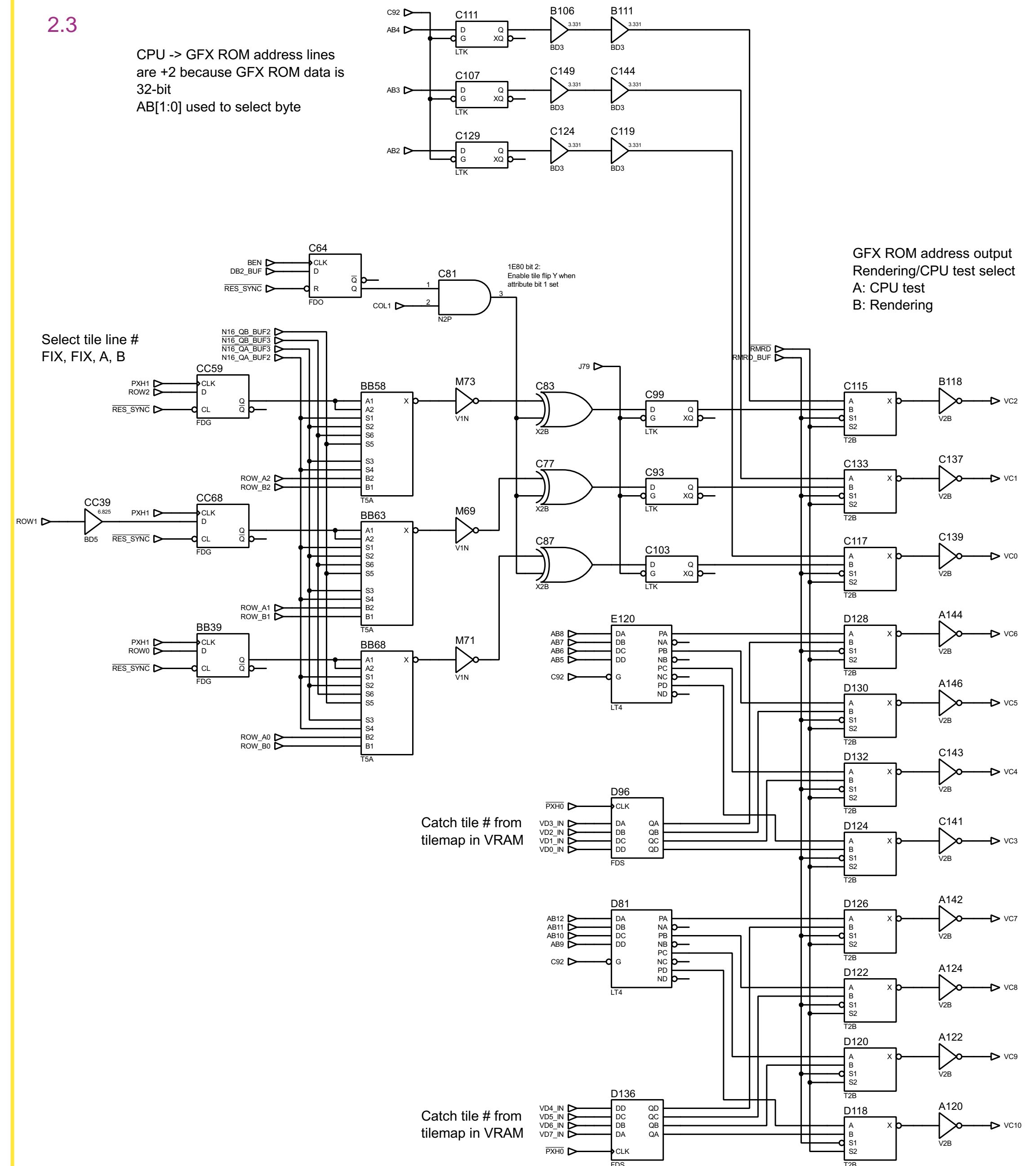
```





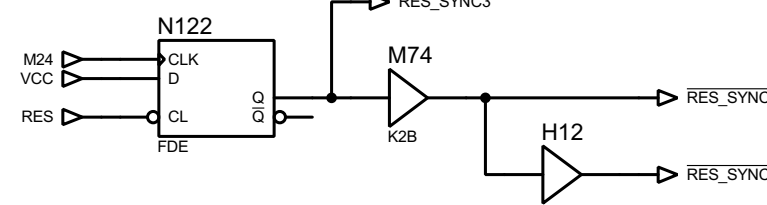
TIMING SIGNALS

CPU -> GFX ROM address lines
are +2 because GFX ROM data is
32-bit
AB[1:0] used to select byte



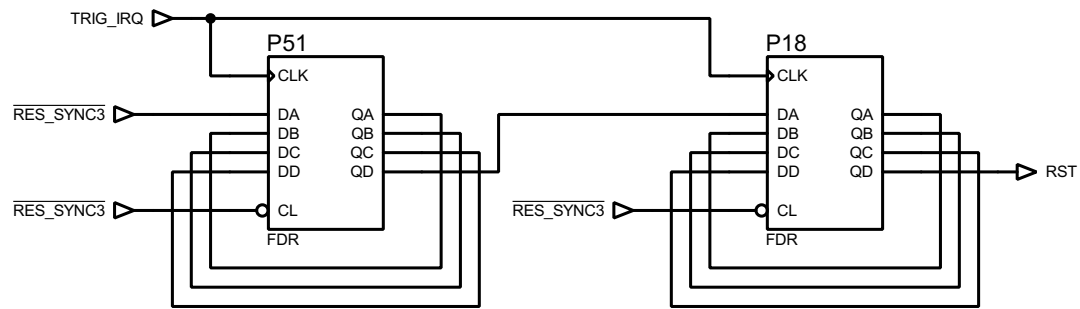
RES_SYNC signals generator

3.1 ✓

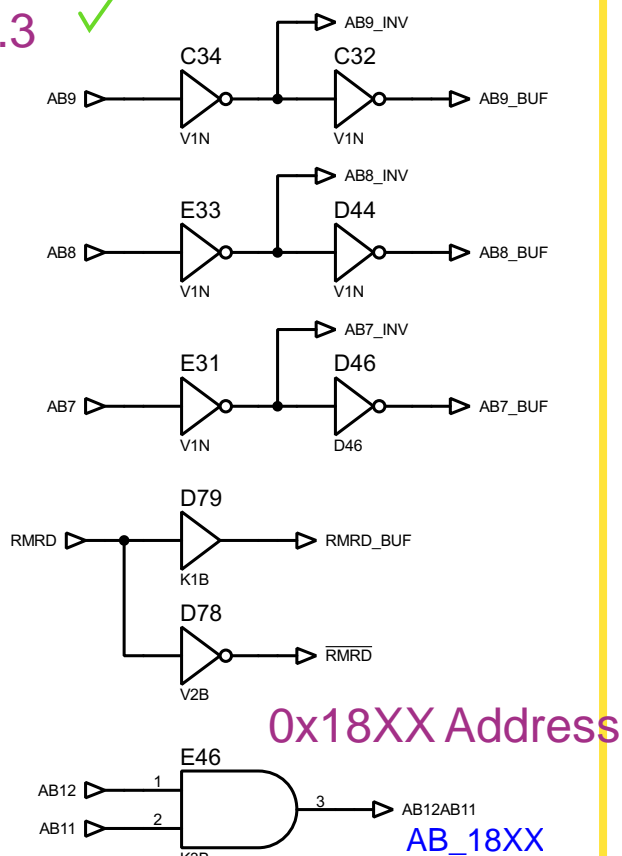


3.2 ✓

8-frame delay for
RES -> RST
Same in k051962 ?

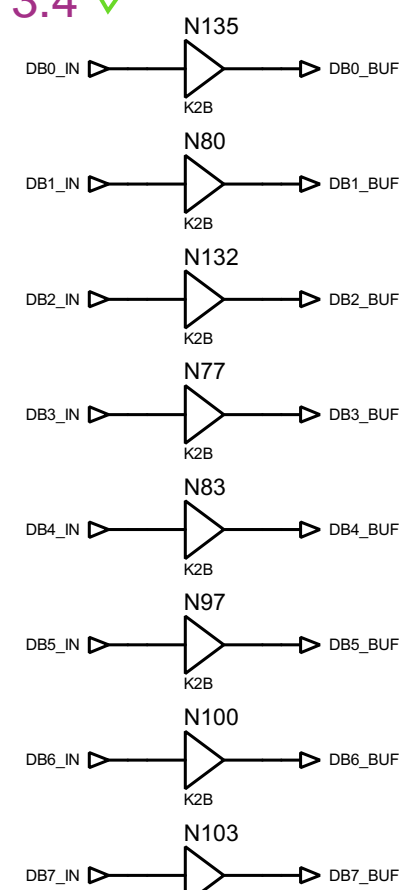


3.3 ✓



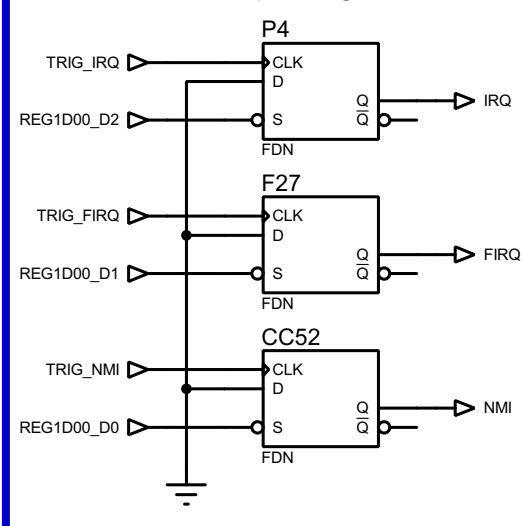
180c-1833: Layer A Y Scroll

3.4 ✓

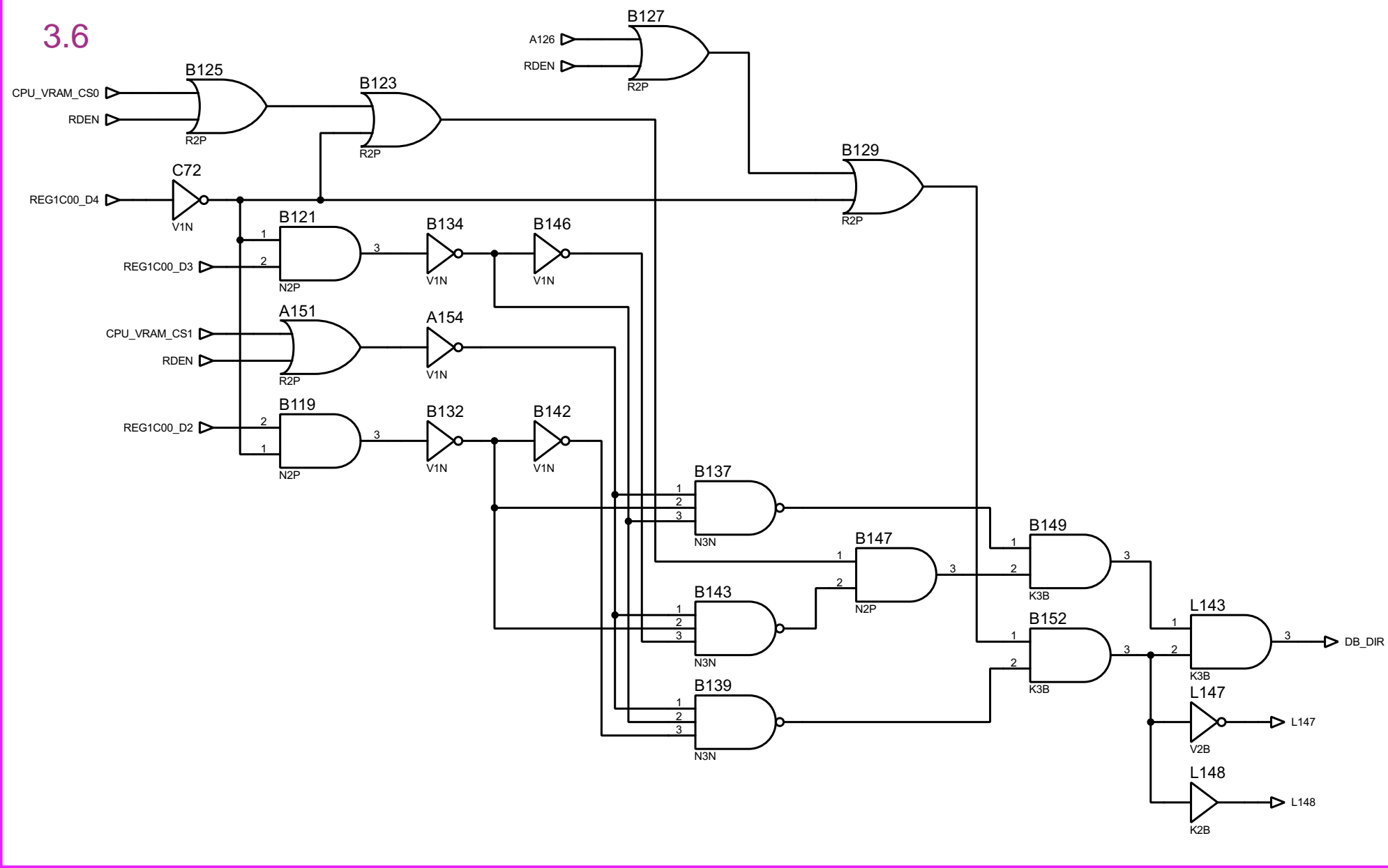


3.5 ✓

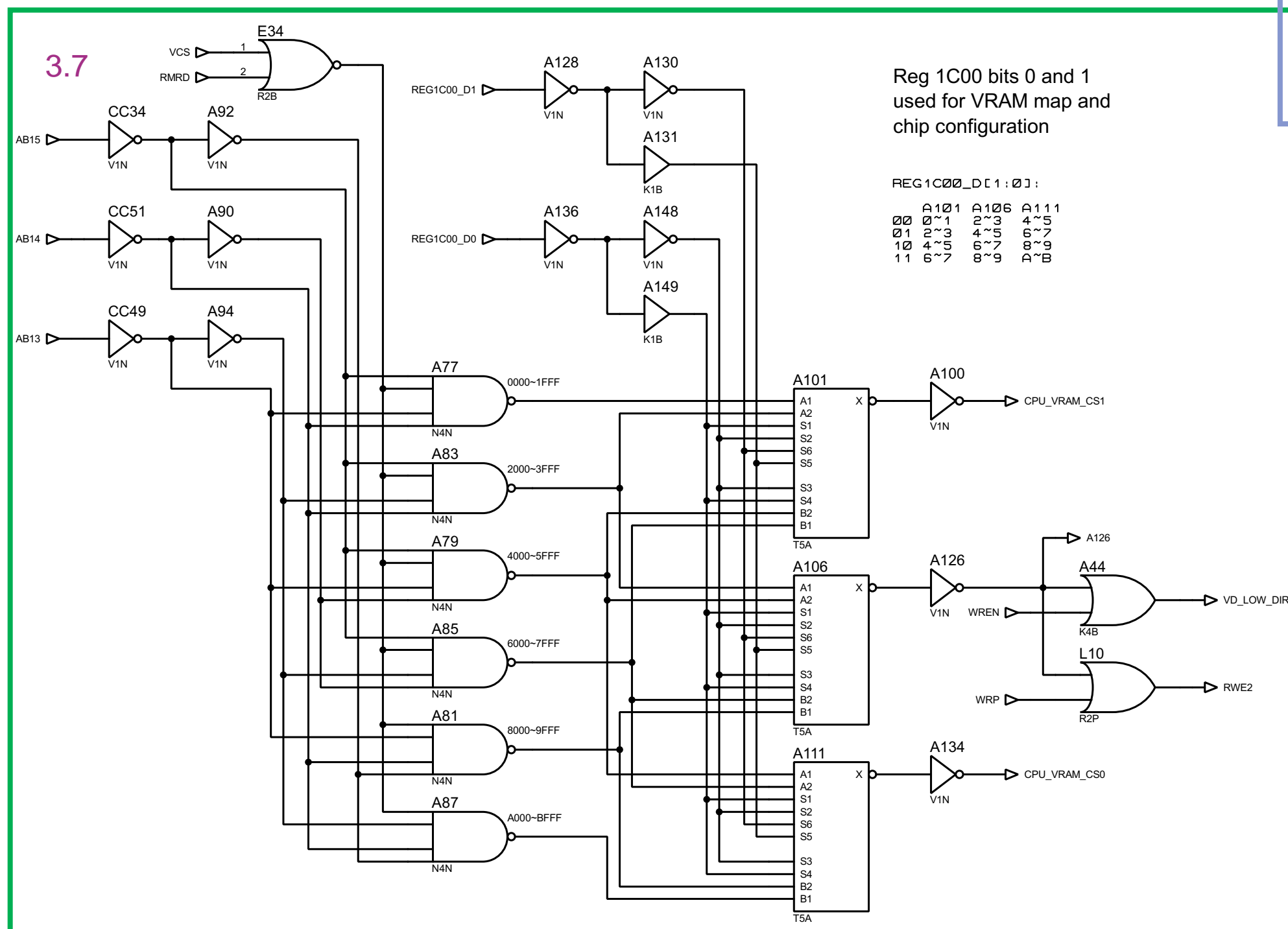
Interrupts flags



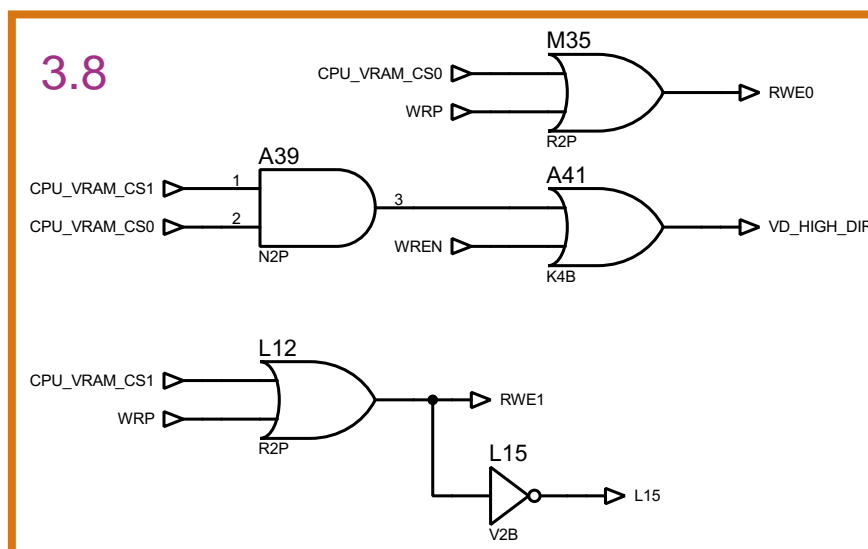
3.6



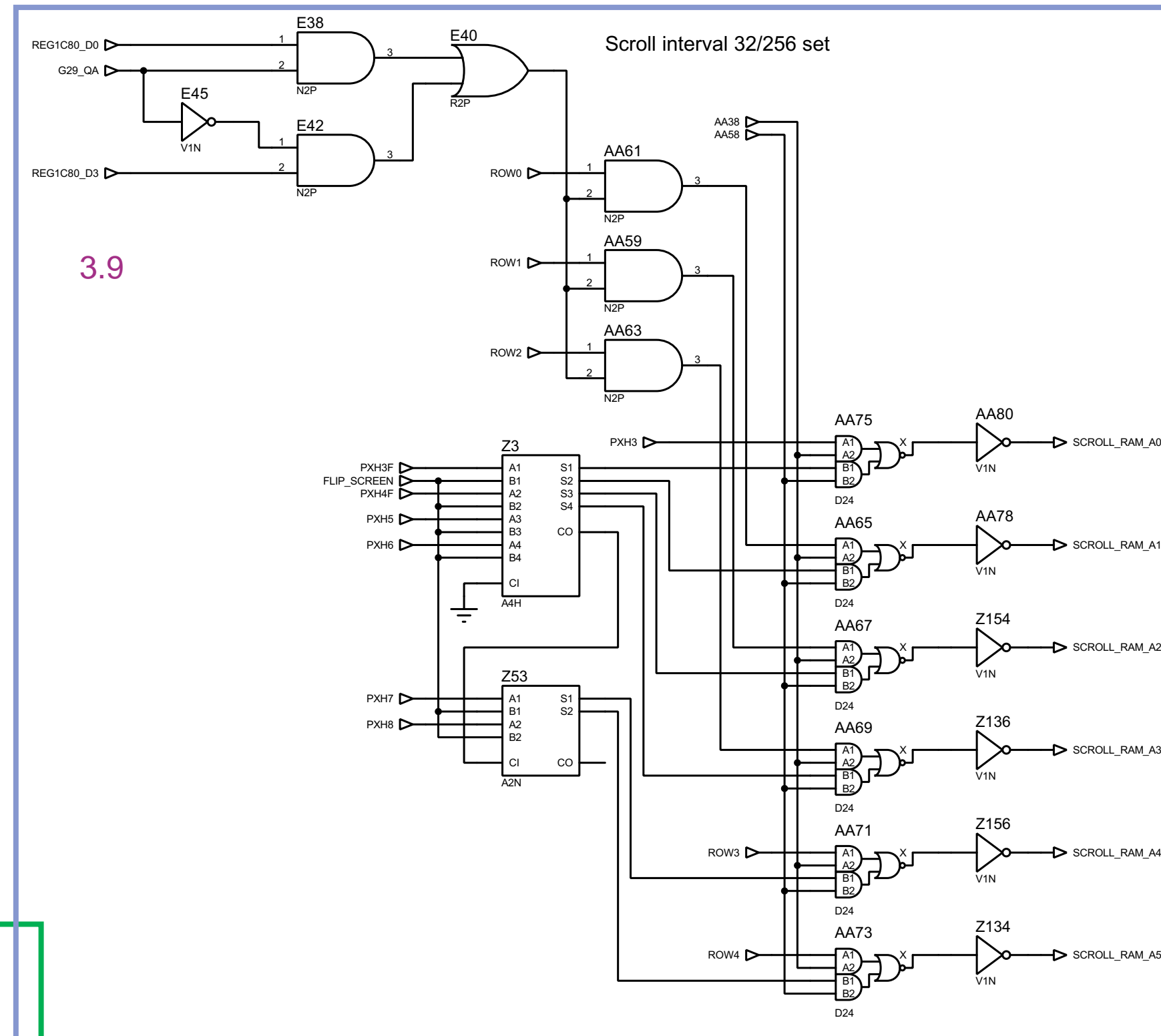
3.7



3.8

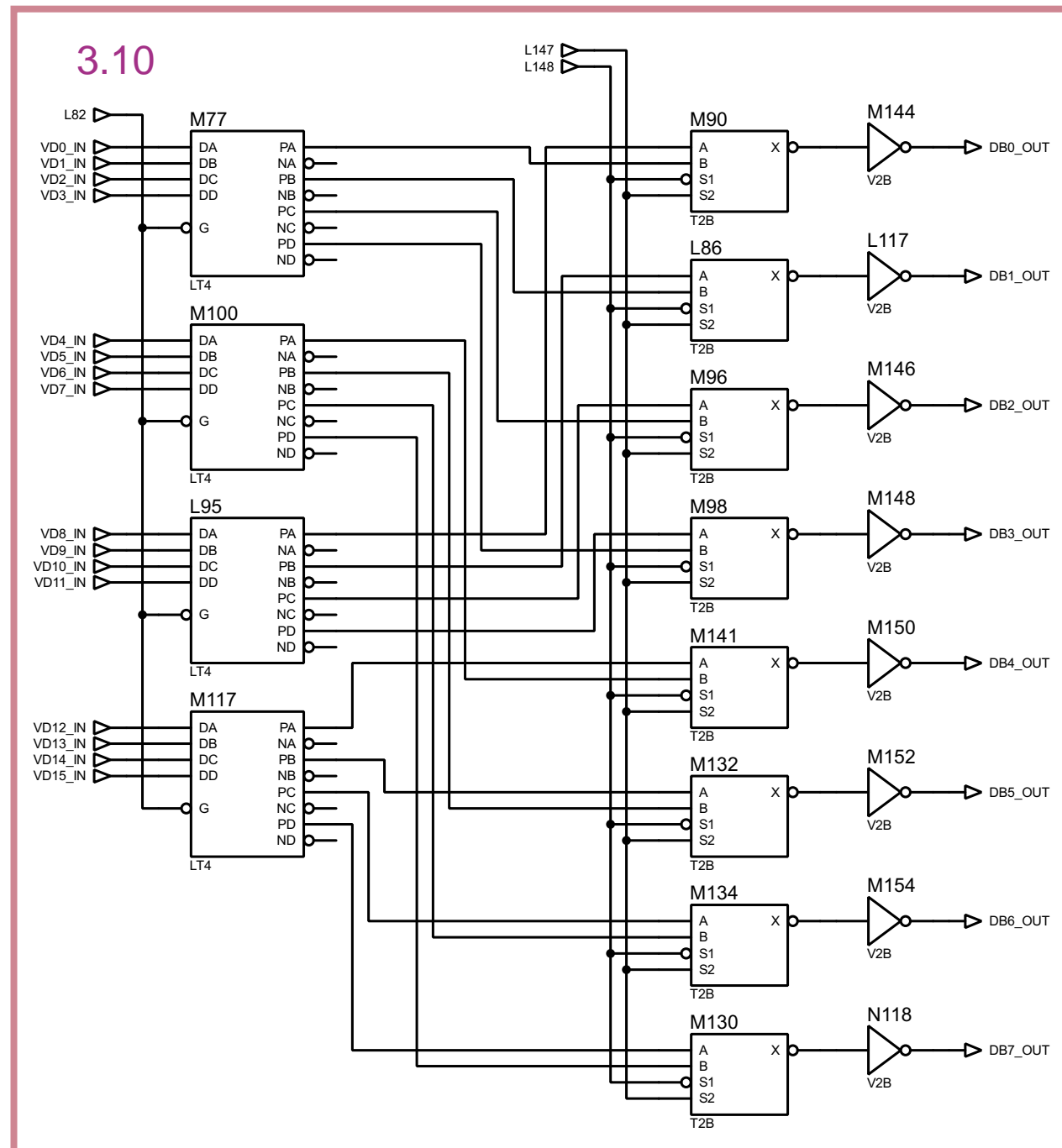


3.9



VRAM read by CPU

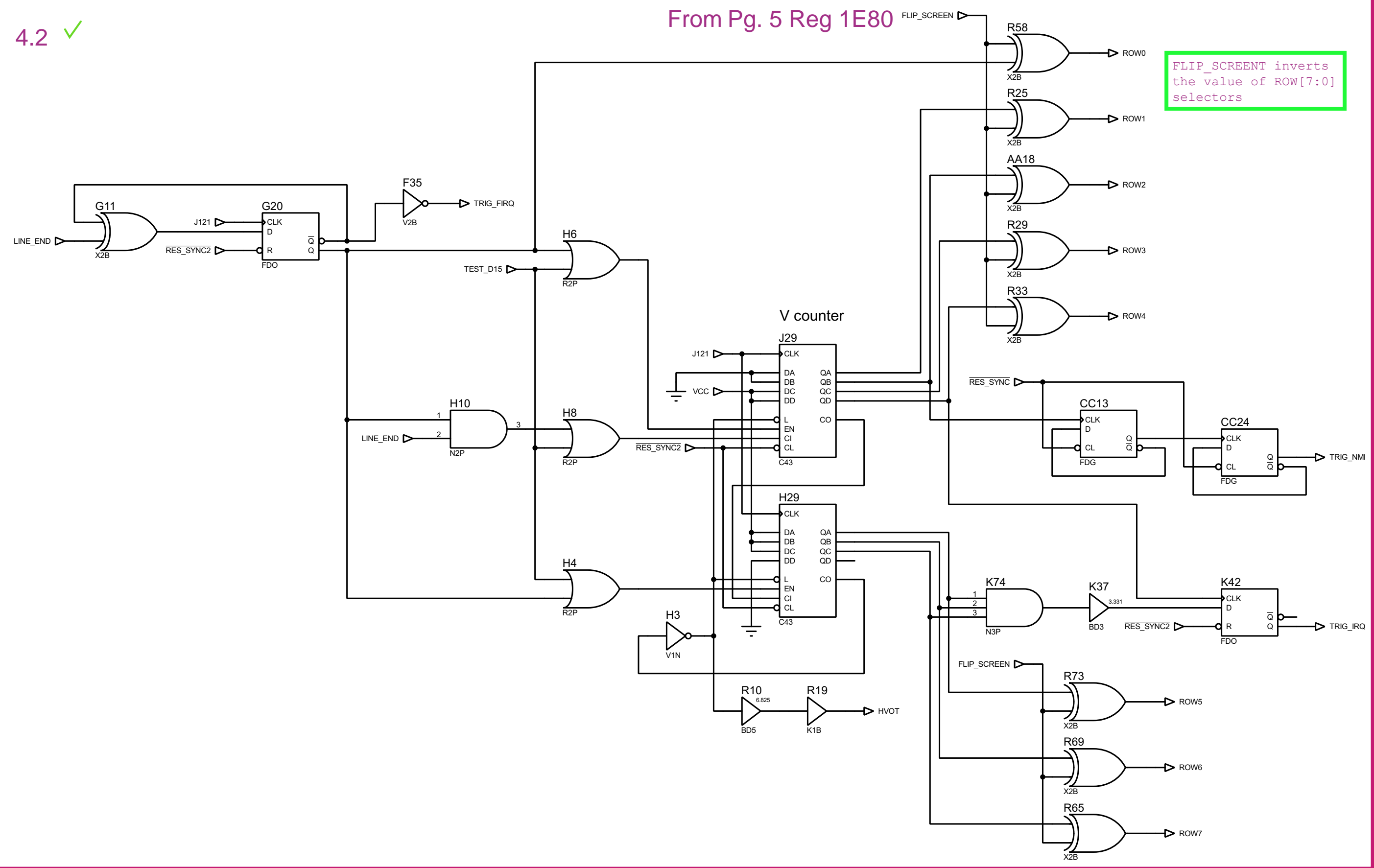
3.10



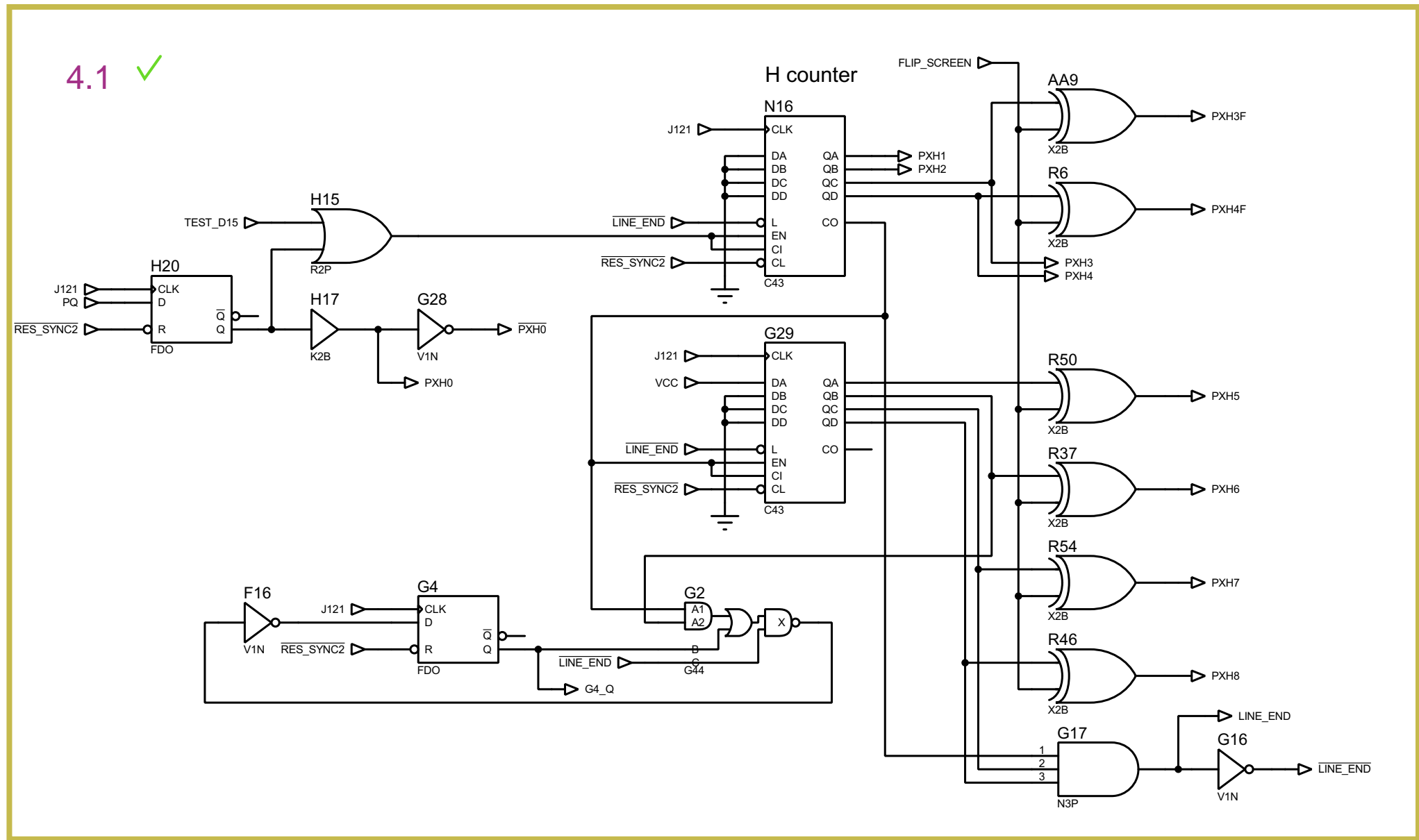
wire [7:0] DB_IN

wire [7:0] DB_BUF

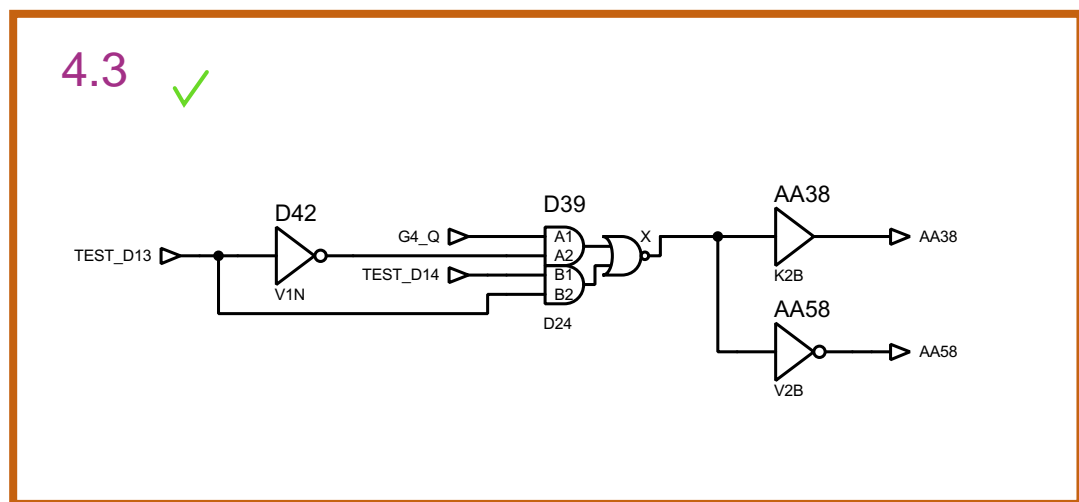
4.2 ✓



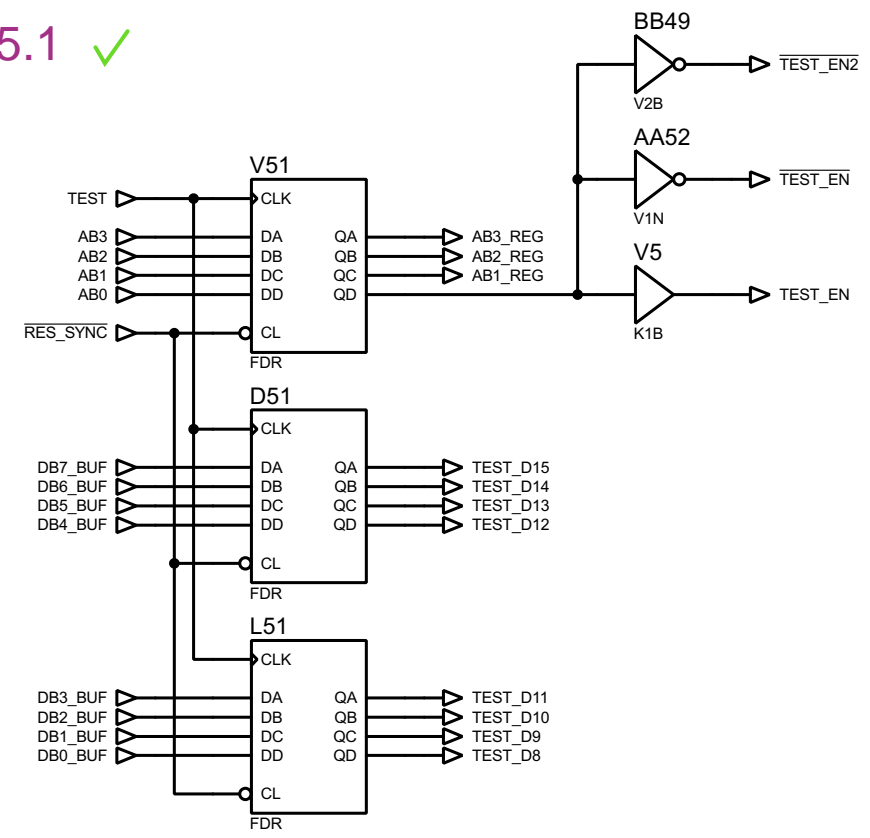
4.1 ✓



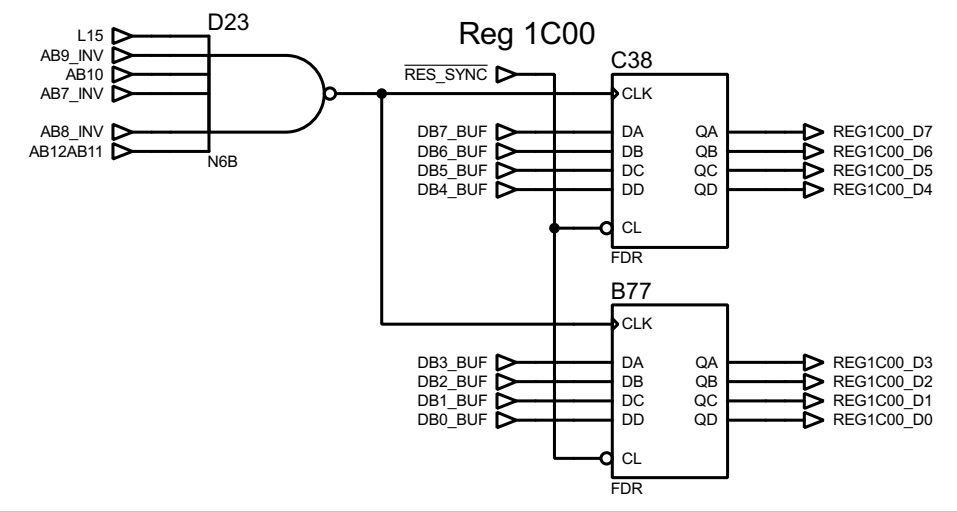
4.3 ✓



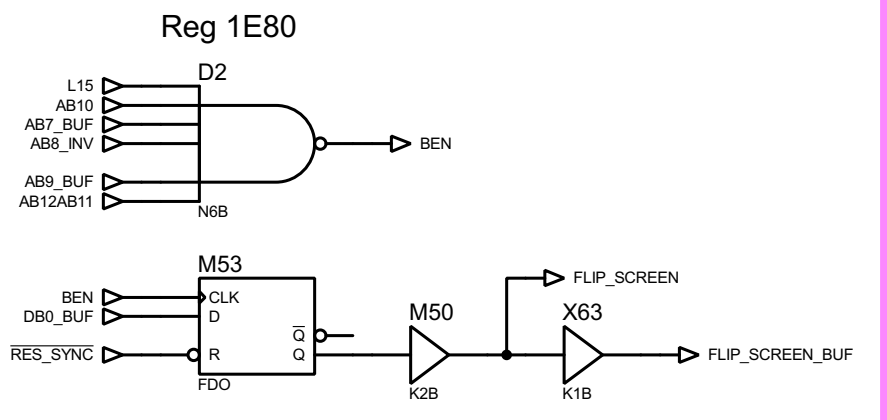
5.1 ✓



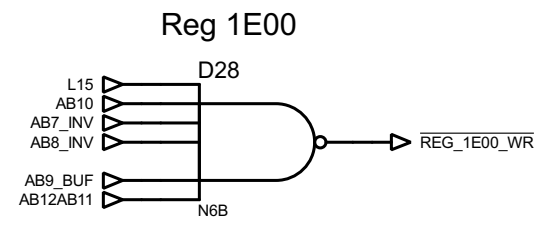
5.4 ✓



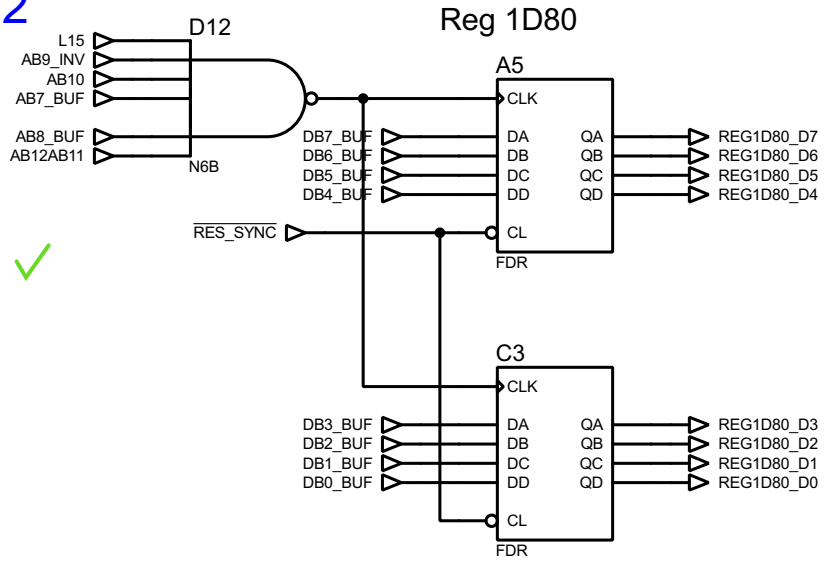
5.7 ✓



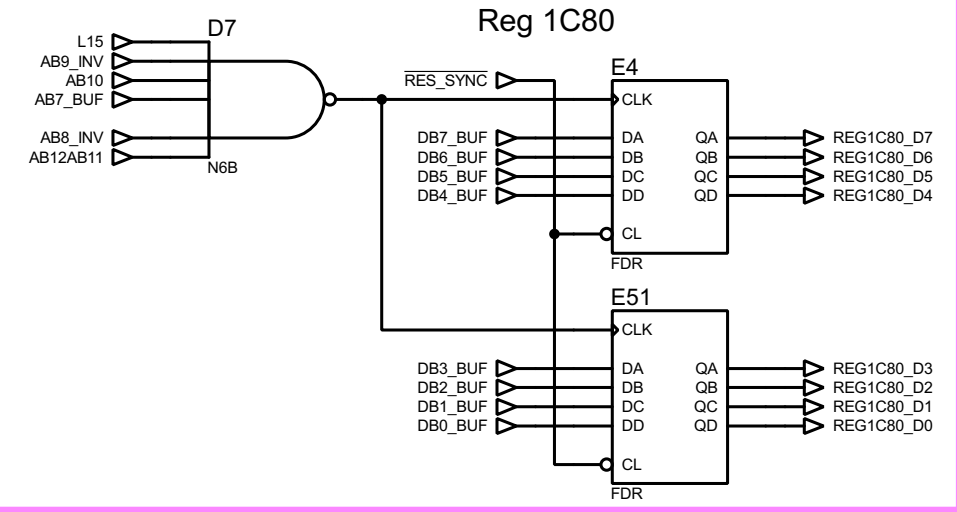
5.8 ✓



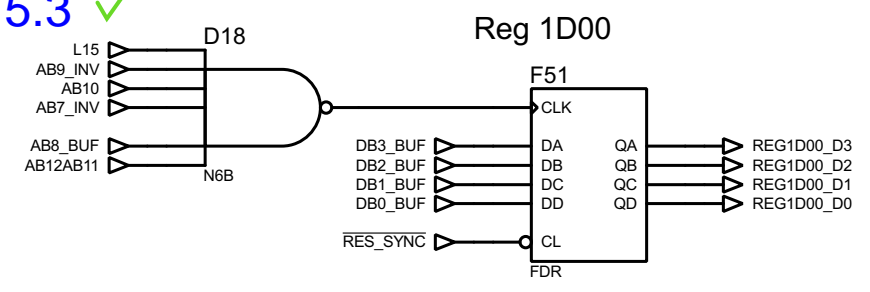
5.2 ✓



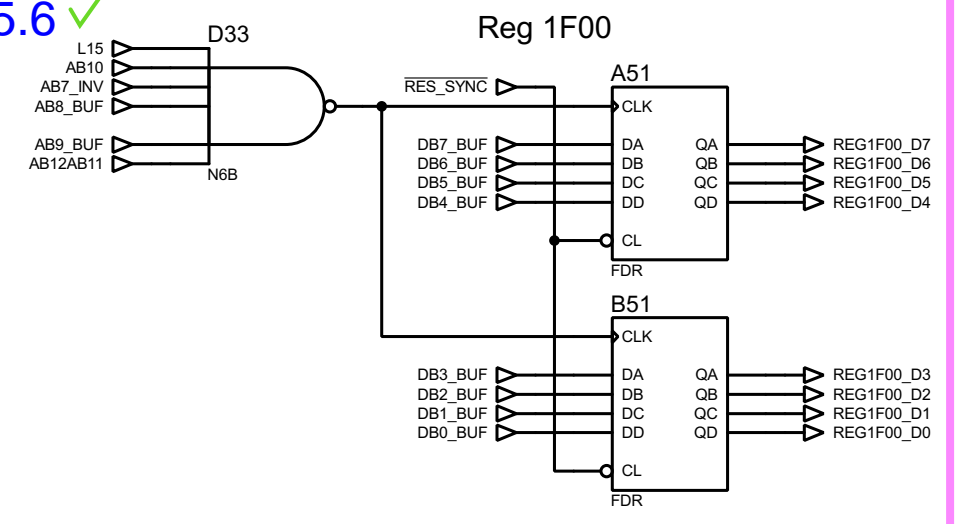
5.5 ✓



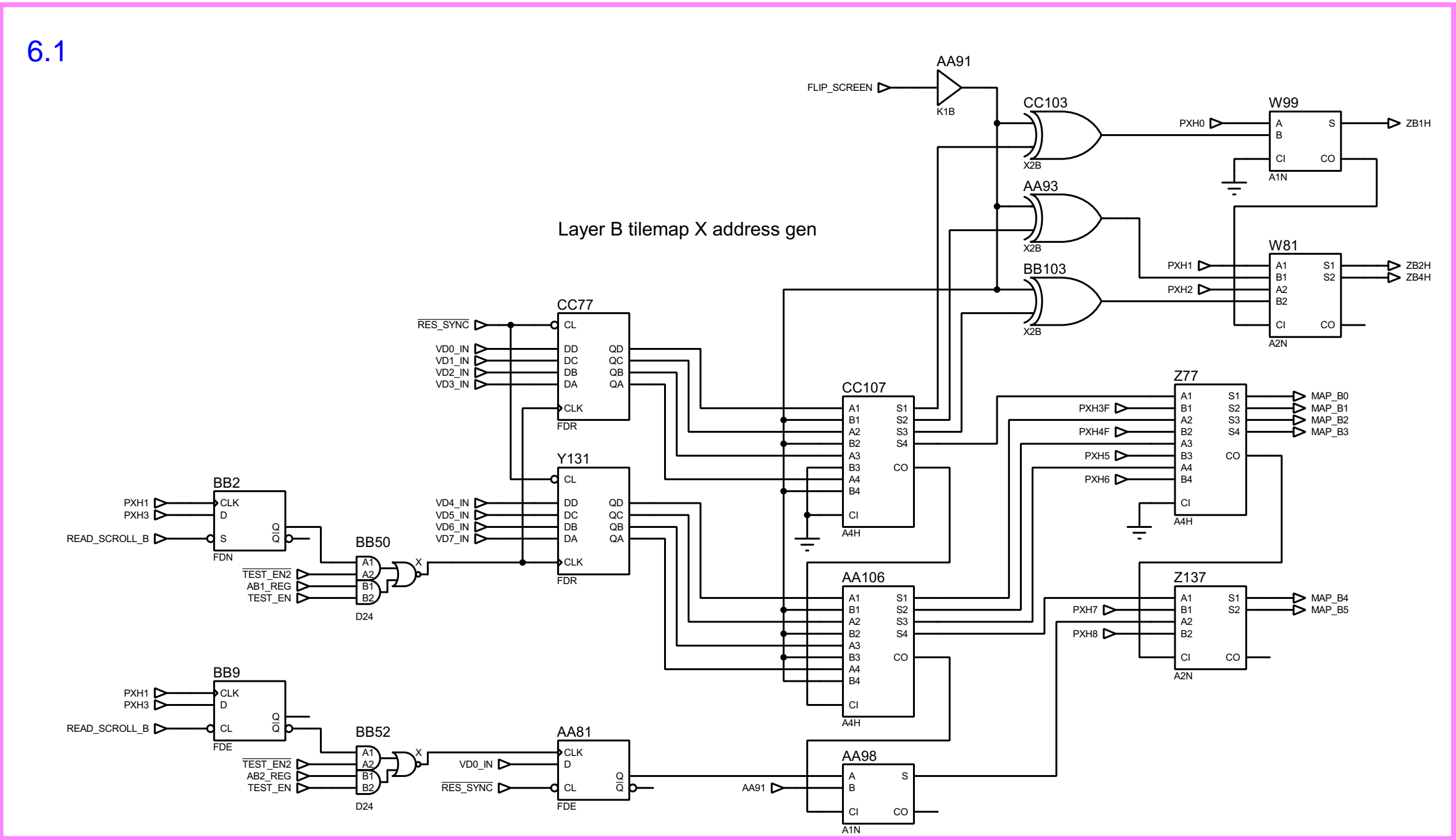
5.3 ✓



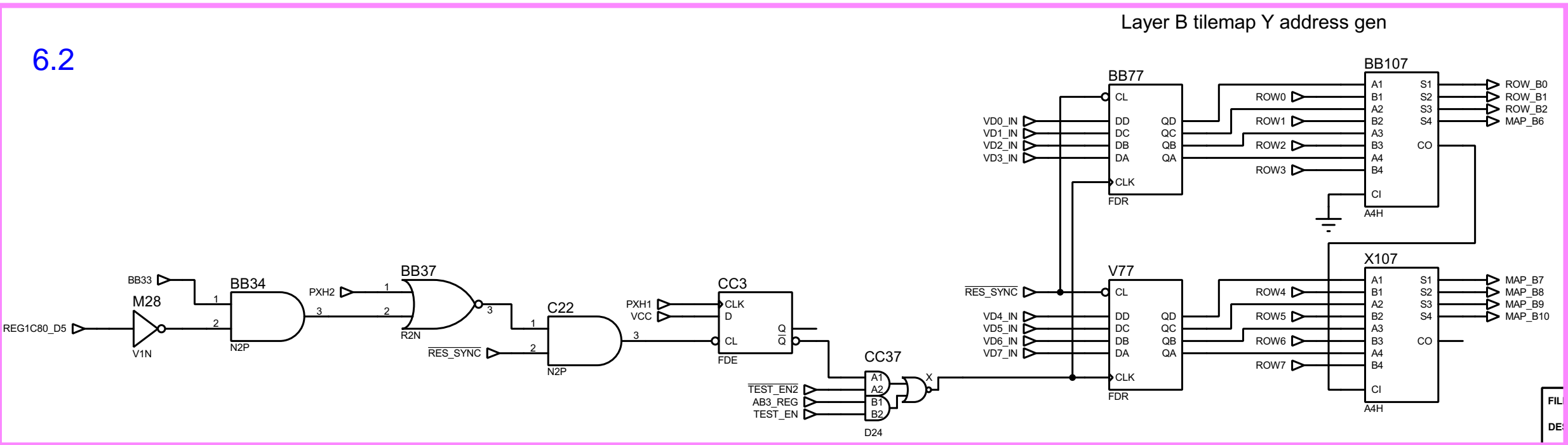
5.6 ✓



6.1



6.2



The diagram illustrates the logic for the GFX ROM bank during CPU testing. It features a 4-to-1 multiplexer (E77) that selects between four 8-bit ROM banks (DB3_BUF, DB2_BUF, DB1_BUF, DB0_BUF) based on the REG_TE00_WR signal. The selected data is then routed through various logic gates (AND, OR, NOT) and registers (REG1C00_D5, REG1C00_D6) to produce the final output signals (COL2, COL3).

Key Components and Signals:

- Inputs:** REG_TE00_WR, DB3_BUF, DB2_BUF, DB1_BUF, DB0_BUF, RES_SYNC, F41, F24, REG1D80_D0, REG1D80_D4, REG1F00_D0, REG1F00_D4, REG1D80_D1, REG1D80_D5, REG1F00_D1, REG1F00_D5, REG1D80_D2, REG1D80_D6, REG1F00_D2, REG1F00_D6, REG1D80_D3, REG1D80_D7, REG1F00_D3, REG1F00_D7.
- Logic Gates:** AND gates (B3, B19, B40, B28), OR gates (C36, C29, C75, C155), NOT gates (A35, A31, C74, E149, E150, E145, E141, H124).
- Registers:** REG1C00_D5, REG1C00_D6.
- Outputs:** COL2, COL3.

7.2

7.3

GFX ROM bank for CPU testing

7.4

7.5

Scroll RAM read triggers

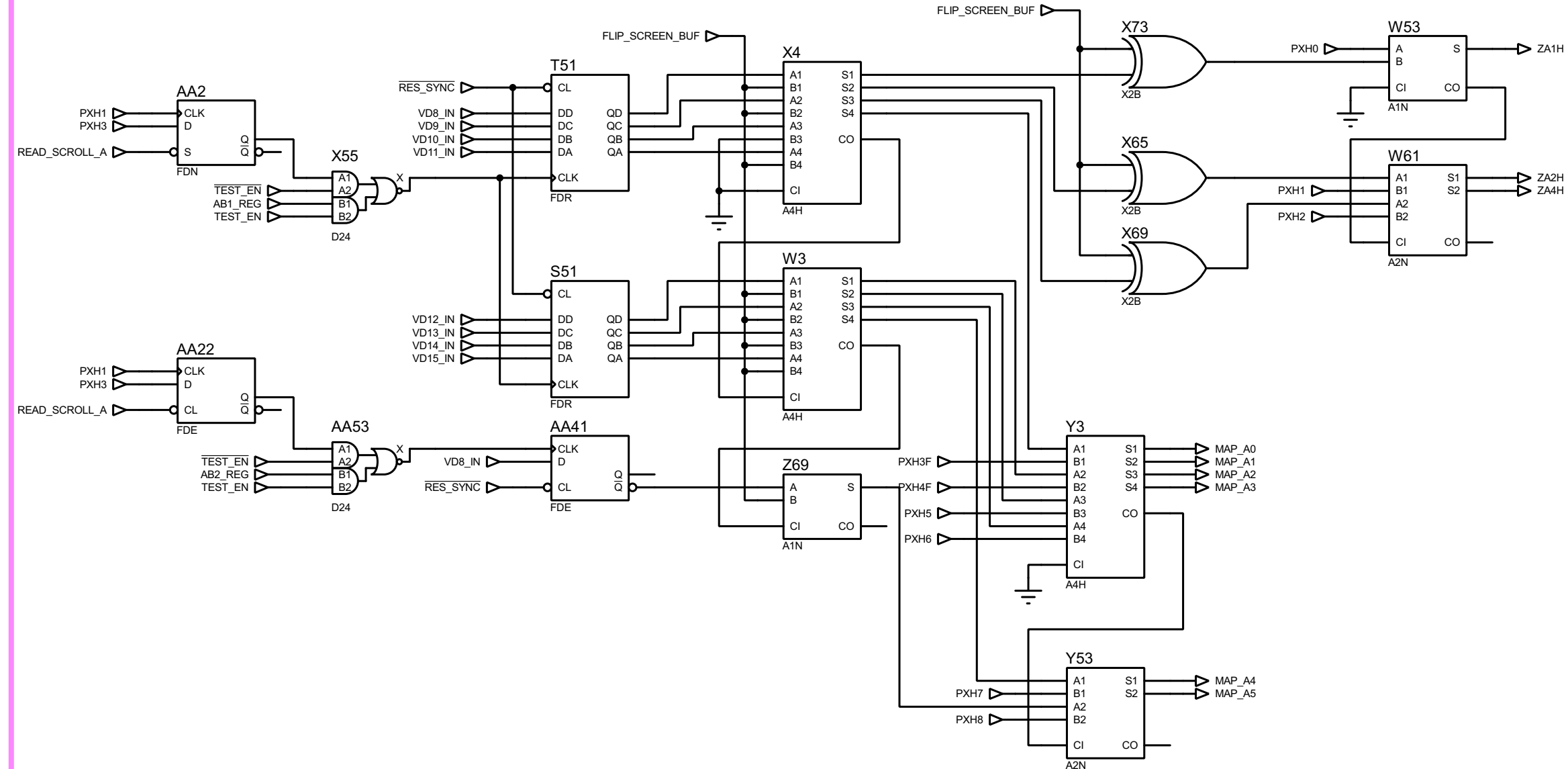
Read scroll RAM at least once at row 0

```

graph LR
    ROW0[ROW0] --> X57
    ROW4[ROW4] --> X57
    ROW3[ROW3] --> X57
    ROW2[ROW2] --> X57
    ROW1[ROW1] --> X57
    ROW7[ROW7] --> X57
    ROW5[ROW5] --> X57
    X57 --> REG1C80_D4
    REG1C80_D4 --> F8
    REG1C80_D1 --> F25
    F8 --> R2P
    F25 --> R2P
    G4_Q --> F7
    G29_QA --> F14
    F7 --> F10
    F14 --> F10
    F7 --> F36
    F14 --> F36
    RES_SYNC --> F10
    RES_SYNC --> F36
    F10 --> READ_SCROLL_B
    F36 --> READ_SCROLL_A
    F10 --> N4P1[N4P]
    F36 --> N4P2[N4P]
  
```

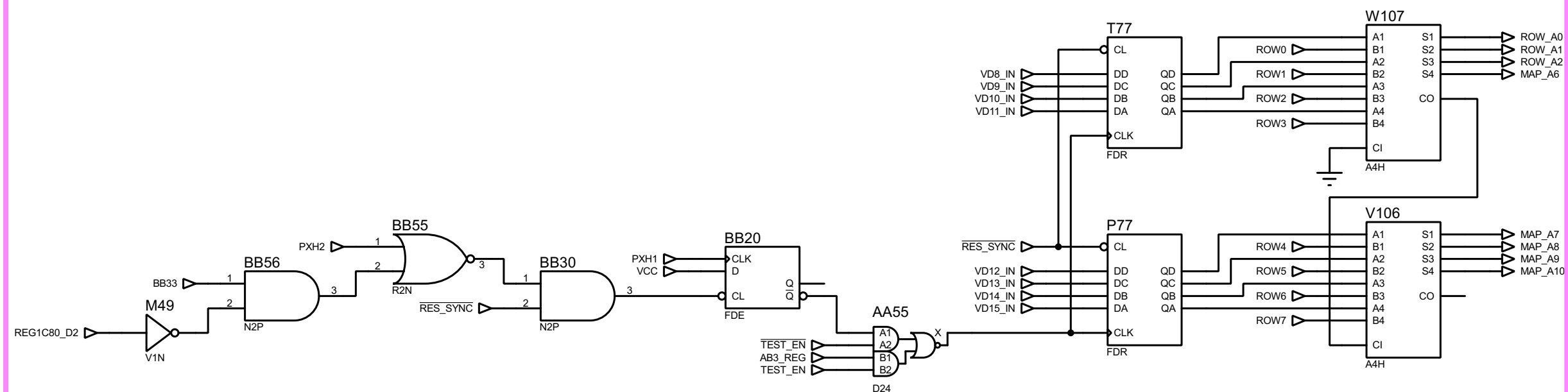
8.1

Layer A tilemap X address gen



8.2

Layer A tilemap Y address gen



FILE NAME: k052109.pdsprj

DESIGN TITLE: Konami 052109
LAYER A SCROLL

BY: Sean Gonsalves

REV: A

DATE: 22/06/2021

PAGE: 8 of 8