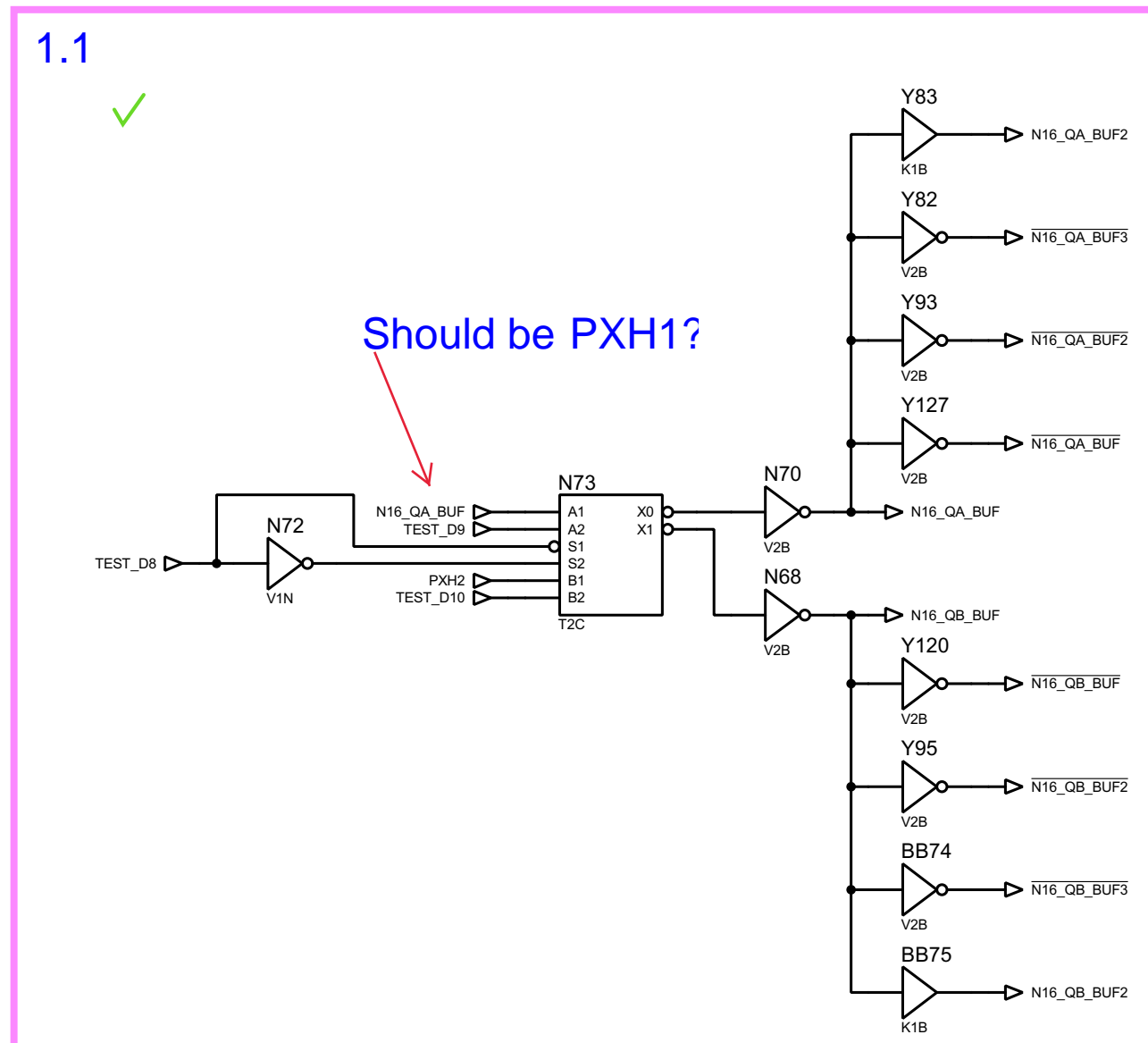


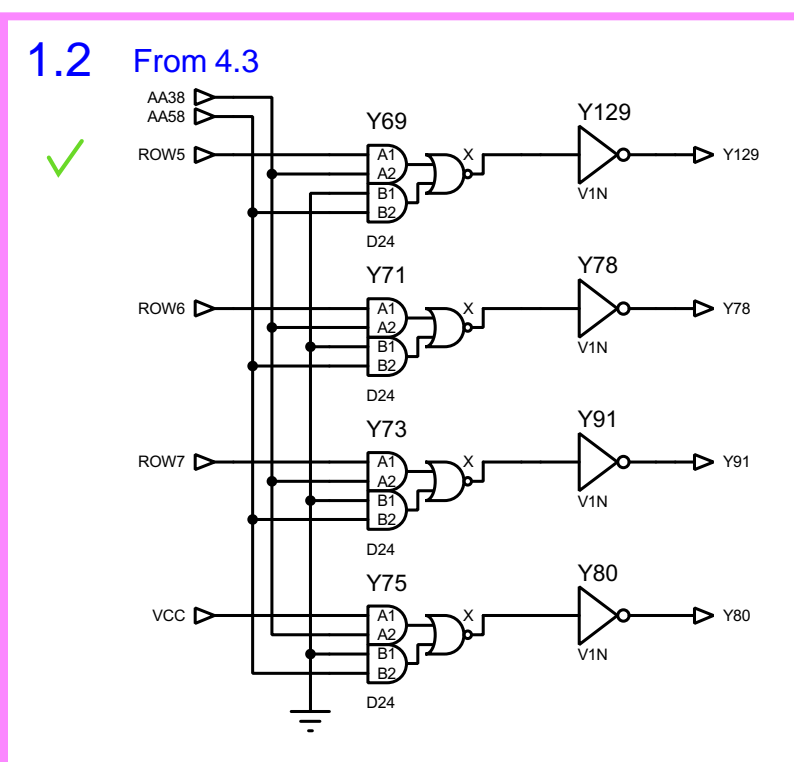
```

VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 01xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 110x xxxx xxxx A y scroll
0000 110x xxxx xxxx B y scroll
0000 01xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 110x xxxx xxxx B y scroll
0001 110x xxxx xxxx B x scroll
0001 1101 x xxxx x Tilemaps X
          xxx x Tilemaps Y

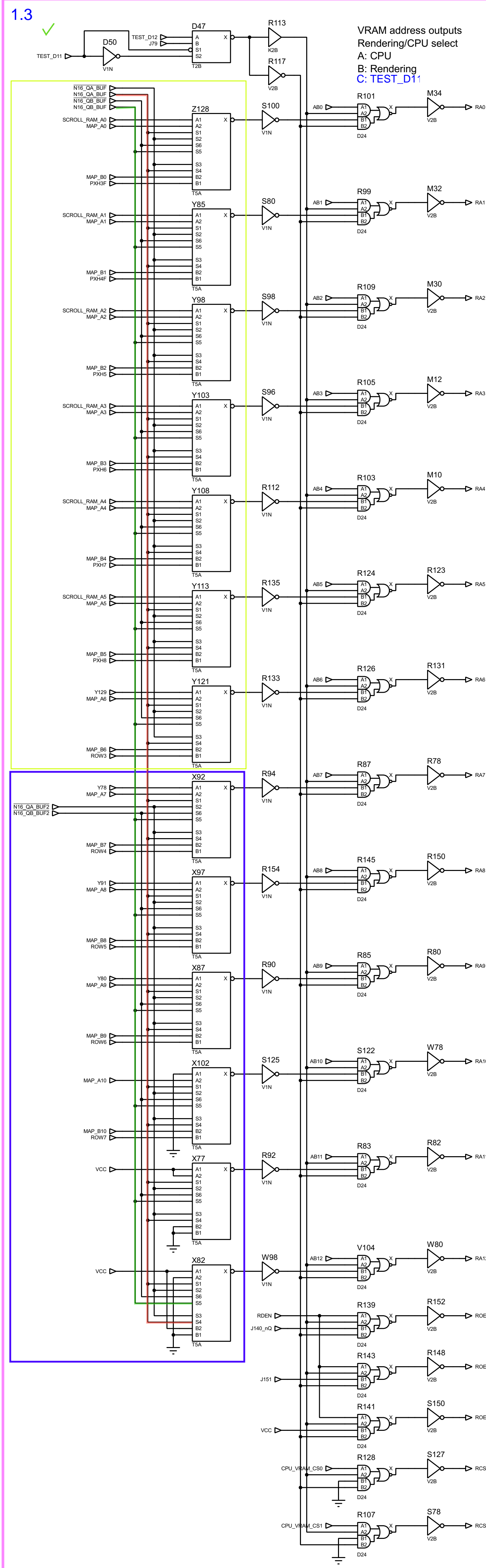
```

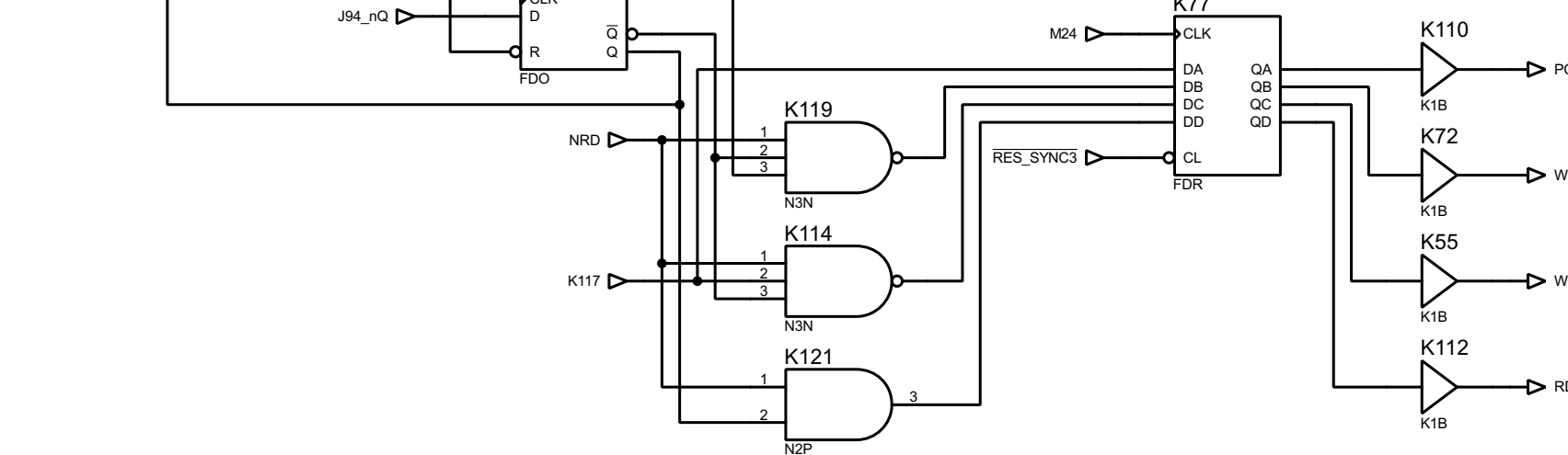
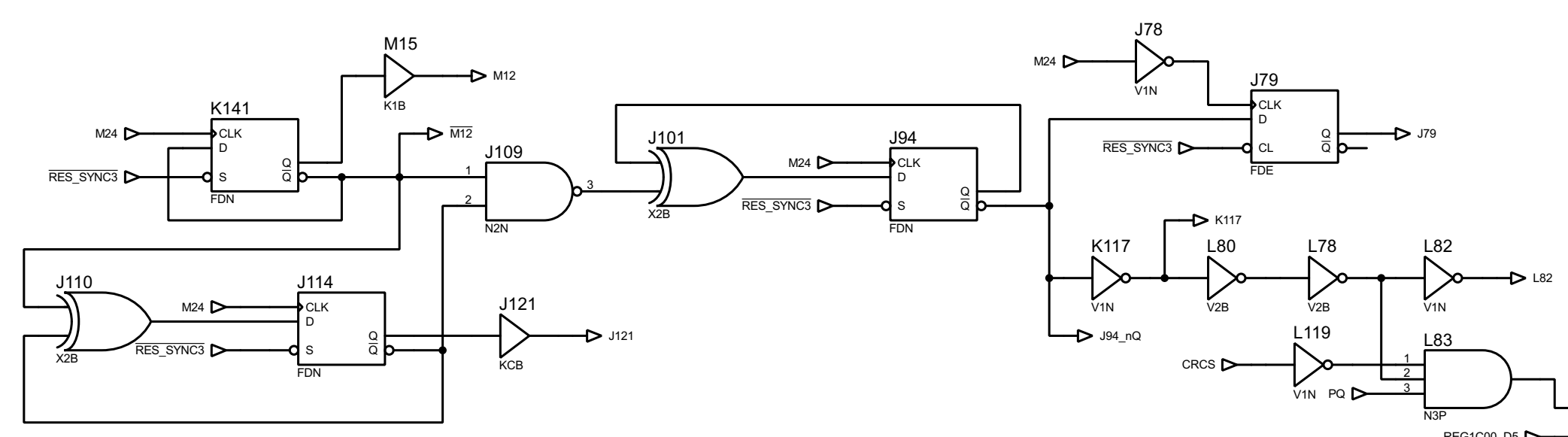


### TEST\_D13 Addresses Selector



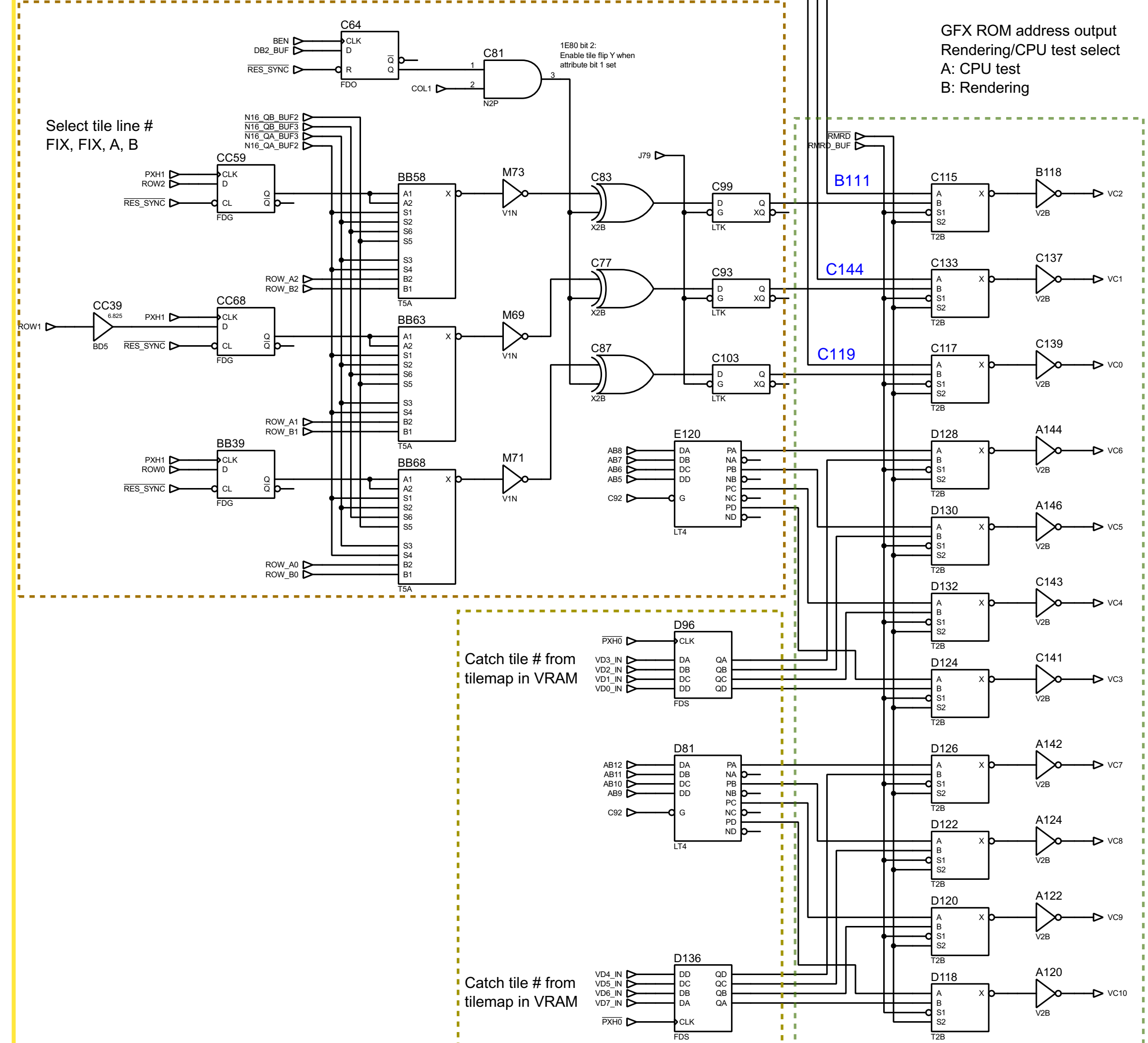
Selection can be simplified using AA38 (and AA38n) only, AA58 always selects 1'b0.





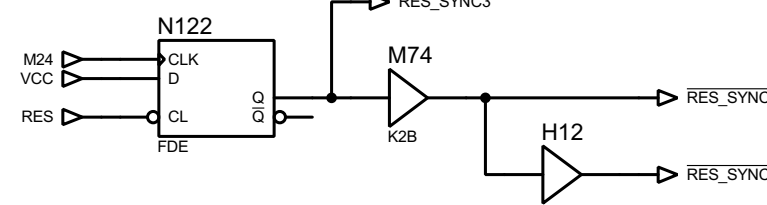
## TIMING SIGNALS

SKIP because AB[1:0] used to select byte



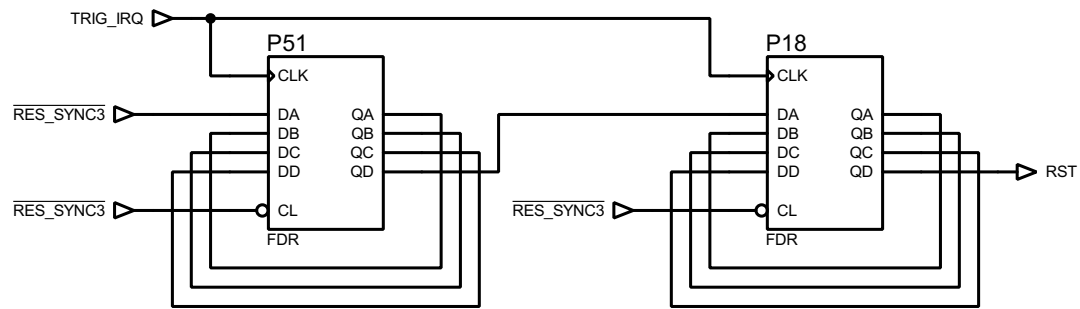
### RES\_SYNC signals generator

3.1 ✓

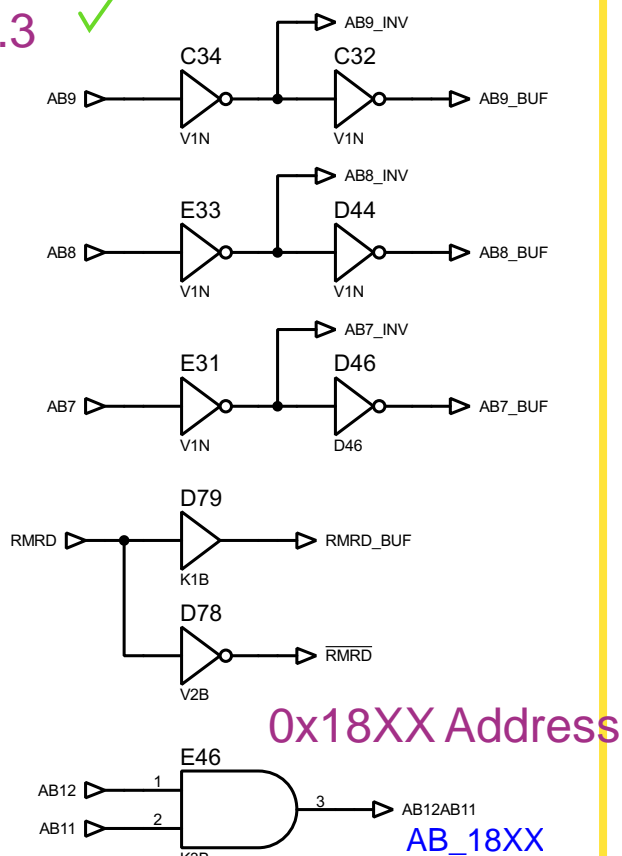


3.2 ✓

8-frame delay for  
RES -> RST  
Same in k051962 ?

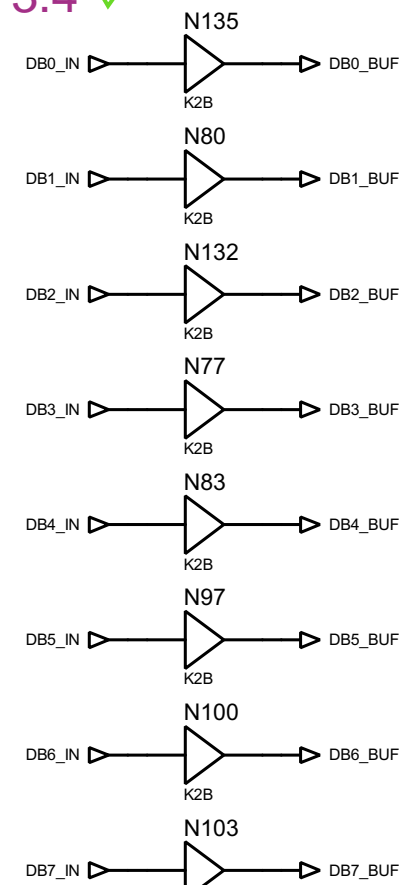


3.3 ✓



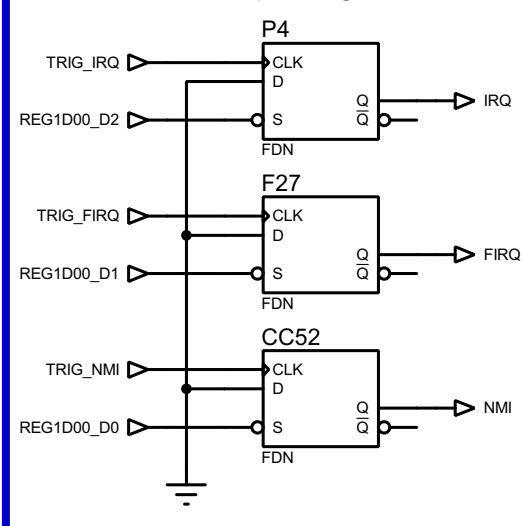
180c-1833: Layer A Y Scroll

3.4 ✓

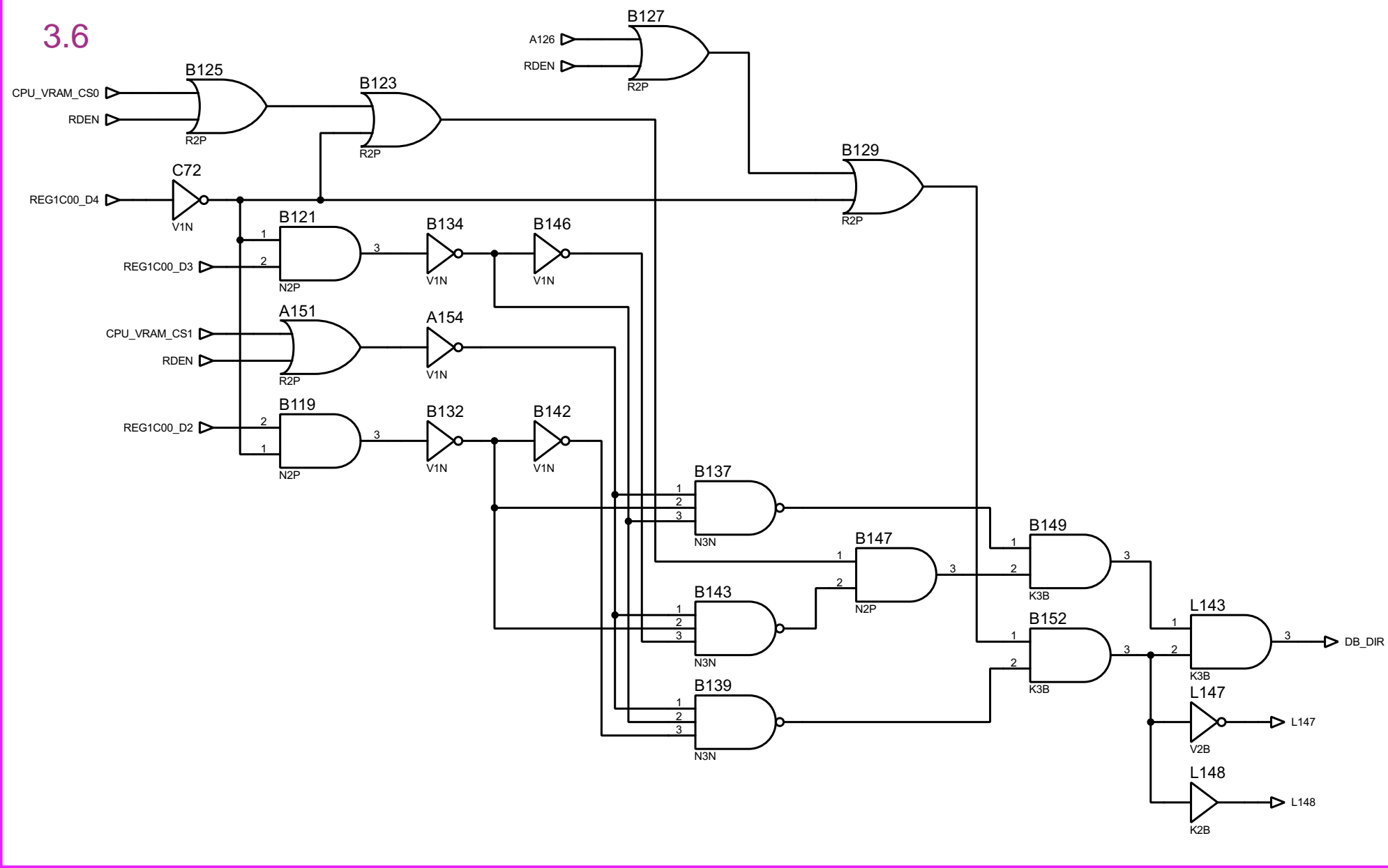


3.5 ✓

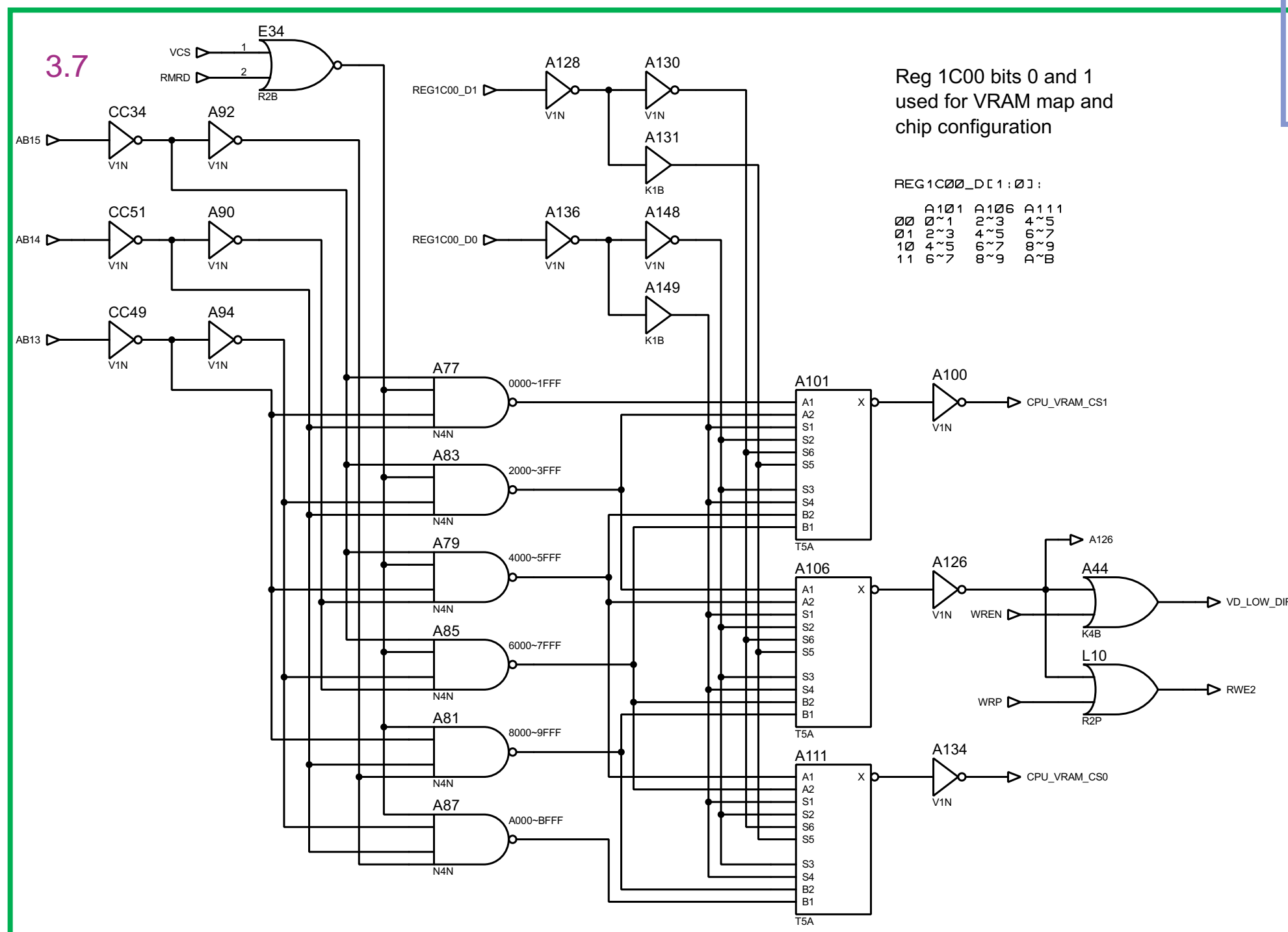
Interrupts flags



3.6



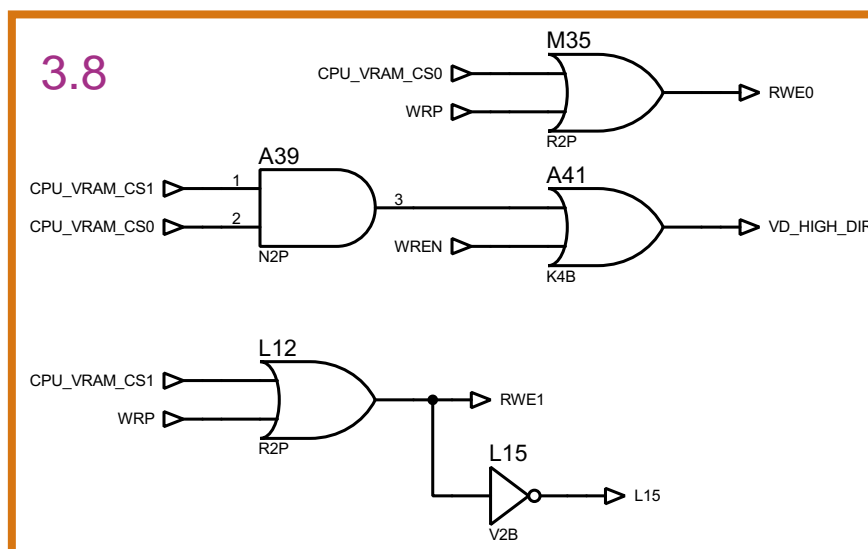
3.7



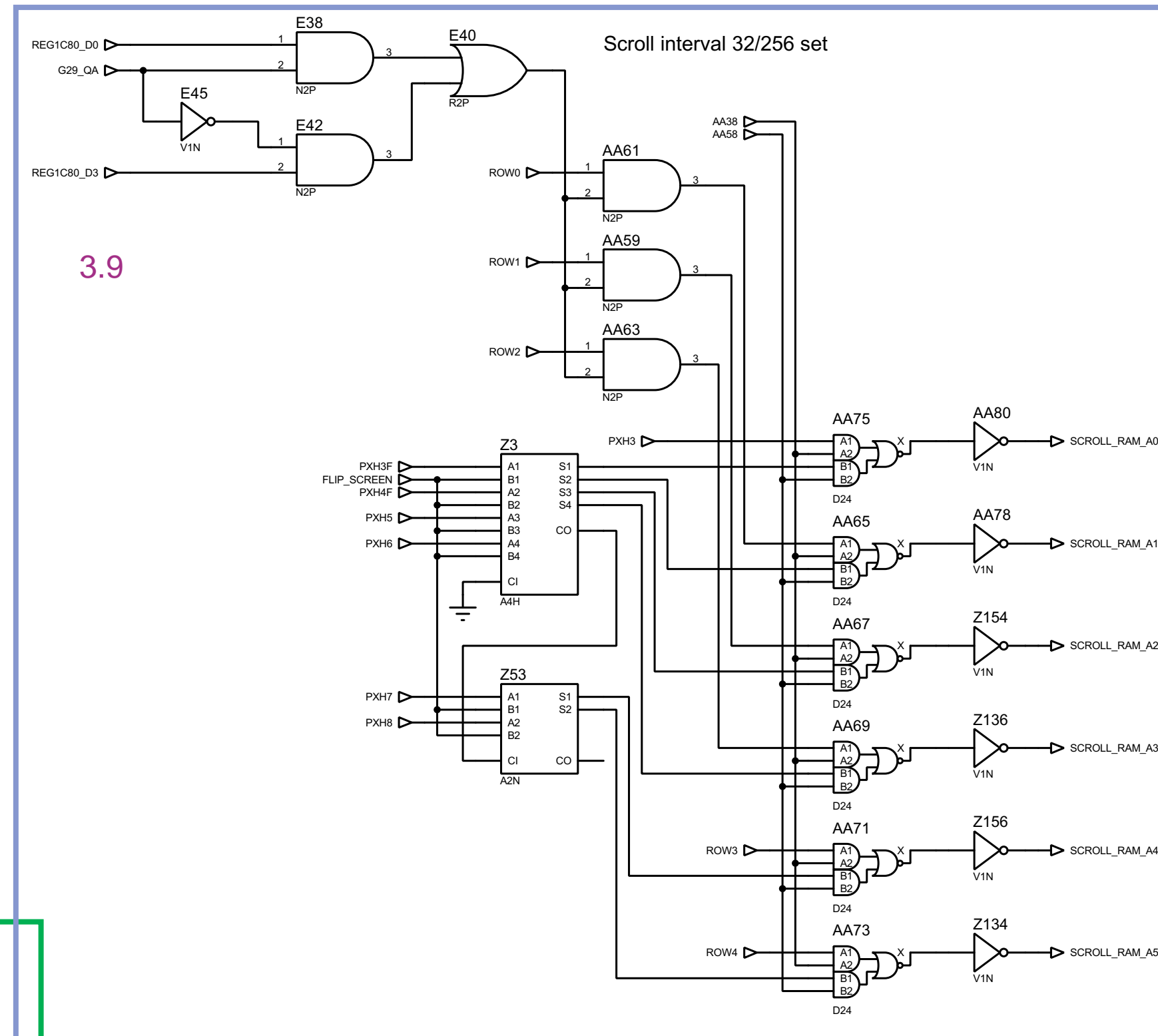
Reg 1C00 bits 0 and 1  
used for VRAM map and  
chip configuration

REG1C00\_D[1:0]:  
00 0~1 2~3 4~5 6~7 8~9 A~B  
01 2~3 4~5 6~7 8~9 A~B  
10 4~5 6~7 8~9 A~B  
11 6~7 8~9 A~B

3.8

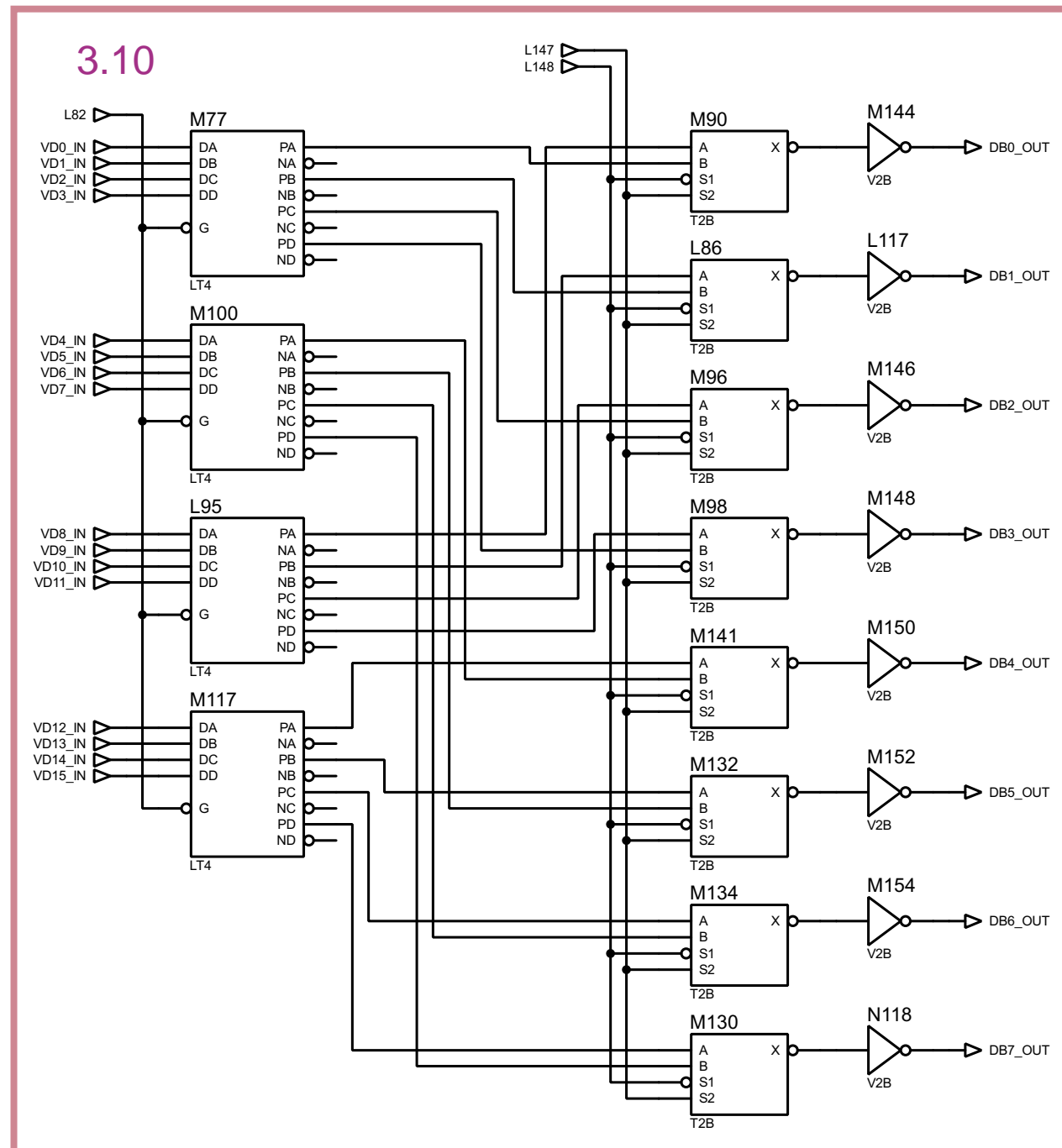


3.9



VRAM read by CPU

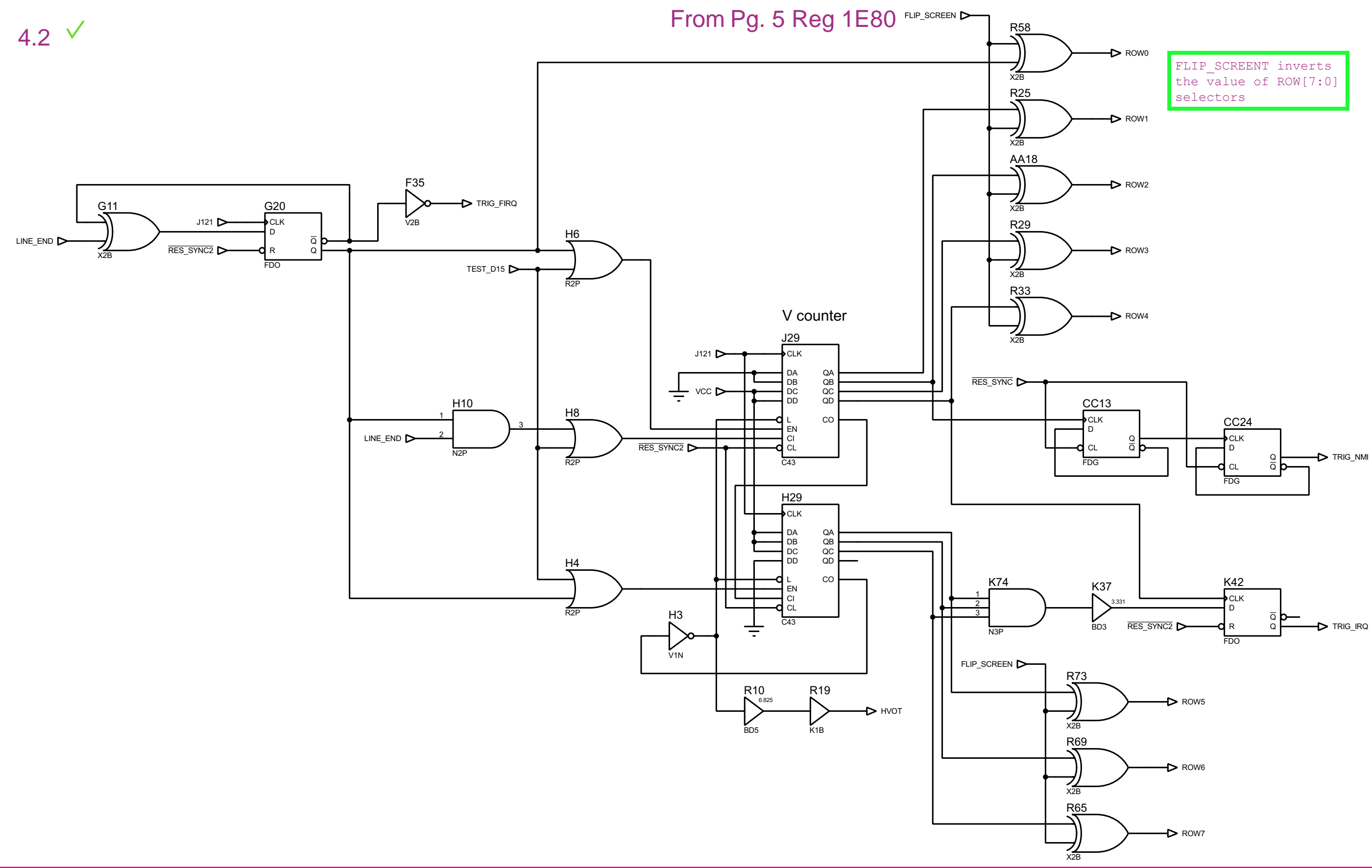
3.10



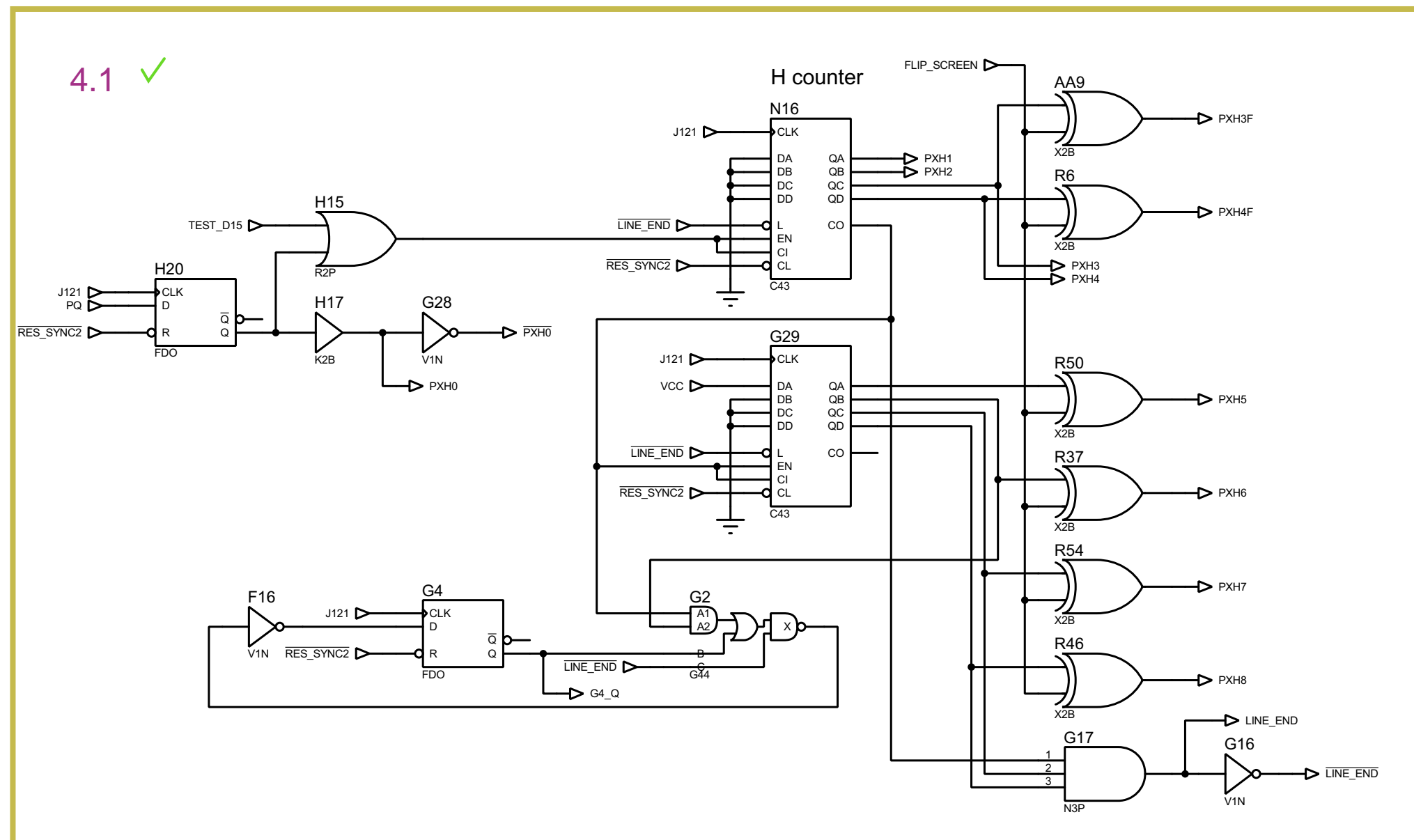
wire [7:0] DB\_IN

wire [7:0] DB\_BUF

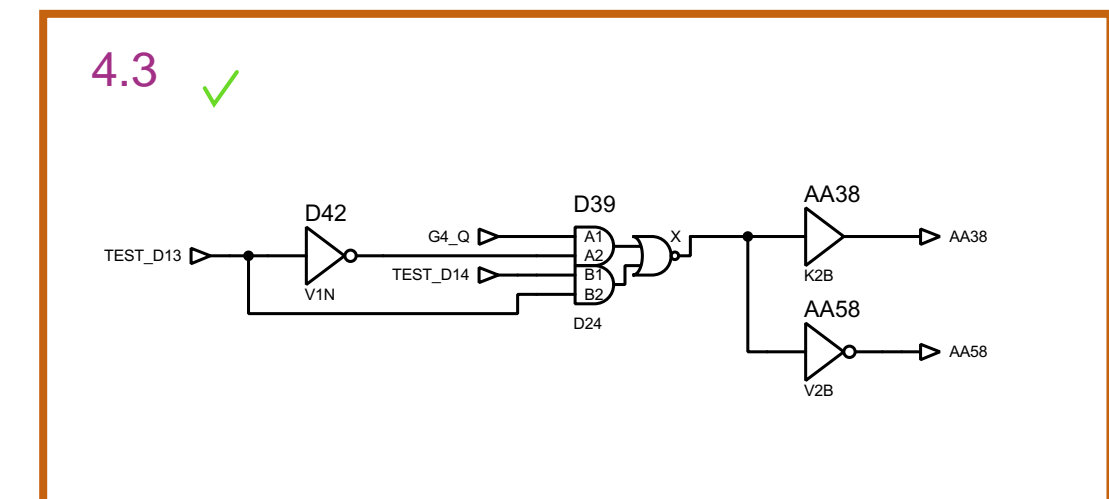
4.2 ✓



4.1 ✓

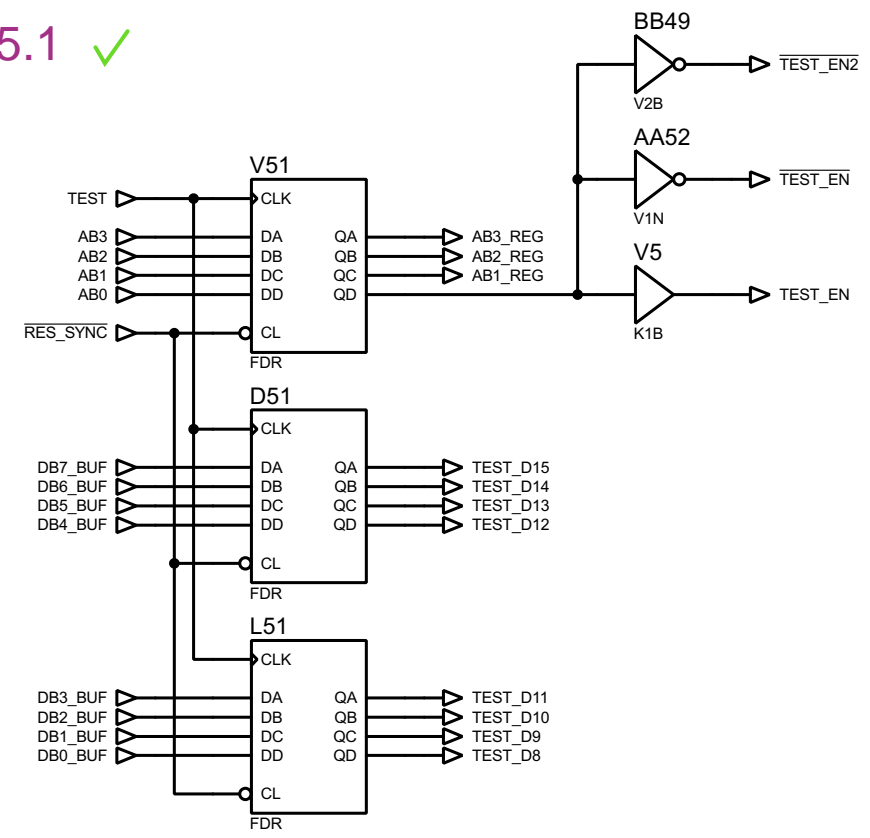


4.3 ✓

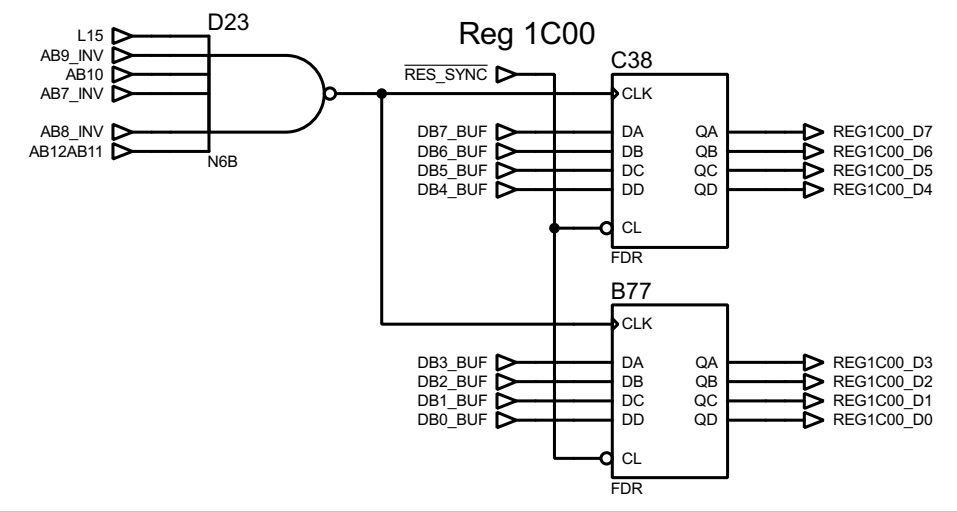




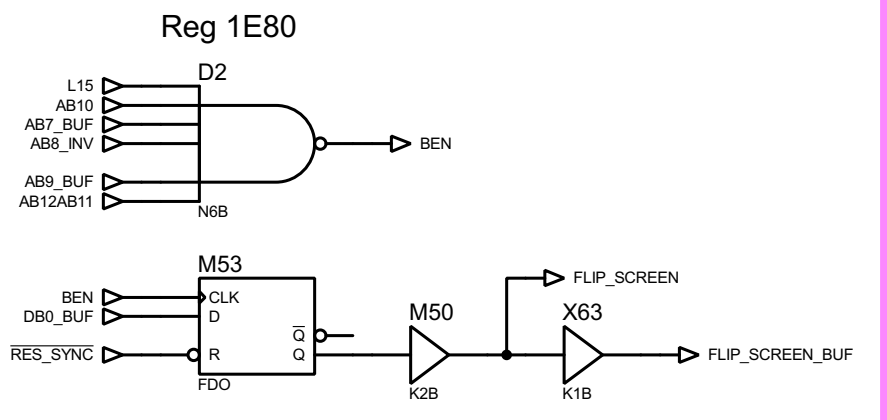
5.1 ✓



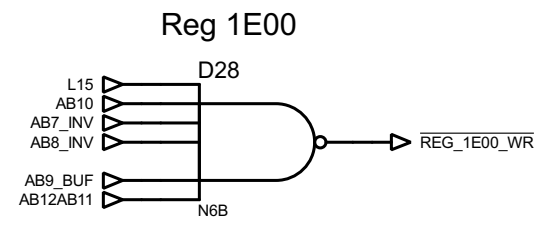
5.4 ✓



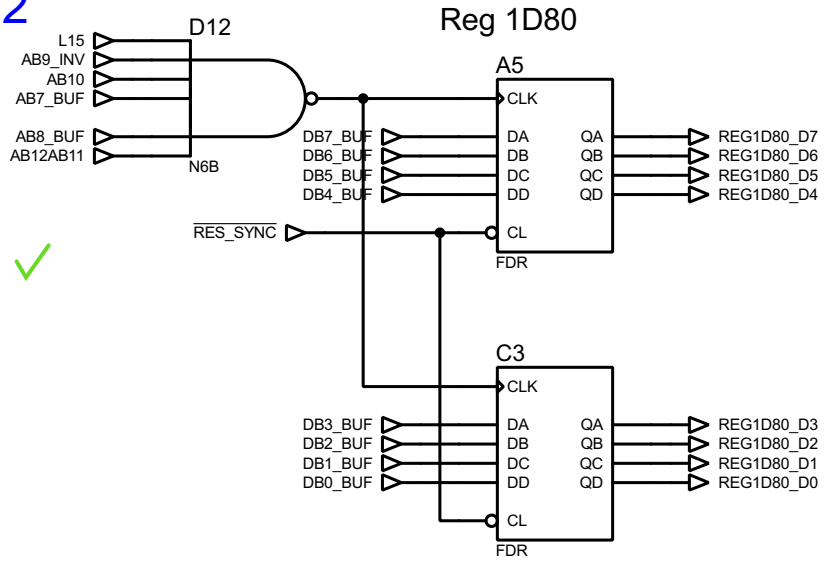
5.7 ✓



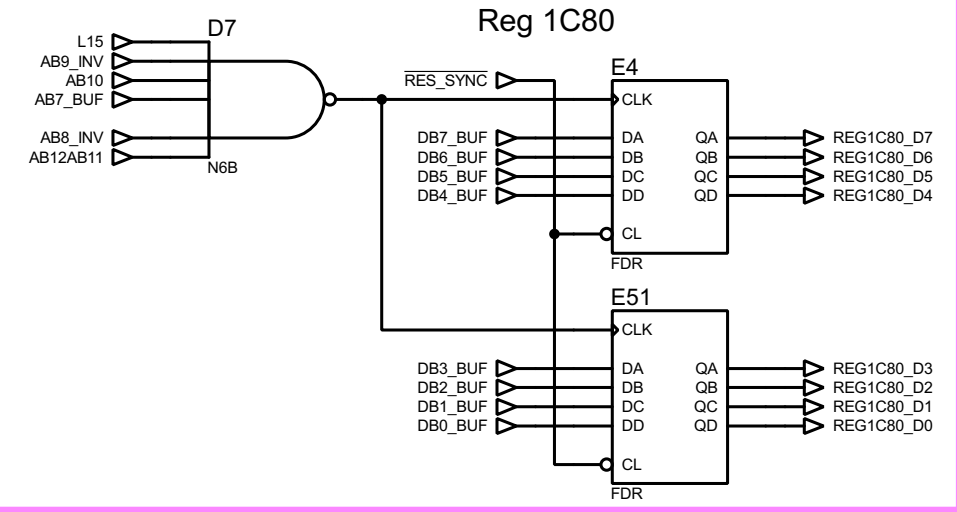
5.8 ✓



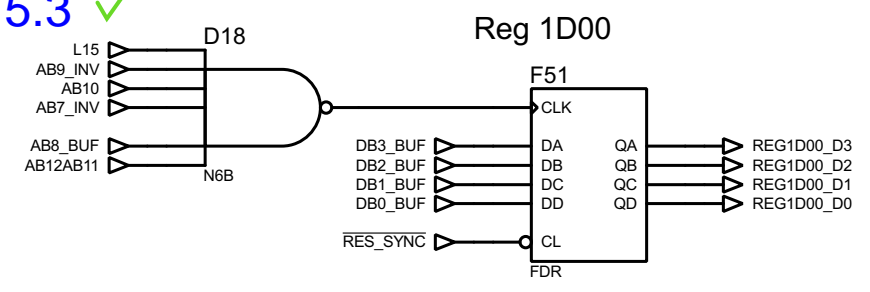
5.2 ✓



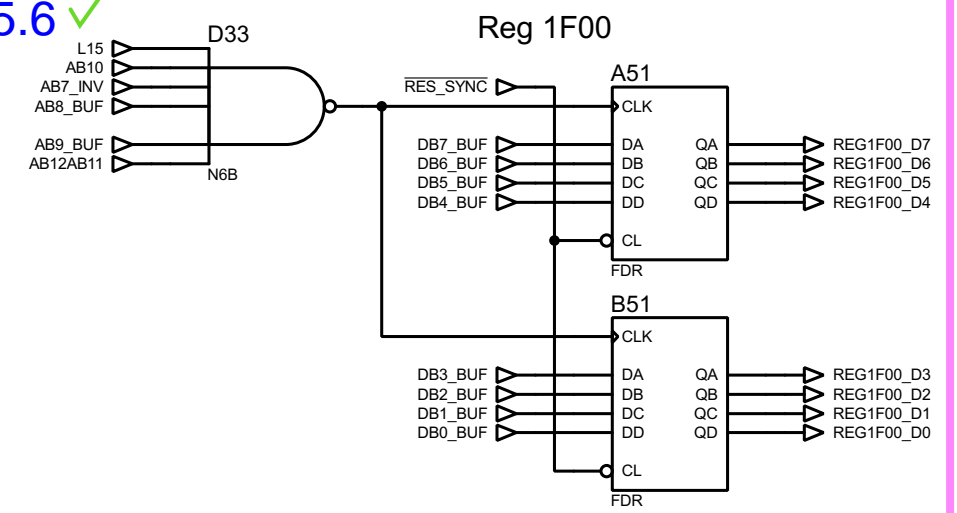
5.5 ✓



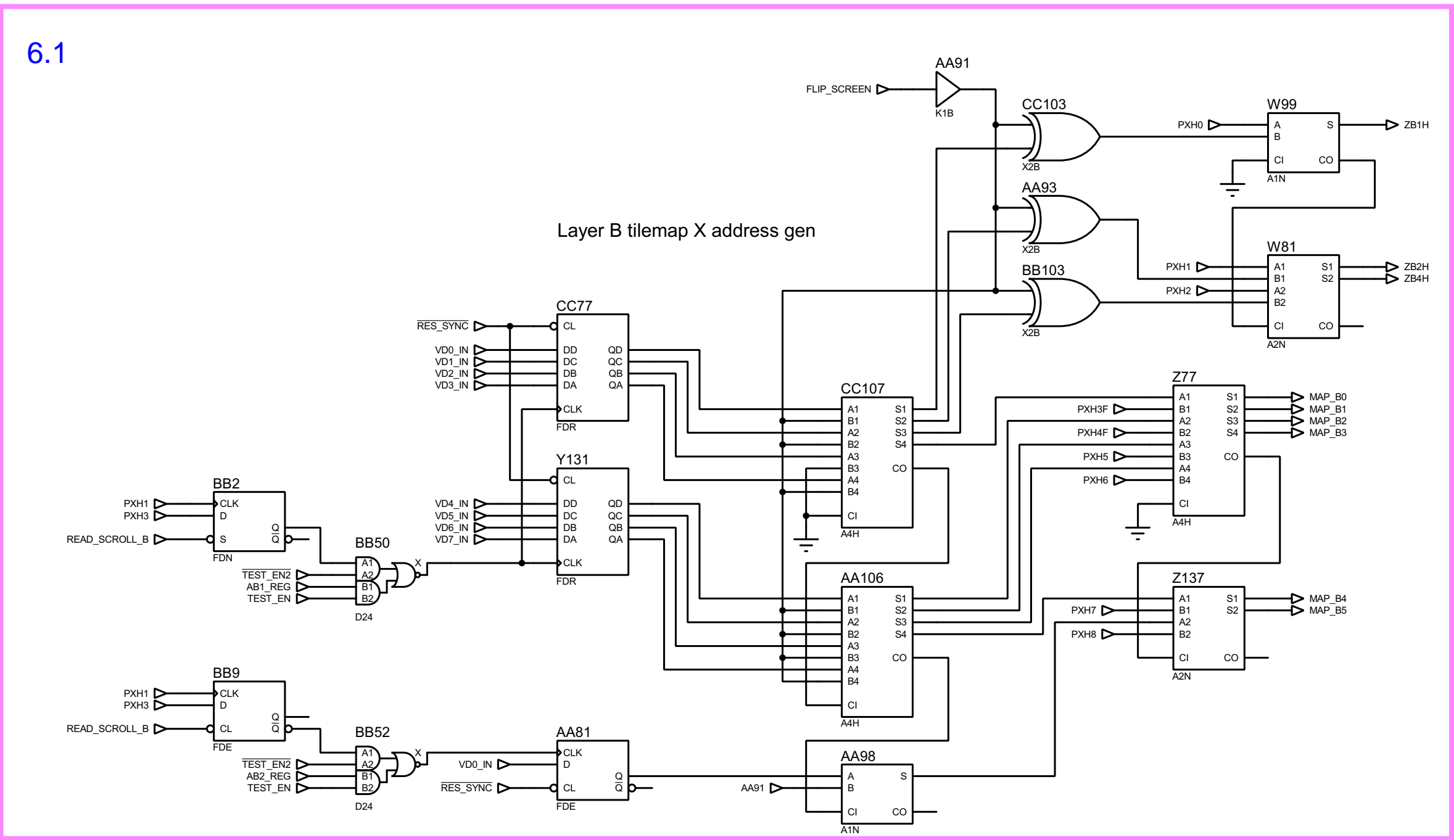
5.3 ✓



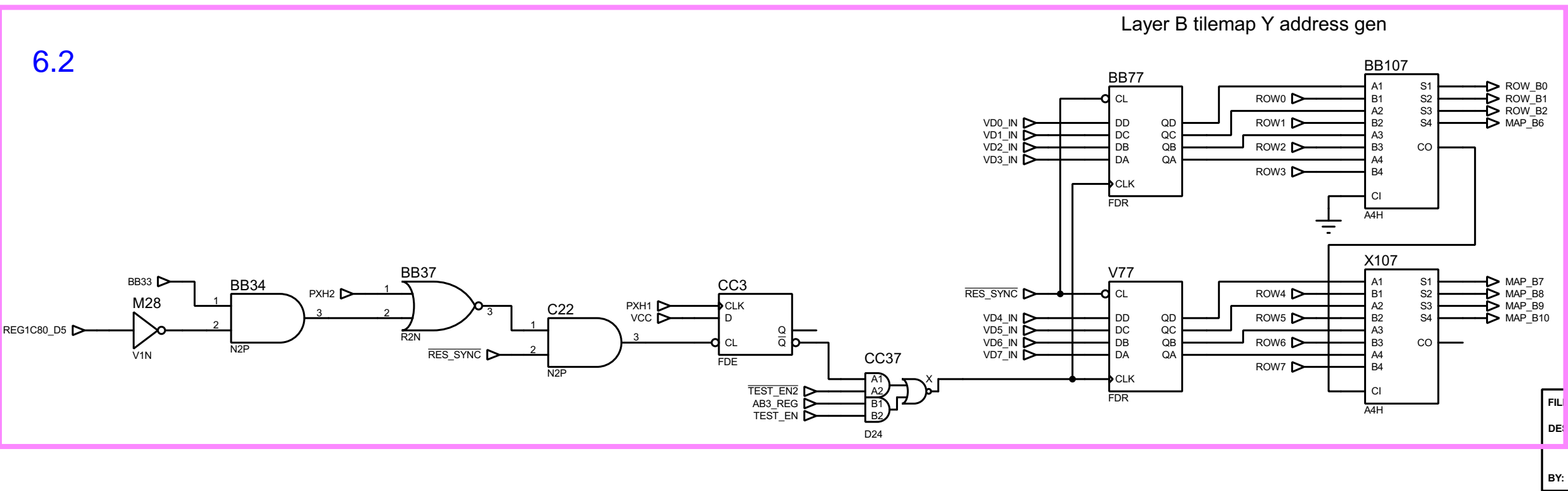
5.6 ✓



6.1



6.2



The diagram illustrates the internal logic of the GFX ROM bank for CPU testing. It features a 4-to-1 multiplexer (E77) that selects between four 8-bit ROM banks (DB3\_BUF, DB2\_BUF, DB1\_BUF, DB0\_BUF) based on the REG\_TE00\_WR signal. The selected data is then routed through various logic gates (AND, OR, NOT) and registers (REG1C00\_D5, REG1C00\_D6) to produce the final output signals (COL2, COL3). The diagram also shows the internal structure of the ROM banks, which are organized into four groups of four 8-bit words each, labeled B3, B19, B40, and B28. Each group is connected to a 4-to-1 multiplexer (A3, A9, A2, A3) and a 4-to-1 multiplexer (B1, B2, B3, B3). The outputs of these multiplexers are then routed through various logic gates and registers to produce the final output signals.

## 7.2

### 7.3

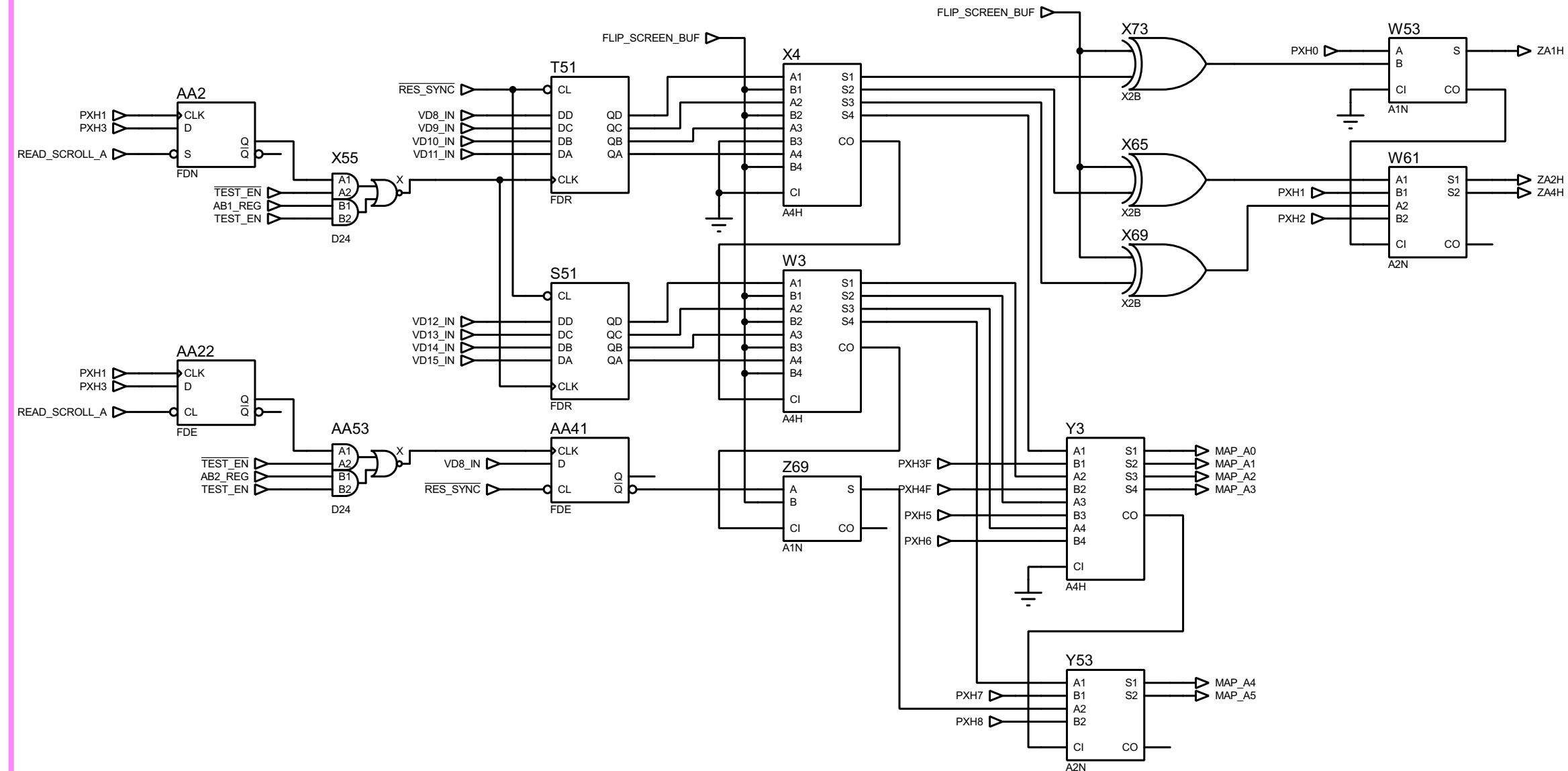
The diagram illustrates the logic for the GFX ROM bank during CPU testing. It features four 3-to-8 decoders (G77, H92, F77, and a group of four decoders G101, G106, G117, and G111) and four multiplexers (L140, L142, J150, J148). The decoders are connected to various inputs and outputs, including CLK, DA, DB, DC, DD, QA, QB, QC, QD, FDS, REG\_TERR\_WR, DB7\_BUF, DB6\_BUF, DB5\_BUF, DB4\_BUF, CL, FDR, and a common set of inputs (F128, G100, G133, F126). The outputs of the decoders are connected to a common set of outputs (A1, A2, S1, S2, S6, S5, S3, S4, B2, B1). The multiplexers are connected to the common set of outputs and output COL7, COL6, COL5, and COL4 respectively.

## 7.4

## 7.5

## 8.1

### Layer A tilemap X address gen



## 8.2

### Layer A tilemap Y address gen

