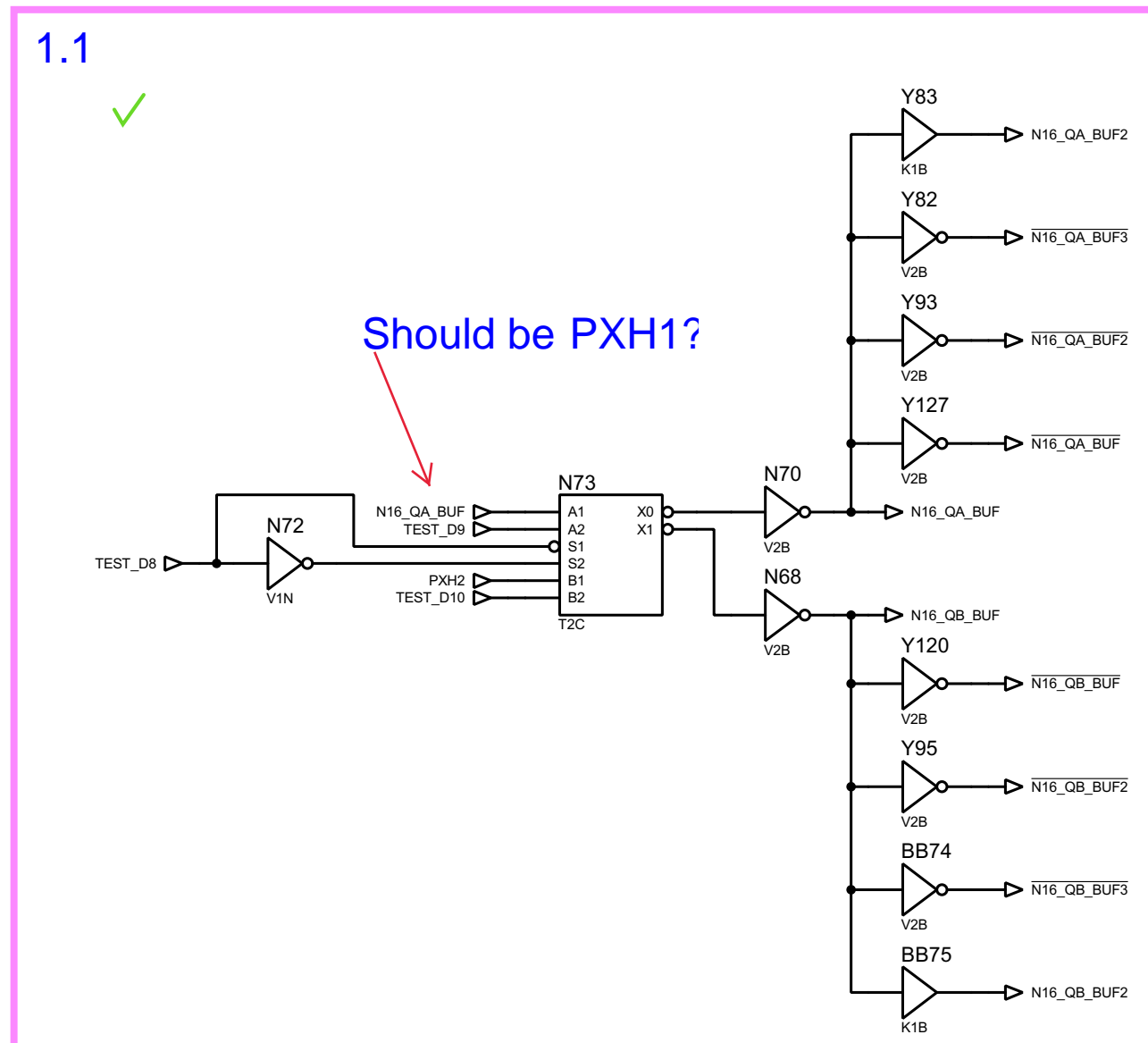


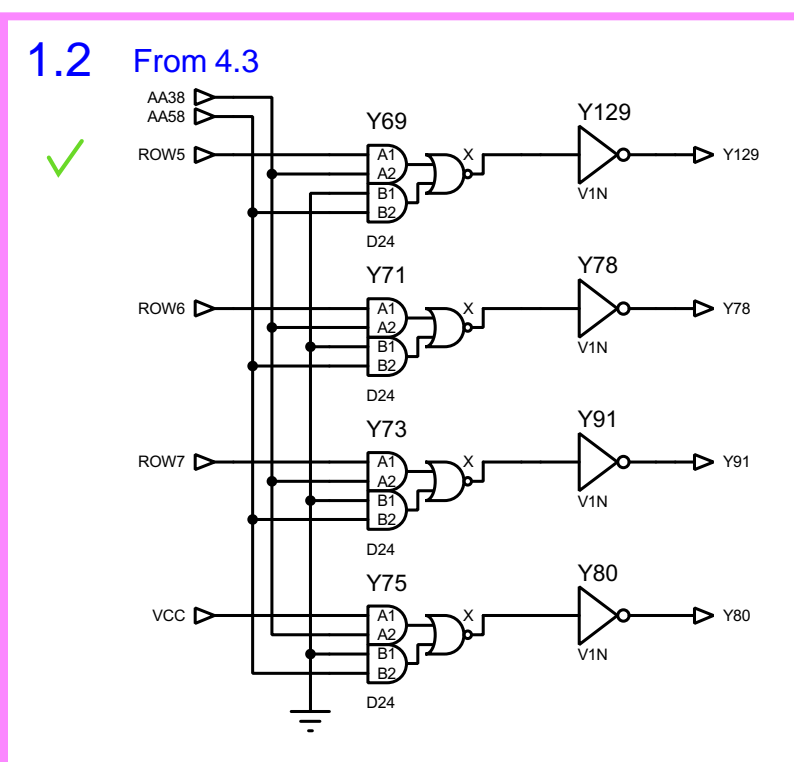
```

VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 01xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 110x xxxx xxxx A y scroll
0000 110x xxxx xxxx B y scroll
0000 01xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 110x xxxx xxxx B y scroll
0001 110x xxxx xxxx B x scroll
0001 1101 x xxxx x Tilemaps X
          xxx x Tilemaps Y

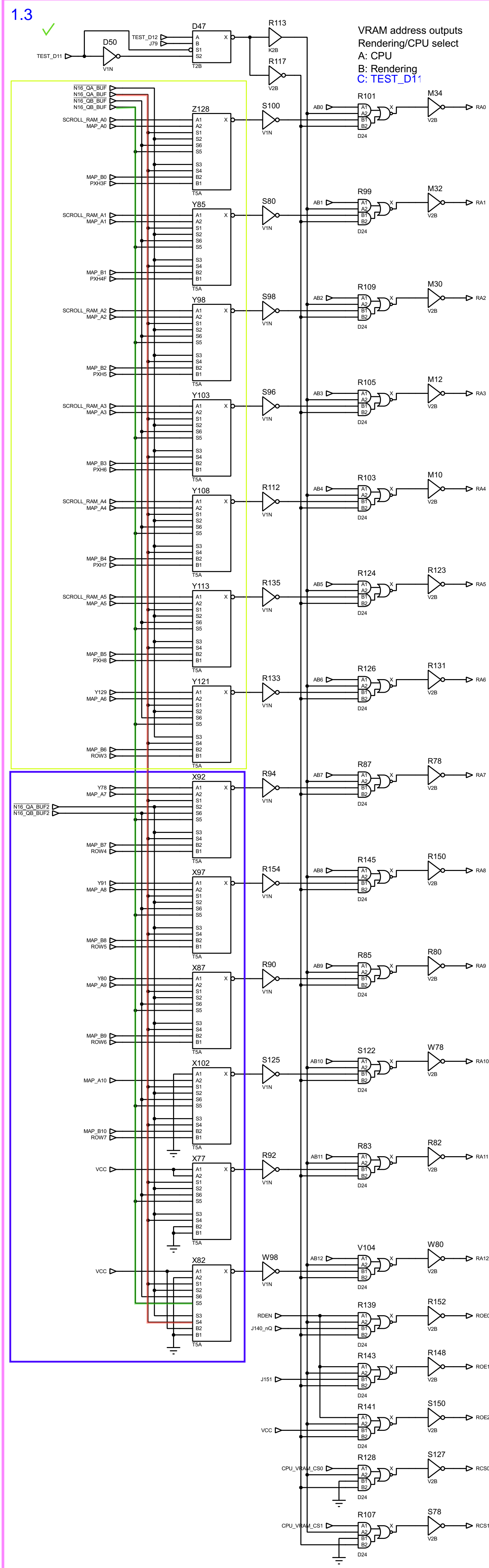
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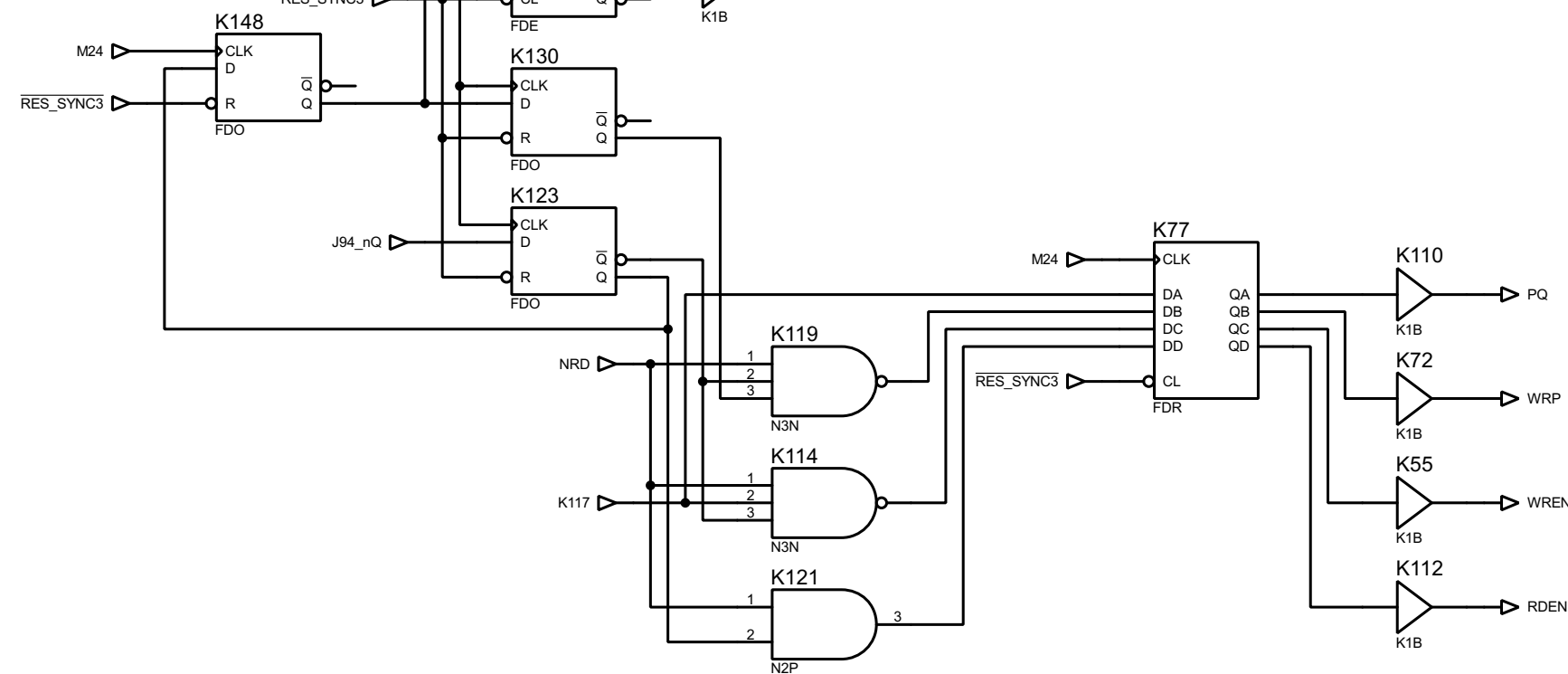
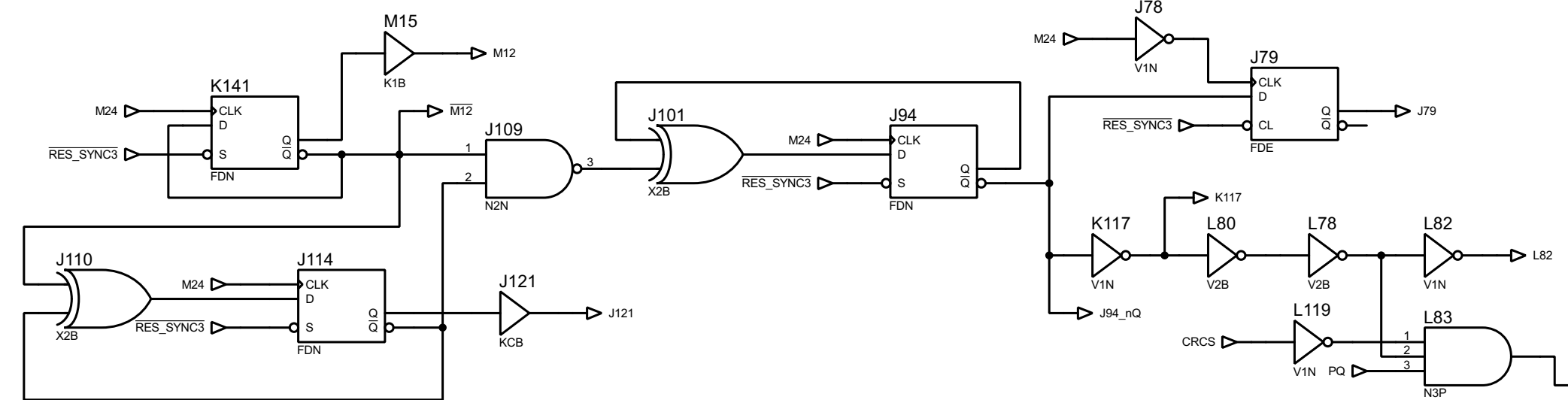


TEST_D13 Addresses Selector



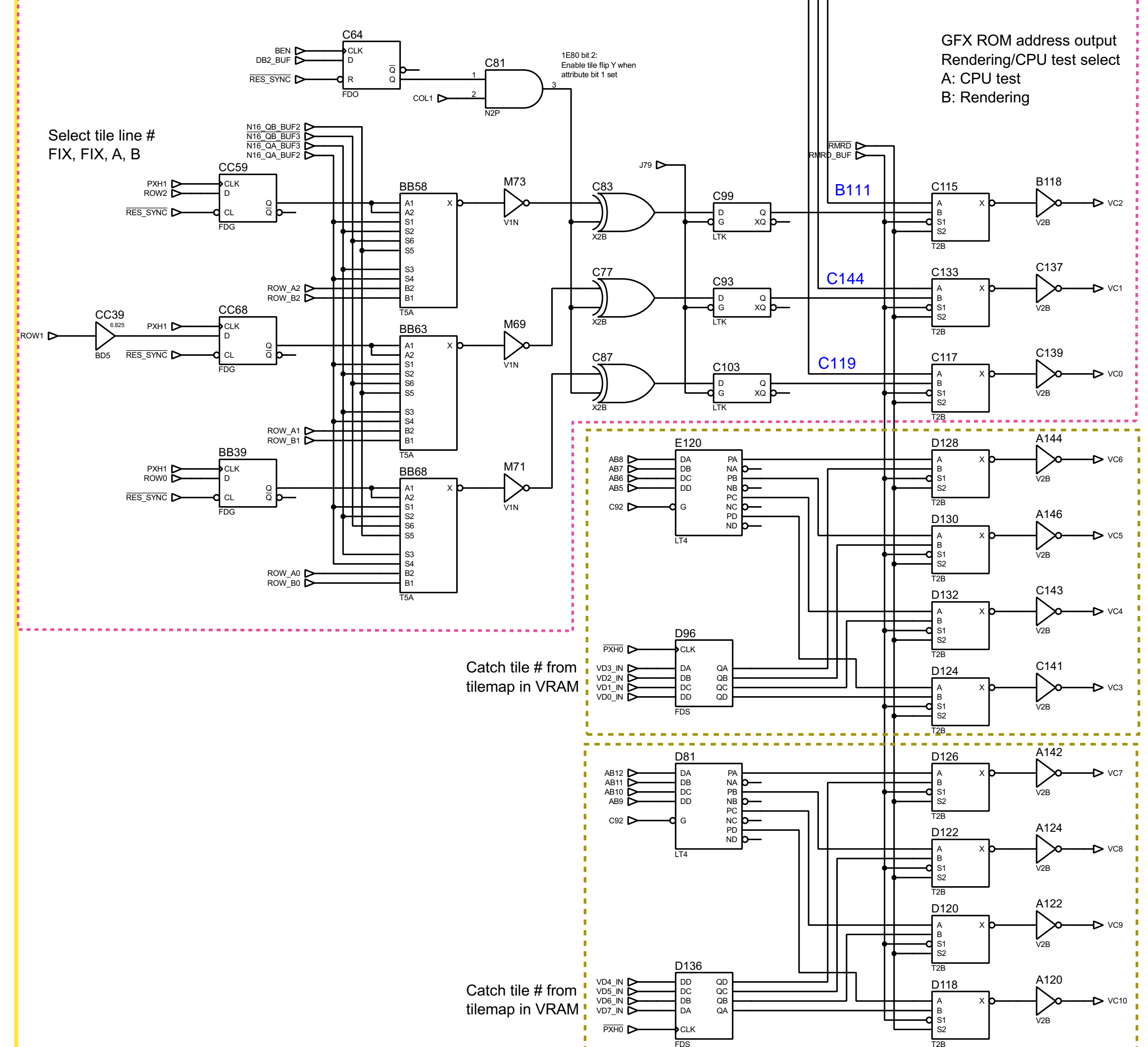
Selection can be simplified using AA38 (and AA38n) only, AA58 always selects 1'b0.





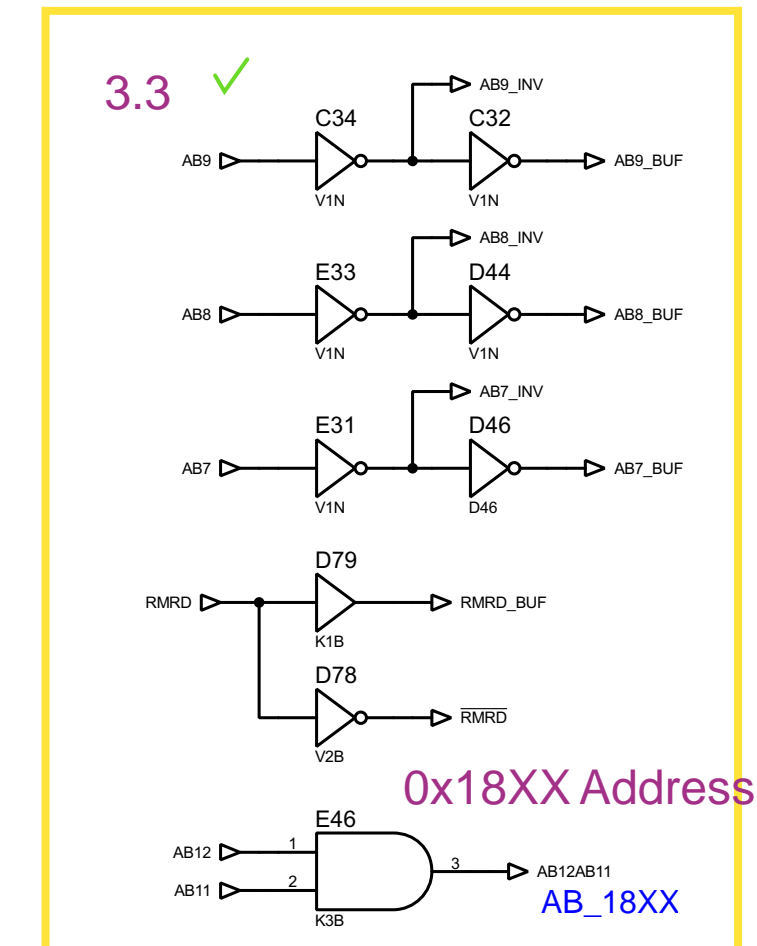
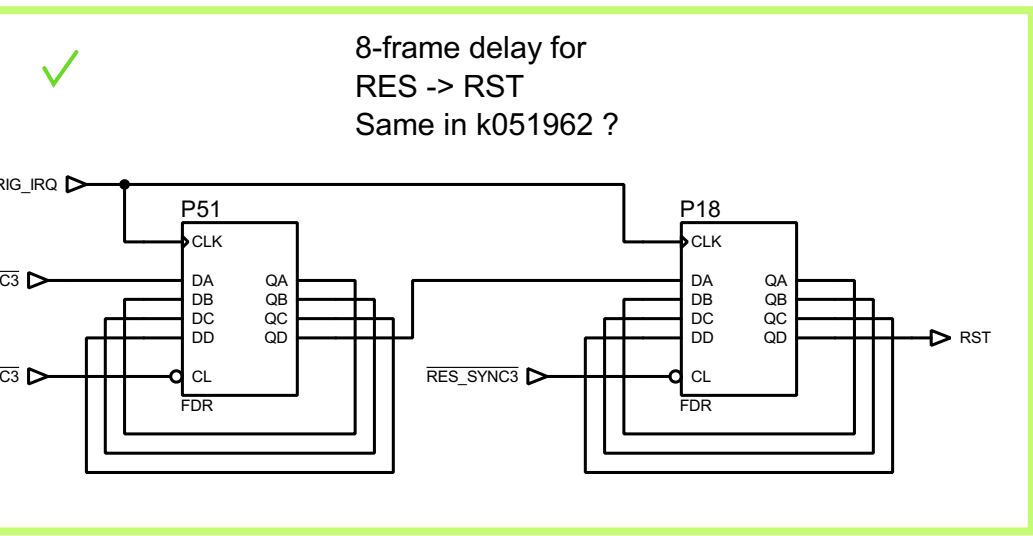
TIMING SIGNALS

SKIP because AB[1:0] used to select byte



3.1 ✓

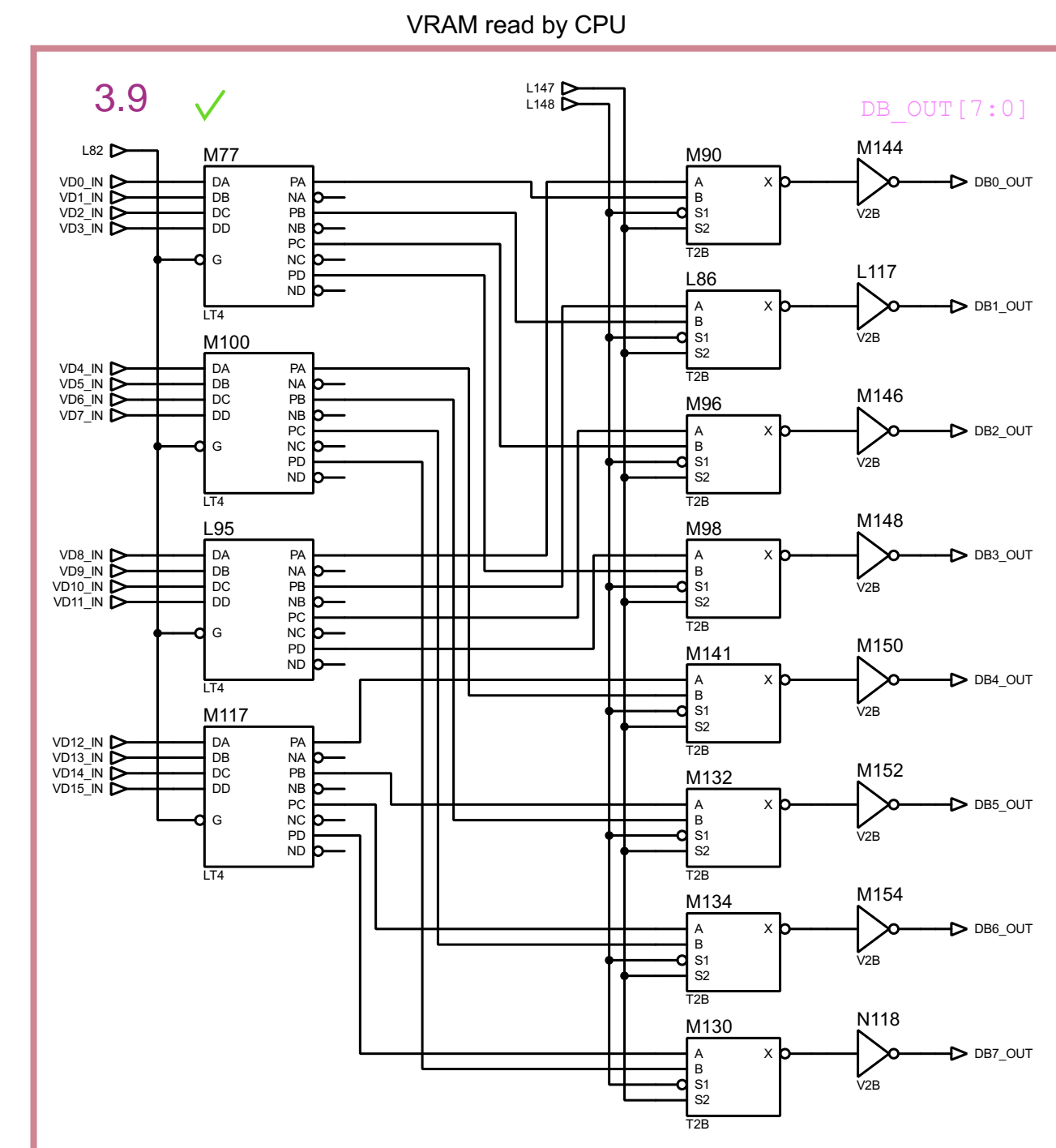
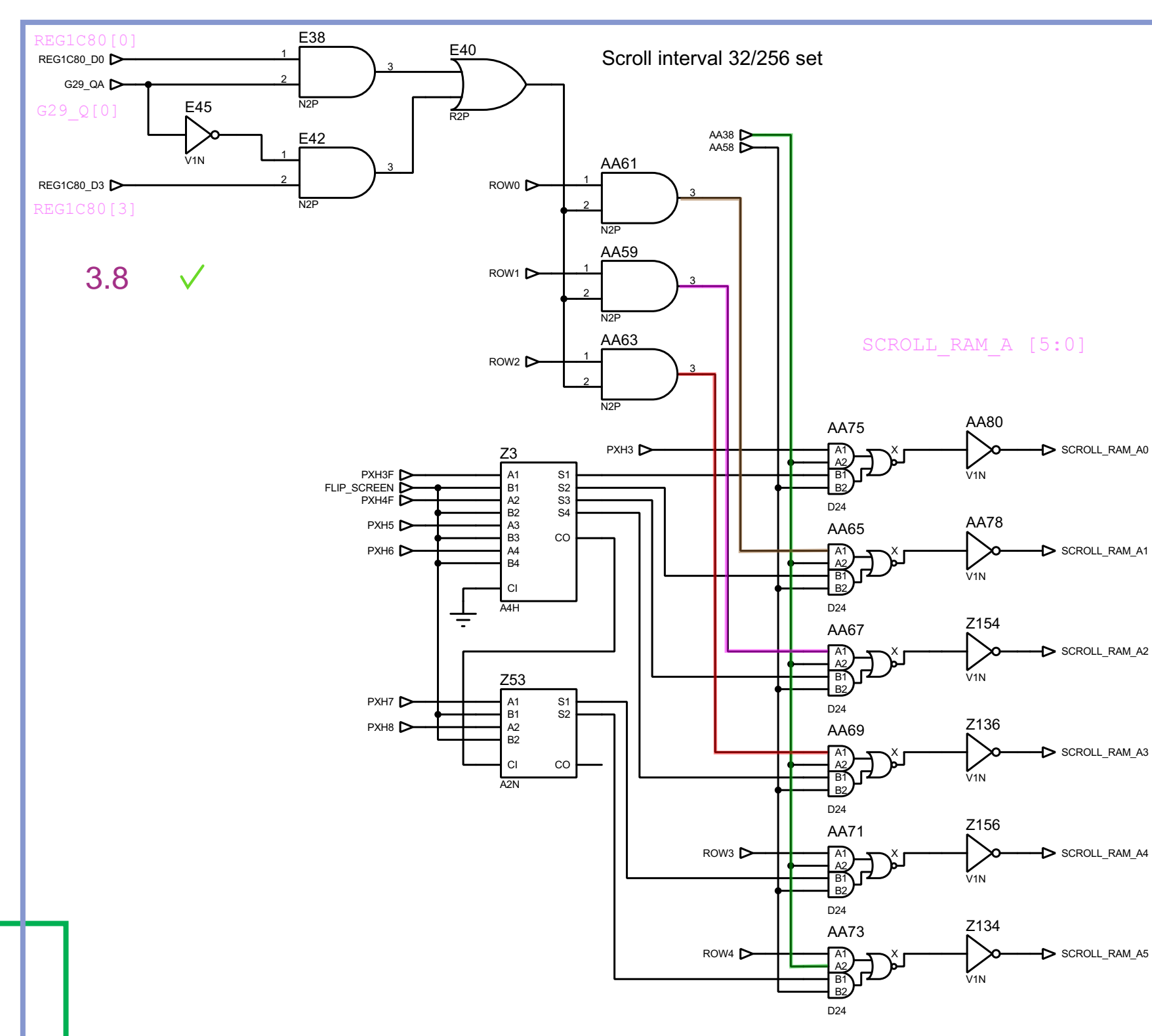
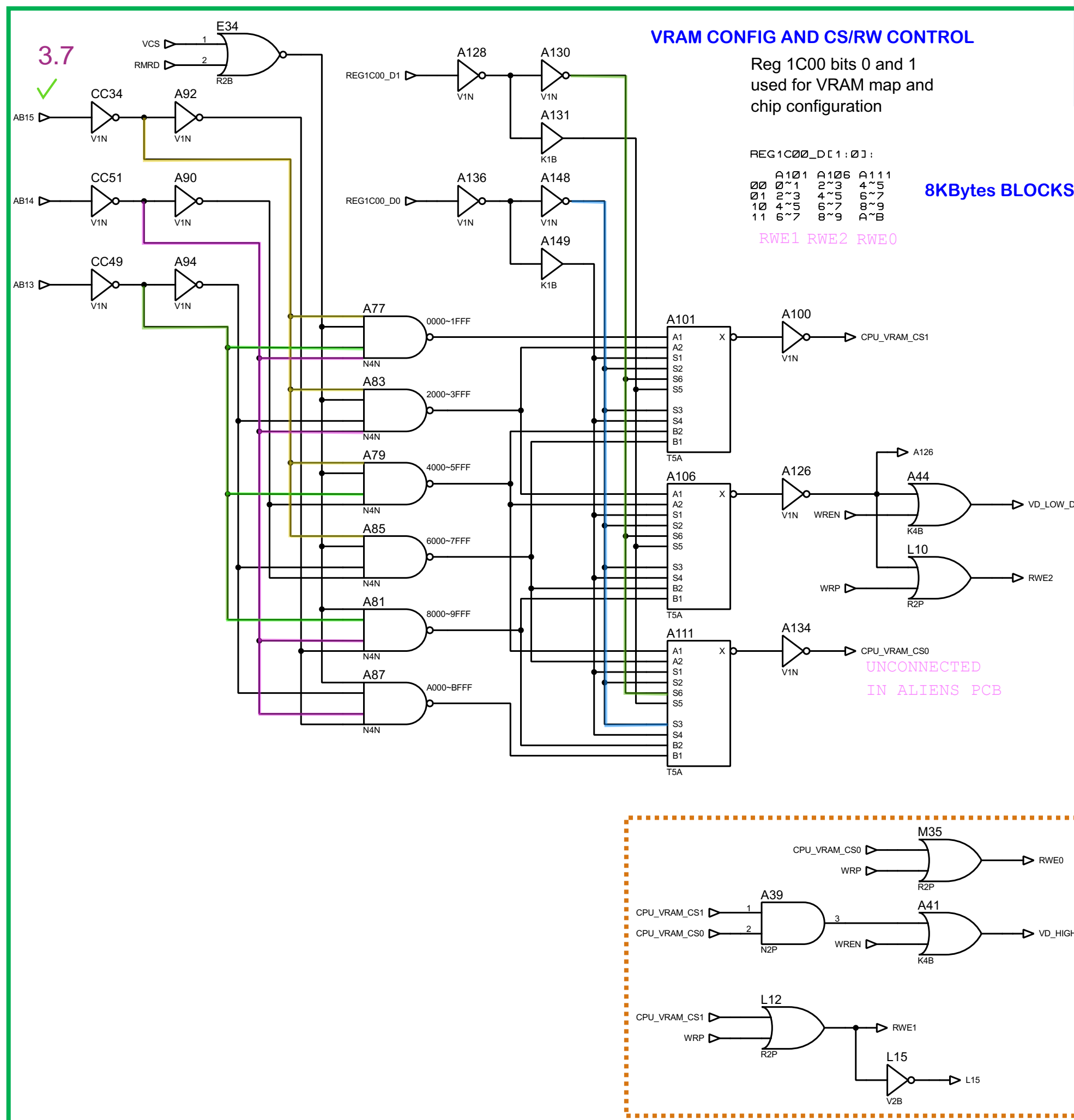
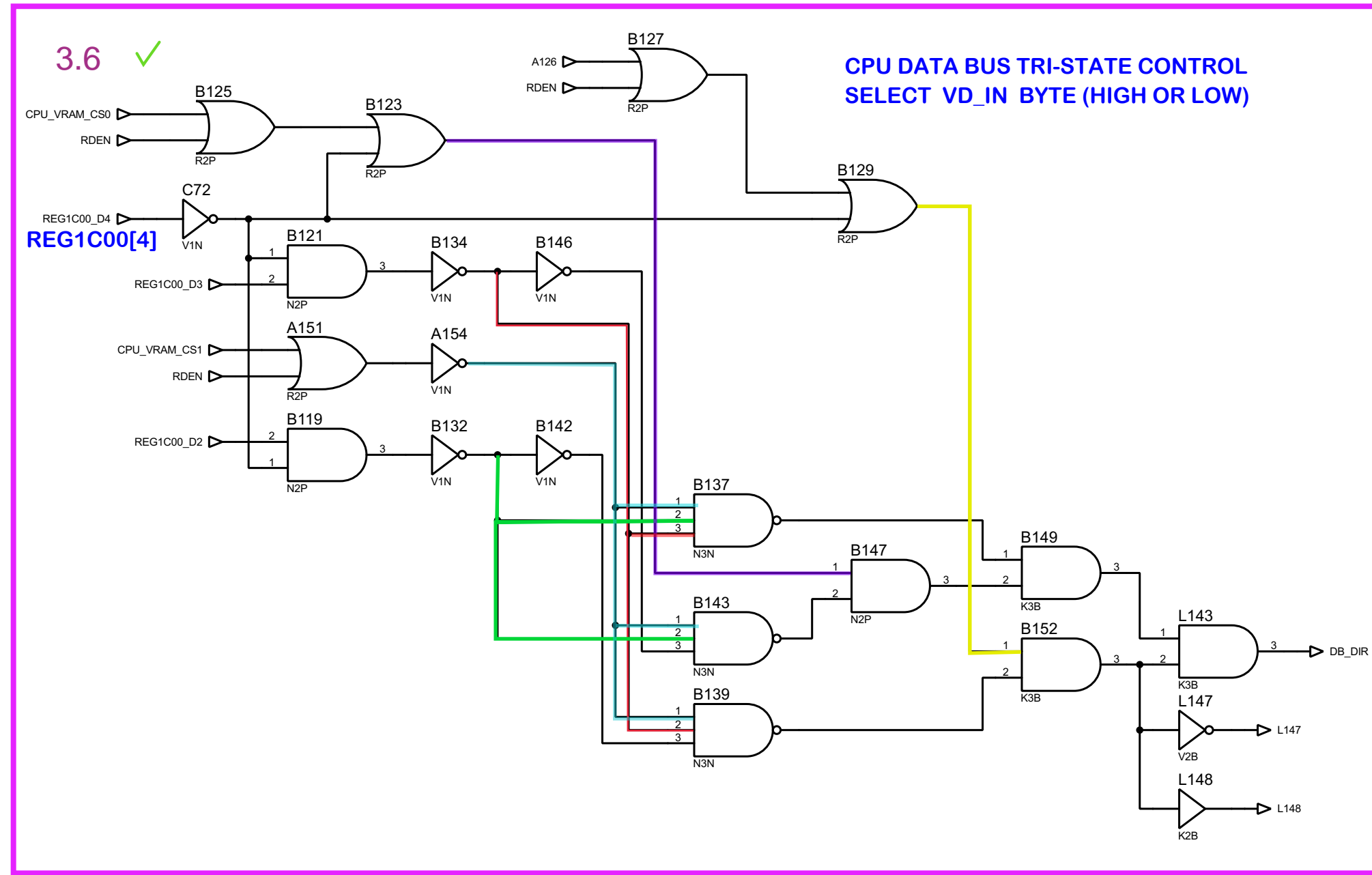
The diagram shows a circuit for a 3-bit counter. It consists of three main components: an N122 flip-flop, an M74 3-to-8 decoder, and an H12 3-input OR gate. The N122 flip-flop has inputs M04 (CLK), V02 (D), and RES (CL), and outputs Q and FDE. The M74 decoder has a 3-bit input (Q, Q-bar, and FDE) and eight outputs, one of which is RES_SYNC3. The H12 OR gate has three inputs (Q, Q-bar, and FDE) and two outputs, RES_SYNC and RES_SYNC2.



3.4 ✓

The diagram illustrates a set of 8 input buffers (DB0_IN to DB7_IN) connected to 8 output buffers (DB0_BUF to DB7_BUF) via inverters (N135, N80, N132, N77, N83, N97, N100, N103). Each inverter is labeled K2B.

```
wire [7:0] DB_BUF
```



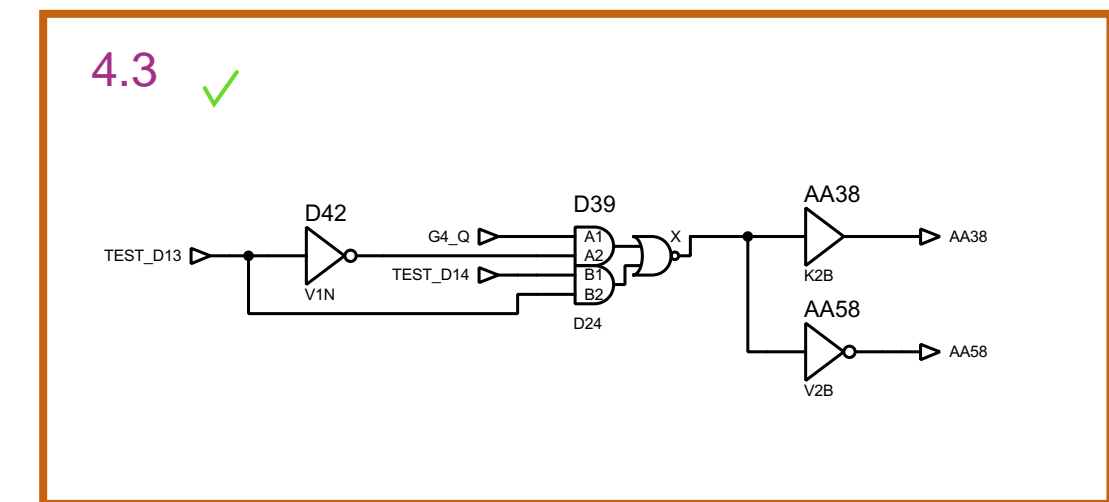
4.2 ✓

From Pg. 5 Reg 1E80

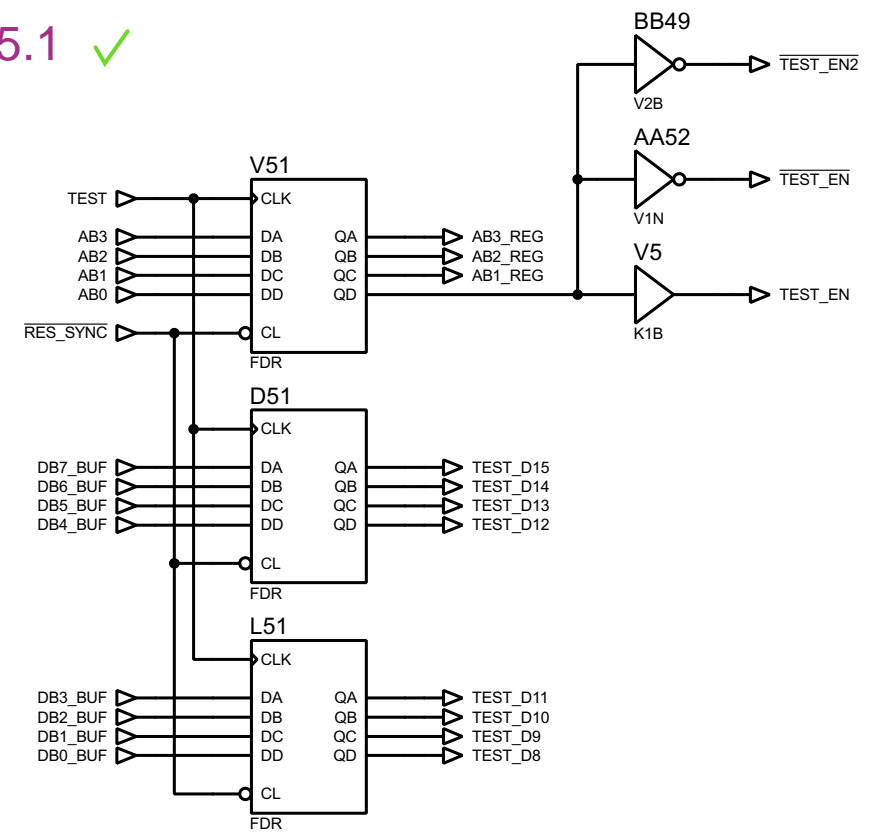
FLIP_SCREEN inverts the value of ROW[7:0] selectors

ROW[7:0]

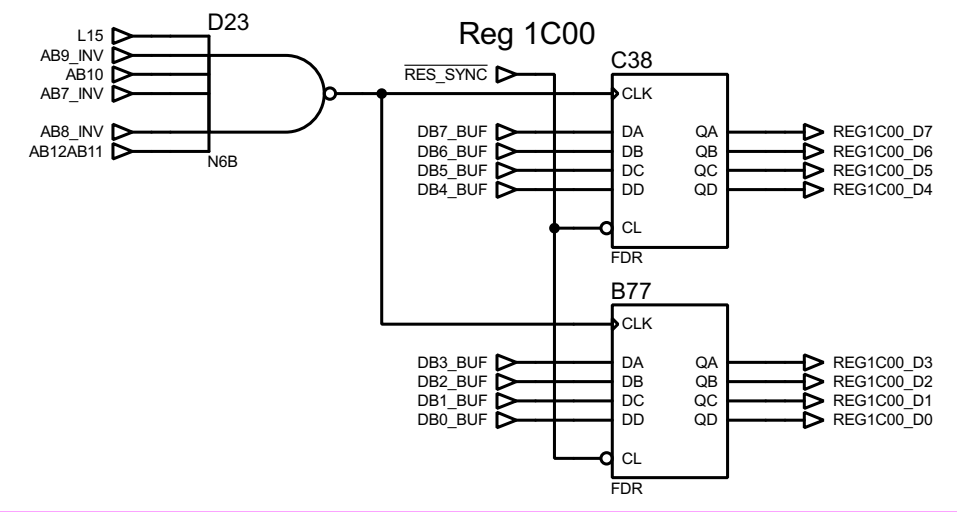
The diagram illustrates the logic for generating row selectors (ROW0-ROW7) based on the input LINE_END and RES_SYNC2. The circuit uses a D flip-flop (G20) to store the state of RES_SYNC2. The output of the flip-flop is connected to the clock of a 4-bit counter (J29) and the clock of a 4-bit counter (H29). The counter outputs are connected to the row selectors (ROW0-ROW7) via a series of OR gates (R58, R25, AA18, R29, R33, K74, R73, R69, R65). The circuit also includes a 4-bit counter (J29) and a 4-bit counter (H29) to generate the row selectors. The output of the counter is connected to the row selectors (ROW0-ROW7) via a series of OR gates (R58, R25, AA18, R29, R33, K74, R73, R69, R65). The circuit also includes a 4-bit counter (J29) and a 4-bit counter (H29) to generate the row selectors. The output of the counter is connected to the row selectors (ROW0-ROW7) via a series of OR gates (R58, R25, AA18, R29, R33, K74, R73, R69, R65).



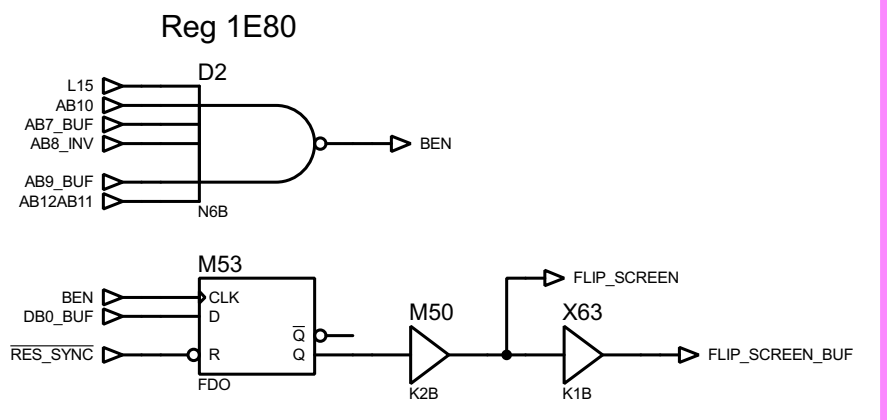
5.1 ✓



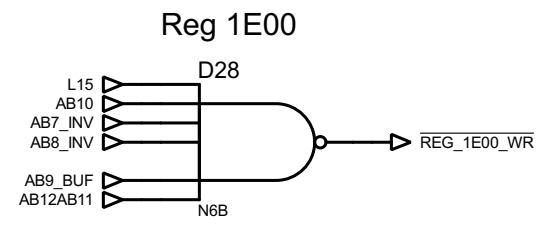
5.4 ✓



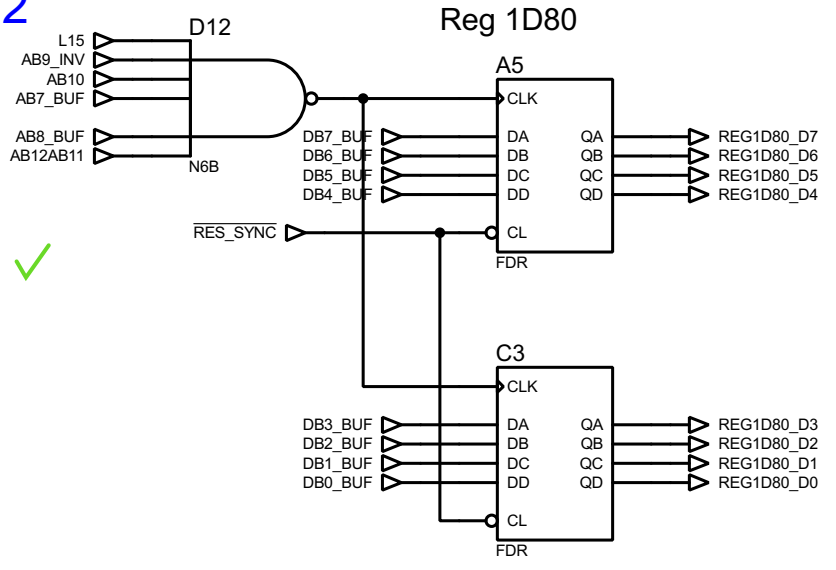
5.7 ✓



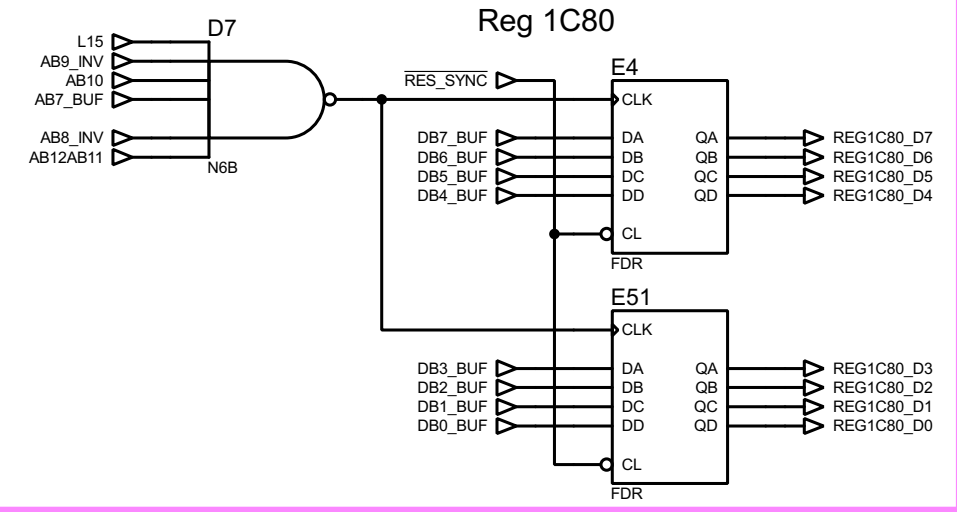
5.8 ✓



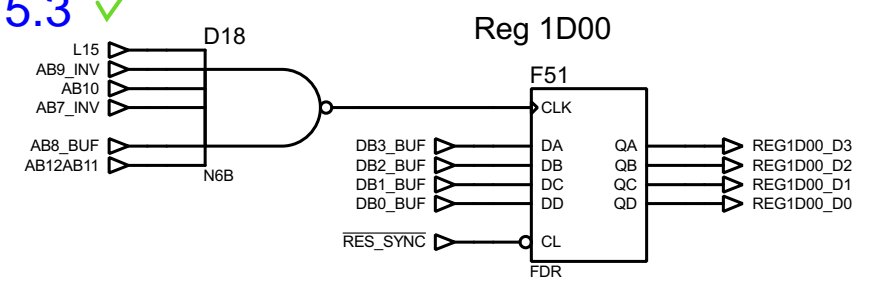
5.2 ✓



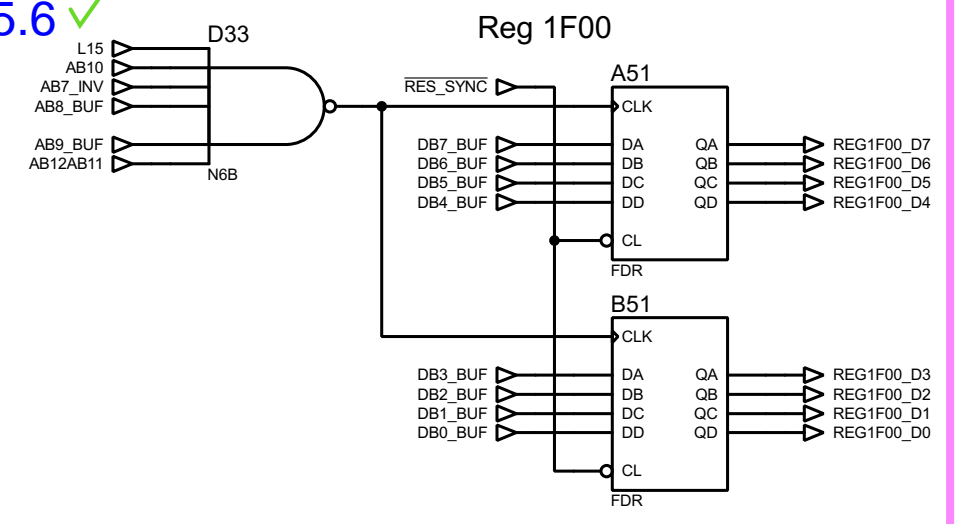
5.5 ✓



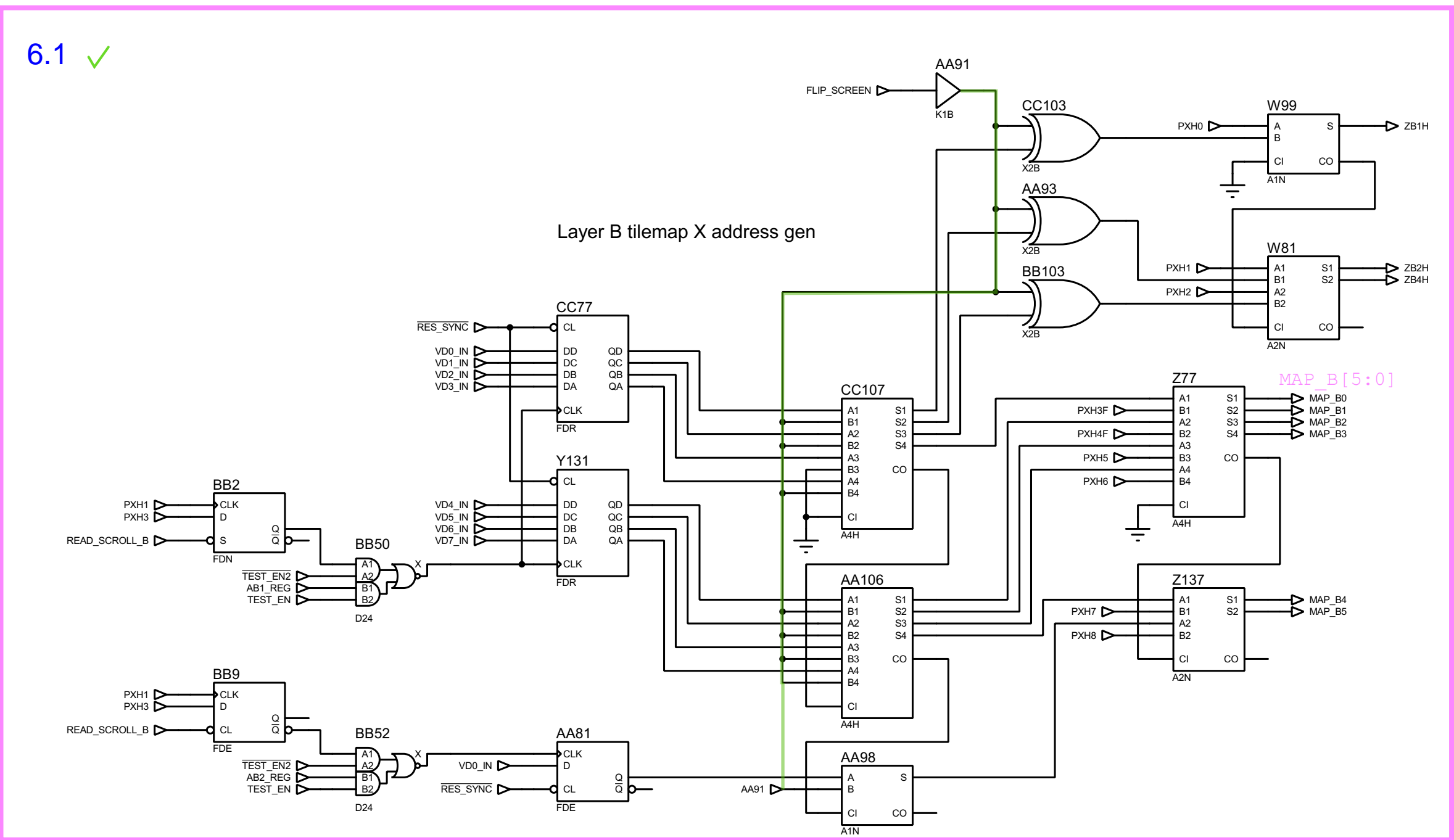
5.3 ✓



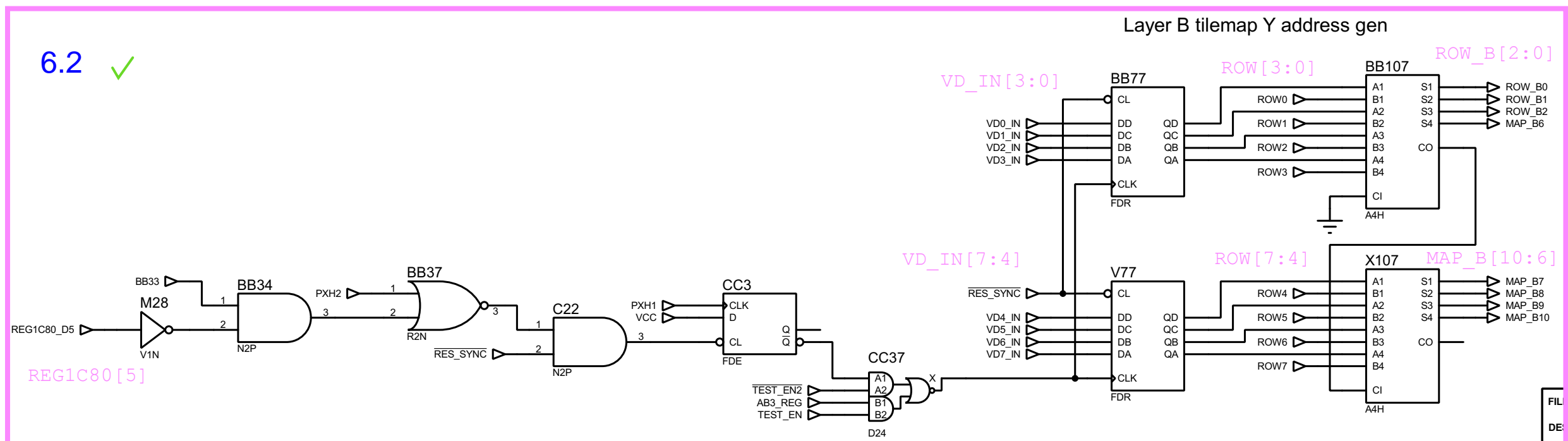
5.6 ✓



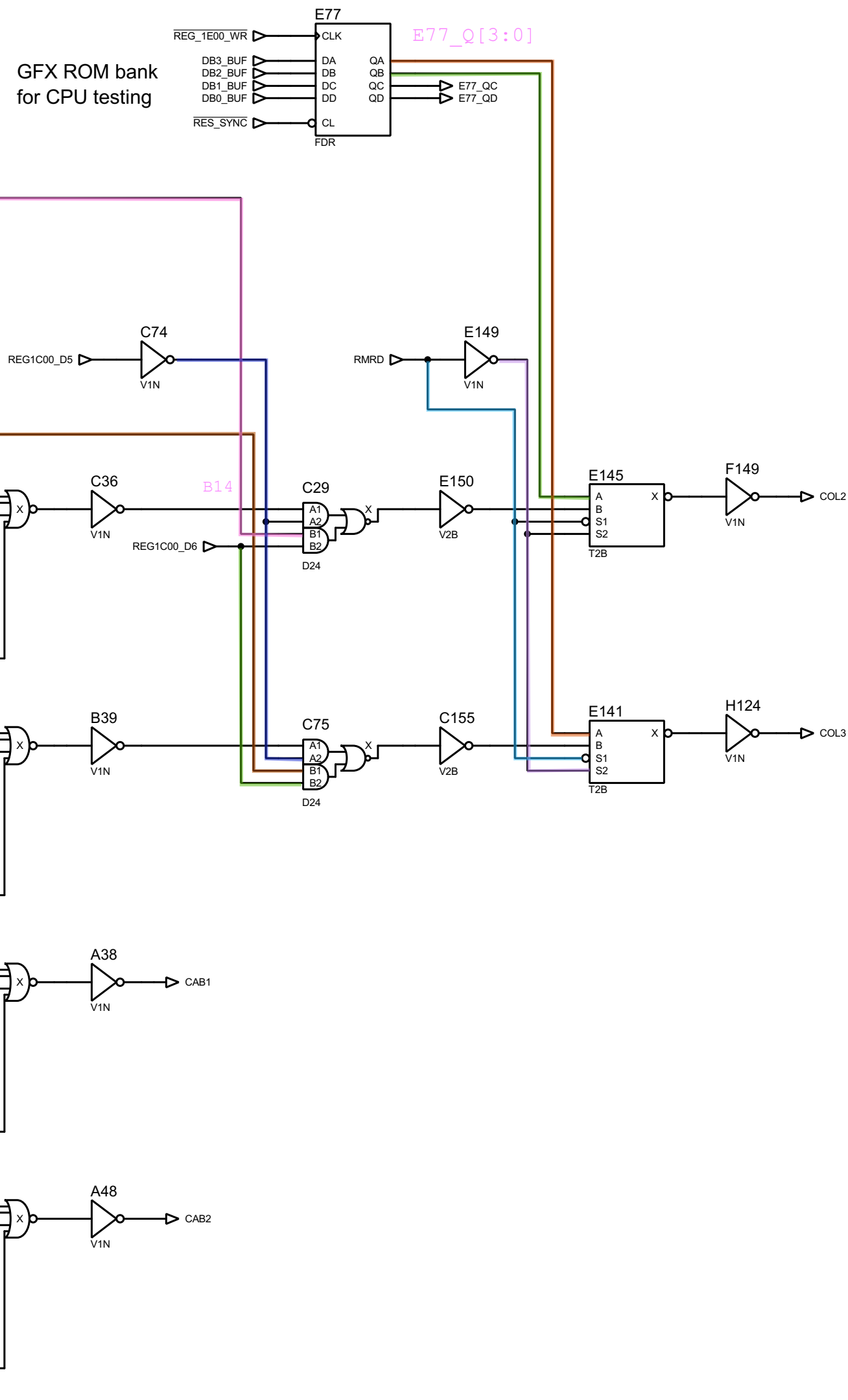
6.1 ✓



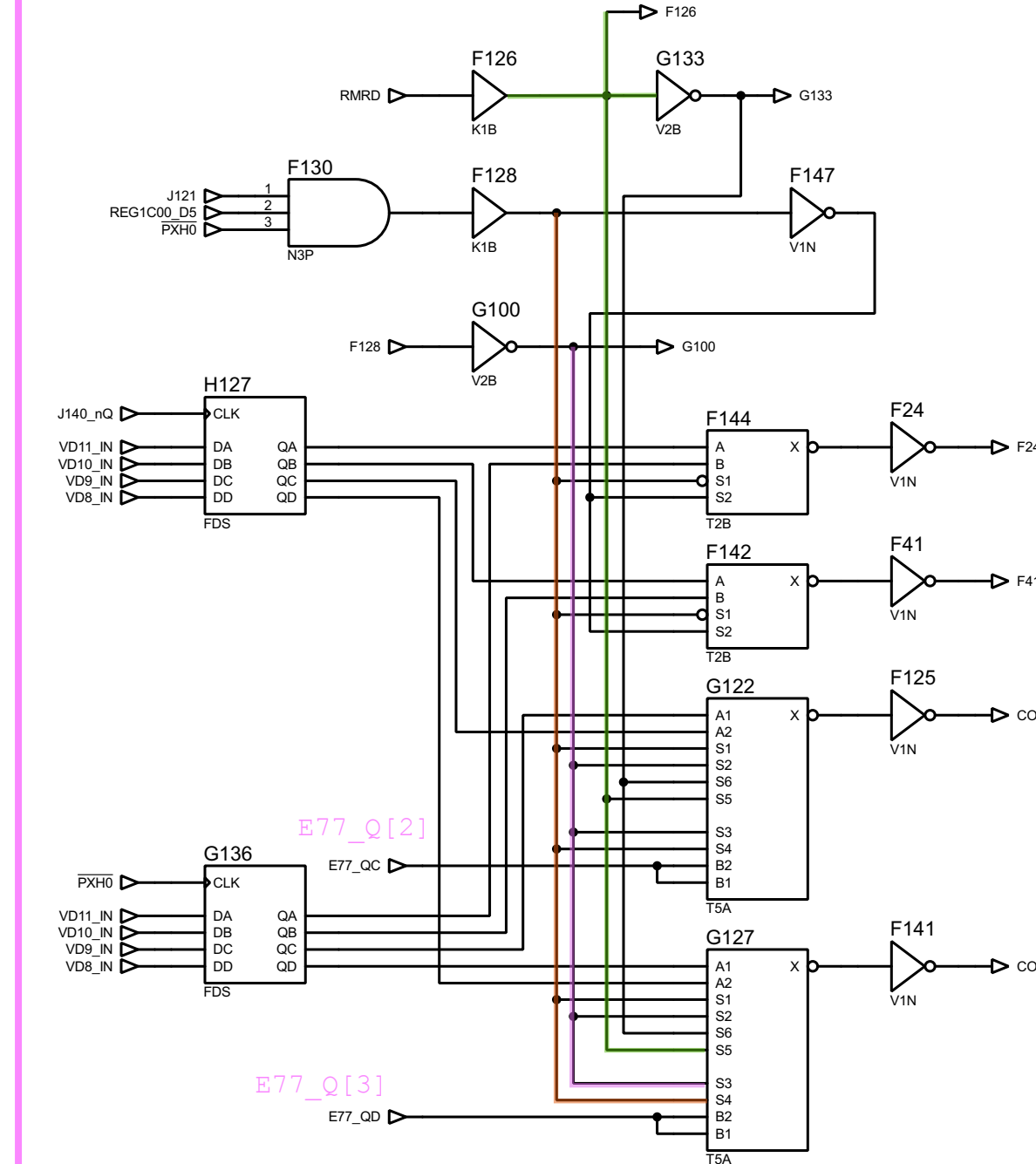
6.2 ✓



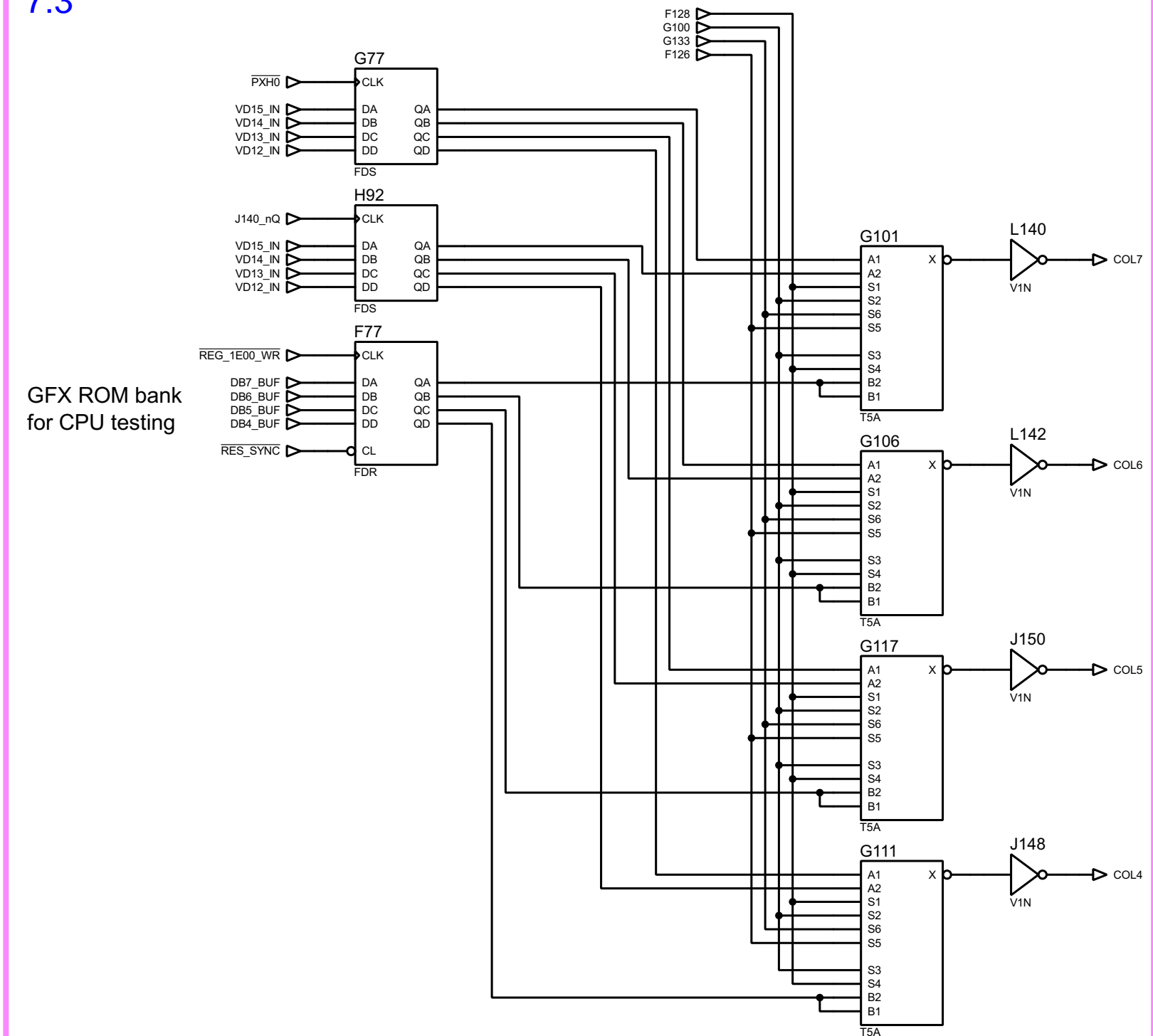
7.2



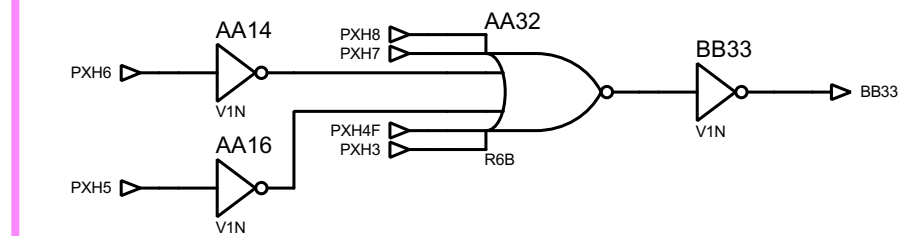
7.1



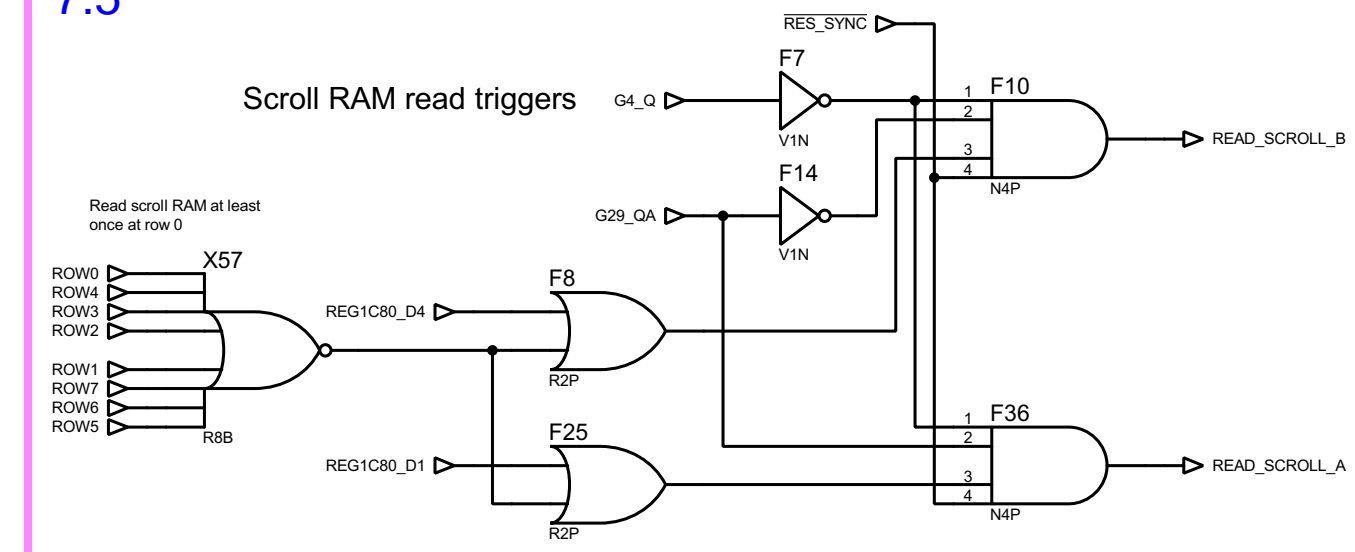
7.3



7.4

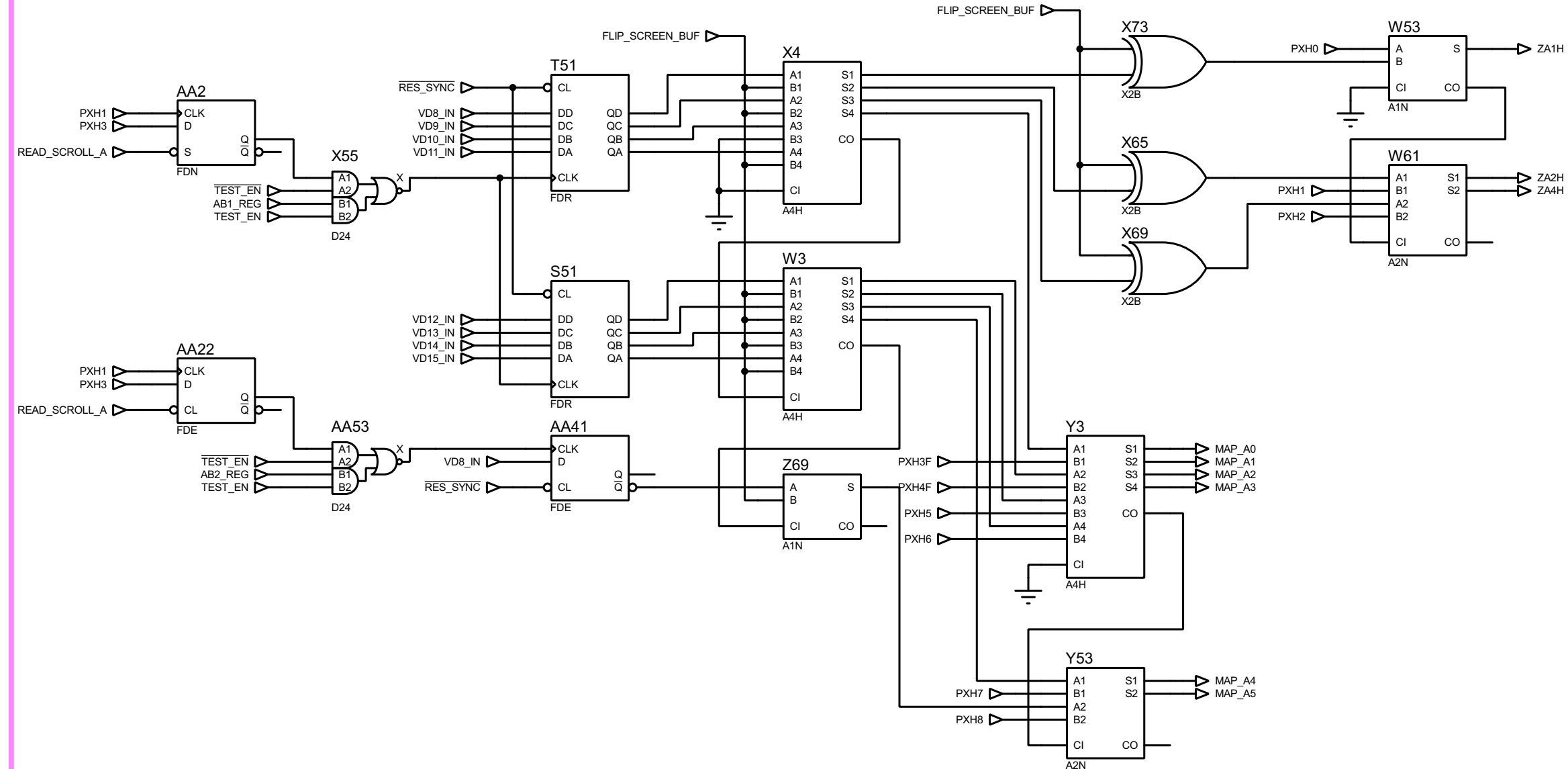


7.5



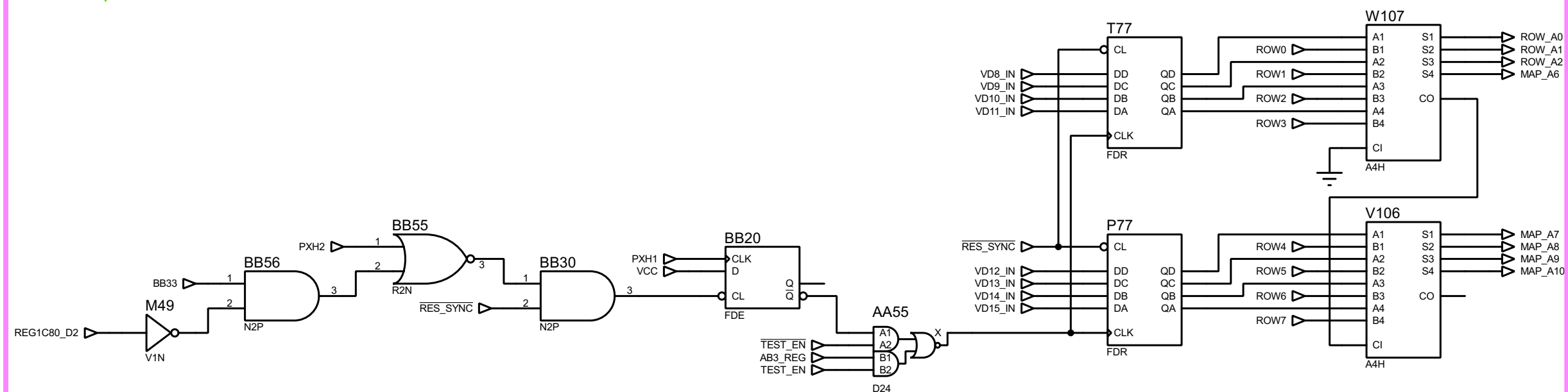
8.1 ✓

Layer A tilemap X address gen



8.2 ✓

Layer A tilemap Y address gen



FILE NAME: k052109.pdsprj

DESIGN TITLE: Konami 052109
LAYER A SCROLL

BY: Sean Gonsalves

REV: A

DATE:

22/06/2021

PAGE:

8 of 8