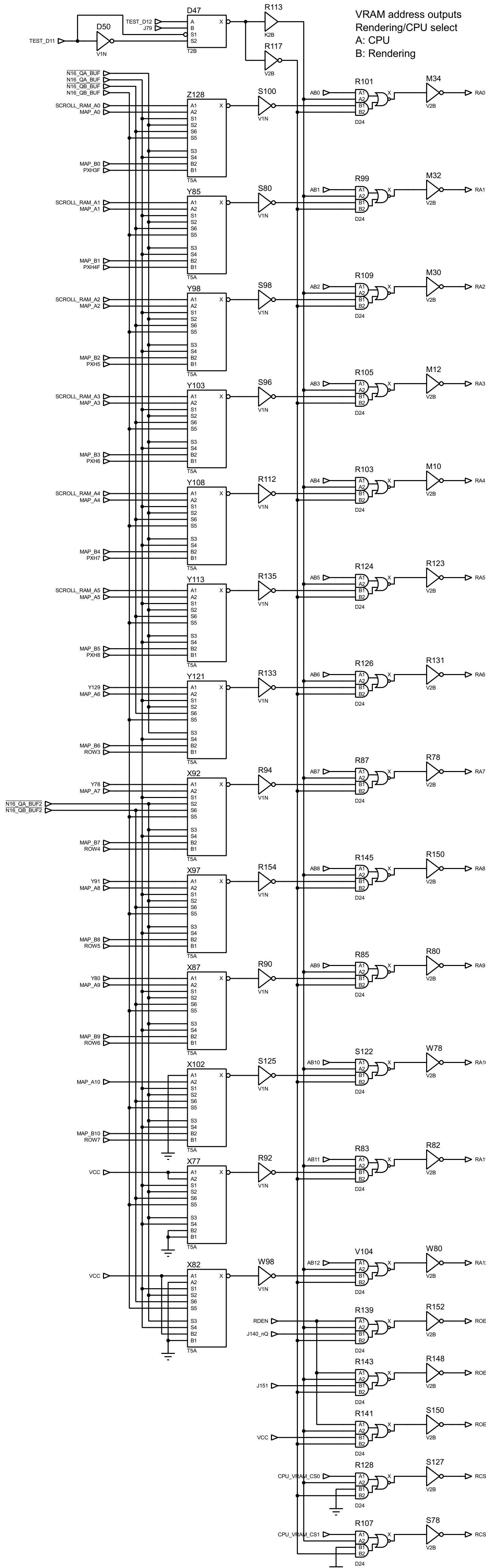
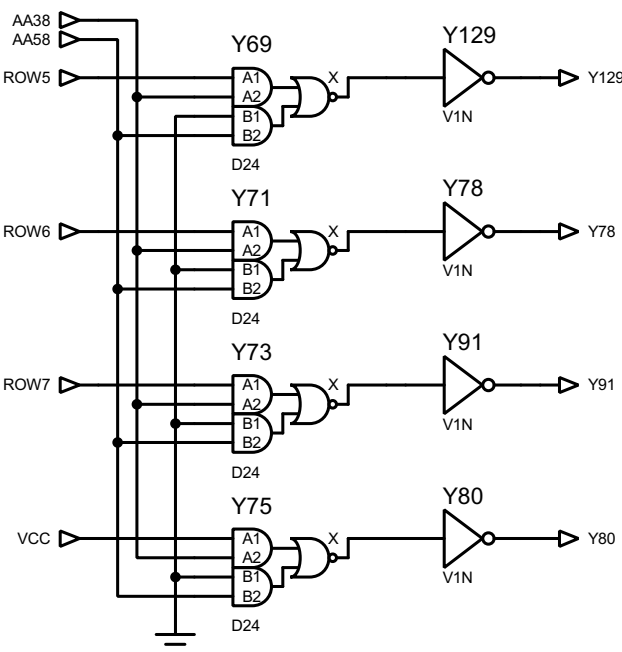
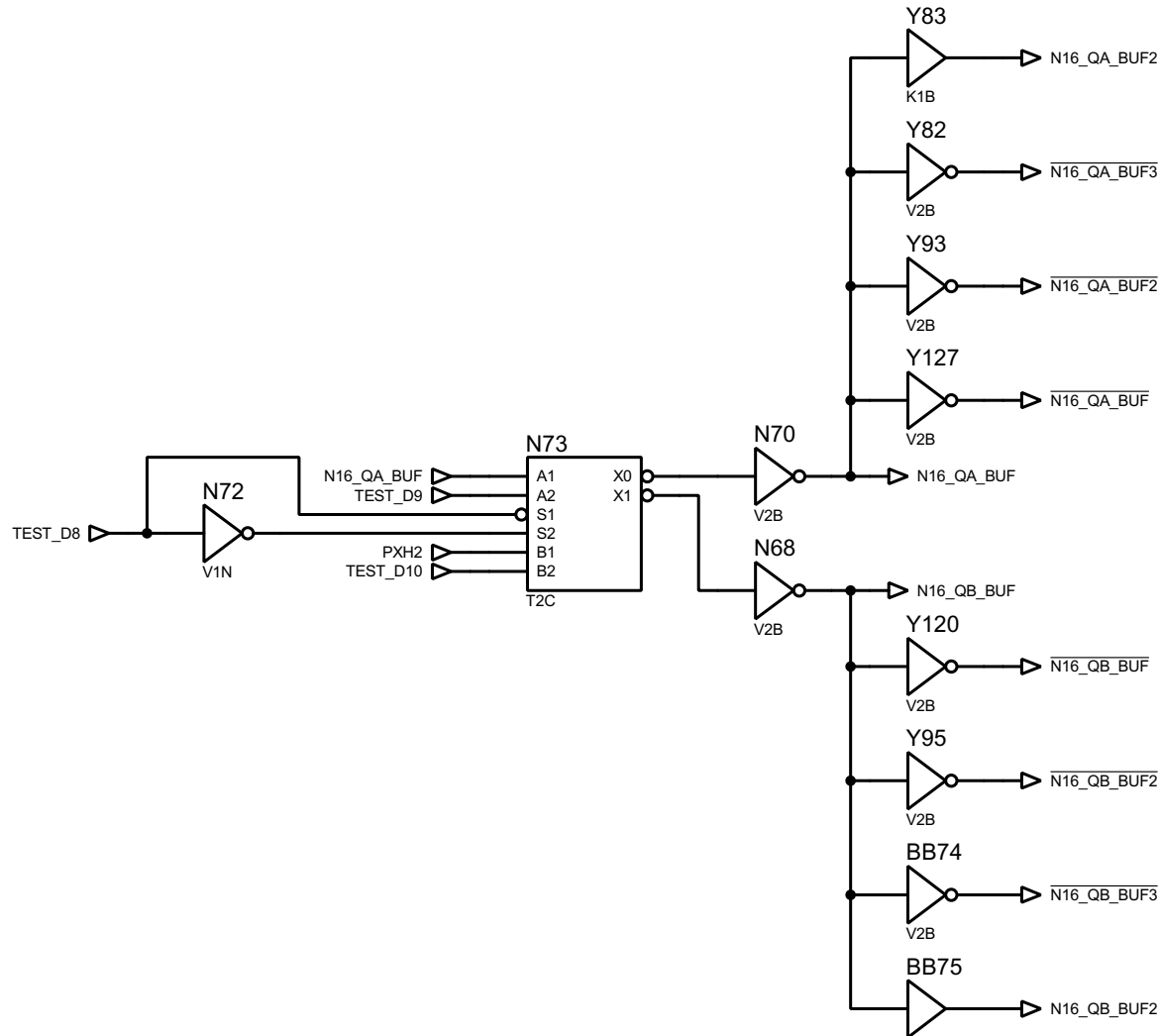
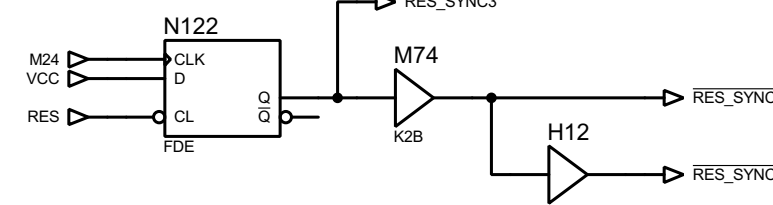


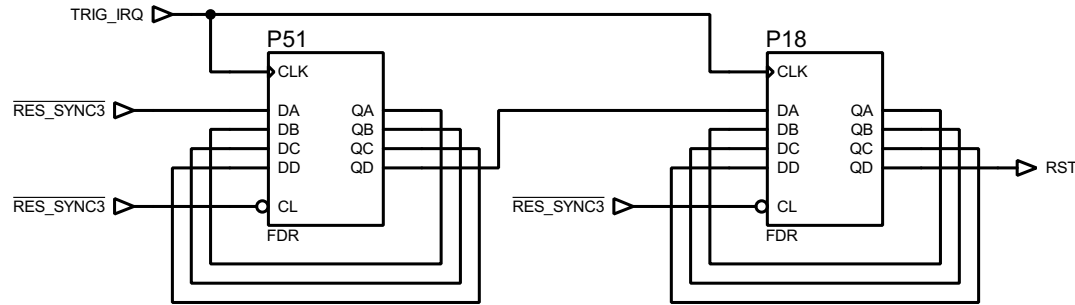
VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 00xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 1100 xxxx xxxx A Y scroll
0000 1101 xxxx xxxx A X scroll
0001 00xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 1100 xxxx xxxx B Y scroll
0001 1101 xxxx xxxx B X scroll
0001 1111 xxxx xxxx B tilemaps X
0001 1110 xxxx xxxx B tilemaps Y
xx xxx tilemaps Y



3.1



8-frame delay for
RES -> RST
Same in k051962 ?



The schematic diagram illustrates the input logic for the 8051 microcontroller. It features four input buffers (AB9_BUF, AB8_BUF, AB7_BUF, RMRD_BUF) and their associated logic components. AB9_BUF is connected to AB9 through a buffer V1N. AB8_BUF is connected to AB8 through a buffer V1N, with an additional input from AB8_INV through a buffer D44. AB7_BUF is connected to AB7 through a buffer V1N, with an additional input from AB7_INV through a buffer D46. RMRD_BUF is connected to RMRD through a buffer D79, with an additional input from RMRD through a buffer D78.

180c-1833: Layer A Y Scroll

```

graph LR
    DB0_IN --> N80[N80]
    N80 -- k2B --> DB0_BUF
    DB1_IN --> N132[N132]
    N132 -- k2B --> DB1_BUF
    DB2_IN --> N77[N77]
    N77 -- k2B --> DB2_BUF
    DB3_IN --> N83[N83]
    N83 -- k2B --> DB3_BUF
    DB4_IN --> N97[N97]
    N97 -- k2B --> DB5_BUF
    DB5_IN --> N100[N100]
    N100 -- k2B --> DB6_BUF
    DB6_IN --> N103[N103]
    N103 -- k2B --> DB7_BUF

```

[illegible]

3.6

The logic diagram for the 3.6 testbench is a complex circuit involving several logic gates and flip-flops. The inputs include CPU_VRAM_CS0, RDEN, REG1C00_D4, REG1C00_D3, CPU_VRAM_CS1, RDEN, and REG1C00_D2. The circuit features a series of AND gates (B125, B123, B127, B129, B121, B134, B146, B151, B154, B119, B132, B142, B137, B143, B139, B147, B149, B152) and OR gates (A126, A151, A154, A129, A137, A143, A147, A148). The outputs include DB_DIR, L147, and L148. The circuit is designed to simulate the behavior of the 3.6 testbench, with various signals and components labeled throughout.

3.7

Reg 1C00 bits 0 and 1 used for VRAM map and chip configuration

| REG1C00_D0 | 0 | 1 |
|------------|-----|-----|
| 00 | 0~1 | 2~3 |
| 01 | 2~3 | 4~5 |
| 10 | 4~5 | 6~7 |
| 11 | 6~7 | 8~9 |

3.8

Logic diagram for the RWE0 signal:

- Gate M35 (3-input OR) has inputs CPU_VRAM_CS0, WRP, and R2P. Its output is RWE0.
- Gate A39 (3-input OR) has inputs CPU_VRAM_CS1 and CPU_VRAM_CS0. Its output is 1.
- Gate A41 (3-input OR) has inputs 3 and WREN. Its output is VD_HIGH_DIF.
- Gate L12 (3-input OR) has inputs CPU_VRAM_CS1 and WRP. Its output is R2P.
- Gate L15 (3-input OR) has inputs RWE1 and R2P. Its output is L15.
- A signal V2B is connected to the output of L15.

3.9

Scroll interval 32/256 set

REG1C80_D0

G29_OA

E38

E40

E42

V1N

REG1C80_D3

AA61

AA59

AA63

ROW0

ROW1

ROW2

Z3

S1

S2

S3

S4

CO

PXH3

PXH4

PXH5

PXH6

PXH7

PXH8

Z53

A1

B1

A2

B2

A3

B3

A4

B4

CI

A4H

A1

B1

A2

B2

CI

A2N

AA75

AA65

AA67

AA69

AA71

AA73

AA80

AA78

Z154

Z136

Z156

Z134

SCROLL_RAM_A0

SCROLL_RAM_A1

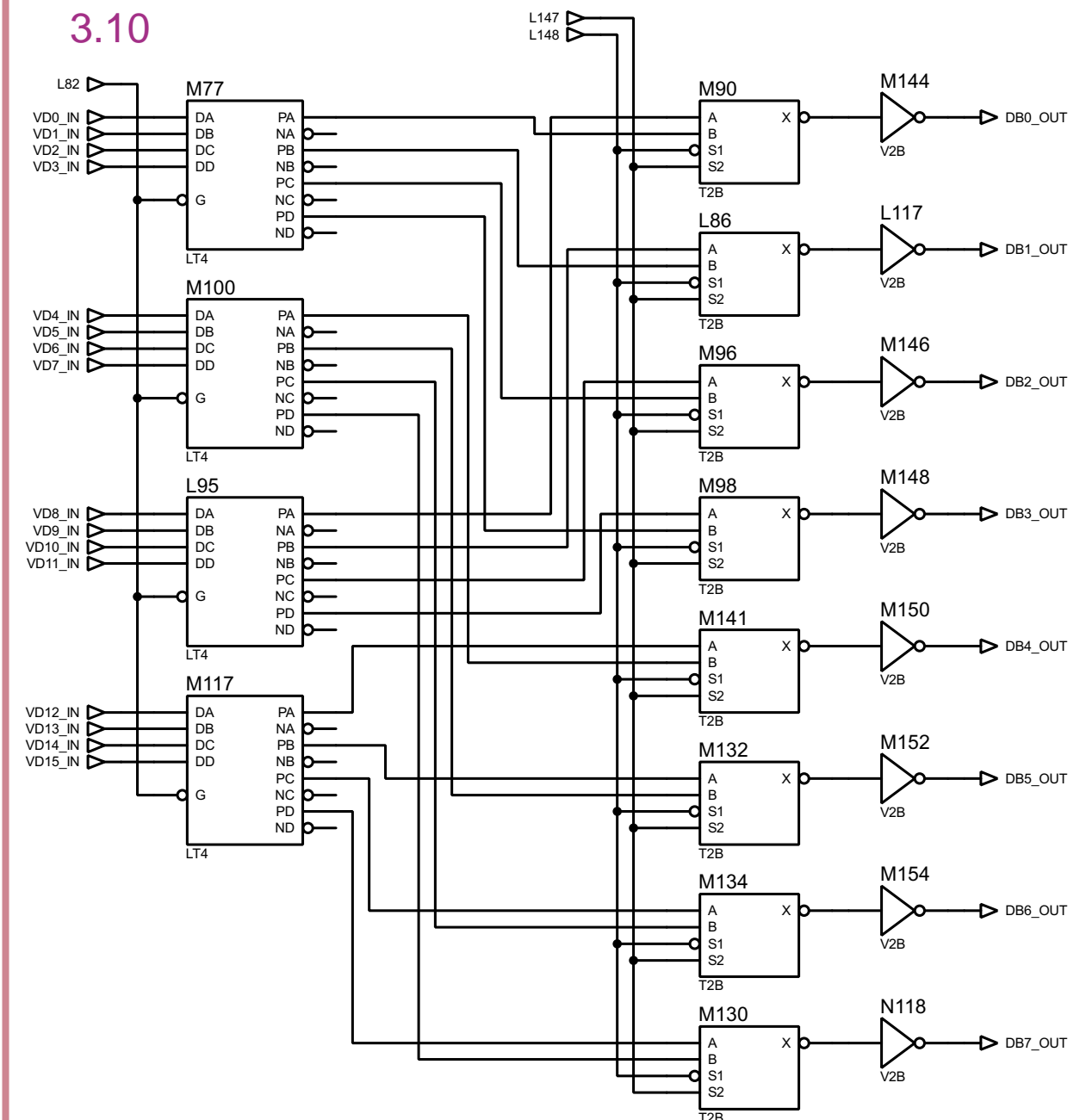
SCROLL_RAM_A2

SCROLL_RAM_A3

SCROLL_RAM_A4

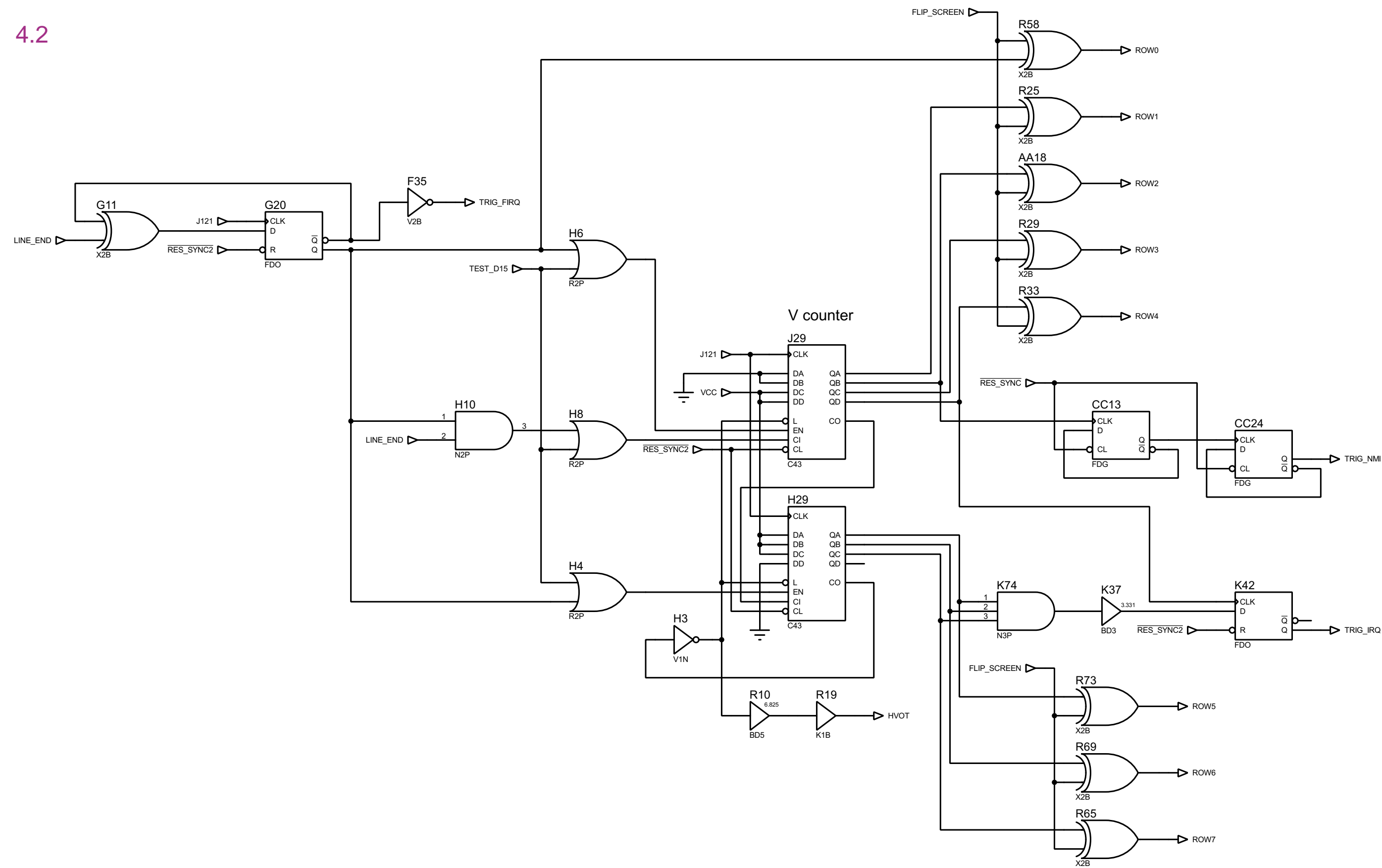
SCROLL_RAM_A5

3.10

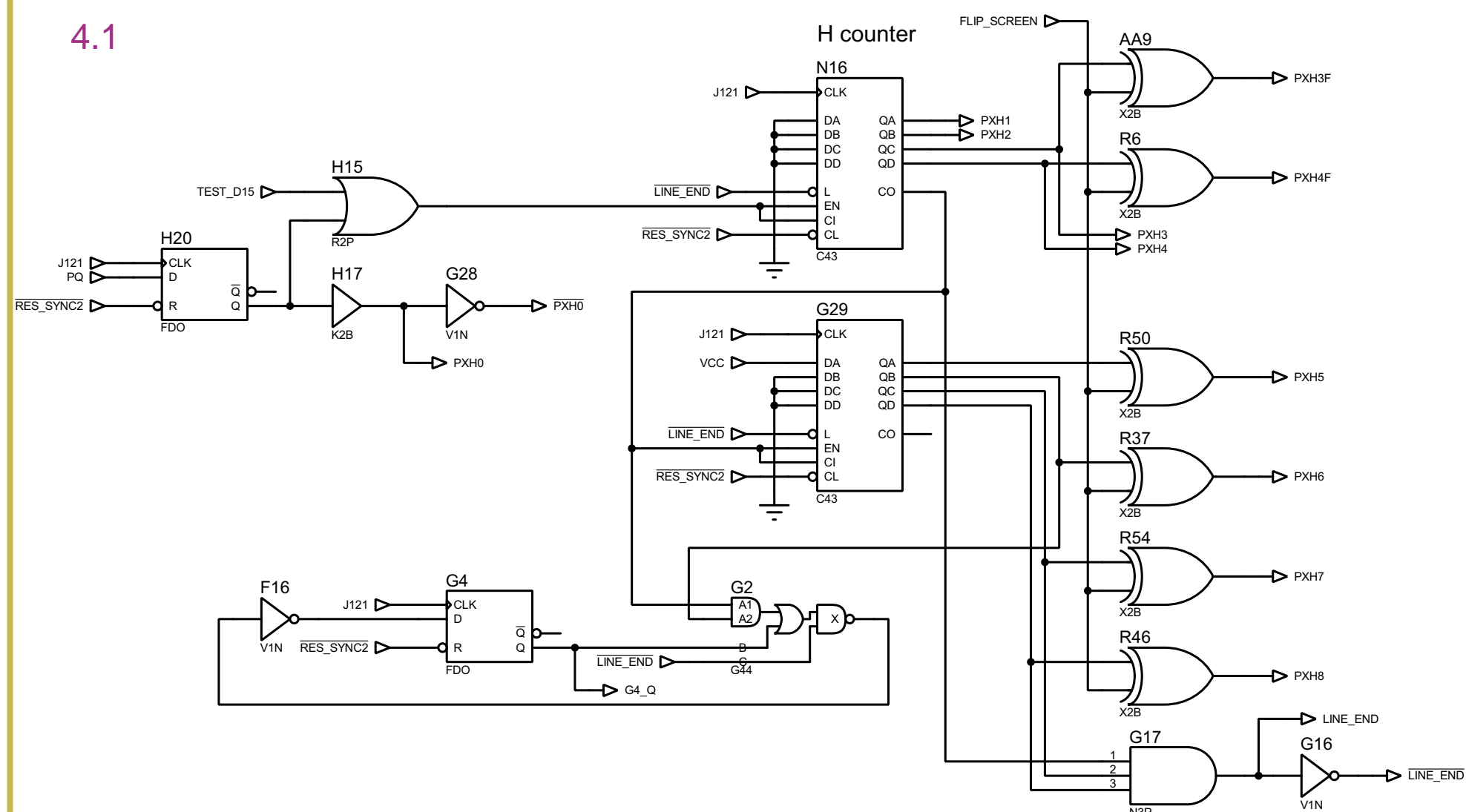


```
wire [7:0] DB_BUF
```

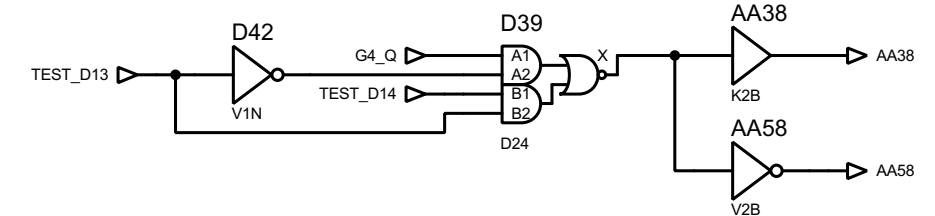
4.2

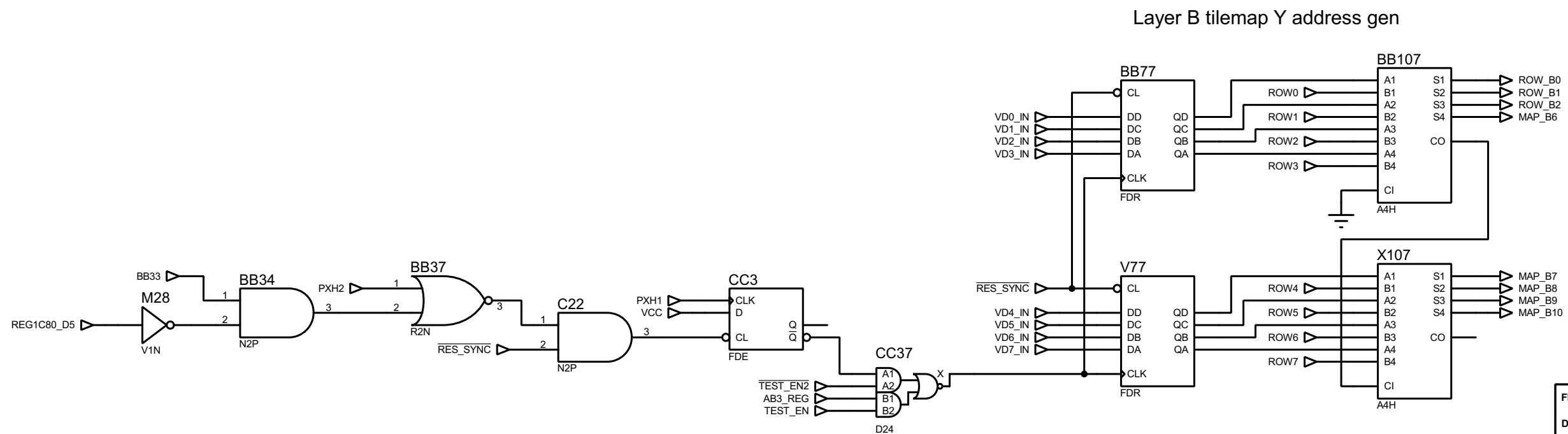
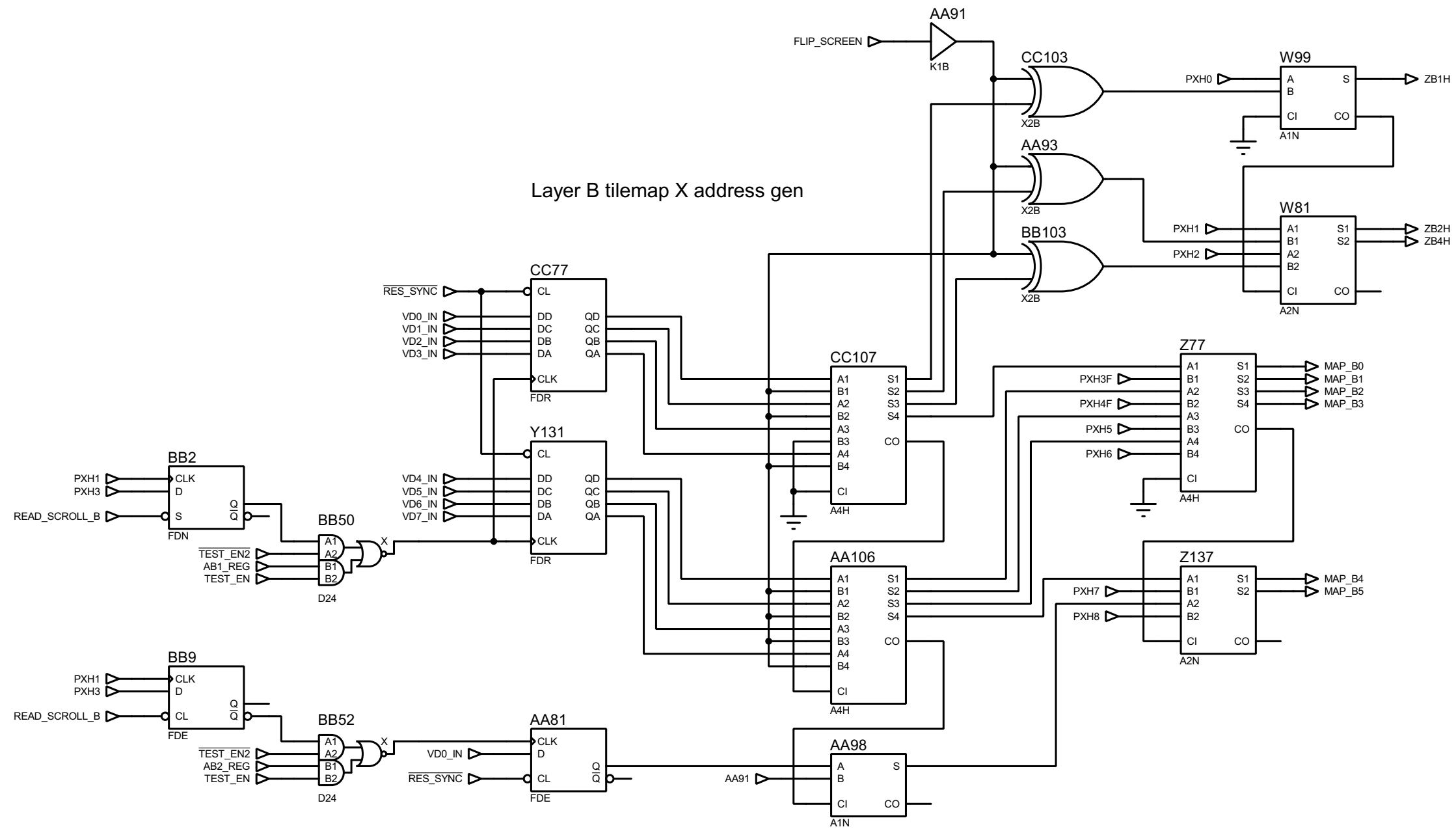


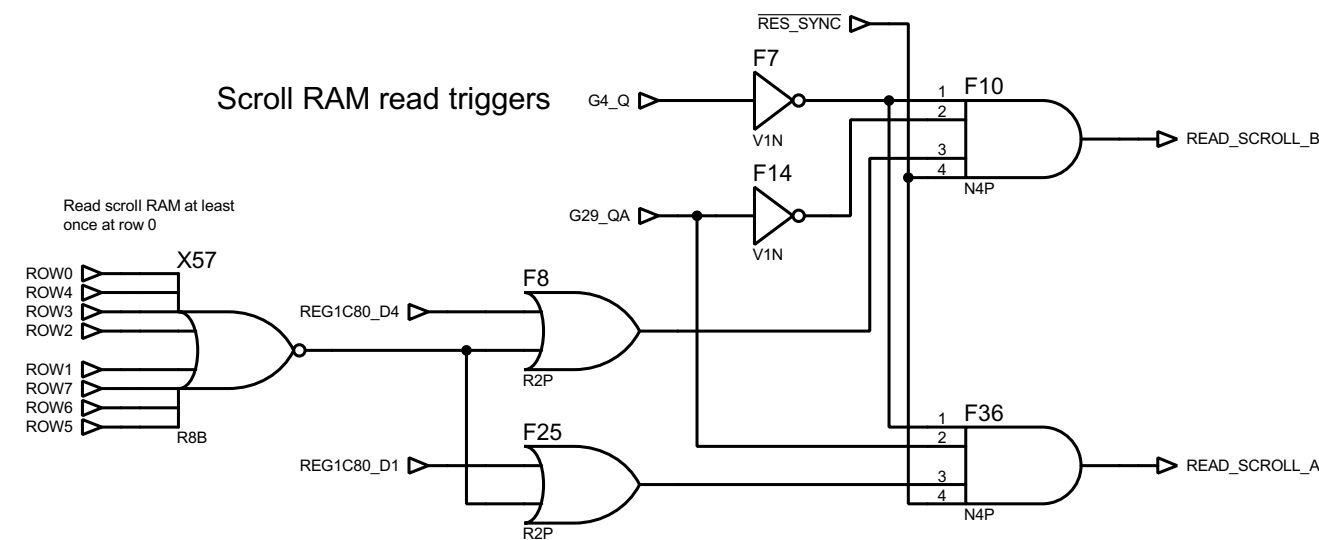
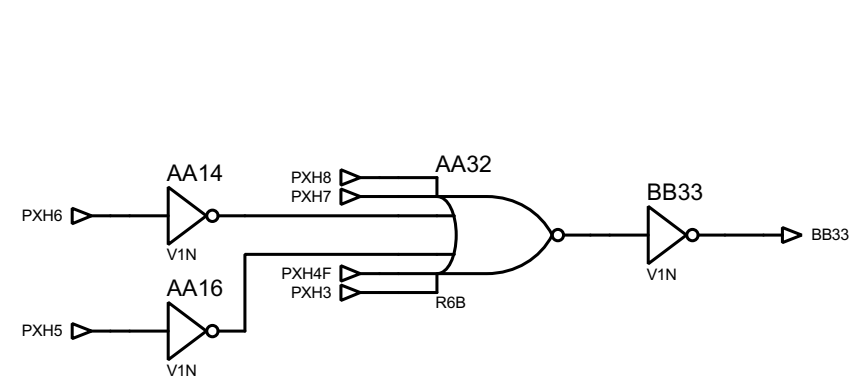
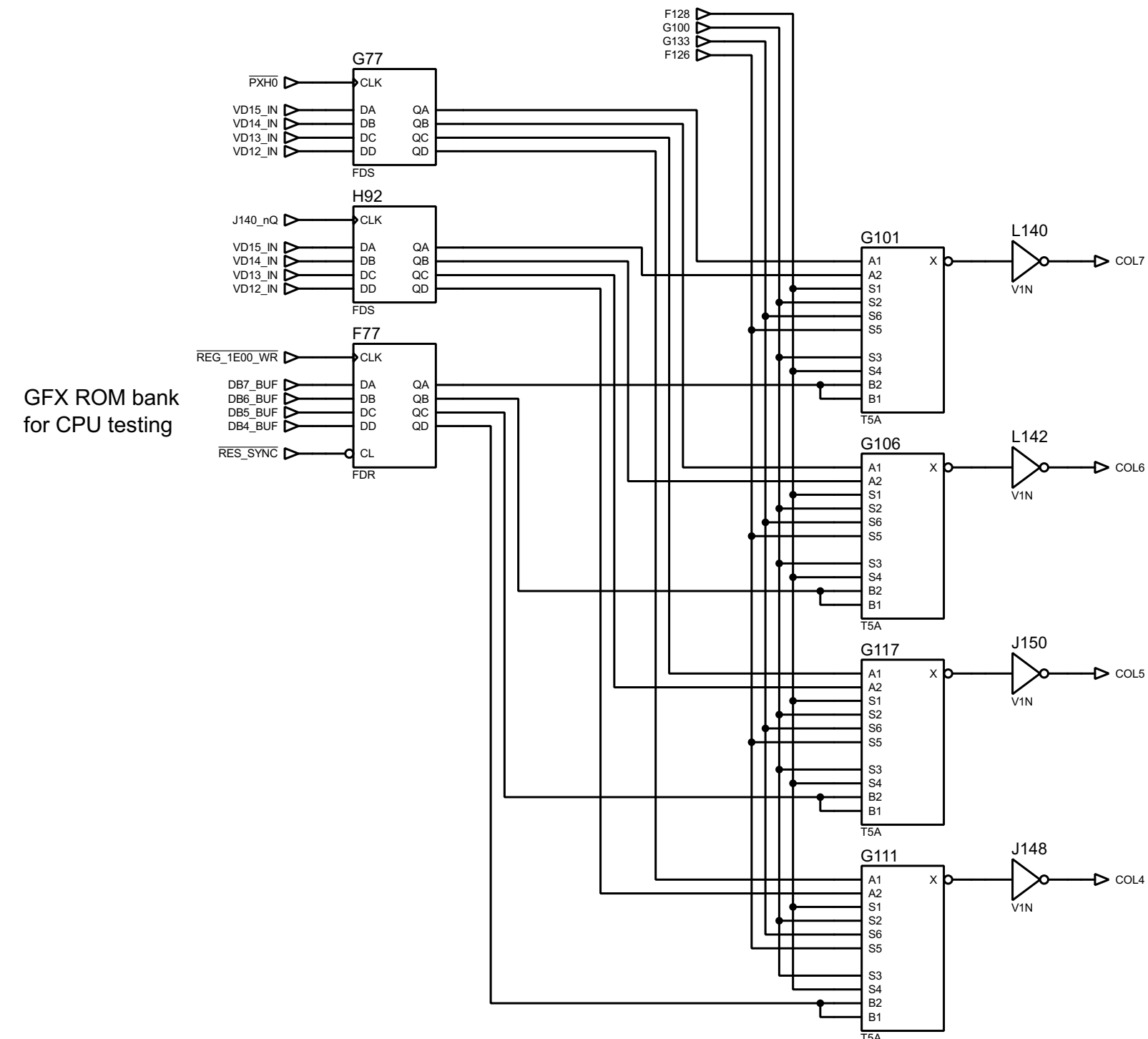
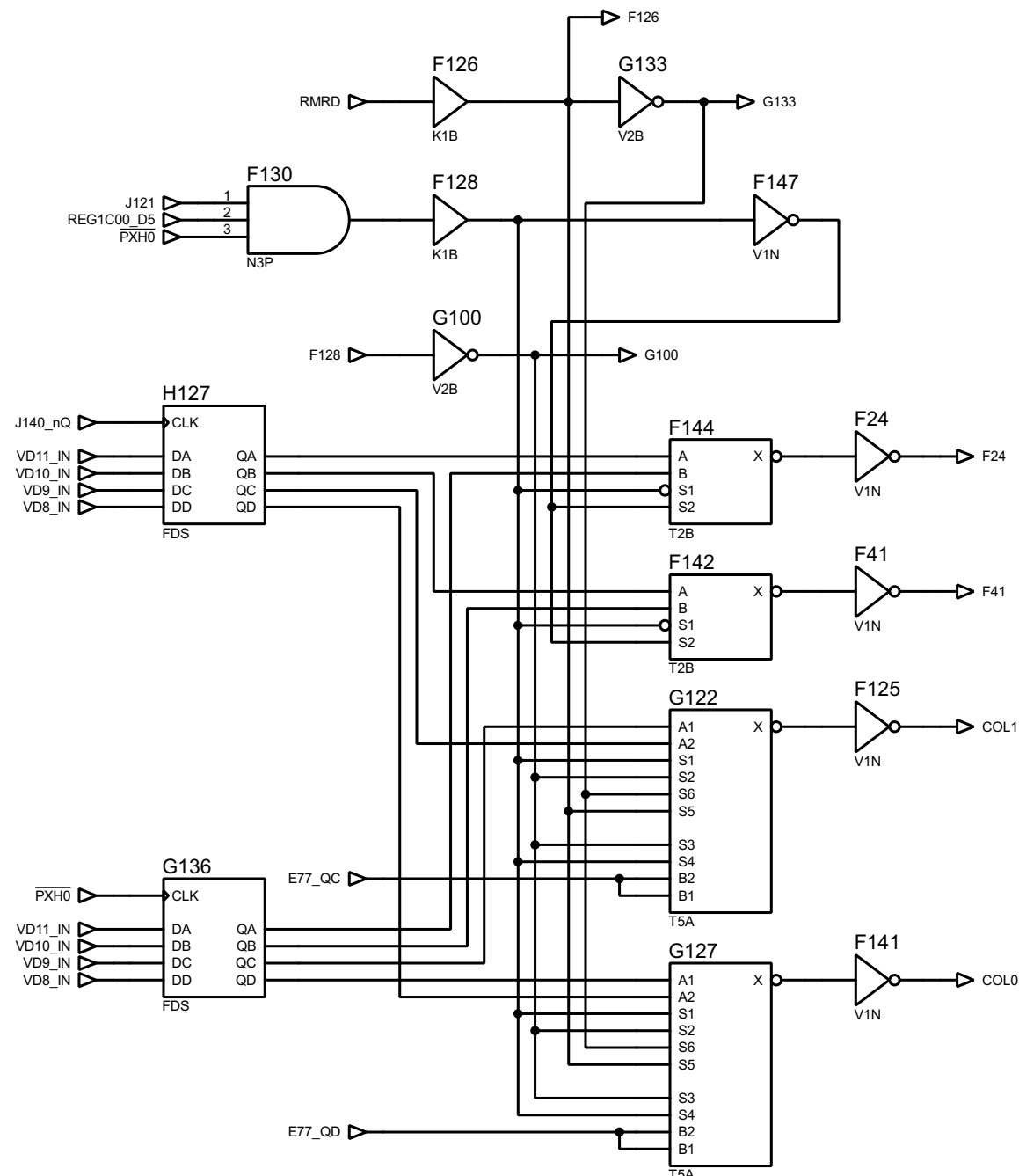
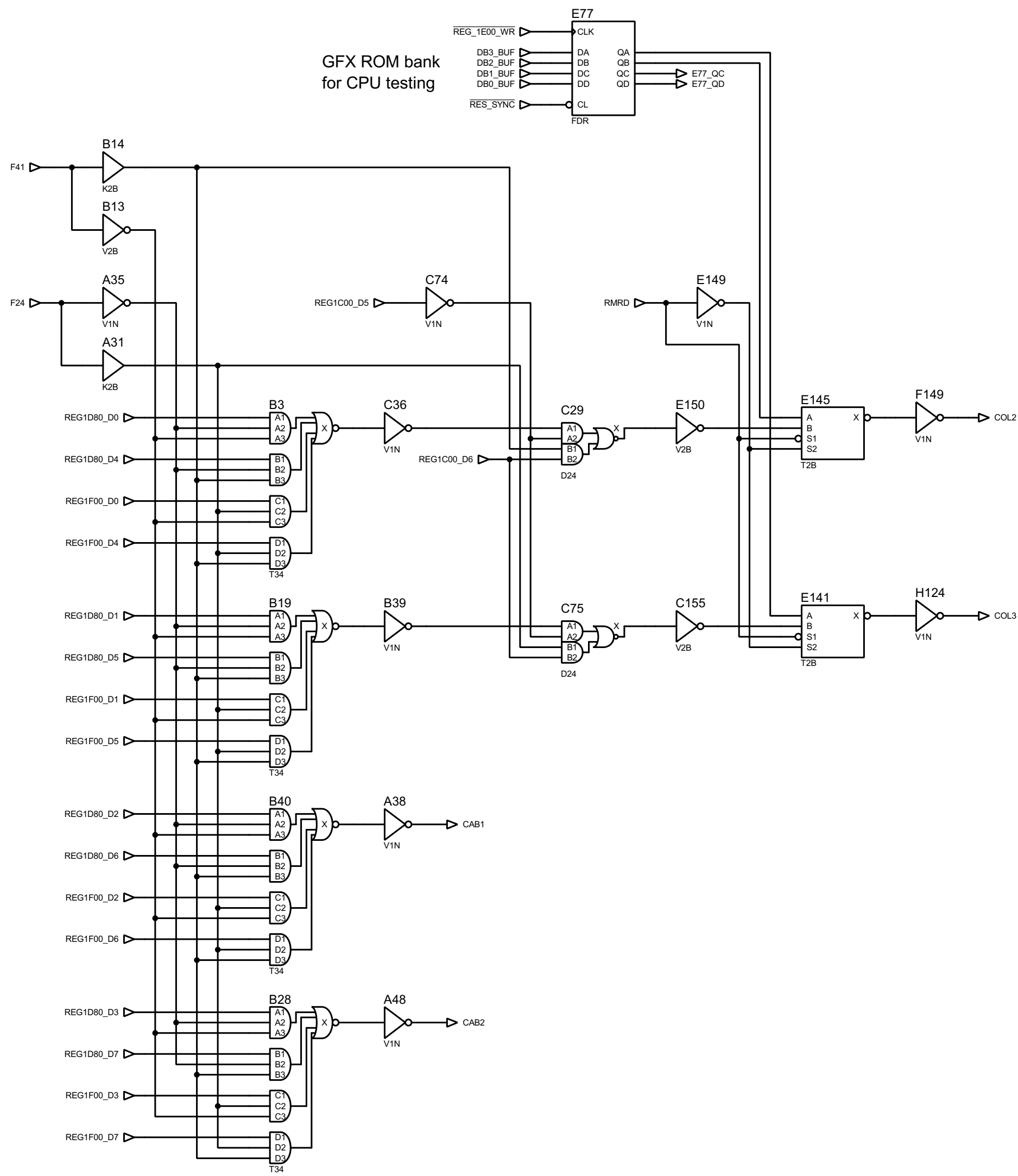
4.1



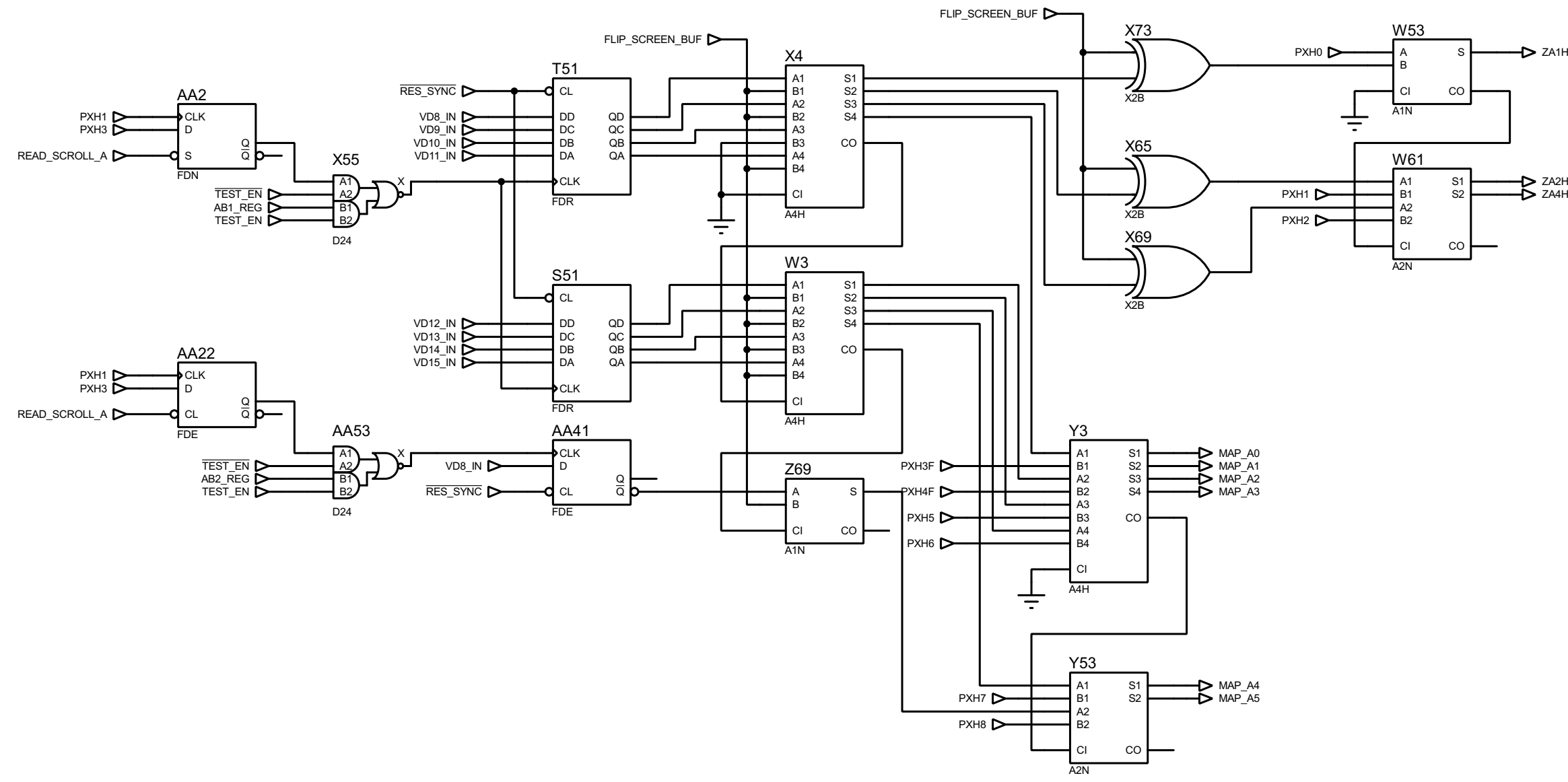
4.3







Layer A tilemap X address gen



Layer A tilemap Y address gen

