

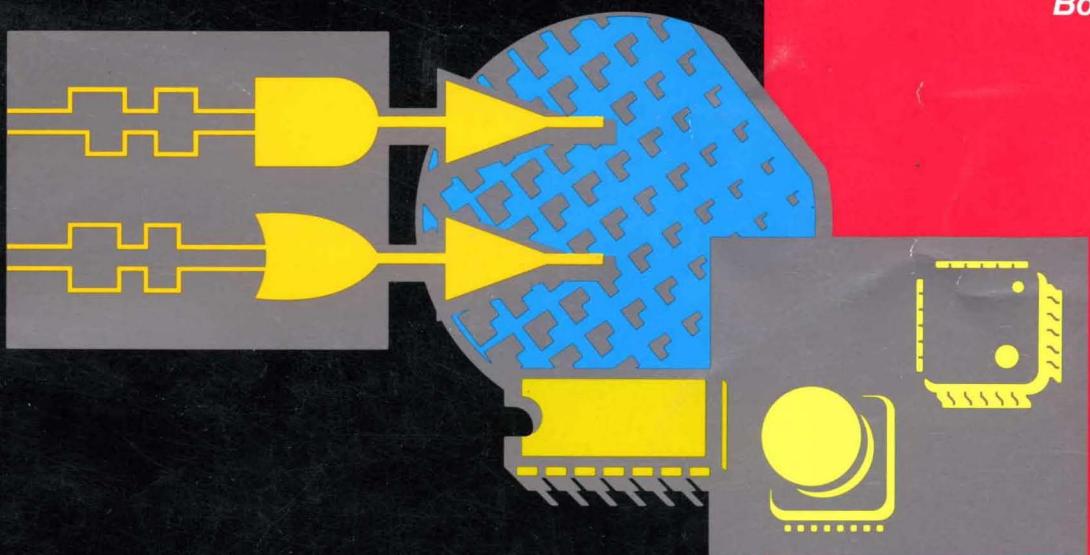
CMOS Channeled Gate Arrays

1989



CMOS Channeled Gate Arrays

1989
Data
Book



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Design Information **1**

UHB Series Unit Cell Library **2**

AV Series Unit Cell Library **3**

Sales Information **4**



Price \$10.00

CMOS Channeled Gate Arrays



1989 Data Book

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Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art electronic products.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc., with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, Fujitsu Microelectronics has grown to include one R&D division, two marketing divisions, two manufacturing divisions and a subsidiary. Fujitsu Microelectronics offers a complete array of semiconductor products for its customers.

The R&D Division, APD (Advanced Products Division), using U.S.-based engineering, has jointly developed RISC for Sun Microsystems and Ethernet®, a chip set used in local area networks. APD also markets AFP, an adaptive filter processor, and EtherStar®, the first VLSI device to integrate both StarLAN® and Ethernet protocols into one device.

The Microwave and Optoelectronics Division markets GaAs FETs and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors. The second marketing division, and the largest FMI division, is ICD (Integrated Circuits Division).

Memory and programmable devices marketed by ICD include DRAMs, EPROMs, EEPROMs, NOVRAMs, CMOS masked ROMs, bipolar PROMs, CMOS SRAMs, ECL RAMs, STRAMs (the first self-timed RAM), high speed ECL Logic, linear ICs and transistors.

ASIC products offered by ICD include bipolar gate arrays, CMOS gate arrays, and standard cells. Customer support and customer CAE training for ASIC designs is available through FMI's five design centers: San Jose, Dallas, Atlanta, Chicago, and Boston, with additional design centers planned for Gresham, Oregon and Irvine, California.

Microcomputer and communications products offered by ICD include 4-bit MCUs, 8- and 16-bit MPUs, SCSI and controllers, DSPs, prescalers, and PLLs.

Fujitsu Microelectronics' manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, FMI opened the Gresham Manufacturing Division to manufacture ASIC products. This facility has one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

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Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a totally owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Western Europe. The wide range of IC products, LSI memories and, in particular, gate arrays are noted throughout Western Europe for design excellence and unmatched reliability. Five branch offices to support Fujitsu's semiconductor operations are located in Munich, London, Paris, Stockholm, and Milan.

Fujitsu Microelectronics Ireland, Ltd. (European Production Center)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980 in the suburbs of Dublin as Fujitsu's European Production Center for integrated circuits. FME supplies 64K/256K DRAMs, 64K CMOS/NMOS EPROMs, 256K EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd. (European Design Center)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with a highly sophisticated CAD system to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Pacific Asia Ltd. (Asian/Oceanian Sales Center)

Fujitsu Microelectronics Pacific Asia Ltd. (FMP) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

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- ™ EtherStar is a trademark of Fujitsu Microelectronics, Inc.
- ™ StarLAN is a trademark of AT&T.

Preface

Fujitsu Microelectronics introduced its first commercially available gate array, a bipolar chip called the B200, in 1974 (Fujitsu had been making them for internal use since 1972). Over the years it has been so popular that it is regarded as the world's most widely implemented gate array. Since that first array, Fujitsu has produced over 9000 successful bipolar and CMOS custom designs.

Fujitsu designs are successful because they are implemented using the most advanced design verification CAD systems available, allowing the production of chips with 90% cell utilization (more functional logic per chip than the industry standard) and one of the highest performance records in the industry.

This data book provides you with information necessary to choose an application specific IC (ASIC) design using one of Fujitsu's advanced CMOS channeled gate array technologies (AV, AVB, AVL, AVM, and UHB). The data book describes Fujitsu's CMOS channeled gate array technologies, explains the benefits and specifications applicable to each, and outlines the process by which logic and circuit designers create a chip. Except where noted, the material presented in this data book is common to all of Fujitsu's CMOS channeled technologies. The device (unit cell) libraries for these channeled gate array technologies are included at the end of this volume. The second volume in this series provides the same information for Fujitsu's channel-less or sea-of-gates ASIC technologies.

Fujitsu has pioneered and maintained a technological lead in the production of bipolar as well as CMOS ASIC devices; data books describing Fujitsu's other ASIC product families, as well as any other technical or sales-related information, may be obtained from any Fujitsu Technical Resource Center or Sales Office listed at the end of this book or by calling or writing Fujitsu Microelectronics Inc., 3545 North First Street, San Jose, CA 94135-1804, (408) 922-9000.

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Fujitsu ASIC Products Listing

CMOS Channeled Gate Arrays Data Book

UHB Series High Drive Gate Arrays — 1.5μ , 0.9 ns typical delay

Description	Name	Device Part Number
336 Gates, 58 I/O	C330UHB	MB625xxx
530 Gates, 64 I/O	C530UHB	MB624xxx
830 Gates, 74 I/O	C830UHB	MB623xxx
1,233 Gates, 88 I/O	C1200UHB	MB622xxx
1,724 Gates, 102 I/O	C1700UHB	MB621xxx
2,220 Gates, 115 I/O	C2200UHB	MB620xxx
3,066 Gates, 140 I/O	C3000UHB	MB606xxx
4,174 Gates, 155 I/O	C4100UHB	MB605xxx
6,000 Gates, 155 I/O	C6000UHB	MB604xxx
8,768 Gates, 188 I/O	C8700UHB	MB603xxx
12,734 Gates, 220 I/O	C12000UHB	MB602xxx

AV Series CMOS Gate Arrays — 1.8μ , 1.4 ns typical delay

AV Series High Speed Gate Arrays

Description	Name	Device Part Number
2,640 Gates, 106 I/O	C2600AV	MB654xxx
3,900 Gates, 127 I/O	C3900AV	MB653xxx
5,022 Gates, 127 I/O	C5000AV	MB652xxx
6,664 Gates, 160 I/O	C6600AV	MB651xxx
8,000 Gates, 160 I/O	C8000AV	MB650xxx

AVB Series High Drive Gate Arrays

Description	Name	Device Part Number
357 Gates, 38 I/O	C350AVB	MB675xxx
549 Gates, 48 I/O	C540AVB	MB674xxx
852 Gates, 58 I/O	C850AVB	MB673xxx
1,245 Gates, 68 I/O	C1200AVB	MB672xxx
1,674 Gates, 74 I/O	C1600AVB	MB671xxx
2,052 Gates, 88 I/O	C2000AVB	MB670xxx

AVL Series Low Power Gate Arrays — 2.3μ , 2.9 ns typical delay at 3V

Description	Name	Device Part Number
357 Gates, 38 I/O, 3 Volt Operation	C350AVL	MB685xxx
549 Gates, 48 I/O, 3 Volt Operation	C540AVL	MB684xxx
852 Gates, 58 I/O, 3 Volt Operation	C850AVL	MB683xxx
1,245 Gates, 68 I/O, 3 Volt Operation	C1200AVL	MB682xxx
1,674 Gates, 74 I/O, 3 Volt Operation	C1600AVL	MB681xxx
2,052 Gates, 88 I/O, 3 Volt Operation	C2000AVL	MB680xxx

AVM Series Gate Arrays with Memory

Description	Name	Device Part Number
1,564 Gates with 4.6K ROM or 2.3K RAM, 107 I/O	C1502AVM	MB662xxx
2,375 Gates with 2K ROM or 1K RAM, 117 I/O	C2301AVM	MB661xxx
4,087 Gates with 4.6K ROM or 2.3K RAM, 120 I/O	C4002AVM	MB660xxx

CMOS Channelless Gate Arrays Data Book

AU Series CMOS Series Gate Arrays — 1.2 μ , 0.6 ns typical delay

Description	Name	Device Part Number
10,224 Gates, 108 I/O	C10KAU	MB637xxx
15,486 Gates, 138 I/O	C15KAU	MB636xxx
20,876 Gates, 155 I/O	C20KAU	MB635xxx
31,500 Gates, 178 I/O	C30KAU	MB634xxx
41,184 Gates, 220 I/O	C40KAU	MB633xxx
52,164 Gates, 257 I/O	C50KAU	MB632xxx
75,140 Gates, 300 I/O	C75KAU	MB631xxx
10,2144 Gates, 332 I/O	C100KAU	MB630xxx

BiCMOS Gate Arrays Data Book

BC Series BiCMOS Gate Arrays — 1.5 μ /1.4 μ , 0.65 ns typical delay

Description	Name	Device Part Number
645 Gates, 52 I/O	BC400	MB211xxx
1,218 Gates, 72 I/O	BC800	MB212xxx
1,872 Gates, 96 I/O	BC1200	MB213xxx
3,240 Gates, 112 I/O	BC2000	MB214xxx

BC-H Series BiCMOS Gate Arrays — 1.0 μ /0.5 μ , 0.45 ns typical delay

4,312 Gates, 96 I/O	BC4000H	MB221xxx
8,160 Gates, 128 I/O	BC8000H	MB222xxx
11,968 Gates, 160 I/O	BC12000H	MB223xxx
16,720 Gates, 200 I/O	BC16000H	MB224xxx

ECL Gate Arrays Data Book

ET Series ECL Gate Arrays — 1.0 μ , 220 ps typical delay

Description	Name	Device Part Number
1,056 Gates, 64 I/O	ET750	MB121Kxxx
2,112 Gates, 88 I/O	ET1500	MB123Kxxx
4,224 Gates, 120 I/O	ET3000	MB125Kxxx
6,160 Gates, 120 I/O	ET4500	MB128Kxxx
2,640 Gates, 120 I/O with 4.6 Kb RAM	ET2004M	MB181/191xxx
2,640 Gates, 136 I/O, with 9.2 Kb RAM	ET2009M	MB182/192xxx
3,960 Gates, 136 I/O, with 4.6 Kb RAM	ET3004M	MB183/193xxx

H Series ECL Gate Arrays — 0.5 μ , 100 ps typical delay

9,856 Gates, 200 I/O	ET10000H	MB147/157xxx
9,856 Gates, 300 I/O	E10000H	MB148/158xxx
4,928 Gates, 200 I/O, with 5.1Kb RAM	ET5005HM	MB185/195xxx
128 Gates, 23 I/O	E128H	MB1800
32 Gates, 13 I/O	E32	MB1700
128 Gates 16 I/O	E128	MB1600

CMOS Standard Cell Data Book

AU Series Standard Cells — 1.2 μ , 0.6 ns typical delay

Section 1



Design Information

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1

Chapter 1 – Fujitsu CMOS Products

Contents of This Chapter

- 1.1 Introduction
 - 1.2 CMOS Technology for ASICs
 - 1.3 CMOS Gate Array Structure
 - 1.4 Fujitsu's CMOS Channeled Gate Array Technologies: UHB and AV Data Sheets
-

1.1 Introduction

This section of the data book gives an overview of CMOS technology and introduces the CMOS channeled gate array technology families developed by Fujitsu to implement ASIC designs.

1.2 CMOS Technology for ASICs

ASICs (Application Specific Integrated Circuits) are large scale integrated circuits that provide customers with made-to-order functions. These ICs implement the unique value designed into customer products by producing custom semiconductor designs that allow customers to take advantage of perceived market opportunities in a timely manner. The customized solutions offered by ASICs combine the power of personalized electronics and the advantage of increased system efficiency.

CMOS technology has long been chosen for ASIC applications because of its low power and high density characteristics. Advancing process technology and new production and fabrication techniques have now allowed device speed to increase to the point where it is competitive with bipolar devices. Fujitsu CMOS gate arrays are manufactured using advanced silicon gate technology utilizing two-layer and three-layer metal. This fabrication process yields parts that:

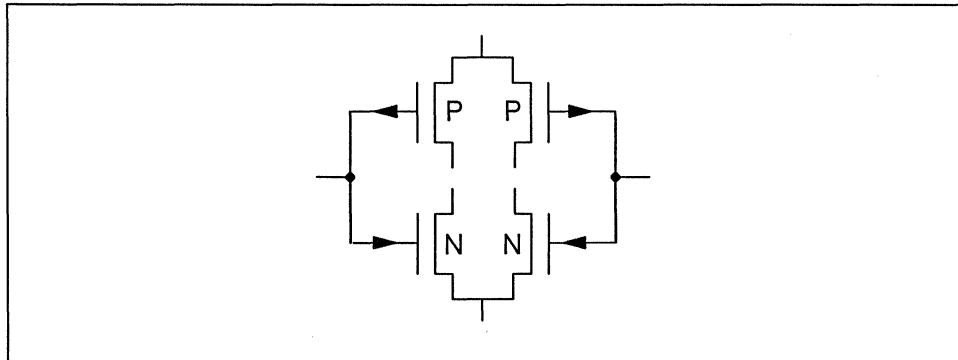
- a) require very low power dissipation (typically less than 500 mW per channeled array)
- b) operate at speeds equaling existing bipolar technologies
- c) feature higher gate densities than competing bipolar devices
- d) use a single power supply of 5 volts or less
- e) provide top-grade noise immunity and programmable logic levels compatible with TTL and CMOS logic families

1.3 CMOS Gate Array Structure

Fujitsu CMOS gate arrays are configured in a matrix of basic cells in the center of the chip with input-output (I/O) cells on the device periphery. One basic cell is equivalent to a two-input NAND gate. The custom logic function is realized by interconnecting basic cells with double-layer metalization (or triple-layer metalization for the largest arrays). Fujitsu's gate array products are fabricated using a twin-tub polysilicon CMOS process to produce high-speed, high-density arrays consisting of 300 to 100,000 basic cells.

1.3.1 The Basic Cell

The basic cell of Fujitsu's CMOS gate array is a common building block consisting of one pair of P-channel and one pair of N-channel MOS transistors interconnected as shown in Figure 1-1.



1

Figure 1-1. The Basic Cell

Since this is a "generic" basic cell, no connections are shown to the power supply (+5 volts), to ground, or to the two common control gate terminals of the circuit. These connections are made as required during the metalization phase of the manufacturing process. All CMOS gate arrays are built up of basic cells.

Figure 1-2 shows a schematic representation of the basic cell with the addition of the custom metalization required to convert the generic basic cell into a two-input NAND gate.

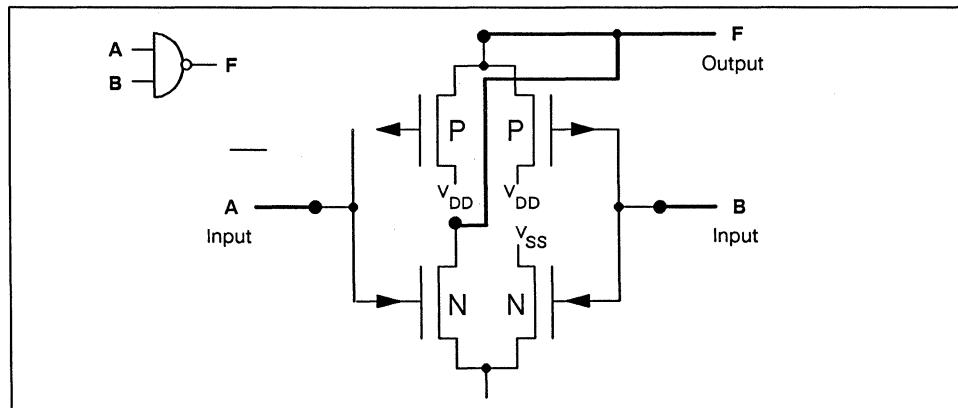


Figure 1-2. The Basic Cell as a 2-Input NAND Gate

1.3.2 Basic Cell Construction

Basic cell construction varies somewhat among Fujitsu's CMOS technologies; however, an explanation based on AV technology provides a good model of how a basic cell is fabricated in any

of the CMOS families. In AV, the basic cell is constructed from an N-type silicon substrate upon which a P-well is deposited. The surface of the substrate is then covered with a thin layer of silicon dioxide (glass) and two strips of polysilicon are deposited perpendicular to the P-well and geometrically parallel. (Polysilicon is a silicon-based compound chemically altered so that it has good electrical conduction properties.) The polysilicon strips serve as the gate control elements of the basic cell and also as the two electrical interconnections between the sources of the P and N transistor pairs. See Figure 1-3.

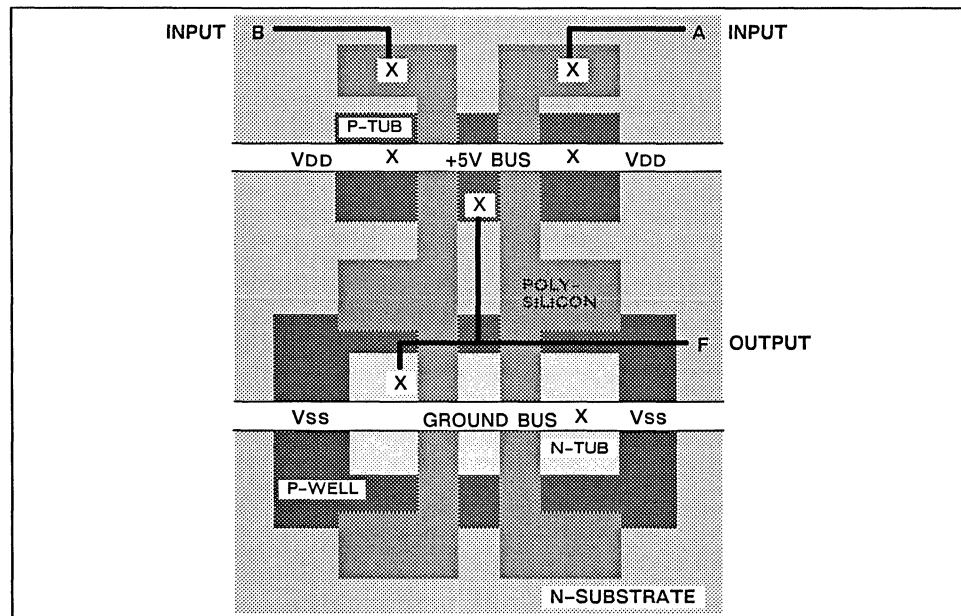


Figure 1-3. Physical Construction of the Unit Cell NAND Gate

The silicon dioxide layer is then stripped away from all areas of the substrate not protected by polysilicon. In two separate steps, the N-type and the P-type material of the twin tubs is diffused onto the substrate.

For the next step, N-type material is diffused or implanted into the P-well that was previously laid down. It straddles the two strips of polysilicon close to their ends. The polysilicon resists the diffusion, which results in the formation of three pads of N-type material separated by the two strips of polysilicon (self-aligned processing). The center pad of N-type material serves as a common drain terminal for both N-channel transistors. The outer pads are the separate source elements.

Then the P-type material is deposited on the the N-type substrate straddling the two polysilicon strips. Similarly the center pad of P-type material forms the common source connection for both P-channel transistors. The basic cell is then converted to a unit cell by application of a custom metalization pattern that connects (or wires) various points of the basic cell, or a number of basic cells, together. Figure 1-3 shows the structure of a basic cell configured as a NAND gate after metalization (represented by the solid bold line connections) has been laid down.

Some unit cells require two or even three layers of metal to be applied. Such layers are separated by an insulating layer of silicon dioxide. Interconnections between the metal layers are made by means of "vias" passing through the glass.

1.3.3 Structure of the Chip

The arrangement of the basic cells on the chip differs according to the technology. The fundamental chip layout is a matrix of basic cells surrounded by a perimeter of I/O cells. Basic cells can be arranged in single columns, with the channels between the columns used for routing unit cell interconnections, as in AV, AVB, AVL, and AVM technologies, or in double columns as in UHB technology. See Figure 1-4. The sea-of-gates technologies are constructed with no wiring channels between the double columns, allowing the wiring to go over the cells, rather than between the cells. See Figure 1-5. The channel-less or sea-of-gates technologies are covered in a separate data book.

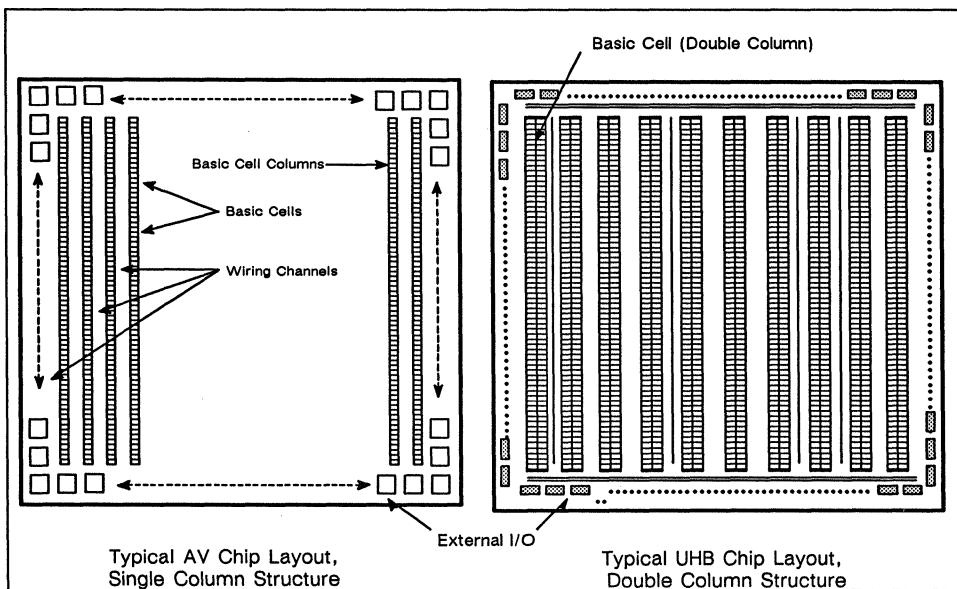


Figure 1-4. Channelled Gate Array Chip Structure

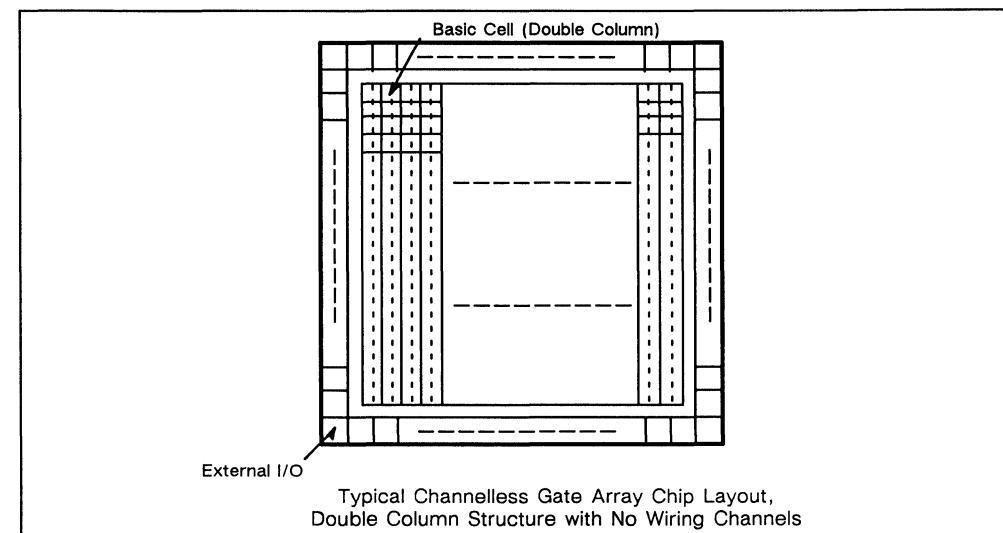


Figure 1–5. Channelless Gate Array Chip Structure

Larger gate arrays depart from the fundamental layout scheme by partitioning the basic cell matrix into four blocks. In some instances the designer may define the size of each block within certain limitations, while in other cases the block size is fixed. The purpose of chip partitioning is to improve speed performance by controlling wire length. Each block can be looked at as a small gate array, with four such gate arrays inside one package. (Smaller arrays exhibit less delay than larger ones.) In some technologies, AVM, for example, a block can be devoted to RAM or ROM for special applications requiring memory.

1.3.4 Basic Cell Arrangement

Basic cells can be arranged in any of the following configurations:

- (a) Fundamental logic function units called unit cells (e.g. NAND gate, flip-flop, etc.).
- (b) User macros, which are composed of unit cells to form higher level logic block functions (e.g., shift register or decoder). Such blocks are user-defined and may contain any unit cell configuration.
- (c) RAM macros, which are available in seven basic configurations.

1.3.5 I/O Cells

I/O cells are input/output buffer cells located on the periphery of the basic cell matrix (and memory block, if one is present). I/O cells are usually not included in the basic cell count. These buffer cells convert external voltage levels into internal CMOS levels. The output buffers provide a sufficient voltage level to drive TTL components but the input buffers must convert TTL levels to CMOS levels when appropriate.

1.3.6 Macros

Different macros are available for each technology group. For a list of available macros for each technology, contact any of the Fujitsu Technical Resource Centers listed in the back of this volume.

1.4 Fujitsu's CMOS Channeled Gate Array Technologies

Fujitsu offers over 50 different CMOS gate array devices, fabricated with advanced silicon gate technology. Fujitsu's channeled CMOS gate arrays include the technology options described in detail in the data sheets that follow:

- UHB Series CMOS Gate Arrays
- AV Series CMOS Gate Arrays (including AVB, AVL, and AVM)

Complete information on Fujitsu's channel-less CMOS gate array families is provided in a separate data book.

All offer the same fast turnaround on design, simplified customer interface, full support by Fujitsu ViewCAD system design software if requested, full design support of other major CAE workstations, and a wide variety of packaging options.

Fujitsu's newest channeled gate array technology, QCL (Quickly Customized Logic) offers the UHB cell library and UHB compatibility using AU technology with one level of metalization to provide ASIC designers with a product proven reliability with an especially fast turnaround.

The number of gates in relationship to the processing speed of each new CMOS technology is shown in Figure 1-6. Figure 1-7 shows in tabular form the equivalent gate count for each technology family.

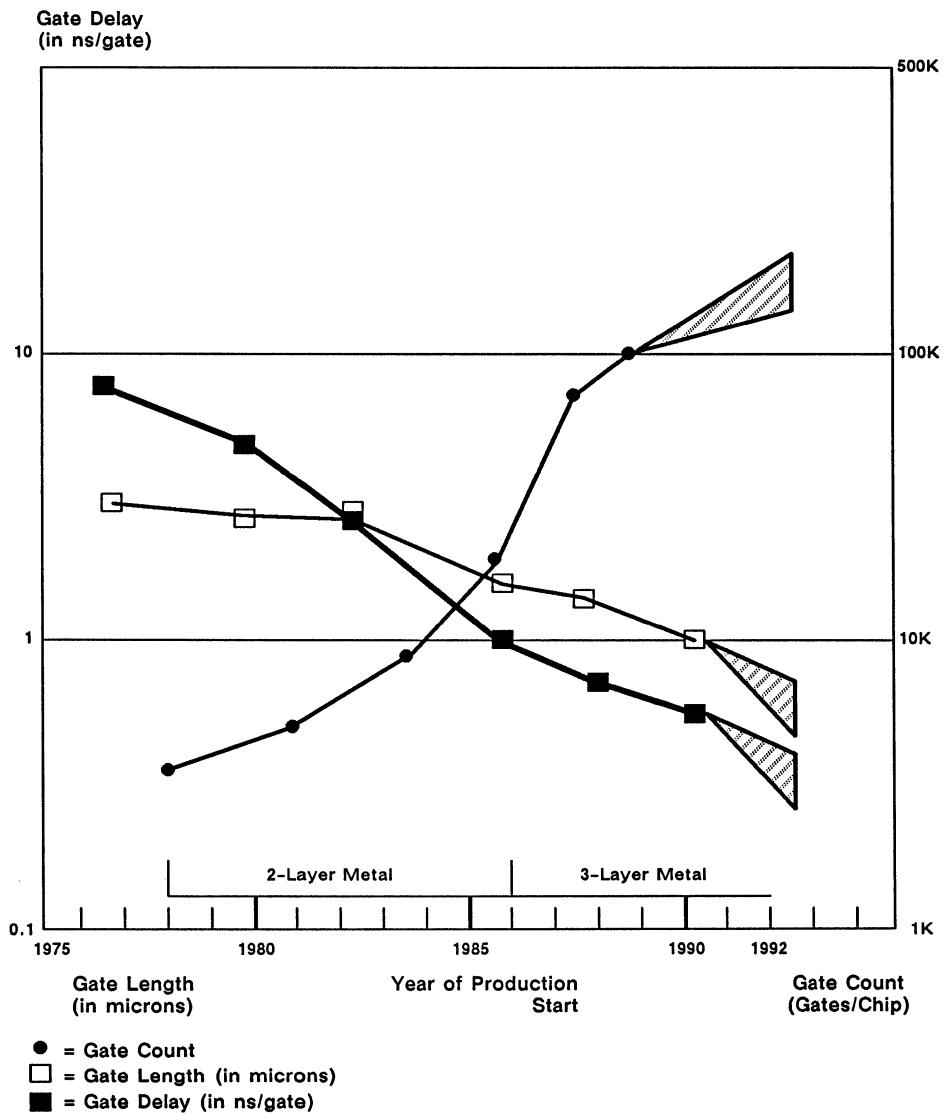


Figure 1-6. Equivalent Gate Count vs. Processing Speed,
Fujitsu CMOS Gate Array Technologies

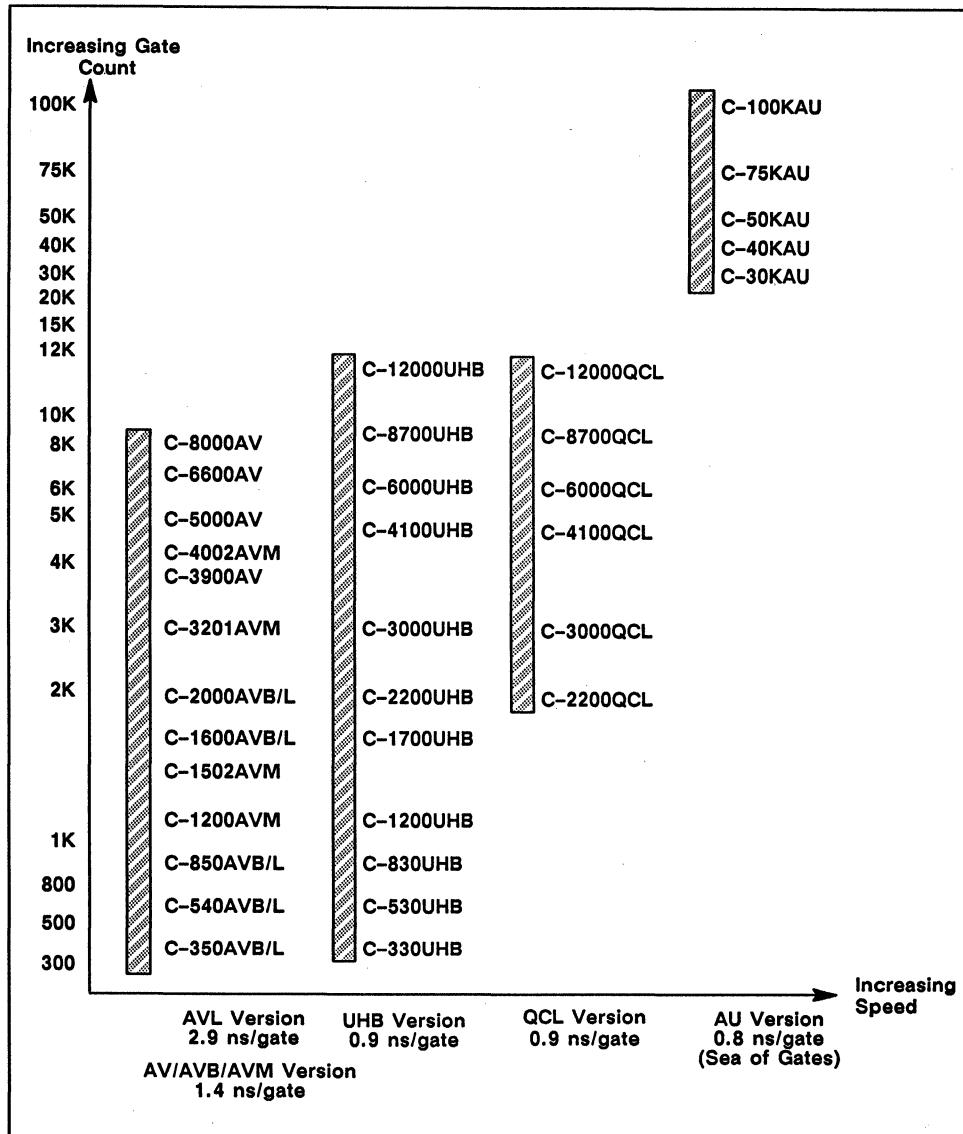


Figure 1-7. Equivalent Gate Count, Fujitsu CMOS ASIC Technology Families

FUJITSU

UHB SERIES 1.5 μ CMOS GATE ARRAYS

MB62XXXX
MB60XXXXSeptember 1988
Edition 1.1

DESCRIPTION

The UHB series of 1.5-micron CMOS gate arrays is a highly integrated low-power, ultra high-speed product family that derives its enhanced performance and increased user flexibility from the use of a system-proven, dual-column gate structure and 2-layer metal interconnect technology. The unique dual-column gate structure increases density and speed performance, as well as gate utilization.

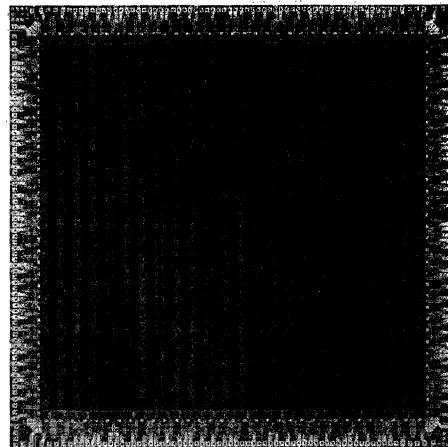
Internal high-drive clock buffers minimize clock skew across the chip while internal bus performance and integrity is assured by incorporating 3-state transmission gate logic underneath the routing channels. The high-drive output buffers provide highly symmetrical output waveforms.

FEATURES

- High-density silicon gate CMOS technology
 - 330 to 12,000 usable gates
 - 90% maximum utilization fully autorouted
- Ultra high speed
 - typical 0.9 ns gate delay
 - narrow delay variation
- High sink current capability
 - 3.2 mA, 8 mA, 12 mA, and 24 mA options available
 - selectable edge rate control
- Low-skew clock signal distribution
 - High-performance clock drivers
 - Hierarchical clock distribution
 - Frequency-dependent clock routing
- Automatic test pattern generation for 6K gates and up
 - complete family of scan design macros available
- 2-column gate structure enhances macro performance
- High-performance internal 3-state bus
 - buried cells within the routing channels ensure high density and reliable performance
- Proven 1.5-micron 2-layer metal technology
- Highest pin-to-gate count commercially available
 - 60 logic I/O for 336 gates
 - 222 logic I/O for 1200 gates
- Input buffers incorporating pull-up/pull-down resistance
- Built-in feedback resistors for oscillators
- User-defined hierarchy-driven placement

Device Name	Utilizable Gates ¹	Maximum Signal Pins ²
C-330UHB	336 gates	60
C-530UHB	530 gates	66
C-830UHB	830 gates	76
C-1200UHB	1233 gates	92
C-1700UHB	1724 gates	108
C-2200UHB	2220 gates	123
C-3000UHB	3066 gates	148
C-4100UHB	4174 gates	163
C-6000UHB	6000 gates	163
C-8700UHB	8768 gates	188
C-12000UHB	12734 gates	220

1. Gates available for logic (exclusive of I/O usage).
2. Maximum signal pin numbers depend on the output drive requirements and the package selected.



PRODUCT FAMILY DESCRIPTIONS

Device Name	Part Number	2-Input Gate Equivalent Complexity	Maximum Signal Pins	Total Number of Basic Cells on Chip
C-330UHB	MB625xxx	336 gates	60	610 gates
C-530UHB	MB624xxx	530 gates	66	840 gates
C-830UHB	MB623xxx	830 gates	76	1176 gates
C-1200UHB	MB622xxx	1233 gates	92	1680 gates
C-1700UHB	MB621xxx	1724 gates	108	2232 gates
C-2200UHB	MB620xxx	2220 gates	123	2800 gates
C-3000UHB	MB606xxx	3066 gates	148	3744 gates
C-4100UHB	MB605xxx	4174 gates	163	4888 gates
C-6000UHB	MB604xxx	6000 gates	163	6976 gates
C-8700UHB	MB603xxx	8768 gates	188	9720 gates
C-12000UHB	MB602xxx	12734 gates	220	13728 gates

Notes: 1. Typical device gate speed, with F/O=2, for a 2-input NAND gate, is 0.9 ns.

2. A basic cell is equivalent to a 2-input gate.

3. Basic cells on chip are also used for I/O buffer function.

4. The maximum signal pin numbers depend on the output drive requirements and the package selection.

AC CHARACTERISTICS

BEST/WORST CASE MULTIPLIERS FOR PROPAGATION DELAYS

Propagation delays characteristic of a gate array are a function of several factors, including operating temperature, supply voltage, fanout loading, interconnection routing metal, process variation, input transition time, and input signal polarity. Temperature and supply voltage factors affecting propagation delays in the UHB CMOS family of gate arrays are given in the table below.

Temperature Range	Pre-Layout Simulation				Post-Layout Simulation			
	$V_{DD} = 5V \pm 5\%$		$V_{DD} = 5V \pm 10\%$		$V_{DD} = 5V \pm 5\%$		$V_{DD} = 5V \pm 10\%$	
	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case
1. 0 - 70°C	0.35	1.65	0.30	1.75	0.40	1.60	0.35	1.70
2. -20 - 70°C	0.35	1.65	0.25	1.75	0.35	1.60	0.30	1.70
3. -40 - 70°C	0.25	1.65	0.20	1.75	0.30	1.60	0.25	1.70
4. -40 - 85°C	0.25	1.75	0.20	1.85	0.30	1.70	0.25	1.80

1. = commercial temperature range

4. = industrial temperature range

Constants for calculating the delays due to process variation, fanout loading, interconnection routing metal, transition time, and signal polarity are given for each unit cell in the UHB Unit Cell Library. Delays using these factors are calculated for a representative selection of unit cells and are shown in the Propagation Delays table on the following page.

REPRESENTATIVE PROPAGATION DELAYS

Calculations are representative of unit cells in the C12000UHB (UHB 12000-Gate CMOS Gate Array).

Typical values are indicated. Worst case multipliers are applied to typical values. Smaller arrays can exhibit significantly greater speed.

Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Input Transition	Propagation Delays (in ns)						
				NDI (Fan-out)						
				1	2	4	8	16	32	
Inverter	V1N	1	t_{PLH} , t_{PHL}	0.86 0.67	1.51 1.04	2.36 1.52	3.53 2.18	5.19 3.11	8.09 4.74	
Power 2-Input NAND	N2K	2	t_{PLH} , t_{PHL}	0.66 0.68	.99 .97	1.41 1.34	1.99 1.85	2.83 2.58	4.27 3.85	
Power 16-Input NAND	NGB	11	t_{PLH} , t_{PHL}	1.82 3.69	2.15 3.93	2.57 4.25	3.15 4.69	3.99 5.31	5.43 6.40	
Power 2-Input NOR	R2K	2	t_{PLH} , t_{PHL}	0.95 0.67	1.53 0.91	2.27 1.23	3.29 1.67	4.75 2.29	7.28 3.38	
Power Exclusive OR	X2B	4	t_{PLH} , t_{PHL}	1.72 1.82	2.05 2.03	2.47 2.29	3.05 2.66	3.89 3.18	5.33 4.08	
3-wide 2-AND 6-Input AND-OR Inverter ($A \rightarrow Y$)	D36	3	t_{PLH} , t_{PHL}	1.78 1.22	2.93 1.80	4.41 2.54	6.45 3.56	9.37 5.02	4.43 7.55	
2-wide 2-OR 4-Input OR-AND-Inverter ($A \rightarrow X$)	G24	2	t_{PLH} , t_{PHL}	1.54 1.20	2.73 1.78	4.27 2.52	6.39 3.54	9.40 5.00	14.65 7.53	
Power 2-AND 8-Wide Multiplexer ($A \rightarrow X$)	T28	11	t_{PLH} , t_{PHL}	2.41 1.66	2.74 1.83	3.16 2.04	3.74 2.33	4.58 2.75	6.02 3.47	
Power Clock Buffer	K2B	3	t_{PLH} , t_{PHL}	1.30 1.38	1.57 1.58	1.90 1.83	2.30 2.13	2.81 2.51	3.61 3.11	
Scan 8-bit D FF with Clock Inhibit and 2:1 Data Multiplexer ($CK, IH \rightarrow Q$)	SHK	88	t_{PLH} , t_{PHL}	5.22 4.92	5.87 5.29	6.72 5.77	7.89 6.43	9.55 7.36	12.45 8.99	
Non-Scan D FF with Reset ($CK \rightarrow Q$)	FDO	7	t_{PLH} , t_{PHL}	2.51 2.14	3.16 2.55	4.01 3.08	5.18 3.81	6.84 4.85	9.74 6.66	
Non-Scan Power D FF with Clear ($CK \rightarrow Q$)	FD5	8	t_{PLH} , t_{PHL}	2.17 1.89	2.50 2.10	2.92 2.36	3.50 2.73	4.34 3.25	5.78 4.15	
Non-Scan 4-bit Binary Synchronous Up Counter ($Cl \rightarrow CO$)	C43	48	t_{PLH} , t_{PHL}	2.18 1.10	2.83 1.43	3.68 1.85	4.85 2.43	6.51 3.27	9.41 4.71	
Non-Scan 4-bit Binary Synchronous Up Counter ($Cl \rightarrow CO$)	C45	48	t_{PLH} , t_{PHL}	2.52 1.68	3.22 2.05	4.12 2.53	5.36 3.19	7.13 4.12	10.21 5.75	

Note: Delays for inter-block wiring are not included

REPRESENTATIVE PROPAGATION DELAYS (Continued)

Calculations are representative of unit cells in the C12000UHB (UHB 12000-Gate CMOS Gate Array).
 Typical values are indicated. Worst case multipliers are applied to typical values.

Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Input Transition	Propagation Delays (in ns)						
				NDI (Fan-out)						
				1	2	4	8	16	32	
Non-Scan 4-bit Binary Synchronous Up/Down Counter (DU→CO)	C47	68	t_{PLH} , t_{PHL}	2.87 3.30	3.32 3.63	3.90 4.05	4.70 4.63	5.85 5.47	7.84 6.91	
4-bit Binary Full Adder with Fast Carry (CI→S1)	A4H	48	t_{PLH} , t_{PHL}	1.97 2.13	2.87 2.71	4.04 3.45	5.65 4.47	7.93 5.93	11.92 8.46	
4:1 Selector (S5→X)	T5A	5	t_{PLH} , t_{PHL}	1.39 1.12	2.33 1.77	3.55 2.62	5.23 3.79	7.62 5.45	11.79 8.35	
4-bit Shift Register with Synchronous Load	FS2	30	t_{PLH} , t_{PHL}	2.90 3.46	3.55 3.83	4.40 4.31	5.57 4.97	7.23 5.90	10.13 7.53	
9-bit Odd Parity Generator/Checker	P09	22	t_{PLH} , t_{PHL}	5.78 6.00	6.43 6.33	7.28 6.75	8.45 7.33	10.11 8.17	13.01 9.61	
4-wide 2:1 Data Selector (A→X)	P24	12	t_{PLH} , t_{PHL}	1.24 0.97	1.57 1.14	1.99 1.35	2.57 1.64	3.41 2.06	4.85 2.78	
4-bit Magnitude Comparator (IS→OG)	MC4	42	t_{PLH} , t_{PHL}	3.17 2.60	4.36 2.93	5.90 3.35	8.02 3.93	11.03 4.77	16.28 6.21	
4-bit Bus Driver (A→X)	B41	9	t_{PLH} , t_{PHL}	1.99 1.87	2.48 2.29	3.05 2.78	3.76 3.39	4.64 4.14	6.04 5.34	
Input Buffer (Inverter)	I1B	5	t_{PLH} , t_{PHL}	1.84 1.78	2.11 2.05	2.44 2.38	2.84 2.78	3.35 3.29	4.15 4.09	
Clock Input Buffer (Inverter)	IKB	4	t_{PLH} , t_{PHL}	2.49 1.94	2.63 2.08	2.79 2.24	2.99 2.44	3.24 2.69	3.64 3.09	
				Output Buffer Load in pF						
				12	25	50	100	200	400	
Output Buffer (True)	O2B	2	t_{PLH} , t_{PHL}	2.37 3.24	3.10 4.85	4.50 7.95	7.30 14.15	12.90 26.55	24.10 51.35	
Power Output Buffer (True)	O2L	2	t_{PLH} , t_{PHL}	2.53 2.47	3.02 3.01	3.94 4.03	5.79 6.08	9.49 10.18	16.89 18.38	
3-State Output Buffer (True)	O4T	4	t_{PLH} , t_{PHL}	3.09 4.08	3.82 5.77	5.22 9.02	8.02 15.52	13.62 28.52	24.82 54.52	
Power 3-State Output Buffer (True)	O4W	4	t_{PLH} , t_{PHL}	3.48 4.68	3.97 5.30	4.92 6.47	6.82 8.82	10.62 13.52	18.22 22.92	
3-State Output and Input Buffer (True)	H6T	8	t_{PLH} , t_{PHL}	3.09 4.08	3.82 5.77	5.22 9.02	8.02 15.57	13.62 28.52	24.82 54.52	
Power 3-State Output and Input Buffer (True)	H6W	8	t_{PLH} , t_{PHL}	3.48 4.68	3.97 5.30	4.92 6.47	6.82 8.82	10.62 13.52	18.22 22.92	

Note: Delays for inter-block wiring are not included

DC CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS¹**

Rating	Symbol	Minimum	Maximum	Unit	
Supply Voltage	V _{DD}	V _{SS} ² -0.5	6.0	V	
Input Voltage	V _I	V _{SS} ² -0.5	V _{DD} +0.5	V	
Output Voltage	V _O	V _{SS} ² -0.5	V _{DD} +0.5	V	
Output Current ³	I _{OL} =3.2mA	I _{OS}	-40	+40	
	I _{OL} =8mA		-40	+80	
	I _{OL} =12mA		-60	+120	
	I _{OL} =24mA		-90	+180	
Storage Temperature	Ceramic Plastic	T _{stg}	-65 -40	+150 +125	°C
Temperature Under Bias	Ceramic Plastic	T _{bias}	-40 -25	+125 +85	°C

Notes: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. V_{SS} = 0V.

3. Only one output at a time may be shorted for more than one second.

1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V _{DD}	4.75	5.0	5.25	V
Input High Voltage for TTL Input	V _{IH}	2.2	-	-	V
Input Low Voltage for TTL Input	V _{IL}	-	-	0.8	V
Input High Voltage for CMOS Input	V _{IH}	V _{DD} × 0.7	-	-	V
Input Low Voltage for CMOS Input	V _{IL}	-	-	V _{DD} × 0.3	V
Operating Temperature	T _A	0	-	70	°C

CAPACITANCE (T_A = 25°C, V_{DD} = V_I = 0V, f = 1 MHz)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Pin Capacitance	C _{IN}	-	-	16	pF
Output Pin Capacitance (I _{OL} =3.2mA, 8mA or 12mA)	C _{OUT}	-	-	16	pF
Output Pin Capacitance (I _{OL} =24mA)	C _{OUT}	-	-	18	pF
I/O Pin Capacitance (I _{OL} =3.2mA, 8mA or 12mA)	C _{I/O}	-	-	16	pF
I/O Pin Capacitance (I _{OL} =24mA)	C _{I/O}	-	-	23	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Current	I_{DDS}	Steady State ¹	0	—	100	μA
Output High Voltage for Normal Output ($I_{OL} = 3.2mA$)	V_{OH}	$I_{OH} = -2mA$	4.0	—	V_{DD}	V
Output High Voltage for Driver Output ($I_{OL} = 8mA$)	V_{OH}	$I_{OH} = -2mA$	4.0	—	V_{DD}	V
Output High Voltage for Driver Output ($I_{OL} = 12mA$)	V_{OH}	$I_{OH} = -4mA$	4.0	—	V_{DD}	V
Output High Voltage for Driver Output ($I_{OL} = 24mA$)	V_{OH}	$I_{OH} = -8mA$	4.0	—	V_{DD}	V
Output Low Voltage ² for Normal Output ($I_{OL} = 3.2mA$)	V_{OL}	$I_{OL} = 3.2mA$	V_{SS}	—	0.4	V
Output Low Voltage ² for Driver Output ($I_{OL} = 8mA$)	V_{OL}	$I_{OL} = 8mA$	V_{SS}	—	0.4	0V
Output Low Voltage ² for Driver Output ($I_{OL} = 12mA$)	V_{OL}	$I_{OL} = 12mA$	V_{SS}	—	0.4	0V
Output Low Voltage ² for Driver Output ($I_{OL} = 24mA$)	V_{OL}	$I_{OL} = 24mA$	V_{SS}	—	0.4	0V
Input High Voltage for TTL Input	V_{IH}	—	2.2	—	—	V
Input Low Voltage for TTL Input	V_{IL}	—	—	—	0.8	V
Input High Voltage for CMOS Input	V_{IH}	—	$V_{DD} \times 0.7$	—	—	V
Input Low Voltage for CMOS Input	V_{IL}	—	—	—	$V_{DD} \times 0.3$	V
Schmitt Trigger CMOS Input ³ Positive-going Threshold Negative-going Threshold Hysteresis	V_{T+} V_{T-} $V_{T+} - V_{T-}$	— $V_{IL} \text{ to } V_{IH}$ $V_{IH} \text{ to } V_{IL}$	2.5 0.7 1.1	3.3 1.4 1.9	4.0 2.0 2.7	V V V
Schmitt Trigger TTL Input ³ Positive-going Threshold Negative-going Threshold Hysteresis	V_{T+} V_{T-} $V_{T+} - V_{T-}$	— $V_{IL} \text{ to } V_{IH}$ $V_{IH} \text{ to } V_{IL}$	1.4 0.8 0.4	1.9 1.3 0.6	2.5 1.8 0.7	V V V
Input Pull-up/Pull-down Resistor	R_P	$V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$	25	50	100	$k\Omega$
Input Leakage Current	I_{LI}	$V_I = 0 - V_{DD}$	-10	—	10	μA
Input Leakage Current (3-state)	I_{LZ}	$V_I = 0 - V_{DD}$	-10	—	10	μA

Notes: 1. $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$

2. With certain restrictions on pin assignment

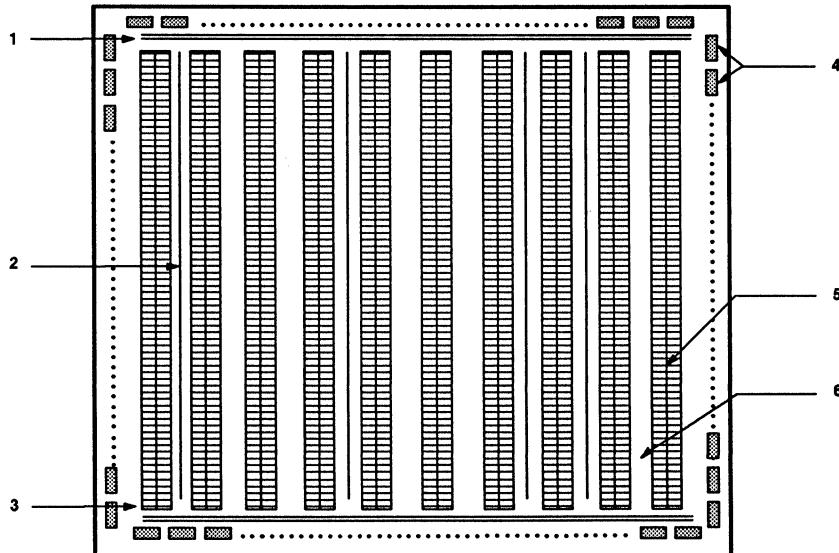
3. These values for reference only

ARRAY ARCHITECTURE

The typical UHB chip is composed of double columns of CMOS gates (basic cells) separated by dedicated wiring channels. A basic cell consists of a pair of N-channel and a pair of P-channel transistors interconnected by polysilicon gate control terminals. Groups of basic cells are interconnected by custom metalization into unit cells. Fujitsu unit cells provide a wide range of standard logic functions such as exclusive OR gates, flip-flops, buffers, and counters. The UHB Series CMOS Gate Array family includes over 250 different unit cells. These unit cells are the building blocks from which complex designs are constructed.

The spaces between the double columns of basic cells are occupied by channels for custom metalization. Nearly half of these wiring channels contain transmission gates that implement internal 3-state buses. Bus terminators located at the ends of the double columns of cells maintain the last value to be sent through the bus to ensure proper operation under all conditions.

The I/O cells around the perimeter of the matrix of cells are composed of internal cells with input protection networks and the potential to be configured as input buffers, clock input buffers, output buffers, power output buffers, or bidirectional buffers.



Typical Chip Layout, Double Column Structure

1. Dedicated Clock Network – for high frequency clocks
2. 3-state Bus Logic – located in wiring channels
3. Bus Terminators – prevent floating state on buses
4. Driver Transistors and I/O Protection Networks – provide high I/O count
5. Double Columns – for optional macro utilization and speed
6. Wiring Channel Area – for metalization between unit cells

DESIGN COMPONENTS

DESIGNING WITH THE UHB PRODUCT FAMILY

To implement logic functions, the designer builds up the elements of the circuit from unit cells. Simple unit cells are used hierarchically to build higher level functions until the logic is completely defined. Fujitsu offers a complete line of standard logic functions in the unit cell library.

Soft macros are used to implement large super-cell functions such as expandable ALU's and multipliers.

I/O BUFFERS

Each UHB I/O buffer around the perimeter of the array consists of an input protection network and large N-channel and P-channel transistors capable of supplying the standard 3.2-mA, 8-mA, and 12-mA output currents. Two of these large transistor pairs may be connected in parallel, using high-output-current macros, to obtain 24-mA drive. One of the I/O pads whose output transistors have been used for the 24-mA high-current option may still be used as an input.

Input I/O buffers convert external TTL levels to internal CMOS levels or may receive CMOS level signals directly. Output I/O buffers are totem pole and may drive either CMOS and TTL levels, depending on their AC and DC loads. Any of the pins except the dedicated power and ground pads can be designed to be an input buffer, an input buffer with pull-up/pull-down resistance, a clock input buffer, an output buffer, a high-drive output buffer, an output buffer with noise limiting resistance, a 3-state output buffer, a bi-directional buffer, or a Schmitt trigger input buffer. There are some restrictions on the location of 24-mA buffers.

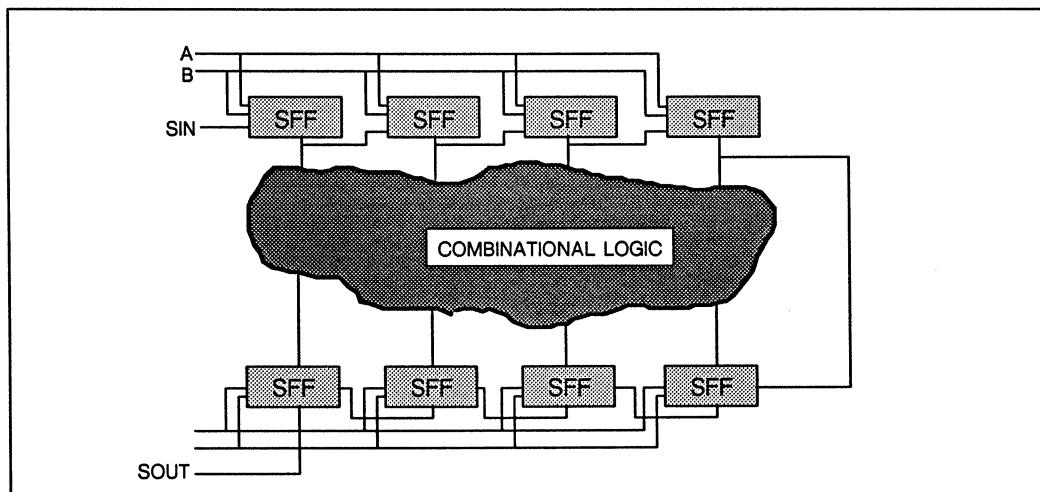
INPUT CLOCK DRIVERS

The large output I/O transistor pair is used in a high-drive input clock driver for high fanout applications within the array. This allows the designer to fully utilize the high speed capabilities of the UHB technology.

TESTING UHB DEVICES

Two options are available for testing UHB designs: (1) the standard designer-supplied test patterns and test vectors (in Fujitsu's FTDL format) and (2) the use of scan cells combined with Automatic Test Generation (ATG) performed by Fujitsu computers for additional diagnostic test patterns. If the designer has designed with scan cells and other scan logic elements, Fujitsu will complete the scan test program generation.

Regardless of the selected test option, it is the responsibility of the designer to furnish Fujitsu with enough test patterns to guarantee that the submitted design completely performs its intended logic functions. These patterns include the designer's test function of each I/O pin.



Diagrammatic Representation of Design Structure for Scan Testing

VDD and VSS REQUIREMENTS

Each UHB Series gate array device has two options for each package type, both supporting a different number of power and ground pins. The number of power and ground pins required depends on the number of simultaneously switching outputs used in the design. Simultaneously switching outputs (SSOs) are output signals that change from H to L or L to H or from Z to H or Z to L within a 20-ns window (including possible skew).

Multiple outputs that switch at the same time can cause noise on Vdd and Vss lines and affect the performance of a device. Therefore, to achieve maximum reliability, Fujitsu limits the number of SSOs per Vdd pin according to the table below. The maximum number of SSOs per pin is determined by a representative value specified for the driving capability of each type of output. The total representative value of all SSOs used in a design must not exceed 80 per Vss pin. For example, 11 normal 3.2-mA outputs with edge rate control, four 12-mA outputs, or three 24-mA outputs per Vss pin may be SSOs.

Output Drive Type	Representative Value per Output
Normal (3.2 mA)	10
High Drive (12 mA)	20
Normal (3.2 mA) with Edge Rate Control	7
High Drive (12 mA) with Edge Rate Control	14
High Drive (24 mA) with Edge Rate Control	26

ESTIMATION OF POWER DISSIPATION

In order to select a suitable ASIC package and determine system cooling requirements and system power supply requirements, the designer needs to estimate the power dissipation of the circuit.

Power dissipation calculation in CMOS technologies is complicated by the fact that transient currents involved in charging and discharging capacitances dominate the total power dissipation.

Fujitsu has simplified the calculation of power dissipation by studying a long history of designs to determine what typical circuit activity constitutes, and by observing the power dissipation characteristics of individual gates as they operate. These parameters are summarized below and are incorporated into the worksheet that follows.

$$\begin{aligned} P_{d(in)} &= 0.073 \text{mW/MHz} \\ P_{d(out)} &= 0.025 \text{mW/pF} \\ P_{d(seq)} &= 0.20 \text{mW/MHz} \\ P_{d(comb)} &= 0.033 \text{mW/MHz} \\ C^V(5V \pm 5\%) &= 1.11 \end{aligned}$$

The example below assumes a system clock frequency (f) of 25 MHz for a circuit of 2700 gates with 90 inputs and 50 outputs, all outputs loaded at 20 pF. The circuit activity, that is, the maximum number of internal gates, inputs, and outputs that are simultaneously active, is 20%. The mix of sequential to combinational gates is 1:5 (20%).

Note: P is in units of mW/MHz, except $P_{d(out)}$, which is in mW/MHz/pF.

1.0 I/O AC POWER CALCULATION

$$1.1 \text{ Number of inputs } 90 \times \text{freq } 25/2 \times P_{d(in)} \times 20\% = 16.43 \text{ mW}$$

$$1.2 \text{ Number of outputs } 50 \times \text{freq}^1 25/4 \times \text{load } 20F \times P_{d(out)} \times 20\% = 31.25 \text{ mW}$$

$$1.3 \text{ Total I/O AC (transient) Power} \dots \boxed{PAC = 47.68 \text{ mW}}$$

2.0 I/O DC POWER CALCULATION

$$2.1 \text{ Number of 3.2 mA outputs}^2 34 \times (0.15 \times (I_{OL} + I_{OH})) = 26.52 \text{ mW}$$

$$2.2 \text{ Number of 8 mA outputs } 16 \times (0.15 (I_{OL} + I_{OH})) = 24 \text{ mW}$$

$$2.3 \text{ Number of 12 mA outputs } 0 \times (0.15 (I_{OL} + I_{OH})) = 0 \text{ mW}$$

$$2.4 \text{ Number of 24 mA outputs } 0 \times (0.15 (0.15 \times (I_{OL} + I_{OH}))) = 0 \text{ mW}$$

$$2.5 \text{ Total I/O DC (steady state) Power} \dots \boxed{PDC = 50.52 \text{ mW}}$$

3.0 INTERNAL GATE POWER CALCULATION

$$3.1 \text{ Number of used gates } 2700 \times \% \text{ seq. } 20\% \times \text{freq } 25/8 \times P_{d(seq)} = 337.5 \text{ mW}$$

$$3.2 \text{ Number of used gates } 2700 \times \% \text{ comb. } 80\% \times \text{freq}^3 25/20 \times P_{d(comb)} = 89.1 \text{ mW}$$

$$3.3 \text{ Total Internal Gate Transient Power} \dots \boxed{PINT = 426.6 \text{ mW}}$$

4.0 TOTAL CHIP ESTIMATED POWER DISSIPATION

$$4.1 P_t (\text{typical}) = PAC \ 47.68 \text{ mW} + PDC \ 50.52 \text{ mW} + PINT \ 426.6 \text{ mW} = 524.8 \text{ mW}$$

$$4.2 P_D(\text{worst case}) = P_t = 524.8 \text{ mW} \times C_V \ 1.11 = 582.5 \text{ mW} = .6W \text{ W}$$

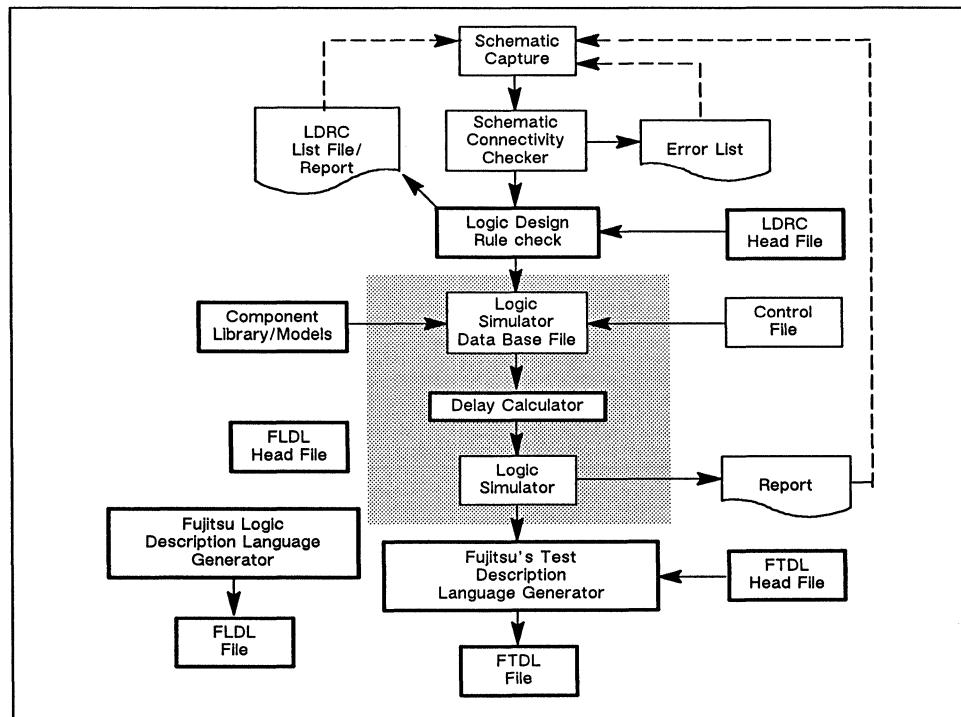
- Notes:**
1. It is assumed that outputs will toggle at one fourth the frequency of the system clock on the average.
 2. The $(I_{OL} + I_{OH})$ term assumes outputs are symmetrically high and low.
 3. It is assumed that only 20% of the combinational gates are simultaneously active, and at a frequency of one fourth the clock frequency.

WORKSTATION DESIGN FLOW

Fujitsu ASICs customers have a choice of four popular CAE design packages (Daisy, Mentor, Valid, and HP 9000) plus Fujitsu's own new Sun-based workstation software (ViewCAD) for schematic capture and design implementation. The design flow process is summarized in the diagram below. The boxes outlined in bold indicate Fujitsu-supplied software that integrates with standard CAE software to produce the data files necessary to implement a design. The design process flowchart is somewhat simpler for the Fujitsu (ViewCAD) software because ViewCAD was written specifically for Fujitsu's high-reliability design process.

A design logic file and a test data file, known as Fujitsu Logic Design Language (FLDL) and Fujitsu Test Design Language (FTDL), are the ultimate result of the workstation design process.

1

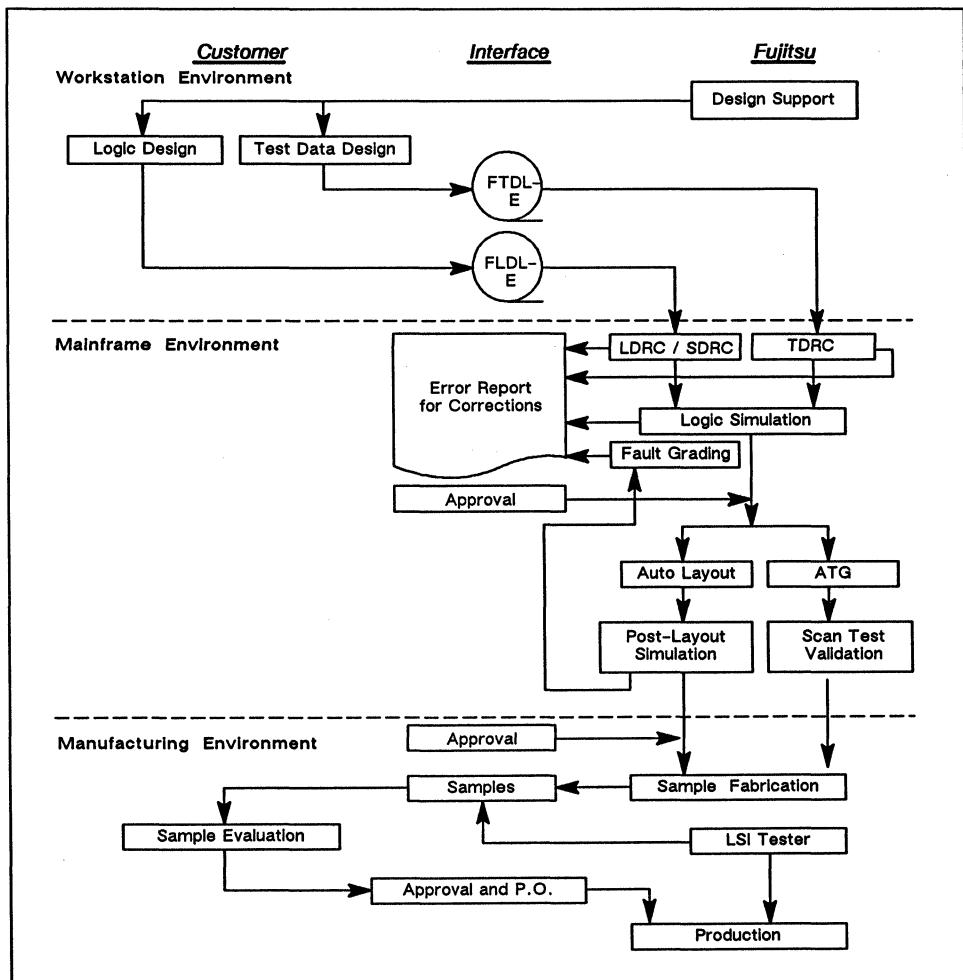


Workstation Design Process

DESIGN IMPLEMENTATION FLOW

After the workstation design process is complete, the FLDL and FTDL files are transferred to the mainframe environment at one of Fujitsu's Technical Resource Centers. There, the FLDL file is checked by the Logic Design Rule Check (LDRC) and a pre-layout simulation is made using the test data generated in FTDL. Then, after automated layout takes place, simulation is run to validate the LSI function.

When the design data is validated, the design files are sent to the prototype manufacturing area where mask sets are fabricated and engineering sample devices are manufactured for test and approval. After the engineering samples are fully tested and signed off, full production can begin.



Post-Design Process

FUNCTIONAL INDEX OF UNIT CELL LIBRARY

Note: The load unit (ℓ_u) is a normalized loading unit of capacitance representing the input load of an inverter without metal interconnection.

Inverter and Buffer Family				
Unit Cell Name	Description	Basic Cells	Drive (ℓ_u)	Polarity
V1N	Inverter	1	18	Neg
V2B	Power Inverter	1	36	Neg
V1L	Double Power Inverter	2	55	Neg
B1N	True Buffer	1	18	Pos
BD3	True Delay Buffer (> 5ns)	5	18	Pos
BD4	Delay Cell (> 4ns)	4	6	Pos
BD5	Delay Cell (>10ns)	9	18	Pos
BD6	Delay Cell (>22ns)	17	18	Pos
Clock Buffer Family				
Unit Cell Name	Description	Basic Cells	Drive (ℓ_u)	Polarity
K1B	True Clock Buffer	2	36	Pos
K2B	Power Clock Buffer	3	55	Pos
K3B	Gated Clock (AND) Buffer	2	36	Pos
K4B	Gated Clock (OR) Buffer	2	36	Pos
K5B	Gated Clock (NAND) Buffer	3	36	Neg
KAB	Block Clock (OR) Buffer	3	55	Pos
KBB	Block Clock (OR x 10) Buffer	30	55	Pos
NAND Family				
Unit Cell Name	Description	Basic Cells	Drive (ℓ_u)	
N2N	2-Input NAND	1	18	
N2B	Power 2-Input NAND	3	36	
N2K	Fast Power 2-Input NAND	2	36	
N3N	3-Input NAND	2	14	
N3B	Power 3-Input NAND	3	36	
N4N	4-input NAND	2	10	
N4B	Power 4-Input NAND	4	36	
N6B	Power 6-Input NAND	5	36	
N8B	Power 8-Input NAND	6	36	
N9B	Power 9-Input NAND	8	36	
NCB	Power 12-Input NAND	10	36	
NGB	Power 16-Input NAND	11	36	
N3K	Fast Power 3-input NAND	3	36	
N4K	Fast Power 4-Input NAND	4	36	

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

NOR Family				
Unit Cell Name	Description	Basic Cells	Drive (μ)	
R2N	2-Input NOR	1	14	
R2B	Power 2-Input NOR	3	36	
R2K	Power 2-input NOR	2	36	
R3N	3-Input NOR	2	10	
R3B	Power 3-Input NOR	3	36	
R3K	Power 3-input NOR	3	36	
R4N	4-Input NOR	2	6	
R4B	Power 4-Input NOR	4	36	
R4K	Power 4-input NOR	4	36	
R6B	Power 6-Input NOR	5	36	
R8B	Power 8-Input NOR	6	36	
R9B	Power 9-Input NOR	8	36	
RCB	Power 12-Input NOR	10	36	
RGB	Power 16-Input NOR	11	36	

AND Family				
Unit Cell Name	Description	Basic Cells	Drive (μ)	
N2P	Power 2-Input AND	2	36	
N3P	Power 3-Input AND	3	36	
N4P	Power 4-Input AND	3	36	
N8P	Power 8-Input AND	6	36	

OR Family				
Unit Cell Name	Description	Basic Cells	Drive (μ)	
R2P	Power 2-Input OR	2	36	
R3P	Power 3-Input OR	3	36	
R4P	Power 4-Input OR	3	36	
R8P	Power 8-Input OR	6	36	

Exclusive NOR/OR Family (EXOR/EXNOR)				
Unit Cell Name	Description	Basic Cells	Drive (μ)	Polarity
X1N	Exclusive NOR	3	18	Neg
X1B	Power Exclusive NOR	4	36	Neg
X2N	Exclusive OR	3	14	Pos
X2B	Power Exclusive OR	4	36	Neg
X3N	3-Input Exclusive NOR	5	14	Neg
X3B	Power 3-Input Exclusive NOR	6	36	Neg
X4N	3-Input Exclusive OR	5	14	Pos
X4B	Power 3-Input Exclusive OR	6	36	Pos

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

AND-OR-Inverter Family (AOI)					
Unit Cell Name	Description		Basic Cells	Drive (μ A)	
D23	2 AND into 2 NOR AOI		2	14	
D14	3 AND into 2 NOR AOI		2	14	
D24	2, 2 AND into 2 NOR AOI		2	14	
D34	2 AND into 3 NOR AOI		2	10	
D36	3, 2 AND into 3 NOR AOI		3	10	
D44	2 OR into 2 AND into 2 NOR AOI		2	10	

Note: AND-OR-Invert unit cells are useful in implementing sum-of-products (SOP) expressions.

OR-AND-Inverter Family (OAI)					
Unit Cell Name	Description		Basic Cells	Drive (μ A)	
G23	2 OR into 2 NAND OAI		2	18	
G14	3 OR into 2 NAND OAI		2	10	
G24	2, 2 OR into 2 NAND OAI		2	10	
G34	2 OR into 3 NAND OAI		2	10	
G44	2 AND into 2 OR into 2 NAND OAI		2	14	

Note: OR-AND-Invert unit cells are useful in implementing product-of-sums (POS) expressions.

Multiplexer Family					
Unit Cell Name	Type	Description	Basic Cells	Drive (μ A)	Function
T24*	4:1	Power 4, 2 ANDs into 4 NOR Multiplexer	6	36	SOP
T26*	6:1	Power 6, 2 ANDs into 6 NOR Multiplexer	10	36	SOP
T28*	8:1	Power 8, 2 ANDs into 8 NOR Multiplexer	11	36	SOP
T32	2:1	Power 2, 3 ANDs into 2 NOR Multiplexer	5	36	SOP
T33*	3:1	Power 3, 3 ANDs into 3 NOR Multiplexer	7	36	SOP
T34*	4:1	Power 4, 3 ANDs into 4 NOR Multiplexer	9	36	SOP
T42	2:1	Power 2, 4 ANDs into 2 NOR Multiplexer	6	36	SOP
T43	3:1	Power 3, 4 ANDs into 3 NOR Multiplexer	10	36	SOP
T44	4:1	Power 4, 4 ANDs into 4 NOR Multiplexer	11	36	SOP
T54	4:1	Power 2, 2-3-4 ANDs into 4 NOR Multiplexer	10	36	SOP
U24*	4:1	Power 4, 2 OR into 4 NAND Multiplexer	6	36	POS
U26*	6:1	Power 6, 2 OR into 6 NAND Multiplexer	9	36	POS
U28*	8:1	Power 8, 2 OR into 8 NAND Multiplexer	11	36	POS
U32	2:1	Power 2, 3 OR into 2 NAND Multiplexer	5	36	POS
U33*	3:1	Power 3, 3 OR into 3 NAND Multiplexer	7	36	POS
U34*	4:1	Power 4, 3 OR into 4 NAND Multiplexer	9	36	POS
U42	2:1	Power 2, 4 OR into 2 NAND Multiplexer	6	36	POS
U43	3:1	Power 3, 4 OR into 3 NAND Multiplexer	9	36	POS
U44	4:1	Power 4, 4 OR into 4 NAND Multiplexer	11	36	POS

* Convenient for typical multiplexer applications

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Data Selectors/Multiplexers							
Unit Cell Name	Type	Description	Basic Cells	Drive (f <u>u</u>)	Selects	Output	Bit Width
P24*	2:1	Data Selector	12	36	S, XS	Q	4
T2E	2:1	Selector	5	18	S	XQ	2
T2F	2:1	Selector	8	18	S	XQ	4
T2B*	2:1	Selector	2	18	S, XS	XQ	1
T2C*	2:1	Selector	4	18	S, XS	XQ	2
T2D*	2:1	Selector	2	14	S, XS	XQ	1
T5A*	4:1	Selector	8	9	S, XS	XQ	1
V3A*	1:2	Selector	2	14	S, XS	XQ	1
V3B*	1:2	Selector	4	14	S, XS	XQ	2

* These are transmission gate devices whose outputs can be tied because they can be inhibited with true/inverted selects.

Decoders							
Unit Cell Name	Type	Description	Basic Cells	Drive (f <u>u</u>)	Active Level Outputs	Enable	
DE2	2:4	Decoder	5	18	Low	—	
DE3	3:8	Decoder	15	14	Low	—	
DE4	2:4	Decoder	8	14	Low	Low	
DE6	3:8	Decoder	30	18	Low	1 High 2 Low	

Internal Bus Unit Cells							
Unit Cell Name	Type	Description	Basic Cells	Drive (f <u>u</u>)	Bus Size	Enable	
B41	4-bit Bus Driver		9	36	4 bits	Low	

Notes:

1. The number of B41s used is limited by the chosen array series, as shown in the table below.
2. On-chip buses (managing more than one bus source and/or a bi-directional bus) may be implemented with either multiplexer-type unit cells or bus drivers. While bus drivers impose certain design restrictions, the optimum choice is dictated by the specific design.

Device Name	Maximum B41s
C-330UHB	4
C-530UHB	5
C-830UHB	6
C-1200UHB	8
C-1700UHB	12
C-2200UHB	16
C-3000UHB	21
C-4100UHB	26
C-6000UHB	50

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Data Latch Family

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Enable	Bits	Output	Clear
YL2	Data Latch with TM	5	36	High	1	Q	—
YL4	Data Latch with TM	14	36	High	4	Q	—
LTK	Data Latch	4	18	Low	1	Q, XQ	Async
LTL	Data Latch with Clear	5	18	Low	1	Q, XQ	Async
LTM	Data Latch with Clear	16	18	Low	4	Q, XQ	—
LT1	S-R Latch with Clear	4	18	Low	1	Q, XQ	Async
LT4	Data Latch	14	18	Low	4	Q, XQ	—

Note: Y-type latches incorporate inhibit inputs and transparent mode (TM) to facilitate scan implementation.

Scan-Flip-Flop Family (Positive-Edge Triggered)

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Bits	Output	Clear	Preset	Clock Inhibit
SDH*	Scan D FF with 2:1 Multiplex	14	36	1	Q, XQ	Async	—	Yes
SDJ*	Scan D FF with 4:1 Multiplex	15	36	1	Q, XQ	Async	—	Yes
SDK*	Scan D FF with 3:1 Multiplex	16	36	1	Q, XQ	Async	—	Yes
SJH	Scan J-K FF	16	36	1	Q, XQ	Async	—	Yes
SDD*	Scan DFF with 2:1 Multiplex	16	36	1	Q, XQ	Async	Async	Yes
SDA	Scan 1-Input D FF	12	36	1	Q, XQ	—	—	Yes
SDB	Scan 1-Input D FF	42	36	4	Q, XQ	—	—	Yes
SHA	Scan 1-Input D FF	68	18	8	Q, XQ	—	—	Yes
SHB	Scan 1-Input D FF	62	18	8	Q	—	—	Yes
SHC	Scan 1-Input D FF	62	18	8	XQ	—	—	Yes
SHJ*	Scan D FF with 2:1 Multiplex	78	18	8	Q, XQ	—	—	Yes
SHK*	Scan D FF with 3:1 Multiplex	88	18	8	Q, XQ	—	—	Yes

Note: * Indicates D Flip-Flop with multiplexed inputs.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Non-SCAN Flip-Flop Family								
Unit Cell Name	Description	Basic Cells	Drive (ℓ_u)	Bits	Outputs	Clear	Preset	Clock Edge
FDN	Non-Scan D FF with Set	7	18	1	Q, XQ	—	Async	Pos
FDM	Non-Scan D F	6	18	1	Q, XQ	—	—	Pos
FDO	Non-Scan D FF with Reset	7	18	1	Q, XQ	Async	—	Pos
FDP	Non-Scan D FF with Set and Reset	8	18	1	Q, XQ	Async	Async	Pos
FDQ	Non-Scan D FF	21	18	4	Q	—	—	Neg
FDR	Non-Scan D FF with Clear	26	18	4	Q	Async	—	Pos
FDS	Non-Scan D FF	20	18	4	Q	—	—	Pos
FD2	Non-Scan Power D FF	7	36	1	Q, XQ	—	—	Neg
FD3	Non-Scan Power D FF with Preset	8	36	1	Q, XQ	—	Async	Neg
FD4	Non-Scan Power D FF with Clear and Preset	9	36	1	Q, XQ	Async	Async	Neg
FD5	Non-Scan Power D FF with Clear	8	36	1	Q, XQ	Async	—	Neg
FJD	Non-Scan Positive Edge Clocked Power J-K FF with Clear	12	36	1	Q, XQ	Async	—	Pos

Note: Synchronous flip-flops may be constructed by adding a simple AND gate (such as N2P) to the input of a flip-flop to create a synchronous clear.

Binary Counter Family										
Unit Cell Name	Description	Basic Cells	Drive (ℓ_u)	Bits	Outputs ¹	Load	Clear	Enable	Carry In	Up/Down
SC7 ²	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62	36	4	Q, XQ, CO (S)	Sync	—	Low	High	Up
SC8 ²	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66	36	4	Q, XQ, CO (S)	Sync	—	High	Low	Down
C11 ³	Non-Scan Flip-Flop for Counter	11	18	—	Q, XQ	—	—	—	—	—
C41	Non-Scan 4-bit Binary Asynchronous Counter	24	18	4	Q, (A)	—	Async	—	—	Up
C42	Non-Scan 4-bit Binary Synchronous Counter	32	18	4	Q	—	Async	—	—	Up
C43	Non-Scan 4-bit Binary Synchronous Up Counter	48	18	4	Q, CO(S)	Sync	Async	High	High	Up
C45	Non-Scan Binary Synchronous Up Counter	48	18	4	Q, CO	Sync	Sync	High	High	Up
C47	Non-Scan Binary Synchronous Up/Down Counter	68	18	4	Q, CO	Async	—	Low	Low	Up/Down

Notes: 1. (S), (A) indicate the counter is (S)ynchronous or (A)synchronous.
 2. Scan counters include clock inhibit and high drive (CDR = 36 ℓ_u). For non-Scan counters CDR = 18 ℓ_u .
 3. C11 may be used for purposes other than counters.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Shift Register Family							
Unit Cell Name	Description	Basic Cells	Drive (ℓ_u)	Bit Width	Load	Outputs	Clock Polarity
FS1	Serial-In Parallel-out Shift Register	18	16	4	Serial-In only	Q-Parallel	Neg
FS2	Shift Register with Synchronous Load	30	16	4	Sync-High	Q-Parallel	Neg
FS3	Shift Register with Asynchronous Load	34	18	4	Async-Low	Q-Parallel	Pos
SR1	Serial-In Parallel-out Shift Register with Scan	36	36	4	Serial-In only	Q-Parallel	Pos

Datapath Operators (Adder, ALU, Parity)							
Unit Cell Name	Description	Basic Cells	Drive (ℓ_u)	Bit Width	Outputs	Carry In	
MC4	Magnitude Comparator	42	$18(=)$ $10(<,>)$	4	A>B, A=B, A<B	A>B,A=B,ALB	
A1A	1-bit Half Adder	5	36	1	S, CO	—	
A1N	1-bit Full Adder	8	18	1	S, CO	CI	
A2N	2-bit Full Adder	16	14	2	S, CO	CI	
A4H	4-bit Binary Full Adder w/Fast Carry	48	$18(CO)$ $14(S)$	4	S, CO	CI	
PE5	Even Parity Generator/Checker	12	36	5	EVEN, ODD	—	
PO5	Odd Parity Generator/Checker	12	36	5	ODD, EVEN	—	
PE8	Even Parity Generator/Checker	18	18	8	EVEN, ODD	—	
PO8	Odd Parity Generator/Checker	18	18	8	ODD, EVEN	—	
PE9	Even Parity Generator/Checker	22	18	9	EVEN, ODD	—	
PO9	Odd Parity Generator/Checker	22	18	9	ODD, EVEN	—	

Miscellaneous Cells							
Unit Cell Name	Description	Basic Cells	Function				
Z00	0 Clip	0	Tie to VSS				
Z01	1 Clip	0	Tie to VDD				

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Input Buffer Family						
Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Logic Level	Type	Input/Output Polarity
I1B	Input Buffer	5	36	TTL	Signal	Invert
I1BU	I1B with Pull-up Resistance	5	36	TTL	Signal	Invert
I1BD	I1B with Pull-down Resistance	5	36	TTL	Signal	Invert
I2B	Input Buffer	4	36	TTL	Signal	True
I2BU	I2B with Pull-up Resistance	4	36	TTL	Signal	True
I2BD	I2B with Pull-down Resistance	4	36	TTL	Signal	True
IKB	Clock Input Buffer	4	72	TTL	Clock	Invert
IKBU	IkB With Pull-up Resistance	4	72	TTL	Clock	Invert
IKBD	IKB with Pull-down Resistance	4	72	TTL	Clock	Invert
ILB	Clock Input Buffer	6	72	TTL	Clock	True
ILBU	ILB with Pull-up Resistance	6	72	TTL	Clock	True
ILBD	ILB with Pull-down Resistance	6	72	TTL	Clock	True
I1C	CMOS Interface Input Buffer	5	36	CMOS	Signal	Invert
I1CU	I1C with Pull-up Resistance	5	36	CMOS	Signal	Invert
I1CD	I1C with Pull-down Resistance	5	36	CMOS	Signal	Invert
I2C	CMOS Interface Input Buffer	4	36	CMOS	Signal	True
I2CU	I2C with Pull-up Resistance	4	36	CMOS	Signal	True
I2CD	I2C with Pull-down Resistance	4	36	CMOS	Signal	True
I1S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	Invert
I1SU	I1S with Pull-up Resistance	8	18	CMOS	Schmitt	Invert
I1SD	I1S with Pull-down Resistance	8	18	CMOS	Schmitt	Invert
I2S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	True
I2SU	I2S with Pull-up Resistance	8	18	CMOS	Schmitt	True
I2SD	I2S with Pull-down Resistance	8	18	CMOS	Schmitt	True
I1R	Schmitt Trigger Input Buffer	6	18	TTL	Schmitt	Invert
I1RU	I1R with Pull-up Resistance	6	18	TTL	Schmitt	Invert
I1RD	I1R with Pull-down Resistance	6	18	TTL	Schmitt	Invert
I2R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	True
I2RU	I2R With Pull-up Resistance	8	18	TTL	Schmitt	True
I2RD	I2R with Pull-down Resistance	8	18	TTL	Schmitt	True

Note: A "U" suffixed to the name of an input buffer indicates pull-up resistance of $50\text{K}\Omega$ (typical) and a "D" indicates a pull-down resistance of the equivalent value.

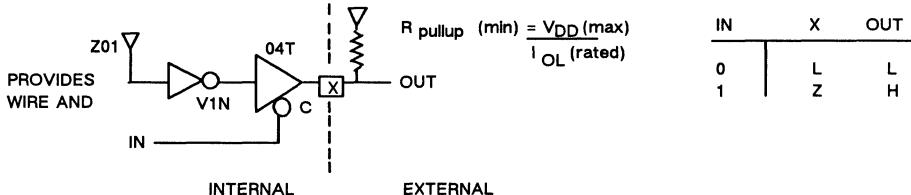
FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Output Buffer Family

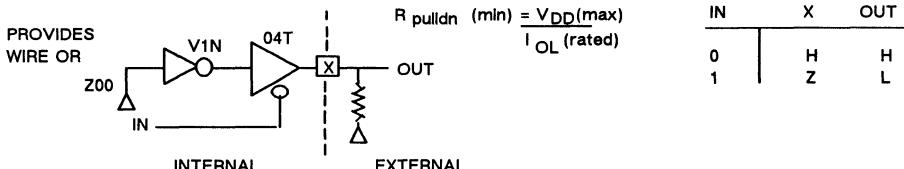
Unit Cell Name	Description	Basic Cells	Drive (I _{OL})	Logic ^a Level	Type	Edge Rate Control	Input/Output Polarity
O1B	Output Buffer	3	3.2mA	TTL/CMOS	Standard	No	Invert
O1L	Power Output Buffer	3	12mA	TTL/CMOS	Standard	No	Invert
O1S	Power Output Buffer	5	12mA	TTL/CMOS	Standard	Yes	Invert
O2B	Output Buffer	2	3.2mA	TTL/CMOS	Standard	No	True
O2L	Power Output Buffer	2	12mA	TTL/CMOS	Standard	No	True
O2S	Power Output Buffer	4	12mA	TTL/CMOS	Standard	Yes	True
O4T ¹	Output Buffer	4	3.2mA	TTL/CMOS	3-state	No	True
O4W ¹	Power 3-state Output Buffer	4	12mA	TTL/CMOS	3-state	No	True
O4S ¹	Power 3-state Output Buffer	5	12mA	TTL/CMOS	3-state	Yes	True
O1R	Output Buffer	5	3.2mA	TTL/CMOS	Standard	Yes	Invert
O2R	Output Buffer	4	3.2mA	TTL/CMOS	Standard	Yes	True
O4R ¹	Output Buffer	5	3.2mA	TTL/CMOS	3-state	Yes	True
O2S2	High Power Output Buffer	6	24mA	TTL/CMOS	Standard	Yes	True
O4S2 ¹	High Power Output Buffer	7	24mA	TTL/CMOS	3-state	Yes	True
O1BF	Output Buffer	3	8mA	TTL/CMOS	Standard	No	Invert
O1RF	Output Buffer	5	8mA	TTL/CMOS	Standard	Yes	Invert
O2BF	Output Buffer	2	8mA	TTL/CMOS	Standard	No	True
O2RF	Output Buffer	4	8mA	TTL/CMOS	Standard	Yes	True
O4RF	3-state Output Buffer	5	8mA	TTL/CMOS	3-state	Yes	True
O4TF	3-state Output Buffer	4	8mA	TTL/CMOS	3-state	No	True

Note: 1. While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs.

EXAMPLE OF OPEN DRAIN OUTPUT



EXAMPLE OF OPEN SOURCE OUTPUT



Note: 2. Totem pole outputs, such as these buffers have, can drive both TTL and CMOS levels. Voltage margins depend on actual source or sink current (see DC specifications).

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectional I/O Buffers (Buses)						
Unit Cell Name	Description	Basic Cells	Drive (IOL)	Logic Level	Edge Rate Control	Input/Output Polarity
H6T	3-state Output and Input Buffer	8	3.2mA	TTL	No	True
H6TU	H6T with Pull-up Resistance	8	3.2mA	TTL	No	True
H6TD	H6T with Pull-down Resistance	8	3.2mA	TTL	No	True
H6W	Power 3-state Output and Input Buffer	8	12mA	TTL	No	True
H6WU	H6W with Pull-up Resistance	8	12mA	TTL	No	True
H6WD	H6W with Pull-down Resistance	8	12mA	TTL	No	True
H6C	3-state Output and CMOS Interface Input Buffer	8	3.2mA	CMOS	No	True
H6CU	H6C with Pull-up Resistance	8	3.2mA	CMOS	No	True
H6CD	H6C with Pull-down Resistance	8	3.2mA	CMOS	No	True
H6E	Power 3-state Output and CMOS Interface Input Buffer	8	12mA	CMOS	No	True
H6EU	H6E with Pull-up Resistance	8	12mA	CMOS	No	True
H6ED	H6E with Pull-down Resistance	8	12mA	CMOS	No	True
H6S	3-state Output and Schmitt Trigger Input Buffer	12	3.2mA	CMOS	No	True
H6SU	H6S with Pull-up Resistance	12	3.2mA	CMOS	No	True
H6SD	H6S with Pull-down Resistance	12	3.2mA	CMOS	No	True
H6R	3-state Output and Schmitt Trigger Input Buffer	12	3.2mA	TTL	No	True
H6RU	H6R with Pull-up Resistance	12	3.2mA	TTL	No	True
H6RD	H6R with Pull-down Resistance	12	3.2mA	TTL	No	True
H8T	3-state Output and Input Buffer	9	3.2mA	TTL	Yes	True
H8TU	H8T with Pull-up Resistance	9	3.2mA	TTL	Yes	True
H8TD	H8T with Pull-down Resistance	9	3.2mA	TTL	Yes	True
H8W	Power 3-state Output and Input Buffer	9	12mA	TTL	Yes	True
H8WU	H8W with Pull-up Resistance	9	12mA	TTL	Yes	True
H8WD	H8W with Pull-down Resistance	9	12mA	TTL	Yes	True
H8W2	High Power 3-state Output and Input Buffer	11	24mA	TTL	Yes	True
H8W1	H8W2 with Pull-up Resistance	11	24mA	TTL	Yes	True
H8W0	H8W2 with Pull-down Resistance	11	24mA	TTL	Yes	True
H8C	3-state Output Buffer and CMOS Interface Input Buffer	9	3.2mA	CMOS	Yes	True
H8CU	H8C with Pull-up Resistance	9	3.2mA	CMOS	Yes	True
H8CD	H8C with Pull-down Resistance	9	3.2mA	CMOS	Yes	True

Note: A "U" suffixed to the name of a bidirectional buffer indicates a pull-up resistance of 50Ω (typical) and a "D" indicates a pull-down resistance of the equivalent value.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectional I/O Buffers (Buses) continued						
Unit Cell Name	Description	Basic Cells	Drive (IOL)	Input Logic Level	Edge Rate Control	Input/Output Polarity
H8E	Power 3-state Output Buffer and Interface Input Buffer	9	12mA	CMOS	Yes	True
H8EU	H8E with Pull-up Resistance	9	12mA	CMOS	Yes	True
H8ED	H8E with Pull-down Resistance	9	12mA	CMOS	Yes	True
H8E2	High Power 3-state Output and Input Buffer	11	24mA	CMOS	Yes	True
H8E1	H8E2 with Pull-up Resistance	11	24mA	CMOS	Yes	True
H8E0	H8E2 with Pull-down Resistance	11	24mA	CMOS	Yes	True
H8S	3-state Output and Schmitt Trigger Input Buffer	13	3.2mA	CMOS	Yes	True
H8SU	H8S with Pull-up Resistance	13	3.2mA	CMOS	Yes	True
H8SD	H8S with Pull-down Resistance	13	3.2mA	CMOS	Yes	True
H8R	3-state Output and Schmitt Trigger Input Buffer	13	3.2mA	TTL	Yes	True
H8RU	H8R with Pull-up Resistance	13	3.2mA	TTL	Yes	True
H8RD	H8R with Pull-down Resistance	13	3.2mA	TTL	Yes	True
H6TF	3-state Output and Schmitt Trigger Input Buffer	8	8mA	TTL	No	True
H6TFU	H6TF with Pull-up Resistance	8	8mA	TTL	No	True
H6TFD	H6TF with Pull-down Resistance	8	8mA	TTL	No	True
H6CF	3-state Output and Input Buffer	8	8mA	CMOS	No	True
H6CFU	H6CF with Pull-up Resistance	8	8mA	CMOS	No	True
H6CFD	H6CF with Pull-down Resistance	8	8mA	CMOS	No	True
H8TF	3-state Output and Input Buffer	9	8mA	TTL	Yes	True
H8TFU	H8TF with Pull-up Resistance	9	8mA	TTL	Yes	True
H8TFD	H8TF with Pull-down Resistance	9	8mA	TTL	Yes	True
H8CF	3-state Output and Input Buffer	9	8mA	CMOS	Yes	True
H8CFU	H8CF with Pull-up Resistance	9	8mA	CMOS	Yes	True
H8CFD	H8CF with Pull-down Resistance	9	8mA	CMOS	Yes	True
Note: While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs, which includes all bidirectional buffers.						
Oscillator Circuits						
Unit Cell Name	Description	Basic Cells	Input Logic Level			
HOC	Output Buffer for Oscillator and Input Buffer	8	CMOS			
HOCS	Output Buffer for Oscillator and Schmitt Trigger Input Buffer	8	TTL			
HOCR	Output Buffer for Oscillator with feedback Resistance	8	CMOS			
IT1O	Input Buffer for Oscillator	0	—			

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Availability Characteristics of UHB Gate Array Packages

Dual In-line Packages (Standard DIP)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
DIP-16	DIP-16P-MO2	DIP-16C-C03	1	2	13
	DIP-16P-MO4				
DIP-18	DIP-18P-MO1	DIP-18C-C01			
	DIP-18P-MO2				
DIP-20	DIP-20P-MO2	DIP-20C-C02	1	2	17
DIP-20U			1	1	18
DIP-22	DIP-22P-MO2	DIP-22C-C02	2	2	18
	DIP-22P-MO3				
DIP-22U			1	1	20
DIP-24	DIP24P-MO1	DIP-24C-C01	2	2	20
	DIP24P-MO2				
DIP-24U			1	1	22
DIP-28	DIP-28P-M02	DIP-28C-C02	2	2	24
	DIP-28P-M03				
DIP-28U			1	1	26
DIP-40	DIP-40P-M01	DIP-40C-A01	2	4	34
		DIP-40C-A02			
DIP-40U			1	1	38
DIP-42	DIP-42P-MO1	DIP-42C-A01	2	4	36
	DIP-42P-MO2				
DIP-42U			1	1	40
DIP-48	DIP-48P-MO1	DIP-48C-A01	2	4	42
	DIP-48P-MO2				
DIP-48U			1	1	46
Dual In-line Packages (Shrink DIP, 70 mil Pin Pitch)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
DIP-28SH			2	2	24
DIP-28SHU			1	1	26
DIP-42SH			2	4	36
DIP-42SHU			1	1	40
DIP-48SH			2	4	36
DIP-48SHU			1	1	46
DIP-64SH			2	4	58
DIP-64SHU			2	2	60

Subject to Change

MB62xxxx
MB60xxxx



Availability Characteristics of UHB Gate Array Packages

Dual In-line Packages (Skinny DIP, 300mil Body Width)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
DIP-22SK			2	2	18
DIP-22SKU			1	1	20
DIP-24SK			2	2	20
DIP-24SKU			1	1	22
DIP-28SK			2	2	24
DIP-28SKU			1	1	26
Flatpack Packages (Dual-Leaded)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
FPT-16	FPT-16P-MO3		1	2	13
FPT-16U			1	1	14
FPT-20	FPT-20P-MO2		1	2	17
FPT-20U			1	1	18
FPT-24	FPT-24-MO2		2	2	20
FPT-24U			1	1	22
FPT-28	FPT-28P-MO1		2	2	24
FPT-28U			1	1	26
Flatpack Packages (Quad-Leaded)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
FPT-44			2	4	36
FPT-44U			2	2	40
FPT-48	FPT-48P-MO2		2	4	42
FPT-48U			2	2	44
FPT-48 *			2	4	42
FPT-48U *			2	2	44
FPT-64*	FPT-64P-MO1		2	4	58
FPT-64U	FPT-70P-MO1		1	1	62
FPT-80	FPT-80P-MO1		2	6	72
FPT-80U			2	4	74
FPT-100	FPT-100P-MO1		4	8	88
FPT-100U			4	4	92
FPT-120			6	12	102
FPT-120U			4	8	108
FPT-160			8	14	138
FPT-160U			6	12	142

* Small body size.

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Availability Characteristics of UHB Gate Array Packages

Pin Grid Arrays (PGA, Thru-Hole, 100mil Pin Pitch)					
Pinout Code	Package Code		Number # Vdd	Number # Vss	Available Number of Signal Pins
	Plastic	Ceramic			
PGA-64		PGA-64C-A02	2	4	58
PGA-64U			2	2	60
PGA-88		PGA-88C-A01	4	6	78
PGA-88U			4	4	80
PGA-135			8	12	115
PGA-135U			4	8	127
PGA-179			8	16	155
PGA-179U			8	8	163
PGA-208			12	18	178
PGA-256			16	20	220
Flatpack Packages (Dual-Leaded)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
LCC-28		LCC-28C-A02	2	2	24
LCC-28U			1	1	26
LCC-48		LCC-48C-A01	2	4	42
LCC-48U			1	2	45
LCC-64		LCC-64C-A01	2	4	58
LCC-64U			2	2	60
LCC-68			2	4	62
LCC-68U			2	2	64
LCC-84			4	6	74
LCC-84U			3	4	77
Plastic Leaded Chip Carriers (PLCCs, 50mil Pitch)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
PLCC-28	LCC-28P-M01		2	2	24
PLCC-28U			1	1	26
PLCC-44	LCC-44P-M01		2	4	38
PLCC-44U			1	2	41
PLCC-68	LCC-68P-M01		2	4	62
PLCC-68U			2	2	64
PLCC-84	LCC-84P-M01		4	6	74
PLCC-84U			2	4	78

Subject to Change

MB62xxxx
MB60xxxx

PACKAGE AVAILABILITY

PACKAGE OPTIONS

	C-330 UHB		C-530 UHB		C-830 UHB		C-1200 UHB		C-1700 UHB		C-2200 UHB		C-3000 UHB		C-4100 UHB		C-6000 UHB		C-8700 UHB		C-12000 UHB			
	C	P	C	P	C	P	C	P	C	P	C	P	C	P	C	P	C	P	C	P	C	P	C	P
DIP	16	●																						
	18	●	●		●	●		●		●		●		●		●		●		●		●		
	20	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	22	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	24	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	28	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	40	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	42	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	48	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
SDIP (SHRINK)	28	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	42	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	48	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	64	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
SKDIP (SKINNY)	22	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	24	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	28	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
FPT with leads on two sides of the package	16	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	20	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	24	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	28	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
FPT with leads on four sides of the package	44	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	48	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	48*	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	64	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	80	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	100	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	120	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	160	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
PLCC	28	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	44	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	68	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	84	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
PGA	64	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	88	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	135	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	179	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	208	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	256	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
LCC	28	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	48	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	64	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	68	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	84	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	

C = Ceramic

P = Plastic

●: available now

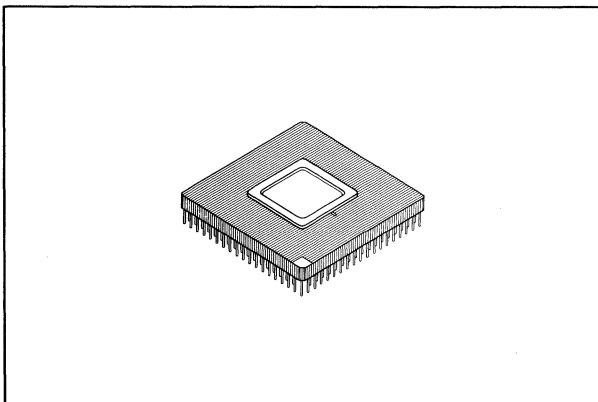
○: under development

* = 48-pin FPT, smaller than the other 48 FPT

MB62xxxx
MB60xxxx

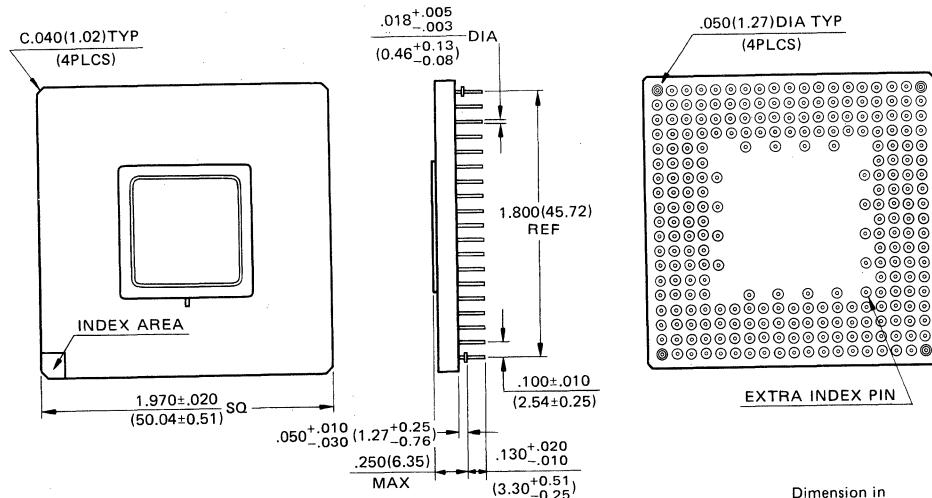


PACKAGE DEMENSIONS



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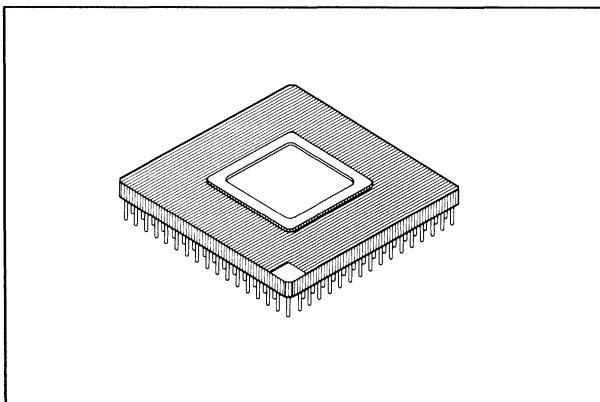
**256-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-256C-A03)**



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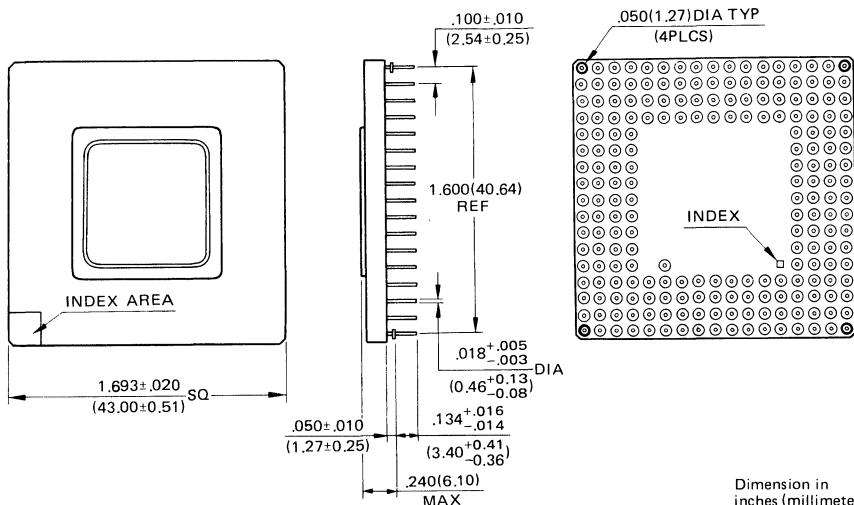
MB62xxxx **FUJITSU**
MB60xxxx

PACKAGE DEMENSIONS (Continued)



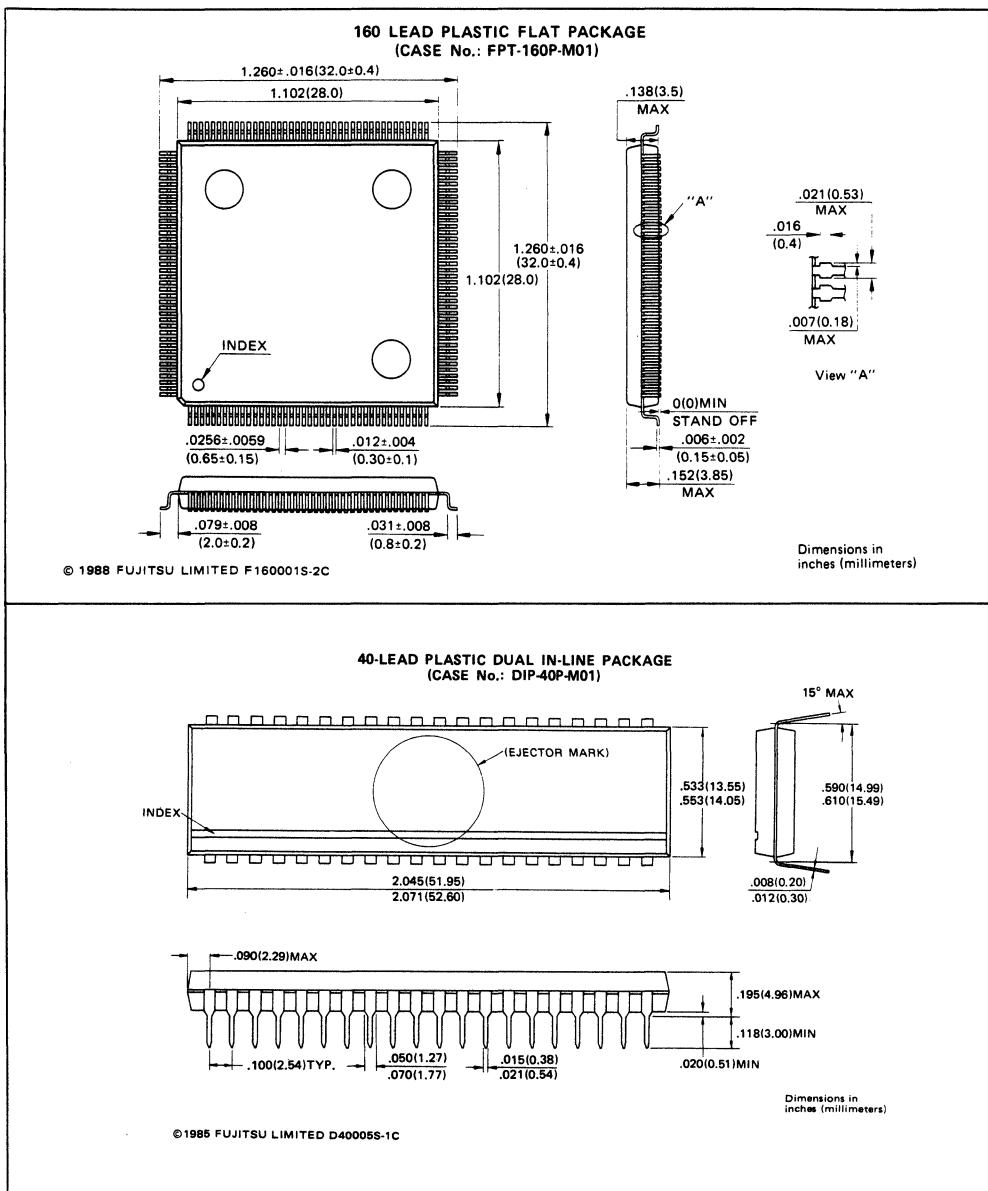
1

**208-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-208C-A02)**



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PACKAGE DEMENSIONS (Continued)



FUJITSU

AV CMOS SERIES GATE ARRAYS

**MB65xxxx
MB66xxxx
MB67xxxx**

 June 1986
 Edition 2.0

DESCRIPTION

The Fujitsu MB65xxxx/MB66xxxx/MB67xxxx family are a series of high performance CMOS gate arrays designed to provide high density, low power, and operating speeds that are comparable to standard bipolar logic. The AV (MB65xxxx) series is an ideal choice for LSI and VLSI applications that require up to 8000 gates, 2304 bits of RAM, 4608 bits of ROM or for bus interface circuits with high-drive requirements. The AVB (MB67xxxx) series include optional 10 mA buffered outputs and input pull-up/pull-down resistors for easy interfacing with bus organized logic. The AVM (MB66xxxx) series of memory arrays include, in addition to the 1.5K, 2.3K, and 4K gates of logic, two basic sizes of static registered memories:

The C4002 and C1502 have up to 2304 bits of RAM organized in an optional by-nine memory configuration that is system compatible with most modern designs. The C301 has 1024 bits of RAM that may be configured into any by-four multiple from 256-by-4 to 32-by-32.

The AVM memories contain duplicate decoder and address register logic so that they may be split and used as two independent memories without borrowing any of the unit cells.

All AV, AVB and AVM arrays use the same basic internal cell structure and common logic Macros.

FEATURES

- 1.4 ns gate delay typical.
(2-Input NAND gate, F.O.=2)
- Static RAM or ROM on chip.
- Silicon-gate 1.8 micron dual metal.
- 100% automatic placement and routing with guaranteed 90% cell utilization.
- Three-state and bidirectional outputs available.
- High-drive output.
- Buffers, I_{OL} = 10.0 mA, available.
- Pull-up/pull-down input buffers available.
- Single 5V power supply.
- TTL compatible I/O, CMOS Input and Schmitt trigger input.
- Popular CAE workstations supported.
- Over 100 unit cells available for design.
- Predesigned software macros available. (F-Macros).
- Fast turnaround: 5 weeks after final validation.
- Evaluation samples available.
- Extended temperature range available.

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AV-CMOS SERIES		Device	Part No.	Gates	I/O	Gate Speed	Features
C2600AV	MB654xxx	2640		106		1.4 ns	High Density
C3900AV	MB653xxx	3900		127		1.4 ns	High Density
C5000AV	MB652xxx	5022		127		1.4 ns	High Density
C6600AV	MB651xxx	6664		160		1.4 ns	High Density
C8000AV	MB650xxx	8000		160		1.4 ns	High Density
AVB-CMOS SERIES		C350AVB	MB675xxx	357	38 (42) ¹	1.4 ns	High-Drive
		C540AVB	MB674xxx	549	48 (50) ¹	1.4 ns	High-Drive
		C850AVB	MB673xxx	852	58 (60) ¹	1.4 ns	High-Drive
		C1200AVB	MB672xxx	1245	68 (68) ¹	1.4 ns	High-Drive
		C1600AVB	MB671xxx	1674	74 (76) ¹	1.4 ns	High-Drive
		C2000AVB	MB670xxx	2052	88 (92) ¹	1.4 ns	High-Drive
AVM-CMOS SERIES		C1502AVM	MB662xxx	1564	107 (109) ²	1.4 ns	4K ROM/2K RAM ³
		C2301AVM	MB661xxx	2375	117 (119) ²	1.4 ns	2K ROM/1K RAM ³
		C4002AVM	MB660xxx	4087	120 (122) ²	1.4 ns	4K ROM/2K RAM ³

Notes:

1. I/O numbers in parentheses indicate I/O available when no high-drive outputs are used.

2. When ROM is provided.

3. Available options.

MB65xxxx
MB66xxxx
MB67xxxx

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS¹

(V_{ss} = 0V.)

Rating	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V _{DD}	V _{ss} - 0.5	-	6.0	volts
Input Voltage	V _I	V _{ss} - 0.5	-	V _{DD} + 0.5	volts
Output Voltage	V _O	V _{ss} - 0.5	-	V _{DD} + 0.5	volts
Output Current ² AVB	I _{OS}	-80	-	140	mA
Output Current ² AVM,AVM	I _{OS}	-40	-	70	mA
Storage Temperature	T _{TSG}	-65 Ceramic	-	150 Ceramic	°C
		-40 Plastic	-	125 Plastic	°C
Bias Temperature	T _{bias}	-40 Ceramic	-	125 Ceramic	°C
		-25 Plastic	-	85 Plastic	°C

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Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions of recommended operation. Exposure to absolute maximum ratings for extended periods may affect device reliability.
2. No more than one output can be shorted at a time and no output can be shorted for more than one second.

RECOMMENDED OPERATING CONDITIONS

(V_{ss} = 0V.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V _{DD}	4.75	5.0	5.25	volts
Input High Voltage	V _{IH}	2.2	-	-	volts
for CMOS Inputs	V _{IH}	V _{DD} × 0.7	-	-	volts
Input Low Voltage	V _{IL}	-	-	0.8	volts
for CMOS Inputs	V _{IL}	-	-	V _{DD} × 0.3	volts
Ambient Temperature	T _A	0	-	70	°C

AV, AVM SERIES CAPACITANCE

(Ta = 25 °C, V_{DD} = V_I = 0 volts, f = 1 MHz.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Capacitance	C _{IN}	-	-	9	pF
Output Capacitance	C _{OUT}	-	-	9	pF
I/O Pin Capacitance	C _{I/O}	-	-	11	pF

AVB SERIES CAPACITANCE

(Ta = 25 °C, V_{DD} = V_I = 0 volts, f = 1 MHz.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Capacitance	C _{IN}	-	-	8	pF
Output Capacitance	C _{OUT}	-	-	16	pF
I/O Pin Capacitance	C _{I/O}	-	-	21	pF

MB65XXXX
MB66XXXX
MB67XXXX

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power Supply Current (Steady state, $V_I = 0V$ or V_{DD})	I_{DDS}	-	-	100	μA
Output High Voltage ($I_{OH} = -0.4$ mA)	V_{OH}	4.2	-	V_{DD}	volts
for Driver Output ($I_{OH} = -0.4$ mA)	V_{OH}	4.2	-	V_{DD}	volts
Output Low Voltage ($I_{OL} = 3.2$ mA)	V_{OL}	V_{SS}	-	0.4	volts
for Driver Output ($I_{OL} = 10.0$ mA)	V_{OL}	V_{SS}	-	0.5	volts
Input High Voltage for CMOS Input	V_{IH}	2.2	-	-	volts
	V_{IH}	$V_{DD} \times 0.7$	-	-	volts
Input Low Voltage for CMOS Input	V_{IL}	-	-	0.8	volts
	V_{IL}	-	-	$V_{DD} \times 0.3$	volts
Input Leakage Current ($V_I = 0 - V_{DD}$)	I_{LI}	-10	-	10	μA
Input Leakage Current (3-state, $V_I = 0 - V_{DD}$)	I_{LZ}	-10	-	10	μA
Input Pull-Up/Down Resistor (Pull up: $V_{IL} = 0V$, Pull down $V_{IH} = V_{DD}$)	R_P	25	50	100	$k\Omega$

AC CHARACTERISTICS DELAY MULTIPLIERS FOR PRE-LAYOUT SIMULATION

(See AV Series Gate Arrays Unit Cell Library)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Propagation Delay	t_{pd}				
Enable Time	t_{PZL}/t_{PZH}				
Disable Time	t_{PLZ}/t_{PHZ}	Typ x 0.45		Typ x 1.6	ns
Set-up Time	t_{SD}				
Hold Time	t_{HD}				
Pulse Width	t_{cw}				

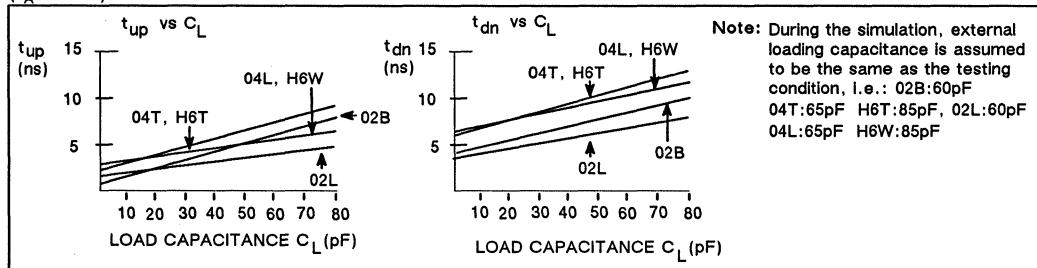
AC CHARACTERISTICS DELAY MULTIPLIERS FOR POST-LAYOUT SIMULATION

(See AV Series Gate Arrays Unit Cell Library)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
-	-	Typ x 0.50	-	Typ x 1.55	ns

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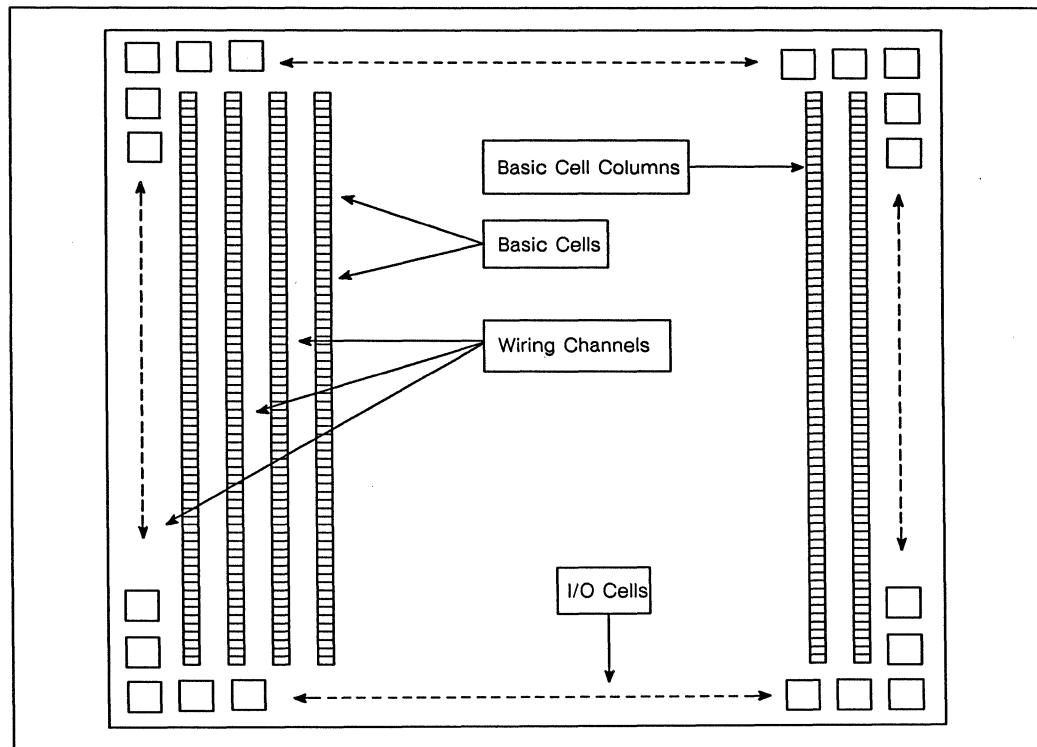
OUTPUT BUFFER PROPAGATION DELAY CHARACTERISTIC
($T_A = 25^\circ\text{C}$)



AV AND AVB-CMOS GATE ARRAY CHIP LAYOUT AND ORGANIZATION

1

CHIP LAYOUT AV AND AVB SERIES EXCEPT C6600AV AND C8000AV



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AV AND AVB ORGANIZATION

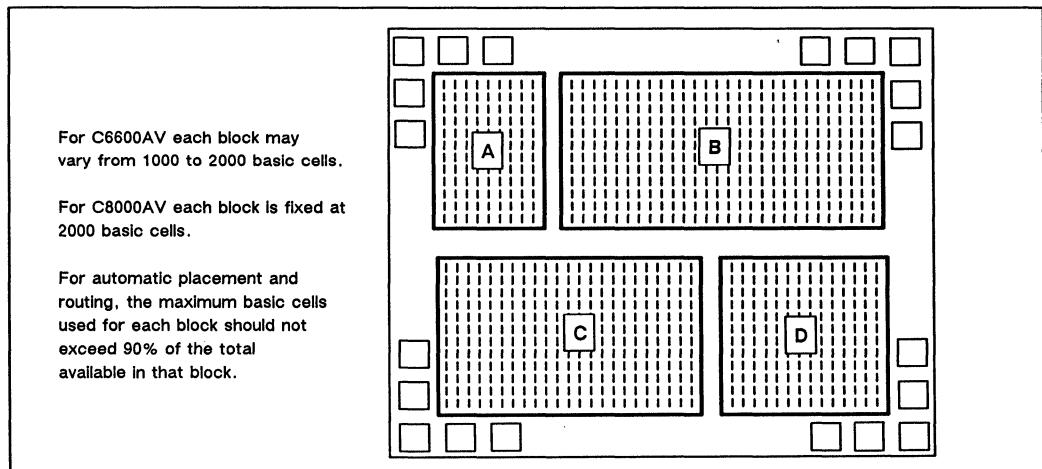
Device	Total Basic Cells	Columns	Basic Cells per Column	Total I/O Cells
C350AVB	357	7	51	38 (42) ¹
C540AVB	549	9	61	48 (50) ¹
C850AVB	852	12	71	58 (60) ¹
C1200AVB	1245	15	83	68 (68) ¹
C1600AVB	1674	18	93	74 (76) ¹
C2000AVB	2052	18	114	88 (92) ¹
C2600AV	2640	22	120	106
C3900AV	3900	25	156	127
C5000AV	5022	27	186	127

Note:

1. I/O numbers in parentheses indicate I/O available when no high-drive outputs are used.

C6600AV, C8000AV AND AVM GATE ARRAY CHIP LAYOUT AND ORGANIZATION

C6600AV, C8000AV CHIP LAYOUT



C6600AV, C8000AV ORGANIZATION

Device	Total Basic Cells	Blocks	BC/Block	Rows/Block	Columns/Block	Total I/O Cells
C6600AV	6664	4	1000 - 2000	-	Variable	160
C8000AV	8000	4	2000	100	20	160

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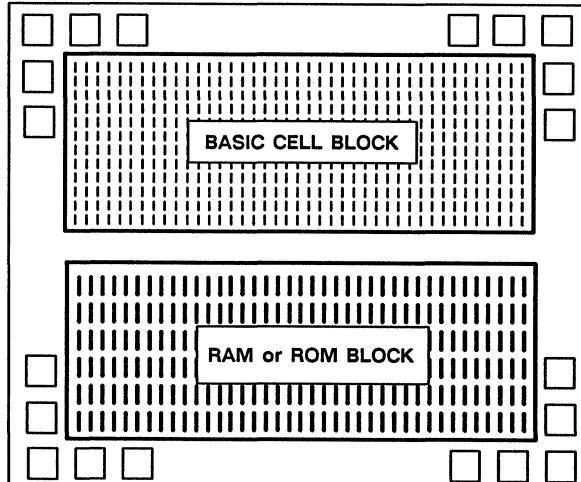
C1502AVM, C2301AVM CHIP LAYOUT

The maximum basic cells used for the basic cell block should not exceed 90% of the total available.

The block is configurable for either 1024 or 2304 total bits organized from 2-bits per word to 32-bits per word, or 9-bits per word to 36-bits per word.

8-bit word sizes and larger (for C2301AVM) or 18-bit word sizes and larger (for C1502AVM) allow division of the RAM block into two separate RAMSs.

ROM can be provided in place of RAM. The ROM block is configurable for either 2048 or 4608 total bits.



1

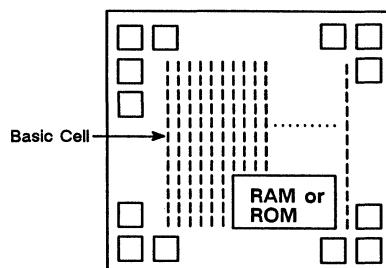
C4002AVM CHIP LAYOUT

For automatic placement and routing the maximum basic cells should not exceed 90% of the total available.

The RAM block is configurable for 2304 total bits organized from 9 bits per word to 36 bits per word.

18-bit word sizes and larger allow division of the RAM block into two separate RAMs.

ROM can be provided in place of RAM. The ROM block is configured for 4608 total bits.



C1502AVM, C2301AVM, C4002AVM ORGANIZATION

Device	Total Basic Cells	Columns	BC/Column	RAM Size	Total I/O Cells
C1502AVM	1564	23	68	2K, 9-bit to 36-bit	107 (109) ¹
C2301AVM	2375	25	95	1K, 4-bit to 32-bit	117 (119) ¹
C4002AVM	4087	6 25	202 115	2K, 9-bit to 36-bit	120 (122) ¹

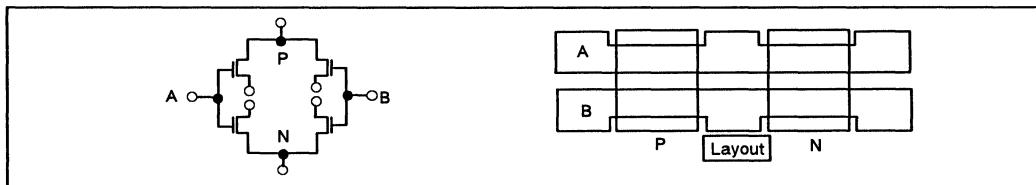
Note:

1. When ROM is provided.

DESIGN COMPONENTS

BASIC CELL

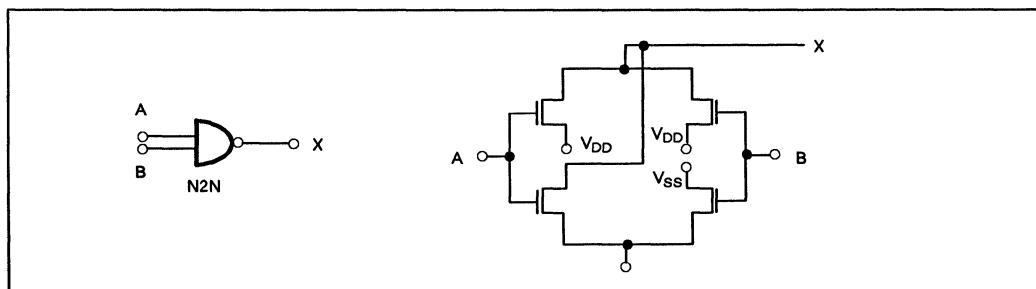
An unprogrammed gate array is an array of basic cells. Thus the "gates" in a gate array are actually the basic cells which will make up final logic. Fujitsu's basic cell contains enough transistors to form a two-input NAND gate.



Unprogrammed Basic Cell

UNIT CELL

A design is implemented in a gate array by logically combining unit cells from the Fujitsu unit cell library to form the logic. Fujitsu provides unit cells to perform most common logic functions and the designer need only name the unit cells required to form the higher level logic functions of his design.

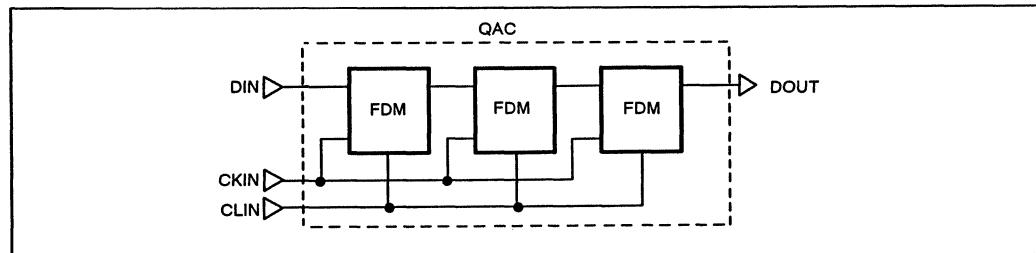


Two-Input NAND Gate Unit Cell (One Basic Cell)

A two-input NAND gate requires only one basic cell to implement. Other unit cells may require as many as 60 or more basic cells. (C47, a counter, requires 68.) Over 100 unit cells are available for design with AV/AVB/AVM-CMOS arrays.

USER MACROS

User Macros are groups of unit cells which perform an identifiable function within the design. It is a user macro because it is defined by the designer. The primary utility of a user macro is that it allows the designer to compose a macro function from unit cells once, then use it any number of times simply by calling it by name.



User Macro QAC is Composed of Three FDM Unit Cells

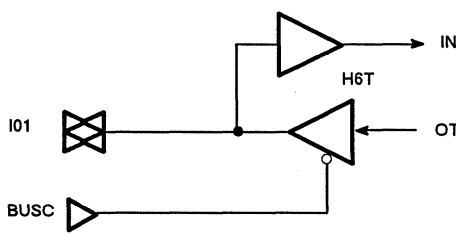
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F-MACROS

F-Macros are created and offered by Fujitsu to emulate the function of popular industry-standard TTL devices. They are identical in application to user macros. Using F-Macros, a designer may convert an existing design directly into gate array. For example, the 74LS191 function is emulated by the Fujitsu F191 F-Macro.

I/O Cells

The I/O cells located on the periphery of the gate array chip are programmable to any of the input or output buffers available. The actual location of an I/O buffer on the chip is determined by the location on the chip of the associated circuitry and any pin location requirements that may be in effect.



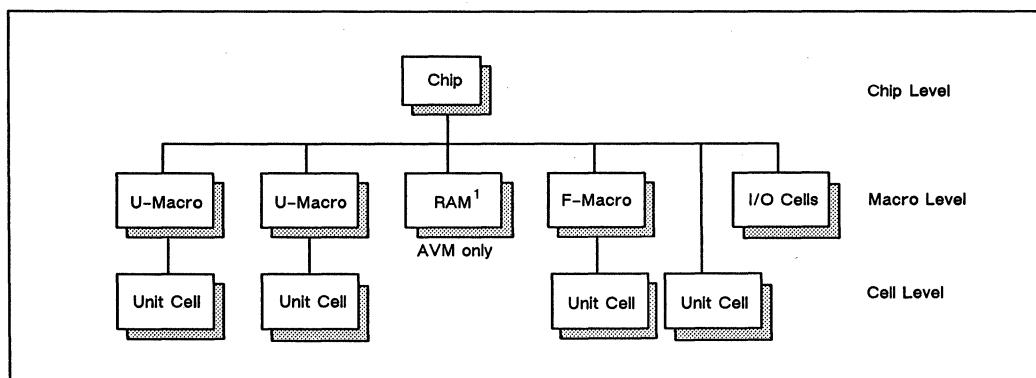
Bidirectional Buffer

DESIGN DESCRIPTION

DESIGN DESCRIPTION

Fujitsu requires only two basic inputs to complete a gate array design: A Logic Description and a Test Description. The logic description defines the logical function of the circuit to be implemented in the array. The test description defines the electrical operation required.

AV, AVB AND AVM LOGIC HIERARCHY

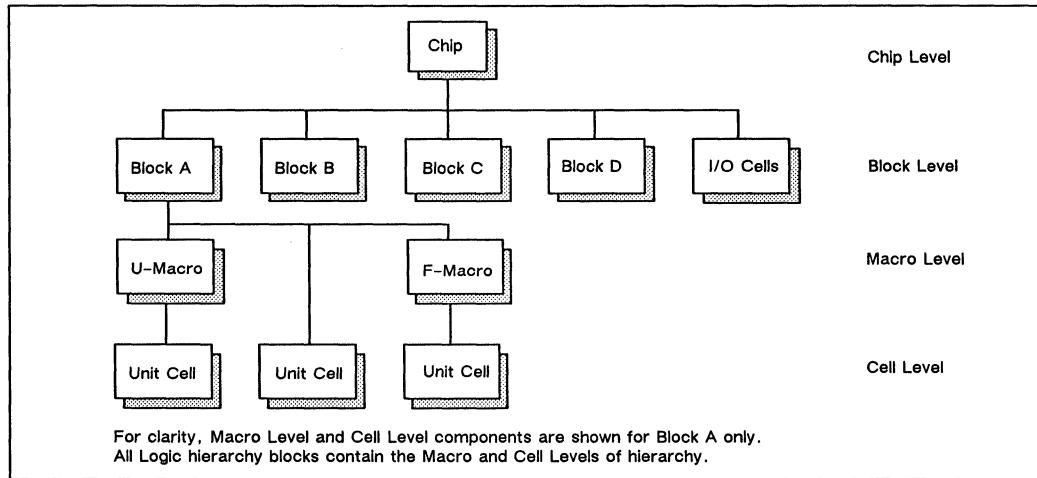


Note:

1. ROM can be made available in place of RAM.

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C6600AV, C8000AV LOGIC HIERARCHY



1

LOGIC DESCRIPTION

The Logic Description, sometimes called a "netlist," calls out the unit cells utilized and their interconnection to form the designer's circuit. Fujitsu uses a proprietary description language, the Fujitsu Logic Description Language (FLDL), to enter the logic description language into the design flow to produce the array design. Designers may prepare their logic description using FLDL or use other description media which Fujitsu will convert to FLDL. Designers using Daisy, Valid or Mentor design workstations are provided with conversion programs as part of the Fujitsu Design Kits for these workstations. In all cases, the design description must follow the fundamental design description structure provided by the logic hierarchy. In many cases Fujitsu will provide turnkey design services.

LOGIC HIERARCHY

The Logic Description is organized into a hierarchy of design components. The logic hierarchy provides the fundamental structure for all logic description inputs and allows a designer to divide his logic into major macro functions and follow a step-by-step approach in describing their interconnection. User Macros may be created to allow repeating the same logic function many times in the design without describing the entire function each time. Fujitsu provides predefined macros (F-Macros) which duplicate the function of many popular industry-standard TTL devices and RAM macros which provide from 1K to 2K of single-port static RAM on chip. Also, ROM macros can be provided. The C6600AV and C8000AV are further divided into "blocks" of cells to ease the layout operations.

CHIP LEVEL

The Chip Level of the logic description defines the interconnection of the design components to each other and the I/O cells. For most AV-CMOS family devices, all types of design components including user macros, F-Macros, RAM macros, ROM macros, and unit cells may be interconnected with each other and the I/O cells to form the chip level logic provided the basic cells total required does not exceed 90% of the basic cell total on the array. For the C6600AV and C8000AV, the same basic cells total restriction applies; the chip level of hierarchy describes only the interconnection of the blocks with the I/O cells to form the chip level logic.

BLOCK LEVEL

The Block Level of the logic description defines the interconnection of design components to form each block of the logic description. C6600AV and C8000AV allow up to 90% of the available basic cells to be utilized for each block. Designers may utilize any of the available design components, including user macros, F-Macros and unit cells for interconnection within the blocks provided the basic cell total required to implement the block design does not exceed the maximum allowed for the block. C6600AV provides a flexible block arrangement, allowing block sizes to range between 1000 and 2000 basic cells provided the total does not exceed 90% of the total available on the array.

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MACRO LEVEL

The Macro Level of the logic description defines the interconnection of unit cells to form user macros. F-Macros may not be used to form user macros. Nor may user macros be nested to form other user macros. The total number of basic cells included in one User Macro can be larger than the total number of basic cells available in one column of the array provided the number of BCs in any of the Unit Cells used in the User Macro does not exceed the total number of basic cells available in one column of the array.

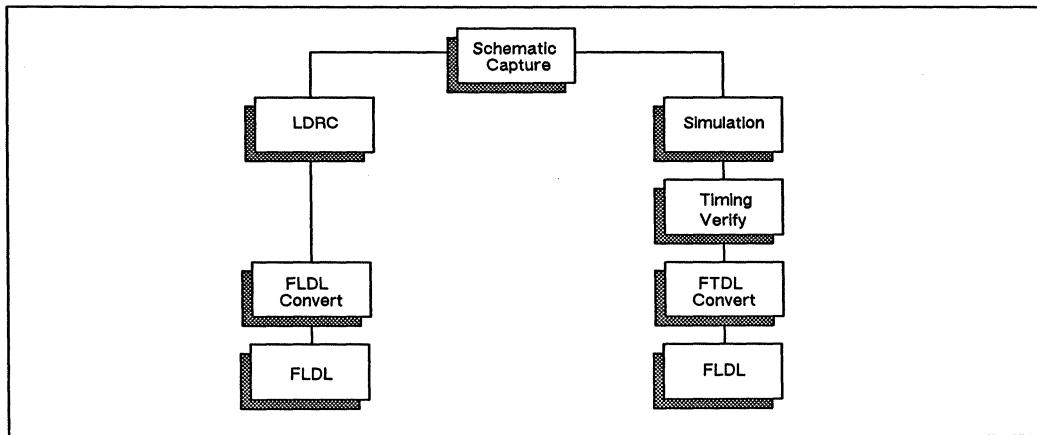
TEST DESCRIPTION

The Test Description defines the electrical performance required of the finished array. Test descriptions are used for all simulation operations and are ultimately converted into final test programs for prototype and production testing. Fujitsu utilizes the proprietary Fujitsu Test Data Description Language (FTDL) for all test description inputs to the design operation. As with the logic description, designers may submit test descriptions utilizing other media and Fujitsu will convert to FTDL. Designers using Daisy, Valid or Mentor design workstations are provided with conversion programs as part of the Fujitsu Design Kits for these workstations. Turnkey services may be available. A complete test description will include D.C. testing and functional testing. Delay testing may be performed under some conditions.

DESIGN DEVELOPMENT FLOW

1

DESIGN WORKSTATION SIMPLIFIED FLOW



WORKSTATION DESIGN

Fujitsu provides workstation support software free of charge to designers using workstations manufactured by Daisy, Valid or Mentor. This software includes a complete design library of unit cells, I/O cells, and memory macros for AV-CMOS gate arrays and conversion programs which generate the logic and test descriptions in the FFLDL and FTDL languages required for design input to Fujitsu.

FUJITSU DESIGN DEVELOPMENT FLOW SUMMARY

Fujitsu accepts a variety of design input media but all media must be converted to logic and test descriptions using the FFLDL and FTDL description languages. Fujitsu may request additional engineering fees for conversion. Logic and test descriptions are collected into data files for access by the Fujitsu CAD system. The test data file provides the basic information used to conduct simulations and generate the final test program.

LDRC

The Logic Design Rule Check conducts a verification that no design rule violations for interconnect, hierarchy or design description language syntax have occurred, and that the description is complete. Fujitsu will work with the designer to resolve any discrepancies before proceeding with the design development.

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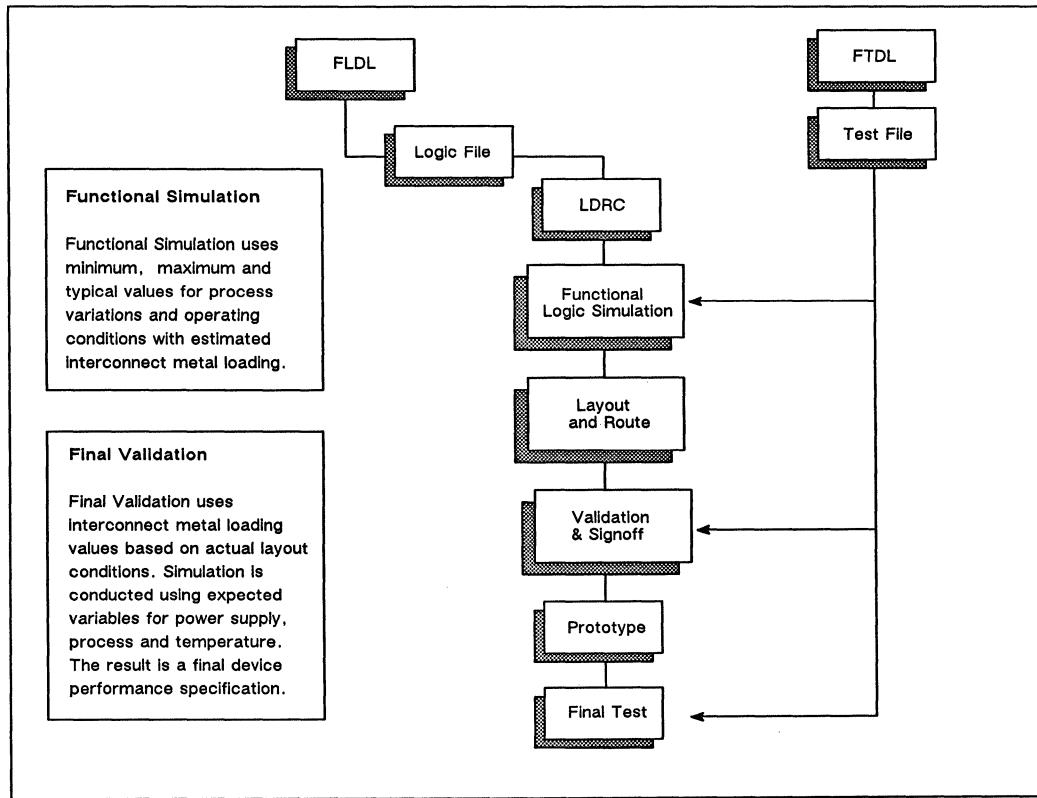
SIMULATION

The Functional Logic Simulation is conducted using minimum, maximum and typical values for process, power supply and temperature conditions, with estimated interconnect metal loading. The functional logic simulation must successfully demonstrate device operation according to the designer's test description before any layout operations are attempted.

FINAL VALIDATION

Final Validation is conducted to produce the device operating specification for approval and signoff by the designer. The simulation is conducted using values for interconnect metal loading based on the actual layout. Full range values for process, temperature and power supply variation are also used. A final operating specification is presented to the designer which defines the parameters which will be guaranteed by Fujitsu in the prototype and production devices.

FUJITSU DESIGN DEVELOPMENT FLOW SUMMARY



PROTOTYPES

At the completion of the design development Fujitsu provides the designer with prototypes for on-site design evaluation. Ten prototype devices (Five for C8000AV) are provided with the development fee. Additional prototypes may be provided for an additional fee.

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UNIT CELL LIBRARY

	Unit Cell	Function	Basic Cells	Unit Cell	Function	Basic Cells
INVERTER, CLOCK BUFFER FAMILY	V1N	Inverter	1	K3B	Gated Clock Buffer (AND)	3
	V2B	Power Inverter	1	K4B	Gated Clock Buffer (OR)	3
	K1B	Clock Buffer	2	KCB	Block Clock Buffer	11
	K2B	Power Clock Buffer	3	-	-	-
NAND FAMILY	N2N	2-input NAND	1	N6B	6-input Power NAND	5
	N3N	3-input NAND	2	N8B	8-input Power NAND	6
	N4N	4-input NAND	2	N9B	9-input Power NAND	7
	N2B	2-input Power NAND	3	NCB	12-input Power NAND	9
	N3B	3-input Power NAND	3	NGB	16-input Power NAND	11
	N4B	4-Input Power NAND	4	-	-	-
AND FAMILY	N2P	2-Input Power AND	2	N4P	4-Input Power AND	3
	N3P	3-Input Power AND	3	-	-	-
NOR FAMILY	R2N	2-Input NOR	1	R6B	6-Input Power NOR	5
	R3N	3-Input NOR	2	R8B	8-Input Power NOR	6
	R4N	4-Input NOR	2	R9B	9-Input Power NOR	7
	R2B	2-Input Power NOR	3	RCB	12-Input Power NOR	9
	R3B	3-Input Power NOR	3	RGB	16-Input Power NOR	11
	R4B	4-Input Power NOR	4	-	-	-
OR FAMILY	R2P	2-Input Power OR	2	R4P	4-Input Power OR	3
	R3P	3-Input Power OR	3	-	-	-
ENOR/EOR	X1B	Power ENOR	4	X2B	Power EOR	4
AND-NOR FAMILY	D14	2-wide 3-AND 4-Input AND-OR Invert	2	D34	3-wide 2-AND 4-Input AND-OR Invert	2
	D23	2-wide 2-AND 3-Input AND-OR Invert	2	D44	2-wide 2-OR 2 AND 4-Input AND-OR Invert	2
	D24	2-wide 2-AND 4-Input AND-OR Invert	2	-	-	-
OR-NAND FAMILY	G14	2-wide 3-OR 4-Input OR-AND Invert	2	G34	3-wide 2-OR 4-Input OR-AND Invert	2
	G23	2-wide 2-OR 3-Input OR-AND Invert	2	G44	2-wide 2-AND 2-OR 4-Input OR-AND Invert	2
	G24	2-wide 2-OR 4-Input OR-AND Invert	2	-	-	-

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UNIT CELL LIBRARY

MUX FAMILIES

Unit Cell	Function	Basic Cells	Unit Cell	Function	Basic Cells
T24	Power 2-AND 4-wide	6	U24	Power 2-OR 4-wide	6
T26	Power 2-AND 6-wide	9	U26	Power 2-OR 6-wide	9
T28	Power 2-AND 8-wide	11	U28	Power 2-OR 8-wide	11
T32	Power 3-AND 2-wide	5	U32	Power 3-OR 2-wide	5
T33	Power 3-AND 3-wide	7	U33	Power 3-OR 3-wide	7
T34	Power 3-AND 4-wide	9	U34	Power 3-OR 4-wide	9
T42	Power 4-AND 2-wide	6	U42	Power 4-OR 2-wide	6
T43	Power 4-AND 3-wide	9	U43	Power 4-OR 3-wide	9
T44	Power 4-AND 4-wide	11	U44	Power 4-OR 4-wide	11

FLIP-FLOP FAMILIES

FD2	Power DFF	8	FDD	Positive Edge Power DFF with Clear/Preset	11
FD3	Power DFF with Preset	9	FDE	Positive Edge Power DFF with Clear	10
FD4	Power DFF with Clear/Preset	10	FDG	Positive Edge with Clear	9
FD5	Power DFF with Clear	9	FJD	Positive Edge Power JKFF with Clear	12
FD6	DFF	7	FJ4	Power JKFF with Clear	11
FD7	DFF with Clear	8	FJ5	Power JKFF with Clear/Preset	12
FD8	DFF with Latch	9	-	-	-

FLIP-FLOP FAMILIES USING TRANSMISSION GATES

FDM	DFF	6	FDP	DFF with Set/Reset	8
FDN	DFF with Set	7	FDQ	4-bit DFF	21
FDO	DFF with Reset	7	FDR	4-bit DFF with Clear	26
FDS	4-Bit DFF	20	-	-	-

LATCH FAMILIES

LT1	SET-RESET with Clear	4	LT3	4-bit Data Latch	15
LT2	1-bit Data Latch	4	LT4	4-bit Data Latch	13
LTK	Data Latch	4	LTL	Data Latch with Clear	5
LTM	4-Bit Data Latch with Clear	15	-	-	-

SHIFT REGISTER FAMILIES

FS1	4-bit S_{in} - P_{out}	18	FS3	4-bit with Async Load	34
FS2	4 bit S_{in} - P_{out} with Sync Load	30	-	-	-

DECODER FAMILIES

DE2	2:4 Decoder	5	DE3	3:8 Decoder	15
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COUNTER FAMILIES

C11	Flip-Flop for Counter	11	C43	4-bit Sync UP with Clear	48
C41	4-bit Async	24	C45	4-bit Sync UP	48
C42	4-bit Sync	32	C47 ¹	4-bit Sync UP/DOWN	68

Note:

1. C47 is not available for C-350AVB and C540AVB.

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UNIT CELL LIBRARY

	Unit Cell	Function	Basic Cells	Unit Cell	Function	Basic Cells
SELECTOR FAMILY	T2B	2:1 Selector	2	V3A	1:2 Selector	2
	T2C	Dual 2:1 Selector	4	V3B	Dual 1:2 Selector	3
	T2D	2:1 Selector	2	T5A	4:1 Selector	5
COMPARATOR	MC4	4-bit Magnitude Comparator	42	-	-	-
ADDER FAMILY	A1N	1-bit Full Adder	8	A4H	4-bit Full Adder	50
	A2N	2-bit Full Adder	16	-	-	-
SCHMITT TRIGGER	SM1 ¹	Schmitt Trigger	8	SM2 ¹	Schmitt Trigger	7
DELAY UNIT CELLS	BD3	Buffer (Delay Cell)	5	BD6	Buffer (Delay Cell)	17
	BD5	Buffer (Delay Cell)	9	-	-	-
I/O CELL FAMILY	I2B	Input Buffer	0	IKB	Clocked Input Buffer (Inverting)	0
	I2BU ²	I2B with Input Pull-up	0	IKBU ²	IKB with Input Pull-up	0
	I2BD ²	I2B with Input Pull-down	0	IKBD ²	IKB with Input Pull-down	0
	ILB	Clocked Input Buffer	0	I2C	CMOS Interface Input Buffer (True & Inverter)	0
	ILBU ²	ILB with Input Pull-up	0			
	ILBD ²	ILB with Input Pull-down	0	I2CU ²	I2C with Input Pull-up	0
	IT1	Input Buffer for Schmitt-Trigger Input	0	I2CD ²	I2C with Input Pull-down	0
				H6T	Tri-state Output & Input Buffer	0
	IT1U ²	IT1 with Input Pull-up	0	H6TU ²	H6T with Input Pull-up	0
	IT1D ²	IT1 with Input Pull-down	0	H6TD ²	H6T with Input Pull-down	0
	O2B	Output Buffer	0	O4T	Tri-state Output Buffer	0
	O2L ²	Power Output Buffer (True)	0	O4W ²	Power Tri-state Output Buffer (True)	0
	H6W ²	Power Tri-state Output and Input Buffer (True)	0		H6C ²	Tri-state Output and CMOS Interface Input Buffer (True)
	H6WU ²	H6W with Input Pull-up	0	H6CU ²	H6C with Input Pull-up	0
	H6WD ²	H6W with Input Pull-down	0	H6CD ²	H6C with Input Pull-down	0
	H6E ²	Power Tri-state Output and CMOS Interface Input Buffer (True)	0	H6EU ²	H6E with Input Pull-up	0
				H6ED ²	H6E with Input Pull-down	0

Note:

1. SM1 and SM2 must not be used together in one chip.
2. Available only for AVB.

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F-MACRO LIBRARY

F-MACRO FUNCTION

Fujitsu's F-Macros are direct software macro implementations of popular industry-standard TTL functions. They may be used in the design exactly the same as user macros. Designers's converting existing TTL designs to gate array will find the F-Macro a particularly useful implementation.

F-MACROS AVAILABLE TO REPLACE THESE TTL DEVICES

Device	Basic Cells	Device	Basic Cells	Device	Basic Cells
7400		7498	36	74176	76
7402		7499		74177	72
7404		74100	60	74178	63
7408		74101		74179	71
7410		74102		74180	33
7411		74103		74181	
7420		74106		74182	49
7421		74107		74183	36
7425		74108		74190	106
7427		74109		74191	73 ¹
7430		74112		74192	92
7432		74113		74193	82
7442	32	74114		74194	78
7443	32	74116	82	74195	51
7444	32	74120	34	74198	132
7451	7	74135		74199	98
7454	9	74137	48	74260	
7455	6	74138	28	74261	107
7456		74139	26	74273	
7457		74147	49	74278	46
7464	9	74148	53	74279	18
7468	89	74150	112	74280	57
7469	79	74151	54	74283	50
7473		74152	29	74290	45
7474		74153	24	74293	33
7475	32	74154	96	74298	36
7476		74155	29	74352	28
7477	18	74157	23	74375	18
7478		74158	23	74377	71
7482	16	74160	82	74378	55
7483	50	74161	48	74379	39
7485	42	74162	83	74381	192
7486		74163	48	74382	201
7487		74164	70	74386	
7490	41	74165	73	74390	82
7491	43	74166	80	74393	52
7492	64	74168	111	74396	60
7493	33	74169	74 ¹	74398	37
7494	47	74171		74399	37
7495	42	74174	46		
7496	56	74175	32		
7497					

Note:

1. These F-Macros utilize complex unit cells and may not be available for smaller arrays.

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RAM MACRO LIBRARY

C2301AVM

32-WORD RAM MACROS

RAM Macro Name	RAM 1 Configuration	RAM 2 Configuration
R51	32-word x 32-bit	-
R51A	32-word x 28-bit	32-word x 4-bit
R51B	32-word x 24-bit	32-word x 8-bit
R51C	32-word x 20-bit	32-word x 12-bit
R51D	32-word x 16-bit	32-word x 16-bit

64-WORD RAM MACROS

R61	64-word x 16-bit	-
R61A	64-word x 12-bit	64-word x 4-bit
R61B	64-word x 8-bit	64-word x 8-bit

128-WORD RAM MACROS

R71	128-word x 8-bit	-
R71A	128-word x 4-bit	128-word x 4-bit

256-WORD RAM MACROS

R83	256-word x 4-bit	-
R83A	256-word x 2-bit	256-word x 2-bit

C1502AVM/C4002AVM

64-WORD RAM MACROS

RAM Macro Name	RAM 1 Configuration	RAM 2 Configuration
R610	64-word x 36-bit	-
R611	64-word x 20-bit	64-word x 16-bit

128-WORD RAM MACROS

R711	128-word x 18-bit	-
R712	128-word x 9-bit	128-word x 9-bit

256-WORD RAM MACROS

R87	256-word x 9-bit	-
-----	------------------	---

ROM MACRO LIBRARY

C2301AVM

256-WORD ROM MACROS

ROM Macro Name	Configuration	
YRn	256-word x 8-bit	-

Note:

Contact nearest Fujitsu Design Center for additional ROM data.

PACKAGE AVAILABILITY MATRIX

MB65xxxx
MB66xxxx
MB67xxxx

PACKAGE AVAILABILITY MATRIX

DUAL IN-LINE PACKAGES, PLASTIC SHRINK TYPE (SH-DIP)

DUAL IN-LINE PACKAGES, PLASTIC (PDIP)

PACKAGE PRODUCT	PDIP-16	PDIP-18	PDIP-20	PDIP-22	PDIP-24	PDIP-28	PDIP-40	PDIP-42	PDIP-48
350AVB	●	●	●	●	●	●	●	●	
540AVB	●	●	●	●	●	●	●	●	
850AVB			●	●	●	●	●	●	
1200AVB				●	●	●	●	●	●
1502AVM					●	●	●	●	
1600AVB					●	●	●	●	●
2000AVB					●	●	●	●	●
2301AVM					●		●	●	
2600AV					●	●	●	●	●
3900AV					●		●	●	
4002AVM									
5000AV						●			
6600AV									
8000AV									

DUAL IN-LINE PACKAGES, PLASTIC SKINNY TYPE (SK-DIP)

PACKAGE PRODUCT	DIP-28SH SHRINK	DIP-42SH SHRINK	DIP-48SH SHRINK	DIP-64SH SHRINK	DIP-24SK SKINNY
350AVB	●	●	●	●	
540AVB	●	●	●	●	●
850AVB	●	●	●	●	●
1200AVB	●	●	●	●	●
1502AVM		●	●	●	●
1600AVB	●	●	●	●	●
2000AVB		●	●	●	●
2301AVM			●	●	●
2600AV		●	●	●	●
3900AV			●	●	●
4002AVM					
5000AV				□	
6600AV					
8000AV					

PLASTIC LEADED CHIP CARRIERS (PLCC)

PACKAGE PRODUCT	PLCC-28	PLCC-44	PLCC-68	PLCC-84
350AVB	●	●		
540AVB	●	●		
850AVB	●	●		
1200AVB	●	●		
1502AVM		●	●	●
1600AVB	●	●	●	
2000AVB	●	●	●	
2301AVM		●	●	●
2600AV	●	●	●	●
3900AV		●	●	●
4002AVM				
5000AV			●	●
6600AV				
8000AV				

FLAT PACKS, PLASTIC (FPT)

PACKAGE PRODUCT	FPT-16	FPT-20	FPT-24	FPT-28	FPT-48	FPT-64	FPT-80	FPT-100	FPT-120	FPT-160
350AVB	●	●	●	●	●					
540AVB	●	●	●	●	●	●				
850AVB		●	●	●	●	●				
1200AVB			●	●	●	●				
1502AVM				●	●	●	●	●	●	
1600AVB					●	●	●	●	●	
2000AVB					●	●	●	●	●	
2301AVM					●	●	●	●	●	
2600AV					●	●	●	●	●	□
3900AV					●	●	●	●	●	□
4002AVM										
5000AV						●	●	●	□	□
6600AV							□	□	□	□
8000AV							□	□	□	□

● - QUALIFIED PRODUCTION OFFICIALLY AVAILABLE NOW

□ - PACKAGE COMBINATION UNDER DEVELOPMENT

Note:

Contact nearest Fujitsu Design Center for current package information and power supply pin restrictions.
Plastic PGA packages (64, 88, 135, 179-pin) are now under development.

MB65XXXX
MB66XXXX
MB67XXXX

June 1986

PACKAGE AVAILABILITY MATRIX

DUAL IN-LINE PACKAGES, CERAMIC (CDIP)										
CMOS	PACKAGE PRODUCT	CDIP-16	CDIP-18	CDIP-20	CDIP-22	CDIP-24	CDIP-28	CDIP-40	CDIP-42	CDIP-48
	350AVB	●	●	●	●	●	●	●		
	540AVB	●	●	●	●	●	●	●	●	
	850AVB				●	●	●	●		
	1200AVB				●	●	●	●	●	●
	1502AVM							●	●	●
	1600AVB				●	●	●	●	●	●
	2000AVB						●	●	●	●
	2301AVM							●	●	●
	2600AV						●	●	●	●
	3900AV							●	●	●
	4002AVM									
	5000AV									
	6600AV									
	8000AV									

CERAMIC LEADLESS CHIP CARRIERS (LCC) CERAMIC J-LEADED CHIP CARRIERS (JLCC) CERAMIC PIN GRID ARRAY (PGA)												
CMOS	PACKAGE PRODUCT	LCC-28	LCC-48	LCC-64	LCC-68	JLCC-68	JLCC-84	PGA-64	PGA-88	PGA-135	PGA-179	PGA-256
	350AVB	●	●									
	540AVB	●	●	●	□				●			
	850AVB	●	●	●	□				●			
	1200AVB	●	●	●	□				●			
	1502AVM	●	●	●	□	□	□	●	●	●	●	
	1600AVB	●	●	●	□	□			●	●	●	
	2000AVB	●	●	●	□	□			●	●		
	2301AVM	●	●	●	□	□	□	●	●	●	●	
	2600AV	●	●	●	□	□	□	●	●	●	●	
	3900AV	●	●	●	□	□	□	●	●	●	●	
	4002AVM		●	●	●				●	●	●	
	5000AV		●	●	□	□	□	●	●	●	●	
	6600AV		●	●	□				●	●	●	●
	8000AV		●	●	□				●	●	●	●

● - QUALIFIED PRODUCTION OFFICIALLY AVAILABLE NOW

□ - PACKAGE COMBINATION UNDER DEVELOPMENT

Note:

Contact nearest Fujitsu Design Center for current package information and power supply pin restrictions.

Chapter 2 – Steps Toward Design

Contents of This Chapter

- 2.1 Introduction
 - 2.2 Choosing Fujitsu as your ASIC Manufacturer
 - 2.3 Choosing a Device
 - 2.4 Choosing a Package
 - 2.5 Technical Review
 - 2.6 Design Interface Options
-

2.1 Introduction

This section of the data book takes a look at the issues that must be considered before a design is ready to be entered on a computer-aided engineering (CAE) workstation.

2.2 Choosing Fujitsu as Your ASIC Manufacturer

The first step in implementing a given ASIC design is to choose the manufacturer that offers semiconductor processes capable of actualizing the performance requirements of the IC. The manufacturer should also offer consistent and easily accessible customer support, timely transfer of the design into silicon, and a highly reliable end product.

The data sheets and supplementary information in Chapter 1 enable customers to determine whether their requirements fall within the broad range of Fujitsu's technical capability.

The second step is to discuss the design requirements with one of Fujitsu's Field Applications Engineers at either a Regional Sales Office or a Technical Resource Center. Regional Sales Office and Technical Resource Center addresses and telephone numbers are listed at the back of this volume. Fujitsu's Field Applications Engineers work with each customer to determine which technology would be most suitable for a given design, taking into account the factors outlined in more detail below.

Fujitsu's highly developed software tools, high-capacity manufacturing facilities (the largest in the world) and long history of excellence in the field (Fujitsu has been producing custom gate arrays commercially since 1974) enable customers to turn designs into highly reliable products in a cost-effective time frame.

2.3 Choosing A Device

Speed is usually the deciding factor in choosing the technology for a design, but sometimes special requirements such as package availability, on-chip memory (available in the AU and AVM technology), or the necessity for battery power (a feature of the AVL technology) influence the final decision.

Usually the device type is a requirement of the design and is chosen before the package size is determined. The size of the package will depend on array size, partitioning, the number of power

and ground pins required by the SSOs (simultaneously switching outputs) used in the design, and the high power drive buffers and clock inputs used in the design.

To determine the most suitable device within a given technology, the designer must determine the gate count and pinout requirements from the schematic diagram of the design to be implemented.

The functions in the schematic or logic block diagram may be described using standard logic functions, programmable logic, or Fujitsu's Unit Cell Library.

Gate counts are calculated in terms of how many basic cells make up each component function (unit cell). This number is given for each unit cell in the unit cell library for each technology. By adding up the number of basic cells used in each logic element in a design, a designer can arrive at a good first estimate of the design complexity.

In technologies in which the basic cells are arranged in single columns (AV/AVB/AVL/AVM), unit cells may not bridge two basic cell columns, and therefore, there may not be more unit cells requiring the majority of cells in a column than there are columns. In the double-column technologies (UHB and AU), unit cells take up parts of two adjacent columns. It is recommended that no more than 90% of the basic cells in a channeled array be used. Respecting this limitation facilitates fully automated layout.

1

2.4 Choosing a Package

Before the final choice of an array can be made, however, the choice of a package must be considered. The intended use of the IC generally determines the type of package used; packaging issues are discussed in detail in the application note "Choosing the Best Package for Your ASIC Design" included in Chapter 8 of this data book. The types of packages available for Fujitsu's ASIC products are shown in Table 2-1. The number of pins per package for each device is shown on the data sheets in Section 1.

Table 2-1. Fujitsu CMOS ASIC Package Options

Package Type	Package Options
Standard DIP (100 mil)	16 – 64 pins, Ceramic 16 – 48 pins, Plastic
Shrink DIP (70 mil)	28 – 42 pins, Ceramic 28 – 64 pins, Plastic
Skinny DIP (300 mil row space)	22 – 28 pins, Plastic
PLCC	22 – 28 pins, Plastic
LCC	28 – 64 pins, Ceramic
Flat Package	16 – 160 pins, Plastic 48 – 260 pins, Ceramic
Pin Grid Array	64 – 401 pins, Ceramic 64 – 135 pins, Plastic

The size of the package chosen is regulated by the number of inputs and outputs required, the number of Vss and Vdd pins required, and the number of simultaneously switching outputs (SSOs) included in the design.

Package Size vs. SSOs

The number of SSOs can influence the size of the package chosen because additional ground pins are sometimes required in a design that has more simultaneously switching outputs than is acceptable for a given package type. Simultaneously switching outputs are those that switch from a logic low or a high impedance (Z) to a logic high or from a logic high or Z state to a logic low within 20 nanoseconds of each other.

A general rule is to use one ground pin for each group of 10 simultaneously switching low power outputs or for 20 non-simultaneous outputs. For the actual restrictions for each technology and situation, the design manual must be consulted.

Although the Vss and Vdd pins are preassigned in each package and cannot be changed, alternate packages are available offering varying numbers of power and ground pins.

2.5 Technical Review

When the CMOS technology, the device, and the package have been decided upon, the customer and Fujitsu's Field Applications Engineer hold a technical review to ensure that all the information necessary to implement the design is available and to allow Fujitsu to derive a schedule and price. Often, especially for new customers, a technical review form, such as the one reproduced below and on the following pages as Figure 2-1, is used.

Technical Resource Center Engineer : _____

Field Applications Engineer : _____

Technical Review Form
Fujitsu Microelectronics Incorporated
ASIC Products

RFQ # _____

Quote # _____

Company: _____

Prepared by: _____ Date: _____

Customer Design Engineer: _____

Designer's Phone Number: _____

Customer Engineering Manager: _____

Design City/State: _____

Production City/State: _____

Reviewed by: _____ Date: _____

The purpose of this form is to compile data that will impact or affect the cost and delivery of Custom/Semicustom products. Any price or delivery quotation will be based solely on the information provided in this document.

Customer Part Number: _____

Customer Part Name: _____

Customer Program Name: _____

If Member of a Set, Set Name: _____

Figure 2-1a. Sample Technical Review Form

1.0 General Information**1.1 Device Technology (specify exact technology and size)**

1.2 Design Approach:

Gate Array _____ Standard Cell _____

1.3 Number of hierarchical levels in design: _____**1.4 Logic Cell Count:**

Basic Cell Count _____ (non-hierarchical) without memory

If hierarchical, _____
Block A Block B Block C Block D

Block E Block F Block G Block H**1.5 Memory Requirements**

1.5.1 RAM ROM None (Circle to indicate)

1.5.2 Size: _____

1.5.3 Organization: _____

1.5.4 Number of Ports: _____

1.5.4.1 Reads: _____

1.5.4.2 Writes: _____

1.5.5 State the custom RAM cell organization _____

1.5.6 Memory Cell Count _____

1.6 Special F-macro Requirements: _____**1.7 Package Type (e.g. DIP-20C-C03):** _____**1.8 Special Heatsink:** _____**1.9 Special Carrier:** _____**1.10 Special Markings or Customer Logo:** _____**Figure 2-1b. Sample Technical Review Form**

<p>1.11 Number of Input Pins: CMOS _____ TTL _____ Schmitt Trigger _____</p> <p>1.12 Number of Output Pins: CMOS _____ TTL _____</p> <p>1.13 Number of Bidirectional Pins: CMOS _____ TTL _____</p> <p>1.14 Composition of Simultaneously Switched Output Groups: ($\pm 10\text{ns}$ of each other) _____</p> <p>1.14.1 Indicate the number of buffer types contained within each group.</p>								
	Output Buffer Type							
Group Number	3.2mA	6.4mA	8.0mA	10mA	12mA	12mA w/NLR	24mA w/NLR	Total I _{OL} per Group
1								
2								
3								
4								
5								
6								
Total I _{OL} per Buffer Type								
1.14.2 Other Special Group(s)					(Consult a TRC Design Engineer)			
Group #_____ : #_____ @ _____ mA								
Group #_____ : #_____ @ _____ mA								
1.15 Total Number of Ground Pins Required: _____								
1.16 Total Number of Power Pins Required: _____								
1.17 Meets Fujitsu Standard Pinout: Yes No (If No, consult a TRC Design Engineer)								

Figure 2-1c. Sample Technical Review Form

- 1.18 Attach a completed photocopy of the chosen pin assignment table from the Design Manual (e.g., for a C-4002AVM, LCC-68, attach Table 24).

Note: The standard placement for the power supply and special purpose pins are shown in the Pin Assignment Tables. Any variation from the standard is subject to approval by Fujitsu.

- 1.19 Complete the Attached "I/O Pin Specification/Special Requirement" Form When Requesting Package Variances.

- 1.20 Maximum Output Frequency: _____ MHz into _____ pF Load
Buffer Type: CMOS TTL (Circle to indicate)

- 1.21 Maximum Input Frequency: _____ MHz

- 1.22 Maximum Toggle Frequency: _____ MHz

- 1.23 Crystal Oscillator Requirements:

On-chip Resistor Required: Yes No

Pin Numbers _____ Frequency _____

- 1.24 Power Supply Requirements (Referenced to ground):

PS _____ Volts ± _____ %

- 1.25 Customer Maximum Power Dissipation Limit: _____

- 1.26 Customer Maximum Temperature Range/Variation:

Min. _____ °C Max. _____ °C

2.0 Design Input Format: (Circle or Complete)

- 2.1 Logic Data: FLDL Other _____

- 2.2 Test Data: FTDL Other _____

- 2.3 Input Media: _____ Mag Tape (IBM Standard or Non Label)

_____ Diskette (Daisy, Valid, Mentor, Other) _____

_____ File Transfer (Kermit and Telebit or Hayes Modem)

- 2.4 Workstation Used _____

Figure 2-1d. Sample Technical Review Form

1

3.0 Test Data:

3.1 Description of the FTDL

<u>No. Of Test Blocks</u>	<u>Cycle Time</u>	<u>No. Of Test Patterns</u>
Function: _____	_____	_____
2-function: _____	_____	_____
DC: _____	1000ns	_____
(Optional) AC: _____	_____	_____
Other: _____	_____	_____

3.2 For an additional fee, the customer requests Fujitsu to perform fault grading on the design and provide results. Yes ____ No ____

3.3 For an additional fee, the customer requests Fujitsu to provide a copy of the test tape in the following format:

Sentry Advantest (Circle one)

4.0 Critical Path Propagation Delay Estimation:

4.1 In the space below and on the attached delay calculation form, describe all critical paths that should not violate maximum or minimum delay requirements and/or are skew sensitive. Use as many sheets as necessary.

4.2 Critical Path Description:

4.2.1 Critical Path Name/Number: _____

4.2.2 Delay Required: _____ Min _____ Max _____

4.2.3 Logic Diagram Drawing:

Figure 2-1e. Sample Technical Review Form

2.6 Design Interface Options

The next step is to determine which computer-aided engineering (CAE) workstation will be used to enter the design. The desired result of entering the design on a CAE workstation is the generation of a successful Fujitsu Logic Description Language (FLDL) file and Fujitsu Test Description Language (FTDL) file. These two files (which may be generated on any of several different CAE workstation systems) enable Fujitsu's host mainframe to perform automated layout and rigorous test and simulation of the design.

Four popular dedicated CAE workstation systems (Valid, Mentor, Daisy, and the HP 9000) as well as several hardware-independent CAE packages support Fujitsu's design software. In addition, Fujitsu now offers design support on ViewCAD®, a computer-aided engineering system originated by Fujitsu for ASIC designs.

ViewCAD is written in the C programming language and runs on any UNIX® platform that supports the XWindow System® (such as the Sun 3 or 4 series of workstations). It includes in one package all of the necessary functions for the design, simulation, and analysis of an ASIC design. ViewCAD makes use of a graphics-oriented interface that allows visual examination of all circuits, circuit test data, and simulation results. Its final product is the logic and test data description files (FLDL and FTDL) that are required by the host mainframe computer to process a design.

Through long experience, Fujitsu has found that by far the most efficient way to achieve a trouble-free end product is for customers to implement the design on a workstation themselves. This can be done:

- (a) on CAD equipment that the customer is already using (Fujitsu provides cell library information files and the expertise to help write a conversion program to produce the FLDL and FTDL files if necessary)
- (b) on one of the design systems that specifically support Fujitsu software (Daisy, Mentor, Valid, HP 9000) either at the customer's workplace or in one of the Technical Resource Centers
- (c) on ViewCAD either on the customer's own Sun equipment or at a Technical Resource Center.

1

Chapter 3 – Design Procedures

Contents of This Chapter

- 3.1 Introduction
 - 3.2 ViewCAD Design Procedures
 - 3.3 Generic Workstation Design Procedures
 - 3.4 Post-Design Process
-

3.1 Introduction

This section of the data book explains the steps necessary to implement an ASIC design in one of Fujitsu's CMOS technologies using a CAE (computer-aided engineering) workstation. Designs can be implemented with Fujitsu's ViewCAD design software or with one of the CAE systems or software applications that support Fujitsu designs.

3.2 ViewCAD Design Procedures

Fujitsu developed the ViewCAD design software to complement a wide range of customer third party design tools. It includes:

- A Schematic Capture Module utilizing the XWindow System
- A Logic Design Rule Check Module that screens for design violations in the areas of fanout and drive, gate count, I/O requirements, etc.
- A Test Data or Waveform Entry Module for test vector entry
- An Interactive Simulation Module that replicates the Fujitsu mainframe for both functional and timing simulation
- Conversion Modules to define the net list and test vectors in the FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Data Description Language) formats required by Fujitsu's host mainframe.

Figure 3-1 shows the ASIC design flow using ViewCAD. This design flow includes the use of schematic capture and test data generated on other workstations as well as on ViewCAD. The numbers on the left side of Figure 3-1 correspond to the numbers of the paragraphs below that explain the corresponding portion of the figure.

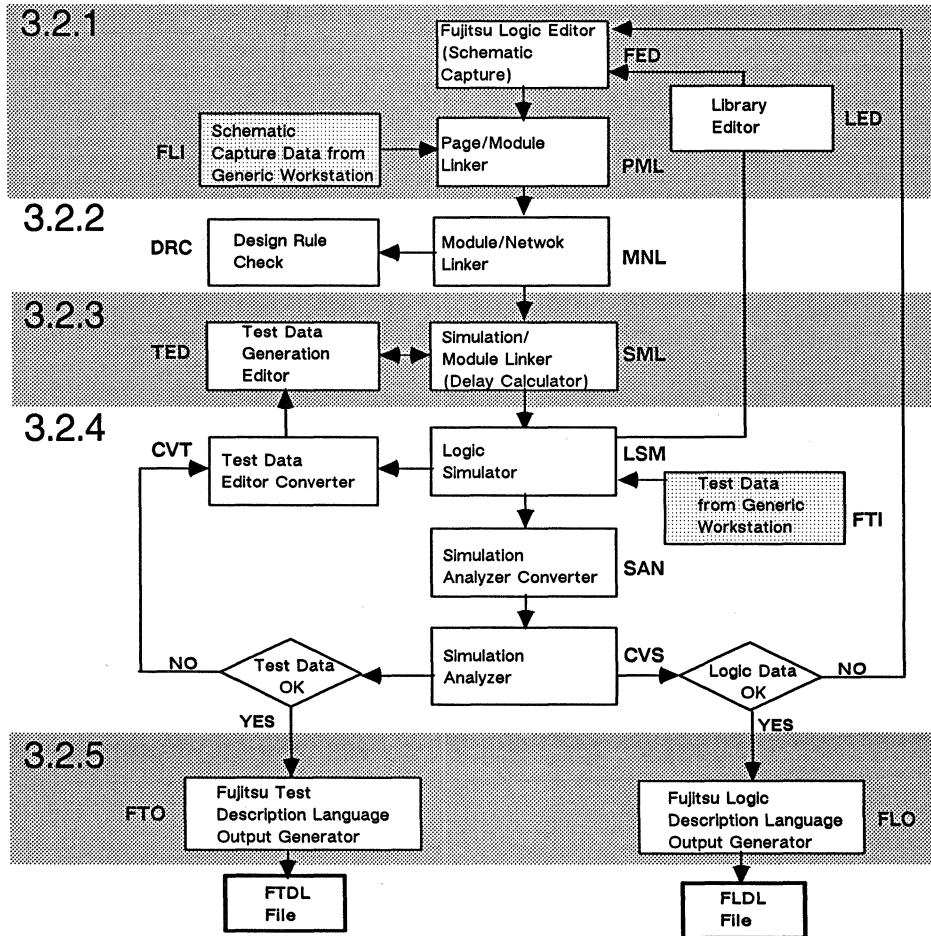


Figure 3-1. ASIC Design Flow with ViewCAD

3.2.1 Schematic Capture

ViewCAD users accomplish logic circuit entry (schematic capture) through the Fujitsu Schematic Editor (FED) module. After running a setup utility requiring the entry of the design name, technology series, and package type, users can insert unit cells and connect them to create circuit diagrams and see a graphic representation of the resulting schematic. The Schematic Editor also provides a basic verification routine. If the schematic has already been entered in another CAE system, it can be converted to ViewCAD-compatible data by the FLDL-to-ViewCAD translator (FLI) module. A Library Editor (LED) module is available to specify design hierarchies, create user macros, and implement blocks in partitioned arrays. ViewCAD allows the user to go back and forth between LED and FED to facilitate the development of complex hierarchical designs.

The designer then uses a Page/Module Linker (PML) module to link pages, ensuring connectivity between the pages of the schematic.

3.2.2 Logic Design Rule Check

DRC, ViewCAD's Design Rule Check module, examines the data files produced by the editor and page linker modules for conformity to the design rules of the CMOS technology in which the design is executed.

Subsequently a Module/Network Linker (MNL) is run on the PML file to expand macros and link the levels of the design hierarchy to prepare the data for the logic simulator.

3.2.3 Circuit Test Data Entry

The designer then provides the Test Data Editor (TED) with test signals for the simulator. Like the schematic capture module, the test data generator displays the data graphically. It allows the user to create and modify signal data and to prepare the data for the simulator module by saving it in a format that the simulator understands. If test data has already been prepared on another CAE system, it can be converted to data usable to the Test Data Editor.

The Simulation Module Linker (SML), which takes the output of the Module/Network Linker and generates the delay estimates for the logic simulator, is run before the logic simulator can be executed.

3.2.4 Simulation and Analysis

The Logic Simulator Module (LSM) reads the data created by SML and combines it with the test information in the TED file to run a simulation of the design.

The Test Data Editor Converter (CVT) then converts the output of the simulation module (LSM) back into a TED file. It provides the path from the simulator back to TED so that output that was previously given an undefined value of "X" can be assigned actual simulated values.

The Simulation Analyzer Converter (CVS) translates the output of the logic simulator (LSM) into an acceptable format for the simulation analyzer.

The Simulation Analyzer Module (SAN) analyzes the output from the simulator to determine whether it performs as it was intended to. SAN allows the user to display the simulation output and manipulate the display to help the user analyze the output.

3.2.5 Data Conversion for Mainframe Interface

The last step in the implementation of an ASIC design on ViewCAD is the generation of the all-important FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Description Language) files.

After any design errors that may have been found by simulation and analysis have been corrected in the schematic capture module, the designer runs the Fujitsu Logic Language Output Generator (FLO) module to convert the schematic data into an FLDL file for use on Fujitsu's host mainframe.

If any errors in test data are discovered during the simulation analysis process, the test data can be sent back to the Test Data Editor Converter Module to be reconverted into a form that the test Data Editor understands (since the errors must be corrected in the Test Data Editor module). After

error correction or if no errors are found, the designer sends the test data file to the Fujitsu Test Description Language Output Generator (FTO) module for conversion into an FTDL file for use on the mainframe.

3.3 Generic Workstation Design Procedures

Fujitsu provides ASIC Design Software Kits for designers using some of the popular design tools on generic workstations. The kits offer support for Daisy, Mentor, Valid, and HP9000 and include:

- Fujitsu Symbol Model Libraries for the CAE system's schematic capture module
- A Logic Design Rule Check module
- Fujitsu Timing Model Libraries for the system's simulator
- A Delay Calculator module
- Conversion Modules to define the net list and test vectors in the FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Description Language) formats required by host mainframe computer.

These Fujitsu-supplied software modules are shown in boldface boxes in the diagram in Figure 3-2.

In addition, Fujitsu now offers FAME (Fujitsu's ASIC Management Environment), a menu-driven design management program that enables the user to select the technology, the approximate gate count and I/O, pinout, and the package requirements, and to create a design database that is referenced by the other modules to assure correct-by-construction design. FAME includes a test vector module that creates test vectors automatically for complex functions, assists in defining test groupings, cycle times, and strobe settings, and checks created test files against restrictions.

Fujitsu designs are also supported by several high-performance third party CAE tools. These include:

- Verilog-XL® (Gateway Design Automation) mixed-mode system simulator
- LASAR Version 6 (Teradyne) design simulator and test program generator with fault simulation
- HILO-3® (GenRad) design verification, fault simulation, and test generation tools
- IKOS® 800 logic validation hardware accelerator
- Synopsys Design Compiler® interactive behavioral/logic synthesizer

Figure 3-2 shows a flowchart of the generic workstation-based design process. Because the function and file names used by each different CAE system may differ, generalized names for each operation are used rather than system-specific names in the following list of steps.

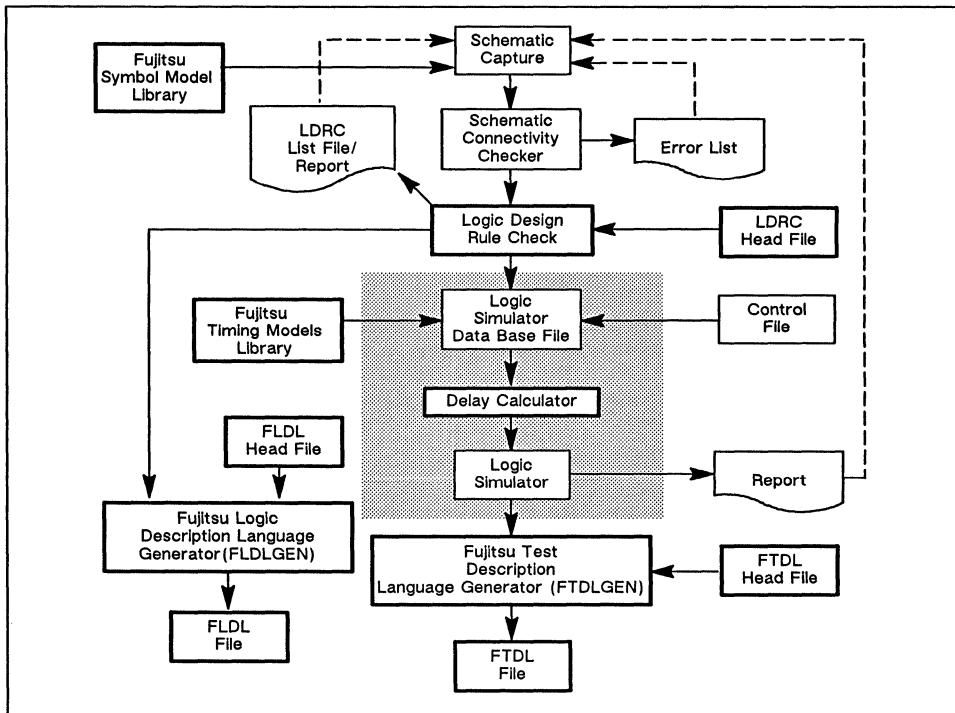


Figure 3-2. Generic Workstation Design Flow

3.3.1 Schematic Capture

Logic circuit entry (schematic capture) is the first step in the generic design automation process. The designer uses the drawing editor program of the applicable workstation software and Fujitsu-supplied symbol model libraries for schematic capture. In most of the Fujitsu-compatible CAE applications, as in ViewCAD, circuits can be defined as macros, for use as sub-parts of other circuits.

3.3.2 Schematic Connectivity Checker/Page Compiler.

After the schematic has been entered, it is scrutinized for violation of design rules by the connectivity checking program of the applicable software. The connectivity check produces a list file of the schematic and an error report. The error report lists common violations of design rules of the technology being used, such as unit cells having unconnected inputs and/or outputs, unnamed signals, and signals having multiple names. Errors detected at this level can be easily corrected by going back into the schematic drawing editor program in which schematic capture was performed.

3.3.3 Logic Design Rule Check

The Logic Design Rule Check (LDRC) module is Fujitsu software, written specifically for each technology to check gate array designs. This program is run before simulation because it catches

errors that, undetected under normal workstation design rules, often cannot be tolerated in a Fujitsu gate array. Even a seemingly small design flaw undetected prior to simulation may be severe enough to invalidate the functional simulation of the design and any test signal data that may be generated from as a result. LDRC checks that the design conforms to the logic design rules applicable to all Fujitsu designs, to those unique to a technology and to those required by the chosen package type. When hierarchy is used, LDRC checks for hierarchy violations.

In order to tailor the LDRC to a particular technology, device, and package, the customer enters required information via an LDRC Head File, which supplies the device and package name and sets the LDRC to output information in the form of a report either on all nets or on only nets that contain errors.

LDRC Report

When the LDRC is finished running, it produces a report containing the following information:

- (a) errors, alarms, and warnings of detected violations
- (b) chip information such as:
 - number of basic cells used vs. cells available
 - number of unit cells and of different unit cell types
 - total number of unit cell terminals vs. number of connected unit cell terminals
 - total number of nets
 - total number of external input, output, and bus terminals
 - package name
 - signal pins used and maximum number of signal pins available
- (c) loading unit check list (a list of the load units associated with each input and output signal)

Errors detected during LDRC can now be corrected before the Logic Simulation Program is run.

3.3.4 Logic Simulation

The steps that make up the logic simulation process vary between workstations. For some workstations, logic simulation is all one step (see the shaded box in Figure 3-2), while for others it is three separate steps:

- (a) logic simulator data base file compilation
- (b) delay calculation
- (c) logic simulation

Logic Simulator Data Base File

The logic simulator data base file uses a Fujitsu-supplied library to apply behavioral characteristics such as component functions, delay parameters, loading factors, and minimum pulse width, set-up time, and hold time for flip-flops. These values are supplied by the Fujitsu libraries for the appropriate technology. Input stimulus to the circuit is supplied by the designer in the form of the Control File.

Delay Calculator

Fujitsu provides the program for performing the delay timing calculations. The execution of the program calculates the delay times unique to each net in accordance with the loading condition

(fan-out and hierarchy) in the schematic data file. These calculated delays are representative of pre-layout loading conditions.

The calculations for metal loading are based on the same look-up tables and load equations used in the Design Manual. These loads are subject to change after layout, reflecting the actual metal loads experienced.

Logic Simulator

The event-driven logic simulator evaluates the outputs of each gate as a function of its inputs and displays the results as either a waveform drawing or as a data file. Workstation simulations performed under the influence of the Delay Calculator are vitally important to verification of design functionality and to the creation of successful test vectors. Using in-circuit application stimulus from the Logic Simulator Data Base File, simulations are executed in minimum, nominal, and maximum modes, with timing checks enabled, to ensure that the design is responding as expected and is stable under all conditions. The results are written to a print-on-change file, which is a list of the signals that changed state, their new state, and the time at which they changed.

3.3.5 FLDL Generator

Any errors found by the logic simulation process can be corrected at this point before Fujitsu's Logic Design Language generator (FLDLGEN) program is run on the schematic data file to create the FLDL file. The purpose of the FLDL file is to provide information to the host mainframe for automatic layout and logic simulation. An FLDL head file must be created by the customer containing the customer's name, the workstation type, the revision, the date, and the designer. The FLDLGEN program receives input from the FLDL Head File and the schematic data base file created at schematic capture and amended if necessary according to the results of the LDRC and Logic Simulation. The FLDLGEN program can then create a Logic Description (FLDL) file that describes the customer's design for the mainframe software.

3.3.6 FTDL Generator

The FTDL Generator (FTDLGEN) is a conversion program that translates the Logic Simulator's output file into Fujitsu's Test Description Language. In the process of doing this, it applies Fujitsu tester restrictions to the simulator results. If any signal or timing violations are detected, the operator is informed so that the necessary changes can be made to the data file. The final output file of the FTDL Generator becomes the FTDL File, that is, the test vectors for the mainframe simulator as well as for the LSI tester.

3.4 Post-Design Process

At this point, the customer has gone as far as possible in designing a CMOS gate array on a CAE workstation. Now the design is transferred to the mainframe environment at one of the Technical Resource Centers for mainframe simulation on a Fujitsu M780 35 mips computer. This process is described in more detail in Chapter 6.

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Chapter 4 – Design Considerations

Contents of This Chapter

- 4.1 Introduction
 - 4.2 Logic Design Considerations
 - 4.3 Designing for Reliability and Testability
 - 4.4 Designing for Speed
 - 4.5 Bus Circuit Design
 - 4.6 I/O Design
 - 4.7 Designing for Scan Test Technology
-

4.1 Introduction

This section of the data book gives an overview of the logic and I/O design considerations that must be kept in mind to implement a successful design is one of Fujitsu's CMOS technologies. Specific design recommendations for each technology can be found in the Design Manual for that technology.

4.2 Logic Design Considerations

In order to benefit from fully automated layout, a designer may use no more than 90% of the actual cell count of an AV or UHB gate array. The actual cell count is the number of basic cells used in the device. It is important to note, however, that this percentage may vary with device type as well as technology.

In Fujitsu's channeled CMOS technologies, the unit cells are grouped in single or double columns alternating with wiring channels. Within the columnar architectures, unit cells are always constructed on one single or double column, i.e., a unit cell cannot bridge the wiring channel between two basic cell columns. This limits the number and complexity of unit cells that can be placed on a double or single column.

The number of inputs and outputs and therefore input and output buffers required also limit the number of basic cells available for logic design in most technologies.

4.3 Designing for Reliability and Testability

The following considerations must be made to ensure maximum testability and therefore reliability of a design:

- (a) External signal paths must be interfaced to the array by an I/O buffer.
- (b) The outputs of a unit cell other than 3-state bus macros may not be wire-ANDed. Generally, if output functions must be tied together, they must be combined through a logic function.
- (c) Only one I/O buffer cell can be connected to an external terminal.
- (d) Inputs to the same cell may not be tied together.
- (e) Unused inputs must be tied high or low, never left floating.

- 1**
- (f) At least one output of a unit cell must be connected.
 - (g) Functions such as one-shots and other monostable or astable circuits cannot be incorporated into a Fujitsu CMOS gate array. All logic state changes detected at the output of the array must be predictable for the purpose of test, and as such, be the direct result of changes of input stimulus. Series inverters must not be used for the purpose of creating a delay.
 - (h) Circuits incorporating sequential devices (for instance, flip-flops, counters, shift registers, and so on) must have a traceable method of initialization designed into the circuit, independent of feedback loops.
 - (i) No logic function should be incorporated within the array if it cannot be directly or indirectly set or initialized from a primary input.

Designers have two choices for initialization:

- (1) Supply an external signal (for CLEAR, LOAD, etc.).
- (2) Supply known inputs and allow time for them to propagate through the circuit. If the propagation method is used, UNKNOWN ("X" state) must be an acceptable output state until the initialization is completed.

4.4 Designing for Speed

In general, signal delays are caused by the signal having to travel through more gates or over longer distances, especially to enter a different block in gate arrays having block architecture (partitioned arrays). Delay is proportional to length of interconnection metal along which the signal must travel. The following recommendations are therefore made to optimize overall design speed by minimizing the interconnect metal length.

4.4.1 Interblock Connections

Devices that are not physically partitioned do not allow the designer to control relative path lengths. It is highly recommended, therefore, to design hierarchically, dividing the cell into blocks and the blocks into sub-blocks so that functional groups of unit cells are laid out in close proximity and signals have less far to travel. When it becomes necessary to link blocks, the use of high-power "high-drive" unit cells is recommended to drive signals in the inter-block metal.

4.4.2 Clock Line Design

A clock network is a circuit used for the efficient distribution of an external clock input to internal sequential and combinatorial unit cells clock. Clock skew is the differential delay of a clock signal as it proceeds through a system; it is determined by the types and relative positions of the gates and blocks within the array. Clock networks must be optimized to minimize skews for both internal and inter-chip clock distribution to assure high-speed operation.

Optimization of clock networks is made possible by using dedicated input buffers called clock input buffers and dedicated unit cells called clock distribution buffers.

Clocks must enter the array through the clock input buffers. They should be further distributed via the clock distribution buffers. Proper use of clock buffers to boost signal strength and balance loads reduces the problems of clock skew and clock pulse variation. The locations of clock input buffers for signals with frequencies greater than 5 MHz are limited to paths on two sides of the die; the number of such buffers is limited depending on the CMOS technology used.

External clock signals must be wired in parallel with chips; once inside the chip, clock signals must be wired in parallel with logic blocks.

4.4.3 Delay Unit Cells

Fujitsu supplies delay unit cells to assist the designer in solving timing problems such as set-up and hold time requirements. The designer should not, however, use delay cells to construct asynchronous circuits (one-shots or glitch generators).

4.5 Bus Circuit Design

The AV (AV, AVB, AVL, and AVM) Gate Array family has no 3-state buses internal to the array. As a result, busing is accomplished through one-way multiplex networks. The UHB technology has special provisions for implementing high-performance internal 3-state buses. The internal 3-state bus can be implemented on the chip using bus driver cells and bus terminators, which maintain the last logic level on each bus line when all bus drivers switch to their high impedance state. The bus terminator maintains this logic level until any bus driver begins to drive the bus line. The bus terminator is invisible to a logic designer; it will be connected to each of the bus lines automatically by the mainframe CAD system. It uses only one basic cell per bus line.

The number of internal 3-state buses permitted depends on the technology and on the size of the gate array and the bus width (number of bits per bus) required.

4.6 I/O Design

4.6.1 Pin Assignment Guidelines

The following parameters apply to the assignment of I/O pins:

- (a) All VSS pins must be tied to ground.
- (b) All VDD pins must be tied to 5 volts.
- (c) Voltage and ground pins are predetermined by the package type and cannot be altered.
- (d) Pins designated "No Connection" cannot be used.
- (e) Additional VSS and VDD pins may not be assigned by the designer without first negotiating this deviation with Fujitsu.
- (f) Fujitsu recommends that the designer assign the pin numbers to the circuit in the *ASSIGN or *OPTION section of FLDL or submit the complete pin assignment table with the design. It is also possible to allow the Technical Resource Center to do the assignment automatically on the mainframe or manually from a customer-supplied form.

4.6.2 Simultaneously Switching Outputs (SSOs)

Outputs are defined as switching simultaneously when they switch from a logic low (or a high impedance state) to a logic high or switch from a logic high (or high impedance state) to a logic low within 20 nanoseconds of each other.

When a number of outputs switch from high to low simultaneously, a problem condition may arise when the ground potential is momentarily pulled up from 0 volts to a more positive level. This momentary tug on ground can appear as noise spikes or ringing. It is possible, with insufficient Vss pins, for the ground plane to be pulled up to a point where the threshold limit for VIH is violated.

When the ground level is raised by the noise, the input threshold (V_{IH}) of the gates is also raised, relatively, for the duration of the impulse, as illustrated in Figure 4-1. This could cause logic high outputs close to the V_{IH} (minimum) threshold to momentarily change to logic low.

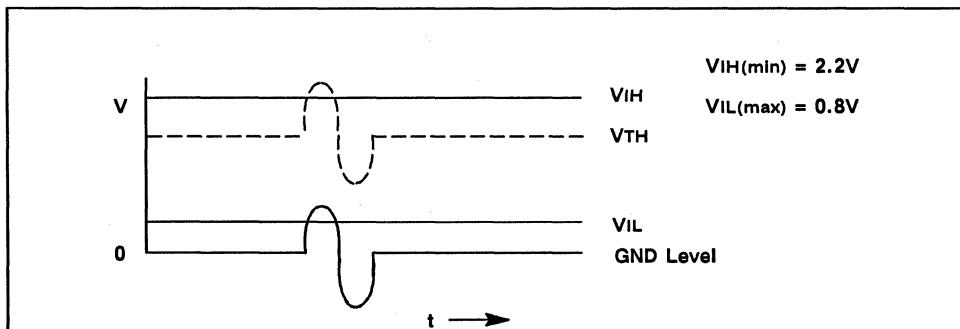


Figure 4-1. SSO-Generated Noise

The intensity of the effect of SSOs is determined by:

- the number of SSOs
- the density and distribution of SSOs in the package
- the size of the load (capacitance) being driven

To prevent their interference with the signals on other outputs, SSOs must be grouped around ground pins. The number of SSOs allowed in a package is restricted by the number of ground pins available, their location on the package, and the drive capability of the output buffers.

Different CMOS technologies have different rules and guidelines regarding number of SSOs per ground pin. A general rule is to use one ground pin for each group of ten simultaneously switching low power outputs or 30 non-simultaneous outputs. For example, in a package with two V_{SS} pins, a maximum of 20 low power outputs may switch simultaneously.

Asynchronous inputs such as clock, clear, and preset should be physically isolated from SSOs. It is better to place these inputs near a ground pin (if one is available) away from the SSOs. Asynchronous inputs should not be placed on the corners of the packages, especially when the chip is packaged in DIP. Corner DIP pins have the longest lead lengths and therefore the greatest inductance. Outputs to be used as clock, preset, and clear for other devices should be similarly physically isolated. In partitioned chips, pins should be grouped by internal blocks to keep internal interconnect wiring as short as possible.

4.6.3 Test Pins

To facilitate testing, external pins should be provided whenever conditions warrant. The addition of supplementary test pins often allows the reduction of the overall test complexity for a circuit, thus reducing the number of test patterns required and the time necessary to determine functionality of the circuit.

4.7 Designing for Scan Test Technology

Scan testing is a special technique that supplements the customer's submitted test patterns to achieve greater fault coverage, thus assuring both Fujitsu and the customer of a highly reliable gate array. Scan testing is implemented by constructing a circuit that allows Fujitsu ATG (automatic test generation) software to automatically generate the scan test patterns (both applied input stimulus and expected outputs). Scan testing is optional and is offered by Fujitsu for the partitioned arrays of the UHB technology.

The unit cells in a device designed for scan testing are arbitrarily connected by the designer to form an enormous shift register. This shift register can contain up to 3000 stages and is formed by connecting the Q-output of one state to the dedicated scan input (SI) of the next. To implement scan testing, designers use special scan-compatible unit cells for all sequential logic functions. With the use of the serial scan method, the difficult problem of testing a logic circuit containing both combinatorial and sequential logic is simplified to testing combinatorial logic and a shift register.

The scan chain can be considered a data carrier with the ability to carry test input stimulus deep into the design and to apply it to the unit cell(s) under test. Once a unit cell has been tested, its output (test result) may, if necessary, be stored in the scan data chain and be carried out of the design for comparison to that which was expected. To the designer, scan unit cells perform exactly the same as non-scan cells, the only difference being the provision of additional basic cells to facilitate the scan test.

4.7.1 Scan Test Modes

Scan testing consists of two modes of operation: SISO (Scan Input/Scan Output test) mode and TC (Test Clock) mode. Sequential logic is primarily addressed by SISO and combinatorial logic is addressed by TC; the two modes are alternated during the scan test.

4.7.2 Scan Test Signals

Scan test implementation requires the assignment of up to seven dedicated package pins, six of which are in predefined package locations:

XACK – for the SISO A-clock signal

BCK – for the SISO B-clock signal

XSM – for the SISO mode signal

XTCK – for the TC mode clock signal

SDI – for the serial data input to the first device of the scan path from outside the chip. This is the only one of the scan pins that can serve a dual purpose. It may also be used as a principal input during regular operation.

- SDO – for the serial data output from the last device of the scan-configured shift register to the “outside world.” The location of the SDO pin is not fixed, and may be placed by the designer at any convenient location.
- XTST – for the scan test signal. XTST is used only if the isolation of asynchronous functions or non-scan cells is required during scan testing. If no circuit isolation is required, then XTST is not required and is not provided for.
- XMM – for the signal that sets up the compiled cell for test. The pin location of XMM is user defined. This pin is used only in AU series channel-less gate arrays and provided only if compiled cells (RAM or ROM) are a part of the design.
- XTWE – for data to be written into RAM in the TC mode. The pin location of XTWE is user defined. This pin is used only in AU series channel-less gate arrays and provided only if RAM cells are a part of the design.

To implement scan path testing in a device, a designer must use specially designed scan components for all sequential (storage) functions such as flip-flops, latches, and shift registers. The scan test feature cannot be implemented for a gate array employing any non-scan sequential unit cell in any portion of the design, with the exception of certain test mode data latches described for each technology in the appropriate Design Manual. Non-scan sequential functions constructed with combinatorial logic (e.g., NAND-gate flip-flops, NOR-gate flip-flops, etc.) are permitted. If, however, non-scan sequential functions constructed with combinatorial logic are used, then the customer-generated function test will be the only means to exercise the nodes in the associated circuits.

Chapter 5 – Delay Estimation Principles

Contents of This Chapter

- 5.1 Introduction
 - 5.2 Choosing Critical Paths
 - 5.3 Load Units and Loading Guidelines
 - 5.4 The Delay Equation
 - 5.5 Estimating Gate Delay
 - 5.6 Estimating Total Circuit Delay
 - 5.7 Delay Calculations when Load Exceeds CDR
 - 5.8 Delay Calculations and the Operating Environment
 - 5.9 Clock Loading
-

5.1 Introduction

This section of the data book gives an overview of the engineering considerations important to the design of an ASIC using Fujitsu's CMOS technologies. Included are the loading rules for CMOS gate arrays and a demonstration of how to estimate the delay through a circuit. In addition to the basic delay equation, this chapter also considers the loading limitations for clock signals and the effects of the operating environment on typical delay figures.

5.2 Choosing Critical Paths

A critical path is a logic path whose timing requirements must be satisfied to ensure proper system function. In an ordinary synchronous circuit, data propagates from one register through combinatorial logic into another register. For the circuit to function properly, the sum of the clock-to-Q delay of the source register, the propagation delay through the logic, and the set-up time on the target register must be less than the worst-case system clock period. Correct timing of the signal along the critical path guarantees that this condition is met.

Usually, the critical path is the one with the greatest number of gate levels. However, if such a path is speeded up by redesign, another, less complex path may become the new critical path.

For example, in a design in which a path has eight levels of gating, the designer may determine upon inspection that two groups of NAND-NAND structures can be changed to AND-OR inverters, an efficient CMOS implementation that noticeably increases the speed of the path. In this case, after applying DeMorgan's theorem and reducing the result, the designer finds that another path is now the critical path.

Since each logic state sensitizes different branches, logic paths must be analyzed using the inputs (rising or falling) that will actually be applied to them (since rising and falling delays are not equal) to determine the longest path that will be sensitized and ensure that it meets critical path requirements.

The path delay calculation worked through in this section shows how a designer can analyze each element of a Fujitsu CMOS circuit to make sure the design meets critical path requirements. In this case, the effect of a rising input on the sample circuit is calculated as it would be if this were a critical path and the rising input were forcing the transition of interest.

5.3 Load Units and Loading Guidelines

The Fujitsu CMOS load unit (I_{lu}) is the input capacitance of an inverter used as the basic unit for measurement and calculation of capacitive loads presented to unit cells within the gate array. Both the output drive factor of a unit cell and its input load factor are defined in terms of load units. Both factors are listed for each unit cell in the unit cell library for the appropriate technology.

5.3.1 Output Drive Factor

The output drive factor (CDR) is a parameter expressing the load driving capability of a unit cell. Unit cells can drive loads greater than the output drive factor. The performance of CMOS circuits degrades exponentially with increased loading; if too great a load is driven, an exaggerated increase in delay through the unit cell may be experienced.

It is permissible for the load to exceed CDR if the associated additional delays are anticipated and tolerable. Additional calculation factors are required to estimate delays of loads greater than CDR. Figure 5-1 indicates the delays that may be generated when the load exceeds these guidelines.

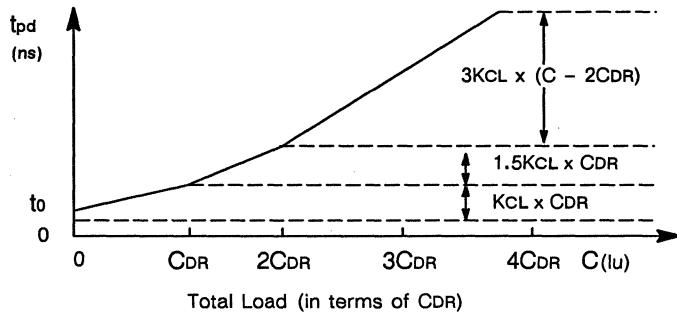


Figure 5-1. Delay Time vs. Loading Factor

5.3.2 Input Load Factor

The input load factor of a unit cell is used to estimate the propagation delay of a critical path in a design. The total propagation delay of a path is defined as the sum of the delay factor of each of the unit cells in the path.

5.3.3 Delay Factor

The delay factor of each unit cell is made up of two types of capacitive loading:

- Load capacitance inherent in the input of each cell (the input loading factor)
- Load capacitance due to the metal interconnection of unit cells (CL)

The total load (C) presented by a unit cell is estimated by adding the total cell input load or NF/O (the input loading factors of all other cells connected to the output network of the cell in question) to the total metal load (CL),

$$\text{or } C = \text{NF/O} + \text{CL}$$

5.4 The Delay Equation

The basic delay equation combines the AC parameters of a cell and its associated capacitive loads to estimate the delay time through the cell. The rise and fall time of a unit cell may not be

symmetrical due to differences in the transconductivity of the N and P transistors as well as to differences in the arrangement of the transistors to form unit cells. The same equation is used with different variables for positive-going and negative-going signals at the unit cell output. These signal polarity variables must be considered separately.

$$t_{up} = t_{0up} + KCL_{up}(NF/O + CL)$$

$$t_{dn} = t_{0dn} + KCL_{dn}(NF/O + CL)$$

where:

t_{0xx} is the circuit delay through the unit cell under no-load conditions (a value given in ns for each cell in the unit cell library).

KCL_{xx} is the load derating constant or delay time per loading unit conversion factor (ns/pF) defined for each unit cell.

NF/O is the sum total of the input loads of all unit cells driven on the net (expressed in load units).

CL is the amount of loading, in load units, on the unit cell output due to interconnect metal (metal load).

The term "net" refers to the network of metal wiring connecting all the unit cells driven by a specified unit cell. Interconnect metal refers to the metal wiring, also called routing metal, that makes up each net.

5.5 Estimating Gate Delay

Figure 5-2 shows a sample circuit for the purposes of demonstrating how the total accumulated delay (tpd) through a short path is estimated.

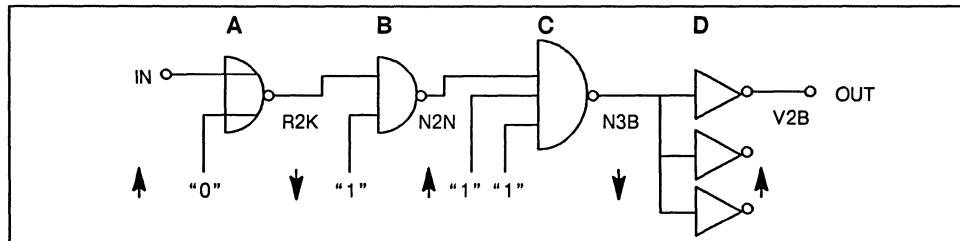


Figure 5-2. Delay Path Sample Circuit

Ordinarily a designer looks up the specifications of each unit cell in the unit cell library of the applicable technology. For this example, however, all of the necessary specifications have been assembled in Table 5-1, using the values for UHB technology.

Table 5-1. AC Parameters of Unit Cells

Cell Function	Cell Name	Basic Cells Used	Input Load Factor	Output Drive Factor	Propagation		Delay Time	
					t _{up}		t _{dn}	
					t ₀	KCL	t ₀	KCL
2-Input NOR	R2K*	2	2	36	0.45	0.14	0.45	0.06
2-Input NAND	N2N	1	1	18	0.37	0.16	0.56	0.14
3-Input NAND	N3B*	3	1	36	1.28	0.08	1.70	0.04
Inverter	V2B	1	2	36	0.25	0.08	0.25	0.05

* These are high drive cells that operate faster than their low drive equivalents under these circumstances.

The delays for rising (t_{up}) and falling (t_{dn}) edges of a pulse can differ widely. Digital pulses are either lengthened or shortened while passing through a unit cell. It is therefore important to calculate the pulse width variations along the entire signal path to verify that pulse width is sufficient to pass through each gate.

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In the example that follows, based on Figure 5-2, calculations are based on a rising pulse entering the input of unit cell A and changing state several times as it proceeds through the sample circuit. To find the total delay for the circuit, it would be necessary to calculate the values resulting from the opposite case, in which a falling pulse enters the circuit at unit cell A.

5.5.1 Delay Parameter for Rising Edge (t_{up})

The unit cell library shows that the delay time (t₀) for an upward transitioning signal at the unit cell output (t_{up}) for R2K, a 2-input NOR, is 0.45. It shows that the load/delay conversion factor for an upward transitioning signal (KCL_{up}) for R2K is 0.14.

5.5.2 Number of Fan-outs (NF/O)

The sample schematic in Figure 5-2 shows that the NF/O, the number of cells that the R2K must drive, is one (an N2N). The unit cell library shows that the N2N has an input load factor of 1 lu.

5.5.3 Number of Driven Inputs (NDI) and Metal Load (CL)

The value for CL is based on the number of inputs the cell in question must drive and is derived from the Estimation Tables for Metal Loading at the beginning of the unit cell library. Table 5-2 is a sample metal load table; each technology and device has unique load/delay characteristics. Since the number of driven inputs (or NDI) for R2K, N2N, and V2B in Figure 5-2 is one, the amount of loading due to metalization (L) is 1.0 lu. The NDI for N3B in Figure 5-2 is three; therefore the CL is 3.0.

Table 5-2. NDI vs. CL*

NDI	CL (f <u>u</u>)
1	1.0
2	2.2
3	3.0
4	3.5
5	3.9
6	4.2
7	4.6
8	4.8
9	4.9
10	5.0

* For a 330UHB gate array.

The value given for CL in the Estimation Tables for Metal Loading is an estimate of the loading effect of the metalization capacitance on the output based on Fujitsu's careful statistical analysis of typical designs. Actual metal loading is based on the effect of the routing and therefore may vary from these estimates. To compensate for this uncertainty, Fujitsu incorporates a $\pm 5\%$ variation into the prelayout delay multipliers. After routing, another set of simulations is run to verify the effect of the actual metal routing.

NOTE: In an array partitioned into blocks, if the interconnected unit cells are located in different blocks, the loading is greatly increased. The designer can avoid this worst-case situation by using the hierarchical approach during the schematic capture process to confine circuits to one block whenever path delay is critical.

5.6 Estimating Total Circuit Delay

Based on the values from Tables 5-1 and 5-2, the propagation delay for R2K in the sample circuit is:

$$\begin{aligned}
 t_{dn}(A) &= t_{0dn} + KCl_{dn}(NF/O + CL) \\
 t_{dn} &= 0.45 + 0.06(1+1.0) \\
 t_{dn} &= 0.45 + 0.06(2.0) \\
 t_{dn} &= 0.45 + 0.12 \\
 t_{dn} &= 0.57 \\
 t_{dn}(A) &= 0.6 \quad (\text{rounded up to the next } 0.1 \text{ ns})
 \end{aligned}$$

The propagation delay for N2N, found by following the same procedure, is:

$$\begin{aligned}
 t_{up}(B) &= t_{0up} + KCl_{up}(NF/O + CL) \\
 t_{up} &= 0.37 + 0.16(1+1.0) \\
 t_{up} &= 0.37 + 0.16(2.0) \\
 t_{up} &= 0.37 + 0.32 \\
 t_{up} &= 0.69 \\
 t_{up}(B) &= 0.7 \quad (\text{rounded up to the next } 0.1 \text{ ns})
 \end{aligned}$$

The propagation delay for N3B, found by following the same procedure, is:

$$\begin{aligned}
 tdn(C) &= t0dn + KCLdn(NF/O + CL) \\
 tdn &= 1.70 + 0.04(3 + 3.0) \\
 tdn &= 1.70 + 0.04(6.0) \\
 tdn &= 1.70 + 0.24 \\
 tdn &= 1.94 \\
 tdn(C) &= 2.0 \quad (\text{rounded up to the next 0.1 ns})
 \end{aligned}$$

The propagation delay for V2B, found by following the same procedure, is:

$$\begin{aligned}
 tup(D) &= t0up + KCLup(NF/O + CL) \\
 tup &= 0.25 + 0.08(1 + 1.0) \\
 tup &= 0.25 + 0.08(2.0) \\
 tup &= 0.25 + 0.16 \\
 tup &= 0.41 \\
 tup(D) &= 0.5 \quad (\text{rounded up to the next 0.1 ns})
 \end{aligned}$$

Therefore, the total delay for the sample circuit shown in Figure 5-2 is:

$$\begin{aligned}
 tpd &= tdn(A) + tup(B) + tdn(C) + tup(D) \\
 tpd &= 0.6 + 0.7 + 2.0 + 0.5 \\
 tpd &= 3.8 \text{ ns}
 \end{aligned}$$

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5.7 Delay Calculations when Loads Exceed CDR

Fujitsu CMOS gate arrays are capable of driving loads beyond their published Output Drive Factor (CDR). It must be emphasized, however, that the delays that result from this practice are considerably increased. Unit cells may be loaded beyond their CDRs provided that the increased delay is acceptable.

Anticipation of the effects of loading beyond the published CDR requires recalculation of delay. Different delay equations must be used depending on the technology being used and the amount that the loading exceeds CDR.

The general formula for loading beyond CDR are listed below; different delay equations must be used depending on the degree that the loading exceeds CDR.

NOTE: All degrees of loading shown below are not necessarily permitted in all technologies and certain technologies may further modify the equations to reflect different characteristics.

When C is CDR or less:

$$tpd = t0 + (KCL \times C) \text{ where } C = NF/O + CL$$

When C is between CDR and 2CDR:

$$tpd = t0 + (KCL \times CDR) + 1.5 KCL(C - CDR)$$

When C is between 2CDR and 4CDR:

$$tpd = t0 + (KCL \times CDR) + 1.5 (KCL \times CDR) + 3KCL(C - 2CDR)$$

When C is greater than 4CDR:

FORBIDDEN

NOTE: Clock networks are never loaded beyond CDR because clock timing is critical to the proper functioning of the gate array. (See Section 5.9)

5.8 Delay Calculations and the Operating Environment

The operating environment of the array can cause variations from the calculated typical delay figures. Influencing factors include ambient temperature, applied voltage, and variations in the manufacturing processes. Figure 5-3 shows how supply voltage and temperature affect the performance of a sample array. It is necessary, therefore, to simulate worst-case conditions during test. Revised estimates of delay under these harsher circumstances may be arrived at by multiplying the typical delay figures by delay multipliers when temperature or supply voltage varies beyond the operating condition specifications published for each technology. The actual multipliers used depend on the device technology and/or the device type.

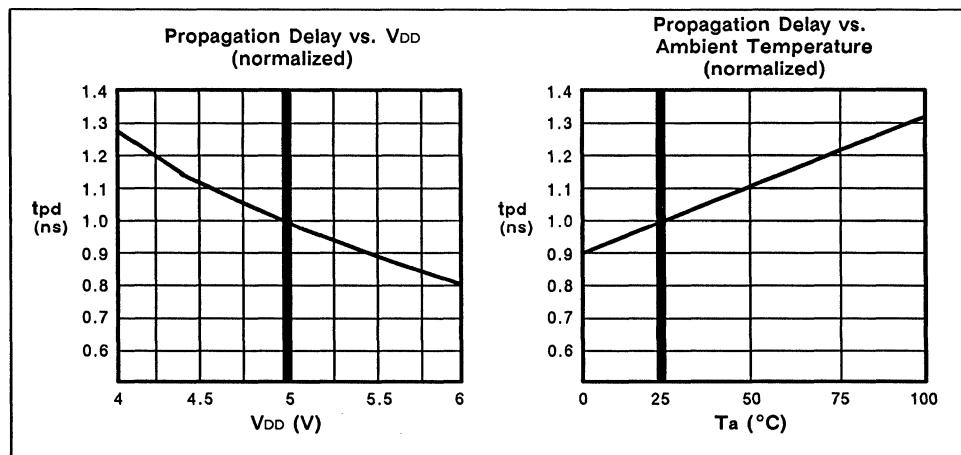


Figure 5-3. Factors Influencing Delay

5.8.1 Minimum/Maximum Delay Multipliers

The minimum delay multiplier and the maximum delay multiplier for typical Fujitsu CMOS technologies given below incorporate process, power supply, and temperature variation.

	Minimum Delay Multiplier (0° C, 2.5V)	Maximum Delay Multiplier (70° C, 4.75V)
UHB Technology	0.35	1.65
AV Technology	0.45	1.60

These delay multipliers are applied in one of two different ways, depending upon whether they are to be used for the optional delay test calculations or for the other tests performed on the mainframe using the information in the FTDL (Fujitsu Test Description Language) file, such as DC test, function test, or high impedance test. More information on the testing process is included in the following section, Chapter 6.

5.8.2 Delay Calculations for Delay Test (AC Test)

The min/max delays for the delay test are determined by taking the sum of the typical delays and multiplying it by the appropriate minimum or maximum delay factor. The maximum delay figure

must be rounded up to the next highest 0.1 ns, while the minimum delay figure must be rounded down to the next lowest 0.1 ns. The result of the equation shown for delay calculation is repeated here and also shown in its modified form. The delay factors used are those for UHB technology.

Typical delay:

$$tpd = 0.6 + 0.7 + 2.0 + 0.5 = 3.8 \text{ ns}$$

Maximum delay (rounded up to 0.1 ns):

$$tpd = (0.6 + 0.7 + 2.0 + 0.5) \times 1.65 = 6.27 = 6.3 \text{ ns}$$

Minimum delay (rounded down to 0.1 ns):

$$tpd = (0.6 + 0.7 + 2.0 + 0.5) \times 0.35 = 1.33 = 1.3 \text{ ns}$$

5.8.3 Delay Calculations for DC Test, Function Test, and High Impedance Test

The minimum and maximum delays for these tests are determined by multiplying the typical delays for each cell individually by the delay factors. The resulting figures for both maximum and minimum delays are rounded up to the next 0.1 ns for each cell. The final figures for each unit cell of the path are totaled. The delay calculation used earlier is repeated here and is also shown calculated for the DC, Function and High Impedance tests. The delay factors used are those for UHB technology.

Typical delay (rounded up to 0.1 ns):

$$tpd = 0.6 + 0.7 + 2.0 + 0.5 = 3.8 \text{ ns}$$

Maximum delay (delay for each gate rounded up to the next 0.1 ns):

$$\begin{aligned} tpd &= (0.6 \times 1.65) + (0.7 \times 1.65) + (2.0 \times 1.65) + (0.5 \times 1.65) = \\ &0.99 + 1.155 + 3.3 + 0.825 = \\ &1.0 + 1.2 + 3.3 + 0.9 = 6.4 \text{ ns} \end{aligned}$$

Minimum delay (delay for each gate rounded up to the next 0.1 ns):

$$\begin{aligned} tpd &= (0.6 \times 0.35) + (0.7 \times 0.35) + (2.0 \times 0.35) + (0.5 \times 0.35) = \\ &0.21 + 0.245 + 0.7 + 0.175 = \\ &0.3 + 0.3 + 0.7 + 0.2 = 1.5 \text{ ns} \end{aligned}$$

Minimum/maximum delays are also calculated this way for minimum clock pulse width, minimum data set-up time, minimum data hold time, preset timing, and clear timing. The values of the maximum and minimum delay multipliers shown above apply to pre-layout calculations only; different factors, specific to each technology, are used for post-layout analysis.

5.9 Clock Loading

It is acceptable, though not a recommended design practice, to load the output of a unit cell that does not carry a clock signal beyond its Output Drive Factor (ODR). To ensure maximum clock accuracy, however, unit cells that output clock signals must never be loaded beyond ODR. These different loading limitations for clock and non-clock unit cells can lead to "race conditions," in which the clock signal arrives at a flip-flop before the data signal set-up time has elapsed. It is therefore most important, when loading a unit cell beyond ODR, to modify the fundamental delay equation using the extra delay factors explained in Section 5.7.

Chapter 6 – Simulation and Test

Contents of This Chapter

- 6.1 Introduction
 - 6.2 Post-Design Simulation and Test
 - 6.3 Engineering Sample Testing
 - 6.4 ATG Testing and Scan Design
-

6.1 Introduction

This section of the data book explains the simulation and testing processes performed by Fujitsu after the customer completes the CMOS gate array design process on a CAE workstation. These simulation and test processes are carried out using the Fujitsu mainframe software at a Technical Resource Center. Simulation and testing ensure that the data collected in the FLDL (Fujitsu Logic Design Language) file and the FTDL (Fujitsu Test Design Language) file result in an error-free layout and a successful ASIC design. Figure 6-1 describes the post-design process in flowchart form.

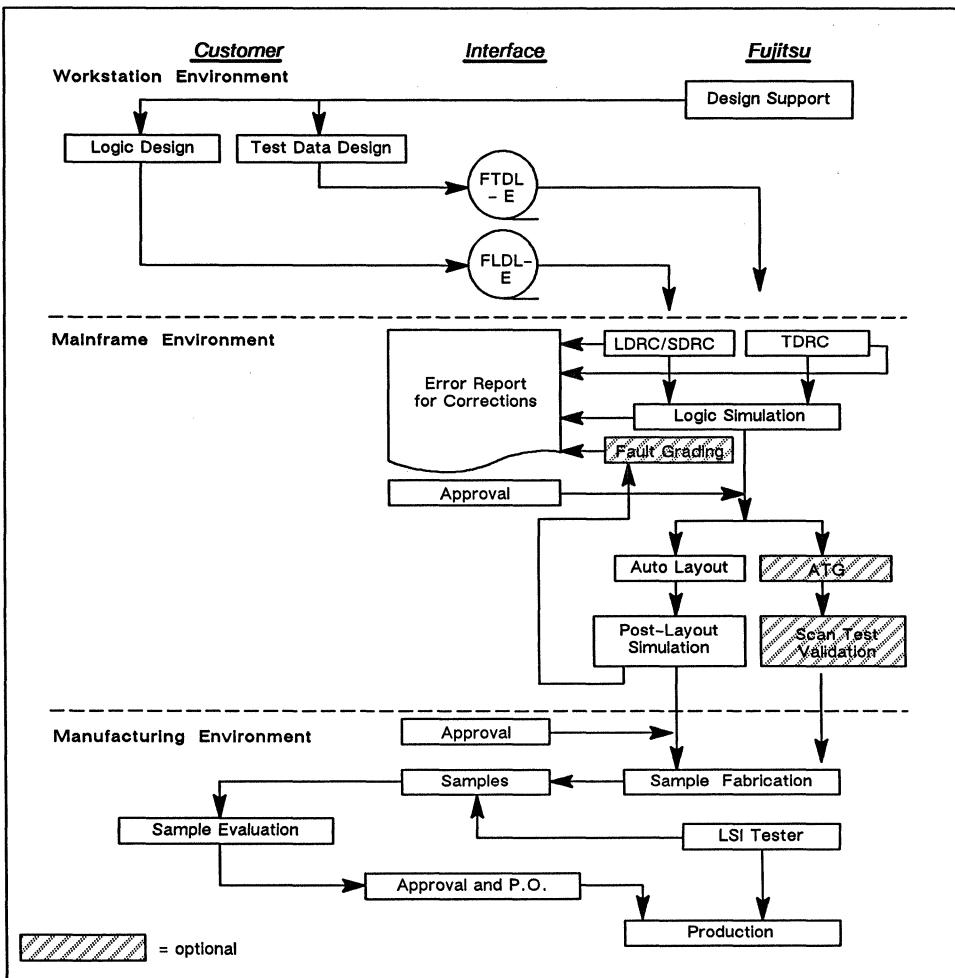


Figure 6-1. Post-Workstation Design Process

6.2 Post-Design Simulation and Test

6.2.1 LDRC and TDRC

The FLDL and FTDL files are provided to a Technical Resource Center usually in the form of magnetic tape or floppy disk. On the mainframe, the FLDL is checked by the mainframe's Logic Design Rule Check (LDRC) to confirm the validity of the logic data and for formatting errors, unconnected inputs and outputs, loading conditions, etc. The FTDL file is checked by a similar mainframe program called the Test Data Rule Check (TDRC), which flags any violations of the published test data restrictions.

6.2.2 Pre-layout Simulation

After the LDRC and TDRC have been run successfully on the FLDL and FTDL, the mainframe pre-layout simulation can be performed. This is a logic simulation run at nominal, minimum, and maximum propagation delay times using estimated metalization capacitance values. If there is no discrepancy between simulation results and the expected outputs, the design is presumed to be correct. One of two simulators, LBS6 or ViewCAD, runs functional simulations and timing verification including the checking of set-up and hold time, pulse width, and removal times.

6.2.3 Automatic Layout

After a successful pre-layout simulation has taken place and customer approval has been obtained, a proprietary Fujitsu mainframe application performs automatic placement and metal interconnection routing.

6.2.4 Fault Grading

After pre-layout simulation is completed, customers have the option of requesting that Fujitsu subject the test data to a process called "fault grading." This CPU-intensive process analyzes the customer's circuit and test data to calculate the percentage of fault coverage. The input test data is analyzed to determine the adequacy of the stimulus patterns to detect any "stuck" (malfunctioning) nodes. The result, a report of all nodes not tested by the stimulus provided, is given to the customer. The customer then has the option of either changing the test vectors or acknowledging that the untested nodes are acceptable.

6.2. 5 Post-Layout Simulation

Post-layout simulation, also known as final validation, is again performed at nominal, minimum, and maximum propagation delay times, but using actual calculated capacitance based on the metal interconnection routing resulting from automatic layout.

6.2.6 Sample Fabrication

After a successful post-layout fabrication has been performed and customer approval has again been obtained, engineering samples of the array are fabricated for customer evaluation.

6.3 Engineering Sample Testing

6.3.1 LSI Tester

Once sample chips have been fabricated, they are tested on the LSI Tester, a test instrument located at the manufacturing facility. Sample chips are tested with input test patterns and expected outputs obtained from the FTDL file.

One of the most important tasks of post-layout simulation is to validate the test vectors for later use on the LSI Tester. For this reason, simulation is executed under conditions adhering as closely as possible to the conditions imposed by the tester. A device that passes all phases of simulation is likely to pass the LSI tester.

The limitations of the LSI Tester places various restrictions upon test data. These restrictions must be respected when preparing the test data pattern and when creating the (stimulus) Control file for running workstation simulations.

A "Summary of Test Data Restrictions" is published for each CMOS Gate Array technology and is included in the design manual for the specific technology.

Test data restrictions involve such issues as the numbers of test patterns acceptable for each test type, the minimum test cycle length, input signal timing, output strobe timing, bidirectional buffer simulation, input and output cycle timing, tester skew, and the treatment of data signals.

Tests performed on the LSI Tester include the function test, the delay test, the DC test, and the high impedance ("Z function") test. Specific data (given in the Design Manual for each technology) must be included in FTDL to perform each of these tests.

6.3.2 Function Test

The function test guarantees the designed function of the gate array by exercising as many of the internal nodes as possible and detecting functional failures. Fujitsu requires the function test because it is the primary means of determining if an ASIC is functioning properly as it comes from manufacturing.

In the course of the function test, input signals are applied in accordance with customer timing specifications, using worst-case input voltage at a clock frequency not to exceed 16 MHz (a period of 63 ns). The dynamic performance of this test also partially verifies the AC characteristics of the device.

The function test may be run in multiple units (blocks), allowing changes to be made in the test vectors to assure thorough testing of the device. The transition from one block to the next requires that the device be powered off, adjustments made to the tester and pins regrouped as required. After all changes have been made, the test is restarted.

The test vectors used in the function test originate with the Print on Change file (the output results of the workstation simulation) and the FTDL head file created by the user. The Print on Change file is a list of the signals sampled and a history of the transitions in a given test block with the actual times that the transitions occurred. The FTDL head file adds the parameters needed to qualify the test data in the Print on Change File: definition of the test cycle time, signal delays, pulse types and pulse widths, and output strobes.

6.3.3 Z-Function Test

The Z-Function test is administered in the last block(s) of the function test. Its purpose is limited to the verification of the high-impedance function of 3-state and bidirectional output buffers. The Z-function test is necessary only when there are two or more logic combinations that can generate the high-impedance state for a given I/O cell. The test can verify all these logic combinations. If only one logic combination generates the high-impedance condition, then the DC test is adequate.

6.3.4 DC Test

The DC test, as its name implies, verifies the DC characteristics of the array. It is not intended to check circuit functionality, but it can be used as a function test of 3-state circuits having only one signal path that generates the high-impedance condition.

The designer supplies the sequence of input signals and expected outputs in the FTDL. These test patterns must generate every possible output state for every type of output and input buffer being used (high, low, and high-impedance).

The DC test applies the specified inputs to measure the following DC parameters:

- (a) Steady State Power Supply Current (IDDS)
- (b) Output High Voltage (VOH)
- (c) Output Low Voltage (VOL)
- (d) Input Leakage Current (ILI)
- (e) High-Impedance Output Leakage Current (ILZ)

6.3.5 Delay Test

The delay test is optional. It is used to verify critical paths or as a means to characterize the device by performing this test on a small number of paths. The purpose of the test is to check that signal paths from various inputs of the chip to their respective outputs meet the customer's standards for minimum and/or maximum delay times. The paths may be sequential and/or combinatorial but only the propagation delay, not the toggle frequency, is measured.

6.4 ATG Testing and Scan Design

ATG testing is a special technique that supplements the customer's submitted test patterns (FTDL) to assure both Fujitsu and the customer of a highly reliable gate array by achieving a high degree of fault coverage. ATG testing is implemented by using scan design techniques described in Section 4.7. Scan test patterns (both applied input stimulus and expected outputs) are automatically generated by Fujitsu's Automatic Test Generator (ATG) software. ATG is offered by Fujitsu for partitioned arrays of the UHB technology and for all arrays in the channel-less gate array technologies.

1

Chapter 7 – Quality and Reliability

Contents of This Chapter

- 7.1 Introduction
 - 7.2 Engineering Testing
 - 7.3 In-process Inspection and Quality Control
 - 7.4 Reliability Testing
 - 7.5 Test Methods and Criteria
 - 7.6 Reliability Theory
-

7.1 Introduction

This section explains Fujitsu's approach to quality and reliability. A single-minded emphasis on quality and a dedication to providing components to meet exacting requirements is the reason Fujitsu integrated circuits are known for their exemplary performance.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. (See Figure 7-1) Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end on the Fujitsu factory floor. It extends to a policy of meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use Fujitsu products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The QC process begins with incoming inspection of all raw materials and ends with shipping tests and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

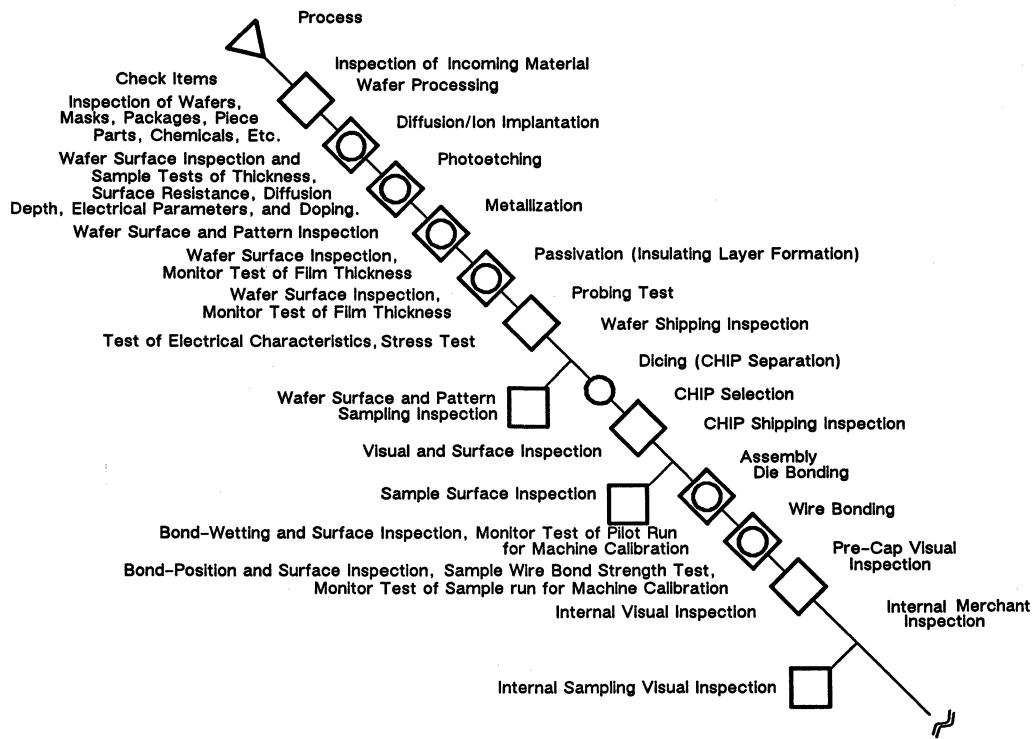


Figure 7-1. Quality Control Flowchart

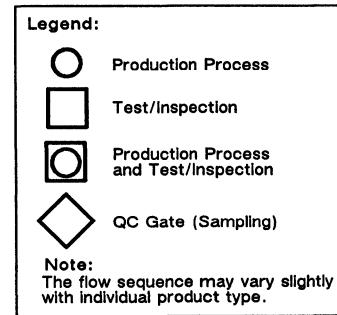
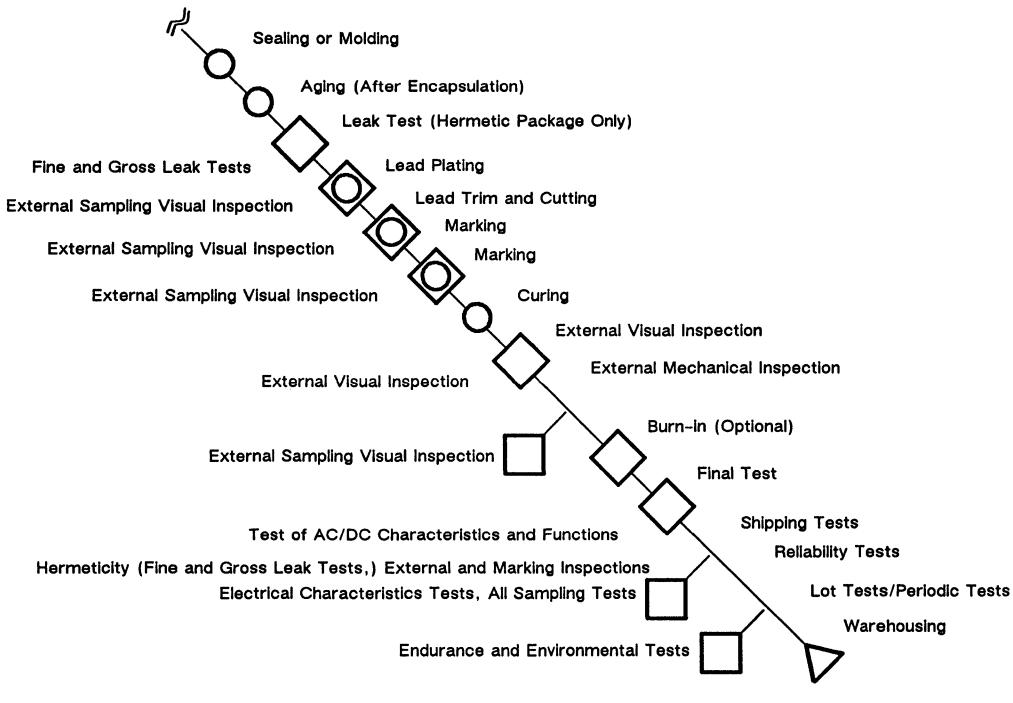


Figure 7-1. Quality Control Flowchart (Continued)

7.2 Engineering Testing

Engineering testing is the heart of reliability and quality control. The reliability engineering department plans and performs most engineering testing. Whenever a device is developed, it must undergo engineering approval tests. After the device passes these tests, production engineering approval tests are performed on a representative sample of the device. All factors that could influence production of the device are examined. Only if all conditions are favorable and the device passes thorough testing, can the new device go into production.

Table 7-1 shows a sampling plan for engineering testing. These tests are in compliance with MIL-STD 883, Class B, as indicated in Table 7-1a. When a change in production (e.g., a material change) is needed, engineering tests are performed on specific items for the change.

Since the representative samples tested must accurately reflect the reliability of the device, the following conditions must also be satisfied: the functions performed by the same basic circuit; the same processing techniques, materials, parts and packages used; and the same processing followed at the same factory.

Table 7-1a. Sampling Plan for Engineering Testing: Endurance Test

Test Items	MIL-STD-883	LTPD* (%)	Acceptance number**	Note
High-temperature storage 150°C	1008 C	7	1	
High-temperature continuous operation 150°C or 125°C	1005 D	7	1	
High-temperature continuous operation 125°C	1055 D	5	2	
Low-temperature continuous operation -55°C	(1055 C or D)	7	1	As applicable
High-temperature high-humidity storage 85°C, 85% RH	—	7	1	Plastic package only
High-temperature high-humidity continuous operation 85°C, 85%RH	(1005 C or D)	7	1	Plastic package only

* Lot test percent defects

** Number of failures permitted per lot

Table 7-1b. Sampling Plan for Engineering Testing: Environmental and Mechanical Test

Test Items	MIL-STD -883	LTPD (%)	Acceptance number	Note
External visual inspection	2009	15	1	Same sample
Physical dimensions	2016	15	1	
Radiophotography	2012	3 devices	0	
Internal visual inspection	2013	15	0	
Lead integrity: Tension Bending stress Lead fatigue	2004 A B1 B 1	15 15 15	0 0 0	Devices which failed in electrical characteristics test are acceptable to this test. Each test is performed on one third of the leads of each sample.
Resistance to soldering heat	—		7	Same sample
Temperature cycling	1010 C	7	1	
Thermal shock	1011 A	7	1	
Vibration, variable-frequency	2007 A			
Mechanical shock	2002 B	10	1	
Constant acceleration	2001 D			
Seal: (Fine and gross leak checks)	1014 A1 C	7 7	1 1	Hermetic package only
Resistance to solvents	2015	40 devices	1	Devices which failed in electrical characteristics test are acceptable to this test.
Solderability (260°C)	2003	15	1	Devices which failed in electrical characteristics test are acceptable to this test.
Solderability (230°C)	—	15	1	Devices which failed in electrical characteristics test are acceptable to this test.
Internal water-vapor content	1018	3 devices	0	Hermetic package only
Electrostatic discharge sensitivity	3015 A	15	1	1
Pressure-Temperature-Humidity Storage (PTHS) 121°C, 2 atm.	—	15	1	Plastic package only

The following tests are performed only when required or when requested by the customer.

Table 7-1c. Sampling Plan for Engineering Testing: Optional Environmental Mechanical Test

Test Items	MIL-STD -883	LTPD (%)	Acceptance number	Note
Bond strength	2011 D(orC)	15	2 wires	34 wires/4 devices
Dle shear strength	2019	3 devices	0	Hermetic package only
Moisture resistance	1004	15	0	
Salt atmosphere (corrosion)	1009 A	15	0	
Vibration fatigue	2005	15	0	
Immersion	1002 B	15	0	
SEM inspection of metalization	2018	3 devices	0	
Particle impact noise detection (PIND) test	2020 B	15	1	Hermetic package only
Lid torque	2024			Frit sealed package only, as applicable
Adhesion of lead finish	2025			As applicable

1

Table 7-1d. Sampling Plan for Engineering Testing: Continuity Test

Test Items	MIL-STD -883	LTPD (%)	Acceptance number	Note
Continuity check	—	5	2	Plastic package only

7.3 In-Process Inspection and Quality Control

Every department involved in the manufacturing process is responsible for the quality-control inspection in its sphere of operation. In-process checks, sampling tests, and other inspections are assigned so that each department has certain allotted tasks for which it takes full responsibility. This total control system has rationalized overall operations dramatically.

7.3.1 In-Process Checks (Including screening)

In-process checks are performed after each key step that is critical to the next process in wafer processing and assembly. Defective or substandard products are weeded out at an early stage. Testing falls into three categories:

- Probe testing, chip selection, and final testing. These are defined for each process.
- Voluntary-checks. These include inspection of the wafer surface after window opening (before the diffusion process) and inspection of the wafer surface after the metalization.
- 100% screening. This includes the aging and visual inspection that are performed during wafer processing and assembly.

7.3.2 In-Process Sampling Test

The in-process sampling test is performed as a part of process quality control. The Manufacturing and QC departments check randomly drawn samples at key points in the manufacturing process to check process and facility conditions. This helps in maintaining product quality at the customary high level. The following items are checked in these sampling inspections or monitoring:

- Surface resistance after diffusion, film thickness, evaporated or sputtered electrode thickness, and device characteristics.

- (b) Product quality (checked by visual inspection of the chip surface).
- (c) Bonding machine calibration, visual inspection and bond strength after wire bonding, product appearance, marking permanency tests.

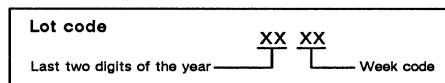
7.3.3 In-Process Inspection

The Manufacturing and QC departments perform stringent quality checks between major processes to ensure the highest quality. Four types of inspections are performed:

- (a) Inspection of incoming materials, parts, and chemicals
- (b) Wafer shipping inspection
- (c) Chip shipping inspection
- (d) Shipping test

7.3.4 Lot Configuration

A "lot" consists of the same devices produced over a stated period, having the same design and using the same processing techniques, materials, and production line. In addition to the Fujitsu logo, part number and others, each IC is marked with a lot code as shown below.



7.4 Reliability Testing

Reliability testing includes three types of tests—lot tests, periodic tests, and “occasional” tests. This section explains the details of each test in turn.

7.4.1 Lot Tests

There are two types of lot tests, called Group A tests and Group B tests. Group A tests and Group B tests are performed on items that are tested regularly, usually every week. Table 7-2 lists the specific lot tests.

Details of individual tests vary with the product under test, but all samples are selected at random from every weekly lot. Tests are not performed in any particular order unless specified, but are performed for each device type.

Note that the high-temperature storage and continuous-operation tests usually take 500 hours, although they may take only 168 hours in special cases. Good samples are returned to their lots after non-destructive testing. No-good samples and samples that have undergone destructive testing are destroyed.

7.4.2 Periodic Tests

Particulars of the periodic tests are also listed in Table 7-2. There are two types of periodic tests: Group C tests and Group D tests. Group C tests are performed on items that are tested regularly, usually every 13 weeks. Group D tests include special reliability tests and very long life tests. The Group D tests are usually done once every 26 weeks.

Details of individual tests vary with the product under test, but all samples are selected at random. Tests are not performed in any particular order unless specified, but are performed for each device type. Note that the high-temperature storage and continuous operation tests for Group C take 1000 hours and those for Group D take 3000 hours.

Table 7-2. Sampling Plan for Reliability Testing

Group	Subgroup	Device classification		Device group 1		Device group 2			
		Test Items		Sampling plan					
A	A1	External visual inspection		100% test of sampled devices (All sampled devices)					
	A2	Electrical Characteristics	Function test	LTPD	5%	Ac=0			
	A3		Static Characteristics	LTPD	5%	Ac=0			
	A4		Dynamic/Switching characteristics	LTPD	5%	Ac=0			
				Sample size	Acceptance number	Sample size	Acceptance number		
B	B1	Physical dimensions		9	1	6	1		
	B2	Environmental tests	Resistance to solvent + Temp-cycling	9	1 ^a	9	1 ^a		
	B3		Thermal shock test	9	1 ^a	9	1 ^a		
	B4-I		Mechanical environmental test	9	1	9	1		
	B4-II	Solderability (230°C, 5s) ¹		9	1	3	1		
	B5	Solderability (260°C, 5s) ¹		9	1	3	1		
	B6	Lead Integrity		9	1 ^a	3	1 ^a		
	B7	Pressure-temperature-humidity storage ²	Pressure-temperature-humidity storage ²	9	1 ^a	3	1 ^a		
	B8		High-temperature storage	14	1 ^a	7	1 ^a		
	B9		Continuous operation	24	1 ^a	11	1 ^a		
C	C1	Endurance test	High-humidity storage 85°C, 85% RH ²	24	1 ^a	11	1 ^a		
	C2		High-temperature storage	14	1 ^a	7	1 ^a		
	C3		Continuous operation	24	1 ^a	11	1 ^a		
D	D1	High-humidity storage 85°C, 85% RH ²		24	1 ^a	11	1 ^a		
	D2	High-temperature storage ⁶		14	—	7	—		
	D3	Continuous operation ⁶		24	—	11	—		
Test cycle: Group A and B for every weekly lot, Group C every 13 weeks, Group D every 26 weeks									
Notes									
1: Electrical reject devices can be used in this test.									
2: These tests are performed on resin-sealed devices.									
3: This test takes 96 hours.									
4: These tests normally take 500 hours. But if no defects are found in the first 168 hours, the lot can be passed and the test may be terminated.									
5: These tests take 1000 hours.									
6: These tests take 3000 hours.									
7: This test takes 48 hours.									
8: These tests take 100 cycles.									

7.4.3 Occasional Tests

Occasional tests are performed on products whenever necessary. The tests are similar to periodic tests, but their details are specified by the QC/Reliability Engineering Division according to the purpose of the test.

7.5 Test Methods and Criteria

The reliability of Fujitsu ICs is assured by severe environmental and endurance testing. Test methods are usually based on Japan Industrial Standards (JIS), the standards of the Electronic Industrial Association of Japan (EIAJ), and MIL standards.

Reliability tests are performed for two reasons. Firstly, they check or guarantee the reliability of a type or a lot according to specified standards. Secondly, they are used to determine the failure rate or mode. The most appropriate test method is chosen for each test, and test results are processed in the most suitable manner. Fujitsu usually performs the tests listed in Tables 7-3, 7-4, and 7-5.

Table 7-3. Example of Reliability Testing

Test Items	MIL-STD-883	Condition
Resistance to soldering heat	—	260°C, 10s
Temperature cycling	1010 C	-65°C (30 min.) to 150°C (30 min.), 100 cycles
Thermal shock	1011 A	0°C (5 min.) to 100°C (5 min.), 100 cycles
Vibration, variable-frequency	2007 A	20 to 2,000Hz, 20G
Mechanical shock	2002 B	1,500G, 0.5ms
Constant acceleration	2001 E	30,000G, 1 min, Y1 only
Final leak ¹	1014 A1	Using compressed helium 99.5 psig, 4 hrs.
Gross leak ¹	1014 C	Using fluorocarbon 75 psig., 1 hr., 125°C
Solderability	—	230°C, 5s
	2003	260°C, 5s
Lead fatigue	2004 B2	0.25kgf, 90°, twice
PTHS/PTHB ²	—	121°C, 2 atm
High-temperature storage	1008 C	150°C, 1,000 hrs.
Continuous operation	1005 A to D	125°C, 1,000 hrs.
High-humidity storage ²	—	85°C, 85%RH, 1,000 hrs.

Notes: 1 Applies to hermetic packages.

2 Applies to hermetic packages.

Table 7-4. Example of Electrical Testing

Circuit classification	Characteristics	Bipolar	MOS
Gates	DC AC	VOH, VOL, I _H , I _L , I _{CC} (IEE) Function	VOH, VOL, I _H , I _L , I _{DD} (I _{sub}) Function
Flip-flops	DC AC	VOH, VOL, I _H , I _L , I _{OH} , I _{CC} (IEE) Function	VOH, VOL, I _H , I _L , I _{DD} (I _{sub}) Function
Shift registers	DC AC	VOH, VOL, I _H , I _L , I _{OH} , I _{CC} (IEE) Function	VOH, VOL, I _H , I _L , I _{DD} (I _{sub}) Function
Memories	DC AC	VOH, VOL, I _H , I _L , I _{CC} (IEE) Function	VOH, VOL, I _H , I _L , (I _{OH}), (I _{OL}) I _{DD} (I _{sub}) Function
Random-logic devices	DC AC	VOH, VOL, I _H , I _L , I _{CC} (IEE) Function	VOH, VOL, I _H , I _L , (I _{OH}), (I _{OL}) I _{DD} (I _{sub}) Function
Analog devices	DC AC	V _{IO} , I _O , I _I , V _{OM} , VOH, VOL, A _V , K _{F2} , N _F	—

Table 7-5. Example of Electrical Criteria

Parameter	Limit value (in multiples of the absolute value)	
	Upper	Lower
V _{OH}	—	Lx0.9
V _{OL}	U x 1.1	—
I _H	U x 2 (No leak: U x 1.1)	—
I _L	U x 1.1 (Leak: U x 2)	—
I _{OH} I _{CC} (IEE) I _{CC} (I _{sub})	U x 1.1 (Leak: U x 2)	—

"U" and "L" stand for the upper and lower limits

7.6 Reliability Theory

7.6.1 Estimating the Failure Rate

The graph of a component failure distribution is usually a downward-bowed curve, what is called the bathtub curve (Figure 7-2). Since semiconductors do not wear out physically, the distribution reflects the initial failure rates. Life tests show that the instantaneous failure rate decreases with time and graphs as a straight line on a Weibull probability sheet. Shape parameter m , which shows the instantaneous failure rate, is between 0.3 and 0.7. (In an exponential distribution, the instantaneous failure rate does not change and $m = 1$. As m becomes smaller than 1, the instantaneous failure rate decreases with time.)

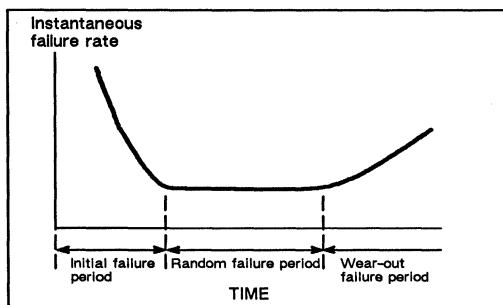


Figure 7-2. Distribution of Component Failure

Usually, the failure rates during the initial and random failure periods are the most important for semiconductors. Figure 7-3 shows an example of life test data graphed on a Weibull probability chart.

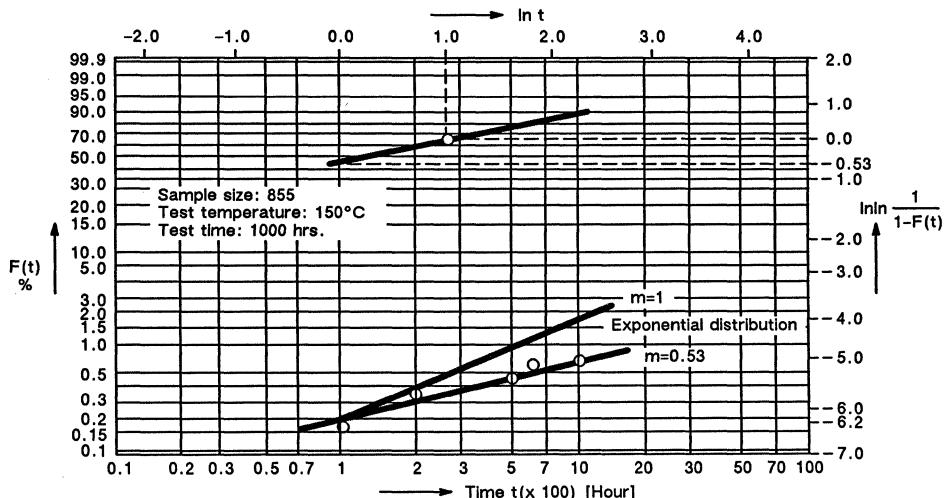


Figure 7-3. Example of High-temperature Storage on MOS IC

7.6.2 Accelerated Life Test

Modern applications require an extremely low failure rate for semiconductors. To guarantee such strict quality, Fujitsu uses an accelerated life test. There is no fixed acceleration rate for semiconductors but, since semiconductor failure is usually caused by physical and chemical changes in materials, an acceleration rate can be calculated from the Arrhenius equation for the progress speed of physical and chemical phenomena (assuming the R is proportional to the degradation speed):

$$R = A \exp(-E_a/kT)$$

R: Reaction rate

A: Proportionally constant

E_a: Activation energy

K: Boltzmann constant

T: Absolute temperature

The proportionality constant A corresponds to the component reliability. The activation energy, E, depends on the component's materials and their combination, but it ranges from 0.3 to 1.35 eV for semiconductors. This equation does not fit the data perfectly because it assumes that the failure rate is affected only by temperature when, in fact, there are many contributing factors. However, the equation does give a good rough fit. Using the equation on data from the accelerated life test, engineers can estimate and guarantee the field failure rate with reasonable accuracy.

The calculation method for the field failure rate is given below for Fujitsu semiconductor products. Although this method is not generally accepted yet, it has been found to be useful.

- (1) Calculate the junction temperature($T_{j(op)}$) for actual use from the temperature rise (ΔT_j) and the ambient temperature (T_a) under an average load (do not use the worst-case load), $T_{j(op)} = \Delta T_j + T_a$.
- (2) Calculate the junction temperature(T_{jt}) for a life test. For a high-temperature storage test, T_{jt} equals T_a (the storage temperature). For a continuous operation test, the temperature rise under load plus the ambient temperature (25°C except for high-temperature operation) for an operating temperature, $T_{jt} = \Delta T_j + T_a$.
- (3) Calculate the acceleration rate (α) from the difference of $T_{j(op)}$ and T_{jt} using Figure 7-3.

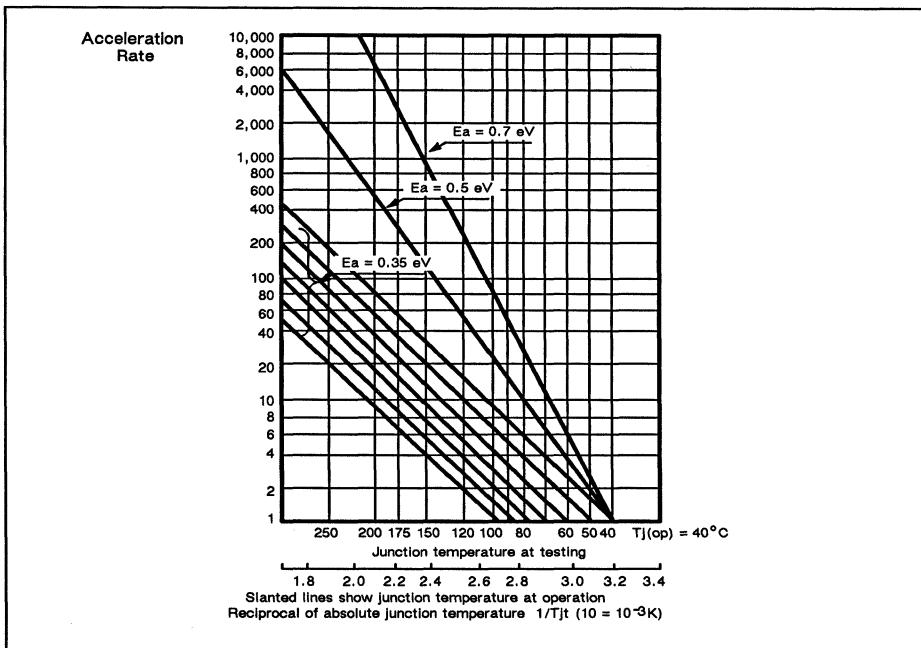


Figure 7-4. Acceleration Rate α vs. Junction Temperature

- (4) If planning reliability testing or calculating reliability in the field from data obtained in steps (1) to (3), determine the coefficient γ for the 60% confidence level in Table 7-6 from the number of defective units allowed or from the total number of failures found in the test.

$$\text{Reliability} = \frac{n}{\alpha NT} \times Y \times 10^9 \text{ [FIT] where:}$$

N: Number of samples

T: Total test time (hrs)

n: Number of failed samples in test

Table 7-6. Determination of coefficient

No. of failures	Confidence level	
	60%	90%
0	(0.92)	(2.30)
1	2.02	3.89
2	1.55	2.66
3	1.39	2.23
4	1.31	2.00
5	1.26	1.85
6	1.22	1.76
7	1.20	1.68
8	1.18	1.62
9	1.16	1.58
10	1.15	1.54

The above equation applies only when n/N is equal to or less than 10% for the total test time, T . If n/N exceeds 10%, use the following method of calculation: divide the total test duration time, T , into subsections, Δt_i ($i = 1, 2, \dots, m$), so that for each Δt_i the failure rate, $(n_{i+1} - n)/(\Delta t_i)$ (where n_i is the cumulative number of failed samples for Δt_i), does not exceed 10%. Calculate $(N - n_i) \Delta t_i$ for each time section Δt_i . Calculate the summation $\sum (N - n_i) \Delta t_i$ for all the time sections in T . The summation $\sum (N - n_i) \Delta t_i$ must then be substituted for NT in the above equation.

7.6.3 Failure and Causes

Circuit format differences, package types, and operating environments can change the mechanisms of IC failures, so it is difficult to foresee which factor will be the most important in a failure mechanism. Figure 7-5 shows specific electrical failures for ICs, their most common causes, and general corrective actions. Causes of IC failures are largely the same as for planar transistor failures, but the following problems are more common or specific to ICs:

- (a) Surface degradation
 - (b) Flaws in an evaporated or sputtered metal film
 - (c) Contact failures due to an increased number of wire bondings per package
 - (d) Package failures due to an increased number of external leads

Table 7-7 lists failures with their most common causes, and Table 7-8 shows the relationship between operating environments and failure causes. Test items can be listed only if the failure cause can be pinpointed by the test.

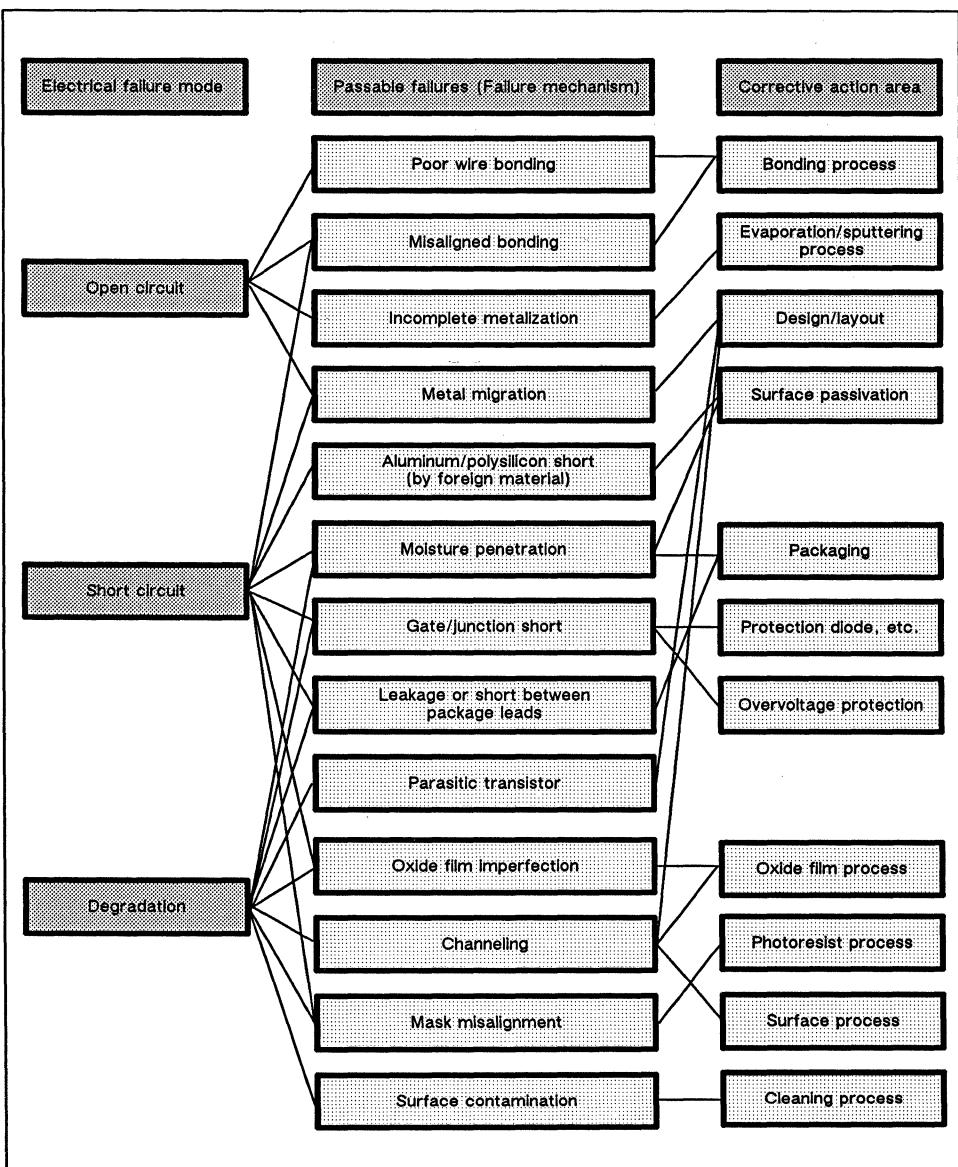


Figure 7-5. Digital IC Failures and Corrective Actions

Table 7-7. Process Defects Analysis

Defect Area	Defect mechanism	Frequency	Source				
			Design	Factory Process Control	Manuf. Tech.	Operator Skill	User Application
Junction (Internal)	Junction failure due to current crowding	High	●				●
	Metal migration	Low	●	●	●	●	
Junction (Surface)	Oxide film Imperfection (Pinhole, crack, void, etc.)	Medium		●		●	
	Impurity contamination	High	●	●		●	
Inter-connection	Metal peeling	Medium		●	●	●	
	Mask misalignment	Medium				●	
	Incomplete metallization	Medium		●	●	●	
	Improper metallization	Medium					
	Metal over-stress	High					●
	Aluminum corrosion	Medium		●	●	●	
	Aluminum migration	Medium	●			●	
Wire	Bonding peel	High			●	●	
	Purple plague	Medium	●		●	●	
	Wire over-stress	High			●		●
	Particle/wire short	Low				●	
Package	Leakage	Medium			●	●	
	Die bond failure	Low	●		●	●	
	Lead breakage	Medium			●		●
	Package corrosion	Medium	●	●	●		●
Others	Chip crack	Medium			●	●	●
	Seal contamination	Low		●		●	

Table 7-8. Relationship between Failure Causes and Analytical Test Methods

Failure Cause	Test											
	Solderability (2003.2)	Temperature Cycling (1010.2)	Thermal shock (1011.2)	Constant Acceleration (2001.2)	Mechanical shock (2002.2)	Vibration, variable frequency (2007.1)	Lead fatigue (2004.2)	Barometric pressure reduced (1001)	Moisture resistance (1004.2)	Salt atmosphere (1009.2)	Vibration fatigue (2005.1)	Vibration noise (2006.1)
Bond integrity (Chip or wire)		●	●	●	●	●					●	●
Cracked chip		●	●		●							●
Internal structural defect					●	●						
Contamination-/ contact-induced short		●		●	●	●					●	●
Wire or chip breakage				●	●	●					●	
Glass crack	●	●	●		●		●	●				
Lead fatigue							●					
Contamination of junction (Surface)	●	●	●									●
Thermal fatigue		●										
Seal integrity		●										
Seal contamination				●	●	●						●
Leakage		●	●				●	●	●	●		
Package/material integrity		●	●		●			●	●	●		

Chapter 8 – Application Notes

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- 8A Developing Test Patterns with Consideration of the Physical Tester
 - 8B Selecting the Best Package for Your ASIC Design
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8A. Developing Test Patterns that Work with the Physical Tester

1.0 Introduction

This application note briefly describes the process of developing test patterns simulation and test of Fujitsu CMOS ASIC designs. This information supplements testing information found in the Design Manual for the appropriate Fujitsu CMOS ASIC technology.

2.0 Tests to be Created

Fujitsu supports five types of test:

1. DC test
2. Dynamic function test
3. High impedance test (Z-function test)
4. Delay test (AC test)
5. Scan test (optional for certain Fujitsu technologies)

The DC test measures DC characteristics such as I_{DDQ} , V_{OH} , V_{OL} , I_{LH} , and I_{LZ} , while the function test screens for manufacturing faults (metal and transistor faults, principally). The Z-function test augments the DC test and is required for circuits in which one or more enable signals from a 3-state buffer can be generated by logic deeper than one gate of complexity within the ASIC device. The delay test may be used to verify critical timing paths that are necessary for proper system operation. Scan test methods may be used to simplify the process of testing for the manufacturing defects traditionally uncovered by the function test. Automatic test generation (ATG) is supported in conjunction with scan testing in the UH, UHB, and AU technologies as an option.

3.0 Overview of Test Vector Creation

For each set of test patterns defined as a test block, the customer must specify input states and output states (in either a vector or wave format), and the timing of inputs and outputs (with bidirectionals being considered both an input and an output). Many designers rely on one of the Fujitsu-supported CAE workstations when generating test vectors, easing the burden of test pattern development. In these cases, the customer creates input stimuli for the workstation simulator, which then generates a print-on-change file containing the resulting output response and the associated input stimulus previously defined by the designer. The print-on-change file is converted by Fujitsu's workstation software into FTDL (Fujitsu Test Description Language), which is the accepted test pattern description format regardless of the method by which patterns are created.

4.0 Developing the Tester Timing Information

Whether or not the patterns are generated on the CAE workstation, it is necessary for the customer to generate in the FTDL file a Common Block file, containing administrative information and

the test type, and a Test Block file, containing the timing information for all chip inputs and outputs by group (discussed further in the Design Manual). The definition of this overall timing is critical to the success of the test program itself. For example, input timing defines when input signals will transition, while output timing defines when outputs will be compared with their expected values or measured at a transition point.

The designer is responsible for specifying the following timing parameters for the Test Block, depending on the specific type of test:

1. Test Cycle
2. Grouping of inputs and, if necessary, outputs and bidirectionals
3. DT (Delay to Transition) time for each input group of NRZ (non-return to zero) signals
4. tp and W_p (delay-to-transition and pulsewidth) times for the positive-going and negative-going pulses (PP and NP) for each input group of RTZ (return to zero) signals
- 5.* STB (delay-to-strobe time) point for each output group
- 6.* DT and STB times for bidirectionals
- 7.** T time in the SPATH statement for AC tests

*Specified in DC, function and Z-function tests

**Applicable only to AC tests.

This timing is established for the entire test block and is invariant until another test block is invoked. Therefore, test pattern timing is periodic, that is, a group of inputs may only transition at the time specified in the Test Block, which is relative to the beginning of the test cycle. This delay to transition time for inputs is programmed for each input group with the tp parameter in the FTDL INTIM or BUSTIM statement.

Similarly, common output groups are strobed, or sampled, periodically at a time determined by the test cycle and the delay-to-strobe time specified in the OUTTIM or BUSTIM statement, or the T parameter in the FTDL SPATH statement in the case of an AC test.

5.0 Determining Input and Output Timing Parameters

During the function test, outputs should stabilize before being strobed. Therefore, the minimum permissible test cycle programmed by the TIMING statement in the Test Block should be set with consideration of the maximum propagation delay from any input to any output, and the respective DT and STB times for those groups should be set far enough apart in time to assure that the outputs are stable under maximum conditions. Similarly, if the output is strobed before the transition, it must be stable under minimum delay conditions.

Test patterns are required to be invariant over minimum and maximum delay conditions. This is verified in simulation by scaling the typical delays by multipliers representing process, temperature, and power supply variations. Similarly, the strobed or expected output states must be identical under typical, maximum, and minimum conditions. If a propagation delay from input to output is greater than the test cycle defined, output states may not fulfill this requirement (see Figure 8A-1). Furthermore, designers should be careful that glitches or short pulses do not occur anywhere within this minimum/maximum window (see Figure 8A-2).

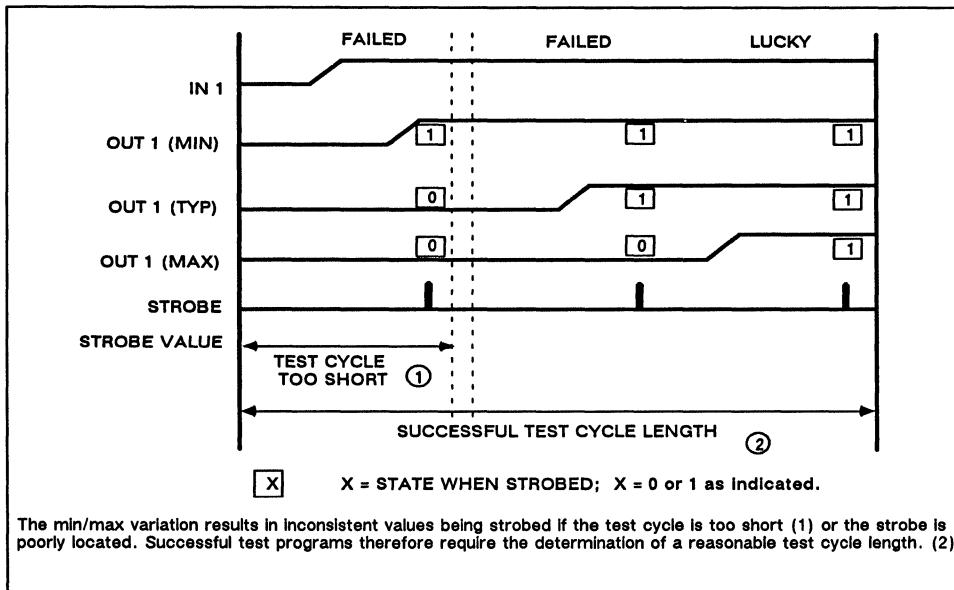


Figure 8A-1. Determining a Successful Test Cycle Length

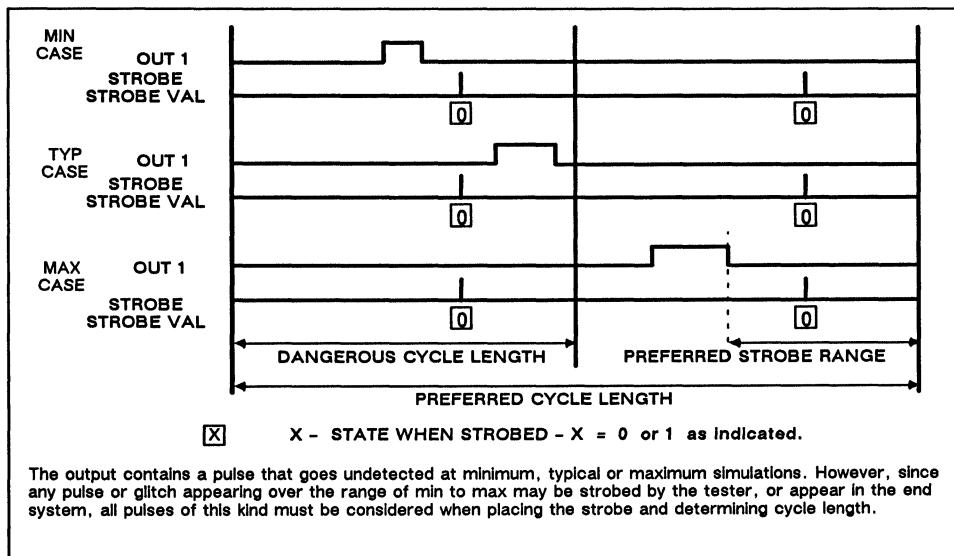


Figure 8A-2. Determining Preferred Cycle Length

6.0 Generating Functional Input Stimulus Given Test Pattern Timing

Issues that must be considered when determining test pattern timing are the relationship between input signals, such as clock/data pairs, which must satisfy set-up and hold times. Other considerations guiding the timing definition are dependent on the particular circuit being tested, and on restrictions imposed by the tester. These restrictions are published in the Summary of Test Data Restriction section of Fujitsu's Design Manuals.

7.0 Tester Skew and its Compensation of Test Timing

The designer must pay particular attention to the issue of tester skew when determining input and output timing for Test Blocks: otherwise, the timing will not correctly represent the behavior of the device under test. Tester skew, specified for each technology in the Summary of Test Data Restrictions, is a result of the variation in the time at which a given signal generator triggers a transition or a comparator measures an output state. Several timings are affected by this skew.

7.1 Input-to-Input Skew

For the purpose of estimating the skew between two signal generators, (one driving data and the other driving its clock, for example), the driver skew, linearity of clocks, clock-to-clock skew, and jitter are collectively called driver accuracy, denoted tDSKEW.

In the case of data/clock pairs, the clocked data may either fail a set-up or hold time, depending on the direction of the skew. Therefore, when determining DT and tp for data/clock pairs, the designer should adjust times to satisfy the following relationships (see Figure 8A-3):

Set-up Time Criteria for Testing: $(tp(CLOCK) - DT(DATA)) \geq ts(MIN) + 2 * tDSKEW$

Hold Time Criteria for Testing: $(DT(DATA) - tp(CLOCK)) \geq th(MIN) + 2 * tDSKEW$

Where $ts(MIN)$ and $th(MIN)$ are the worst case set-up and hold times, respectively, sensitized from the internal circuit to the inputs, tDSKEW is not directly specified in the Summary of Test Data Restrictions; however, TACC, the overall system timing accuracy, is specified and can be substituted for tDSKEW (see Section 7.2).

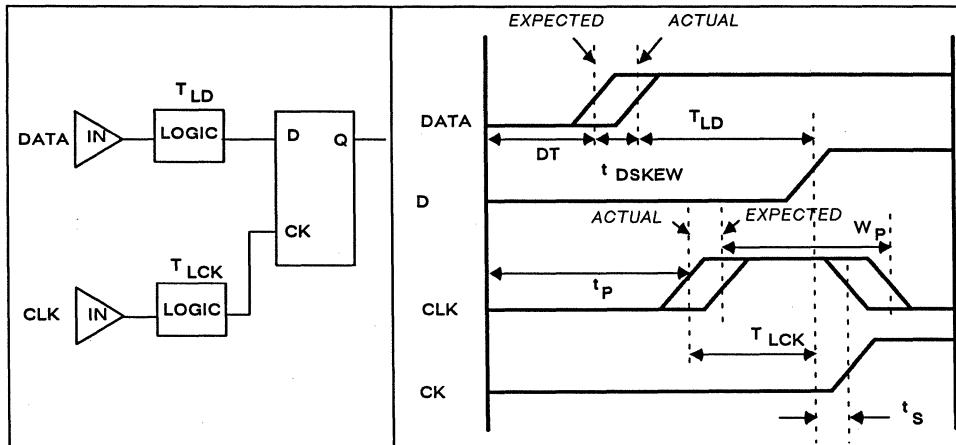


Figure 8A-3. Input-to-Input Skew

7.2 Input-to-Output Skew

In addition to the skew incurred by the signal driver, skew is also introduced by the output comparator of the tester. This skew is dependent on the linearity of the strobe, pin-to-pin skew, skew between dual comparators, and the driver-to-comparator timing error. All factors are considered in the overall system timing accuracy, tACC, which in turn affects output timing as shown in Figure 8A-4.

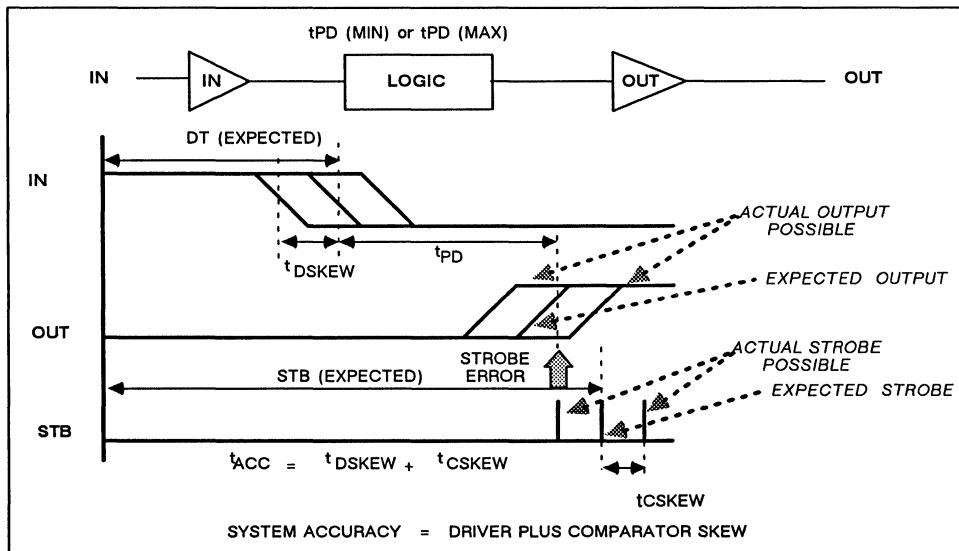


Figure 8A-4. Input-to-Output Skew

7.3 Skew Effect on Input/Output Pairs - Minimum Delay Case

The STB (or T parameter in the SPATH statement) should expect an output transition at a time relative to the stimulated input transition dictated by:

$$(STB - DT) \geq t_{PD(MIN)} - t_{ACC}$$

where STB is the strobe point of the output under consideration, DT is the DT time of the stimulating input of interest, and $t_{PD(MIN)}$ is the minimum propagation delay from this input to the strobed (or measured) output. In the case of the AC test, the quantity $(STB - DT)$ should be replaced by the minimum T parameter in the SPATH statement. Note that if the path delay spans a test cycle boundary, STB should be set to STB plus the test cycle period.

7.4 Skew Effect on Input/Output Pairs - Maximum Delay Case

The complementary case occurs for maximum delay measurements, as described by:

$$(STB - DT) \leq t_{PD(MAX)} + t_{ACC}$$

Note that these guidelines regarding the specification of test data timing as affected by tester skew apply to DC and Z-function tests as well. In these cases, the same rules apply as for the function test.

Again, for the specific values of tACC, and tDSKEW, please refer to the Summary of Test Data Restrictions in the Fujitsu Design Manual for the appropriate technology. A designer interested in a methodical approach to the generation and verification of a good set of test vectors must consider the tester hardware on which it is running. Fujitsu has simplified designer responsibility by providing this information as part of the Test Block Information.

However, a lack of implementation and careful analysis of the timing characteristics of the circuit may result in a poor or unfeasible test, resulting in schedule delays or reduced device yield. Therefore, plan a test approach early, design for testability, and consider the effect and operation of the physical tester.

8B. Selecting the Best Package for Your ASIC Design

1.0 Introduction

The widely varying degrees of complexity (gate count) of Fujitsu's CMOS and BiCMOS devices and the flexibility of their I/O configurations combine to produce devices that can be accommodated in a wide variety of package implementations. With the equally broad selection of packages available from Fujitsu, however, the requirements for package selection go far beyond pin count as the sole determinant of the best package. Selection issues include surface mount versus through-hole, plastic versus ceramic, and exotic versus conventional packaging. In fact, Fujitsu offers over 100 packages and 1000 package-die combinations from which to choose. Compounding the selection problem is the effect of increasingly faster outputs coupled with higher drive and wider bus structures, resulting in greater numbers of simultaneously switching outputs (and thus greater amounts of noise).

The result is that designers are finding ASIC design packaging implementation to be an increasingly complex task. This application note provides information about ASIC packaging that is meant to simplify the designer's task. It provides designers with a review of the various Fujitsu packages and their electrical, thermal, and mechanical characteristics, as well as some problem-solving strategies for their use. The first part (Sections 2.0 and 3.0) addresses system requirements and package availability; the second part (Sections 4.0 and 5.0) discusses noise and thermal issues.

2.0 How System Requirements Affect Package Choice

Section 2.0 presents considerations involved in the selection of packages from a system designer's perspective. Figure 8B-1 lists issues a designer must consider when determining the optimal packaging for an ASIC design.

Manufacturing and Cost-Related Issues	Speed Requirement Issues
Board Integration	Package and Interconnect Delays
Double-sided Component Mounting	The Effect of Package on Noise
Number of Packages	Thermal Considerations
Package Outline Area	
Power Density Limitations	
Producibility Issues	Quality Considerations
Board Layout	Package Quality and Reliability
Package Construction	Number of Devices
Packaging Complexity	Noise
Manufacturing Flow	Thermal Considerations

Figure 8B-1. Considerations for Package Selection

2.1 Manufacturing and Cost-Related Requirements

The manufacturing-related factors discussed below, although not directly related to the design of the device or the number of power and ground pins it requires, are nonetheless important in the choice of an ASIC package.

2.1.1 Board Area

One of the most important issues is the board area consumed by a circuit. Some of the factors affecting overall board density are:

- Integration (gates per square inch of board)
- Double-sided mounting capability (integration)
- Number of packages
- Package outline area
- Additional board space required (for spacing, resistors, capacitors, probe areas, etc.)
- Power density area (discussed in Section 5.0)

The critical issue in board area reduction, however, is overall integration. For example, surface mount devices (SMDs) can be densely mounted on both sides of the board, making them ideal for systems demanding high package integration. But a large design integrated into a few very large Sea-of-Gates arrays, even if packaged in large, through-hole packages, may well consume less board space than the same design using surface mount PLCCs. The PLCC version would require more space because the PLCCs, although small in outline, cannot house as large a die and therefore require the design to be partitioned into a greater number of devices.

Figure 8B-2 illustrates the board area taken up by the outline of each kind of package Fujitsu offers, excluding any area around the package necessary for spacing, decoupling capacitors, series damping resistors, or solder pads.

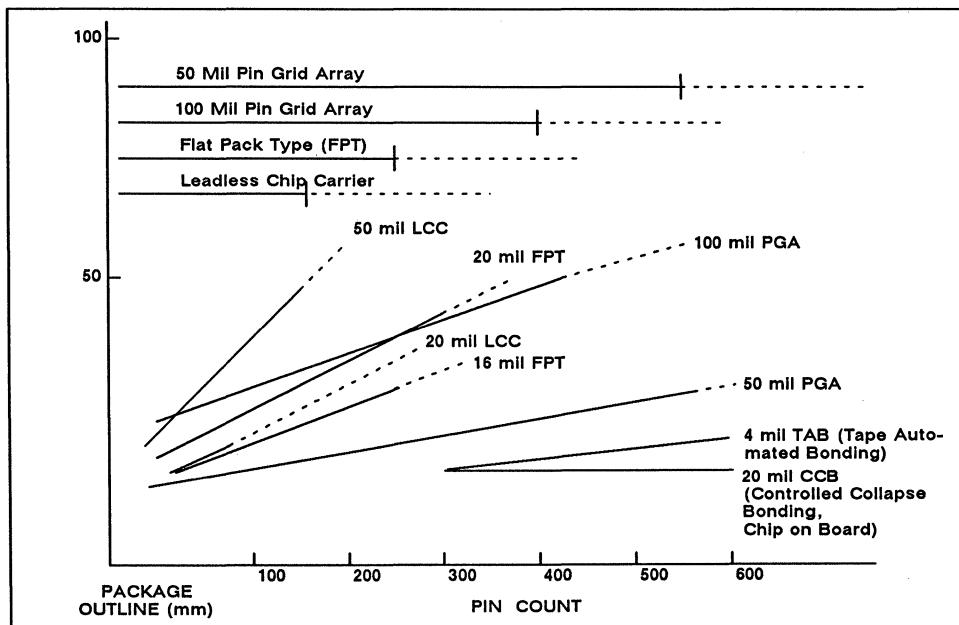


Figure 8B-2. Package Size vs. Pin Count

2.1.2 Board Layout

Restrictions in board layout or construction must be identified and resolved early in the design process. For example, a design containing large buses (16 bits or 32 bits or more) must be split up to comply with SSO restrictions (to maintain proximity to ground pins). Splitting up the buses, however, may result in variations in signal trace length and require extra care in routing. Similarly, flatpacks, a form of SMDs, are a convenient way to support high pin counts in relatively inexpensive plastic packages. However, with pin pitches as narrow as 15 mils ($1\text{ mil} = 1/1000 \text{ of an inch}$), they demand extremely accurate positioning of solder pads. Dense PGAs, on the other hand, provide a spacious 100-mil pin separation, but because of the number of rows of pins, normally require a large number of board layers.

2.1.3 Producibility

Though some unusual packages may appear to promise ultra-high speed or dense integration or minimized component/board cost, the designer must always keep manufacturability in mind. The cost of a system is only partially dependent on materials and labor costs per unit; it is also highly dependent on the manufacturing yield of the end product. Therefore, design and production engineering must consider the choice of package jointly in order to guarantee that the chosen package conforms to existing (or purchasable) manufacturing equipment and that the manufacturing process can meet yield goals.

2.2 Speed Requirements

The speed requirements of a system strongly affect package choice. If the interconnect lengths in the system (both inter- and intra-board) can be reduced, system speed may be increased. Reducing interconnect lengths may involve reducing the required number of packages, choosing packages with smaller outlines, changing to double-sided, modular, or piggy-backed mounting, using small form factors, reorganizing boards, and even changing the number of metal routing layers of the board. See Figure 8B-3.

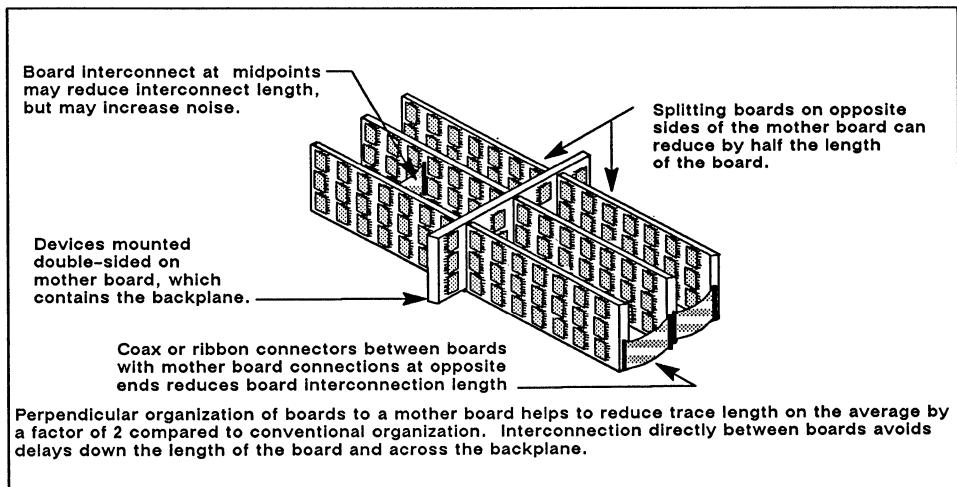


Figure 8B-3. Minimizing Interconnect Length

2.2.1 The Effect of Noise on Speed

There are various sources of noise that can affect an IC, each with its own effect; all forms of noise influence signal speed, quality, and consequently, system reliability. Certain types of noise arise between a chip I/O and ground or power, while other forms of noise are coupled to the power rails and influence system power and ground lines, propagating the noise throughout the entire system. Noise appears to an input buffer (receiver) relative to the receiver's ground. Any noise on this referenced signal is superimposed onto the incoming signal itself, as shown in Figure 8B-4. The V_{IH} or input threshold level of the receiver indicates when the input will switch, if the signal is stable at that level. Therefore, although the input voltage ordinarily would switch 4 ns after the driver switches, when the signal first crosses the threshold, the designer must assume it will not switch until it is stable; in this case at 8 ns, producing a loss of 4 ns due to noise.

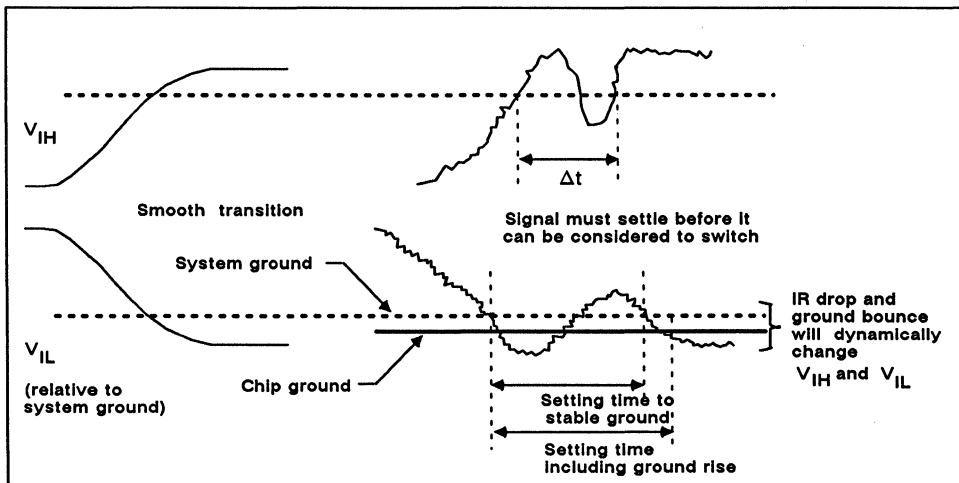


Figure 8B-4. Impact of Noise on Speed

2.2.2 Controlling Noise through Package Selection

Each form of noise is dependent not only on current or its first derivative with respect to time, but also on the real and imaginary components of impedance: resistance (R), inductance (L), and capacitance (C). One solution to noise can be to minimize the package L and R and to locate high drive pins where they will minimize L and R .

2.2.3 The Effect of Thermal Characteristics on Speed

The speed performance of a CMOS or BiCMOS circuit degrades with temperature rise. Therefore, in very high speed systems, it is sometimes necessary to reduce the junction temperature (T_j) or die temperature as a way to improve speed. Certain packages offer better cooling properties than others, making them more suitable for high speed systems. Thermal issues are discussed in Section 5.0.

2.3 Quality and Reliability Requirements

Reliability refers to the defects or failures that appear during the lifetime of a device. Quality, on the other hand, refers to the frequency of occurrence of defects or faults in a device as a result

of the manufacturing process. Quality defects are revealed by testing immediately after manufacturing, while reliability defects are revealed by special long-term or intensive test sequences or by time.

2.3.1 How Package Type Affects Quality Testing

Conventional (through-hole) packages lend themselves to simplified testing because it is easy to access the leads in order to force a state (1 or 0) at a node and/or to observe the state of the node. These tests are performed with board-level in-circuit or functional testers. Such tests facilitate the manufacture of high-quality systems by ensuring proper connectivity and function.

Surface mount devices, however, generally provide poor probe access, and are known to occasionally possess faulty joints that make temporary connections during probe. Through-hole packages also have occasional bad solder joints, although their node access is fairly good.

2.3.2 How Device Integration Affects Reliability

Total system reliability is related to the reliability of the individual devices and to their configurations. Systems may be configured as a series in which all devices are interdependent, in which case any one failure will cause overall system failure, or they may be configured in parallel, in which case all devices must fail for the system to fail. Parallel configuration is used in redundant or fault-tolerant systems.

The reliability of a system also depends on the reliability of the devices that comprise the system. The long-term reliability of a single device is defined as an inverse natural log function in a variable lambda, which is the failure rate of the device in the region of lifetime operation characterized by a constant failure rate. In the first hours of a device's life (the infant mortality period), the failure rate declines. The majority of a device's life is characterized by random failures (expressed as lambda), and the end of a device's life exhibits an increasing failure rate. Today's ICs, however, are designed so that wearout does not even begin to occur for at least several hundred years, and can be considered never to occur. To understand how the partitioning of a system into circuits can affect the reliability of a system, consider a system in which N components are configured in series. Although the density of ASIC devices has increased by two orders of magnitude in the last decade, the reliability of the devices has remained roughly constant. Therefore, it can be assumed that the failure rate of each of the components is constant. The reliability of systems and subsystems in which components are series-dependent is the product of the individual reliability terms for each component. The reliability function of the system just described is therefore:

$$R(t)_{sys} = R(t)_1 * R(t)_2 * \dots R(t)_N$$

where $R(t)_N = e^{-Nlt}$, t is the independent variable time, and l is lambda, the failure rate.

Since all components have the same failure rate, the reliability function of the system is:

$$R(t)_{sys} = e^{-Nlt}$$

Because the number of packages affects the reliability more than the integration factor does, a designer's goal in constructing a reliable system should be to maximize integration and thereby reduce part count.

The disadvantage is that increased integration may in turn increase the package pin count, requiring a more complex package, which usually costs more than a simpler, smaller package. Additionally, the larger die sizes cost slightly more per gate than the smaller ones, although the total NRE (non-recurring engineering charges) would typically be lower.

2.3.3 How Noise Affects Reliability

Even when Schmitt trigger input buffers are used to receive clock signals, noise may go beyond the hysteresis value of the input buffer and cause a counter to be incorrectly clocked or other circuit malfunction. Noise is in this sense a threat to reliability as well to speed and must be considered in the choice of package as well.

2.3.4 How Thermal Issues Affect Reliability

While the junction temperature of a device affects its speed, it also affects reliability expressed as MTBF (mean time between failures) or the mean time a device will operate in a given environment before failure occurs. Figure 7-4 in the previous chapter, Quality and Reliability, illustrates this concept by plotting life test failures as a function of junction temperature. System reliability goals, then, restrict the desired maximum junction temperature in a manner that affects the choice of package according to its thermal characteristics, the chosen type of system thermal management (cooling), and the maximum allowable device power dissipation.

2.3.5 How Package Material Affects Reliability

The different materials used in package construction each have distinct thermal and mechanical properties. The most common materials and their characteristics are listed in the table in Figure 8B-5 below.

Package Type	Body Material	TCE (ppm/ °C)	Thermal Conductivity (W/m * °C)	Dielectric Constant (K)
Ceramic	Al ₂ O ₃ (Alumina)	7.0	20	10
Plastic PGAs	Epoxy Fiberglass	14 – 18	0.16	4.5 – 5.0
Other plastic packages (DIP, PLCC, Flatpack)	Polyimide Epoxy	15 – 18	0.38	4.5 – 5.0

Figure 8B-5. Package and Material Characteristics

To better understand the different characteristics of plastic and ceramic packages, it is helpful to know something about the way they are constructed. Packages provide electrical connection from the IC to the system and isolate the device from destructive elements of the environment. The choice of materials and construction of a package affect its final dimensions, thermal characteristics, and electrical characteristics, as well as device reliability. Fujitsu carefully determines the most appropriate manufacturing methods for a given package and then performs extensive qualification tests to determine its success.

The largest part of the package is the body, which houses the die. The die may be affixed to a lead frame, which physically supports the die and provides the leads that electrically connect the die to the system by means of bonding wires or tab leads. Alternatively, the die may be supported by a cavity on the body of the package or attached to the bottom of the body by a chip carrier.

The die is attached to the surface of the lead frame or to the metallized surface of the cavity or carrier with gold or silver paste, or eutectic. After the die is attached to the lead frame, cavity, or carrier and the bonding pads are bonded to the leads, the assembly is encapsulated. In plastic packages, an epoxy resin is molded around the assembly. In ceramic packages, a cap is sealed

onto the lower part of the body or carrier using a frit glass or metal seal (the metal seal has a higher melting temperature than the glass). A solder seal can be used if the cap is metal.

To ensure that the device is completely isolated from its environment, the surface of the die is then coated with glass (SiO_2) and then polyimide or other coating that prevents gas and moisture from coming in contact with the surface of the die. Figure 8B-6 shows a frontal cross section of the structure of a PLCC package; Figure 8B-7 provides a top view.

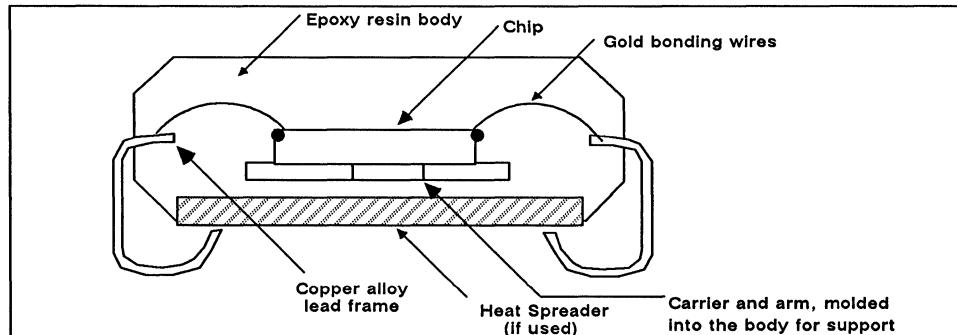


Figure 8B-6. PLCC Package Construction (Front View)

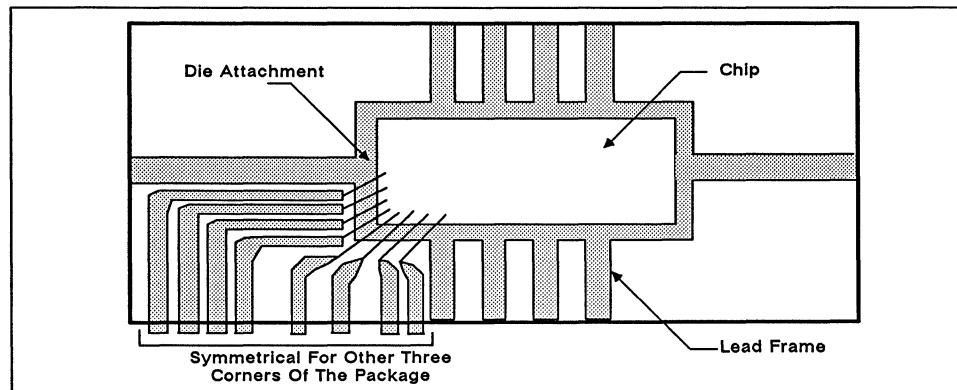


Figure 8B-7. PLCC Lead Frame Construction (Top View)

Each of the various packaging methods has its advantages and disadvantages; for instance each body type and each type of seal has a different maximum case temperature. While plastic packages can tolerate temperatures up to 125°C and high humidity levels with outstanding reliability, ceramic packages are the most reliable for harsh extremes of cold.

Each package type also responds differently to the thermal environment of the board to which the device is attached. Heat can cause thermal stress on the device when different materials expand at different rates, a particularly important factor when surface mount packages are involved.

Different packages also exhibit different electrical characteristics. As the speed and gate densities of CMOS devices rise, the avoidance of electrical parasitics in the form of package delays and noise become increasingly important factors in choosing a package type.

Fujitsu's plastic PGA provides a good example of the tradeoffs involved in package construction. In 1986, Fujitsu introduced the plastic version of its ceramic PGA. The plastic configuration proved to have several advantages over the ceramic version. The body is formed from glass epoxy (VG-10) with an aluminum cap and an epoxy resin sealer. This combination of materials has the same rate of expansion as the PC boards onto which it is mounted; it is also less expensive than ceramic.

Ceramic PGAs have a hermetic seal of solder between the metal lid and the cavity, but plastic PGAs are sealed by filling the cavity with epoxy resin to form an inner seal, then placing a resin sheet over the inner seal to form an outer seal, and then securing an aluminum cap over the outer seal. The aluminum cap provides the necessary rigidity to support the fragile glass epoxy, as well as improving the thermal conductivity of the package.

Connections from the bonding wires to the pins are provided by copper traces designed to minimize mutual and self inductance. Because the plastic PGA is a large package, however, and generally houses a large die, the thermal coefficient of expansion (TCE) difference between the die and the cavity can exert stress on the bonding wires and the die attach. Figure 8B-8 lists the package types discussed in this section and the materials used to construct each type.

Package Type	Lead frame/Metallization	Lead/Pad	Lead Finish	Cap Material	Body Material	Seal Material
Plastic DIP	Fe-Ni or Cu Alloy Lead frame	Same	Solder Dipped	—	Resin	Resin
Ceramic DIP	Tungsten Metallization	Kovar or Fe-Ni	Au/Sn Plated	Metal or Aluminum	Laminated Alumina	Solder, Glass Frit
CERDIP	Fe-Ni Alloy Lead frame	Fe-Ni	Sn Plated	Alumina	Alumina	Glass Frit
Plastic Flatpack	Fe-Ni Alloy Lead frame	Same	Sn Plated	—	Resin	Resin
Ceramic Flatpack	Fe-Ni or Kovar Lead frame	Same	Au Plated	Metal or Aluminum	Laminated Alumina	Solder or Glass Frit
Cerpack	Fe-Ni Alloy Lead frame	Same	Sn Plated & Solder Dipped	Alumina	Alumina	Glass Frit
Plastic PGA	Cu Conductor on Epoxy glass	Kovar	Ni Plated & Solder Dipped	Aluminum	Epoxy Glass	Resin
Ceramic PGA	Tungsten Metallization	Kovar	Au Plated & Solder Dipped	Metal or Alumina	Laminated Alumina	Glass Frit
Plastic LCC	Cu Alloy Lead frame	Same	Solder Plated	—	Resin	Resin
Ceramic LCC	Tungsten Metal. Pad	Tungsten Metal. Pad	Au Plated	Metal or Alumina	Laminated Alumina	Solder, Glass Frit

NOTES: All above packages are hermetic. Alumina is a ceramic. Solder is PbSn. Fe-Ni is ferrous (iron) nickel. Kovar is an alloy. Bonding wires are gold in the case of molded packages (epoxy resin PLCCs, DIPs, Flatpacks) and gold or aluminum for the other cases. Cerpack is the ceramic flatpack equivalent of CERDIP.

Figure 8B-8. Fujitsu Package Types

2.3.6 Package Qualification to Ensure Reliability

Fujitsu performs extensive six-month minimum qualification tests for every package-die combination. After such qualification is performed, the package die-combination is added to a package

matrix that is supplied in the Design Manual for the appropriate technology. The designer can be assured that Fujitsu has considered the issues presented here, as well as others, when releasing an approved package-die combination.

3.0 Package Types

VLSI ASICs are supported by a wide variety of packages, of both surface mount and through-hole types. Through-hole devices, including dual in-line packages (DIPs), and pin grid arrays (PGAs), are a proven technology and are supported by widely available production equipment. The pins of these devices are inserted through holes in the PC board to form electrical contact with traces (usually copper) which are embedded in the board or applied to the surface and are routed to drilled pin holes. Solder applied by reflow or wave technique then completes the connection.

3.1 Through-hole Packages

3.1.1 Dual In-line Package (DIPs)

DIPs have two rows of pins spaced 300 mils to 900 mils apart, with a pin spacing of 70 to 100 mils. Since the length of the package increases as each pair of pins is added, the size of a DIP tends to be unmanageable over 64 pins. The lead width and length of a DIP varies widely, causing variation in the input and output response of the device and thus, skew. Also, due to their high pin inductance, DIPs tend to be noisy, the degree of noise being a function of the location of outputs and sensitive inputs.

The DIP is relatively simple for manufacturing to support, thanks to a large installed base of well-proven equipment and is one of the least expensive packages available. Furthermore, DIPs, being well established, come in many JEDEC-approved options (see JEDEC Standard 95), and are available in both ceramic and plastic cases.

3.1.2 Pin Grid Arrays (PGAs)

Although PGAs are usually through-hole (Fujitsu also offers SMD versions), they differ from DIPs in that pins are arranged in rows on all four sides. While the pin spacing is usually the same as for DIPs (70 to 100 mils), nesting the pins in rows permits a larger number of pins to be contained within a smaller area allowing PGAs to support high pin counts of more than 300 pins. See Figure 8B-9 for a list of Fujitsu PGAs.

Package	Type	Construction	Number of Pins
PGA - 64C, 64P	Through-hole	Ceramic/Plastic	64
PGA - 88C, 88P	Through-hole	Ceramic/Plastic	88
PGA - 135C, 135P	Through-hole	Ceramic/Plastic	135
PGA - 179C, 179P	Through-hole	Ceramic/Plastic	179
PGA - 208C	Through-hole	Ceramic	208
PGA - 256C	Through-hole	Ceramic	256
PGA - 256C	Surface	Ceramic	256
PGA - 299C	Through-hole	Ceramic	299
PGA - 321C	Staggered	Ceramic	321
PGA - 361C	Staggered	Ceramic	361
PGA - 401C	Staggered	Ceramic	401
Through-hole = 100 mil through-hole Surface = 50 mil surface mount PGA Staggered = 71 mil staggered PGA			

Figure 8B-9. PGAs Available from Fujitsu for CMOS

Although PGAs are generally easy to support from a manufacturing standpoint, they may also raise problems. The PC board designer may find it difficult to route signals to and from the inner rows of the PGA, since it has only 100 mils spacing between pins. Additionally, the large cluster of pins confined to a small area tends to create trace congestion and may require boards of up to six layers to be used to support the PGAs. Manufacturing engineers find the solder joints for the pins of inner rows are difficult to inspect, forcing them to rely on the results of "bed-of-nails" in-circuit testers, or sophisticated inspection techniques such as x-ray or infrared.

Although more expensive than DIPs, PGAs have come down in cost with the introduction of plastic PGAs (previous PGAs were usually ceramic). These plastic PGAs are generally constructed of G-10 glass-type epoxy with the traces routed through the epoxy the way they are routed on a typical PC board. (The electrical characteristics are, or course, tightly controlled). Although the reliability of plastic PGAs was initially in question, Fujitsu built them using special construction techniques employing metal lids and heat spreaders to provide rigidity and heat dissipation. Their excellent reliability history up to this point seem to indicate that plastic PGAs will continue to be popular. The widely-used epoxy thick-film substrate, once a quality and reliability concern, has the same thermal coefficient of expansion (TCE) as the most common PC boards, and reduces the stress of expansion and contraction that is typically a concern with larger packages. (The distance of expansion per unit change in temperature increases with the size of the package).

3.1.3 Advances in Through-hole Packaging at Fujitsu

The demand for high pin-count plastic packages cannot be satisfied by merely increasing the number of pins a package supports. As size increases, so do the problems inherent in these lower-cost packages. These problems include greater lead inductance and thermal expansion mismatch between die and package. Ceramic flatpacks can support more pins than plastic packages, but they require special manufacturing capabilities, and are difficult to work with since they may have pin pitches down to 10 mils. Surface mount PGAs (discussed in Section 3.2) can support a large number of pins, but require difficult manufacturing processes.

Fujitsu's answer to these problems, for the customer who wants high levels of integration without the need for exotic manufacturing methods, is the staggered PGA, shown in Figure 8B-10.

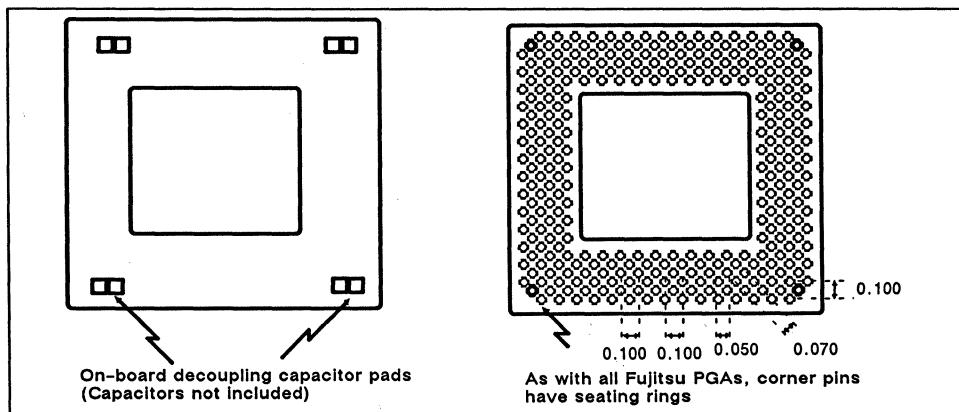


Figure 8B-10. 321-Pin Ceramic Pin Grid Array

Figure 8B-11 illustrates the footprint of the staggered PGA and the method for routing traces through the leads. Note that the routing is oblique, with the traces offset 45 degrees compared to traditional routing. At this angle, the lead spacing is 71 mils, providing the trace density available with standard through-hole devices, while reducing the package outline by approximately 40%.

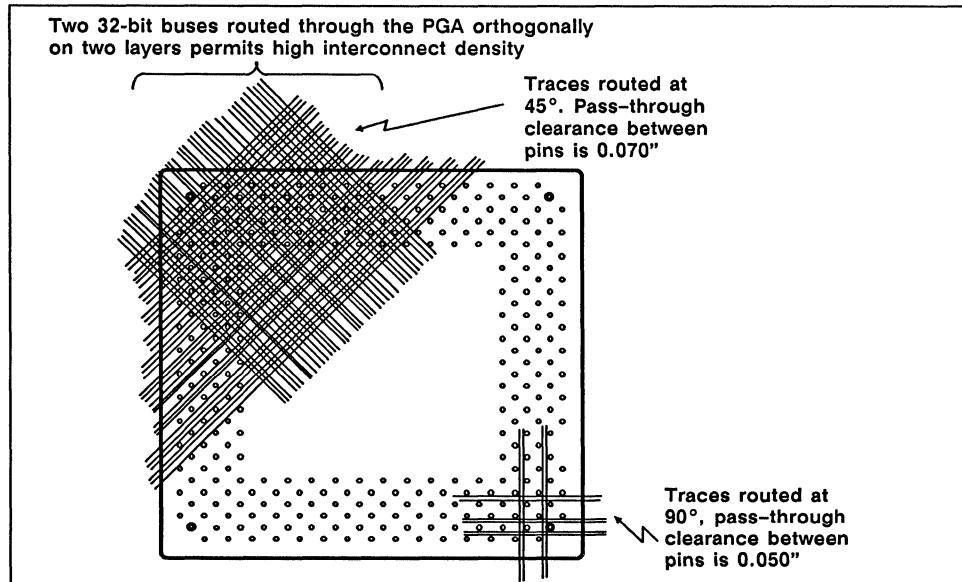


Figure 8B-11. Staggered Pin Grid Array Routing

The lead configuration of a package affects the pin assignment of the ASIC device. For example, Figure 8B-12 shows a situation in which a 32-bit address bus and a 32-bit data bus are routed through the device, with one offset 90 degrees from the other. If you assign consecutive bit significance to the bus, you will notice that the resulting pinout is quite different from an equivalent circuit packaged in a traditional orthogonal PGA. High drive buses can still be distributed around the ground pins, but the associated pads are not concentrated in one specific area of the die, reducing the concentration of simultaneously switching outputs, thereby reducing signal noise.

3.2 Surface Mount Devices (SMDs)

The demands of military applications, space-constrained systems and boards containing large numbers of memory devices were initially responsible for the development of surface mount technology (SMT). However, the accelerated push for physically reduced systems, the appearance of higher pin count ASICs, and the cost of pin grid arrays have forced many more designers to consider surface mount options. Easing the strain of the migration to SMT is the broader availability of pick and place, vapor phase soldering, and other necessary SMT equipment, as well as the availability of SMDs for an increasing percentage of devices on the boards. SMT for VLSI is gaining momentum due to the smaller board area consumption, smaller profile, and proven reliability.

3.2.1 Flatpacks

Plastic flatpacks have been popular for years with manufacturers of peripherals in which the board area is constrained and height is restricted. And recently, the low cost of flatpacks (in plastic) has

made them an attractive alternate to PGAs and even to DIPs in cases of higher pin count. As the following figures show, flatpacks come in several lead type and location configurations. Figure 8B-12a illustrates a SOIC (small outline integrated circuit), with gullwing leads on two sides, Figure 8B-12b illustrates a quad flatpack (QFPT) with gullwing leads on four sides. Flatpacks with axial leads require special assembly, and are generally used only for ECL circuits in which leads may have to be trimmed and formed to tune impedance.

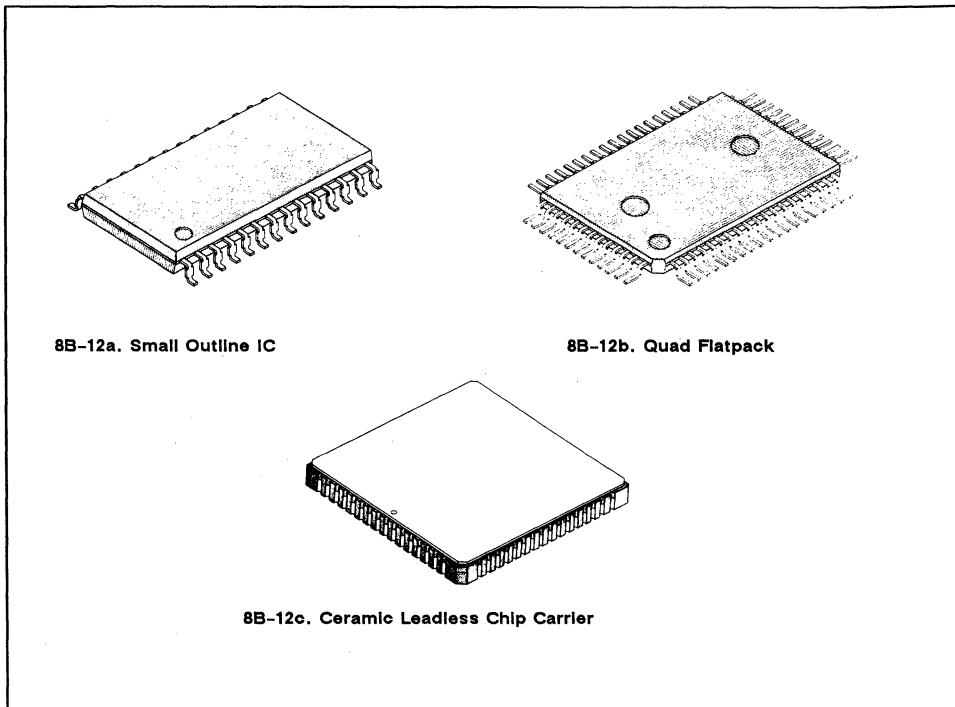


Figure 8B-12. Flatpack Configurations

Because flatpacks feature pin pitches (pin spacing from center to center) down to 10 mils, they can support high pin counts within a small board area. However, the narrow pin spacing means that accuracy in device placement, pad size and placement, and solder paste application tolerance are all more critical. PCB designers also need to determine whether the true package dimensions are in metric or English dimensions, and, when converting between the systems of measure, ensure that enough precision is maintained so that pins on the end of large packages won't roll off due to inaccuracies in pad location.

Probing devices with fine pin pitches can be difficult because the pins do not pierce the bottom of the board, and if probes are attached to the leads, they can easily slip off and short adjacent leads.

3.2.2 Leadless Chip Carriers (LCCs)

Ceramic leadless chip carriers (CLCCs), such as the example shown in Figure 8B-12c, have a long history in surface mount packaging. Ceramic packages perform well in high temperature environments, explaining their popularity in military applications. The term "chip carrier" comes from the process of mounting the die directly to a thick-film chip carrier, which also has pads for external connection on the opposite side of the substrate. This configuration differs from that of the PGA, in which the die is housed in the cavity of the package, or the flatpack, in which the die is held by the lead frame and molded with the package. CLCCs are available in pad counts ranging from 28 to 84 and beyond.

Pads, not leads, are located on the bottom of the carrier and are generally spaced at a 40-mil pitch (standard). Solder paste is applied to the pads on the board to which the device will be mounted, usually by screen printing, and the board is then vapor phase or infrared reflow soldered. Because the pads are located beneath the package, they are typically very difficult to probe and are subject to manufacturing defects such as solder voiding (gas bubbles in solder formed during reflow).

The most challenging problem inherent to LCC devices relates to thermal coefficient of expansion (TCE) mismatch between the chip carrier and the board to which it is mounted. As the temperature of boards and packages rises, the materials expand at different rates. This difference translates to mechanical shear force at the solder joint. This force temporarily deforms the leads of PLCCs and flatpacks, but CLCCs have no leads. Consequently, the force is directed at the solder joint, tending to promote thermal fractures, (shown in Figure 8B-13).

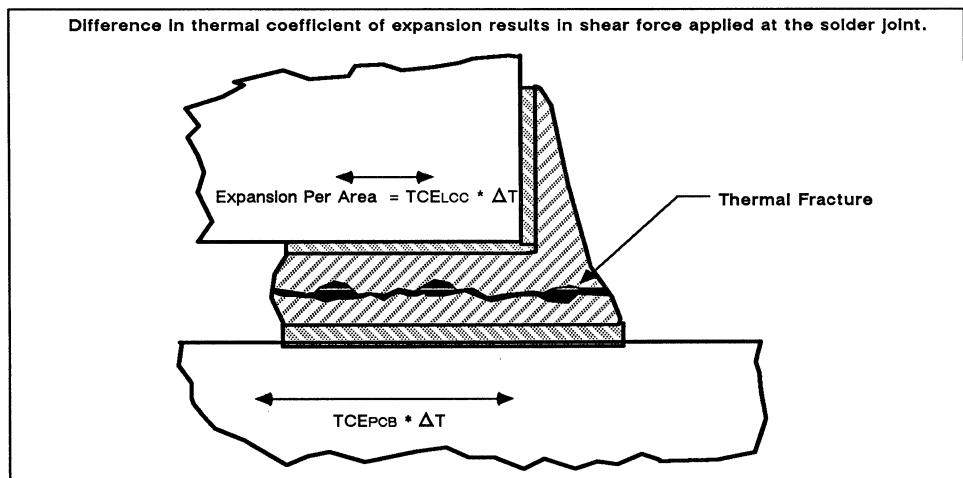


Figure 8B-13. Defect Caused by Difference in Thermal Coefficient of Expansion

Even though CLCC SMDs cost more than equivalent plastic packages, their resistance to high temperatures, availability in hermetically sealed (moisture resistant) packages, and low profile of the CLCC SMDs make them very useful for applications in extreme environments. The TCE mismatch problem affecting LCCs is less severe when they are mounted to ceramic hybrids or PC boards, making their disadvantages acceptable in many circumstances.

3.2.3 Leaded Chip Carriers (PLCCs)

If cost and TCE mismatch are a significant deterrent to the use of LCCs, leaded chip carriers may be more attractive. Though the chip is still mounted on a carrier (see Figure 8B-15), the electrical connections of PLCCs are through pins that deform to absorb the TCE-induced thermal stress. Furthermore, while solvents used in the post-soldering cleaning process may be retained beneath the low profile of the CLCC and flatpack, the board offset of the PLCC permits it to remain free of these contaminants. In addition, the LCC in a plastic package costs less than the equivalent CLCC. This package is termed an SOJ (small outline J-lead) when its bent leads are located on only two sides (Figure 8B-14). The leads are bent into the form of a J in order to permit it to be placed on top of the solder pad.

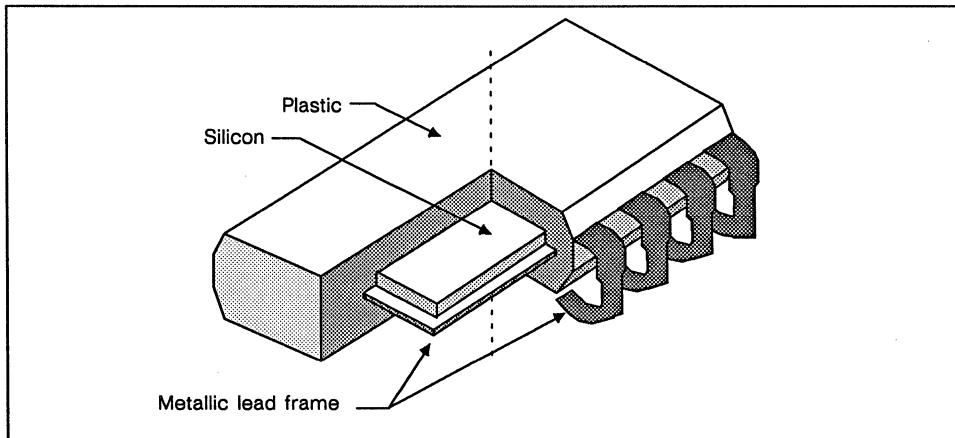


Figure 8B-14. Cross-Section of a Plastic Small-Outline Package

When more pins are necessary (in the 44-, 68-, 84-pin packages necessary for ASICs), the LCC is called a PLCC (shown in Figure 8B-15). It is also available in a ceramic body version; both are available in pin counts of 28 to 84 and beyond.

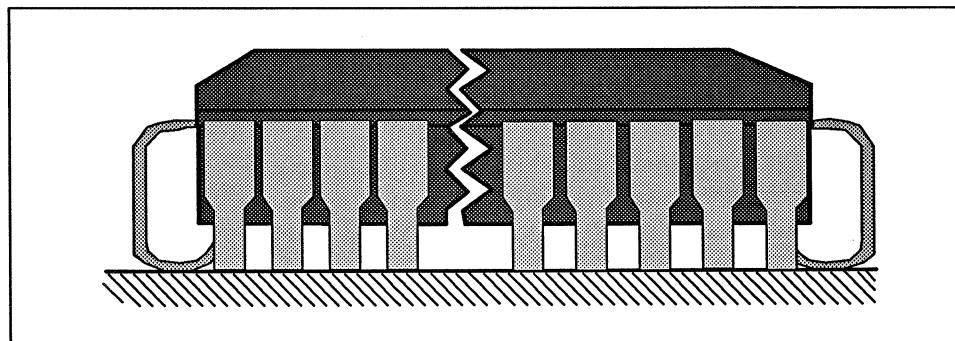


Figure 8B-15. PLCC Package

On the list of drawbacks of the PLCC is its limited ability to withstand high case temperatures, and its unavailability as a hermetic package. It is nevertheless very well suited for industrial and commercial environments. With a 50-mil pin pitch and only slightly greater height and width, the profile of the PLCC is nearly equivalent to the corresponding CLCC.

3.2.4 Advances in Surface Mounted Packages

While smaller process geometries themselves have few disadvantages, the associated increase in integration, speed, power, and particularly pin count place heavy burdens on packaging. The greatest challenges CMOS faces is supporting pin counts in excess of 300 in packages with low lead inductance, capacitance, and resistance.

To respond to these demands, Fujitsu has developed a clever solution in packaging to obtain the highest average pin density per board area yet achieved. This is accomplished with surface mount PGAs, which rely on narrow pin pitch (50 and even 25 mils) in a dense grid of multiple rows of pins. Since through-hole packages cannot effectively support pin pitches narrower than 70 mils, these PGAs must be surface mounted, though they still possess pins (see Figure 8B-16).

Surface mount PGAs offer the greatest pin density and lowest inductance

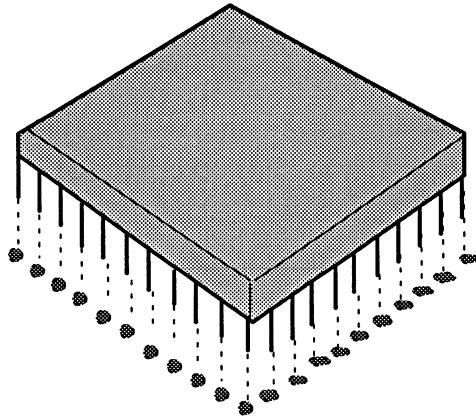


Figure 8B-16. Surface Mount PGA

The surface mount technology also permits traces to run beneath the package leads, increasing available trace density. Figure 8B-17 shows the solder pad design required by these high-pin-density packages.

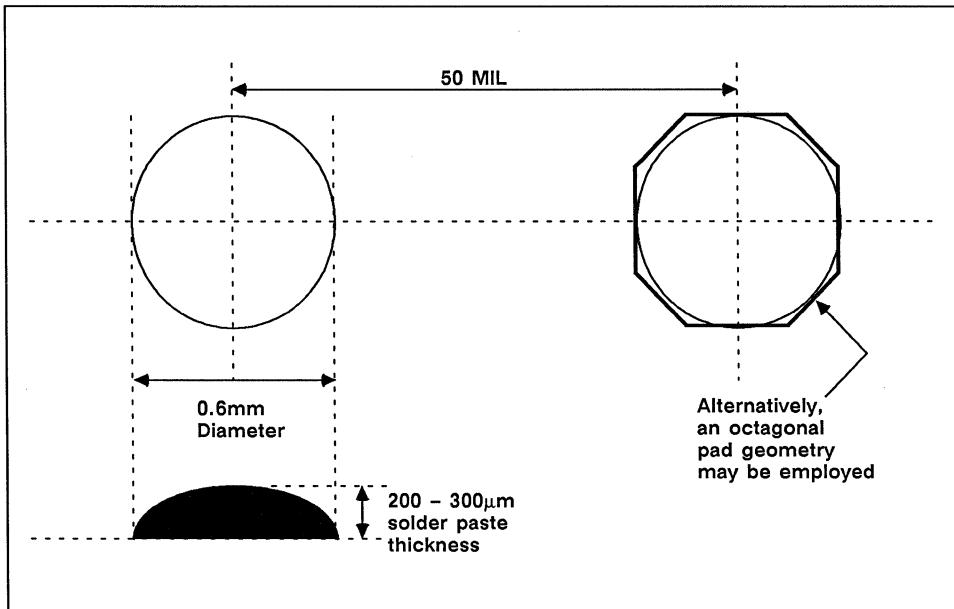


Figure 8B-17. Solder Pad Design for Surface Mount Pin Grid Arrays

The table in Figure 8B-18 provides an item-for-item comparison between PGAs, surface mount PGAs, and flatpacks of similar pin counts.

PACKAGE	TYPE	PIN PITCH	OUTLINE (MAX)	PIN DENSITY (Pins Per Sq. Inch)
FPT - 160	Surface	25 mil	1.276" x 1.276" (1.63 sq in)	98
PGA - 256	Through	100 mil	2" x 2" (4 sq in)	64
PGA - 256	Surface	50 mil	1" x 1" (1 sq in)	256
PGA - 321	Staggered	71 mil	1.72" x 1.72" (2.96 sq in)	109
PGA - 401	Staggered	71 mil	1.922" x 1.922" (3.69 sq in)	109

Figure 8B-18. Comparison of Critical Features

The numerous electrical and mechanical advantages of surface-mount PGAs would seem to outweigh their disadvantages. However, the general state of high volume manufacturing has not kept pace with the rapid advances in semiconductor packaging. This is partly due to the requirement for state-of-the-art manufacturing equipment, which is quite expensive, and also to the need to maintain board yields with such complex devices. Therefore, in order to establish these packages as an attractive alternative, Fujitsu has instituted a program with which to assist customers in the mounting and inspecting of these highly complex packages.

3.3 A Comparison of Through-hole and Surface Mount Devices

SMDs provide improved electrical performance and reduced system size and costs. Furthermore, with plastic flatpacks of up to 160 pins and beyond available, SMDs show promise in supporting the rapidly advancing gate size complexities and high pin count of today's ASIC products at a substantially lower cost than the large ceramic PGAs. However, as the manufacturing complexities that have just been reviewed indicate, surface mounting large ASIC devices may be difficult and risky, and the designer should be cautious in their use.

If board space constraints are not critical, if the economic impact of scaling down the end system is not great, if optimal electrical characteristics in packaging are not a critical concern, then through-hole packaging may be the best solution. On the other hand, if speed and integration requirements dictate the use of very dense gate arrays, PGAs or SMT PGAs provide both through-hole and surface mount alternatives.

3.3.1 Socketing Surface Mount Devices

Some benefits of SMDs are available to manufacturers employing through-hole packages through the use of sockets for SMDs. Sockets are available for QFPs, SOPs (small outline packages), CLCCs and PLCCs; however, the use of QFP and SOP sockets is normally restricted to prototyping and burn-in, while low-cost, reliable production sockets are more commonly available for PLCCs and CLCCs. These production sockets house the SMD (they are tightly tailored to the specific package) in one of two ways. Flatpacks and LCCs use low/zero insertion force with a lid that closes down on the package. PLCCs use pressure socket contacts that drive a pin into the underside of the socket. Socket pins are arranged like those of PGAs: they are through-hole, they have 100-mil spacing (generally), and they are most commonly oriented in a grid of two rows.

One advantage of these sockets is that in applications where through-hole packaging is required and the choice of through-hole packages is limited to PGAs, a plastic SM package plus the production socket will cost less than the through-hole PGA. The scenario typically occurs when the required number of pins is between 40 and 84 for PLCCs and LCCs and up to 160 or more for the flatpacks.

Another significant reason to socket SMDs results from the manufacturing difficulties of SMDs that were presented earlier. ASIC devices are usually among the largest in the system, and the most vital and expensive. For the purpose of field maintenance, many companies feel it is more economical and reliable not to risk running an ASIC device through wave or reflow solder and risking stress fractures or other damage. Furthermore, the test probing difficulties alluded to earlier are alleviated with sockets, which usually provide easy access to the contacts. Often, once reliability of the system is proven, the boards are re-laid out with surface mount devices. Therefore, simply because a manufacturing facility isn't geared up for SMT does not mean that SMT devices cannot be used there.

3.3.2 Noise Problems With Sockets

Sockets for SMDs are convenient for manufacturers not yet ready to go to SMT, or for initial prototyping where the device may frequently be removed. Socketing permits the user to gain many of the benefits of SMDs, such as reduced profile and support of high pin counts in plastic, while avoiding the drawbacks, such as special manufacturing equipment and lead probing difficulties. Unfortunately a major electrical advantage of SMDs, low pin inductance, is compromised when sockets are used. The primary result is greatly increased noise, which, adversely affects overall speed and signal quality. In fact, a socketed SMD generally has a higher lead inductance than an equivalent through-hole PGA.

3.4 Summary of the Packaging Alternatives

Having reviewed the package selection alternatives presented in Section 2.0 and the various trade-offs between the packages discussed in this section and summarized in the table in Figure 8B-19 below, the designer can weigh the benefits and limitations of the various packages and arrive at an optimal packaging scheme.

Package Type	Range of Physical Dimensions	Electrical Characteristics ¹	Thermal Characteristics (°C/Watt)	Gate Complexity ²	Relative Cost (per Pin)
Through-Hole DIP	# PINS: 16 to 64 Pin Pitch: .100 mils Body Length: .75" to 2.3" Body Width: .300" to .700"	R: Medium L: High C: Low	Ceramic/Plastic θJA ³ : 70 - 40/ 120 - 80	Up to 17K gates	1
Surface Mount SOIC	# PINS: 16 to 28 Pin Pitch: .10 mils Body Length: 50 to 70 mils Outline Width: .300" to .400"	R: Medium L: Medium C: Low	Ceramic/Plastic θJA: 110 - 80/ 130 - 105	Up to 6500 gates	1
Surface Mount QFPT	# PINS: 48 to 260 Pin Pitch: .10 mils Body Width: .65" to 1.7"	R: Medium L: Medium C: Low	Plastic θJA: 95 - 60	Up to 17K gates	1
Surface Mount CLCC	# PINS: 28 to 84 Pin Pitch: .40 to .50 mils Body Width: .45" to .97"	R: Medium L: Medium C: Medium	Ceramic θJA: 70 - 45	Up to 25K gates	5
Surface Mount PLCC	# PINS: 28 to 84 Pin Pitch: .50 mils Body Width: .49" to 1.19"	R: Medium L: Medium C: Low	Plastic θJA ² : 65 - 50	Up to 17K gates	1.05
Through-Hole PGA	# PINS: 64 to 299 Pin Pitch: .100 mils, .70 mils Body Width: 1.033" to 1.7"	Ceramic/Plastic R: Low L: Low C: High	Ceramic/Plastic θJA: 40 - 19/ 46 - 38	Up to 75K gates	Ceramic/Plastic 11/ 3.5-5

(1) Assuming 1.5 μ CMOS Technology
 (2) R = Resistance, L = Inductance, C = Capacitance
 (3) Utilizable gates

Figure 8B-19. ASIC CMOS Package Types and their Characteristics

4.0 Electrical Considerations for the Assignment of Signal, Power, and Ground Pins

Driven by the continual demand for high speed systems, CMOS ASICs are now being developed that exhibit output drive levels, rise and fall times, and propagation delays comparable to yesterday's ECL circuits. Consequently, the problems intrinsic to ECL design (even thermal management) are now appearing in CMOS designs. These problems, based on noise and its effect on the device, are introduced in this section and possible solutions are discussed.

4.1 Sources and Magnitude of Noise

CMOS circuits operate by charging and discharging node capacitances through pull-up or pull-down transistor networks constructed of P channel and N channel enhancement mode (normally off) MOSFET transistors. As a result, these circuits generate noise when switching. The following review of basic CMOS circuits and how they work explains this phenomenon in greater depth.

4.1.1 Basic CMOS Circuits

Figure 8B-20 shows a CMOS totem pole output buffer, the typical implementation for CMOS circuits, while Figure 8B-21 illustrates a CMOS-compatible input buffer, and Figure 8B-22 depicts a CMOS input buffer configured to be TTL compatible.

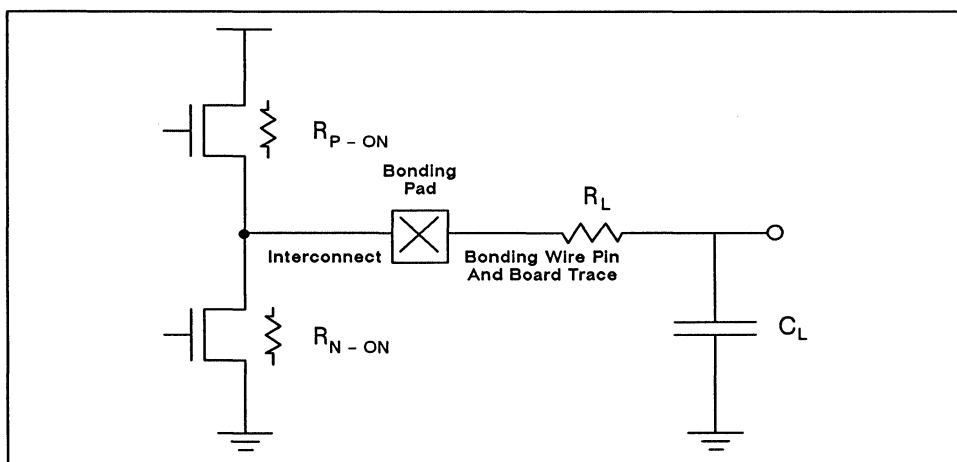


Figure 8B-20. CMOS Output Buffer Model (Totem Pole)

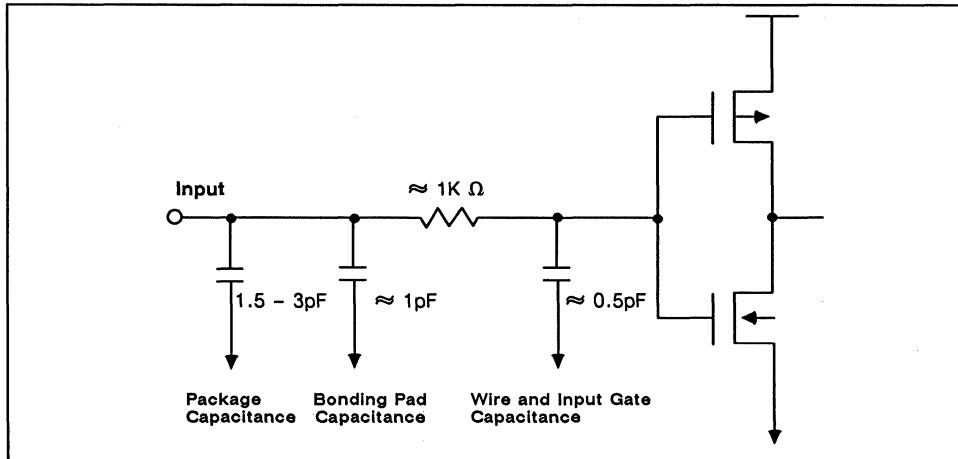


Figure 8B-21. I/O Model, CMOS Input

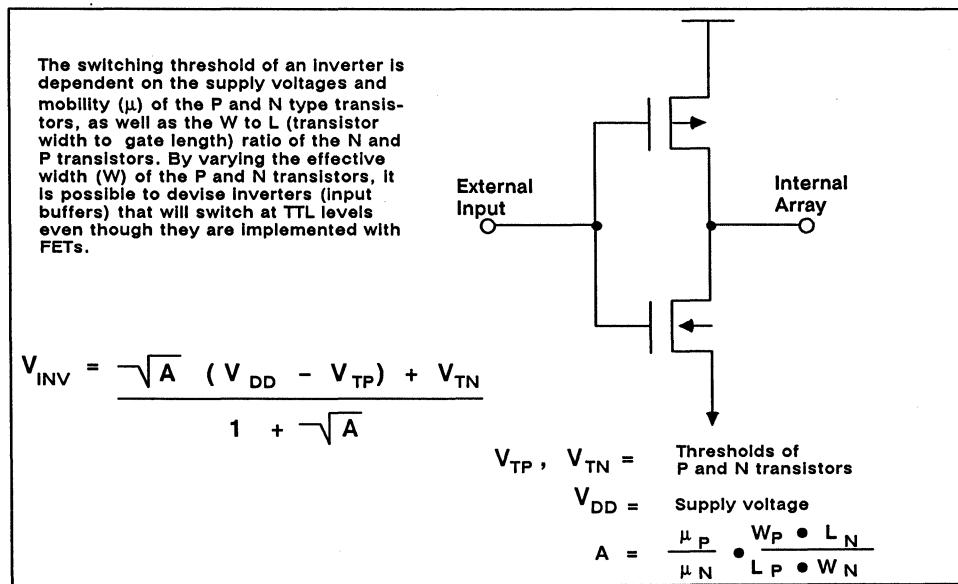


Figure 8B-22. I/O Model, TTL Input

Internal CMOS circuits, such as the NAND gate shown in Figure 8B-23 are typical of CMOS logic designs, which can be represented as a pull-up network and a pull-down network, each with its own logic and analog characteristics.

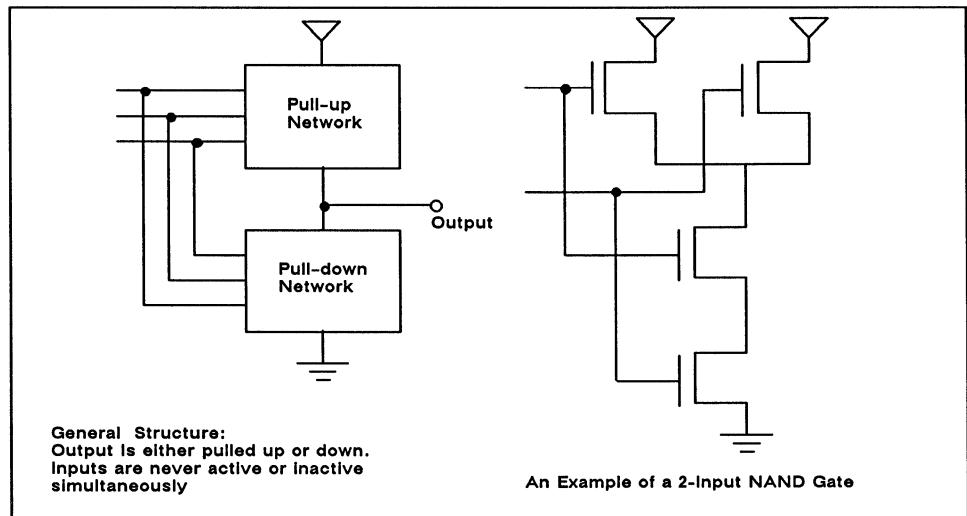


Figure 8B-23. CMOS Basic Gate Structure: The Pull-up/Pull-down Network

The other type of element used in CMOS circuits is the transmission gate, or T-gate, which is useful for the efficient construction of multiplexers and sequential circuits (D-flops, latches, etc.) as shown in Figure 8B-24.

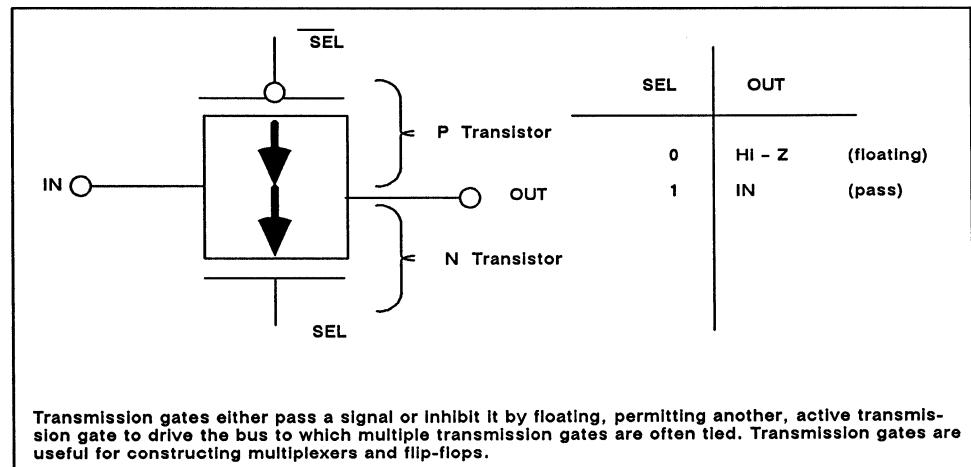


Figure 8B-24. CMOS Basic Gate Structure: The Transmission Gate

4.1.2 Output Switching Noise and Simultaneous Switching Outputs (SSOs)

The greatest source of noise in a CMOS circuit is the result of an output switching either high to low or low to high, particularly into or out of a high capacitive load. CMOS outputs drive two types of loads, either CMOS loads, which are high in capacitance (C) but low in leakage current, or TTL loads, which are lower in capacitance but higher in leakage current. Therefore, the AC and DC currents that the buffers see when they switch depend greatly on the type of driven load and its capacitance. When this load discharges through the N-type transistor of the totem pole output, as illustrated in Figure 8B-22, the effect is that of a capacitor discharging through resistance (R). Consequently, the initial current is high and decreases over time as the output node capacitance becomes charged. Similar currents may be observed when charging the node capacitance, as in the case of a low-to-high transition.

Figure 8B-25 shows the characteristic resistance and capacitance of various parts of the output of an ASIC device.

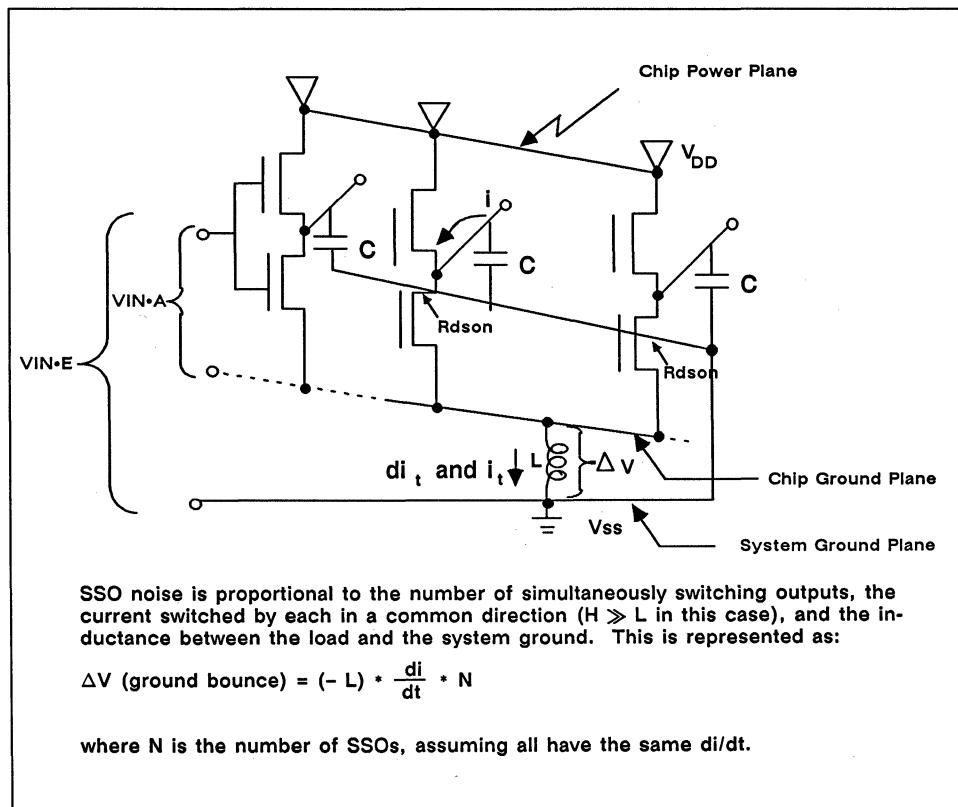


Figure 8B-25. Electrical Model of Simultaneously Switching Outputs

Although small, the total inductance becomes a critical factor when discharging or charging output capacitance, since the instantaneous current (i) is high. Recall that the self-induced voltage in an inductance, (L) is expressed by:

$$\Delta V_{INDUCED} = \frac{L * di}{dt}$$

where t is time and d is rate of change.

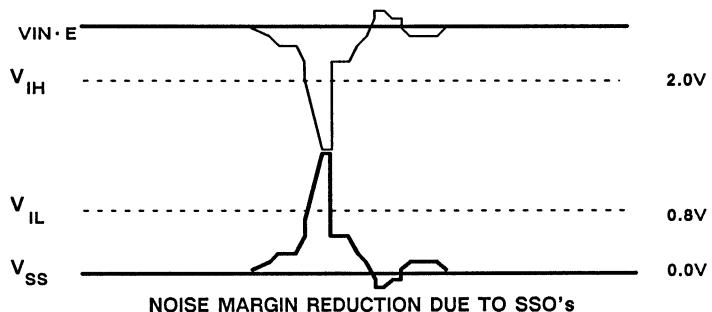
In a high-drive CMOS device driving high loads, such as 200pF, through a voltage swing approaching 5 volts with a rise/fall time of < 2ns, the instantaneous current may be:

$$i = C * \frac{dv}{dt} \approx C * \frac{\Delta V}{\Delta t} \quad (\text{average over rise and fall time})$$

This induced voltage appears as noise on the receiving end of the signal as referenced to the ground. The current on a high-to-low transition is sunk into ground, causing the current to "bounce" or rise relative to other signals referenced to it. This ground bounce phenomenon may also apply to power on low-to-high transitions, yielding a similar noise problem.

Noise on signals may cause false triggering on the input buffer(s) being driven, or at least create a window of ambiguity in the time at which the driven input should switch (see Figure 8B-26). Therefore, noise may result in degradation in speed resulting from adding settling time to a delay and may even result in functional effects if false triggering occurs. Furthermore, if N multiple outputs under this condition switch simultaneously, the induced voltage is increased as a multiple of the number of outputs:

$$\Delta V = N * L * \frac{di}{dt}$$



- In this example, outputs switching $H \gg L$ result in a ground bounce or rise in the chip ground relative to system ground.
- The rise appears as if the input signal voltage levels are reduced proportionally. If the bounce is too great, the input voltage is below V_{IH} causing false triggering.
- In the $L \gg H$ case, it is the low input levels (V_{IL}) that are affected.

Figure 8B-26. Effect of SSO Noise on Thresholds

Not only inductance but also characteristic resistance can create noise problems. The following paragraphs summarize the types of noise that exist in CMOS systems and explain how packaging impacts this noise.

4.1.3 Self-Induced Noise

Self-induced noise results when high-speed, high-drive outputs switch and introduce a spike on the signal relative to ground. The SSO effect, discussed above, is an example of the level of self-induced noise that can occur. It is predicted by:

$$\Delta V_{SI} = L \frac{\Delta i}{\Delta t}$$

where L is the inductance between the pin and ground as well as the trace inductance. Δi is the instantaneous current and Δt is the fall/rise time.

4.1.4 Mutually Induced Noise

A form of crosstalk, this noise occurs when a signal trace running parallel to another for some distance switches, inducing a voltage into the adjacent wire. Since both inductive and capacitive coupling occur only during signal transition and propagation, the effect is additive, as the signal propagates down the trace. Resultant noise propagates in both the forward and backward directions down the line. The forward crosstalk has a pulse duration equal to the rise and fall of the signal, with an amplitude equal to the difference between the capacitive and inductive coupling. Backward crosstalk has a pulse duration equal to the transition time down the trace and an amplitude dependent on the sum of the inductive and capacitive coupling as well as the trace length.

4.1.5 Capacitive Coupled Noise

Another form of crosstalk resulting from mutual signal coupling, this noise occurs in proportion to the dielectric constant of the board, the distance of trace separation, and the trace length and width. Acting as two thin parallel plates, these traces couple switching current as integrated over time.

4.1.6 Ringing on Signals

From basic circuit theory, the designer will recall that if the signal line impedance does not match the output impedance of the buffer, then the signal is not naturally damped. If the impedance of the load is less than that of the buffer, the signal is over-damped and will have a slow rise/fall time. However, if the buffer possesses lower impedance, then the signal is under-damped and may ring, as illustrated by Figure 8B-4 of Section 2. Typically, signal line impedances are in the range of 50 to 250 ohms, while in the past buffers possessed "on" resistances of 500 ohms to 2 Kohms. However, due to the need for higher current sourcing/sinking and faster switching speeds, "on" resistances of output buffers have come down to the 10- to 50-ohm range, requiring the use of special termination techniques, discussed in the Fujitsu Application Note "Interfacing CMOS and BiCMOS VLSIs."

4.1.7 iR Drop

Up to this point, the sources of noise discussed have depended on inductance or capacitance. The familiar voltage drop across a resistor as current passes through it is also a source of noise, since the DC current that a ground pin may sink, or that a power supply pin may source can be significant. This iR drop is the phenomenon that limits the sum of source and sink currents through power and ground pins respectively. Ohm's Law describes the effect of this noise source, as expressed in the equation below where:

R is the output pin-to-ground (sink) resistance or power pin return-loop (source) resistance (including the "on" resistance of the respective N or P channel device) and

i_n is the current through the n th output pin connected to this common ground or power pin.

Given these parameters, the voltage rise or drop due to iR effects is:

$$\Delta V = R \cdot \sum_{n=0}^{N-1} i_n$$

4.1.8 Current Spiking or "Crowbar Noise"

As Figure 8B-22 illustrated, a CMOS output buffer is constructed as totem pole in which the output is taken from the common source (P type) and drain (N type) with the drain of the P type connected to power and the source of the N type connected to ground. When the input to the totem pole, or the P and N gates, switch, the Miller capacitance of the gate causes the gates to charge or discharge at some specified time constant. It is possible that both transistors can be on, one in saturation and the other passing through the linear region, creating a current path between power and ground that can damage the device. This is less a concern for internal transistors than it is for the "beefy" transistors at the I/O. This current spiking can not only introduce noise on the power and ground planes, but may damage the device as well. For this reason, Fujitsu has taken precautions in the design of the CMOS output buffers to prevent this problem from occurring.

4.2 Recommended Strategy for Pin Assignment

The assignment of Clock, Scan, and other signals, as well as power and ground, to specific pins on the package affects electrical behavior (speed, noise, reliability, etc.), board manufacturing requirements, and device reliability. Therefore, optimal pin assignment strategies should consider the variables over which the user has control (placement of non-scan inputs, outputs and bi-directionals) and the variables over which the vendor has control (power, ground and scan signal placement). Out of these relationships a method of placement can be developed, using the following approach:

- a) Prioritize the signals whose placement is most critical.
- b) Establish guidelines for the location of these signals, both in absolute position and relative to other signals.

4.2.1 Prioritization of Signals for Placement

Noise minimization is used to establish signal prioritization. All of the various forms of noise discussed in the last section are dependent on either i or di/dt , and L , M , R , or C . The signals affect i and di/dt , while the package pin location affects L , R and C . Figure 8B-27 provides an illustration of how electrical characteristics vary by pin position.

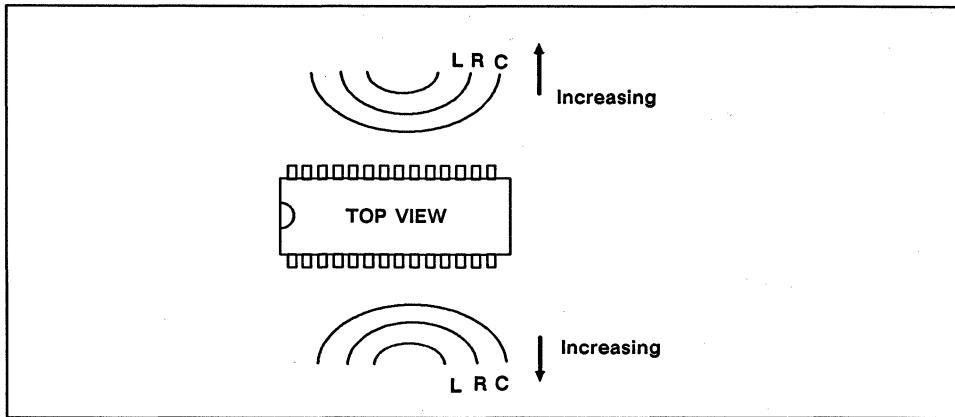


Figure 8B-27. Variation in Inductance, Resistance, and Capacitance as a Function of Pin Position

1

In general, the further a pin's external contact is from the die connection, the greater its resistance, impedance, and capacitance. Therefore, signal prioritization is established according to current or its time derivative, while location is guided by package pin characteristics. Input signals are classified by their noise sensitivity. If a spike on an input could be disastrous (as with a clock), that signal should be carefully located. Figure 8B-28 classifies signal type by electrical characteristics.

Signal Type	Current Characteristics (General)
Ground	Highest i , DC and di/dt
Power	High i , DC and di/dt
High drive outputs	High di/dt
Clocks	Highest noise sensitivity
Low drive outputs	Large di/dt
Other Signals	—

Figure 8B-28. Electrical Characteristics of Each Signal Type

4.2.2 Characteristics of Package Pins by Location

The inductance, capacitance, and resistance, all of which are critical to minimizing noise, are related not only to board construction, but also to the pin position on given packages, and the circuit to which the pins are bonded. The pin, lead frame, bonding wires, pads and buffer (input, output or bi-directional) all influence the characteristic L, R, and C of the line. See Figure 8B-29.

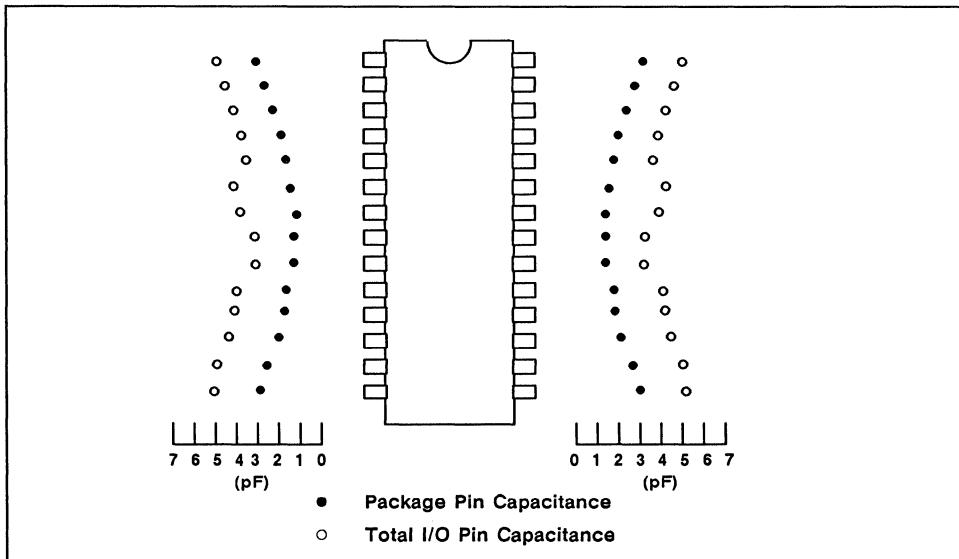


Figure 8B-29. Measured Pin Capacitance by Package Position

4.2.3 Relating Signal Type to Package Location

Since power and ground pins demand a large DC current (i), iR drops are the greatest concern, and so Fujitsu assigns power and ground to pins with the minimum resistance (and inductance as well). High-drive outputs exhibit a large di/dt , resulting from high capacitive loading, on power or high-power outputs. Since $L \ di/dt$ and $M \ di/dt$ noise is their greatest enemy, the best pins for these signals are those of minimum inductance. Furthermore, adjacent pins possess the greatest M , and thus couple the most $M \ di/dt$ noise. This means that noise-sensitive inputs, such as clocks, should be isolated from signals with a high di/dt , namely high-drive outputs.

4.2.4 Minimizing iR Drops on Power and Ground Pins

Since noise on ground affects the voltage level of all signals referenced to it, placement of the ground pins is most critical. For this reason, Fujitsu has preassigned the power (V_{dd}) and ground (V_{ss}) signals for all packages in a given gate array family according to the electrically optimal locations. Fujitsu also took into consideration manufacturing issues such as adjacent pin shorting due to probes and package rotation. Preassigning power pins also permits Fujitsu to develop load boards (which interface the packaged device to the tester) advanced enough to carry out high-speed functional testing of devices with high I/O count and to drive devices with relatively low noise. The predefined power and ground assignments for Fujitsu devices are found in the Package Pin Assignment Guide in the Design Manual for the appropriate gate array family, and are used in conjunction with the Package Matrix to determine pin assignment.

4.2.5 Minimizing the Self-Inductance of a Signal

Fujitsu believes that an ASIC designer concerned about designing a mini-computer, PC, mainframe or other complex system should not have to be concerned with determining specific on-chip noise issues, particularly since board-level noise issues are demanding enough. Therefore, Fujitsu

developed a straightforward grouping scheme for the placement of various types of signals relative to their distance from the nearest power and ground pins. As Figure 8B-30 shows, the self-inductance associated with a given signal is a function of the length of wire between it and its nearest ground (for a falling transition) or power (for a rising transition).

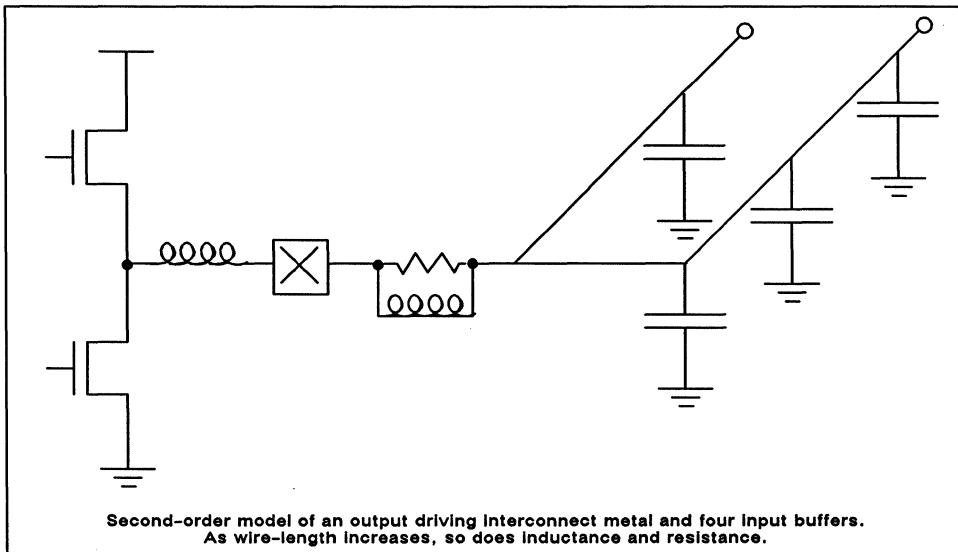


Figure 8B-30. Self-inductance in a Circuit

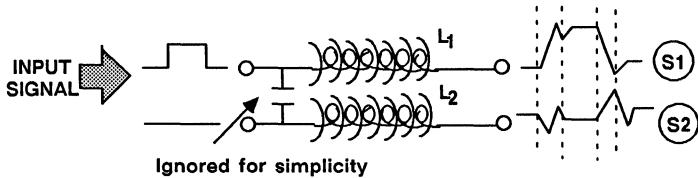
Since di/dt can vary greatly for outputs within a group, there are some general restrictions relating simultaneously switching outputs (SSOs) and their total current to the number of grounds on the chip. This is done by summing representative values like those shown in the UHB Data Sheet, which are weighed depending on the IOL of the given output buffer. Notice that, if the output buffer employs noise limiting circuitry (edge rate grading) then di/dt is less and the representative value is also less, meaning more of these outputs can be supported per ground pin.

In summary, to ensure that the iR drops and the ground bounce effect ($L di/dt$) are within reasonable limitations, Fujitsu has established guidelines for determining the number of necessary grounds and defining the pinout.

4.2.6 Placement of Clocks and Asynchronous Clear/Presets

In addition to causing the ground bounce and iR drops that can deteriorate an output signal's quality and alter the ground reference, output switching can also couple noise into adjacent sensitive inputs by mutual inductance, as shown in Figure 8B-31. For that reason, the designer should ensure that clocks and asynchronous clear and preset signals are not placed near outputs, particularly high drive outputs. To further isolate inputs from noise, the designer should minimize the inductance (length) of the return loop from the input buffer to ground by placing this type of input near a ground pin. The mutual inductance of the input buffer itself can be minimized if it, and any outputs nearby, are not assigned to high inductance pins. As discussed in Section 4.2.1, the center pins of a DIP, flatpack, or PLCC possess the lowest L and R, as do the inner rows of PGAs,

making them most suitable for Vdd, Vss and high drive outputs. But the edges of the package, while suitable for data signals, should be avoided when placing clocks and other sensitive signals, as they exhibit a high mutual inductance and large iR drop.



Noise is introduced on the adjacent lead S2 as S1 is driven in a manner described by Michael Faraday as:

$$V_{S2} = -M \frac{di_{S1}}{dt}$$

where M is the mutual inductance between the adjacent leads.

If S2 is also being driven, then the mutually induced noise is superimposed on the self induced noise already present, as described by:

$$V_{S2} = -M \frac{di_{S1}}{dt} + L_2 \frac{di_{S2}}{dt}$$

1

Figure 8B-31. Crosstalk and What Promotes It.

4.3 Summary: Choosing the Package and Assigning the Pins

This discussion of noise as related to packaging and its effect on pinout should help the designer appreciate the care Fujitsu has taken to ensure that noise margins within the device are restricted to maximize system reliability. It should also provide the designer with a basis for establishing optimum pin assignments. This section will now conclude with a step-by-step procedure to choose an optimal package, and assign pins to it.

4.4 Package Selection Checklist

When selecting the package for an ASIC device, the designer should consider the following points:

1. Define a subset of the Fujitsu packages that can be supported by your company's manufacturing capabilities.
2. Estimate, as closely as possible, the gate and I/O counts of the circuit(s).
3. Determine the number of power and ground pins required by considering the following:
 - a) Representative value limitations for SSOs.
 - b) Limitation of the sum of the sink current (IOL) per ground pin.
 - c) Limitation of instantaneous current per ground pin to satisfy metal migration restrictions.

4. Using the package and pin assignment section of the Design Manual, determine the packages that satisfy the signal, power, and ground pin requirements of the circuit.
5. Make sure that the electrical, mechanical, and thermal properties of the chosen packages are suitable for the application.
6. Check the mechanical dimensions in Fujitsu's ASIC Package Catalog and the power and ground pin assignment tables and grouping charts in the appropriate package and pin assignment tables for the chosen technology. Please contact Fujitsu regarding pricing trade-offs when evaluating packages or partitioning the system.

4.5 Pin Assignment Checklist

1. Follow Fujitsu's pin assignments in the Package and Pin Assignment section of the Design Manuals. Although multiple pinouts of the same package may be offered in some cases, all power and ground signals indicated on the chosen package must be connected on the board.
2. Assign input pins (in excess of 5 MHz) and high power output buffers ($I_{OL} = 24mA$) according to the appropriate pin assignment table.
3. Place all high-drive (power and high power) outputs near ground pins; the higher the drive, the closer they should be placed. SSOs should be placed particularly close to ground pins.
4. Place SSOs in groups belonging to given ground pins.
5. Distance noise-sensitive signals such as clocks and asynchronous clears and presets away from SSOs and high-drive outputs. Also, assign them to pins with low inductance and resistance, preferably near a ground, if one is available away from SSOs or high-drive outputs.
6. Place SSOs on low inductance pins, such as those located on the inner rows and middle position of the PGAs.

Following these guidelines should assist the designer in choosing the best package for the application, one that results in a device with reliable and predictable electrical performance and without harmful DC and AC effects on the system. There are other system interface issues such as device decoupling and termination that should be considered during design. These are discussed in Fujitsu's application note "Interfacing CMOS and BiCMOS VLSIs."

5.0 Thermal Issues in CMOS ASIC Packaging

CMOS has traditionally been associated with low power, one of the classic advantages it has over ECL. While ECL continually draws high current to supply its internal differential amplifiers and emitter-follower circuits, CMOS draws current primarily when it is switching. The total power dissipation of a CMOS device is dependent on the number of gates, the switching frequency, and the loading on the output of the gates. The revolution in CMOS technology that has resulted in gate densities of 100K gates has been accompanied by increases in all of these factors influencing power dissipation. Prior to 1985, when Fujitsu introduced the world's first 20,000 gate array, the C20000UH, CMOS gate arrays were not of sufficient integration density to warrant concerns about thermal control. But advancing CMOS technologies have forced this issue to the surface.

Power dissipation is important in defining the necessary power supply currents, since power is the product of current and voltage. However, the propagation delays and the reliability of a device are also dependent on the temperature at which the die operates, as discussed in Sections 2.2.3 and 2.3.4. To ensure that speed and reliability requirements are satisfied, it is necessary to estimate

the power dissipation of the device and, from this information, choose appropriate packages and system cooling techniques.

5.1 Estimation of Power Dissipation in CMOS Circuits

There are two constituent factors in the power dissipation of a semiconductor device: the DC power, which is dependent on the steady-state (quiescent) current, and the AC or dynamic power.

5.1.1 Estimation of Dynamic (AC) Power Dissipation

CMOS circuits are constructed of FETs, which possess very small leakage currents. Therefore, CMOS possesses a low quiescent or steady-state current. CMOS dissipates power primarily while it is charging or discharging node capacitance, or drawing switching current, which occurs as a gate changes state. This can be modeled as the familiar pull-up/pull-down circuit discussed in Section 4.1, charging and discharging a node capacitance, CL (shown in Figure 8B-25). This model holds true whether the node is internal or off-chip.

The switching current is a result of charging and discharging the node capacitance which, for periodic signals, occurs twice a cycle: once while charging the capacitance, and once while discharging it. The energy involved in charging or discharging a capacitance is $1/2(CL * V^2)$. The power is the energy divided by the period of time between successive changes (the clock period, T), multiplied by the two transitions that occur per cycle. Therefore, the dynamic or switching current of a CMOS circuit is defined as:

$$P_{d-dyn} = 2 * \frac{(CL * V^2)}{2 * T} = (CL * V^2) * f$$

where V is the supply voltage and f is the frequency of the given signal.

This is the power calculation for a single gate. The power dissipation for entire chip, however is much more complicated, since not all gates are simultaneously active. The degree of switching activity varies greatly within a circuit and depends on the nature of the circuits (synchronous sequential gates tend to switch concurrently, while combinational gates switch more randomly), the input stimulus (whether the circuit is stimulated at a periodic interval or asynchronously) and other design-dependent issues. Based on Fujitsu's experience, gate activity is on the average about 20%. This same figure is applied to the power estimation for output and input buffers.

5.1.2 Estimation of Quiescent (DC) Power Dissipation

There are two sources/sinks of DC current in a CMOS ASIC: the leakage current of the gates (gate leakage) and the DC current that flows through output and bidirectional buffers in output mode. The gate leakage in CMOS devices, even dense ones, is in the range of tens of microamperes, and is negligible. The DC current of the output buffers is the current that the buffer sources or sinks in steady state. This current level depends on the leakage currents of the driven loads, but for simplicity will be assumed to be equivalent to the IOL and IOH rating of the buffers. The DC power can be estimated for each output buffer by analyzing:

- (1) the product of source current times the voltage difference from the power rail (Vdd-Voh), and
- (2) the sink current times the low-level voltage (Vol).

This calculation is valid provided the duty cycle, or the portion of the cycle that the output is low versus the portion of the cycle that the output is high, weighs the sum of the two components. The total DC power may be determined by extending this method to each output and bidirectional buffer.

5.1.3 Estimation of Total Power Dissipation

The total power dissipation of a circuit is the sum of the DC and AC components. I/O buffers dissipate both DC and AC power when switching, while internal gates may be considered for the sake of simplicity, to dissipate only AC. The theory behind CMOS power dissipation is simple; however, the task of calculating the power dissipation can be tedious and prone to error. Therefore, Fujitsu has devised methods for estimating the power dissipation for each CMOS technology. These methods are presented in the Design Manual for the appropriate technology, available through the Field Applications Engineers at local Fujitsu Sales Offices or Technical Resource Centers.

5.2 The Relationship Between Power Dissipation and Temperature

A device draws current through the power supply pins and the I/O buffers. As it does so, it dissipates thermal energy proportional to the power dissipated in the device. Assuming that the power dissipation of a device has been estimated as P_d , using the method described in Section 5.1.1, how can one relate this power to the temperature of the die and the package, and also determine the warming effect on the surrounding environment?

The answer lies with two principles of heat transfer: conduction and convection. When an object is in a state of thermal equilibrium it is isothermal, seeing a constant temperature across its body. As the temperature of one end of the object is raised by the introduction of energy, it is no longer in equilibrium; heat begins to flow from the warmer region to the cooler region through the process of conduction.

When a lake in winter is filled with water at a constant temperature, just above 32°F, it may still freeze. It will freeze at the surface, however, not the bottom. This is because heat is drawn from the water into the air through convection, the act of cooling by a gas.

These same mechanisms, conduction and convection, act upon a packaged semiconductor device and determine its junction temperature, the package or case temperature, and the warming effect on the surroundings.

5.2.1 Determining the Junction Temperature of a Device

Figure 8B-32 shows the paths through which heat flows in a packaged device. Each interface of materials with different properties of thermal conduction must be considered when determining the flow of heat from the die to the surroundings. The back side of the die is attached to a lead frame or slug, usually by means of a eutectic bond (material heat bonded with some conductive material, such as silver). Heat flows through this path from the die to the package, then from the package to the surrounding air.

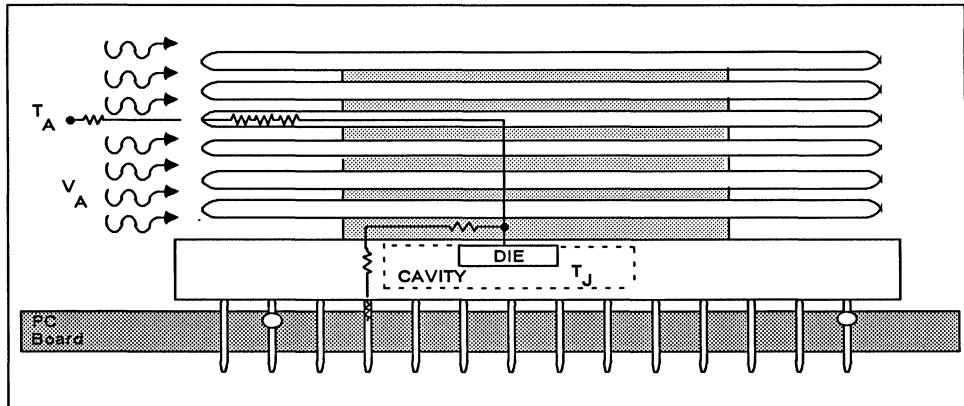


Figure 8B-32. Heat Flow through a Cavity-down Ceramic PGA with an Annular Fin Heat Sink

From the die junction to the package, there is some associated thermal impedance (or resistance to the flow of heat). This impedance can be calculated, but may also be estimated in the following way. Operate a device and determine its power dissipation. Then, using some mechanism such as a thermal diode, whose forward bias voltage tracks linearly with temperature, determine the junction temperature. Then, after measuring the case temperature, determine the thermal impedance along the path from the die junction to the case (package body) using the following equation:

$$\Theta_{jc} = \frac{(T_c - T_j)}{P_d}$$

where T_c and T_j are the case and junction temperatures, respectively.

A similar procedure is followed when determining the thermal impedance between the junction and the ambient environment, except that the case temperature is replaced by the measurement of the ambient temperature:

$$\Theta_{ja} = \frac{(T_a - T_j)}{P_d}$$

While Θ_{jc} relies on conduction as its cooling mechanism, Θ_{ja} reflects convective cooling. Therefore, Θ_{ja} varies with airflow and is specified at a given airflow, or as static ($= 0$).

Since thermal impedance depends on the heat conduction path between the die and some other interface, it can be modeled the same way as current flowing through real impedance or resistance. Therefore, as in circuit theory, when multiple interfaces are oriented in parallel, the thermal impedance is lowered. However, the situation is different from circuit theory in that when a very low impedance interface such as a heat sink is placed in the conduction path the flow capacity is increased, with the heat sink pulling heat out at a faster rate, lowering the thermal impedance.

5.2.2 Using Thermal Impedance Data

Thermal impedance information and power dissipation information are used to estimate junction temperature and ambient temperature rise. Which impedance figure to use is based on how the

device is to be cooled. If the device is air cooled (convective), then Θ_{ja} should be applied, while Θ_{jc} should be used if conductive techniques such as heat pipes or cold plates are employed. For example, the junction temperature may be obtained by multiplying the power dissipation of the device by the appropriate Θ_{ja} and adding the ambient temperature. It is not surprising that this indicates that a small thermal impedance is desirable to achieve a low junction temperature.

Junction temperature is used to determine worst case delay multipliers and the package options for Fujitsu's CMOS AU (Sea-of-Gates) family. The junction temperature also indicates whether reliability goals are being met. The designer can trade off packages (which exhibit varying thermal impedances) with cooling techniques (such as varying the amount of airflow in a system) to achieve the desired junction temperature and consequently, worst case delay multiplier and reliability targets.

5.3 Summary of Thermal Issues

Although thermal considerations in CMOS have not previously been of great concern, since the frequency and density of the devices have not required such concern, current generations of CMOS devices are stimulating an awareness of these matters. This section has surveyed some of the issues involved in applying thermal analysis to CMOS devices and using the information gained from such analysis to determine the appropriate packaging and cooling techniques.

6.0 Summary of the Note

As VLSI circuits increase in complexity, pin count and die size increase as well, placing greater demands on packaging, board layout, and manufacturing. Fujitsu has addressed these problems with more exotic forms of packaging such as the surface mount PGA and the staggered PGA, while also stressing the importance of other surface mount packages. But simply making these packages available is not sufficient; Fujitsu must also provide the support and information necessary to ensure that these packages can successfully be accommodated by our customers in an efficient manner. Field Applications support in the local sales offices, technical information such as this Application Note, and centralized package specialists at Fujitsu's San Jose headquarters have all been established to provide this support.

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Section 2

UHB Series CMOS Gate Array Unit Cell Library

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Unit Cell Specification Information

This section contains specifications for all the unit cells available for the UHB Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates. A basic cell contains one pair of P-channel and one pair of N-channel transistors.

How to Read a Unit Cell Specification

The following paragraphs numbered 1–10 explain how the information given in the UHB Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

1. The unit cell name appears in the upper left corner of the page.
2. The unit cell function is given on the same line as the unit cell name.
3. The number of basic cells (BC) or equivalent that make up the unit cell is shown in the upper right corner of the page.
4. Propagation delay parameters for the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t_0) is given in ns. KCL, the delay constant for the cell (delay time per load unit) is given in ns/pF. KCL2 and CDR2 are a delay constant and an output driving factor used to calculate delay when a unit cell is loaded beyond its published output driving factor (CDR).
5. The cell (logic) symbol is shown in the top left box under the cell name.
6. Clock parameters (in ns) for unit cells such as flip-flops and counters that make use of clock signals are given in a table directly below the propagation delay parameters.
7. Input loading factors are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
8. The output drive factor is shown directly under the input loading factor. The output drive factor is the maximum number of load units the unit cell can drive while performing at published specifications.
9. The function (truth) table, if applicable, is shown in a box at the lower left side of the page.
10. The unit cell schematic, or equivalent circuit, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.

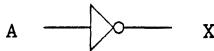
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					UHB Version																																																	
Cell Name	Function				Number of BC																																																	
1 → T2D	2:1 Selector				→ 2																																																	
2	Cell Symbol																																																					
3	Propagation Delay Parameter																																																					
4	tup	KCL	t0	KCL	KCL2																																																	
	0.50 0.54	0.15 0.15	0.56 0.41	0.10 0.10	CDR2																																																	
5	A B S1 S2	X	Path																																																			
6	Parameter																																																					
7	Symbol																																																					
8	Typ (ns)*																																																					
9	Input Loading Factor (ℓ_u)																																																					
	A,B S	1 1																																																				
10	Output Driving Factor (ℓ_u)																																																					
	X	14																																																				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																																																						
Function Table			Equivalent Circuit																																																			
9	<table border="1"> <thead> <tr> <th colspan="3">Inputs</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>S1</th> <th>S2</th> <th>X</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>X</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>X</td> <td>L</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>X</td> <td>H</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>L</td> <td>INHIBIT</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>H</td> <td>INHIBIT</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>H</td> <td>INHIBIT</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>H</td> <td>INHIBIT</td> </tr> </tbody> </table>			Inputs			Output	A	B	S1	S2	X	L	X	L	H	H	H	X	L	H	L	X	L	H	L	H	X	H	H	L	L	L	H	L	L	INHIBIT	L	H	H	H	INHIBIT	H	L	L	H	INHIBIT	H	L	H	H	INHIBIT		
Inputs			Output																																																			
A	B	S1	S2	X																																																		
L	X	L	H	H																																																		
H	X	L	H	L																																																		
X	L	H	L	H																																																		
X	H	H	L	L																																																		
L	H	L	L	INHIBIT																																																		
L	H	H	H	INHIBIT																																																		
H	L	L	H	INHIBIT																																																		
H	L	H	H	INHIBIT																																																		
10	S2																																																					
UHB-T2D-E2 Sheet 1/1			Page 17-17																																																			

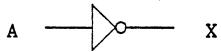
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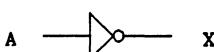
Inverter and Buffer Family

Page	Unit Cell Name	Function	Basic Cells
2-7	V1N	Inverter	1
2-8	V2B	Power Inverter	1
2-9	V1L	Double Power Inverter	2
2-10	B1N	True Buffer	1
2-11	BD3	True Delay Buffer	(> 5ns) 5
2-12	BD4	Delay Cell	(> 4ns) 4
2-13	BD5	Delay Cell	(>10ns) 9
2-14	BD6	Delay Cell	(>22ns) 17

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
V1N	Inverter					1
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.28	0.16	0.35	0.09	0.12	4	A → X
Parameter						Symbol
						Typ(ns)*
Pin Name	Input Loading Factor (λ_u)					
	A	1				
Pin Name	Output Driving Factor (λ_u)					
	X	18				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
V2B	Power Inverter					1
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
		0.25	0.08	0.25	0.05	0.08
					CDR2	Path
					7	A → X
Parameter						Symbol
						Typ(ns)*
Pin Name		Input Loading Factor (ℓ_u)				
A		2				
Pin Name		Output Driving Factor (ℓ_u)				
X		36				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

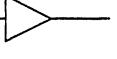
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
V1L	Inverting Clock Buffer					2
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
		0.35	0.04	0.67	0.03	CDR2
		Path				
		A → X				
		Parameter				
		Symbol				
		Typ(ns)*				
Pin Name	Input Loading Factor (λ_u)					
	A 4					
Pin Name	Output Driving Factor (λ_u)					
	X 55					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
B1N	True Buffer					1
Cell Symbol	Propagation Delay Parameter					
	tup		tdn			
	t0	KCL	t0	KCL	KCL2	CDR2
	0.58	0.16	0.68	0.08		
						A → X
Parameter	Symbol			Typ(ns)*		
Pin Name	Input Loading Factor (λ_u)					
A	1					
Pin Name	Output Driving Factor (λ_u)					
X	18					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

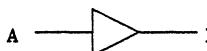
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
BD3	Delay Cell					5
Cell Symbol		Propagation Delay Parameter				
		t _{up}	t _{dn}			
		t ₀	KCL	t ₀	KCL	KCL2 CDR2
		5.33	0.16	4.71	0.12	0.13 4
		Path				
		A → X				
		Parameter				
		Symbol				
		Typ(ns)*				
Pin Name	Input Loading Factor (ℓ_u)					
	A	1				
Pin Name	Output Driving Factor (ℓ_u)					
	X	18				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
BD4	Delay Cell					4		
Cell Symbol		Propagation Delay Parameter						
		tup	tdn					
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.56	0.57	4.10	0.31	0.36	4	A → X
		Parameter				Symbol	Typ(ns)*	
Pin Name	Input Loading Factor (ℓ_u)							
	A	4						
Pin Name	Output Driving Factor (ℓ_u)							
	X	6						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>								
UHB-BD4-E2 Sheet 1/1								
					Page 1-6			

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version					
Cell Name	Function	Number of BC					
Cell Symbol	Propagation Delay Parameter				Path		
	tup	tdn					
	t0	KCL	t0	KCL	KCL2	CDR2	
	10.92	0.16	10.35	0.10	0.15	4	A → X
Pin Name	Input Loading Factor (λ_u)		Parameter	Symbol	Typ(ns)*		
A	1						
Pin Name	Output Driving Factor (λ_u)						
X	18						
* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.							

2

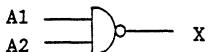
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
BD6	Delay Cell					17
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
		22.00	0.17	21.82	0.09	0.14
					CDR2	Path
					4	A → X
Parameter						Symbol
						Typ(ns)*
Pin Name						
A						
Pin Name						
X						
Input Loading Factor (μ u)						
A						
Output Driving Factor (μ u)						
X						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
UHB-BD6-E1 Sheet 1/1						Page 1-8

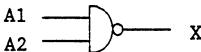
NAND Family

Page	Unit Cell Name	Function	Basic Cells
2-17	N2N	2-input NAND	1
2-18	N2B	Power 2-input NAND	3
2-19	N2K	Fast Power 2-input NAND	2
2-20	N3N	3-input NAND	2
2-21	N3B	Power 3-input NAND	3
2-22	N4N	4-input NAND	2
2-23	N4B	Power 4-input NAND	4
2-24	N6B	Power 6-input NAND	5
2-25	N8B	Power 8-input NAND	6
2-26	N9B	Power 9-input NAND	8
2-27	NCB	Power 12-input NAND	10
2-28	NGB	Power 16-input NAND	11
2-29	N3K	Fast Power 3-input NAND	3
2-30	N4K	Fast Power 4-input NAND	4

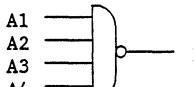
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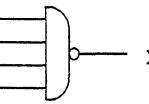
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
N2B	Power 2-input NAND					3
Cell Symbol		Propagation Delay Parameter				
		t _{up}	t _{dn}			
		t ₀	KCL	t ₀	KCL	KCL2
		1.10	0.08	1.42	0.04	CDR2
						Path A → X
		Parameter				Symbol
						Typ(ns)*
Pin Name	Input Loading Factor (λ_u)					
	A	1				
Pin Name	Output Driving Factor (λ_u)					
	X	36				
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>						

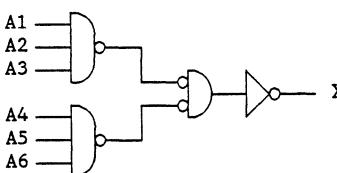
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version					
Cell Name	Function					Number of BC					
N2K	Power 2-input NAND					2					
Cell Symbol		Propagation Delay Parameter									
		t _{up}	t _{dn}								
		t ₀	KCL	t ₀	KCL	KCL2					
		0.37	0.08	0.43	0.07	0.09					
					CDR2	Path					
					7	A → X					
Parameter						Symbol					
						Typ(ns)*					
Pin Name		Input Loading Factor (ℓ_u)									
A		2									
Pin Name		Output Driving Factor (ℓ_u)									
X		36									
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>											

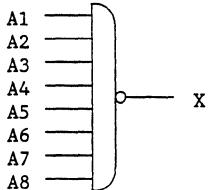
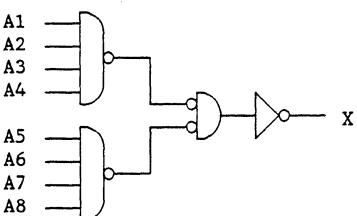
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
N3B	Power 3-input NAND					3		
Cell Symbol	Propagation Delay Parameter							
		tup	tdn			Path		
		t0	KCL	t0	KCL	KCL2	CDR2	A → X
		1.28	0.08	1.70	0.04			
		Parameter	Symbol	Typ(ns)*				
Pin Name	Input Loading Factor (ℓ_u)							
A	1							
Pin Name	Output Driving Factor (ℓ_u)							
X	36							
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								
UHB-N3B-E2 Sheet 1/1						Page 2-5		

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version					
Cell Name	Function					Number of BC					
N4N	4-input NAND					2					
Cell Symbol		Propagation Delay Parameter									
		tup	tdn								
		t0	KCL	t0	KCL	KCL2 CDR2					
		0.62	0.16	0.74	0.24						
		Parameter			Symbol	Typ(ns)*					
Pin Name		Input Loading Factor (ℓ_u)									
A		1									
Pin Name		Output Driving Factor (ℓ_u)									
X		10									
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>											

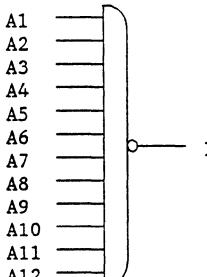
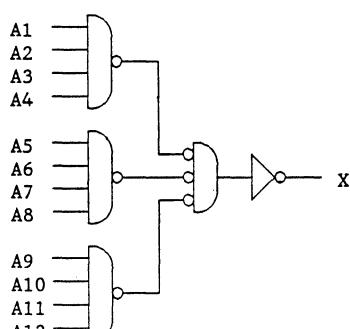
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version					
Cell Name	Function					Number of BC					
N4B	Power 4-input NAND					4					
Cell Symbol		Propagation Delay Parameter									
		tup	tdn			Path					
		t0	KCL	t0	KCL	KCL2	CDR2	A → X			
		1.38	0.08	1.90	0.04						
		Parameter				Symbol	Typ(ns)*				
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (ℓ_u)</th></tr> </thead> <tbody> <tr> <td>A</td><td>1</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓ_u)	A	1						
Pin Name	Input Loading Factor (ℓ_u)										
A	1										
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (ℓ_u)</th></tr> </thead> <tbody> <tr> <td>X</td><td>36</td></tr> </tbody> </table>		Pin Name	Output Driving Factor (ℓ_u)	X	36						
Pin Name	Output Driving Factor (ℓ_u)										
X	36										
		* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.									

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version						
Cell Name	Function					Number of BC						
N6B	Power 6-input NAND					5						
Cell Symbol	Propagation Delay Parameter											
	t _{up}	t _{dn}				Path						
	t ₀ 1.37	KCL 0.08	t ₀ 2.02	KCL 0.04	KCL2 0.07	CDR2 7	A → X					
Parameter					Symbol	Typ(ns)*						
Pin Name	Input Loading Factor (2u)											
A	1											
Pin Name	Output Driving Factor (2u)											
X	36											
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.												
Equivalent Circuit												
												

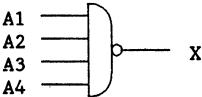
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version				
Cell Name	Function	Number of BC						
N8B	Power 8-input NAND	6						
Cell Symbol		Propagation Delay Parameter						
		t _{up}	t _{dn}					
		t ₀	KCL	t ₀	KCL			
		1.44	0.08	2.21	0.04			
		KCL2	CDR2	Path				
		0.07	7	A → X				
		Parameter			Symbol			
					Typ(ns)*			
Pin Name	Input Loading Factor (ℓu)							
	A	1						
Pin Name	Output Driving Factor (ℓu)							
	X	36						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>								
Equivalent Circuit								
								
UHB-N8B-E2 Sheet 1/1								
Page 2-9								

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version			
Cell Name	Function	Number of BC							
NCB	Power 12-input NAND	10							
Cell Symbol		Propagation Delay Parameter							
		tup	tdn			Path A → X			
		t0	KCL	t0	KCL	KCL2	CDR2		
		1.52	0.08	2.86	0.05	0.09	8		
		Parameter			Symbol	Typ(ns)*			
Pin Name	Input Loading Factor (ℓ_u)								
	A	1							
Pin Name	Output Driving Factor (ℓ_u)								
	X	36							
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Equivalent Circuit									
									
UHB-NCB-E2 Sheet 1/1									
Page 2-11									

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version																				
Cell Name	Function	Number of BC																				
NGB	Power 16-input NAND	11																				
Cell Symbol	Propagation Delay Parameter																					
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="2">tdn</th><th colspan="2"></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th></tr> </thead> <tbody> <tr> <td>1.53</td><td>0.08</td><td>3.47</td><td>0.06</td><td>0.09</td><td>8</td></tr> </tbody> </table>			tup		tdn				t0	KCL	t0	KCL	KCL2	CDR2	1.53	0.08	3.47	0.06	0.09	8	Path
tup		tdn																				
t0	KCL	t0	KCL	KCL2	CDR2																	
1.53	0.08	3.47	0.06	0.09	8																	
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16	X				A → X																	
Pin Name	Input Loading Factor (λ_u)																					
A	1																					
Pin Name	Output Driving Factor (λ_u)																					
X	36																					
<p>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</p>																						
Equivalent Circuit																						
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16	X																					

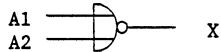
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
N3K	Power 3-input NAND					
Cell Symbol	Propagation Delay Parameter					
	tup		tdn			Path A → X
	t0	KCL	t0	KCL	KCL2	
	0.48	0.07	0.65	0.08		
	Parameter				Symbol	Typ(ns)*
Pin Name	Input Loading Factor (ℓ_u)					
A	2					
Pin Name	Output Driving Factor (ℓ_u)					
X	28					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
N4K	Power 4-input NAND					4	
Cell Symbol		Propagation Delay Parameter					
		tup	tdn			Path A → X	
		t0	KCL	t0	KCL		KCL2
		0.56	0.07	0.76	0.10		
Parameter						Symbol	
						Typ(ns)*	
Pin Name	Input Loading Factor (ℓ_u)						
	A	2					
Pin Name	Output Driving Factor (ℓ_u)						
	X	20					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

NOR Family

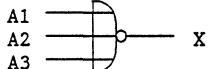
Page	Unit Cell Name	Function	Basic Cells
2-33	R2N	2-input NOR	1
2-34	R2B	Power 2-input NOR	3
2-35	R2K	Power 2-input NOR	2
2-36	R3N	3-input NOR	2
2-37	R3B	Power 3-input NOR	3
2-38	R4N	4-input NOR	2
2-39	R4B	Power 4-input NOR	4
2-40	R6B	Power 6-input NOR	5
2-41	R8B	Power 8-input NOR	6
2-42	R9B	Power 9-input NOR	8
2-43	RCB	Power 12-input NOR	10
2-44	RGB	Power 16-input NOR	11
2-45	R3K	Power 3-input NOR	3
2-46	R4K	Power 4-input NOR	4

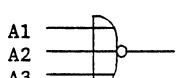
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
R2N	2-input NOR					1
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
		0.40	0.29	0.44	0.08	0.11
					CDR2	4
						Path A → X
Parameter						Symbol
						Typ(ns)*
Pin Name	Input Loading Factor (ℓ_u)					
	A	1				
Pin Name	Output Driving Factor (ℓ_u)					
	X	14				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

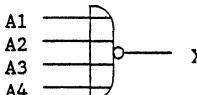
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
R2B	Power 2-input NOR					3
Cell Symbol	Propagation Delay Parameter					
		tup	tdn			
		t0	KCL	KCL2	CDR2	Path
		1.36	0.08	1.25	0.04	A → X
		Parameter	Symbol	Typ(ns)*		
Pin Name	Input Loading Factor (λ_u)					
A	1					
Pin Name	Output Driving Factor (λ_u)					
X	36					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
UHB-R2B-E2 Sheet 1/1						Page 3-2

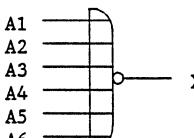
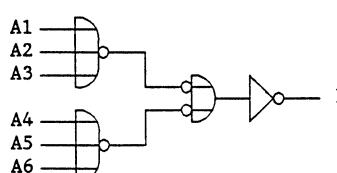
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
R2K	Power 2-input NOR					2				
Cell Symbol		Propagation Delay Parameter								
		tup	tdn							
		t0	KCL	t0	KCL	KCL2				
		0.45	0.14	0.45	0.06	CDR2				
						Path A → X				
		Parameter				Symbol				
						Typ(ns)*				
Pin Name		Input Loading Factor (μ A)								
A		2								
Pin Name		Output Driving Factor (μ A)								
X		36								
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>										

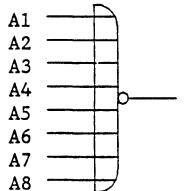
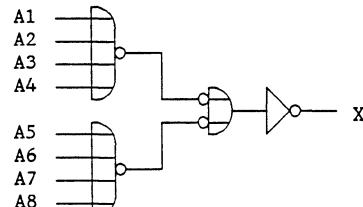
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHE" Version
Cell Name	Function					Number of BC
R3N	3-input NOR					2
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
		0.84	0.41	0.46	0.09	0.12
					CDR2	Path
					4	A → X
		Parameter			Symbol	Typ(ns)*
Pin Name	Input Loading Factor (ℓ_u)					
	A	1				
Pin Name	Output Driving Factor (ℓ_u)					
	X	10				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
UHB-R3N-E2		Sheet 1/1				
					Page 3-4	

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
R3B	Power 3-input NOR					3
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			Path
		t0	KCL	t0	KCL	CDR2
		1.99	0.08	1.37	0.04	A → X
Parameter						Symbol
						Typ(ns)*
Pin Name		Input Loading Factor (ℓ_u)				
A		1				
Pin Name		Output Driving Factor (ℓ_u)				
X		36				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

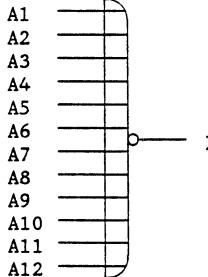
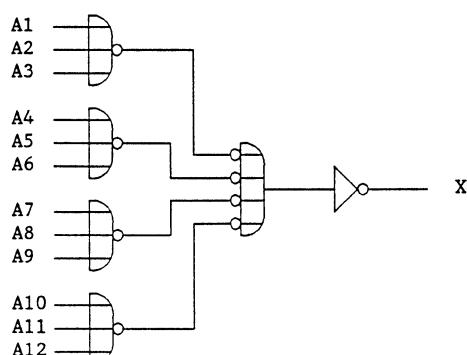
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version				
Cell Name	Function						Number of BC				
R4N	4-input NOR						2				
Cell Symbol		Propagation Delay Parameter									
		tup		tdn							
		t0	KCL	t0	KCL	KCL2	CDR2				
		1.24	0.54	0.46	0.09	0.13	4				
							Path A → X				
		Parameter									
							Symbol				
							Typ(ns)*				
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (λ_u)</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>1</td> </tr> </tbody> </table>		Pin Name	Input Loading Factor (λ_u)	A	1						
Pin Name	Input Loading Factor (λ_u)										
A	1										
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (λ_u)</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>6</td> </tr> </tbody> </table>		Pin Name	Output Driving Factor (λ_u)	X	6						
Pin Name	Output Driving Factor (λ_u)										
X	6										
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>											
UHB-R4N-E2		Sheet 1/1									
						Page 3-6					

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function	Number of BC						
R4B	Power 4-input NOR	4						
Cell Symbol		Propagation Delay Parameter						
		tup	tdn					
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.50	0.08	1.34	0.04			A → X
		Parameter				Symbol	Typ(ns)*	
Pin Name	Input Loading Factor (ℓ_u)							
	A	1						
Pin Name	Output Driving Factor (ℓ_u)							
	X	36						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version				
Cell Name	Function	Number of BG						
R6B	Power 6-input NOR	5						
Cell Symbol		Propagation Delay Parameter						
		tup	tdn					
		t0 2.25	KCL 0.08	t0 1.48	KCL 0.04			
		KCL2	CDR2		Path A → X			
		Parameter			Symbol			
					Typ(ns)*			
Pin Name	Input Loading Factor (ℓ_u)							
	A	1						
Pin Name	Output Driving Factor (ℓ_u)							
	X	36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								
Equivalent Circuit								
								

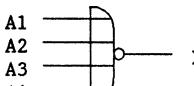
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																						
Cell Name	Function	Number of BC																								
R8B	Power 8-input NOR																									
Cell Symbol	Propagation Delay Parameter																									
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="3">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th></tr> </thead> <tbody> <tr> <td>2.84</td><td>0.08</td><td>1.51</td><td>0.04</td><td></td></tr> <tr> <td></td><td></td><td></td><td></td><td>CDR2</td></tr> </tbody> </table>					tup		tdn			t0	KCL	t0	KCL	KCL2	2.84	0.08	1.51	0.04						CDR2	Path A → X
tup		tdn																								
t0	KCL	t0	KCL	KCL2																						
2.84	0.08	1.51	0.04																							
				CDR2																						
A1 A2 A3 A4 A5 A6 A7 A8																										
Pin Name	Input Loading Factor (λ_u)																									
A	1																									
Pin Name	Output Driving Factor (λ_u)																									
X	36																									
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																										
Equivalent Circuit																										
A1 A2 A3 A4 A5 A6 A7 A8																										

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version																					
Cell Name	Function	Number of BC																					
R9B	Power 9-input NOR	8																					
Cell Symbol	Propagation Delay Parameter																						
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="3">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th></tr> </thead> <tbody> <tr> <td>2.49</td><td>0.08</td><td>1.68</td><td>0.04</td><td></td></tr> <tr> <td></td><td></td><td></td><td></td><td>CDR2</td></tr> </tbody> </table>		tup		tdn			t0	KCL	t0	KCL	KCL2	2.49	0.08	1.68	0.04						CDR2	Path A → X
tup		tdn																					
t0	KCL	t0	KCL	KCL2																			
2.49	0.08	1.68	0.04																				
				CDR2																			
A1 A2 A3 A4 A5 A6 A7 A8 A9	X																						
Parameter	Symbol	Typ(ns)*																					
Pin Name	Input Loading Factor (lu)																						
A	1																						
Pin Name	Output Driving Factor (lu)																						
X	36																						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																							
Equivalent Circuit																							
A1 A2 A3																							
A4 A5 A6																							
A7 A8 A9																							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version								
Cell Name	Function	Number of BC										
RCB	Power 12-input NOR	10										
Cell Symbol		Propagation Delay Parameter										
		t _{up}	t _{dn}									
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	Path				
		2.74	0.08	1.75	0.04			A → X				
		Parameter				Symbol	Typ(ns)*					
Pin Name		Input Loading Factor (lu)										
A		1										
Pin Name		Output Driving Factor (lu)										
X		36										
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>												
Equivalent Circuit												
												

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version																					
Cell Name	Function	Number of BC																					
RGB	Power 16-input NOR	11																					
Cell Symbol	Propagation Delay Parameter																						
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="2">tdn</th><th></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th></tr> </thead> <tbody> <tr> <td>3.43</td><td>0.08</td><td>1.82</td><td>0.04</td><td></td></tr> <tr> <td></td><td></td><td></td><td></td><td>CDR2</td></tr> </tbody> </table>		tup		tdn			t0	KCL	t0	KCL	KCL2	3.43	0.08	1.82	0.04						CDR2	Path
tup		tdn																					
t0	KCL	t0	KCL	KCL2																			
3.43	0.08	1.82	0.04																				
				CDR2																			
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16	X			A → X																			
Pin Name	Input Loading Factor (μ u)	Parameter	Symbol	Typ(ns)*																			
A	1																						
Pin Name	Output Driving Factor (μ u)																						
X	36																						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																							
Equivalent Circuit																							
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16	X																						

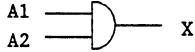
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
R3K	Power 3-input NOR					3	
Cell Symbol	Propagation Delay Parameter						
					tup tdn		
	t0	KCL	t0	KCL	KCL2	CDR2	Path
	0.66	0.17	0.32	0.04	0.07	7	A → X
	Parameter				Symbol	Typ(ns)*	
Pin Name	Input Loading Factor (ℓ_u)						
A	2						
Pin Name	Output Driving Factor (ℓ_u)						
X	20						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

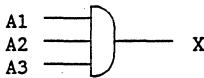
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
R4K	Power 4-input NOR					4				
Cell Symbol		Propagation Delay Parameter								
		tup	tdn							
		t0	KCL	t0	KCL	KCL2				
		1.08	0.23	0.35	0.03	0.05				
					7	Path A → X				
		Parameter			Symbol	Typ(ns)*				
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (ℓ_u)</th></tr> </thead> <tbody> <tr> <td>A</td><td>2</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓ_u)	A	2					
Pin Name	Input Loading Factor (ℓ_u)									
A	2									
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (ℓ_u)</th></tr> </thead> <tbody> <tr> <td>X</td><td>12</td></tr> </tbody> </table>		Pin Name	Output Driving Factor (ℓ_u)	X	12					
Pin Name	Output Driving Factor (ℓ_u)									
X	12									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
UHB-R4K-E1 Sheet 1/1										
Page 3-14										

AND Family

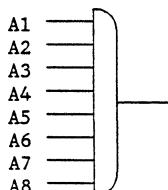
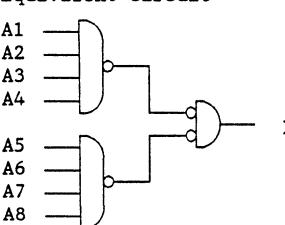
Page	Unit Cell Name	Function	Basic Cells
2-49	N2P	Power 2-input AND	2
2-50	N3P	Power 3-input AND	3
2-51	N4P	Power 4-input AND	3
2-52	N8P	Power 8-input AND	6

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
N2P	Power 2-input AND					2
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
		1.01	0.08	0.86	0.04	0.06
					CDR2	Path
					7	A → X
		Parameter			Symbol	Typ(ns)*
Pin Name	Input Loading Factor (λ_u)					
	A	1				
Pin Name	Output Driving Factor (λ_u)					
	X	36				
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																		
Cell Name	Function						Number of BC																		
N3P	Power 3-input AND						3																		
Cell Symbol		Propagation Delay Parameter																							
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">tup</th><th colspan="4">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th></tr> </thead> <tbody> <tr> <td>1.32</td><td>0.08</td><td>1.07</td><td>0.04</td><td>0.06</td><td>7</td></tr> </tbody> </table>					tup		tdn				t0	KCL	t0	KCL	KCL2	CDR2	1.32	0.08	1.07	0.04	0.06	7	Path A → X
tup		tdn																							
t0	KCL	t0	KCL	KCL2	CDR2																				
1.32	0.08	1.07	0.04	0.06	7																				
Pin Name		Parameter																							
A																									
Pin Name		Symbol																							
X																									
Input Loading Factor (δu)																									
A																									
Output Driving Factor (δu)																									
X																									
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																									

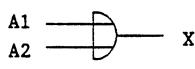
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
N8P	Power 8-input AND				6			
Cell Symbol		Propagation Delay Parameter						
		tup	tdn					
		t0	KCL	t0	KCL			
		1.72	0.14	1.45	0.04			
		KCL2			KCL2			
		CDR2			CDR2			
		8			A → X			
		Parameter			Symbol			
					Typ(ns)*			
Pin Name		Input Loading Factor (μu)						
A		1						
Pin Name		Output Driving Factor (μu)						
X		36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								
Equivalent Circuit								
								

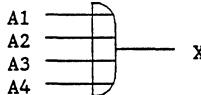
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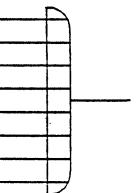
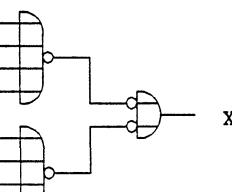
Page	Unit Cell Name	Function	Basic Cells
2-55	R2P	Power 2-input OR	2
2-56	R3P	Power 3-input OR	3
2-57	R4P	Power 4-input OR	3
2-58	R8P	Power 8-input OR	6

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
R2P	Power 2-input OR					2
Cell Symbol		Propagation Delay Parameter				
		t _{up}	t _{dn}			
		t ₀	KCL	t ₀	KCL	KCL2
		0.78	0.08	1.14	0.05	0.07
					CDR2	Path
					8	A → X
		Parameter			Symbol	Typ(ns)*
Pin Name	Input Loading Factor (lu)					
	A	1				
Pin Name	Output Driving Factor (lu)					
	X	36				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
R3P	Power 3-input OR					3
Cell Symbol	Propagation Delay Parameter					
		tup	tdn			
		t0	KCL	t0	KCL	KCL2 CDR2
A1 A2 A3	X	0.90	0.08	1.84	0.06	0.08 8
						Path A → X
Parameter						Symbol Typ(ns)*
Pin Name	Input Loading Factor (ℓu)					
	A	1				
Pin Name	Output Driving Factor (ℓu)					
	X	36				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name		Function				Number of BC		
R4P	Power 4-input OR					3		
Cell Symbol		Propagation Delay Parameter						
		tup		tdn		Path A → X		
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.90	0.08	2.52	0.07	0.10	8	
Parameter		Symbol			Typ(ns)*			
Pin Name	Input Loading Factor (l <u>u</u>)							
	A	1						
Pin Name	Output Driving Factor (l <u>u</u>)							
	X	36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								

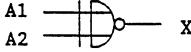
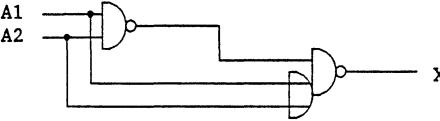
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version																	
Cell Name	Function	Number of BC																	
R8P	Power 8-input OR	6																	
Cell Symbol		Propagation Delay Parameter																	
		<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="2">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th></tr> </thead> <tbody> <tr> <td>0.98</td><td>0.08</td><td>2.68</td><td>0.08</td><td>0.10</td><td>8</td></tr> </tbody> </table>		tup		tdn		t0	KCL	t0	KCL	KCL2	CDR2	0.98	0.08	2.68	0.08	0.10	8
tup		tdn																	
t0	KCL	t0	KCL	KCL2	CDR2														
0.98	0.08	2.68	0.08	0.10	8														
		Path A → X																	
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (ℓ_u)</th></tr> </thead> <tbody> <tr> <td>A</td><td>1</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓ_u)	A	1														
Pin Name	Input Loading Factor (ℓ_u)																		
A	1																		
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (ℓ_u)</th></tr> </thead> <tbody> <tr> <td>X</td><td>36</td></tr> </tbody> </table>		Pin Name	Output Driving Factor (ℓ_u)	X	36														
Pin Name	Output Driving Factor (ℓ_u)																		
X	36																		
<p>* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.</p>																			
Equivalent Circuit																			
																			

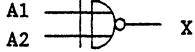
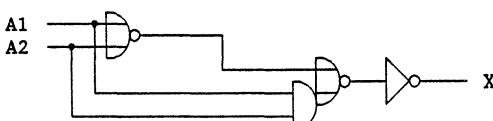
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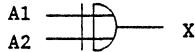
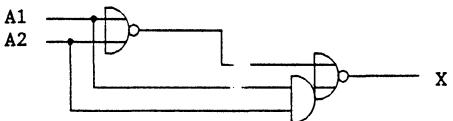
EXNOR/EXOR Family

Page	Unit Cell Name	Function	Basic Cells
2-61	X1N	Exclusive NOR	3
2-62	X1B	Power Exclusive NOR	4
2-63	X2N	Exclusive OR	3
2-64	X2B	Power Exclusive OR	4
2-65	X3N	3-input Exclusive NOR	5
2-66	X3B	Power 3-input Exclusive NOR	6
2-67	X4N	3-input Exclusive OR	5
2-68	X4B	Power 3-input Exclusive OR	6

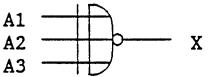
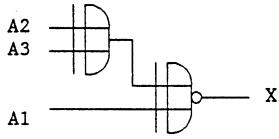
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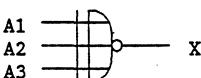
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version					
Cell Name	Function					Number of BC					
X1N	Exclusive NOR					3					
Cell Symbol		Propagation Delay Parameter									
		tup	tdn								
		t0	KCL	t0	KCL	KCL2 CDR2					
		1.16	0.29	0.96	0.13	0.16 4					
		Path									
		A → X									
		Parameter									
		Symbol									
		Typ(ns)*									
Pin Name		Input Loading Factor (ℓ_u)									
A		2									
Pin Name		Output Driving Factor (ℓ_u)									
X		18									
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Equivalent Circuit											
											
UHB-X1N-E2		Sheet 1/1									
						Page 6-1					

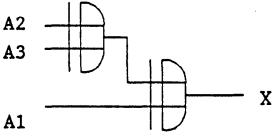
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version	
Cell Name	Function					Number of BC
X1B	Power Exclusive NOR					4
Cell Symbol	Propagation Delay Parameter					
	tup	tdn				Path
	t0 1.49	KCL 0.08	t0 1.77	KCL 0.05	KCL2 0.09	CDR2 7
	A1		X			A → X
Parameter	Symbol	Typ(ns)*				
Pin Name	Input Loading Factor (ℓ_u)					
A	2					
Pin Name	Output Driving Factor (ℓ_u)					
X	36					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
Equivalent Circuit						
						
UHB-X1B-E2 Sheet 1/1				Page 6-2		

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version					
Cell Name	Function					Number of BC					
X2N	Exclusive OR					3					
Cell Symbol		Propagation Delay Parameter									
		tup	tdn								
		t0	KCL	t0	KCL	KCL2 CDR2					
		1.11	0.29	1.17	0.13	0.16 4					
		Path				A → X					
		Parameter				Symbol Typ(ns)*					
Pin Name	Input Loading Factor (λ_u)										
	A	2									
Pin Name	Output Driving Factor (λ_u)										
	X	14									
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>											
Equivalent Circuit											
											
UHB-X2N-E2 Sheet 1/1						Page 6-3					

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version						
Cell Name	Function					Number of BC						
X2B	Power Exclusive OR					4						
Cell Symbol		Propagation Delay Parameter										
		tup	tdn									
		t0	KCL	t0	KCL	KCL2 CDR2						
		1.43	0.08	1.64	0.05	0.07 7						
		Path				A → X						
Parameter						Symbol						
						Typ(ns)*						
Pin Name	Input Loading Factor (λ_u)											
	A		2									
Pin Name	Output Driving Factor (λ_u)											
	X		36									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.												
Equivalent Circuit												
UHB-X2B-E2		Sheet 1/1										
Page 6-4												

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
X3N	3-input Exclusive NOR					5				
Cell Symbol		Propagation Delay Parameter								
		t _{up}	t _{dn}							
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	Path		
		2.72	0.29	2.32	0.13	0.16	4	A → X		
		Parameter				Symbol	Typ(ns)*			
Pin Name	Input Loading Factor (ℓ_u)									
	A	2								
Pin Name	Output Driving Factor (ℓ_u)									
	X	18								
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>										
Equivalent Circuit										
										
UHB-X3N-E2 Sheet 1/1										
Page 6-5										

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version					
Cell Name	Function					Number of BC				
X3B	Power 3-input Exclusive NOR									
Cell Symbol		Propagation Delay Parameter								
		tup		tdn		Path A → X				
		t0	KCL	t0	KCL	KCL2	CDR2			
		2.64	0.08	3.39	0.05	0.09	7			
		Parameter				Symbol	Typ(ns)*			
Pin Name	Input Loading Factor (ℓ_u)									
	A	2								
Pin Name	Output Driving Factor (ℓ_u)									
	X	36								
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>										
Equivalent Circuit										
										
UHB-X3B-E2 Sheet 1/1										
Page 6-6										

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function						Number of BC
X4N	3-input Exclusive OR						
Cell Symbol	Propagation Delay Parameter						
	tup			tdn			
	t0	KCL	t0	KCL	KCL2	CDR2	Path
	2.82	0.29	2.53	0.13	0.16	4	A → X
	Parameter			Symbol	Typ(ns)*		
Pin Name	Input Loading Factor (ℓ_u)						
A	2						
Pin Name	Output Driving Factor (ℓ_u)						
X	14						
	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
Equivalent Circuit							
							
UHB-X4N-E2	Sheet 1/1						

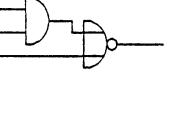
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
X4B	Power 3-input Exclusive OR									
Cell Symbol	Propagation Delay Parameter									
	tup		tdn							
	t0	KCL	t0	KCL	KCL2	CDR2				
	2.47	0.08	3.13	0.05	0.07	7				
						Path A → X				
	A1		X							
	A2									
	A3									
	Parameter									
					Symbol	Typ(ns)*				
	Pin Name		Input Loading Factor (ℓ_u)							
	A		2							
	Pin Name		Output Driving Factor (ℓ_u)							
	X		36							
	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Equivalent Circuit										
	A2									
	A3									
	A1		X							

2

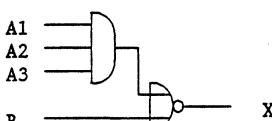
AND-OR-Inverter Family (AOI)

Page	Unit Cell Name	Function	Basic Cells
2-71	D23	2 AND into 2 NOR AOI	2
2-72	D14	3 AND into 2 NOR AOI	2
2-73	D24	2, 2 ANDS into 2 NOR AOI	2
2-74	D34	2 AND into 3 NOR AOI	2
2-75	D36	3, 2 ANDS into 3 NOR AOI	3
2-76	D44	2 OR into 2 AND inot 2 NOR AOI	2

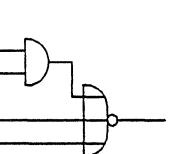
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version																								
Cell Name	Function	Number of BC																								
D23	2-wide 2-AND 3-input AOI	2																								
Cell Symbol	Propagation Delay Parameter																									
		Path																								
<table border="1"> <thead> <tr> <th>tup</th> <th>tdn</th> <th></th> <th></th> <th></th> <th></th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> <th>KCL2</th> <th>CDR2</th> </tr> </thead> <tbody> <tr> <td>0.73</td> <td>0.29</td> <td>0.68</td> <td>0.14</td> <td></td> <td></td> </tr> <tr> <td>0.37</td> <td>0.22</td> <td>0.37</td> <td>0.09</td> <td>0.12</td> <td>4</td> </tr> </tbody> </table>		tup	tdn					t0	KCL	t0	KCL	KCL2	CDR2	0.73	0.29	0.68	0.14			0.37	0.22	0.37	0.09	0.12	4	A → X B → X
tup	tdn																									
t0	KCL	t0	KCL	KCL2	CDR2																					
0.73	0.29	0.68	0.14																							
0.37	0.22	0.37	0.09	0.12	4																					
<table border="1"> <thead> <tr> <th>Parameter</th> <th>Symbol</th> <th>Typ(ns)*</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> </tr> </tbody> </table>		Parameter	Symbol	Typ(ns)*																						
Parameter	Symbol	Typ(ns)*																								
Pin Name	Input Loading Factor (ℓ_u)																									
A	1																									
B	1																									
Pin Name	Output Driving Factor (ℓ_u)																									
X	14																									
<p>* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.</p>																										

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																		
Cell Name	Function					Number of BC																		
D14	2-wide 3-AND 4-input AOI																							
Cell Symbol	Propagation Delay Parameter																							
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="4">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th></tr> </thead> <tbody> <tr> <td>0.90 0.32</td><td>0.29 0.20</td><td>0.70 0.36</td><td>0.19 0.09</td><td>0.21 0.12</td><td>4 4</td></tr> </tbody> </table>					tup		tdn				t0	KCL	t0	KCL	KCL2	CDR2	0.90 0.32	0.29 0.20	0.70 0.36	0.19 0.09	0.21 0.12	4 4	Path
tup		tdn																						
t0	KCL	t0	KCL	KCL2	CDR2																			
0.90 0.32	0.29 0.20	0.70 0.36	0.19 0.09	0.21 0.12	4 4																			
																								
	<table border="1"> <thead> <tr> <th>Parameter</th><th>Symbol</th><th>Typ(ns)*</th></tr> </thead> <tbody> <tr> <td></td><td></td><td></td></tr> <tr> <td></td><td></td><td></td></tr> <tr> <td></td><td></td><td></td></tr> </tbody> </table>					Parameter	Symbol	Typ(ns)*																
Parameter	Symbol	Typ(ns)*																						
Pin Name	Input Loading Factor (ℓ_u)																							
A	1																							
B	1																							
Pin Name	Output Driving Factor (ℓ_u)																							
X	14																							
	<p>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</p>																							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version						
Cell Name	Function						Number of BC						
D24	2-wide 2-AND 4-input AOI						2						
Cell Symbol	Propagation Delay Parameter												
	tup			tdn									
	t0	KCL	t0	KCL	KCL2	CDR2	Path						
	0.54 0.67	0.22 0.22	0.62 0.83	0.14 0.14			A → X B → X						
	Parameter			Symbol	Typ(ns)*								
Pin Name	Input Loading Factor (λ_u)												
A	1												
B	1												
Pin Name	Output Driving Factor (λ_u)												
X	14												
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.													
UHB-D24-E2 Sheet 1/1				Page 7-3									

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
D34	3-wide 2-AND 4-input AOI					2
Cell Symbol		Propagation Delay Parameter				
		t _{up}	t _{dn}			
		t ₀	KCL	t ₀	KCL	KCL2 CDR2
		1.15 0.62	0.41 0.35	0.73 0.43	0.15 0.09	0.12 4
		Parameter				Path
						A → X B → X
Pin Name		Symbol				Typ(ns)*
A						
B						
Pin Name		Parameter				
X						
Input Loading Factor (f <u>u</u>)						
A						
B						
Output Driving Factor (f <u>u</u>)						
Pin Name						
X						
						* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

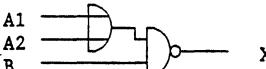
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
D36	3-wide 2-AND 6-input AOI					3
Cell Symbol	Propagation Delay Parameter					
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
		0.77	0.28	0.72	0.14	
		0.98	0.28	0.87	0.14	
		1.17	0.28	1.02	0.14	
						Path
						A → X
						B → X
						C → X
	Parameter	Symbol	Typ(ns)*			
Pin Name	Input Loading Factor (ℓ_u)					
A	1					
B	1					
C	1					
Pin Name	Output Driving Factor (ℓ_u)					
X	10					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
UHB-D36-E1		Sheet 1/1			Page 7-5	

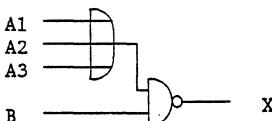
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
D44	2-wide 2-OR 2-AND 4-input AOI					2		
Cell Symbol		Propagation Delay Parameter						
		tup		tdn		Path		
		t0	KCL	t0	KCL	KCL2	CDR2	A → X B → X C → X
		1.04	0.41	0.78	0.14			
		1.03	0.41	0.64	0.14			
		0.99	0.29	0.48	0.09	0.11	4	
		Parameter				Symbol	Typ(ns)*	
Pin Name		Input Loading Factor (ℓ_u)						
A		1						
B		1						
C		1						
Pin Name		Output Driving Factor (ℓ_u)						
X		10						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>								
UHB-D44-E1		Sheet 1/1				Page 7-6		

OR-AND-Inverter Family (OAI)

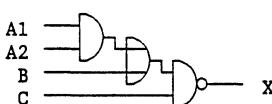
Page	Unit Cell Name	Function	Basic Cells
2-79	G23	2 OR into 2 NAND OAI	2
2-80	G14	3 OR into 2 NAND OAI	2
2-81	G24	2, 2 OR into 2 NAND OAI	2
2-82	G34	2 OR into 3 NAND OAI	2
2-83	G44	2 AND into 2 OR into 2 NAND OAI	2

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
G23	2-wide 2-OR 3-input OAI					2		
Cell Symbol		Propagation Delay Parameter						
		tup	tdn			Path		
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.72	0.29	0.55	0.14			A → X
		0.28	0.16	0.55	0.14			B → X
		Parameter				Symbol	Typ(ns)*	
Pin Name		Input Loading Factor (ℓ_u)						
A		1						
B		1						
Pin Name		Output Driving Factor (ℓ_u)						
X		18						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								
UHB-G23-E1		Sheet 1/1						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version	
Cell Name	Function				Number of BC	
G14	2-wide 3-OR 4-input OAI				2	
Cell Symbol	Propagation Delay Parameter					
	tup	tdn				
	t0 1.20 0.25	KCL 0.42 0.16	t0 0.65 0.65	KCL 0.14 0.14	KCL2 CDR2	Path A → X B → X
						
Parameter	Symbol	Typ(ns)*				
Pin Name	Input Loading Factor (λ_u)					
A	1					
B	1					
Pin Name	Output Driving Factor (λ_u)					
X	10					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version					
Cell Name	Function					Number of BC					
G24	2-wide 2-OR 4-input OAI					2					
Cell Symbol		Propagation Delay Parameter									
		tup	tdn	KCL	KCL2	CDR2					
		t0	KCL	t0	KCL	Path					
		0.50	0.29	0.70	0.14	A → X					
		0.90	0.29	0.60	0.14	B → X					
Parameter						Symbol					
						Typ(ns)*					
Pin Name		Input Loading Factor (ℓ_u)									
A		1									
B		1									
Pin Name		Output Driving Factor (ℓ_u)									
X	10										
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.											
UHB-G24-E2 Sheet 1/1											
Page 8-3											

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
G44	2-wide 2-AND 2-OR 4-input OAI					2	
Cell Symbol		Propagation Delay Parameter					
		t _{up}	t _{dn}				
		t ₀	KCL	t ₀	KCL	KCL2	Path
		0.73	0.29	0.86	0.19		A → X
		0.43	0.29	0.62	0.19		B → X
		0.50	0.16	0.52	0.14		C → X
		Parameter				Symbol	Typ(ns)*
Pin Name		Input Loading Factor (μ u)					
A		1					
B		1					
C		1					
Pin Name		Output Driving Factor (μ u)					
X		14					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							
UHB-G44-E1		Sheet 1/1				Page 8-5	

2

Multiplexer Family

Page	Unit Cell Name	Function	Basic Cells
2-87	T24	4:1 Power 4, 2 ANDs into 4 NOR Multiplexer	6
2-88	T26	6:1 Power 6, 2 ANDs into 6 NOR Multiplexer	10
2-89	T28	8:1 Power 8, 2 ANDs into 8 NOR Multiplexer	11
2-91	T32	2:1 Power 2, 3 ANDs into 2 NOR Multiplexer	5
2-92	T33	3:1 Power 3, 3 ANDs into 3 NOR Multiplexer	7
2-93	T34	4:1 Power 4, 3 AND into 4 NOR Multiplexer	9
2-94	T42	2:1 Power 2, 4 ANDs into 2 NOR Multiplexer	6
2-95	T43	3:1 Power 3, 4 ANDs into 3 NOR Multiplexer	10
2-96	T44	4:1 Power 4, 4 ANDs into 4 NOR Multiplexer	11
2-97	T54	4:1 Power 2, 2-3-4 ANDs into 4 NOR Multiplexer	10
2-98	U24	4:1 Power 4, 2 OR into 4 NAND Multiplexer	6
2-99	U26	6:1 Power 6, 2 OR into 6 NAND Multiplexer	9
2-100	U28	8:1 Power 8, 2 OR into 8 NAND Multiplexer	11
2-101	U32	2:1 Power 2, 3 OR into 2 NAND Multiplexer	5
2-102	U33	3:1 Power 3, 3 OR into 3 NAND Multiplexer	7
2-103	U34	4:1 Power 4, 3 OR into 4 NAND Multiplexer	9
2-104	U42	2:1 Power 2, 4 OR into 4 NAND Multiplexer	6
2-105	U43	3:1 Power 3, 4 OR into 3 NAND Multiplexer	9
2-106	U44	4:1 Power 4, 4 OR into 4 NAND Multiplexer	11

2

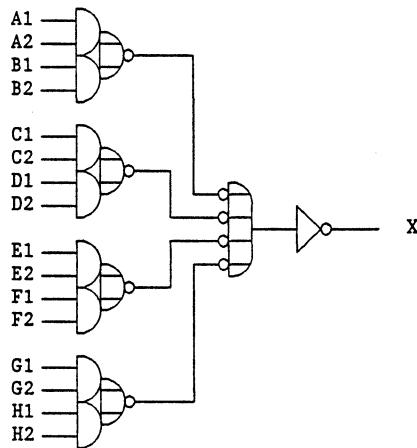
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
T24	Power 2-AND 4-wide Multiplexer							
Cell Symbol		Propagation Delay Parameter						
		tup	tdn					
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.62	0.08	1.52	0.04			A → X
		1.80	0.08	1.76	0.04			B → X
		1.58	0.08	1.64	0.04			C → X
		1.72	0.08	1.88	0.04			D → X
Parameter					Symbol	Typ(ns)*		
Pin Name		Input Loading Factor (ℓ_u)						
A		1						
B		1						
C		1						
D		1						
Pin Name		Output Driving Factor (ℓ_u)						
X		36						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>								
Equivalent Circuit								
UHB-T24-E1 Sheet 1/1								
Page 9-1								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version	
Cell Name	Function				Number of BC	
T28	Power 2-AND 8-wide Multiplexer					
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.12	0.08	1.52	0.04			A → X
2.32	0.08	1.80	0.04			B → X
2.12	0.08	1.68	0.04			C → X
2.28	0.08	1.96	0.04			D → X
2.20	0.08	2.16	0.04			E → X
2.36	0.08	2.08	0.04			F → X
2.20	0.08	1.92	0.04			G → X
2.36	0.08	2.18	0.04			H → X
Parameter				Symbol	Typ(ns)*	
Pin Name		Input Loading Factor (f <u>u</u>)				
A		1				
B		1				
C		1				
D		1				
E		1				
F		1				
G		1				
H		1				
Pin Name		Output Driving Factor (f <u>u</u>)				
X		36				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
UHB-T28-E1 Sheet 1/2			Page 9-3			

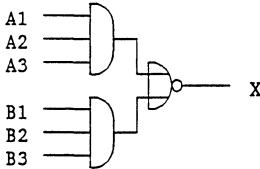
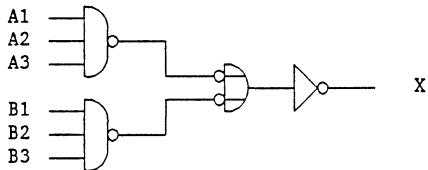
Cell Name

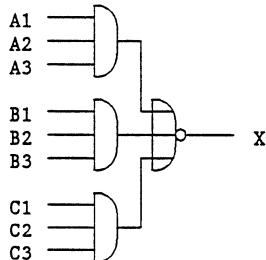
T28

Equivalent Circuit

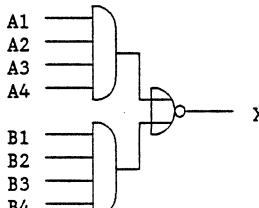
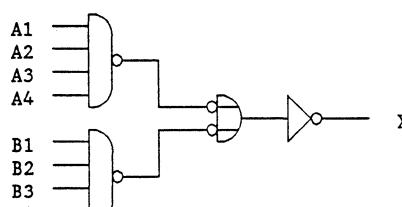


2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version			
Cell Name	Function	Number of BC					
T32	Power 3-AND 2-wide Multiplexer						
Cell Symbol		Propagation Delay Parameter					
		tup	tdn				
		t0	KCL	t0	KCL		
		1.52	0.08	1.68	0.04		
		1.52	0.08	1.80	0.04		
				KCL2	CDR2		
					Path		
					A → X		
					B → X		
Parameter							
Symbol							
Typ(ns)*							
Pin Name	Input Loading Factor (ℓ_u)						
	A	1					
Pin Name	Output Driving Factor (ℓ_u)						
	X	36					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							
Equivalent Circuit							
							
UHB-T32-E1 Sheet 1/1							
Page 9-5							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version				
Cell Name	Function	Number of BC						
T33	Power 3-AND 3-wide Multiplexer	7						
Cell Symbol		Propagation Delay Parameter						
		tup	tdn					
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.75	0.08	1.66	0.04			A → X
		1.75	0.08	1.78	0.04			B → X
		1.75	0.08	1.95	0.04			C → X
		Parameter			Symbol	Typ(ns)*		
Pin Name		Input Loading Factor (μu)						
A		1						
B		1						
C		1						
Pin Name		Output Driving Factor (μu)						
X		36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version											
Cell Name	Function	Number of BC													
T34	Power 3-AND 4-wide Multiplexer	9													
Cell Symbol		Propagation Delay Parameter													
		tup	tdn												
		t0	KCL	t0	KCL	KCL2	GDR2	Path							
		2.08	0.08	1.72	0.04			A → X							
		2.08	0.08	1.88	0.04			B → X							
		2.18	0.08	2.00	0.04			C → X							
		2.18	0.08	2.01	0.04			D → X							
		Parameter			Symbol	Typ(ns)*									
Pin Name	Input Loading Factor (lu)														
	A	1													
	B	1													
	C	1													
Pin Name	Output Driving Factor (lu)														
	X	36													
	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.														
Equivalent Circuit															

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
T42	Power 4-AND 2-wide Multiplexer					6				
Cell Symbol		Propagation Delay Parameter								
		tup	tdn							
		t0	KCL	t0	KCL	KCL2				
		1.60	0.08	1.88	0.04	CDR2				
		1.60	0.08	2.00	0.04					
						Path				
						A → X				
						B → X				
Parameter						Symbol				
						Typ(ns)*				
Pin Name	Input Loading Factor (μu)									
	A	1								
Pin Name	Output Driving Factor (μu)									
	X	36								
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>										
Equivalent Circuit										
										

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version
Cell Name	Function	Number of BC			
T43	Power 4-AND 3-wide Multiplexer				
Cell Symbol	Propagation Delay Parameter				
		tup	tdn		
	t0	KCL	t0	KCL	KCL2 CDR2
A1 A2 A3 A4	1.88 1.88 1.88	0.08 0.08 0.08	1.92 2.04 2.20	0.04 0.04 0.04	
B1 B2 B3 B4					
C1 C2 C3 C4					
	Parameter	Symbol	Typ(ns)*		
Pin Name	Input Loading Factor (ℓu)				
A B C	1 1 1				
Pin Name	Output Driving Factor (ℓu)				
X	36				
	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.				
Equivalent Circuit					
A1 A2 A3 A4					
B1 B2 B3 B4					
C1 C2 C3 C4					

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
T44	Power 4-AND 4-wide Multiplexer					11				
Cell Symbol	Propagation Delay Parameter				Parameter	Symbol				
	tup	tdn				Path				
	t0 KCL	t0 KCL	KCL2	CDR2						
A1 A2 A3 A4	2.16 0.08	1.92 0.04				A → X				
B1 B2 B3 B4	2.16 0.08	1.64 0.04				B → X				
C1 C2 C3 C4	2.16 0.08	2.20 0.04				C → X				
D1 D2 D3 D4	2.16 0.08	2.32 0.04				D → X				
	Parameter				Typ(ns)*					
Pin Name	Input Loading Factor (ℓ_u)				Symbol	Typ(ns)*				
A	1									
B	1									
C	1									
D	1									
Pin Name	Output Driving Factor (ℓ_u)									
X	36									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Equivalent Circuit										

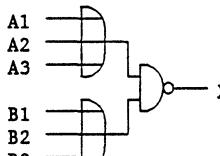
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																							
Cell Name	Function					Number of BC																							
T54	Power 4-2-3-2 AND 4-wide Multiplexer																												
Cell Symbol	Propagation Delay Parameter																												
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tup		tdn																											
t0	KCL	t0	KCL																										
2.06	0.08	1.96	0.04																										
1.92	0.08	1.64	0.04																										
2.06	0.08	2.06	0.04																										
1.92	0.08	1.88	0.04																										
				A → X B → X C → X D → X																									
Pin Name	Input Loading Factor (ℓu)																												
A	1																												
B	1																												
C	1																												
D	1																												
Pin Name	Output Driving Factor (ℓu)																												
X	36																												
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																													
Equivalent Circuit																													

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																																				
Cell Name	Function					Number of BC																																				
U24	Power 2-OR 4-wide Multiplexer							6																																		
Cell Symbol	Propagation Delay Parameter																																									
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tup		tdn																																								
t0	KCL	t0	KCL	KCL2	CDR2																																					
2.00	0.08	1.80	0.05	0.08	7																																					
1.44	0.08	1.75	0.05	0.08	7																																					
1.90	0.08	1.78	0.05	0.08	7																																					
1.38	0.08	1.70	0.05	0.08	7																																					
A1 A2							A → X																																			
B1 B2							B → X																																			
C1 C2							C → X																																			
D1 D2							D → X																																			
Parameter							Symbol																																			
Typ(ns)*																																										
Pin Name	Input Loading Factor (ℓ_u)																																									
A	1																																									
B	1																																									
C	1																																									
D	1																																									
Pin Name	Output Driving Factor (ℓ_u)																																									
X	36																																									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																																										
UHB-U24-E1 Sheet 1/1							Page 9-12																																			

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																																																
Cell Name	Function					Number of BC																																																
U26 Power 2-OR 6-wide Multiplexer						9																																																
Cell Symbol		Propagation Delay Parameter																																																				
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tup		tdn																																																				
t0	KCL	t0	KCL	KCL2	CDR2																																																	
2.00	0.08	2.34	0.05	0.08	7																																																	
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1.64	0.08	2.58	0.05	0.08	7																																																	
2.10	0.08	2.58	0.05	0.08	7																																																	
Pin Name		Parameter																																																				
Input Loading Factor (l <u>u</u>)																																																						
A	1																																																					
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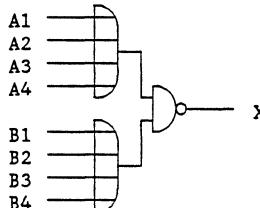
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version
Cell Name	Function						Number of BC
U32	Power 3-OR 2-wide Multiplexer						5
Cell Symbol	Propagation Delay Parameter						
	t _{up}		t _{dn}				
	t ₀	KCL	t ₀	KCL	KCL2	CDR2	Path
	2.15 2.11	0.08 0.08	1.66 1.63	0.05 0.05	0.08 0.08	7 7	A → X B → X
							
Pin Name	Parameter					Symbol	Typ(ns)*
A							
B							
Pin Name	Output Driving Factor (f <u>u</u>)						
X	36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
U33 Power 3-OR 3-wide Multiplexer						7		
Cell Symbol		Propagation Delay Parameter						
		tup	tdn			Path		
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.28	0.08	2.28	0.05	0.11	7	A → X
		2.25	0.08	2.38	0.05	0.11	7	B → X
		2.31	0.08	2.52	0.05	0.10	7	C → X
Parameter						Symbol	Typ(ns)*	
Pin Name		Input Loading Factor (μ u)						
A		1						
B		1						
C		1						
Pin Name		Output Driving Factor (μ u)						
X		36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
U34	Power 3-OR 4-wide Multiplexer					9		
Cell Symbol		Propagation Delay Parameter						
		tup	tdn			Path		
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.11	0.08	2.98	0.06	0.10	7	A → X
		2.13	0.08	3.00	0.06	0.10	7	B → X
		1.92	0.08	2.44	0.06	0.10	7	C → X
		2.11	0.08	2.69	0.06	0.10	7	D → X
Parameter						Symbol		
						Typ(ns)*		
Pin Name	Input Loading Factor (lu)							
	A	1						
Pin Name	Output Driving Factor (lu)							
	X	36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version
Cell Name	Function						Number of BC
U42	Power 4-OR 2-wide Multiplexer						6
Cell Symbol		Propagation Delay Parameter					
		tup			tdn		
		t0	KCL	t0	KCL	KCL2	CDR2
		2.60	0.08	1.71	0.05	0.08	7
		2.53	0.08	1.64	0.05	0.08	7
Parameter							Symbol
							Typ(ns)*
Pin Name		Input Loading Factor (Ω_u)					
A		1					
B		1					
Pin Name		Output Driving Factor (Ω_u)					
X		36					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

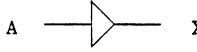
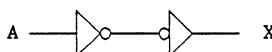
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function					Number of BC		
U43	Power 4-OR 3-wide Multiplexer					9		
Cell Symbol		Propagation Delay Parameter						
		tup	tdn			Path		
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.57	0.08	2.13	0.06	0.08	7	A → X
		2.62	0.08	2.26	0.06	0.08	7	B → X
		2.70	0.08	2.39	0.06	0.08	7	C → X
		Parameter			Symbol	Typ(ns)*		
Pin Name		Input Loading Factor (λ_u)						
A		1						
B		1						
C		1						
Pin Name		Output Driving Factor (λ_u)						
X		36						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>								

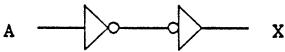
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
U44	Power 4-OR 4-wide Multiplexer					
11						
Cell Symbol	Propagation Delay Parameter					
			tup	tdn		
	t0	KCL	t0	KCL	KCL2	CDR2
A1	2.73	0.08	3.00	0.05	0.11	7
A2	2.72	0.08	2.88	0.05	0.11	7
A3	2.63	0.08	2.44	0.05	0.11	7
A4	2.67	0.08	2.69	0.05	0.11	7
B1						
B2						
B3						
B4						
C1						
C2						
C3						
C4						
D1						
D2						
D3						
D4						
Pin Name	Input Loading Factor (lu)					
A	1					
B	1					
C	1					
D	1					
Pin Name	Output Driving Factor (lu)					
X	36					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

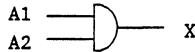
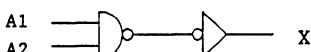
Clock Buffer Family

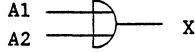
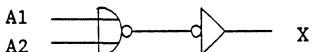
Page	Unit Cell Name	Function	Basic Cells
2-109	K1B	True Clock Buffer	2
2-110	K2B	Power Clock Buffer	3
2-111	K3B	Gated Clock (AND) Buffer	36
2-112	K4B	Gated Clock (OR) Buffer	36
2-113	K4B	Gated Clock (NAND) Buffer	3
2-114	KAB	Block Clock (OR) Buffer	55
2-115	KBB	Block Clock (OR x 10) Buffer	30

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version							
Cell Name	Function					Number of BC						
K1B	True Clock Buffer					2						
Cell Symbol		Propagation Delay Parameter										
		tup	tdn									
		t0	KCL	t0	KCL	KCL2 CDR2						
		0.72	0.08	0.86	0.04							
		Parameter		Symbol	Typ(ns)*							
Pin Name	Input Loading Factor (ℓ_u)											
	A	1										
Pin Name	Output Driving Factor (ℓ_u)											
	X	36										
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>												
Equivalent Circuit												
												

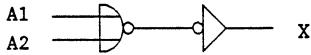
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
K2B	Power Clock Buffer					3				
Cell Symbol	Propagation Delay Parameter									
		tup	tdn							
		t0	KCL	t0	KCL	KCL2				
		1.06	0.04	1.20	0.03	CDR2				
						Path				
						A → X				
Pin Name	Input Loading Factor (λu)	Parameter				Symbol				
A	1									
Pin Name	Output Driving Factor (λu)									
X	55									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Equivalent Circuit										
										

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
K3B	Gated Clock (AND) Buffer							
Cell Symbol		Propagation Delay Parameter						
		tup		tdn				
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.00	0.08	1.00	0.04			A → X
Parameter					Symbol	Typ(ns)*		
Pin Name	Input Loading Factor (lu)							
	A	1						
Pin Name	Output Driving Factor (lu)							
	X	36						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>								
Equivalent Circuit								
								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
K4B	Gated Clock (OR) Buffer					2				
Cell Symbol		Propagation Delay Parameter								
		tup	tdn							
		t0	KCL	t0	KCL	KCL2				
		0.78	0.08	1.14	0.05	0.07				
						Path A → X				
Parameter						Symbol				
						Typ(ns)*				
Pin Name	Input Loading Factor (ℓ_u)									
	A	1								
Pin Name	Output Driving Factor (ℓ_u)									
	X	36								
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Equivalent Circuit										
										

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version					
Cell Name	Function				Number of BC				
K5B	Gated Clock (NAND) Buffer								
Cell Symbol		Propagation Delay Parameter							
		tup	tdn						
		t0	KCL	t0	KCL				
		1.14	0.08	1.48	0.04				
				KCL2	CDR2				
					Path A → X				
Parameter									
Pin Name		Symbol							
Input Loading Factor (λ_u)		Typ(ns)*							
A	1								
Pin Name		Output Driving Factor (λ_u)							
X	36								
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>									
Equivalent Circuit									
UHB-K5B-E2 Sheet 1/1			Page 10-5						

Equivalent Circuit

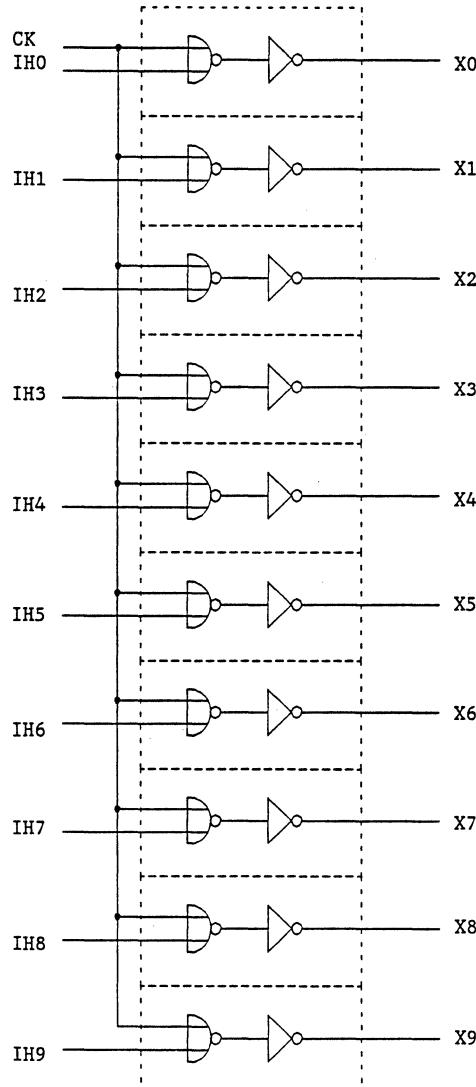


2

Cell Name

KBB

Equivalent Circuit

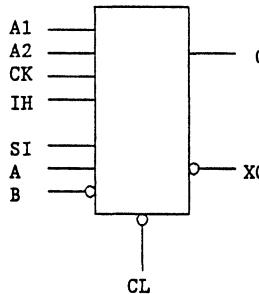


2

Scan Flip-Flop (Positive Edge Type) Family

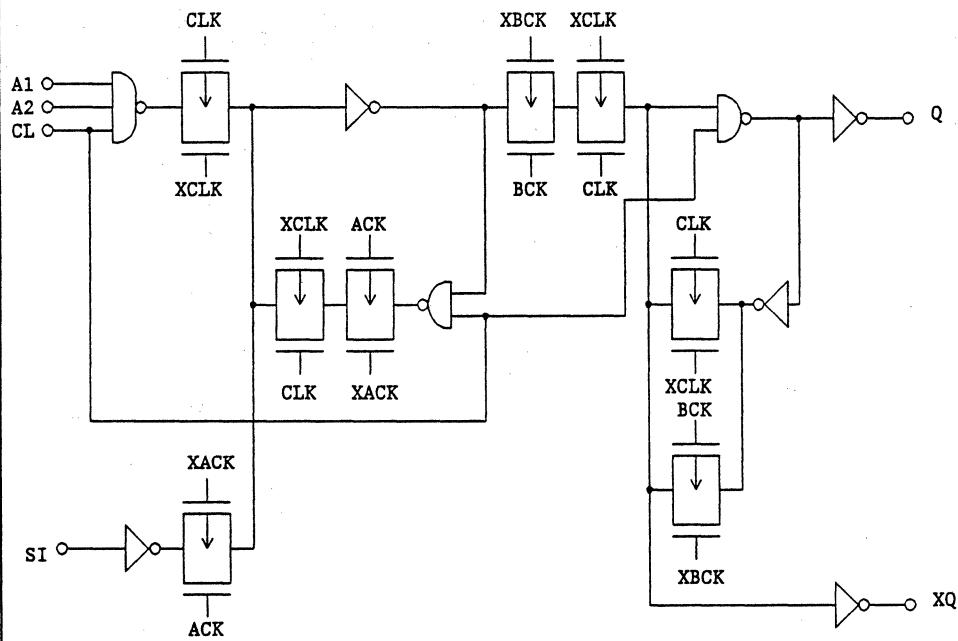
Page	Unit Cell Name	Function	Basic Cells
2-119	SDH	Scan D FF with 2:1 Multiplex with Clear and Clock Inhibit	14
2-122	SDJ	Scan D FF with 4:1 Multiplex with Clear and Clock Inhibit	15
2-125	SDK	Scan D FF with 3:1 Multiplex with Clear and Clock Inhibit	16
2-128	SJH	Scan J-K F with Clear and Clock Inhibit	36
2-131	SDD	Scan D FF with 2:1 Multiplex, Preset Clear, and Clock Inhibit	16
2-135	SDA	Scan 1-input D FF with Clock Inhibit	12
2-138	SDB	Scan 1-input D FF with Clock Inhibit	42
2-142	SHA	Scan 1-input D FF with Clock Inhibit	68
2-145	SHB	Scan 1-input D FF with Clock Inhibit and Q Output	62
2-148	SHC	Scan 1-input D FF with Clock Inhibit and XQ Output	62
2-151	SHJ	Scan D FF with 2:1 Multiplex and Clock Inhibit	78
2-154	SHK	Scan D FF with 3:1 Multiplex and Clock Inhibit	88

2

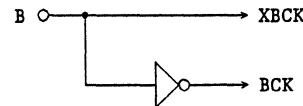
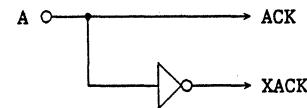
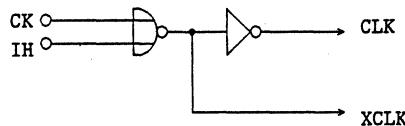
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																																		
Cell Name	Function						Number of BC																																		
SDH	SCAN 2-input DFF with Clear & Clock-Inhibit						14																																		
Cell Symbol	Propagation Delay Parameter																																								
			<table border="1"> <thead> <tr> <th>tup</th> <th>tdn</th> <th></th> <th></th> <th></th> <th></th> <th></th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> <th>KCL2</th> <th>CDR2</th> <th>Path</th> </tr> </thead> <tbody> <tr> <td>3.72</td> <td>0.08</td> <td>2.98</td> <td>0.04</td> <td>0.08</td> <td>7</td> <td>CK, IH → Q</td> </tr> <tr> <td>2.35</td> <td>0.08</td> <td>2.15</td> <td>0.06</td> <td>0.12</td> <td>7</td> <td>CK, IH → XQ</td> </tr> <tr> <td>3.79</td> <td>0.08</td> <td>1.07</td> <td>0.04</td> <td>0.08</td> <td>7</td> <td>CL → Q, XQ</td> </tr> </tbody> </table>		tup	tdn						t0	KCL	t0	KCL	KCL2	CDR2	Path	3.72	0.08	2.98	0.04	0.08	7	CK, IH → Q	2.35	0.08	2.15	0.06	0.12	7	CK, IH → XQ	3.79	0.08	1.07	0.04	0.08	7	CL → Q, XQ		
tup	tdn																																								
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			<table border="1"> <thead> <tr> <th>Parameter</th> <th>Symbol</th> <th>Typ(ns)*</th> </tr> </thead> <tbody> <tr> <td>Clock Pulse Width</td> <td>tCW</td> <td>5.4</td> </tr> <tr> <td>Clock Pause Time</td> <td>tCWH</td> <td>4.5</td> </tr> <tr> <td>Data Setup Time</td> <td>tSD</td> <td>3.7</td> </tr> <tr> <td>Data Hold Time</td> <td>tHD</td> <td>1.0</td> </tr> <tr> <td>Clear Pulse Width</td> <td>tLW</td> <td>4.5</td> </tr> <tr> <td>Clear Release Time</td> <td>tREM</td> <td>3.0</td> </tr> <tr> <td>Clear Hold Time</td> <td>tINH</td> <td>1.5</td> </tr> </tbody> </table>		Parameter	Symbol	Typ(ns)*	Clock Pulse Width	tCW	5.4	Clock Pause Time	tCWH	4.5	Data Setup Time	tSD	3.7	Data Hold Time	tHD	1.0	Clear Pulse Width	tLW	4.5	Clear Release Time	tREM	3.0	Clear Hold Time	tINH	1.5													
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Clear Pulse Width	tLW	4.5																																							
Clear Release Time	tREM	3.0																																							
Clear Hold Time	tINH	1.5																																							
Pin Name	Input Loading Factor (μ u)																																								
A1,A2	1																																								
CK	1																																								
IH	1																																								
CL	3																																								
SI	1																																								
A,B	2																																								
Pin Name	Output Driving Factor (μ u)																																								
Q	36																																								
XQ	36																																								
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Function Table																																									
MODE	INPUT					OUTPUT																																			
	CLK	CL	D	A	B	SI	Q XQ																																		
CLEAR	X	L	X	X	X	X	L H																																		
CLOCK	L→H	H	Di	L	L	X	Di Di																																		
	H	H	X	L	L	X	Q ₀ XQ ₀																																		
SCAN	H	H	X	L→H→L	H	Si	Q ₀ XQ ₀																																		
	H	H	X	L	H→L→H	X	Si Si																																		
Note : CLK = CK + IH D = A1 x A2																																									

Cell Name	
SDH	

Equivalent Circuit



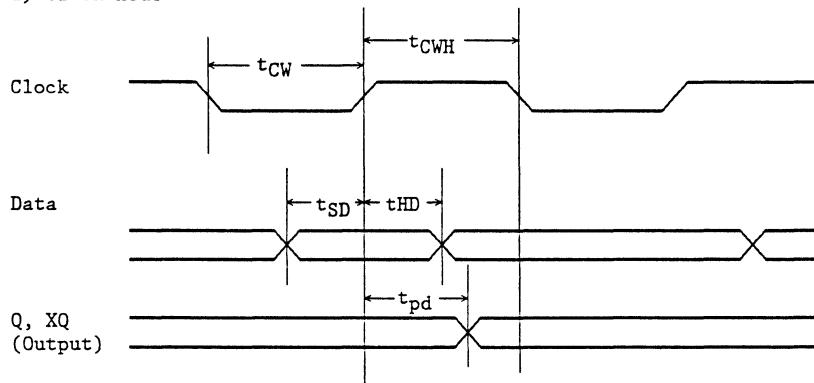
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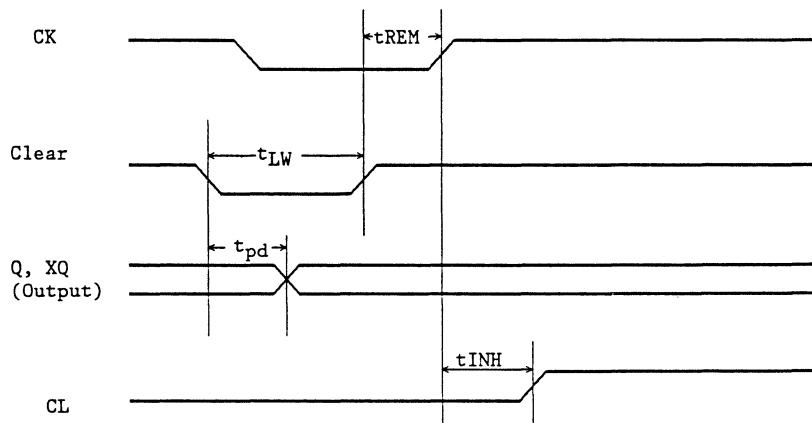
Cell Name
SDH

Definitions of Parameters

i) Clock Mode



ii) Clear Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																																																													
Cell Name	Function						Number of BC																																																													
SDJ	SCAN 4-input DFF with Clear & Clock-Inhibit																																																																			
Cell Symbol		Propagation Delay Parameter																																																																		
		tup	tdn				Path																																																													
		t0	KCL	t0	KCL	KCL2	CDR2																																																													
		2.75	0.08	3.02	0.04	0.08	7																																																													
		2.36	0.08	2.14	0.06	0.12	7																																																													
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		Clock Pause Time				tCWH	4.5																																																													
<table border="1"> <tr> <th>Pin Name</th> <th>Input Loading Factor (μu)</th> </tr> <tr> <td>A1, A2</td> <td>1</td> </tr> <tr> <td>B1, B2</td> <td>1</td> </tr> <tr> <td>CK</td> <td>1</td> </tr> <tr> <td>IH</td> <td>1</td> </tr> <tr> <td>CL</td> <td>3</td> </tr> <tr> <td>SI</td> <td>1</td> </tr> <tr> <td>A, B</td> <td>2</td> </tr> </table> <table border="1"> <tr> <th>Pin Name</th> <th>Output Driving Factor (μu)</th> </tr> <tr> <td>Q</td> <td>36</td> </tr> <tr> <td>XQ</td> <td>36</td> </tr> </table>	Pin Name	Input Loading Factor (μu)	A1, A2	1	B1, B2	1	CK	1	IH	1	CL	3	SI	1	A, B	2	Pin Name	Output Driving Factor (μu)	Q	36	XQ	36		Data Setup Time				tSD	4.4																																							
Pin Name	Input Loading Factor (μu)																																																																			
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Pin Name	Output Driving Factor (μu)																																																																			
Q	36																																																																			
XQ	36																																																																			
Data Hold Time				tHD	0.8																																																															
Clear Pulse Width				tLW	4.5																																																															
Clear Release Time				tREM	3.0																																																															
<table border="1"> <tr> <th>Mode</th> <th colspan="6">Input</th> <th colspan="2">Output</th> </tr> <tr> <th></th> <th>CLK</th> <th>CL</th> <th>D</th> <th>A</th> <th>B</th> <th>SI</th> <th>Q</th> <th>XQ</th> </tr> <tr> <td>CLEAR</td> <td>X</td> <td>L</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>L</td> <td>H</td> </tr> <tr> <td rowspan="2">CLOCK</td> <td>L→H</td> <td>H</td> <td>Di</td> <td>L</td> <td>L</td> <td>X</td> <td>Di</td> <td>Di</td> </tr> <tr> <td>H</td> <td>H</td> <td>X</td> <td>L</td> <td>L</td> <td>X</td> <td>Q_o</td> <td>XQ_o</td> </tr> <tr> <td rowspan="2">SCAN</td> <td>H</td> <td>H</td> <td>X</td> <td>L→H→L</td> <td>H</td> <td>Si</td> <td>Q_o</td> <td>XQ_o</td> </tr> <tr> <td>H</td> <td>H</td> <td>X</td> <td>L</td> <td>H→L→H</td> <td>X</td> <td>Si</td> <td>Si</td> </tr> </table>	Mode	Input						Output			CLK	CL	D	A	B	SI	Q	XQ	CLEAR	X	L	X	X	X	X	L	H	CLOCK	L→H	H	Di	L	L	X	Di	Di	H	H	X	L	L	X	Q _o	XQ _o	SCAN	H	H	X	L→H→L	H	Si	Q _o	XQ _o	H	H	X	L	H→L→H	X	Si	Si		Clear Hold Time				tINH	1.5
Mode	Input						Output																																																													
	CLK	CL	D	A	B	SI	Q	XQ																																																												
CLEAR	X	L	X	X	X	X	L	H																																																												
CLOCK	L→H	H	Di	L	L	X	Di	Di																																																												
	H	H	X	L	L	X	Q _o	XQ _o																																																												
SCAN	H	H	X	L→H→L	H	Si	Q _o	XQ _o																																																												
	H	H	X	L	H→L→H	X	Si	Si																																																												

* Minimum values for the typical operating condition.
The values for the worst case operating condition
are given by the maximum delay multiplier.

Function Table

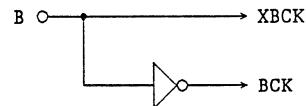
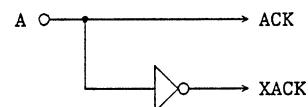
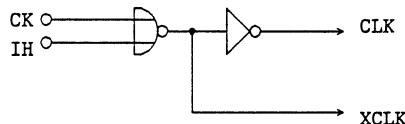
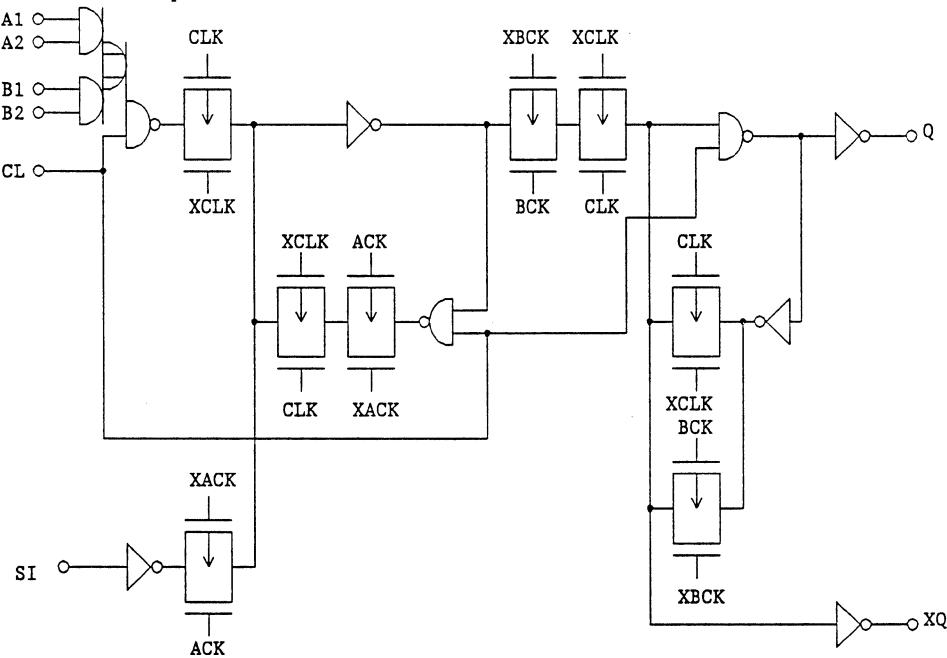
Mode	Input						Output	
	CLK	CL	D	A	B	SI	Q	XQ
CLEAR	X	L	X	X	X	X	L	H
CLOCK	L→H	H	Di	L	L	X	Di	Di
	H	H	X	L	L	X	Q _o	XQ _o
SCAN	H	H	X	L→H→L	H	Si	Q _o	XQ _o
	H	H	X	L	H→L→H	X	Si	Si

Note : CLK = CK + IH

$$D = (A_1 \times A_2) + (B_1 \times B_2)$$

Cell Name	
SDJ	

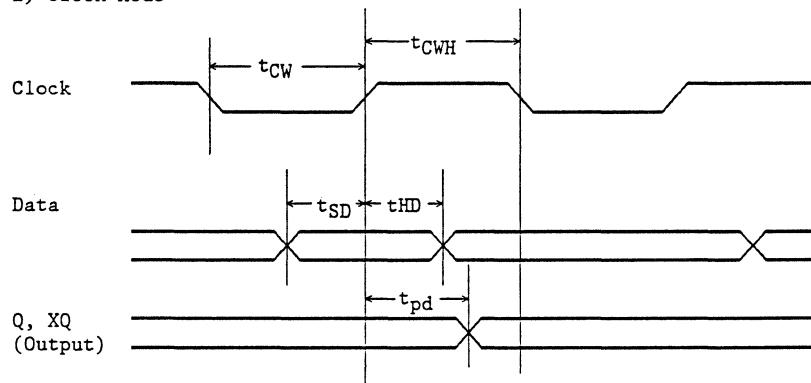
Equivalent Circuit



Cell Name
SDJ

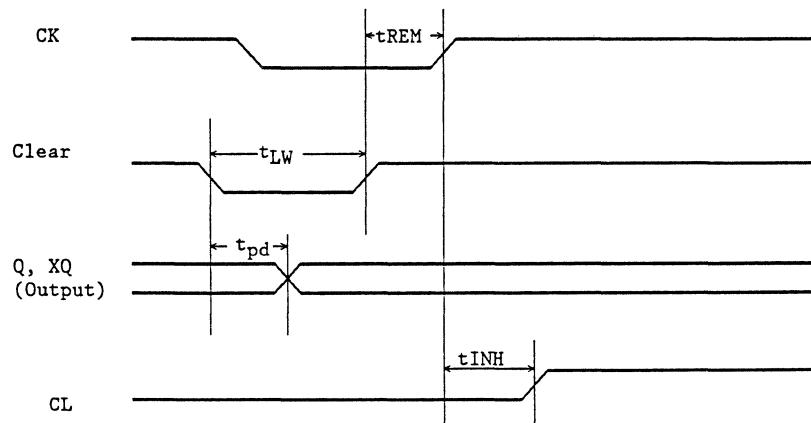
Definitions of Parameters

i) Clock Mode



2

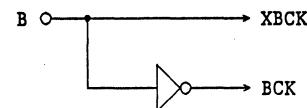
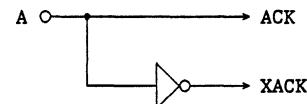
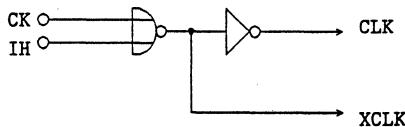
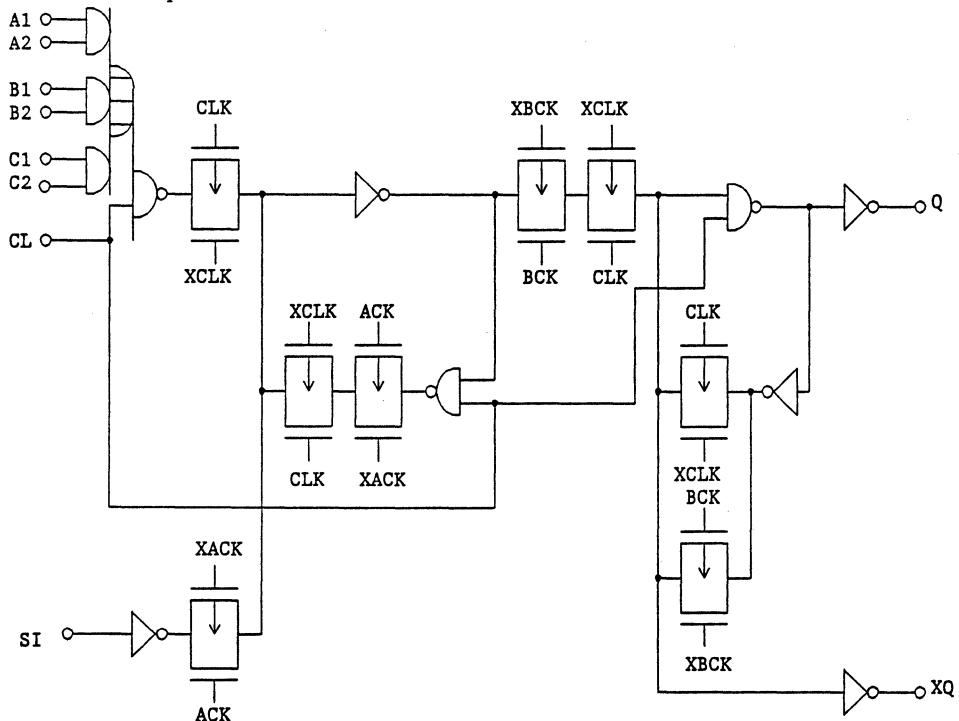
ii) Clear Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version						
Cell Name	Function						Number of BC						
Cell Symbol	Propagation Delay Parameter												
			tup	tdn									
	t0	KCL	t0	KCL	KCL2	CDR2	Path						
A1	3.70	0.08	3.00	0.04	0.08	7	CK, IH → Q						
A2	2.32	0.08	2.16	0.06	0.12	7	CK, IH → XQ						
B1	3.74	0.08	1.02	0.04	0.08	7	CL → Q, XQ						
B2													
C1													
C2													
CK													
IH													
SI													
A													
B													
CL													
			Parameter		Symbol	Typ(ns)*							
	Clock Pulse Width		tCW			5.4							
	Clock Pause Time		tCWH			4.5							
	Data Setup Time		tSD			5.0							
	Data Hold Time		tHD			0.5							
	Clear Pulse Width		tLW			4.5							
	Clear Release Time		tREM			3.0							
	Clear Hold Time		tINH			1.5							
Pin Name	Input Loading Factor (lu)												
A1,A2	1												
B1,B2	1												
C1,C2	1												
CK	1												
IH	1												
CL	3												
SI	1												
A,B	2												
Pin Name	Output Driving Factor (lu)												
Q	36												
XQ	36												
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.													
Function Table													
MODE	INPUT					OUTPUT							
	CLK	CL	D	A	B	SI	Q XQ						
CLEAR	X	L	X	X	X	X	L H						
CLOCK	L→H	H	Di	L	L	X	Di <u>Di</u>						
	H	H	X	L	L	X	Q ₀ XQ ₀						
SCAN	H	H	X	L→H→L	H	Si	Q ₀ XQ ₀						
	H	H	X	L	H→L→H	X	Si <u>Si</u>						
Note : CLK = CK + IH D = (A1 × A2) + (B1 × B2) + (C1 × C2)													
UHB-SDK-E1 Sheet 1/3				Page 11-7									

Cell Name
SDK

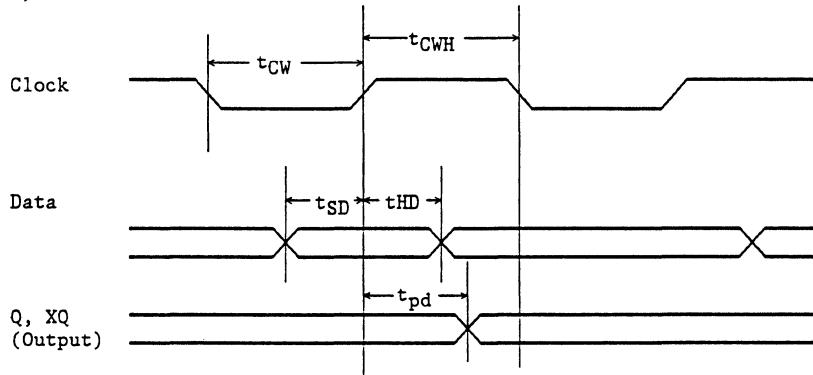
Equivalent Circuit



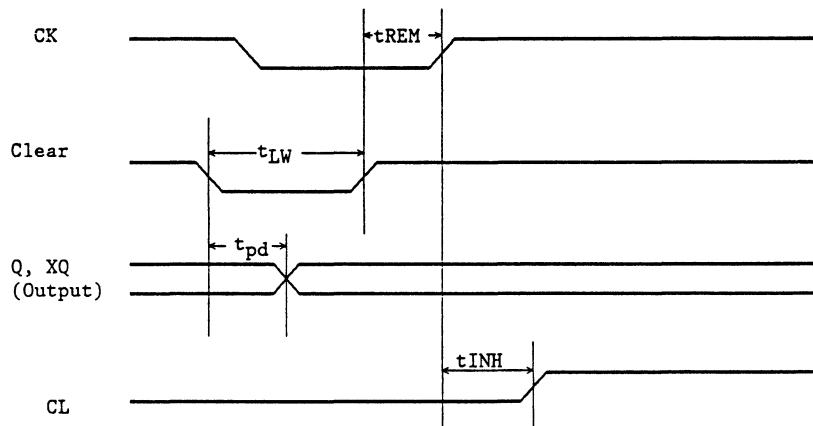
Cell Name
SDK

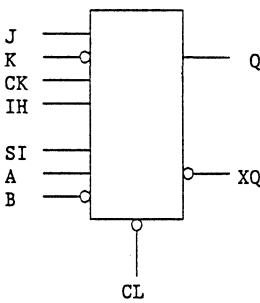
Definitions of Parameters

i) Clock Mode



ii) Clear Mode

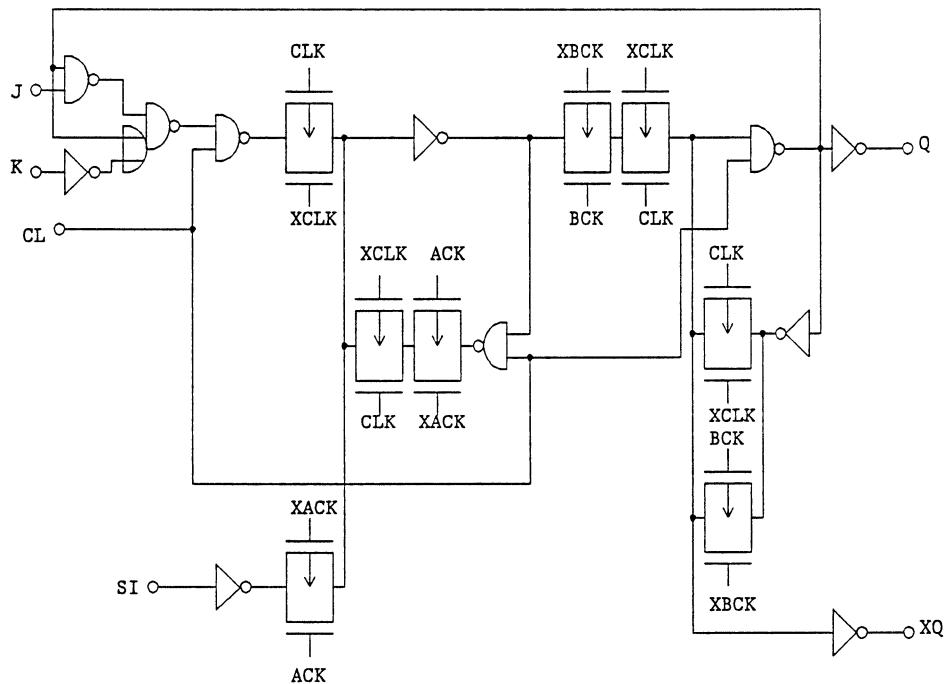


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION								"UHB" Version																														
Cell Name	Function							Number of BC																														
SJH	SCAN J-K FF with Clear & Clock-Inhibit							16																														
Cell Symbol		Propagation Delay Parameter																																				
		<table border="1"> <thead> <tr> <th>tup</th> <th>tDN</th> <th colspan="2"></th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> <th>KCL2</th> <th>CDR2</th> <th>Path</th> </tr> </thead> <tbody> <tr> <td>4.24</td> <td>0.08</td> <td>3.37</td> <td>0.04</td> <td>0.08</td> <td>7</td> <td>CK, IH → Q</td> </tr> <tr> <td>2.36</td> <td>0.08</td> <td>2.16</td> <td>0.06</td> <td>0.12</td> <td>7</td> <td>CK, IH → XQ</td> </tr> <tr> <td>3.76</td> <td>0.08</td> <td>1.39</td> <td>0.04</td> <td>0.08</td> <td>7</td> <td>CL → Q, XQ</td> </tr> </tbody> </table>	tup	tDN			t0	KCL	t0	KCL	KCL2	CDR2	Path	4.24	0.08	3.37	0.04	0.08	7	CK, IH → Q	2.36	0.08	2.16	0.06	0.12	7	CK, IH → XQ	3.76	0.08	1.39	0.04	0.08	7	CL → Q, XQ				
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t0	KCL	t0	KCL	KCL2	CDR2	Path																																
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<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (f<u>lu</u>)</th> </tr> </thead> <tbody> <tr> <td>J,K</td> <td>1</td> </tr> <tr> <td>CK</td> <td>1</td> </tr> <tr> <td>IH</td> <td>1</td> </tr> <tr> <td>CL</td> <td>3</td> </tr> <tr> <td>SI</td> <td>1</td> </tr> <tr> <td>A,B</td> <td>2</td> </tr> </tbody> </table>		Pin Name	Input Loading Factor (f <u>lu</u>)	J,K	1	CK	1	IH	1	CL	3	SI	1	A,B	2																							
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Function Table																																						
MODE	INPUT							OUTPUT																														
	CLK	CL	J	K	A	B	SI	Q	XQ																													
CLEAR	X	L	X	X	X	X	X	L	H																													
CLOCK	L→H	H	L	L	L	L	X	L	H																													
	L→H	H	H	H	L	L	X	H	L																													
	L→H	H	L	H	L	L	X	Q ₀	XQ ₀																													
	L→H	H	H	L	L	L	X	XQ ₀	Q ₀																													
SCAN	H	H	X	X	L	L	X	Q ₀	XQ ₀																													
	H	H	X	X	L	H→L→H	X	Si	Si																													

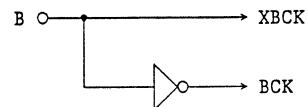
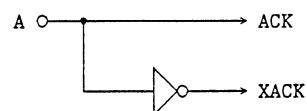
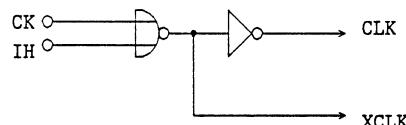
Note : CLK = CK + IH

Cell Name	
SJH	

Equivalent Circuit



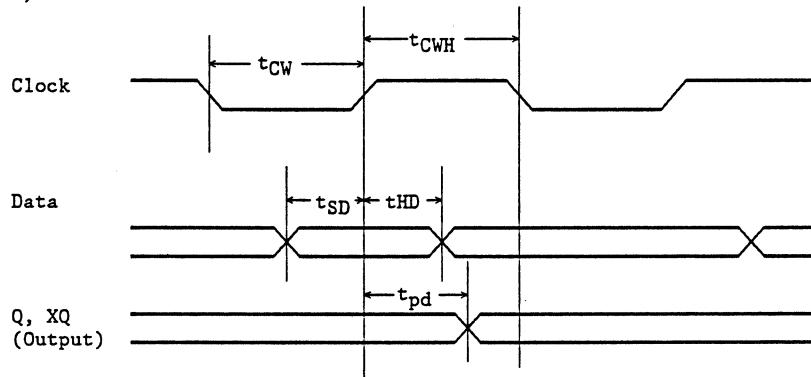
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Cell Name
SJH

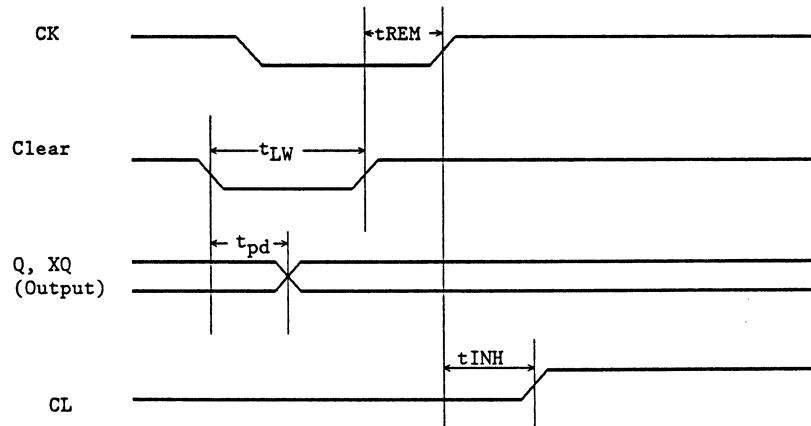
Definitions of Parameters

i) Clock Mode



2

ii) Clear Mode

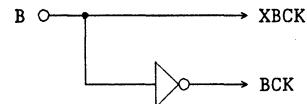
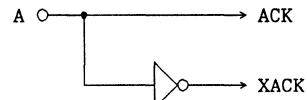
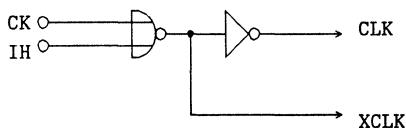
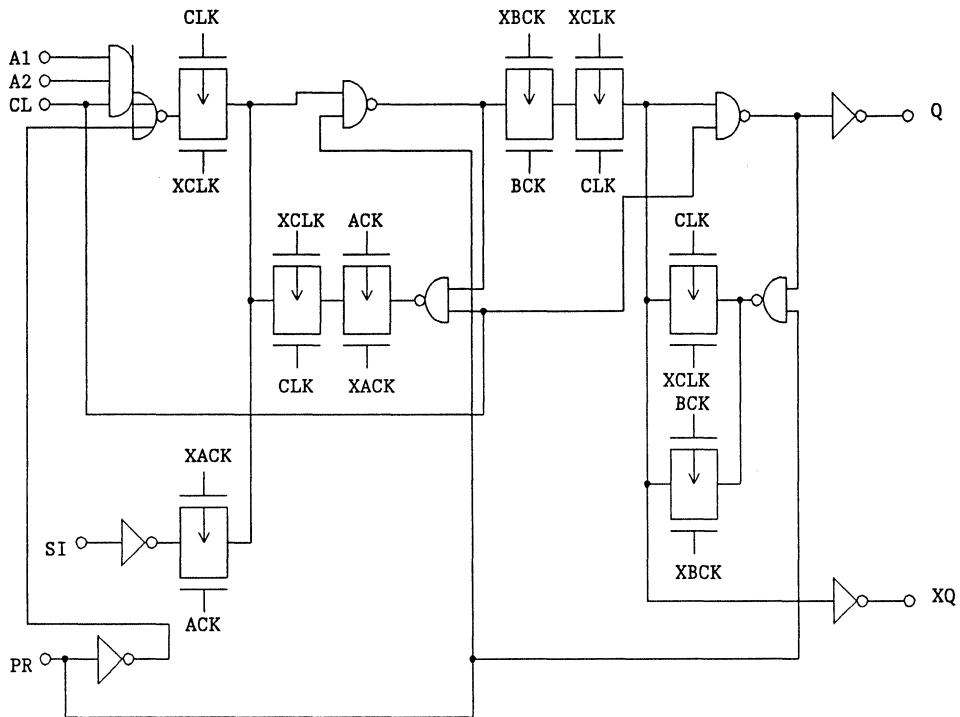


2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version		
Cell Name	Function						Number of BC		
SDD	SCAN 2-input DFF with Clear, Preset & Clock-Inhibit						16		
Cell Symbol	Propagation Delay Parameter								
 PR A1 A2 CK IH SI A B CL	tup		tdn			Path			
	t0	KCL	t0	KCL	KCL2	CDR2			
	3.70	0.08	3.22	0.04	0.08	7	CK, IH → Q		
	2.65	0.08	2.14	0.06	0.12	7	CK, IH → XQ		
	4.50	0.08	1.02	0.04	0.08	7	CL → Q, XQ		
	3.84	0.08	2.35	0.06	0.12	7	PR → Q, XQ		
	Parameter				Symbol	Typ(ns)*			
	Clock Pulse Width				tCW	5.4			
	Clock Pause Time				tCWH	4.5			
	Data Setup Time				tSD	5.4			
Pin Name	Input Loading Factor (ℓu)		Data Hold Time		tHD	1.0			
	A1, A2	1	Clear Pulse Width		tLW	5.0			
	CK	1	Clear Release Time		tREM	3.0			
	IH	1	Clear Hold Time		tINH	1.5			
	CL	3	Preset Pulse Width		tPW	6.8			
Pin Name	PR	3	Preset Release Time		tREM	3.7			
	SI	1	Preset Hold Time		tINH	1.0			
Pin Name	A, B	2							
	Output Driving Factor (ℓu)								
	Q	36							
Pin Name	XQ	36	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
Function Table									
MODE	INPUT						OUTPUT		
	CLK	CL	PR	D	A	B	SI	Q XQ	
CLEAR	X	L	H	X	X	X	X	L H	
PRESET	X	H	L	X	X	X	X	H L	
CLOCK	L→H	H	H	Di	L	L	X	Di \overline{Di}	
	H	H	H	X	L	L	X	Q_0 XQ_0	
SCAN	H	H	H	X	L→H→L	H	Si	Q_0 XQ_0	
	H	H	H	X	L	H→L→H	X	Si \overline{Si}	
CL/PR	X	L	L	X	X	X	X	Prohibited	
Note : CLK = CK + IH D = A1 × A2									

Cell Name
SDD

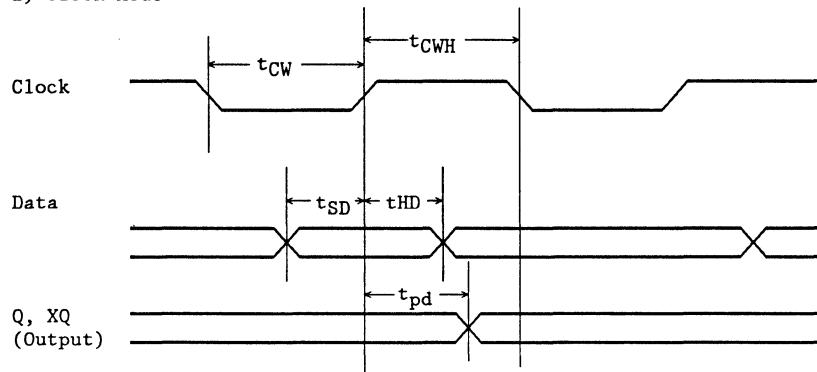
Equivalent Circuit



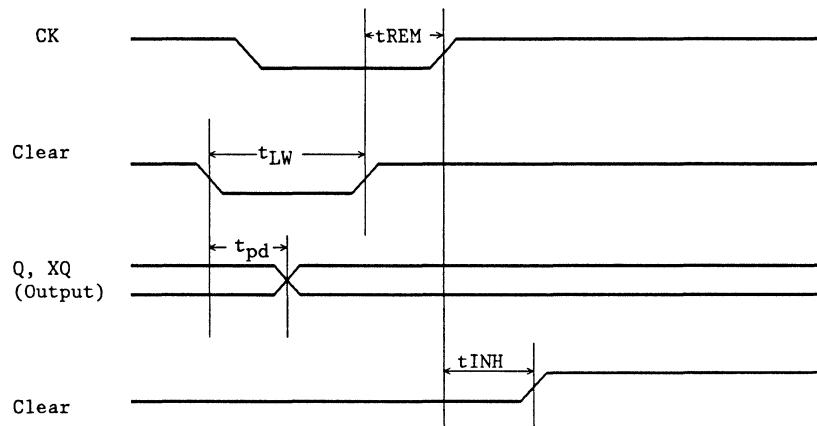
Cell Name
SDD

Definitions of Parameters

i) Clock Mode

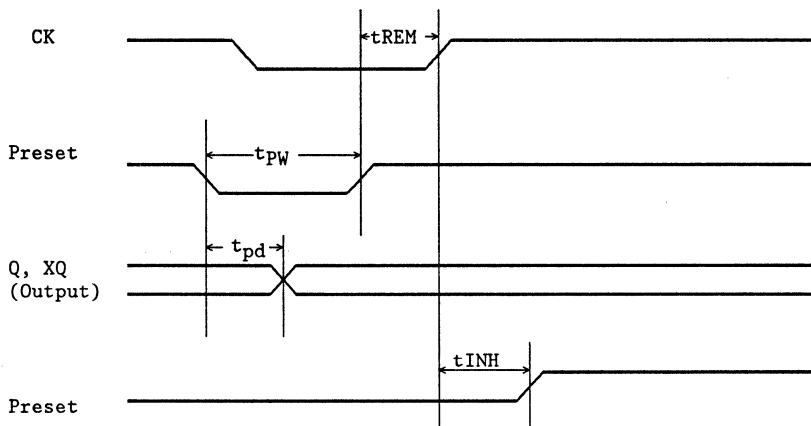


ii) Clear Mode



Cell Name
SDD

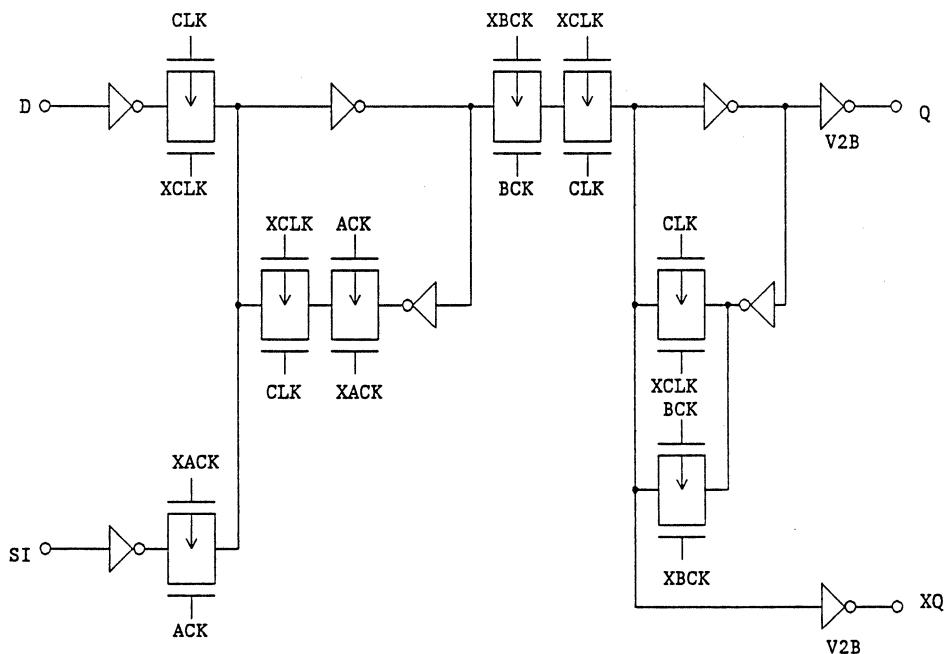
iii) Preset Mode



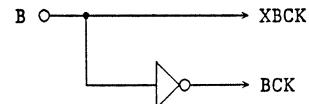
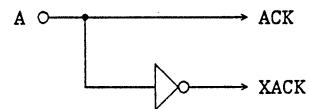
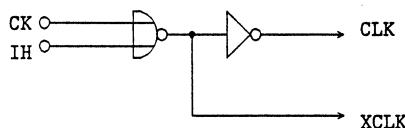
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																											
Cell Name	Function						Number of BC																											
SDA	SCAN 1-input DFF with Clock-Inhibit						12																											
Cell Symbol	Propagation Delay Parameter																																	
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="4">tdn</th><th rowspan="2">Path</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th></tr> </thead> <tbody> <tr> <td>3.18</td><td>0.08</td><td>3.00</td><td>0.04</td><td>0.08</td><td>7</td><td>CK, IH → Q</td></tr> <tr> <td>2.33</td><td>0.08</td><td>2.17</td><td>0.06</td><td>0.12</td><td>7</td><td>CK, IH → XQ</td></tr> </tbody> </table>							tup		tdn				Path	t0	KCL	t0	KCL	KCL2	CDR2	3.18	0.08	3.00	0.04	0.08	7	CK, IH → Q	2.33	0.08	2.17	0.06	0.12	7	CK, IH → XQ
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Data Hold Time	tHD	1.4																																
Pin Name	Input Loading Factor (μ u)																																	
D	1																																	
CK	1																																	
IH	1																																	
SI	1																																	
A, B	2																																	
Pin Name	Output Driving Factor (μ u)																																	
Q	36																																	
XQ	36																																	
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																																		
Function Table																																		
MODE	INPUT					OUTPUT																												
	CLK	D	A	B	SI	Q	XQ																											
CLOCK	L→H	Di	L	L	X	Di	\overline{Di}																											
	H	X	L	L	X	Q_0	XQ_0																											
SCAN	H	X	L→H+L	H	Si	Q_0	XQ_0																											
	H	X	L	H→L+H	X	Si	\overline{Si}																											
Note : CLK = CK + IH																																		

Cell Name	SDA
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Equivalent Circuit



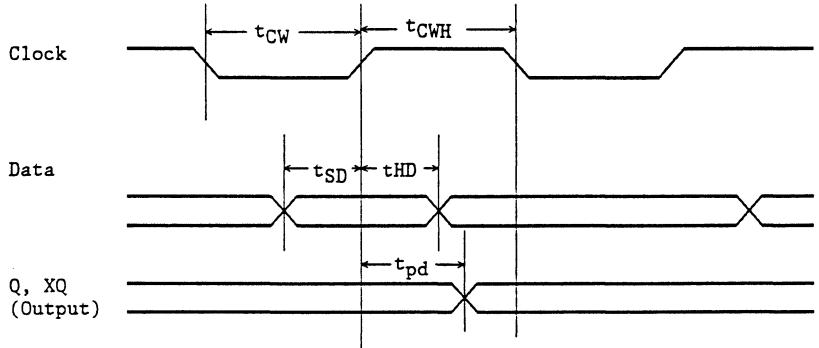
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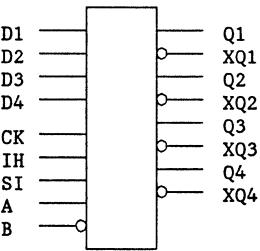


Cell Name
SDA

Definitions of Parameters

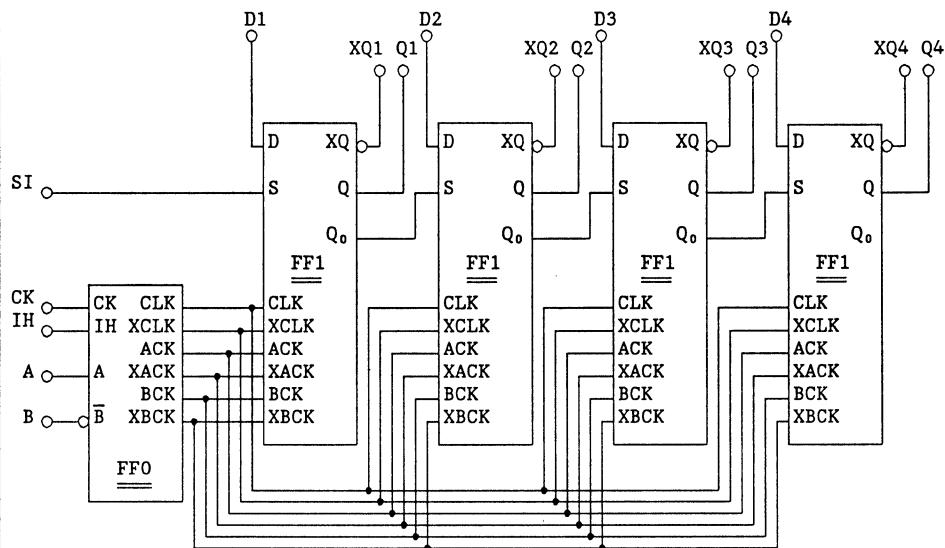
i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																												
Cell Name	Function						Number of BC																												
SDB	SCAN 1-input 4-bit DFF with Clock-Inhibit						42																												
Cell Symbol	Propagation Delay Parameter																																		
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="4">tdn</th><th></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th><th>Path</th></tr> </thead> <tbody> <tr> <td>4.24</td><td>0.08</td><td>3.94</td><td>0.04</td><td>0.08</td><td>7</td><td>CK, IH → Q</td></tr> <tr> <td>3.25</td><td>0.08</td><td>3.32</td><td>0.06</td><td>0.12</td><td>7</td><td>CK, IH → XQ</td></tr> </tbody> </table>						tup		tdn					t0	KCL	t0	KCL	KCL2	CDR2	Path	4.24	0.08	3.94	0.04	0.08	7	CK, IH → Q	3.25	0.08	3.32	0.06	0.12	7	CK, IH → XQ	
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t0	KCL	t0	KCL	KCL2	CDR2	Path																													
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3.25	0.08	3.32	0.06	0.12	7	CK, IH → XQ																													
D1 D2 D3 D4 CK IH SI A B																																			
Pin Name	Input Loading Factor (ℓ_u)																																		
D	1																																		
CK	1																																		
IH	1																																		
SI	1																																		
A, B	2																																		
Pin Name	Output Driving Factor (ℓ_u)																																		
Q	36																																		
XQ	36																																		
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																																			
Function Table																																			
MODE	INPUT					OUTPUT																													
	CLK	D _n	A	B	SI, Q _{n-1}	Q _n	XQ _n																												
CLOCK	L→H	Di	L	L	X	Di	Di																												
	H	X	L	L	X	Q _n	XQ _n																												
SCAN	H	X	L→H+L	H	Si	Q _n	XQ _n																												
	H	X	L	H+L+H	X	Si	Si																												
<small>Note : CLK = CK + IH n = 1 ~ 4</small>																																			

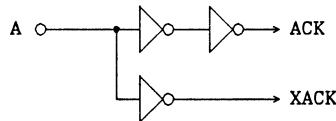
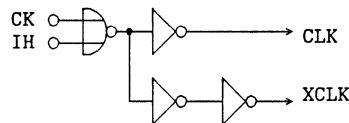
Cell Name
SDB

Equivalent Circuit



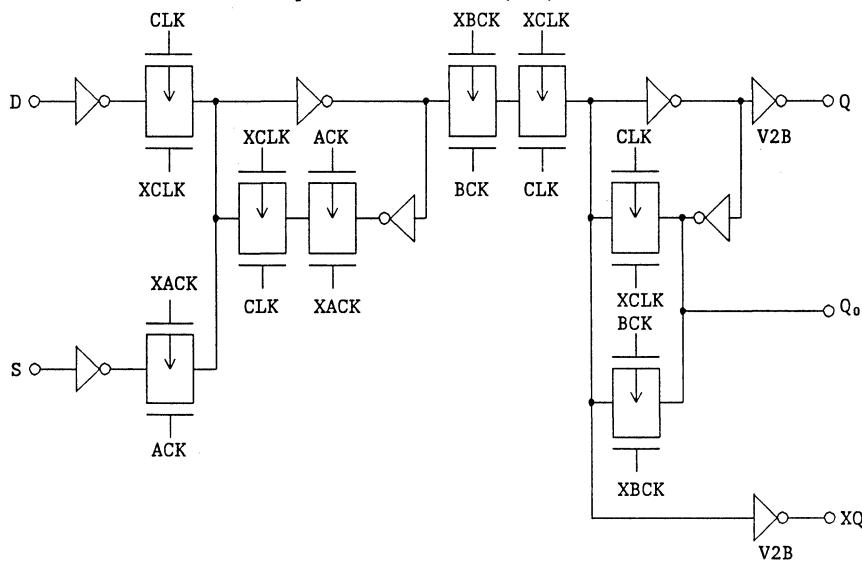
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Equivalent Circuit (FF0)



Cell Name
SDB

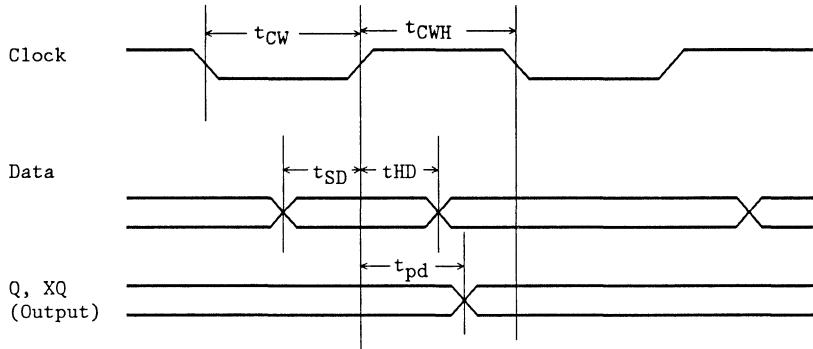
Equivalent Circuit (FF1)



Cell Name
SDB

Definitions of Parameters

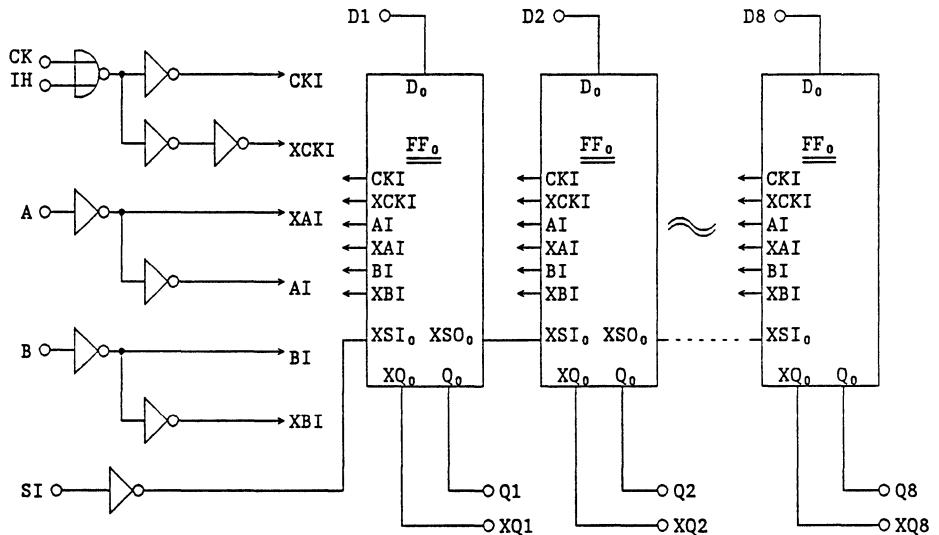
i) Clock Mode



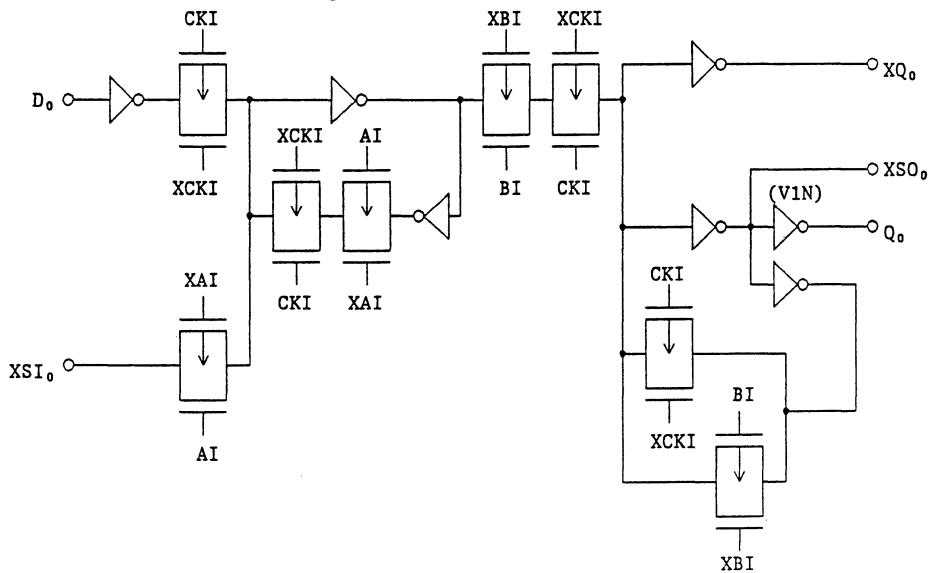
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version																									
Cell Name	Function	Number of BC																									
SHA	SCAN 1-input 8-bit DFF with Clock-Inhibit	68																									
Cell Symbol	Propagation Delay Parameter																										
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="2">tdn</th><th colspan="2"></th> </tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th> </tr> </thead> <tbody> <tr> <td>4.72</td><td>0.16</td><td>4.72</td><td>0.09</td><td>0.10</td><td>4</td> </tr> <tr> <td>4.12</td><td>0.16</td><td>4.00</td><td>0.13</td><td>0.18</td><td>4</td> </tr> </tbody> </table>		tup		tdn				t0	KCL	t0	KCL	KCL2	CDR2	4.72	0.16	4.72	0.09	0.10	4	4.12	0.16	4.00	0.13	0.18	4	Path
tup		tdn																									
t0	KCL	t0	KCL	KCL2	CDR2																						
4.72	0.16	4.72	0.09	0.10	4																						
4.12	0.16	4.00	0.13	0.18	4																						
D1	Q1				CK, IH → Q																						
D2	XQ1				CK, IH → XQ																						
D3	Q2																										
D4	XQ2																										
D5	Q3																										
D6	XQ3																										
D7	Q4																										
D8	XQ4																										
CK	XQ6																										
IH	Q7																										
SI	XQ7																										
A	Q8																										
B	XQ8																										
Parameter		Symbol	Typ(ns)*																								
Clock Pulse Width		tCW	7.2																								
Clock Pause Time		tCWH	5.5																								
Data Setup Time		tSD	1.8																								
Data Hold Time		tHD	3.3																								
Pin Name	Input Loading Factor (Ω_u)																										
D	1																										
CK	1																										
IH	1																										
SI	1																										
A	1																										
B	1																										
Pin Name	Output Driving Factor (Ω_u)																										
Q	18																										
XQ	18																										
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																											

Cell Name	
SHA	

Equivalent Circuit



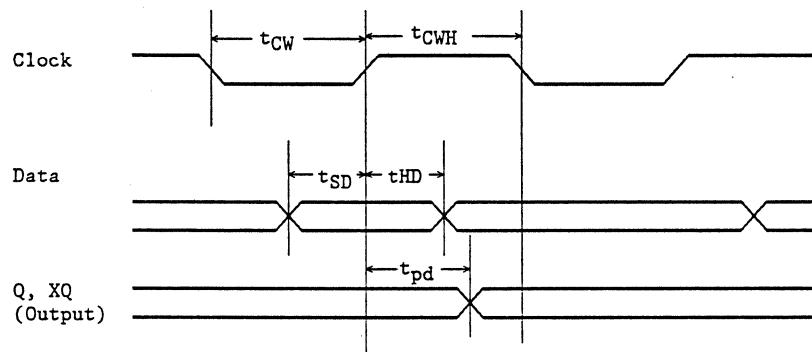
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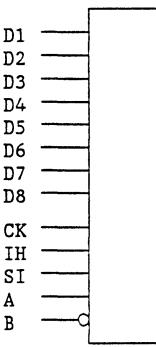
Equivalent Circuit (FF_0)

Cell Name
SHA

Definitions of Parameters

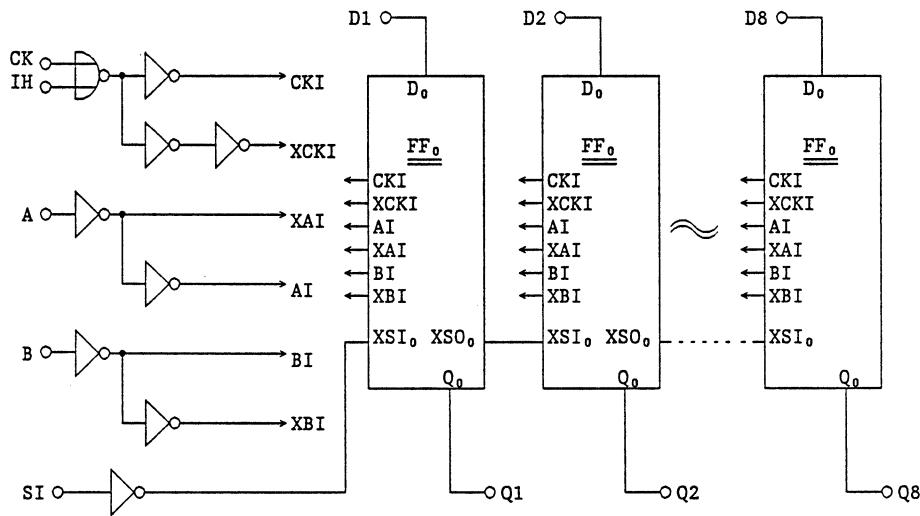
i) Clock Mode



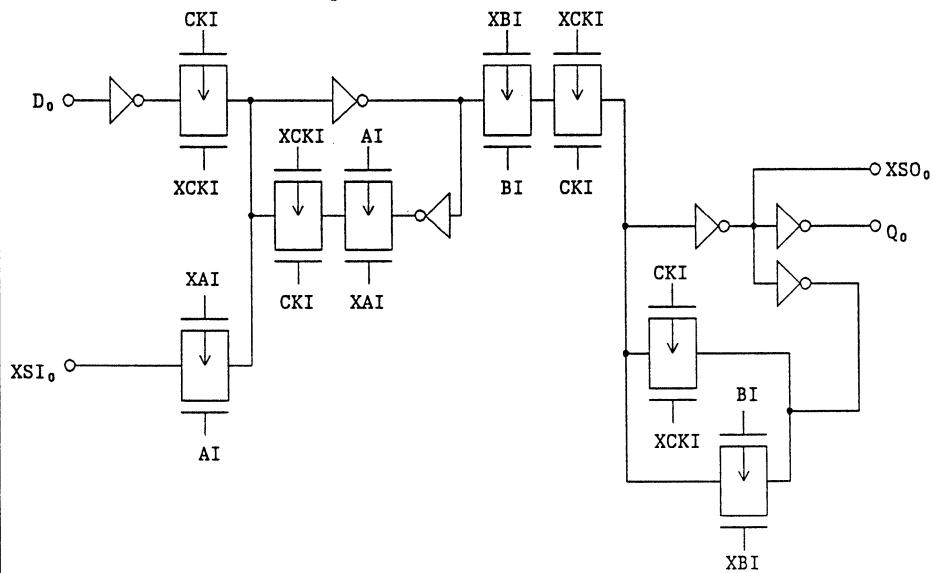
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
Cell Symbol	Propagation Delay Parameter							
		t _{up}		t _{dn}				
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	Path
		4.32	0.16	4.42	0.09	0.10	4	CK, IH → Q
		Parameter			Symbol		Typ(ns)*	
		Clock Pulse Width			t _{CW}		7.2	
		Clock Pause Time			t _{CWH}		5.5	
		Data Setup Time			t _{SD}		1.9	
		Data Hold Time			t _{HD}		3.3	
Pin Name	Input Loading Factor (f <u>)</u>							
D	1							
CK	1							
IH	1							
SI	1							
A	1							
B	1							
Pin Name	Output Driving Factor (f <u>)</u>							
Q	18				* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			

Cell Name	
SHB	

Equivalent Circuit



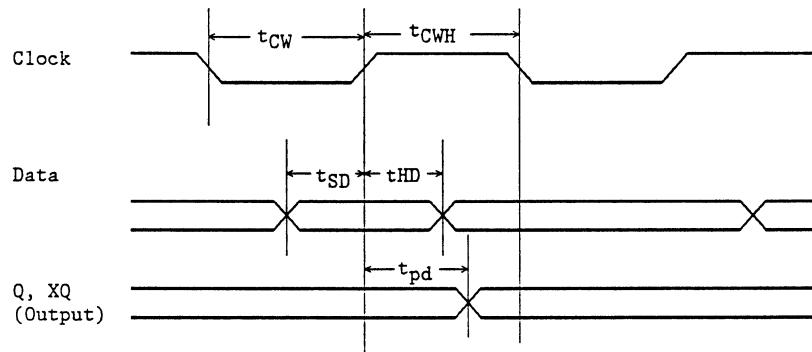
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Equivalent Circuit (FF₀)

Cell Name
SHB

Definitions of Parameters

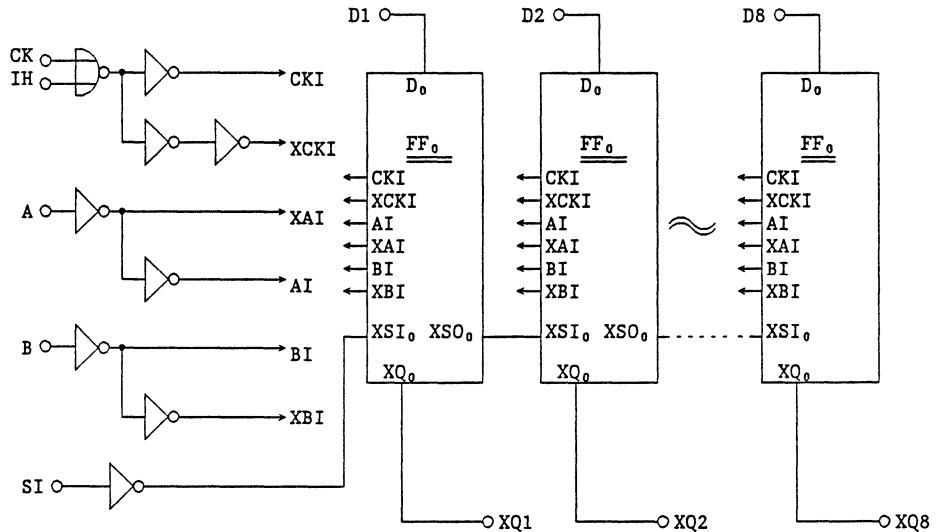
i) Clock Mode



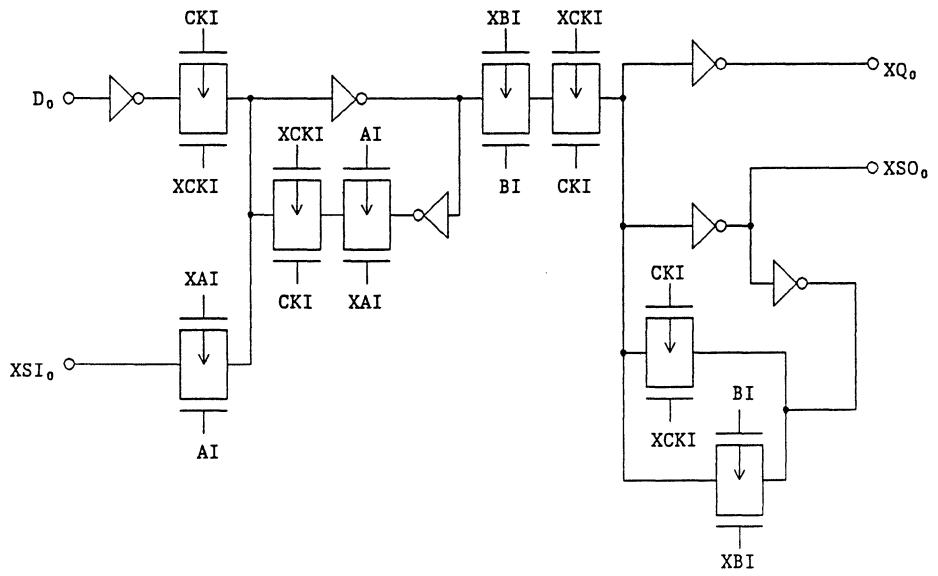
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version																		
Cell Name	Function	Number of BC																		
SHC	SCAN 1-input 8-bit DFF with Clock-Inhibit & XQ Output	62																		
Cell Symbol	Propagation Delay Parameter																			
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="3">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th></tr> </thead> <tbody> <tr> <td>4.18</td><td>0.16</td><td>4.10</td><td>0.13</td><td>0.18</td><td>4</td></tr> </tbody> </table>		tup		tdn			t0	KCL	t0	KCL	KCL2	CDR2	4.18	0.16	4.10	0.13	0.18	4	Path CK, IH → XQ
tup		tdn																		
t0	KCL	t0	KCL	KCL2	CDR2															
4.18	0.16	4.10	0.13	0.18	4															
D1	XQ1																			
D2	XQ2																			
D3	XQ3																			
D4	XQ4																			
D5	XQ5																			
D6	XQ6																			
D7	XQ7																			
D8	XQ8																			
CK																				
IH																				
SI																				
A																				
B																				
Parameter		Symbol	Typ(ns)*																	
Clock Pulse Width		tCW	7.2																	
Clock Pause Time		tCWH	5.5																	
Data Setup Time		tSD	1.9																	
Data Hold Time		tHD	3.3																	
Pin Name	Input Loading Factor (μ u)																			
D	1																			
CK	1																			
IH	1																			
SI	1																			
A	1																			
B	1																			
Pin Name	Output Driving Factor (μ u)																			
XQ	18	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																		
UHB-SHC-E1 Sheet 1/3				Page 11-30																

Cell Name	
SHC	

Equivalent Circuit



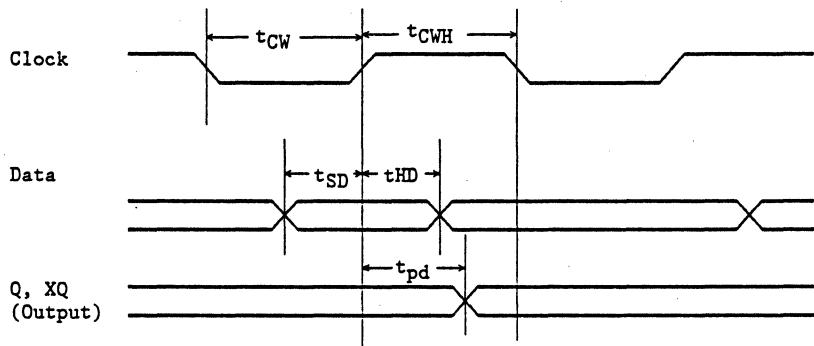
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Equivalent Circuit (FF_0)

Cell Name
SHC

Definitions of Parameters

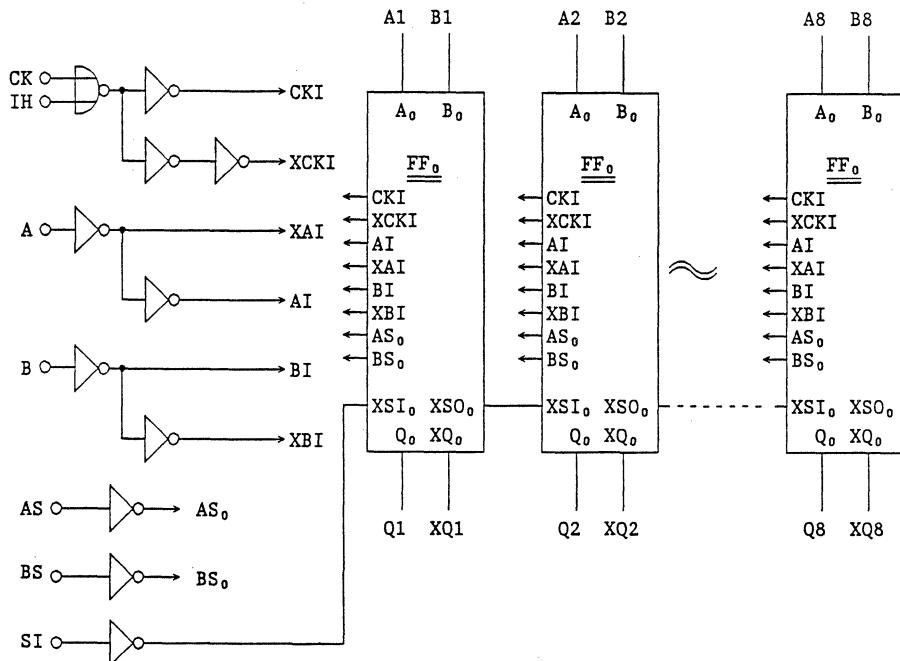
i) Clock Mode



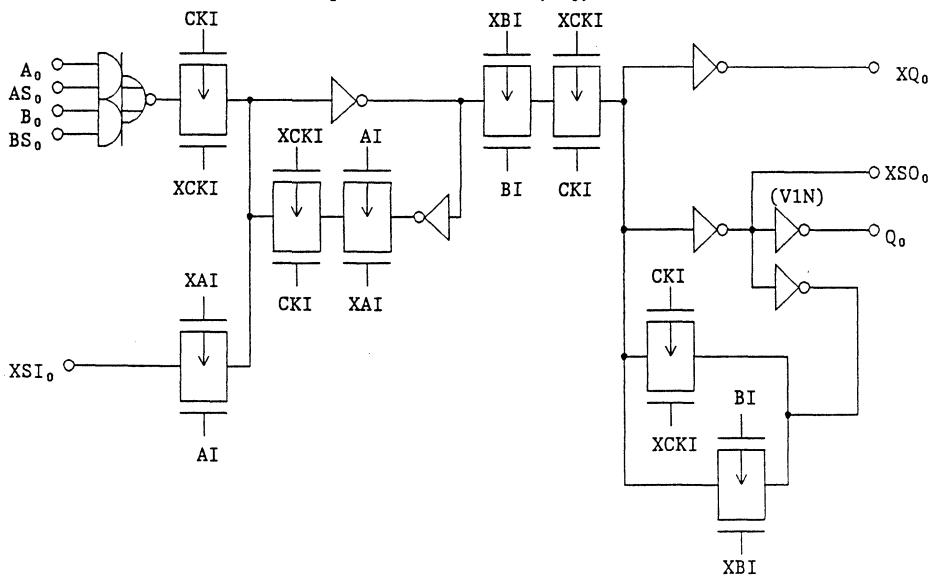
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version			
Cell Name	Function	Number of BC					
SHJ	SCAN 8-bit DFF with Clock-Inhibit & 2-to-1 Data Multiplexer						
Cell Symbol	Propagation Delay Parameter						
	tup	tdn					
	t0	KCL	t0	KCL	KCL2		
A1	4.82	0.16	4.84	0.08	0.12	4	CK, IH → Q
B1	4.12	0.16	4.00	0.11	0.20	4	CK, IH → XQ
A2							
B2							
A3							
B3							
A4							
B4							
A5							
B5							
A6							
B6							
A7							
B7							
A8							
B8							
AS							
BS							
CK							
IH							
SI							
A							
B							
Parameter				Symbol	Typ(ns)*		
Clock Pulse Width				tCW	7.2		
Clock Pause Time				tCWH	5.5		
Data Setup Time				tSD	3.0		
Data Hold Time				tHD	3.1		
Pin Name	Input Loading Factor (μ u)						
An, Bn (n=1~8)	1						
AS, BS	1						
CK	1						
IH	1						
SI	1						
A, B	1						
Pin Name	Output Driving Factor (μ u)						
Q	18						
XQ	18						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							
UHB-SHJ-E2	Sheet 1/3					Page 11-33	

Cell Name	
SHJ	

Equivalent Circuit



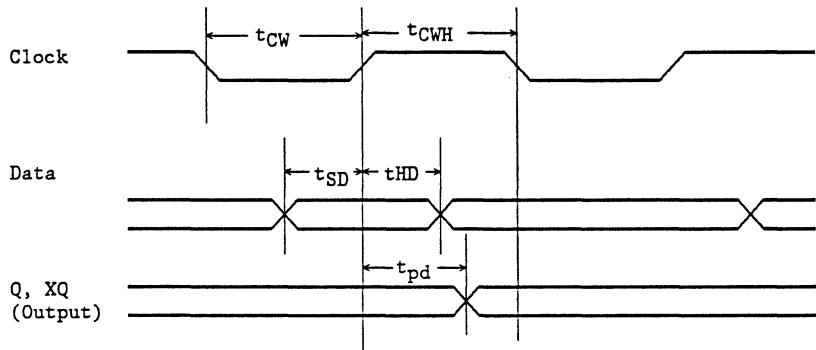
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Equivalent Circuit (\overline{FF}_0)

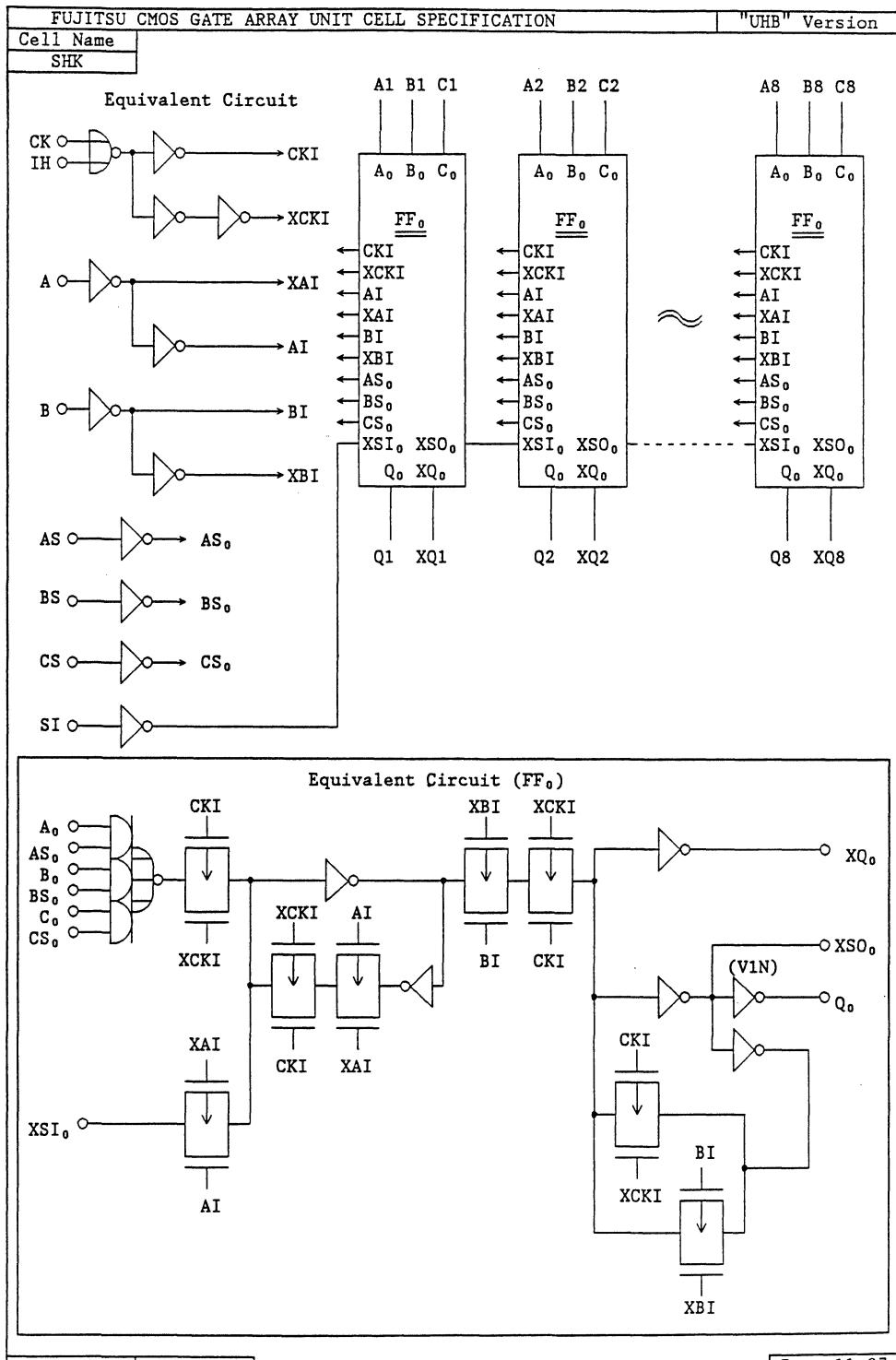
Cell Name
SHJ

Definitions of Parameters

i) Clock Mode



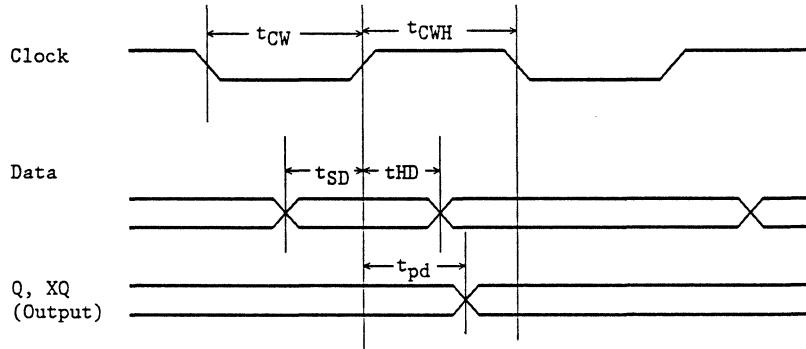
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version			
Cell Name	Function	Number of BC					
SHK	SCAN 8-bit DFF with Clock-Inhibit & 3-to-1 Data Multiplexer						
Cell Symbol	Propagation Delay Parameter						
			tup		tdn		
	t0	KCL	t0	KCL	KCL2	CDR2	Path
A1	4.64	0.16	4.60	0.09	0.10	4	CK,IH → Q
B1	4.08	0.16	4.00	0.13	0.18	4	CK,IH → XQ
C1							
A2							
B2							
C2							
A3							
B3							
C3							
A4							
B4							
C4							
A5							
B5							
C5							
A6							
B6							
C6							
A7							
B7							
C7							
A8							
B8							
C8							
AS							
BS							
CS							
CK							
IH							
SI							
A							
B							
Parameter						Symbol	Typ(ns)*
Clock Pulse Width						tCW	7.2
Clock Pause Time						tCWH	5.5
Data Setup Time						tSD	3.8
Data Hold Time						tHD	2.9
Pin Name	Input Loading Factor (l <u>)</u>						
An,Bn,Cn (n=1~8)	1						
AS,BS,CS	1						
CK	1						
IH	1						
SI	1						
A,B	1						
Pin Name	Output Driving Factor (l <u>)</u>						
Q	18						
XQ	18						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							



Cell Name
SHK

Definitions of Parameters

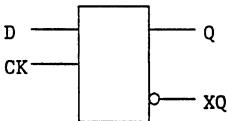
i) Clock Mode



Non Scan Flip-Flop Family

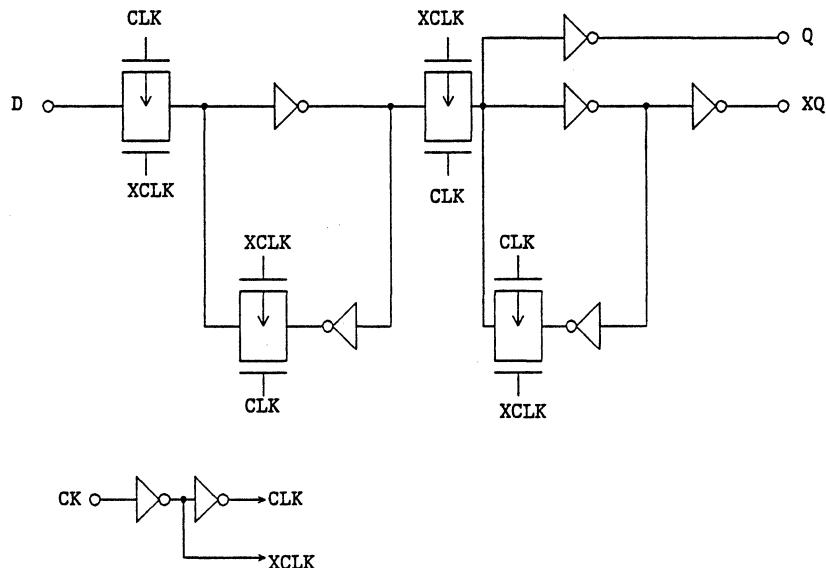
Page	Unit Cell Name	Function	Basic Cells
2-159	FDM	Non-Scan D FF	6
2-161	FDN	Non-Scan D FF with Set	7
2-163	FDO	Non-Scan D FF with Reset	7
2-165	FDP	Non-Scan D FF with Set and Reset	8
2-168	FDQ	Non-Scan D FF	21
2-170	FDR	Non-Scan D FF with Clear	26
2-173	FDS	Non-Scan D FF	20
2-175	FD2	Non-Scan Power D FF	7
2-177	FD3	Non-Scan Power D FF with Preset	8
2-179	FD4	Non-Scan Power D FF with Clear and Preset	9
2-181	FD5	Non-Scan Power D FF with Clear	8
2-183	FJD	Non-Scan Positive Edge Clocked Power J-K FF with Clear	12

2

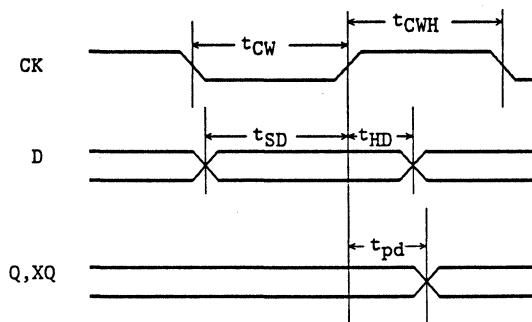
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version						
Cell Name	Function					Number of BC						
FDM	Non-SCAN DFF					6						
Cell Symbol		Propagation Delay Parameter										
		t _{up}	t _{dn}									
		t ₀	KCL	t ₀	KCL	KCL2						
		1.75	0.16	1.80	0.09	CDR2						
		2.16	0.16	2.36	0.09							
						Path						
						CK → Q						
						CK → XQ						
Parameter						Symbol						
Clock Pulse Width						t _{CW}						
Clock Pause Time						t _{CWH}						
Data Setup Time						t _{SD}						
Data Hold Time						t _{HD}						
						Typ(ns)*						
						4.0						
						4.0						
						2.1						
						1.5						
Pin Name		Input Loading Factor (λ_u)										
D		2										
CK		1										
Pin Name		Output Driving Factor (λ_u)										
Q		18										
XQ		18										
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.												
Function Table												
<table border="1"> <thead> <tr> <th>Inputs</th><th>Outputs</th></tr> <tr> <th>D CK</th><th>Q XQ</th></tr> </thead> <tbody> <tr> <td>H ↑ L ↑</td><td>H L L H</td></tr> </tbody> </table>							Inputs	Outputs	D CK	Q XQ	H ↑ L ↑	H L L H
Inputs	Outputs											
D CK	Q XQ											
H ↑ L ↑	H L L H											

Cell Name
FDM

Equivalent Circuit



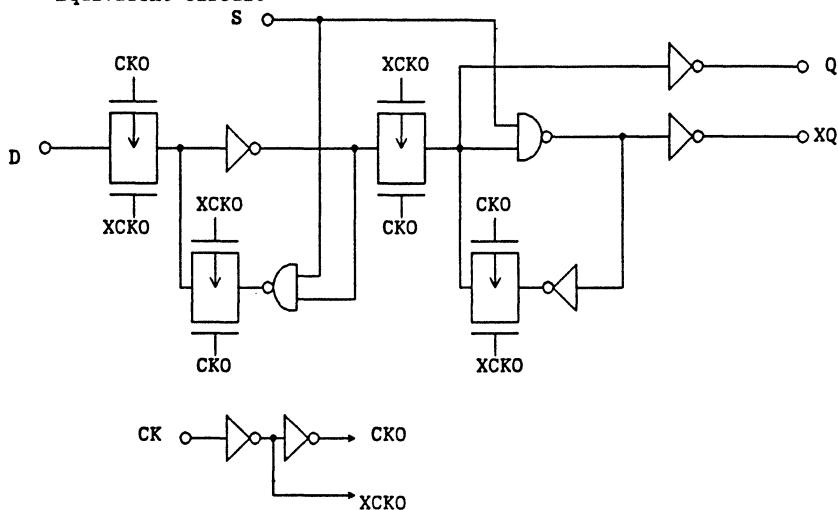
Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																														
Cell Name	Function					Number of BC																														
FDN	Non-SCAN DFF with SET					7																														
Cell Symbol		Propagation Delay Parameter																																		
		t _{up}	t _{dn}			Path																														
		t ₀	KCL	t ₀	KCL	KCL2	CDR2																													
		1.80	0.16	1.75	0.09	0.12	4																													
		2.46	0.16	2.42	0.08		CK → Q																													
		2.24	0.16	1.07	0.08		CK → XQ																													
						S → Q, XQ																														
Parameter						Symbol																														
Clock Pulse Width						t _{CW}																														
Clock Pause Time						t _{CWH}																														
Data Setup Time						t _{SD}																														
Data Hold Time						t _{HD}																														
Pin Name	Input Loading Factor (ℓu)		Set Pulse Width			t _{SW}																														
	D	2	Set Release Time (S)			t _{TREM}																														
	S	2	Set Hold Time			t _{TINH}																														
Pin Name	Output Driving Factor (ℓu)																																			
	Q	18																																		
	XQ	18																																		
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																																				
Function Table																																				
<table border="1"> <thead> <tr> <th colspan="3">Inputs</th><th colspan="3">Outputs</th></tr> <tr> <th>S</th><th>D</th><th>CK</th><th>Q</th><th>XQ</th><th></th></tr> </thead> <tbody> <tr> <td>L</td><td>X</td><td>X</td><td>H</td><td>L</td><td></td></tr> <tr> <td>H</td><td>H</td><td>↑</td><td>H</td><td>L</td><td></td></tr> <tr> <td>H</td><td>L</td><td>↑</td><td>L</td><td>H</td><td></td></tr> </tbody> </table>							Inputs			Outputs			S	D	CK	Q	XQ		L	X	X	H	L		H	H	↑	H	L		H	L	↑	L	H	
Inputs			Outputs																																	
S	D	CK	Q	XQ																																
L	X	X	H	L																																
H	H	↑	H	L																																
H	L	↑	L	H																																
UHB-FDN-E3 Sheet 1/2																																				
Page 12-3																																				

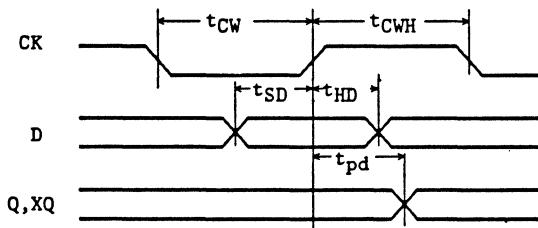
Cell Name
FDN

Equivalent Circuit

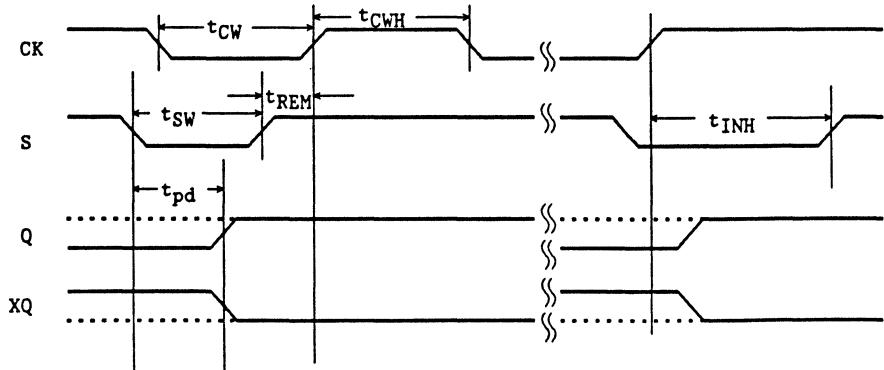


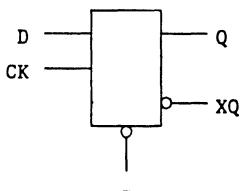
Definition of Parameters

- 2) 1) t_{CW} , t_{CWH} , t_{SD} , t_{HD} and t_{pd} ($CK \rightarrow Q, XQ$)



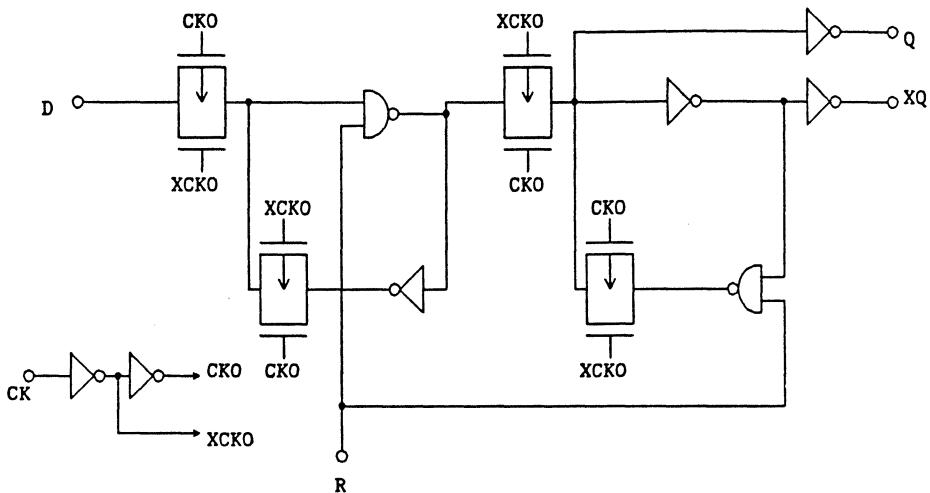
- 2) t_{SW} , t_{REM} , t_{INH} and t_{pd} ($S \rightarrow Q, XQ$)



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																												
Cell Name	Function					Number of BC																												
FDO	Non-SCAN DFF with RESET					7																												
Cell Symbol		Propagation Delay Parameter																																
		tup	tdn			Path																												
		t0	KCL	t0	KCL	KCL2	CDR2																											
		1.93	0.16	1.78	0.10			CK → Q																										
		2.16	0.16	2.58	0.09			CK → XQ																										
		2.00	0.16	1.64	0.10			R → Q, XQ																										
Parameter						Symbol	Typ(ns)*																											
Clock Pulse Width						tCW	4.0																											
Clock Pause Time						tCWH	4.0																											
Data Setup Time						tSD	2.1																											
Data Hold Time						tHD	1.5																											
Pin Name		Input Loading Factor (ℓu)					Reset Pulse Width	tRW	4.0																									
D		2					Reset Release Time (R)	tREM	0.9																									
R		2					Reset Hold Time	tINH	3.3																									
CK		1																																
Pin Name		Output Driving Factor (ℓu)																																
Q		18																																
XQ		18																																
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																																		
Function Table																																		
<table border="1"> <thead> <tr> <th colspan="3">Inputs</th> <th colspan="2">Outputs</th> </tr> <tr> <th>R</th> <th>D</th> <th>CK</th> <th>Q</th> <th>XQ</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>X</td> <td>X</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>↑</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>↑</td> <td>L</td> <td>H</td> </tr> </tbody> </table>		Inputs			Outputs		R	D	CK	Q	XQ	L	X	X	L	H	H	H	↑	H	L	H	L	↑	L	H								
Inputs			Outputs																															
R	D	CK	Q	XQ																														
L	X	X	L	H																														
H	H	↑	H	L																														
H	L	↑	L	H																														

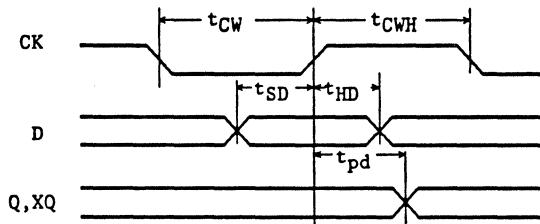
Cell Name	
FDO	

Equivalent Circuit

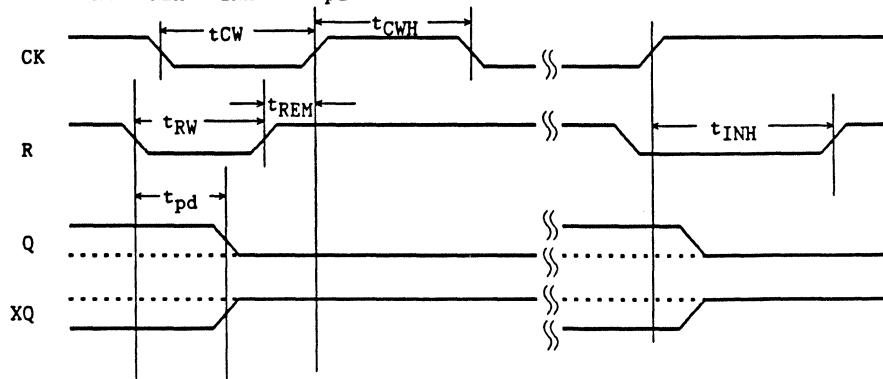


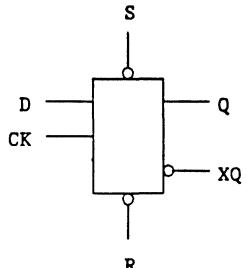
Definition of Parameters

- 2) 1) t_{CW} , t_{CWH} , t_{SD} , t_{HD} and t_{pd} ($CK \rightarrow Q, XQ$)



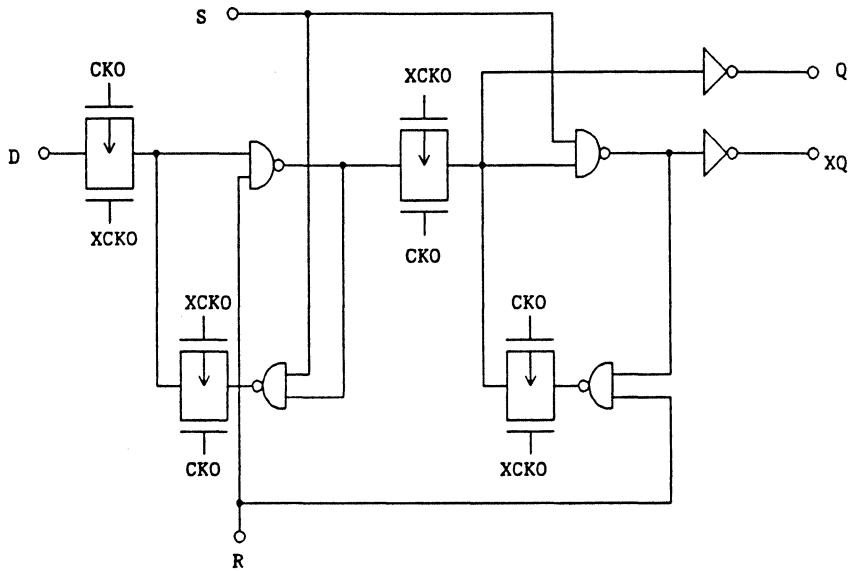
- 2) t_{RW} , t_{REM} , t_{INH} and t_{pd} ($R \rightarrow Q, XQ$)



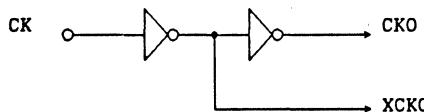
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version														
Cell Name	Function					Number of BC														
FDP	Non-SCAN DFF with Set and Reset					8														
Cell Symbol	Propagation Delay Parameter																			
	tup	tdn																		
	t0	KCL	t0	KCL	KCL2	CDR2	Path													
	1.96	0.16	1.76	0.10			CK → Q													
	2.45	0.16	2.50	0.09			CK → XQ													
	2.24	0.16	1.59	0.10			R → Q, XQ													
	2.54	0.16	1.01	0.09			S → Q, XQ													
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Parameter</th> <th>Symbol</th> <th>Typ(ns)*</th> </tr> </thead> <tbody> <tr> <td>Clock Pulse Width</td> <td>tCW</td> <td>4.0</td> </tr> <tr> <td>Clock Pause Time</td> <td>tCWH</td> <td>4.0</td> </tr> <tr> <td>Data Setup Time</td> <td>tSD</td> <td>2.1</td> </tr> <tr> <td>Data Hold Time</td> <td>tHD</td> <td>1.5</td> </tr> </tbody> </table>	Parameter	Symbol	Typ(ns)*	Clock Pulse Width	tCW	4.0	Clock Pause Time	tCWH	4.0	Data Setup Time	tSD	2.1	Data Hold Time	tHD	1.5					
Parameter	Symbol	Typ(ns)*																		
Clock Pulse Width	tCW	4.0																		
Clock Pause Time	tCWH	4.0																		
Data Setup Time	tSD	2.1																		
Data Hold Time	tHD	1.5																		
Pin Name	Input Loading Factor (λ_u)	Set Pulse Width	tSW	4.0																
		Set Release Time (S)	tREM	0.3																
		Set Hold Time	tINH	3.8																
		Reset Pulse Width	tRW	4.0																
		Reset Release Time (R)	tREM	0.9																
		Reset Hold Time	tINH	3.3																
Pin Name	Output Driving Factor (λ_u)																			
Q XQ	18 18																			
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																				
Function Table																				
Inputs			Outputs																	
S	R	D	CK	Q	XQ															
H	L	X	X	L	H															
L	H	X	X	H	L															
L	L	X	X	Inhibited																
H	H	H	↑	H	L															
H	H	L	↑	L	H															

Cell Name
FDP

Equivalent Circuit



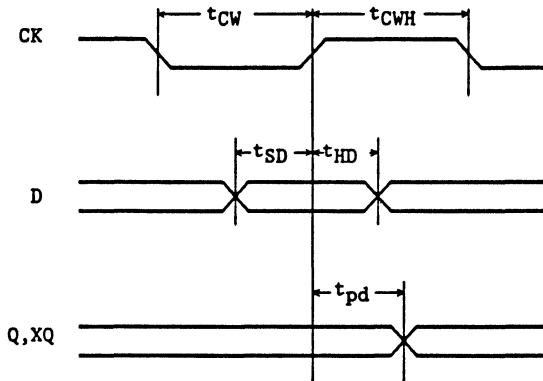
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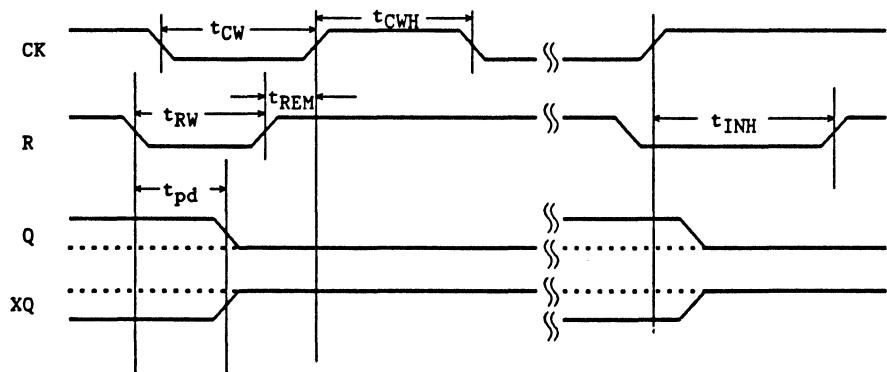
Cell Name	
FDP	

Definition of Parameters

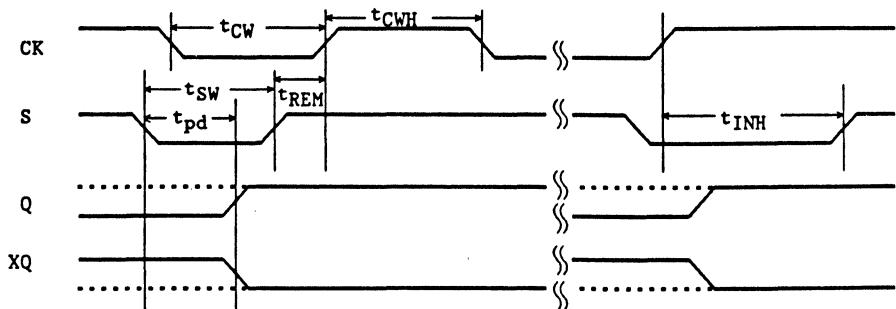
- 1)
- t_{CW}
- ,
- t_{CWH}
- ,
- t_{SD}
- ,
- t_{HD}
- and
- t_{pd}
- (
- $CK \rightarrow Q, XQ$
-)

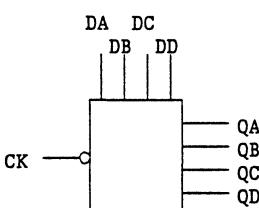


- 2)
- t_{RW}
- ,
- t_{REM}
- ,
- t_{INH}
- and
- t_{pd}
- (
- $R \rightarrow Q, XQ$
-)



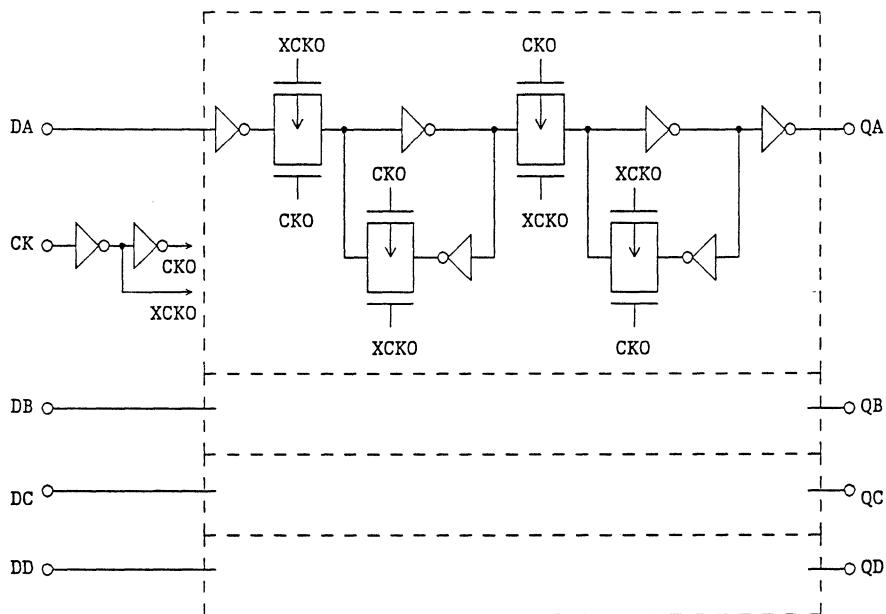
- 3)
- t_{SW}
- ,
- t_{REM}
- ,
- t_{INH}
- and
- t_{pd}
- (
- $S \rightarrow Q, XQ$
-)



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version											
Cell Name	Function				Number of BC											
FDQ	Non-SCAN 4-bit DFF				21											
Cell Symbol		Propagation Delay Parameter														
		t _{up}	t _{dn}													
		t ₀	KCL	t ₀	KCL											
		3.37	0.16	2.74	0.08											
			KCL2		CDR2											
					Path											
					CK → Q											
		Parameter			Symbol											
		Clock Pulse Width			t _{CW}											
		Clock Pause Time			t _{CWL}											
		Data Setup Time			t _{SD}											
		Data Hold Time			t _{HD}											
					Typ(ns)*											
					4.0											
					4.0											
					1.1											
					2.8											
Pin Name		Input Loading Factor (f _{lu})														
D	CK	1														
		1														
Pin Name		Output Driving Factor (f _{lu})														
Q		18														
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																
Function Table																
<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> <tr> <th>CK</th><th>D</th><th>Q</th></tr> </thead> <tbody> <tr> <td>↓ H</td><td>H</td><td></td></tr> <tr> <td>↓ L</td><td>L</td><td></td></tr> </tbody> </table>						Input	Output	CK	D	Q	↓ H	H		↓ L	L	
Input	Output															
CK	D	Q														
↓ H	H															
↓ L	L															
UHB-FDQ-E3 Sheet 1/2																
Page 12-10																

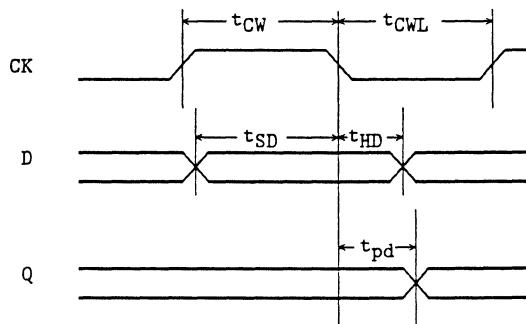
Cell Name	
FDQ	

Equivalent Circuit



2

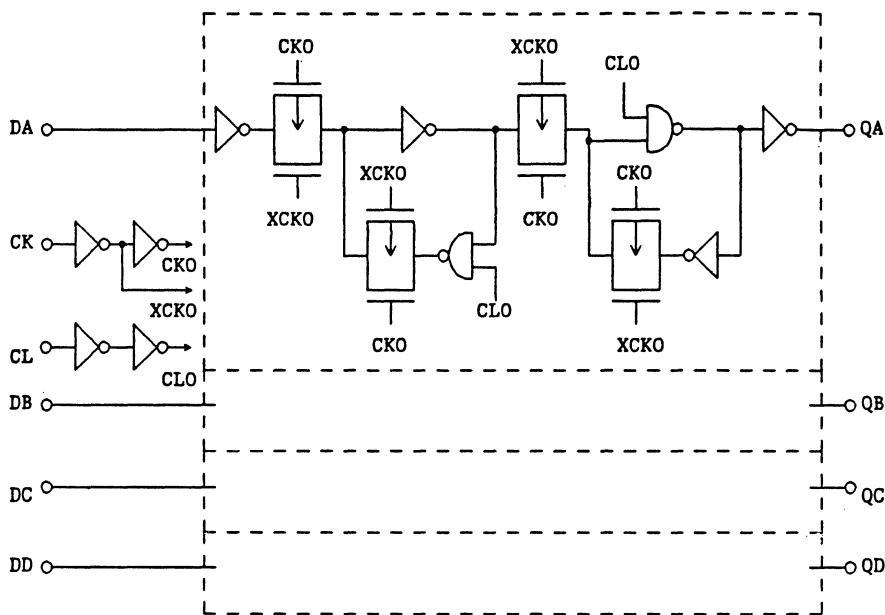
Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version						
Cell Name	Function					Number of BC						
FDR	Non-SCAN 4-bit DFF with CLEAR					26						
Cell Symbol	Propagation Delay Parameter											
	tup		tdn									
	t0	KCL	t0	KCL	KCL2	CDR2						
	2.64	0.16	3.62	0.08								
	-	-	2.18	0.08								
						Path						
						CK → Q						
						CL → Q						
Parameter						Symbol						
Clock Pulse Width						tCW						
4.0												
Clock Pause Time						tCWH						
4.0												
Data Setup Time						tSD						
1.1												
Data Hold Time						tHD						
2.8												
Pin Name	Input Loading Factor (ℓu)		Clear Pulse Width		tLW							
	D		1		4.0							
	CK		1		tREM							
Pin Name	Output Driving Factor (ℓu)		Clear Release Time		1.5							
	CL		1		tINH							
			Clear Hold Time		4.5							
Pin Name	Q		18									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.												
Function Table												
Inputs			Output									
CK	D	CL	Q									
X	X	L	L									
↑	L	H	L									
↑	H	H	H									

Cell Name
FDR

Equivalent Circuit

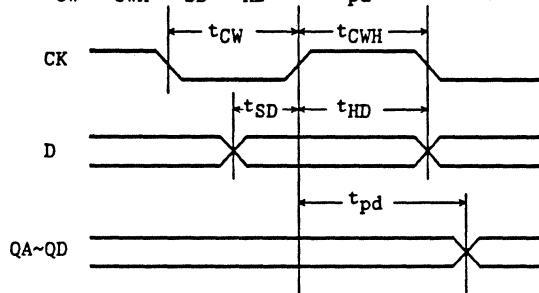


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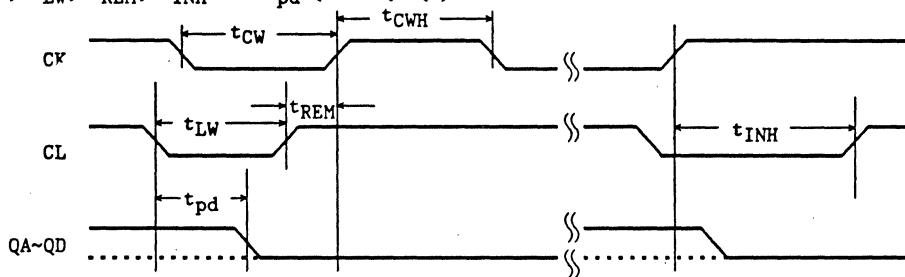
Cell Name	
FDR	

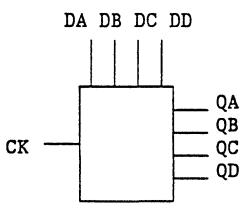
Definition of Parameters

- 1)
- t_{CW}
- ,
- t_{CWH}
- ,
- t_{SD}
- ,
- t_{HD}
- , and
- t_{pd}
- (CK→QA~QD)



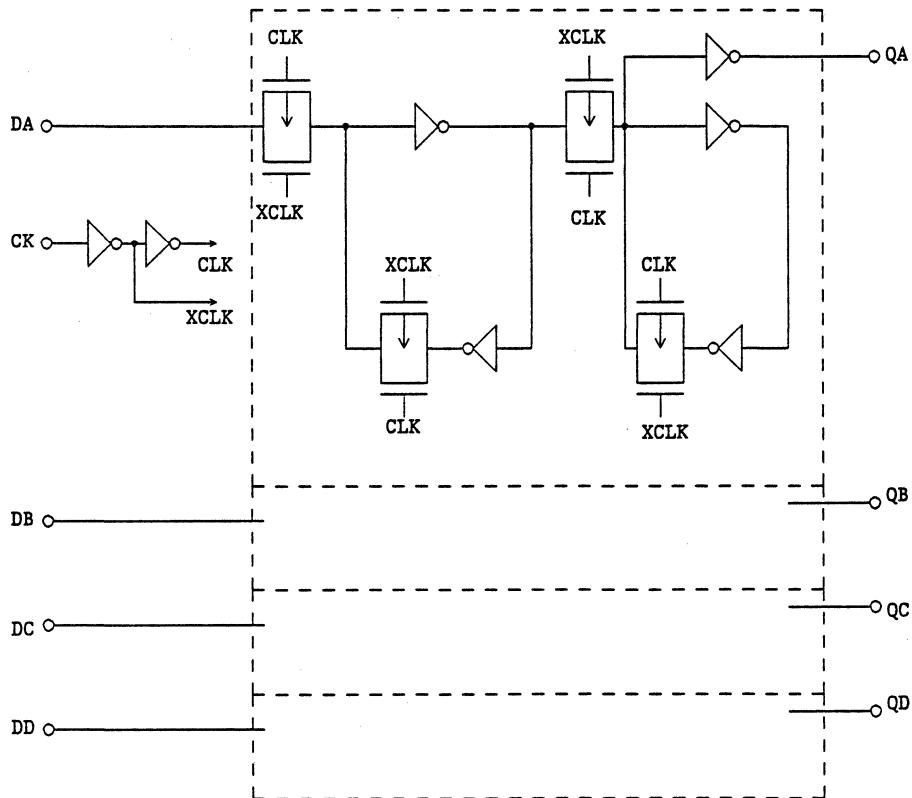
- 2)
- t_{LW}
- ,
- t_{REM}
- ,
- t_{INH}
- and
- t_{pd}
- (CL → QA~QD)



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																
Cell Name	Function					Number of BC																
FDS	Non-SCAN 4-bit DFF					20																
Cell Symbol		Propagation Delay Parameter																				
		tup	tdn			Path																
		t0	KCL	t0	KCL	CK → Q																
		3.03	0.16	2.45	0.09																	
		Parameter																				
		Symbol																				
		Typ(ns)*																				
		Clock Pulse Width																				
		tcw																				
		4.0																				
		Clock Pause Time																				
		tcwh																				
		4.0																				
		Data Setup Time																				
		tSD																				
		1.1																				
		Data Hold Time																				
		tHD																				
		2.5																				
Pin Name		Input Loading Factor (λ_u)																				
D	CK	2																				
		1																				
Pin Name		Output Driving Factor (λ_u)																				
Q		18																				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																						
Function Table																						
<table border="1"> <thead> <tr> <th colspan="2">Inputs</th><th colspan="2">Outputs</th></tr> </thead> <tbody> <tr> <td>CK</td><td>D</td><td>Q</td><td></td></tr> <tr> <td>↑</td><td>L</td><td>L</td><td></td></tr> <tr> <td>↑</td><td>H</td><td>H</td><td></td></tr> </tbody> </table>							Inputs		Outputs		CK	D	Q		↑	L	L		↑	H	H	
Inputs		Outputs																				
CK	D	Q																				
↑	L	L																				
↑	H	H																				
UHB-FDS-E3 Sheet 1/2																						
Page 12-15																						

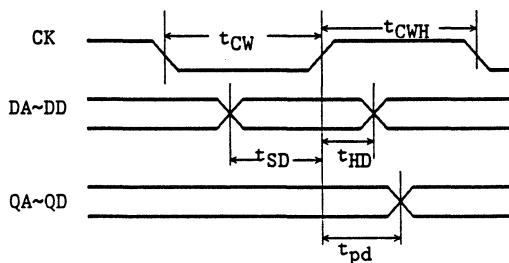
Cell Name	
FDS	

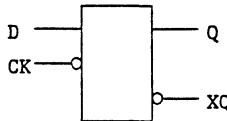
Equivalent Circuit



2

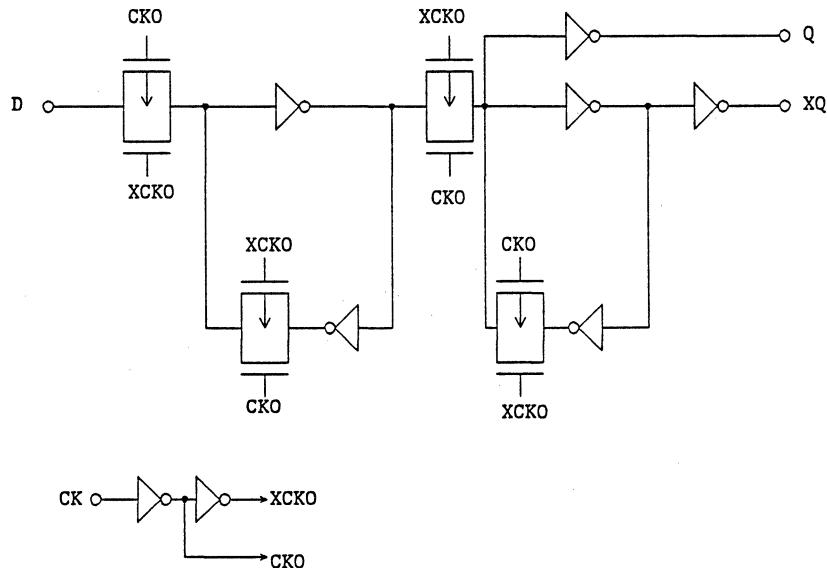
Definition of Parameters



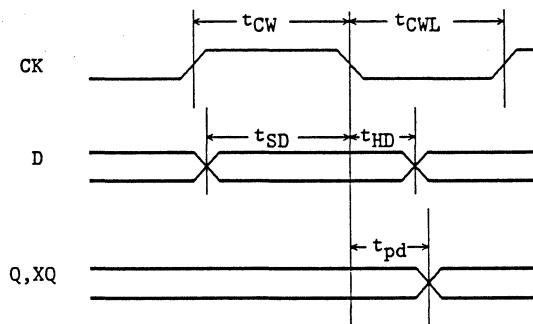
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																
Cell Name	Function	Number of BC																		
FD2	Non-SCAN Power DFF	7																		
Cell Symbol		Propagation Delay Parameter																		
		t _{up}	t _{dn}																	
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	Path												
		1.65	0.08	1.72	0.05	0.10	7	CK → Q												
		2.55	0.08	2.34	0.04	0.07	7	CK → XQ												
		Parameter					Symbol	Typ(ns)*												
		Clock Pulse Width					t _{CW}	4.0												
		Clock Pause Time					t _{CW}	4.0												
		Data Setup Time					t _{SD}	1.1												
		Data Hold Time					t _{HD}	2.4												
Pin Name		Input Loading Factor (ℓ_u)																		
D		2																		
CK		1																		
Pin Name		Output Driving Factor (ℓ_u)																		
Q		36																		
XQ		36																		
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																				
Function Table																				
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Inputs		Outputs																		
CK	D	Q	XQ																	
↓	H L	H L	L H																	

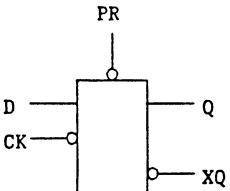
Cell Name	
FD2	

Equivalent Circuit



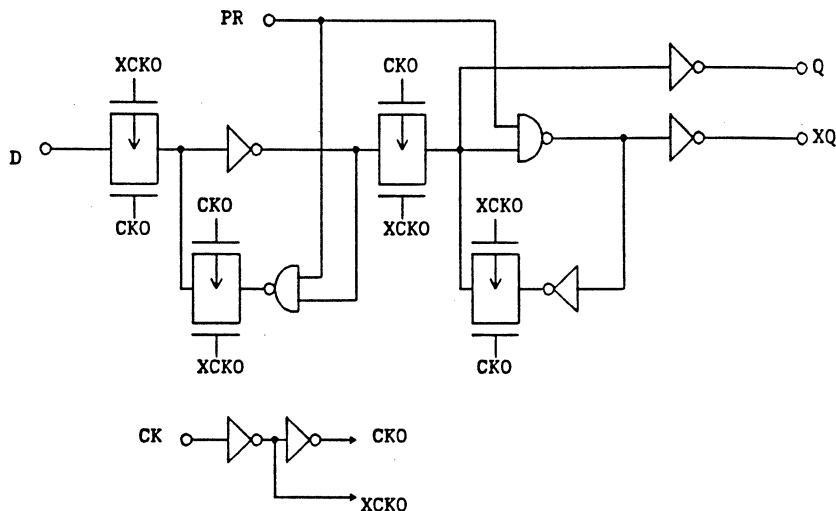
Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																								
Cell Name	Function						Number of BC																								
FD3	Non-SCAN Power DFF with Preset						8																								
Cell Symbol		Propagation Delay Parameter																													
		<table border="1"> <thead> <tr> <th colspan="2">t_{up}</th><th colspan="3">t_{dn}</th></tr> <tr> <th>t₀</th><th>KCL</th><th>t₀</th><th>KCL</th><th>KCL2</th></tr> </thead> <tbody> <tr> <td>1.71</td><td>0.06</td><td>1.73</td><td>0.04</td><td>0.10</td></tr> <tr> <td>2.80</td><td>0.06</td><td>2.50</td><td>0.04</td><td>0.07</td></tr> <tr> <td>2.39</td><td>0.06</td><td>0.91</td><td>0.04</td><td>0.07</td></tr> </tbody> </table>			t _{up}		t _{dn}			t ₀	KCL	t ₀	KCL	KCL2	1.71	0.06	1.73	0.04	0.10	2.80	0.06	2.50	0.04	0.07	2.39	0.06	0.91	0.04	0.07	Path	
t _{up}		t _{dn}																													
t ₀	KCL	t ₀	KCL	KCL2																											
1.71	0.06	1.73	0.04	0.10																											
2.80	0.06	2.50	0.04	0.07																											
2.39	0.06	0.91	0.04	0.07																											
							CK → Q CK → XQ PR → Q, XQ																								
		Parameter																													
		Symbol																													
		Typ(ns)*																													
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		2.1																													
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		t _{PW}																													
		4.0																													
		Preset Release Time																													
		t _{REM}																													
		0.3																													
		Preset Hold Time																													
		t _{INH}																													
		3.8																													

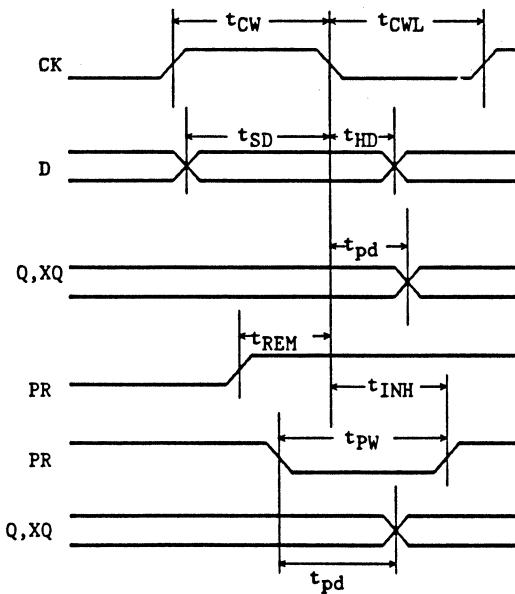
Cell Name	
FD3	

Equivalent Circuit



2

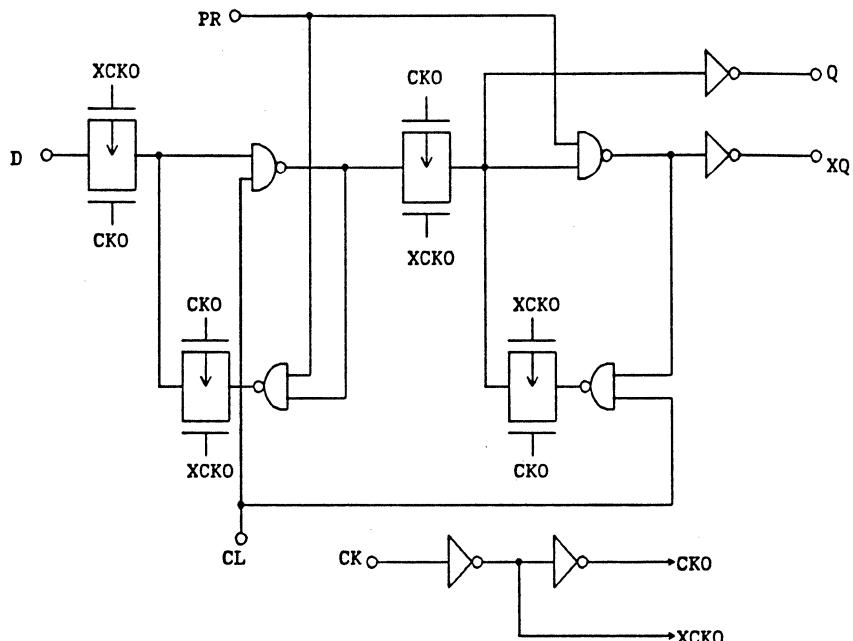
Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																																																																																																																					
Cell Name	Function						Number of BC																																																																																																																					
FD4	Non-SCAN Power DFF with Clear and Preset						9																																																																																																																					
Cell Symbol	Propagation Delay Parameter																																																																																																																											
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Clear Pulse Width	tLW	4.0																																																																																																																										
Clear Release Time	tREM	0.9																																																																																																																										
Clear Hold Time	tINH	3.3																																																																																																																										
Output Driving Factor (λu)																																																																																																																												
Q XQ																																																																																																																												
36 36		<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																																																																																																																										
Function Table																																																																																																																												
Inputs				Outputs																																																																																																																								
PR	CL	CK	D	Q	XQ																																																																																																																							
L	H	X	X	H	L																																																																																																																							
H	L	X	X	L	H																																																																																																																							
H	H	↓	H	H	L																																																																																																																							
H	H	↓	L	L	H																																																																																																																							

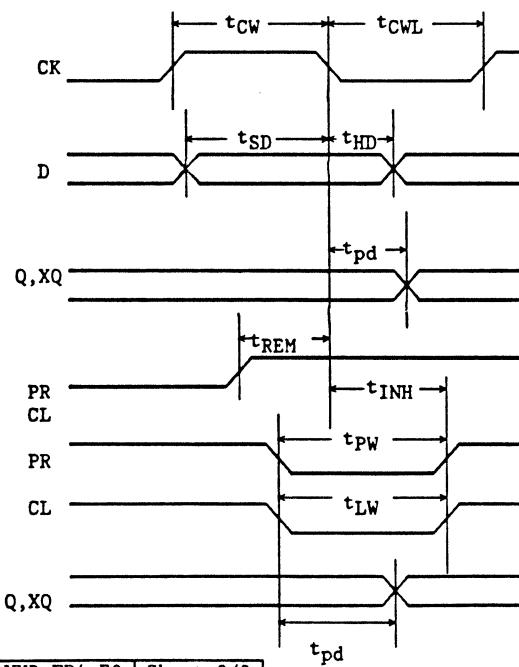
Cell Name	
FD4	

Equivalent Circuit



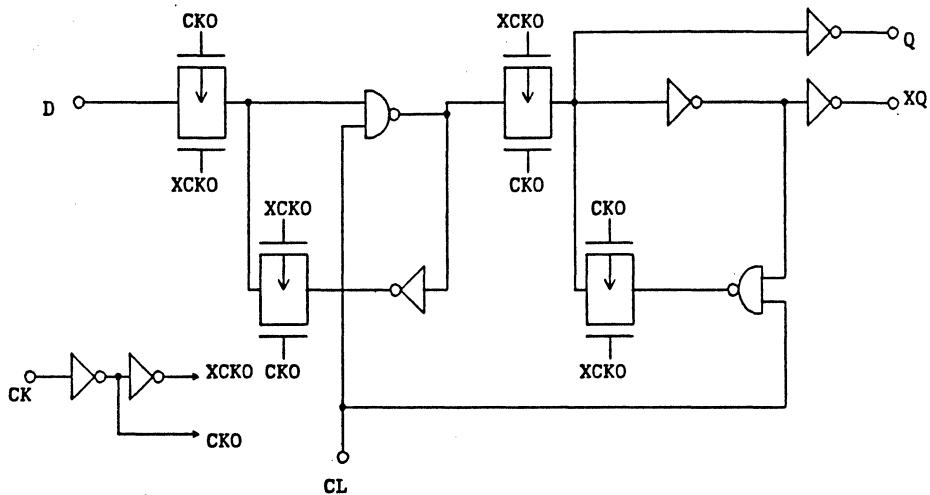
2

Definition of Parameters

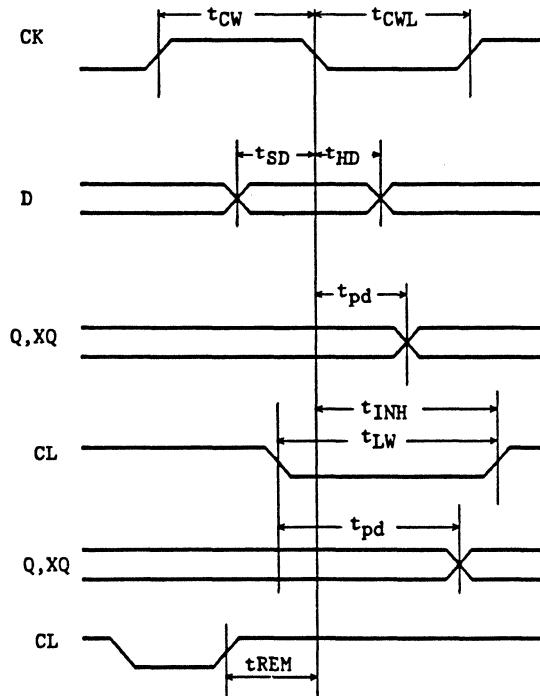


Cell Name
FD5

Equivalent Circuit



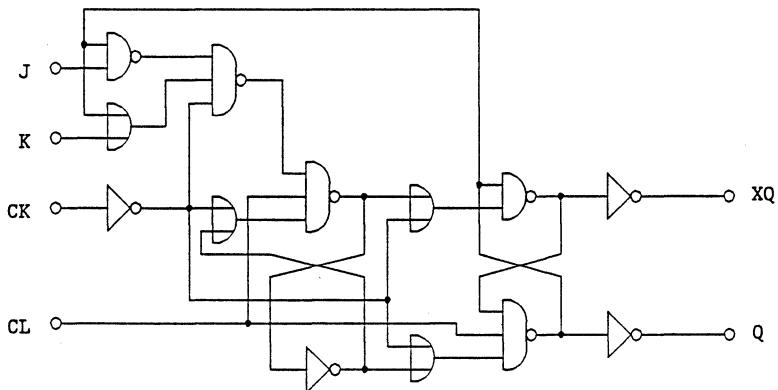
Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version								
Cell Name	Function					Number of BC								
FJD	Non-SCAN Positive edge clocked Power JKFF with Clear					12								
Cell Symbol	Propagation Delay Parameter													
		tup		tdn										
		t0	KCL	t0	KCL	KCL2	CDR2	Path						
		4.40	0.08	2.96	0.05	0.08	7	CK → Q						
		4.43	0.08	2.48	0.05	0.08	7	CK → XQ						
		2.40	0.08	1.29	0.05	0.08	7	CL → Q, XQ						
		J	Q											
		CK		XQ										
		K												
		CL												
Pin Name	Input Loading Factor (f_u)		Parameter				Symbol	Typ(ns)*						
CL	2		Clock Pulse Width				t _{CW}	5.6						
J	1		Clock Pause Time				t _{CWH}	5.6						
K	1		J, K Setup Time				t _{SD}	2.5						
CK	1		J, K Hold Time				t _{HD}	1.2						
Pin Name	Output Driving Factor (f_u)		Clear Pulse Width				t _{LW}	4.0						
Q	36		Clear Release Time				t _{TREM}	2.5						
XQ	36		Clear Hold Time				t _{INH}	4.5						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.														
Function Table														
Inputs			Outputs											
CL	CK	J	K	Q	XQ									
L	X	X	X	L	H									
H	↑	L	L	Q _o	XQ _o									
H	↑	L	H	L	H									
H	↑	H	L	H	L									
H	↑	H	H	XQ _o	Q _o									

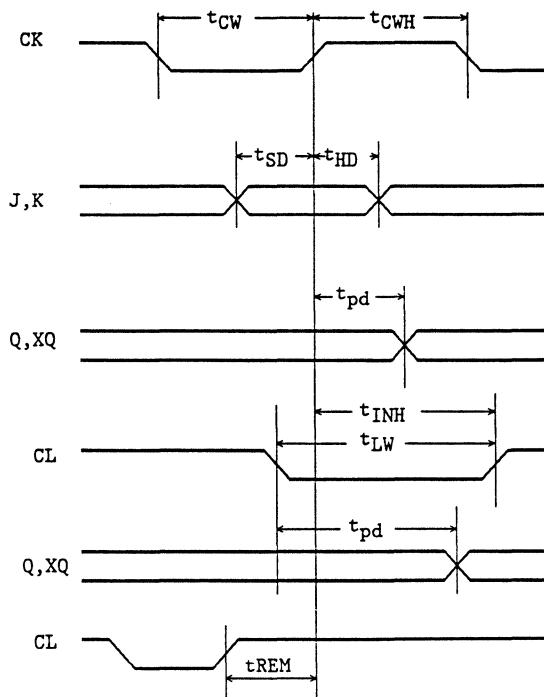
Cell Name	
FJD	

Equivalent Circuit



Definition of Parameters

2



Binary Counter Family

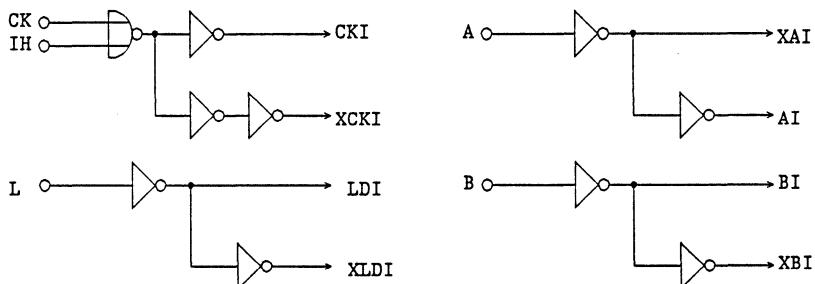
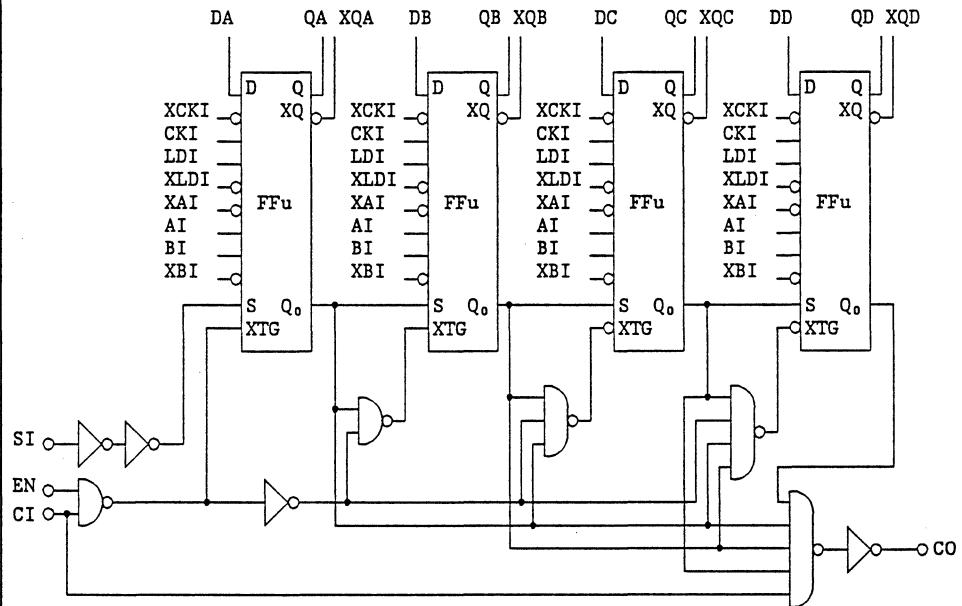
Page	Unit Cell Name	Function	Basic Cells
2-187	SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62
2-192	SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66
2-197	C11	Non-Scan Flip-Flop for Counter	11
2-199	C41	Non-Scan 4-bit Binary Asynchronous Counter	24
2-202	C42	Non-Scan 4-bit Binary Synchronous Counter	32
2-205	C43	Non-Scan 4-bit Binary Synchronous Up Counter	48
2-209	C45	Non-Scan Binary Synchronous Up Counter	48
2-213	C47	Non-Scan Binary Synchronous Up/Down Counter	68

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
SC7	SCAN 4-bit Synchronous Binary Up Counter with Parallel Load				62			
Cell Symbol		Propagation Delay Parameter						
		tup	tdn		Path			
		t0	KCL	t0	KCL	KCL2	CDR2	
		3.30	0.08	3.05	0.06	0.15	7	CK, IH → Q
		5.78	0.08	5.34	0.06	0.15	7	CK, IH → XQ
		7.80	0.08	5.23	0.04	-	-	CK, IH → CO
		2.00	0.08	1.00	0.04	-	-	CI → CO
Parameter						Symbol	Typ(ns)*	
Clock Pulse Width						tCW	7.2	
Clock Pause Time						tCWH	7.2	
Data Setup Time						tSD	2.0	
Data Hold Time						tHD	3.3	
Load Setup Time						tSL	6.3	
Load Hold Time						tHL	3.6	
Pin Name	Input Loading Factor (ℓ_u)	CI Setup Time			tSC	7.2		
		CI Hold Time			tHC	2.7		
	1	EN Setup Time			tSE	7.2		
		EN Hold Time			tHE	2.7		
Pin Name	Output Driving Factor (ℓ_u)	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

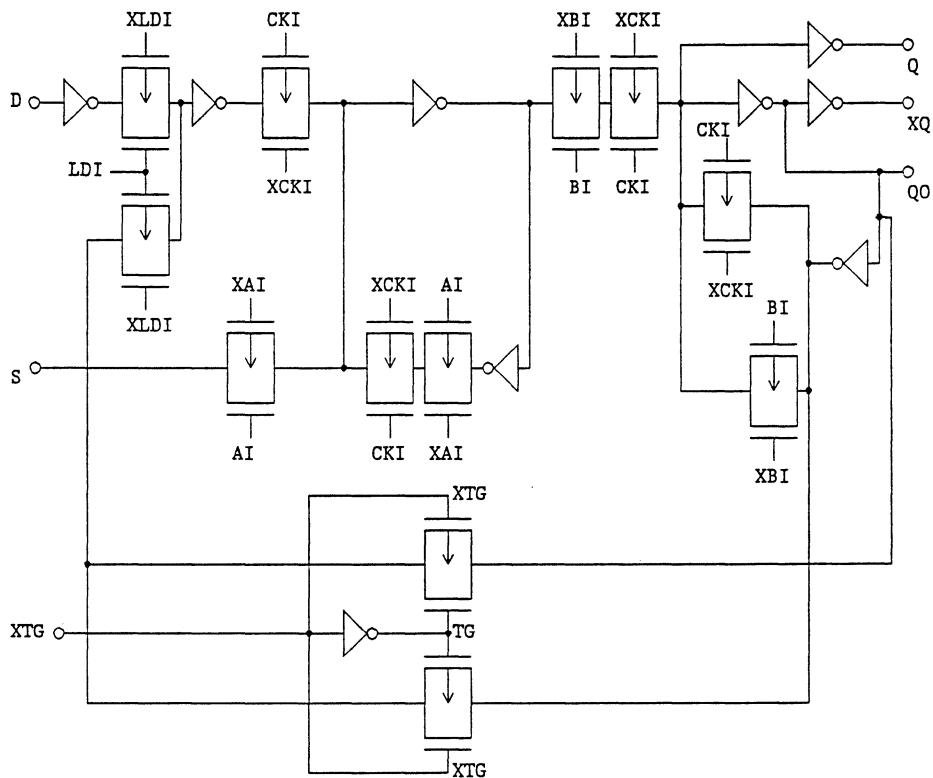
Cell Name	
SC7	

Equivalent Circuit



Cell Name
SC7

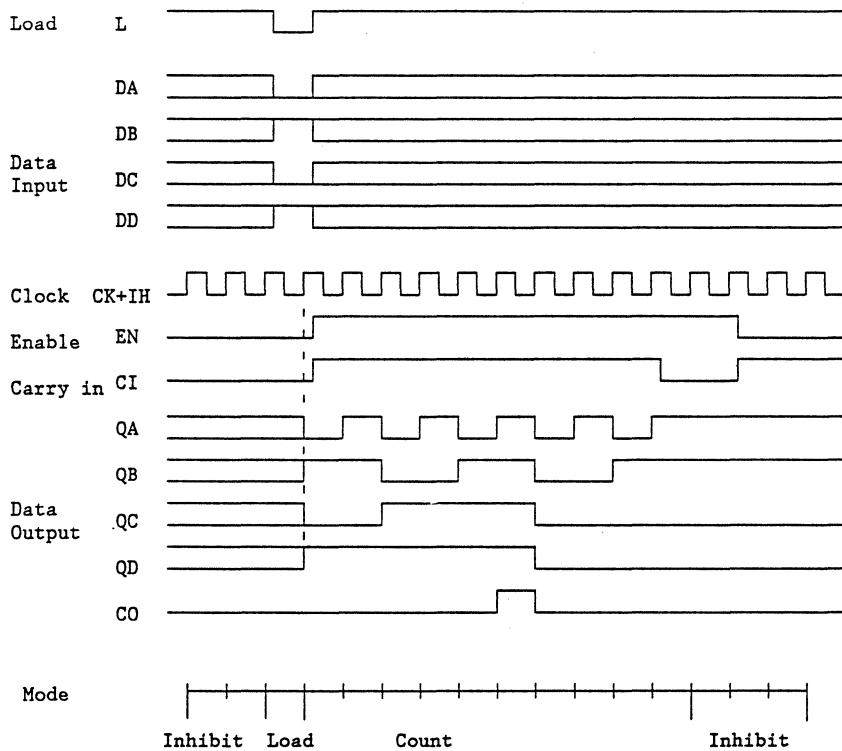
Equivalent Circuit (FFu)



2

Cell Name
SC7

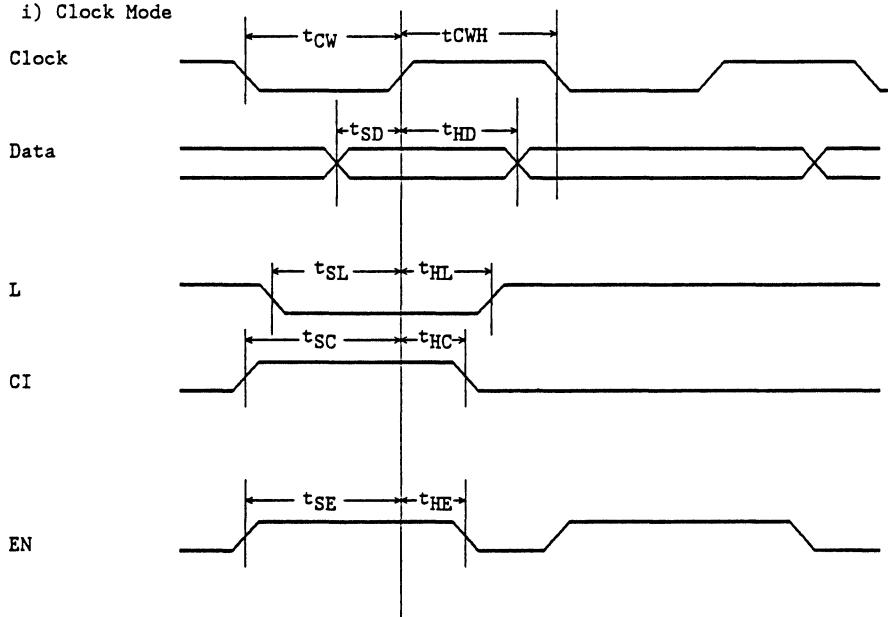
Function



Cell Name
SC7

Definitions of Parameters

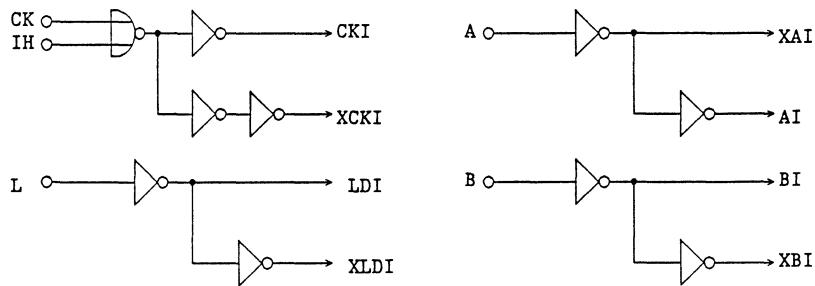
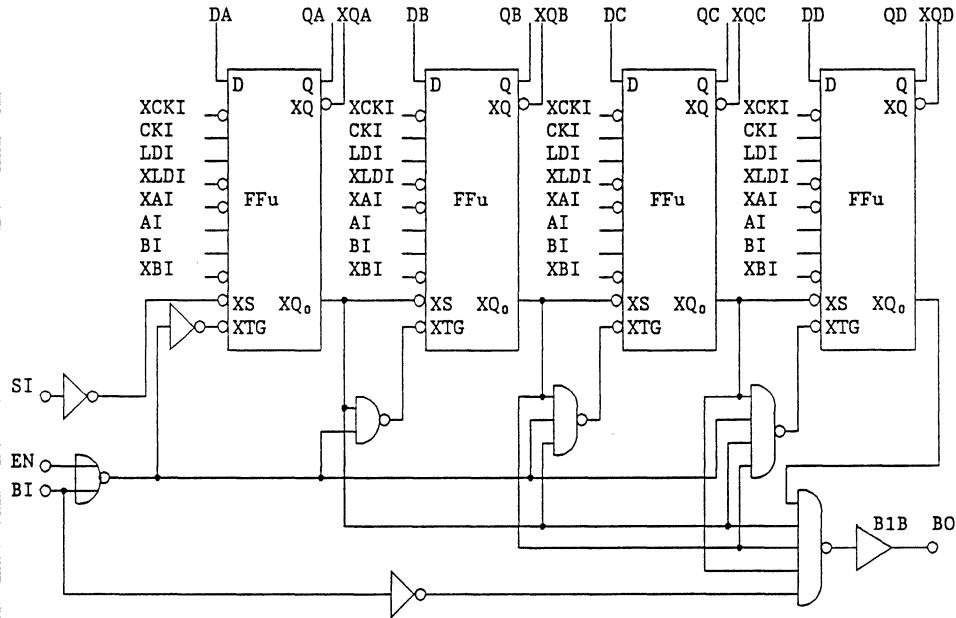
i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
SC8	SCAN 4-bit Synchronous Binary Down Counter with Parallel Load					66
Cell Symbol	Propagation Delay Parameter					
	t _{up}		t _{dn}			
	t ₀	KCL	t ₀	KCL	KCL2	CDR2
	3.37	0.07	3.18	0.06	0.13	7
	4.40	0.06	4.32	0.04		
	6.41	0.08	8.37	0.04		
	1.49	0.08	2.27	0.04		
	Parameter				Symbol	Typ(ns)*
	Clock Pulse Width				t _{CW}	6.8
	Clock Pause Time				t _{CWH}	6.8
	Data Setup Time				t _{SD}	2.0
	Data Hold Time				t _{HD}	3.3
	Load Setup Time				t _{SL}	6.3
	Load Hold Time				t _{HL}	3.6
	Pin Name		Input Loading Factor (μ u)		EN Setup Time	t _{SE}
	D	1				8.1
	CK	1				
	IH	1				
	L	1				
	BI	2				
	EN	1				
	SI	1				
	A,B	1				
	Pin Name		Output Driving Factor (μ u)		BI Setup Time	t _{SB}
	Q	36				8.1
	XQ	36				
	BO	36				
	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					
2						
UHB-SC8-E2	Sheet 1/5					Page 13-6

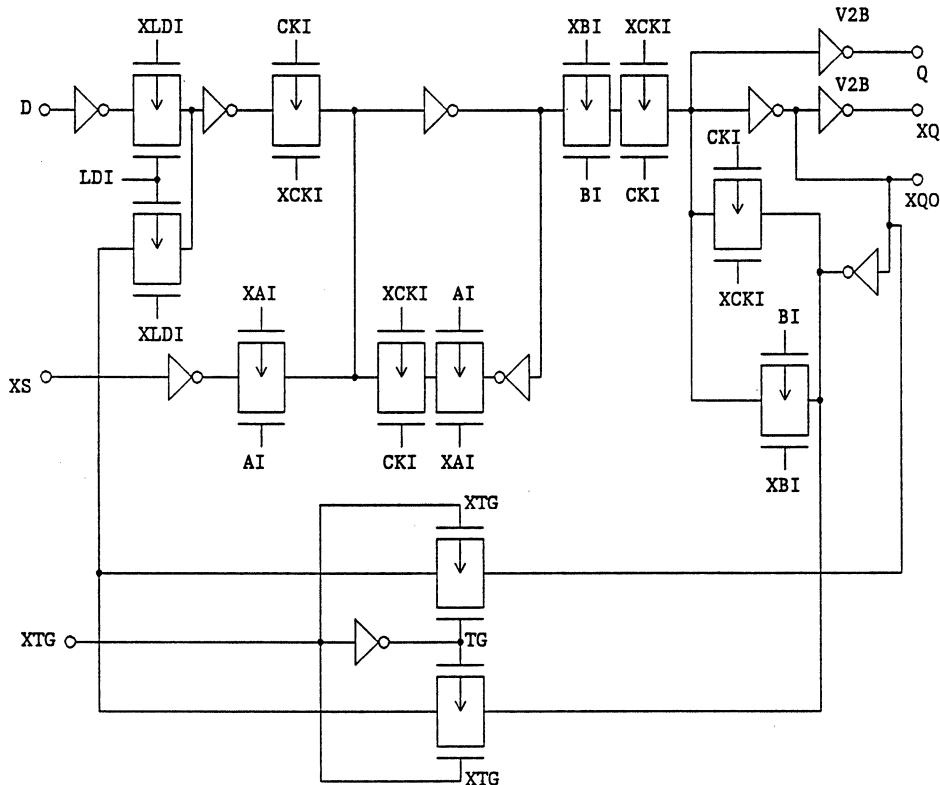
Cell Name
SC8

Equivalent Circuit



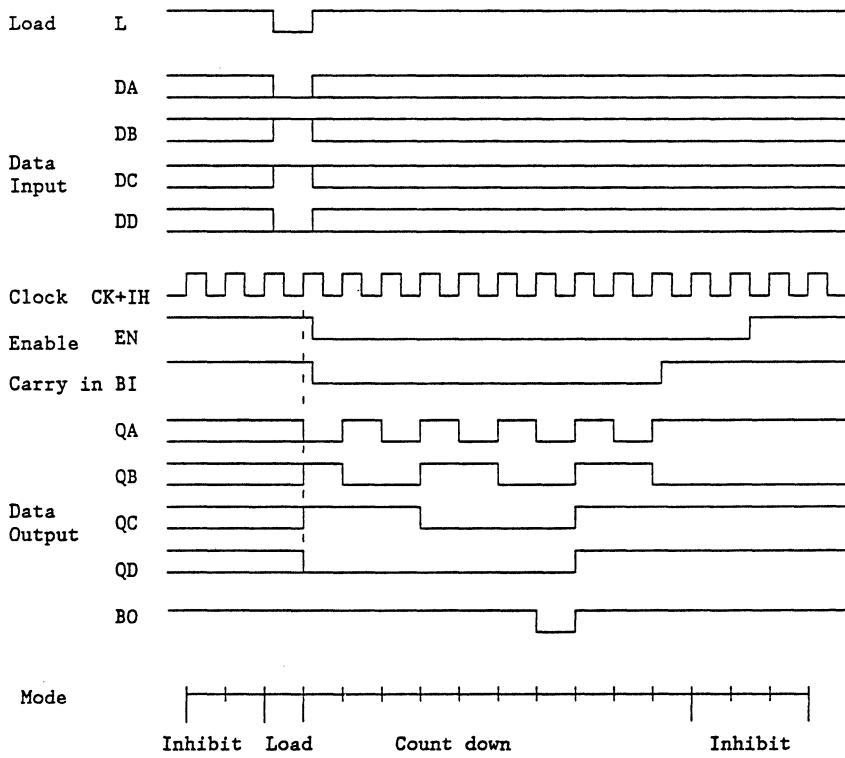
Cell Name
SC8

Equivalent Circuit (FFu)



Cell Name
SC8

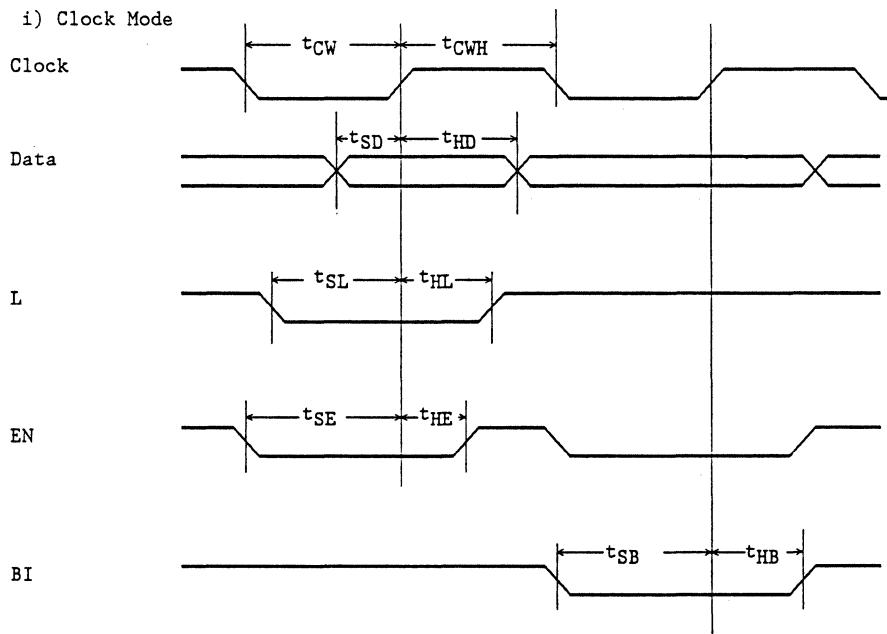
Function

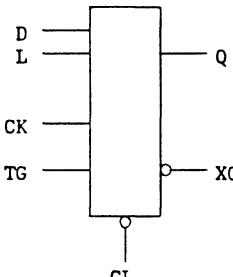


Cell Name
SC8

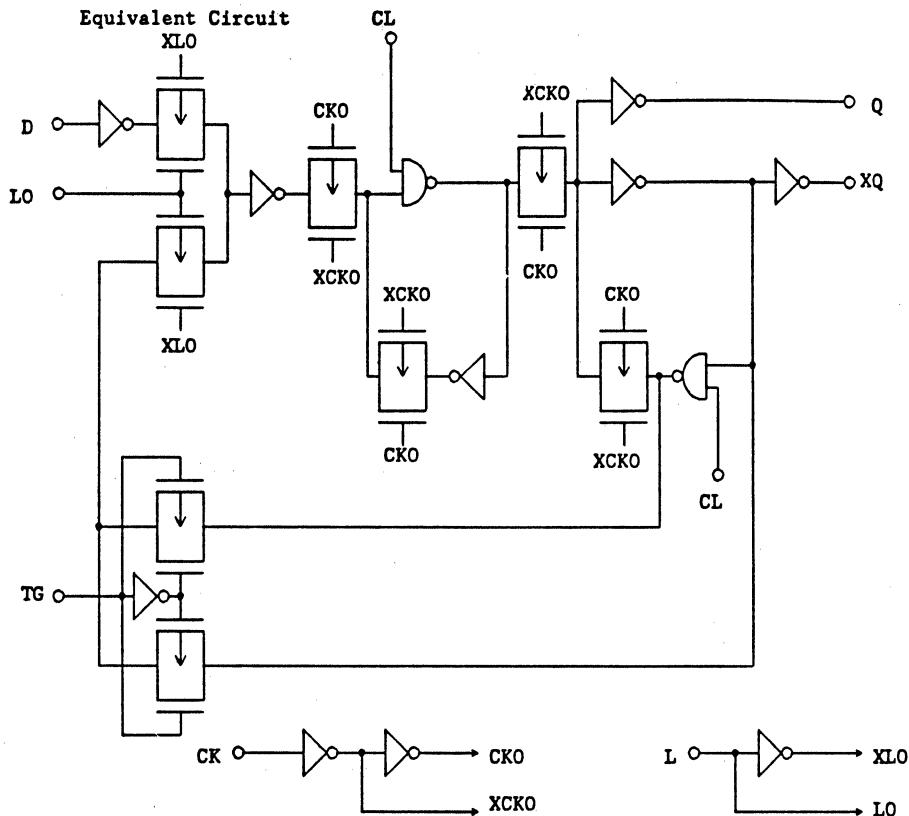
Definitions of Parameters

i) Clock Mode

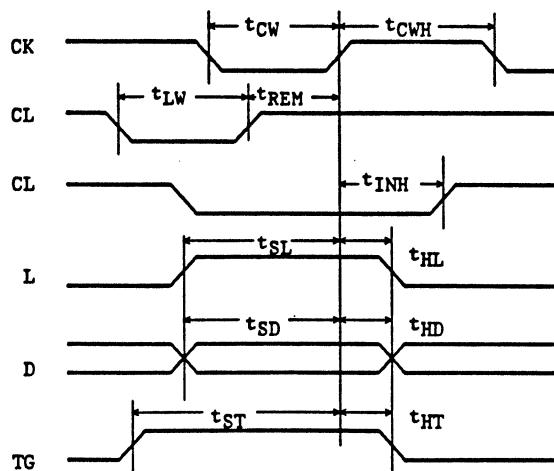


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version											
Cell Name	Function					Number of BC											
C11	Non-SCAN Flip-Flop for Counter					11											
Cell Symbol		Propagation Delay Parameter															
		tup	tdn	KCL	KCL2	CDR2	Path										
		t0 1.90 2.53 2.62	t0 1.75 2.97 1.73	KCL 0.16 0.16 0.16	KCL2	CDR2	CK → Q CK → XQ CL → Q, XQ										
		Parameter															
		Symbol															
		Clock Pulse Width															
		tCW															
		4.0															
		Clock Pause Time															
		tCWH															
		4.2															
		Clear Pulse Width															
		tlW															
		4.0															
		Clear Release Time															
		tREM															
		1.0															
		Clear Hold Time															
		tINH															
		0.5															
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (ℓ_u)</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>2</td> </tr> <tr> <td>TG</td> <td>2</td> </tr> <tr> <td>CL</td> <td>2</td> </tr> <tr> <td>D, CK</td> <td>1</td> </tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓ_u)	L	2	TG	2	CL	2	D, CK	1	Load Setup Time (CK)					
Pin Name	Input Loading Factor (ℓ_u)																
L	2																
TG	2																
CL	2																
D, CK	1																
		tSL															
		0.5															
		Load Hold Time (CK)															
		tHL															
		Data Setup Time (CK)															
		tSD															
		2.5															
		Data Hold Time (CK)															
		tHD															
		0.5															
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (ℓ_u)</th> </tr> </thead> <tbody> <tr> <td>Q</td> <td>18</td> </tr> <tr> <td>XQ</td> <td>18</td> </tr> </tbody> </table>		Pin Name	Output Driving Factor (ℓ_u)	Q	18	XQ	18	TG Setup Time (CK)									
Pin Name	Output Driving Factor (ℓ_u)																
Q	18																
XQ	18																
		tST															
		2.9															
		TG Hold Time (CK)															
		tHT															
		0.0															
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.															
Function Table																	
L	D	TG	CL	CK	Q(Q_0)												
X	X	X	L	X	L												
H	H	X	H	↑	H												
H	L	X	H	↑	L												
L	X	L	H	↑	Q(Q_0)												
L	X	H	H	↑	$\bar{Q}(\bar{Q}_0)$												

Cell Name	C11
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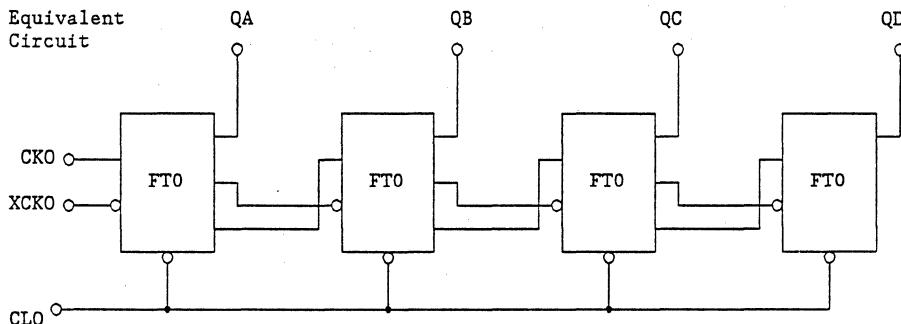
Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
C41	Non-SCAN 4-bit Binary Asynchronous Counter					24		
Cell Symbol	Propagation Delay Parameter							
		tup		tdn		Path		
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.00	0.14	1.86	0.10	-	-	CK → QA
		3.67	0.14	3.28	0.10	-	-	CK → QB
		5.13	0.14	4.75	0.10	-	-	CK → QC
		6.60	0.14	6.20	0.10	-	-	CK → QD
		-	-	4.19	0.10	-	-	CL → Q
Pin Name	Input Loading Factor (f_u)	Parameter					Symbol	Typ(ns)*
CK	1	Clock Pulse Width					tCW	4.3
CL	1	Clock Pause Time					tCWH	4.6
		Clear Pulse Width					tLW	3.9
		Clear Release Time					tREM	2.1
		Clear Hold Time					tINH	6.7
Pin Name	Output Driving Factor (f_u)	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
Function Table								
Inputs		Outputs						
CL	CK	Q						
H	↑	Count up						
L	X	L						

Cell Name	C41
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Equivalent Circuit



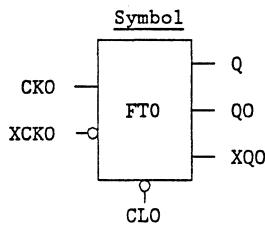
$$\text{CL} \rightarrow \text{CLO}$$

$$\text{CK} \rightarrow \text{CKO}$$

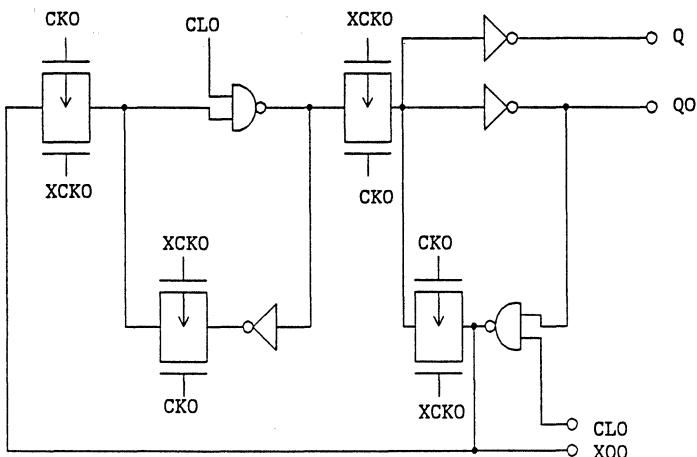
$$\text{XCKO} = \text{CKO}$$

FT0 (Flip-Flop for Counter) (not Unit Cell)

2

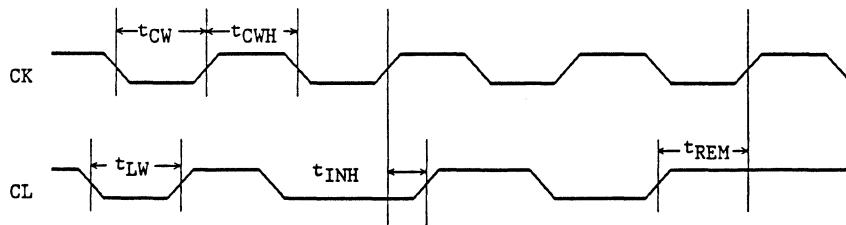
Function Table

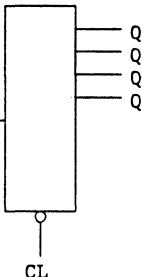
CLO	CKO	Q
L	X	L
H	↑	$\overline{Q_{n-1}}$

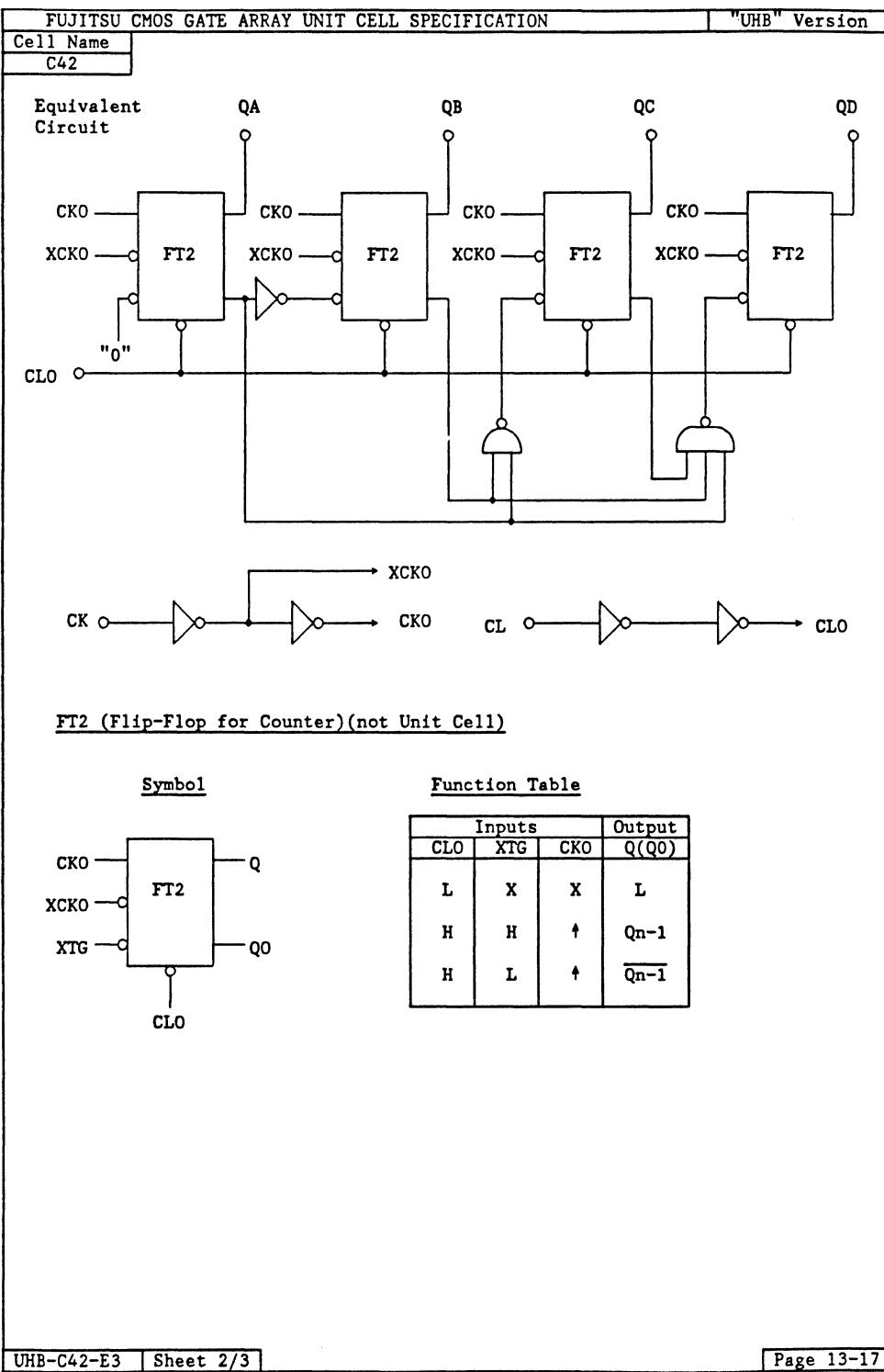


Cell Name
C41

Definition of Parameters

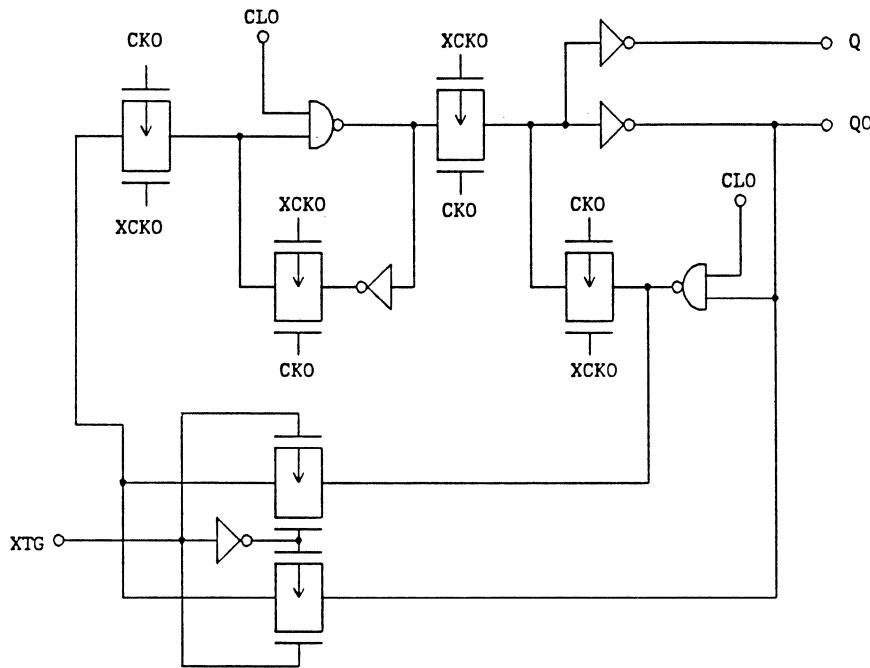


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																															
Cell Name	Function			Number of BC																															
C42	Non-SCAN 4-bit Binary Synchronous Counter				32																														
Cell Symbol	Propagation Delay Parameter																																		
	<table border="1"> <thead> <tr> <th>tup</th> <th>tdn</th> <th colspan="2"></th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>3.18</td> <td>0.14</td> <td>2.34</td> <td>0.09</td> </tr> <tr> <td>-</td> <td>-</td> <td>3.36</td> <td>0.09</td> </tr> <tr> <td></td> <td></td> <td></td> <td>0.12</td> </tr> <tr> <td></td> <td></td> <td></td> <td>CDR2</td> </tr> <tr> <td></td> <td></td> <td></td> <td>4</td> </tr> <tr> <td></td> <td></td> <td></td> <td>4</td> </tr> </tbody> </table>	tup	tdn			t0	KCL	t0	KCL	3.18	0.14	2.34	0.09	-	-	3.36	0.09				0.12				CDR2				4				4	Path	
tup	tdn																																		
t0	KCL	t0	KCL																																
3.18	0.14	2.34	0.09																																
-	-	3.36	0.09																																
			0.12																																
			CDR2																																
			4																																
			4																																
		CK → Q CL → Q																																	
	<table border="1"> <thead> <tr> <th>Parameter</th> <th>Symbol</th> <th>Typ(ns)*</th> </tr> </thead> <tbody> <tr> <td>Clock Pulse Width</td> <td>tCW</td> <td>4.3</td> </tr> <tr> <td>Clock Pause Time</td> <td>tCWH</td> <td>4.6</td> </tr> <tr> <td>Clear Pulse Width</td> <td>tLW</td> <td>4.0</td> </tr> <tr> <td>Clear Release Time</td> <td>tREM</td> <td>2.1</td> </tr> <tr> <td>Clear Hold Time</td> <td>tINH</td> <td>6.7</td> </tr> </tbody> </table>	Parameter	Symbol	Typ(ns)*	Clock Pulse Width	tCW	4.3	Clock Pause Time	tCWH	4.6	Clear Pulse Width	tLW	4.0	Clear Release Time	tREM	2.1	Clear Hold Time	tINH	6.7																
Parameter	Symbol	Typ(ns)*																																	
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Clock Pause Time	tCWH	4.6																																	
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Clear Release Time	tREM	2.1																																	
Clear Hold Time	tINH	6.7																																	
Pin Name	Input Loading Factor (ℓ_u)																																		
CL	1																																		
CK	1																																		
Pin Name	Output Driving Factor (ℓ_u)																																		
Q	18																																		
<p>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</p>																																			
Function Table																																			
<table border="1"> <thead> <tr> <th colspan="2">Inputs</th> <th>Outputs</th> </tr> <tr> <th>CL</th> <th>CK</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>H L</td> <td>↑ X</td> <td>Count up L</td> </tr> </tbody> </table>						Inputs		Outputs	CL	CK	Q	H L	↑ X	Count up L																					
Inputs		Outputs																																	
CL	CK	Q																																	
H L	↑ X	Count up L																																	

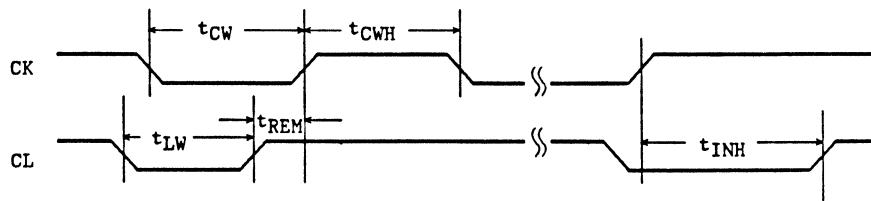


Cell Name	
C42	

Equivalent Circuit of FT2



Definition of Parameters

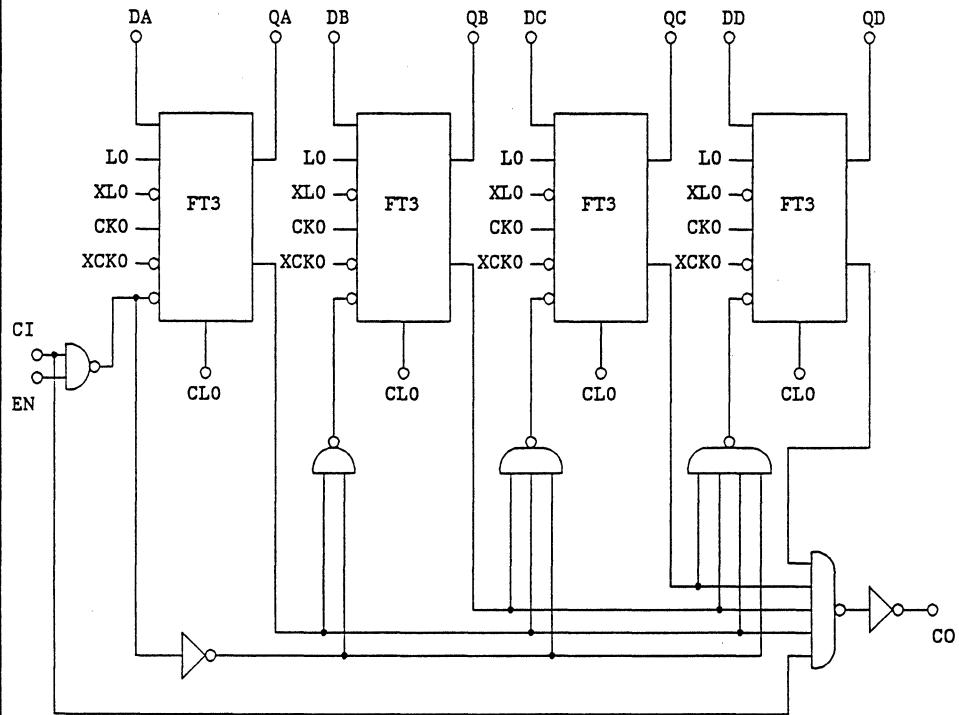


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																																										
Cell Name	Function						Number of BC																																										
C43	Non-SCAN 4-bit Binary Synchronous Up Counter						48																																										
Cell Symbol		Propagation Delay Parameter																																															
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>t_{up}</th> <th>KCL</th> <th>t₀</th> <th>KCL</th> <th>KCL2</th> <th>CDR2</th> <th>Path</th> </tr> </thead> <tbody> <tr> <td>2.96</td> <td>0.16</td> <td>2.40</td> <td>0.09</td> <td></td> <td></td> <td>CK → Q</td> </tr> <tr> <td>5.60</td> <td>0.16</td> <td>3.56</td> <td>0.08</td> <td></td> <td></td> <td>CK → CO</td> </tr> <tr> <td>1.60</td> <td>0.16</td> <td>0.81</td> <td>0.08</td> <td></td> <td></td> <td>CI → CO</td> </tr> <tr> <td>-</td> <td>-</td> <td>3.88</td> <td>0.09</td> <td></td> <td></td> <td>CL → Q</td> </tr> <tr> <td>-</td> <td>-</td> <td>2.64</td> <td>0.08</td> <td></td> <td></td> <td>CL → CO</td> </tr> </tbody> </table>					t _{up}	KCL	t ₀	KCL	KCL2	CDR2	Path	2.96	0.16	2.40	0.09			CK → Q	5.60	0.16	3.56	0.08			CK → CO	1.60	0.16	0.81	0.08			CI → CO	-	-	3.88	0.09			CL → Q	-	-	2.64	0.08			CL → CO	
t _{up}	KCL	t ₀	KCL	KCL2	CDR2	Path																																											
2.96	0.16	2.40	0.09			CK → Q																																											
5.60	0.16	3.56	0.08			CK → CO																																											
1.60	0.16	0.81	0.08			CI → CO																																											
-	-	3.88	0.09			CL → Q																																											
-	-	2.64	0.08			CL → CO																																											
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EN Setup Time	t _{SE}	4.3																																															
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CL	L	D	EN	CI	CK	Q																																											
L	X	X	X	X	X	L																																											
H	L	H	X	X	↑	H																																											
H	L	L	X	X	↑	L																																											
H	H	X	X	L	X	No Counting																																											
H	H	X	L	X	X	No Counting																																											
H	H	X	H	H	↑	Count up																																											

Note : The CO output produces a high level output data when the counter overflows.

Cell Name	
C43	

Equivalent Circuit



2

$$CL \rightarrow CL0$$

$$L \rightarrow L0$$

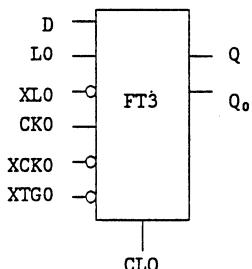
$$L \rightarrow XL0$$

$$CK \rightarrow XCK0$$

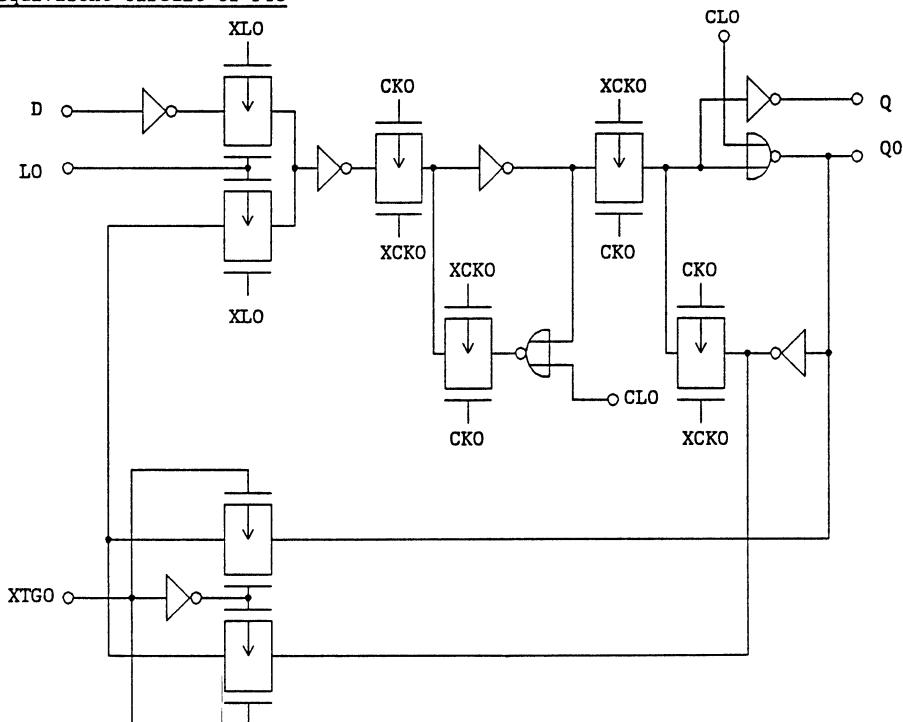
$$CK \rightarrow CK0$$

Cell Name
C43

• FT3 (Flip-Flop for Counter)(not Unit Cell)

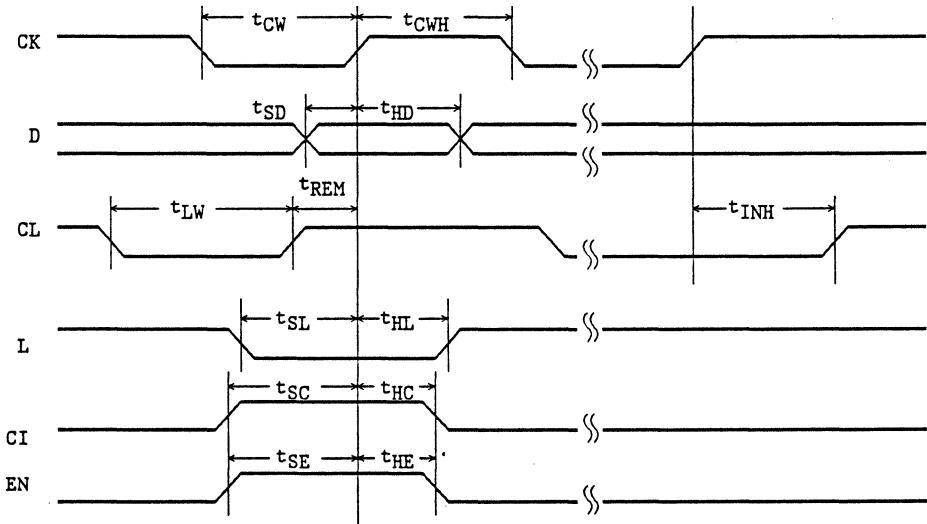
SymbolFunction Table

L0	D	XTGO	CLO	CK	Q(Q0)
X	X	X	H	X	L
H	H	X	L	↑	H
H	L	X	L	↑	L
L	X	H	L	↑	Q(Q0)
L	X	L	L	↑	Q(Q0)

Equivalent Circuit of FT3

Cell Name
C43

Definition of Parameters

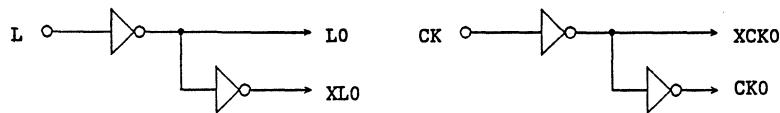
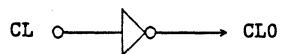
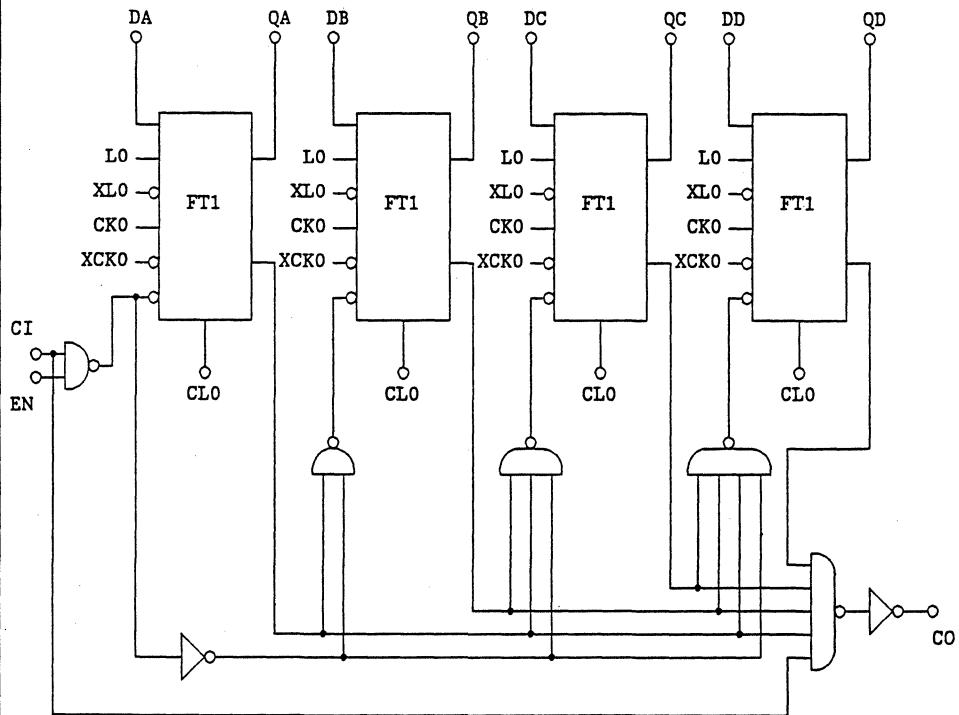


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version
Cell Name	Function						Number of BC
C45	Non-SCAN 4-bit Binary Synchronous Up Counter						48
Cell Symbol	Propagation Delay Parameter						
	t _{up}	KCL	t ₀	KCL	KCL2	CDR2	Path
DA	2.67	0.14	1.87	0.09	0.13	4	CK → Q
DB	5.07	0.17	2.82	0.09			CK → CO
DC	1.91	0.17	1.36	0.09			CI → CO
DD							
L							
CK							
EN							
CI							
CL							
QA							
QB							
QC							
QD							
CO							
Parameter	Symbol	Typ(ns)*					
Clock Pulse Width	t _{CW}	4.0					
Clock Pause Time	t _{CWH}	4.6					
Data Setup Time	t _{SD}	3.8					
Data Hold Time	t _{HD}	2.1					
Load Setup Time	t _{SL}	5.0					
Load Hold Time	t _{HL}	2.1					
CI Setup Time	t _{SC}	6.6					
CI Hold Time	t _{HC}	1.9					
EN Setup Time	t _{SE}	6.6					
EN Hold Time	t _{HE}	1.9					
Clear Setup Time	t _{SR}	3.8					
Clear Hold Time	t _{HR}	2.0					
Pin Name	Input Loading Factor (f <u>u</u>)						
D	1						
L, EN	1						
CK, CL	1						
CI	2						
Pin Name	Output Driving Factor (f <u>u</u>)						
Q	18						
CO	18						
* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.							
Function Table							
Inputs						Outputs	
CL	L	D	EN	CI	CK	Q	
L	X	X	X	X	↑	L	
H	L	H	X	X	↑	H	
H	L	L	X	X	↑	L	
H	H	X	X	L	X	No Counting	
H	H	X	L	X	X	No Counting	
H	H	X	H	H	↑	Count up	

Note : The CO output produces a high level output data when the counter overflows.

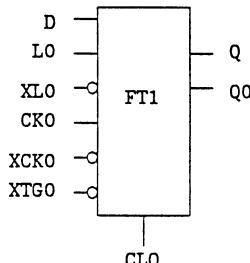
Cell Name
C45

Equivalent Circuit

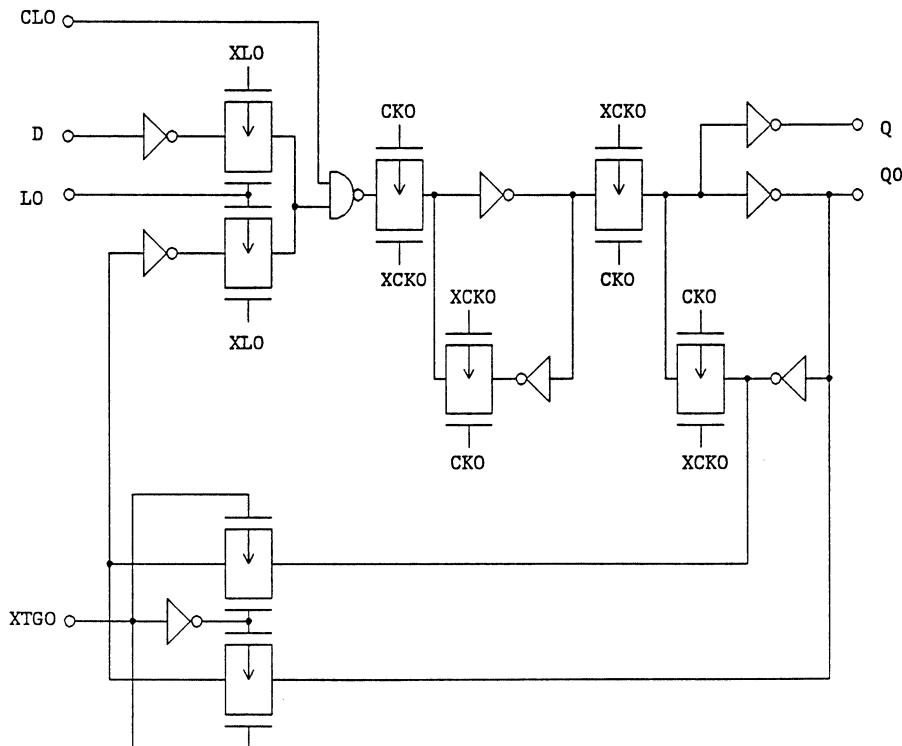


Cell Name	
C45	

- FT1 (Flip-Flop for Counter)(not Unit Cell)

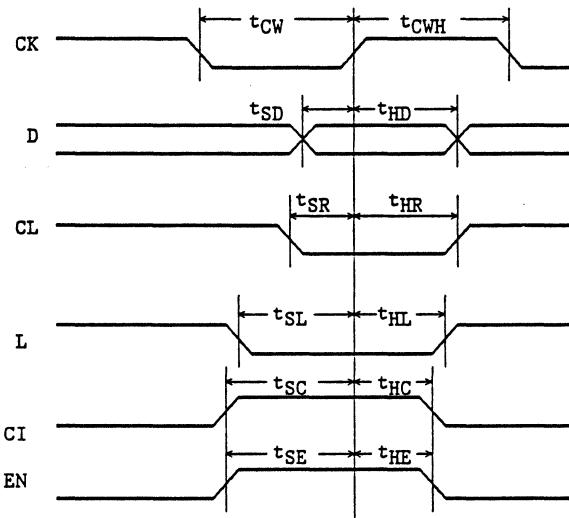
SymbolFunction Table

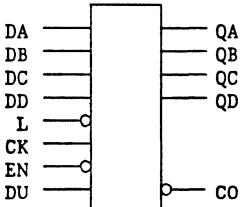
L0	D	XTGO	CL0	CK	Q(Q0)
L	X	X	H	↑	L
H	H	X	L	↑	H
H	L	X	L	↑	L
L	X	H	L	↑	Q(Q0)
L	X	L	L	↑	Q(Q0)

Equivalent Circuit of FT3

Cell Name
C45

Definition of Parameters

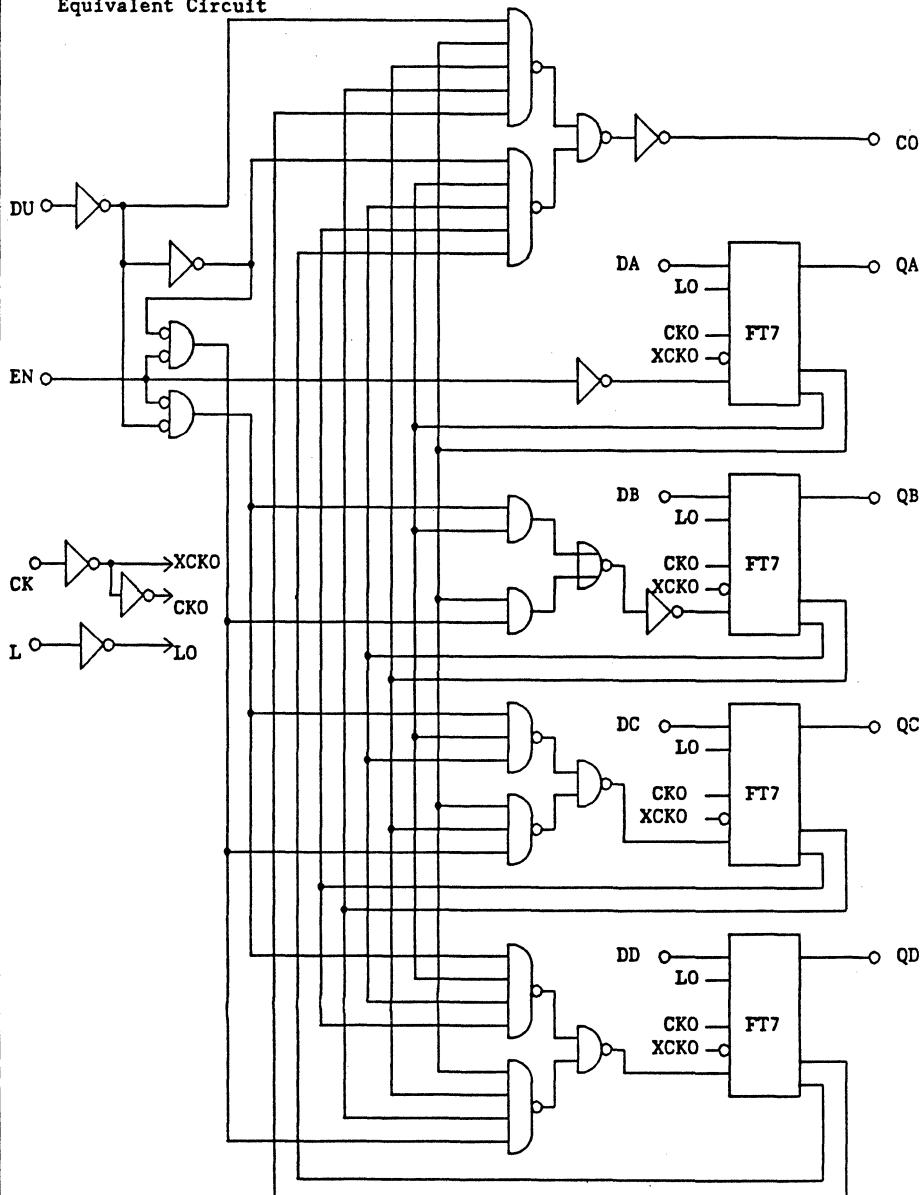


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																																																			
Cell Name	Function					Number of BC																																																			
C47	Non-SCAN 4-bit Binary Synchronous Up/Down Counter					68																																																			
Cell Symbol	Propagation Delay Parameter																																																								
																																																									
<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="4">tdn</th><th>Path</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th><th></th></tr> </thead> <tbody> <tr> <td>3.99</td><td>0.16</td><td>3.59</td><td>0.16</td><td>0.25</td><td>4</td><td>CK → Q</td></tr> <tr> <td>5.41</td><td>0.11</td><td>6.12</td><td>0.08</td><td></td><td></td><td>CK → CO</td></tr> <tr> <td>5.01</td><td>0.16</td><td>5.54</td><td>0.16</td><td>0.25</td><td>4</td><td>L → Q</td></tr> <tr> <td>2.47</td><td>0.11</td><td>3.01</td><td>0.08</td><td></td><td></td><td>DU → CO</td></tr> </tbody> </table>						tup		tdn				Path	t0	KCL	t0	KCL	KCL2	CDR2		3.99	0.16	3.59	0.16	0.25	4	CK → Q	5.41	0.11	6.12	0.08			CK → CO	5.01	0.16	5.54	0.16	0.25	4	L → Q	2.47	0.11	3.01	0.08			DU → CO										
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Q	L	EN	DU	CK	Q																																																				
H	L	X	X	X	H																																																				
L	L	X	X	X	L																																																				
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<p>Note : The CO output produces a low level output pulse when the counter overflows or underflows.</p>																																																									

Cell Name

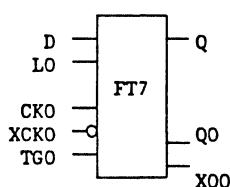
C47

Equivalent Circuit

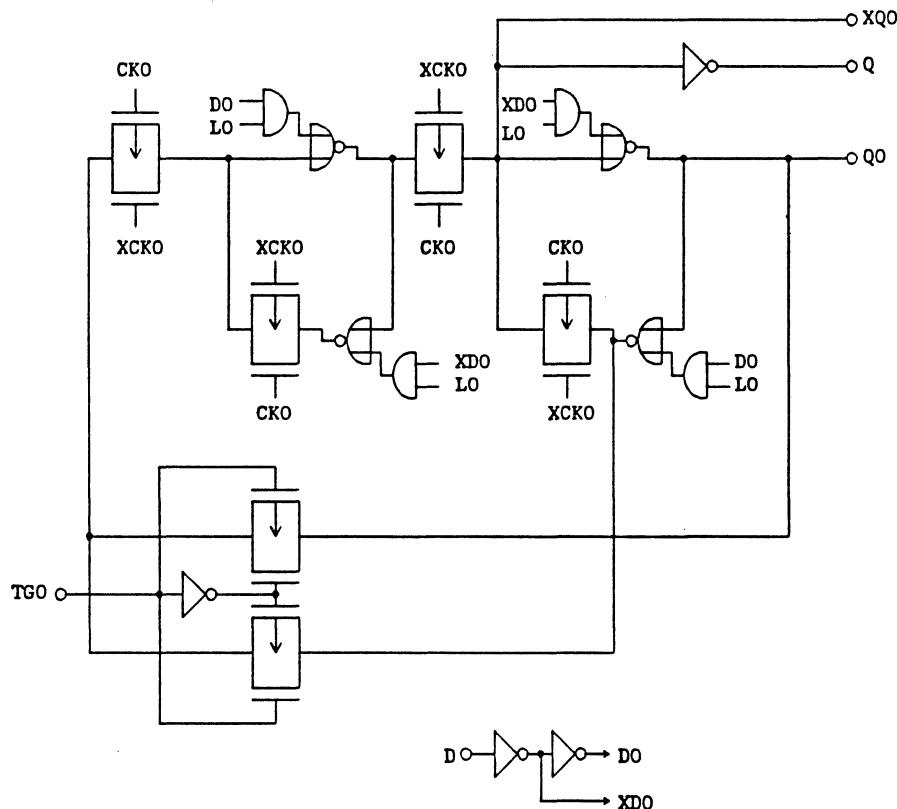


Cell Name
C47

- FT7 (Flip-Flop for Counter) (not Unit Cell)

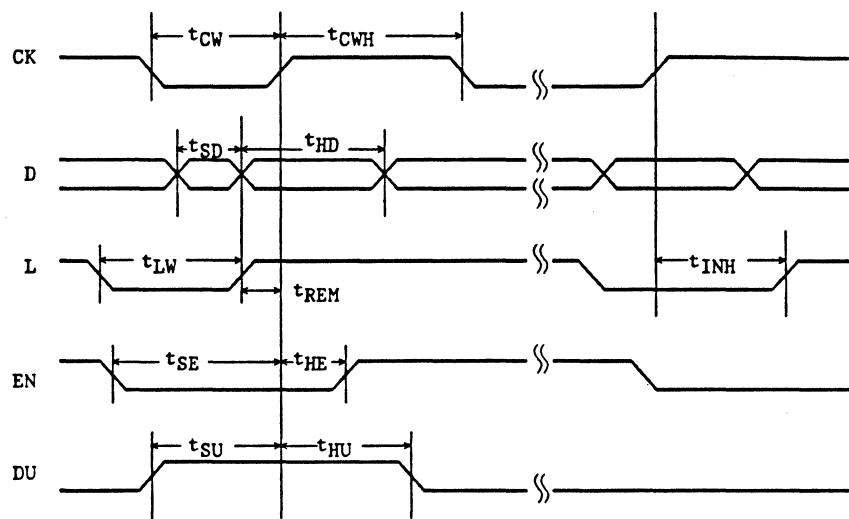
SymbolFunction Table

		Inputs		Outputs	
LO	D	TGO	CKO	Q0(Q)	$\bar{Q}(Q_0)$
H	H	X	X	H	L
H	L	X	X	L	H
L	X	L	↑	Q_{n-1}	$\overline{Q_{n-1}}$
L	X	H	↑	$\overline{Q_{n-1}}$	Q_{n-1}

Equivalent Circuit of FT7

Cell Name
C47

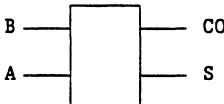
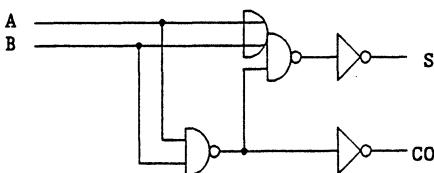
Definition of Parameters

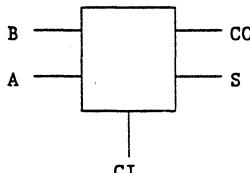
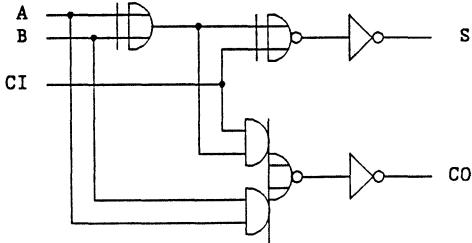


Adder Family

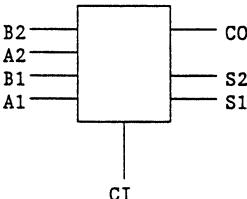
Page	Unit Cell Name	Function	Basic Cells
2-219	A1A	1-bit Half Adder	5
2-220	A1N	1-bit Full Adder	8
2-221	A2N	2-bit Full Adder	16
2-223	A4H	4-bit Binary Full Adder with Fast Carry	48

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																							
Cell Name	Function	Number of BC																									
A1A	1-bit Half Adder	5																									
Cell Symbol		Propagation Delay Parameter																									
		tup	tdn																								
		t0	KCL	t0	KCL	KCL2	CDR2	Path																			
		1.22	0.08	1.44	0.04			A → S																			
		1.09	0.08	1.46	0.04			B → S																			
		1.12	0.08	1.25	0.04			A → CO																			
		1.27	0.08	1.15	0.04			B → CO																			
		Parameter				Symbol	Typ(ns)*																				
Pin Name		Input Loading Factor (ℓ_u)																									
A		2																									
B		2																									
Pin Name		Output Driving Factor (ℓ_u)																									
CO		36																									
S		36																									
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																											
Function Table						Equivalent Circuit																					
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 50px;">A</th><th style="width: 50px;">B</th><th style="width: 50px;">CO</th><th style="width: 50px;">S</th></tr> <tr> <td>L</td><td>L</td><td>L</td><td>L</td></tr> <tr> <td>L</td><td>H</td><td>L</td><td>H</td></tr> <tr> <td>H</td><td>L</td><td>L</td><td>H</td></tr> <tr> <td>H</td><td>H</td><td>H</td><td>L</td></tr> </table>						A	B	CO	S	L	L	L	L	L	H	L	H	H	L	L	H	H	H	H	L		
A	B	CO	S																								
L	L	L	L																								
L	H	L	H																								
H	L	L	H																								
H	H	H	L																								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version																																																				
Cell Name	Function				Number of BC																																																				
A1N	1-bit Full Adder				8																																																				
Cell Symbol		Propagation Delay Parameter																																																							
		tup	tdn	t0	KCL	KCL2	Path																																																		
		2.64	0.16	3.15	0.08		A,B → S																																																		
		1.25	0.16	1.35	0.08		CI → S																																																		
		2.98	0.16	2.38	0.08		A,B → CO																																																		
		1.02	0.16	1.17	0.08		CI → CO																																																		
		Parameter					Symbol																																																		
							Typ(ns)*																																																		
Pin Name		Input Loading Factor (lu)																																																							
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L	L	L	L	L																																																					
H	L	L	H	L																																																					
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L	H	H	L	H																																																					
H	H	H	H	H																																																					
UHB-A1N-E2 Sheet 1/1			Page 14-2																																																						

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																																																																																											
Cell Name	Function						Number of BC																																																																																											
A2N	2-bit Full Adder						16																																																																																											
Cell Symbol		Propagation Delay Parameter																																																																																																
		<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="2">tdn</th><th colspan="2"></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th></tr> </thead> <tbody> <tr><td>2.85</td><td>0.29</td><td>2.81</td><td>0.14</td><td></td><td></td></tr> <tr><td>2.74</td><td>0.29</td><td>2.87</td><td>0.14</td><td></td><td></td></tr> <tr><td>1.58</td><td>0.29</td><td>1.36</td><td>0.09</td><td>0.12</td><td>4</td></tr> <tr><td>1.47</td><td>0.29</td><td>1.36</td><td>0.09</td><td>0.12</td><td>4</td></tr> <tr><td>2.79</td><td>0.29</td><td>2.58</td><td>0.14</td><td></td><td></td></tr> <tr><td>2.97</td><td>0.22</td><td>2.75</td><td>0.14</td><td></td><td></td></tr> <tr><td>2.97</td><td>0.22</td><td>2.75</td><td>0.14</td><td></td><td></td></tr> <tr><td>1.18</td><td>0.22</td><td>1.19</td><td>0.14</td><td></td><td></td></tr> <tr><td>2.82</td><td>0.22</td><td>2.75</td><td>0.14</td><td></td><td></td></tr> <tr><td>3.11</td><td>0.22</td><td>2.95</td><td>0.14</td><td></td><td></td></tr> <tr><td>2.71</td><td>0.22</td><td>2.81</td><td>0.14</td><td></td><td></td></tr> <tr><td>3.11</td><td>0.22</td><td>2.95</td><td>0.14</td><td></td><td></td></tr> <tr><td>2.76</td><td>0.22</td><td>2.52</td><td>0.14</td><td></td><td></td></tr> </tbody> </table>	tup		tdn				t0	KCL	t0	KCL	KCL2	CDR2	2.85	0.29	2.81	0.14			2.74	0.29	2.87	0.14			1.58	0.29	1.36	0.09	0.12	4	1.47	0.29	1.36	0.09	0.12	4	2.79	0.29	2.58	0.14			2.97	0.22	2.75	0.14			2.97	0.22	2.75	0.14			1.18	0.22	1.19	0.14			2.82	0.22	2.75	0.14			3.11	0.22	2.95	0.14			2.71	0.22	2.81	0.14			3.11	0.22	2.95	0.14			2.76	0.22	2.52	0.14			Path					
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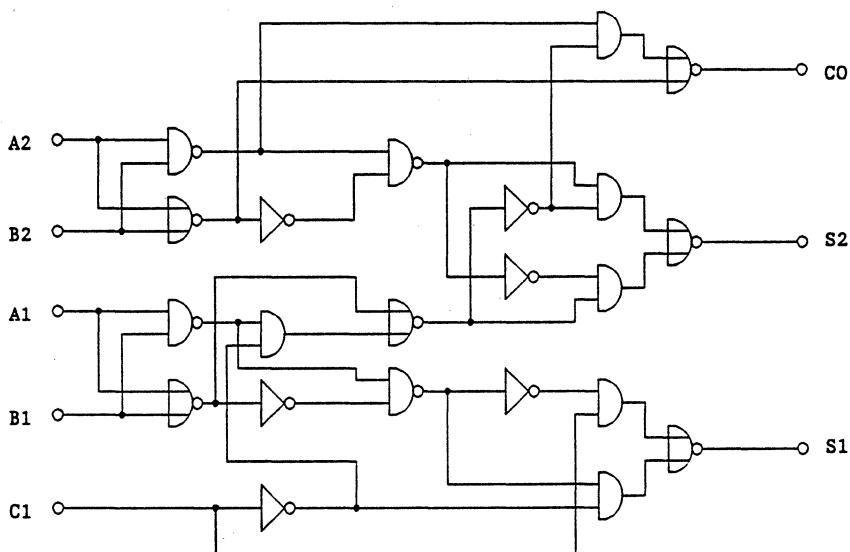
Function Table

Inputs				Outputs							
				CI = L			CI = H				
A1	B1	A2	B2	S1	S2	CO	S1	S2	CO		
L	L	L	L	L	L	L	H	L	L		
H	L	L	L	H	L	L	L	H	L		
L	H	L	L	H	L	L	L	H	L		
H	H	L	L	L	H	L	H	H	L		
L	L	H	L	L	H	L	H	H	L		
H	L	H	L	H	H	L	L	L	H		
L	H	H	L	H	H	L	L	L	H		
H	H	H	L	L	L	H	H	L	H		
L	L	H	H	L	L	H	H	L	H		
H	L	H	H	H	L	H	L	H	H		
L	H	H	H	H	L	H	L	H	H		
H	H	H	H	L	H	H	H	H	H		

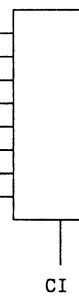
Cell Name

A2N

Equivalent Circuit



2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
A4H	4-bit Binary Full Adder with Fast Carry					48	
Cell Symbol	Propagation Delay Parameter						
	tup	KCL	t0	KCL	KCL2	CDR2	Path
 B4 — CO A4 — S4 B3 — A3 — S3 B2 — A2 — S2 B1 — A1 — S1 CI							
1.18	0.22	1.63	0.14				CI → S1
2.65	0.29	3.07	0.14				CI → S2
3.03	0.29	2.98	0.14				CI → S3
3.14	0.29	3.54	0.14				CI → S4
2.87	0.16	3.21	0.08				CI → CO
3.81	0.22	3.39	0.14				A1, B1 → S1
3.17	0.29	3.08	0.14				A1, B1 → S2
3.42	0.29	3.85	0.14				A1, B1 → S3
3.75	0.29	3.92	0.14				A1, B1 → S4
3.30	0.16	3.78	0.08				A1, B1 → CO
3.09	0.29	3.37	0.14				A2, B2 → S2
3.66	0.29	3.60	0.14				A2, B2 → S3
3.74	0.29	4.05	0.14				A2, B2 → S4
3.87	0.16	3.83	0.08				A2, B2 → CO
2.81	0.29	2.85	0.14				A3, B3 → S3
3.84	0.29	4.04	0.14				A3, B3 → S4
3.80	0.16	3.82	0.08				A3, B3 → CO
2.90	0.22	3.01	0.09	0.12			A4, B4 → S4
3.66	0.16	3.51	0.08		4		A4, B4 → CO
Pin Name	Input Loading Factor (ℓ_u)						
A	2						
B	2						
CI	2						
Pin Name	Output Driving Factor (ℓ_u)						
CO	18						
S1, S3, S4	14						
S2	18						

2

Function Table

INPUT				OUTPUT							
				CI = L		CI = H		L		H	
A1	B1	A2	B2	S1	S2	C2	S1	S2	C2	-	-
A3	B3	A4	B4	S3	S4	C0	S3	S4	C0	-	-
L	L	L	L	L	L	L	H	L	L		
H	L	L	L	H	L	L	L	H	L		
L	H	L	L	H	L	L	L	H	L		
H	H	L	L	L	H	L	H	H	L		
L	L	H	L	L	H	L	H	H	L		
H	L	H	L	H	H	L	L	L	H		
L	H	H	L	H	H	L	L	L	H		
H	H	H	L	L	L	H	H	L	L		
L	L	L	H	L	H	L	H	H	L		
H	L	L	H	H	H	H	L	L	L		
L	H	L	H	H	H	H	L	L	H		
H	H	L	H	L	L	H	H	L	L		
L	L	H	H	L	L	H	H	L	L		
H	L	H	H	H	H	L	L	H	L		
L	H	H	H	H	H	L	H	L	H		
H	H	H	H	L	H	H	H	H	H		

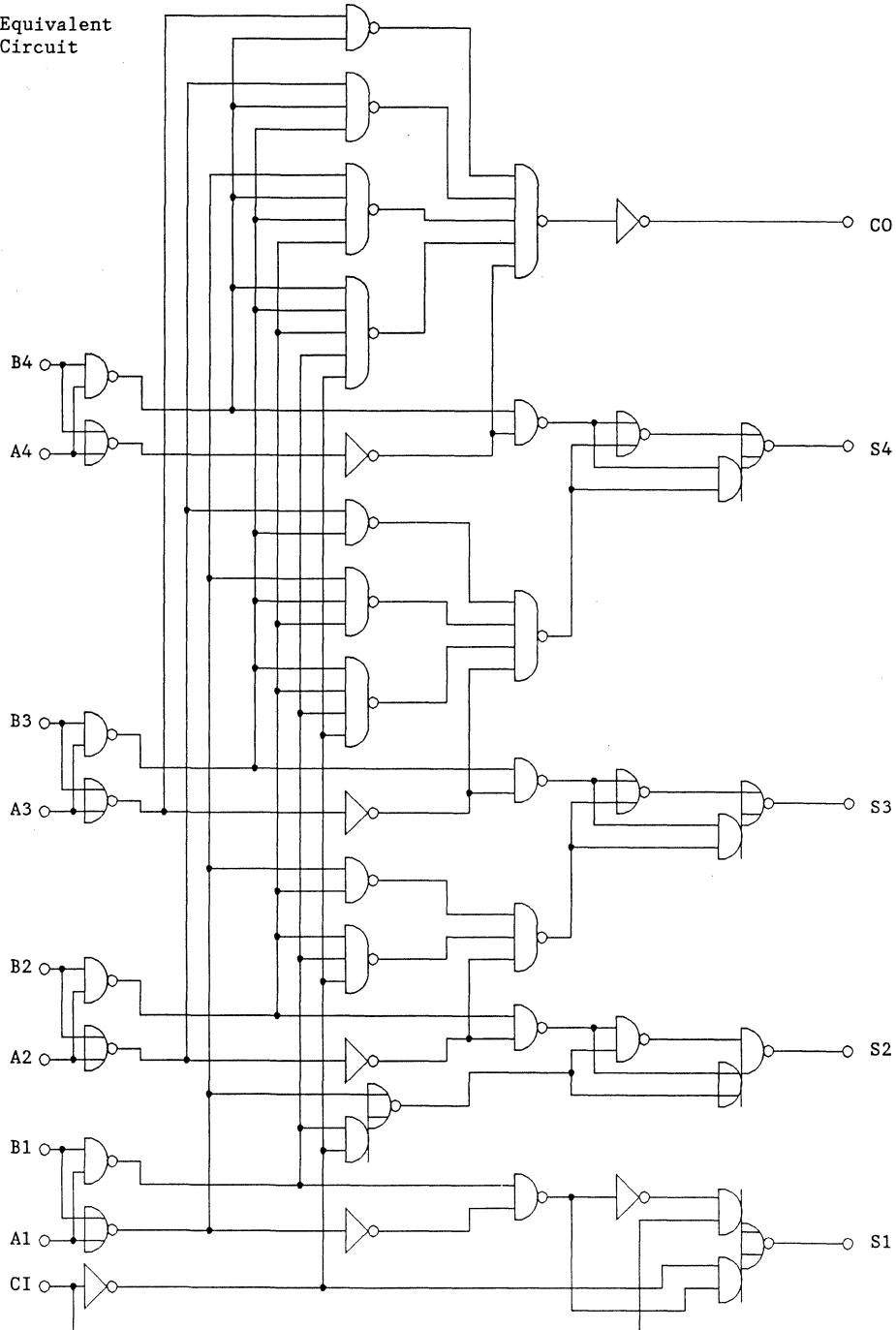
Note :

Input conditions at A1, A2, B1, B2 and CI are used to determine outputs S1 and S2 and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4 and CO.

Cell Name

A4H

Equivalent Circuit



2

Data Latch Family

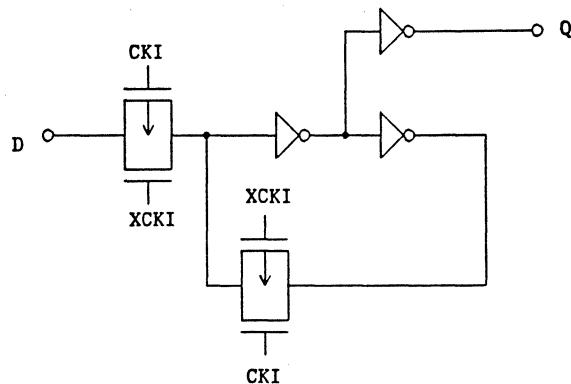
Page	Unit Cell Name	Function	Basic Cells
2-227	YL2	Data Latch with TM	5
2-229	YL4	Data Latch with TM	14
2-231	LTK	Data Latch	4
2-233	LTL	Data Latch with Clear	5
2-235	LTM	Data Latch with Clear	16
2-238	LT1	S-R Latch with Clear	4
2-240	LT4	Data Latch	14

2

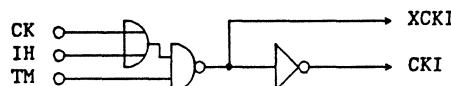
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version																																				
Cell Name	Function				Number of BC																																				
YL2	1-bit Data Latch with TM				5																																				
Cell Symbol		Propagation Delay Parameter																																							
		t _{up}	t _{dn}		Path CK,IH → Q D → Q																																				
		t ₀	KCL	t ₀																																					
		2.73	0.08	2.81	0.04	KCL2																																			
		1.16	0.08	1.28	0.04	CDR2																																			
Parameter					Symbol Typ(ns)*																																				
Clock Pulse Width					t _{CW} 6.8																																				
Data Setup Time					t _{SD} 3.2																																				
Data Hold Time					t _{HD} 2.5																																				
Pin Name		Input Loading Factor (f _u)																																							
D		2																																							
CK		1																																							
IH		1																																							
TM		1																																							
Pin Name		Output Driving Factor (f _u)																																							
Q		36																																							
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																																									
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Input				Output	Mode																																				
TM	IH	CK	D	Q																																					
L	X	X	D	D	SCAN																																				
H	H	X	X	Q _o																																					
H	X	H	X	Q _o	LATCH																																				
H	L	L	D	D																																					
UHB-YL2-E3 Sheet 1/2			Page 15-1																																						

Cell Name
YL2

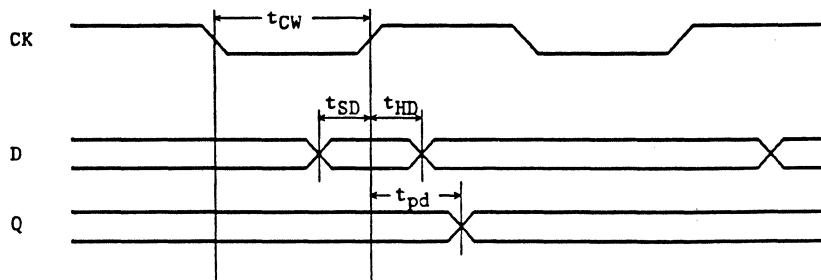
Equivalent Circuit



2



Definitions of Parameters

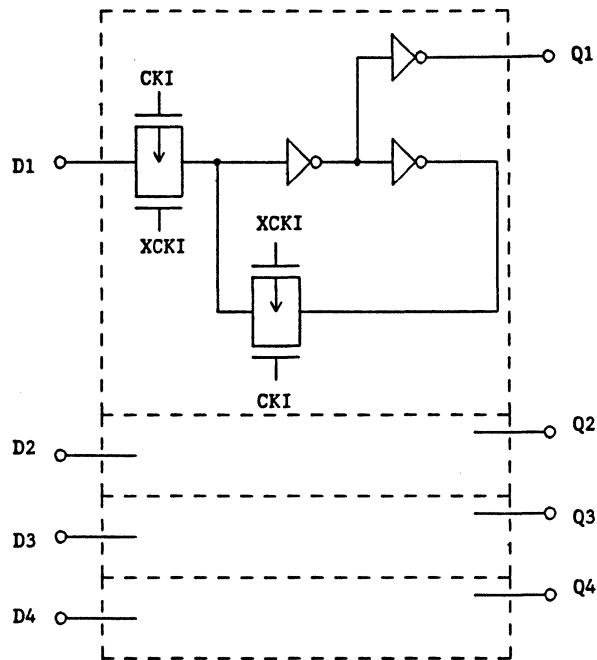


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version			
Cell Name	Function					Number of BC			
YL4	4-bit Data Latch with TM					14			
Cell Symbol	Propagation Delay Parameter								
	tup		tdn		Path				
	t0	KCL	t0	KCL	KCL2	CDR2			
	3.33 1.10	0.08 0.08	3.43 1.29	0.04 0.04					
D1 D2 D3 D4 CK IH TM	Q1 Q2 Q3 Q4								
Parameter				Symbol	Typ(ns)*				
Clock Pulse Width (CK)				tCW	7.2				
Data Setup Time (D)				tSD	1.8				
Data Hold Time (D)				tHD	4.0				
Pin Name	Input Loading Factor (f <u>A</u>)								
D	2								
CK	1								
IH	1								
TM	1								
Pin Name	Output Driving Factor (f <u>A</u>)								
Q	36								
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Note :									
The TM terminal must be kept LOW during the SCAN Mode.									
Function Table									
Input		Output		Mode					
TM	IH	CK	D _n	Q _n					
L	X	X	D	D	SCAN				
H	H	X	X	Q _{no}					
H	X	H	X	Q _{no}	LATCH				
H	L	L	D	D					
n = 1 ~ 4									
UHB-YL4-E3 Sheet 1/2									
Page 15-3									

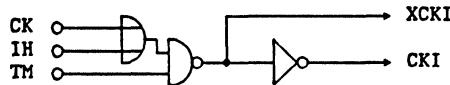
Cell Name

YL4

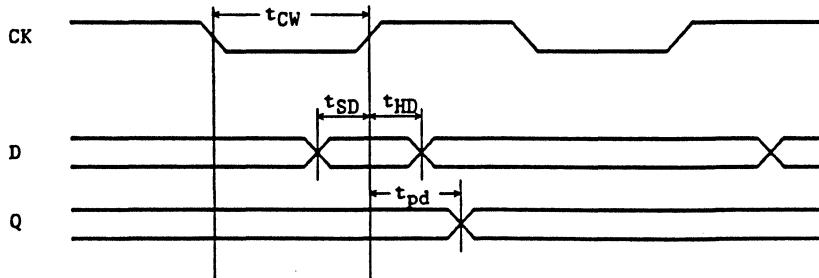
Equivalent Circuit

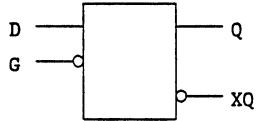


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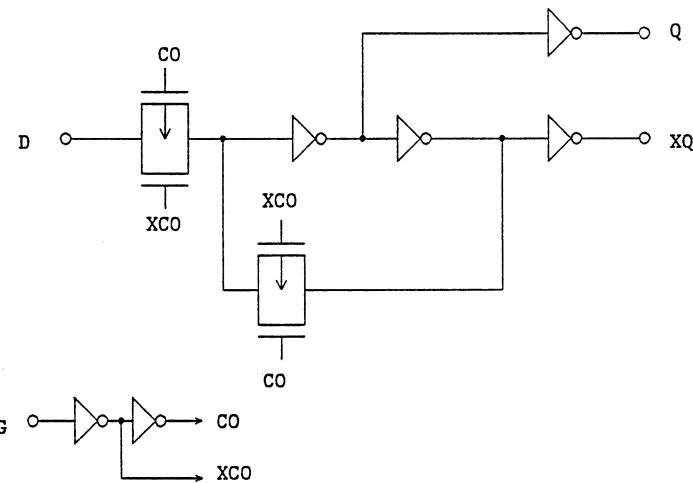
Definitions of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version												
Cell Name		Function					Number of BC												
LTK		Data Latch					4												
Cell Symbol		Propagation Delay Parameter																	
		tup	tdn																
		t0	KCL	t0	KCL	KCL2	CDR2												
		1.03	0.16	1.15	0.08		D → Q												
		1.45	0.16	1.63	0.08		D → XQ												
		1.75	0.16	1.82	0.08		G → Q												
		2.12	0.16	2.34	0.08		G → XQ												
		Parameter				Symbol	Typ(ns)*												
		G Input Pulse Width				tGW	4.0												
		Data Setup Time				tSD	1.6												
		Data Hold Time				tHD	2.3												
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (lu)</th></tr> </thead> <tbody> <tr> <td>D</td><td>2</td></tr> <tr> <td>G</td><td>1</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (lu)	D	2	G	1												
Pin Name	Input Loading Factor (lu)																		
D	2																		
G	1																		
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D	Q																		
G	XQ																		
<table border="1"> <tbody> <tr> <td>X</td><td>H</td><td>Q₀</td><td>XQ₀</td></tr> <tr> <td>H</td><td>L</td><td>H</td><td>L</td></tr> <tr> <td>L</td><td>L</td><td>L</td><td>H</td></tr> </tbody> </table>		X	H	Q ₀	XQ ₀	H	L	H	L	L	L	L	H						
X	H	Q ₀	XQ ₀																
H	L	H	L																
L	L	L	H																

Cell Name	
LTK	

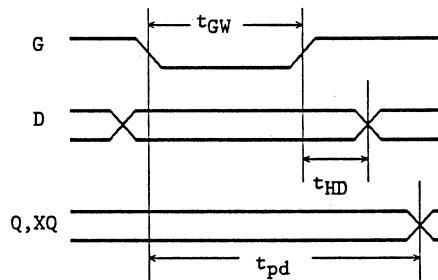
Equivalent Circuit



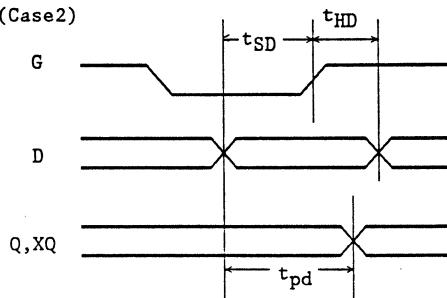
2

Definition of Parameters

(Case1)



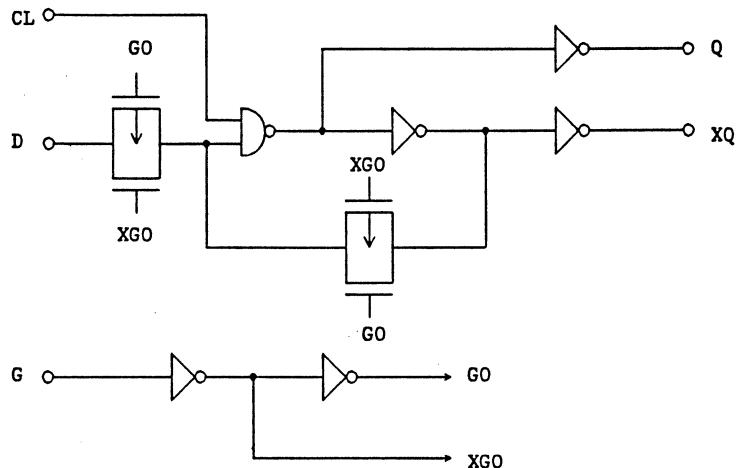
(Case2)



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																														
Cell Name	Function					Number of BC																														
LTL	1-bit Data Latch with Clear					5																														
Cell Symbol		Propagation Delay Parameter																																		
		tup	tdn			Path																														
		t0 KCL	t0 KCL	KCL2	LD2																															
		1.39 0.16	0.85 0.09			CL → Q, XQ																														
		1.18 0.16	1.22 0.09			D → Q																														
		1.52 0.16	1.71 0.09			D → XQ																														
		1.96 0.16	1.92 0.09			G → Q																														
		2.22 0.16	2.51 0.09			G → XQ																														
Parameter						Symbol																														
G Input Pulse Width						tGW																														
						4.0																														
Data Setup Time						tSD																														
Data Hold Time						tHD																														
Clear Pulse Width						tLW																														
						4.0																														
Pin Name	Input Loading Factor (λ_u)																																			
D	2																																			
G	1																																			
CL	1																																			
Pin Name	Output Driving Factor (λ_u)																																			
Q	18																																			
XQ	18																																			
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																																				
Funcion Table																																				
<table border="1"> <thead> <tr> <th colspan="3">Inputs</th> <th colspan="2">Outputs</th> </tr> <tr> <th>CL</th> <th>D</th> <th>G</th> <th>Q</th> <th>XQ</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>X</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>H</td> <td>Q_o</td> <td>XQ_o</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>L</td> <td>H</td> </tr> </tbody> </table>							Inputs			Outputs		CL	D	G	Q	XQ	L	X	H	L	H	H	X	H	Q _o	XQ _o	H	H	L	H	L	H	L	L	L	H
Inputs			Outputs																																	
CL	D	G	Q	XQ																																
L	X	H	L	H																																
H	X	H	Q _o	XQ _o																																
H	H	L	H	L																																
H	L	L	L	H																																
<small>UHB-LTL-E2 Sheet 1/2 Page 15-7</small>																																				

Cell Name	LTL
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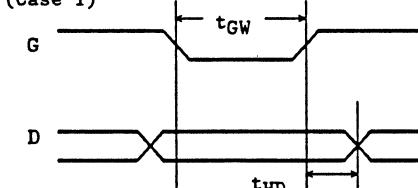
Equivalent Circuit



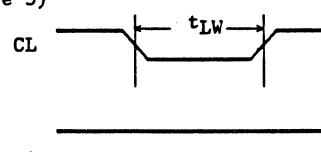
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Definition of Parameters

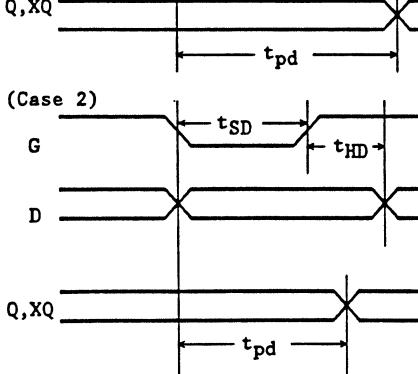
(Case 1)



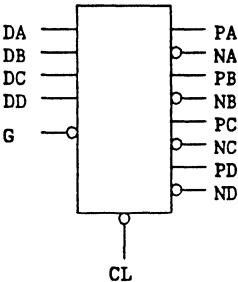
(Case 3)



(Case 2)

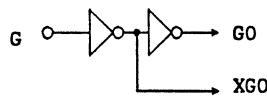
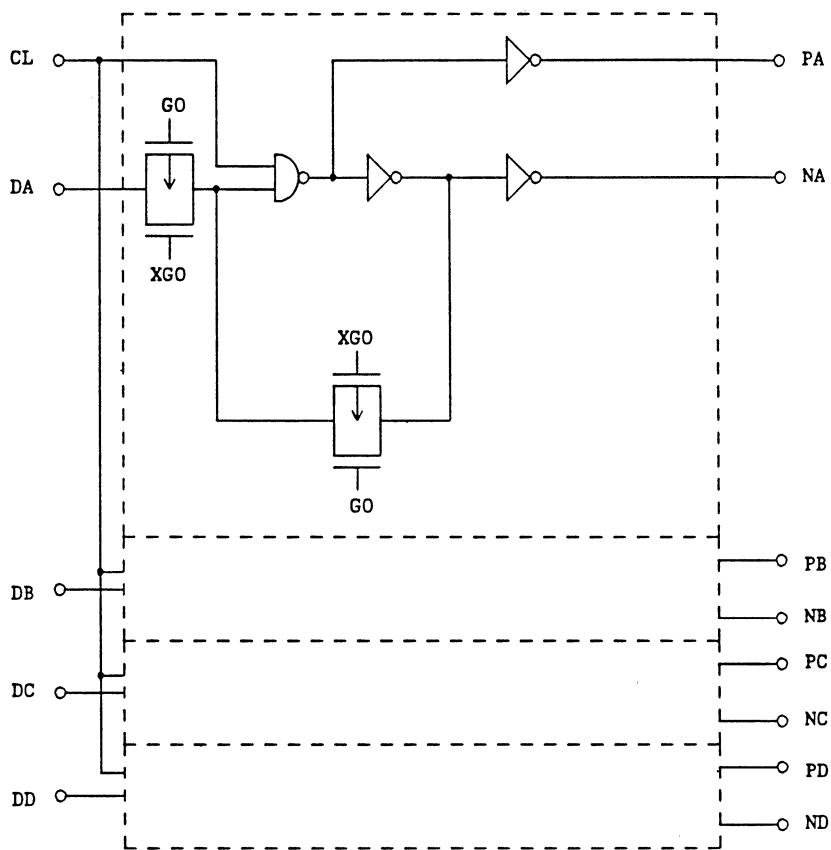


Note*: G input must be high level
at the time this latch
is cleared.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																					
Cell Name	Function			Number of BC																					
LTM	4-bit Data Latch with Clear			16																					
Cell Symbol	Propagation Delay Parameter																								
	t _{up}	KCL	t ₀	KCL	KCL2	CDR2	Path																		
	1.54	0.16	0.97	0.08			CL → P,N																		
	1.22	0.16	1.29	0.08			D → P																		
	1.60	0.16	1.79	0.08			D → N																		
	2.61	0.16	2.45	0.08			G → P																		
	2.73	0.16	3.15	0.08			G → N																		
	Parameter				Symbol	Typ(ns)*																			
	G Input Pulse Width				t _{GW}	4.0																			
	Clear Pulse Width				t _{LW}	4.0																			
	Data Setup Time				t _{SD}	1.6																			
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (f<u>u</u>)</th></tr> </thead> <tbody> <tr> <td>D</td><td>2</td></tr> <tr> <td>G</td><td>1</td></tr> <tr> <td>CL</td><td>4</td></tr> <tr> <td></td><td></td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (f<u>u</u>)</th></tr> </thead> <tbody> <tr> <td>P</td><td>18</td></tr> <tr> <td>N</td><td>18</td></tr> <tr> <td></td><td></td></tr> </tbody> </table>	Pin Name	Input Loading Factor (f <u>u</u>)	D	2	G	1	CL	4			Pin Name	Output Driving Factor (f <u>u</u>)	P	18	N	18			Data Hold Time				t _{HD}	2.3	
Pin Name	Input Loading Factor (f <u>u</u>)																								
D	2																								
G	1																								
CL	4																								
Pin Name	Output Driving Factor (f <u>u</u>)																								
P	18																								
N	18																								
				* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																					
				Function Table																					
Inputs		Outputs																							
CL	D	G	P	N																					
L	X	H	L	H																					
H	X	H	P _o	N _o																					
H	H	L	H	L																					
H	L	L	L	H																					

Cell Name
LTM

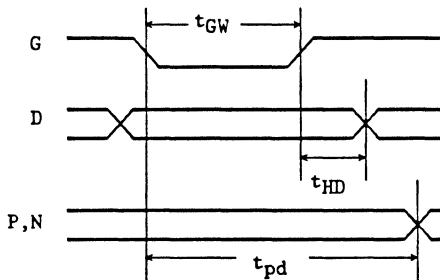
Equivalent Circuit



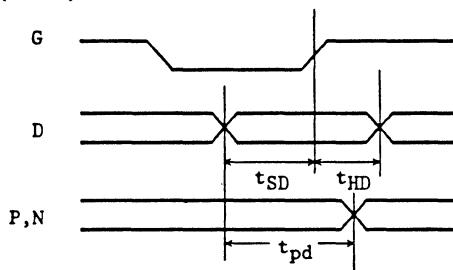
Cell Name
LTM

Definition of Parameters

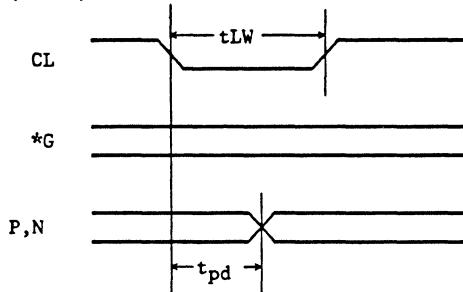
(Case1)



(Case2)



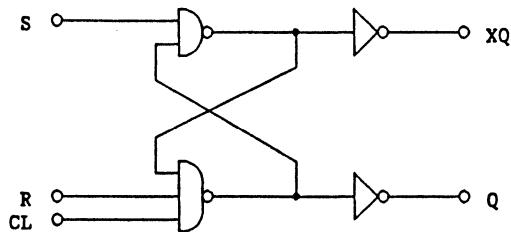
(Case3)



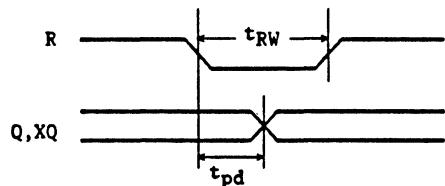
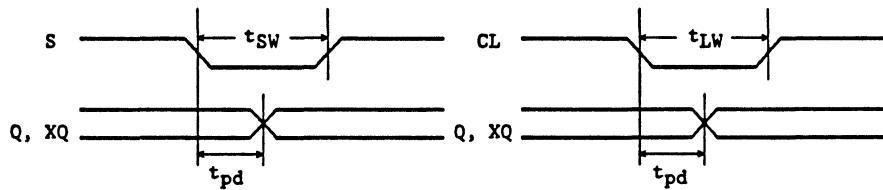
Note *: G input must be high level at the time this latch is cleared.

Cell Name
LT1

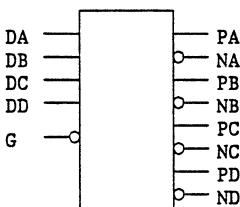
Equivalent Circuit



Definition of Parameters

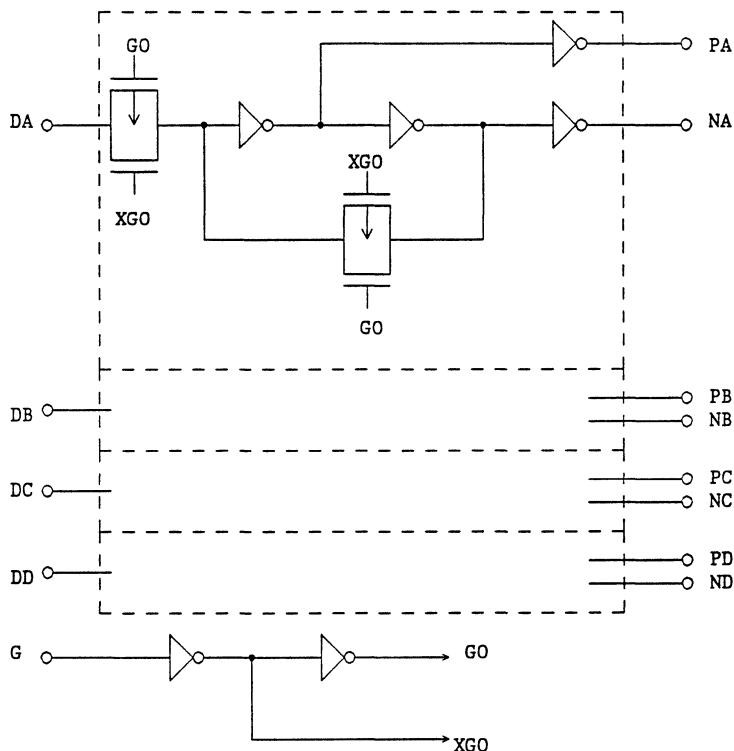


2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																						
Cell Name	Function					Number of BC																						
LT4	4-bit Data Latch					14																						
Cell Symbol		Propagation Delay Parameter																										
		t _{up}		t _{dn}																								
		t ₀	KCL	t ₀	KCL	KCL2	Path																					
		2.50	0.16	2.28	0.08		G → P																					
		2.50	0.16	3.05	0.08		G → N																					
		1.05	0.16	1.18	0.08		D → P																					
		1.40	0.16	1.60	0.08		D → N																					
Parameter						Symbol																						
G Input Pulse Width						t _{GW}																						
						4.0																						
Data Setup Time						t _{SD}																						
Data Hold Time						t _{HD}																						
						1.6																						
						2.3																						
Pin Name		Input Loading Factor (Ω_u)																										
D		2																										
G		1																										
Pin Name		Output Driving Factor (Ω_u)																										
P		18																										
N		18																										
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																												
Function Table																												
<table border="1"> <thead> <tr> <th>Inputs</th><th>Outputs</th></tr> <tr> <th>D</th><th>G</th><th>P</th><th>N</th></tr> </thead> <tbody> <tr> <td>H</td><td>H</td><td>P_o</td><td>N_o</td></tr> <tr> <td>L</td><td>H</td><td>P_o</td><td>N_o</td></tr> <tr> <td>H</td><td>L</td><td>H</td><td>L</td></tr> <tr> <td>L</td><td>L</td><td>L</td><td>H</td></tr> </tbody> </table>							Inputs	Outputs	D	G	P	N	H	H	P _o	N _o	L	H	P _o	N _o	H	L	H	L	L	L	L	H
Inputs	Outputs																											
D	G	P	N																									
H	H	P _o	N _o																									
L	H	P _o	N _o																									
H	L	H	L																									
L	L	L	H																									
UHB-LT4-E2 Sheet 1/3																												
Page 15-14																												

Cell Name
LT4

Equivalent Circuit

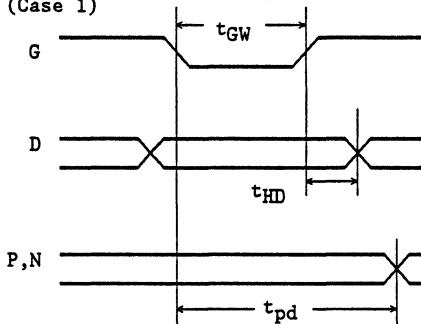


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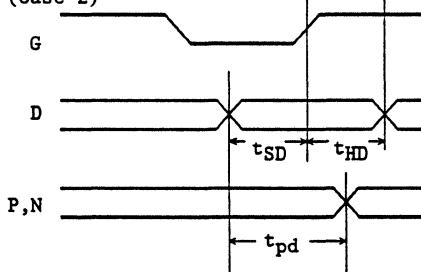
Cell Name
LT4

Definition of Parameters

(Case 1)



(Case 2)



Shift Register Family

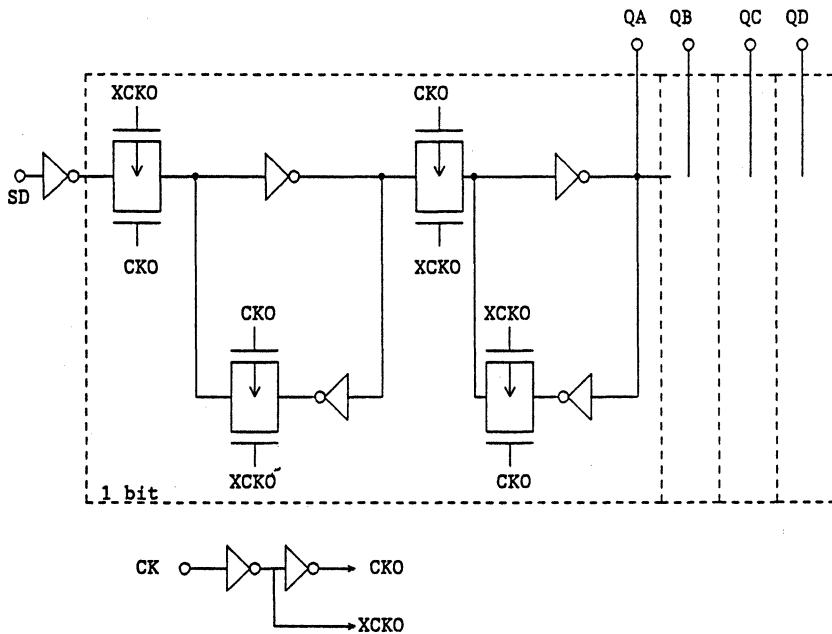
Page	Unit Cell Name	Function	Basic Cells
2-245	FS1	Serial-in Parallel-out Shift Register	18
2-247	FS2	Shift Register with Synchronous Load	30
2-249	FS3	Shift Register with Asynchronous Load	34
2-252	SR1	Serial-in Parallel-out Shift Register with Scan	36

2

2

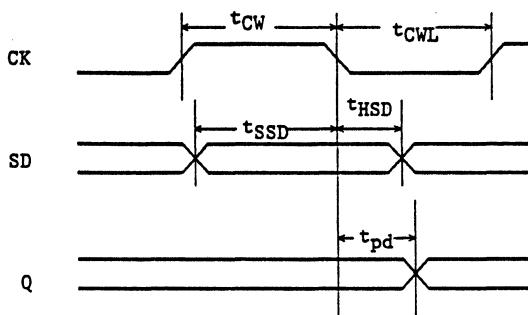
Cell Name	
FS1	

Equivalent Circuit



2

Definition of Parameters

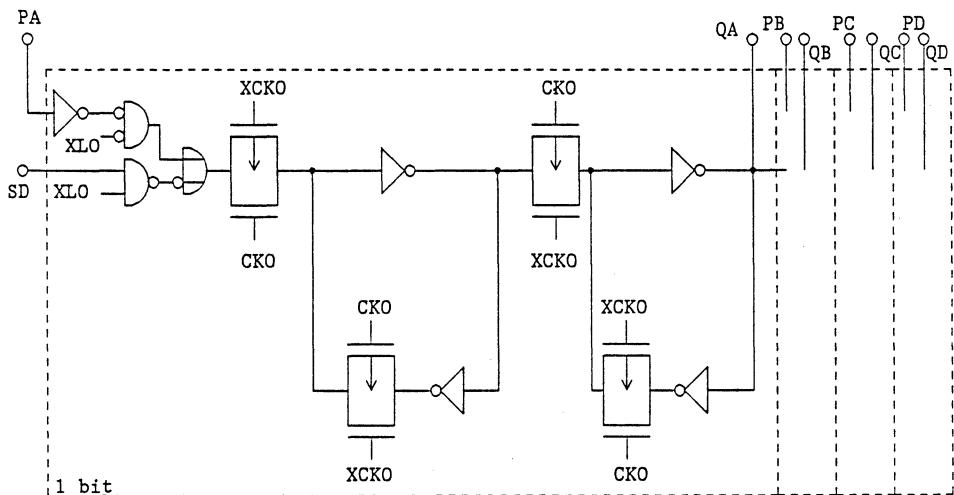


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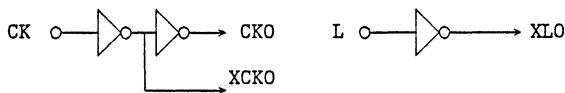
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version
Cell Name	Function						Number of BC
Cell Symbol	Propagation Delay Parameter						
		tup		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2
		2.32	0.16	3.14	0.09	0.12	4
						Path	
						CK + Q	

Cell Name	
FS2	

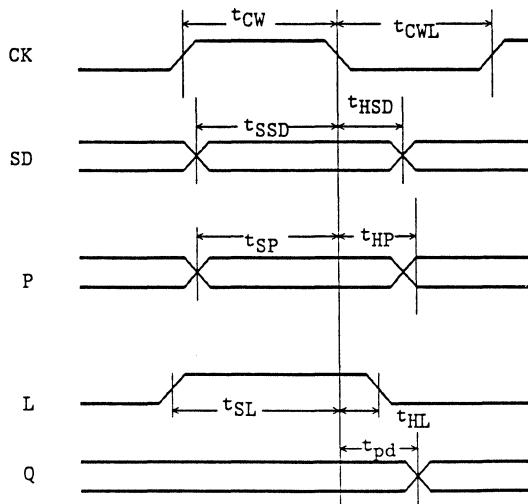
Equivalent Circuit

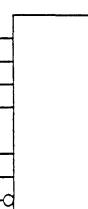


2



Definition of Parameters



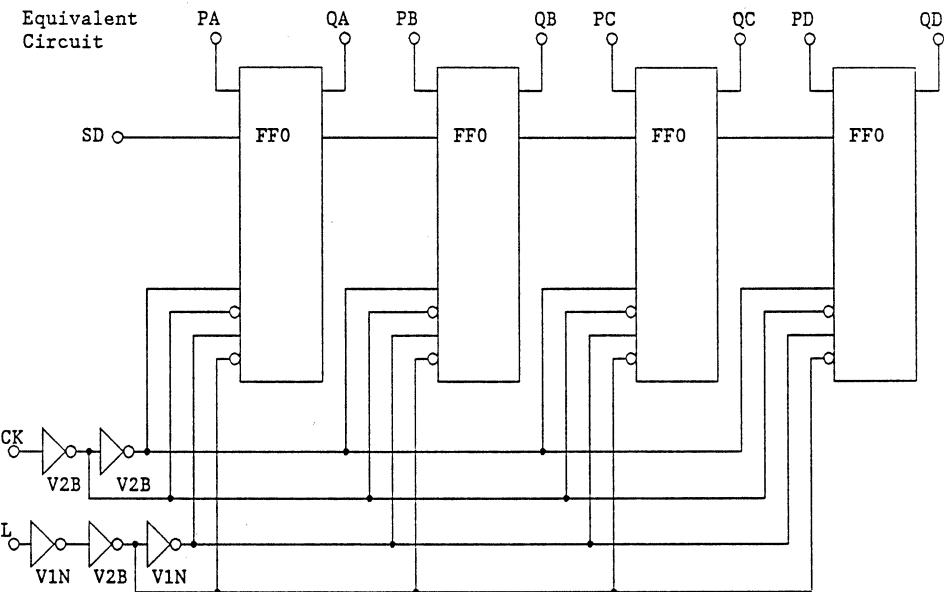
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version								
Cell Name	Function					Number of BC								
FS3	4-bit Shift Register with Asynchronous Load					34								
Cell Symbol	Propagation Delay Parameter													
 PA — QA PB — QB PC — QC PD — QD SD — CK — L — C		tup	tdn			Path								
		t0	KCL	t0	KCL	KCL2	CDR2	CK → Q L → Q P → Q						
		2.28	0.17	2.12	0.11									
		4.64	0.17	3.50	0.11									
		2.03	0.17	3.02	0.11									
Parameter						Symbol	Typ(ns)*							
Clock Pulse Width						tCW	4.0							
Clock Pause Time						tCWH	4.0							
Load Pulse Width						tLW	6.2							
SD Setup Time						tSSD	1.0							
SD Hold Time						tHSD	1.7							
Pin Name	Input Loading Factor (μ u)		P Setup Time	tSP		0.3								
			P Hold Time	tHP		2.3								
CK	2													
SD	2													
L	1													
P	2													
Pin Name	Output Driving Factor (μ u)													
	Q		18											
* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.														
Function Table														
Inputs		Output												
L	P	SD	CK	Q										
L	L	X	X	L										
L	H	X	X	H										
H	X	L	↑	L										
H	X	H	↑	H										

2

Function Table

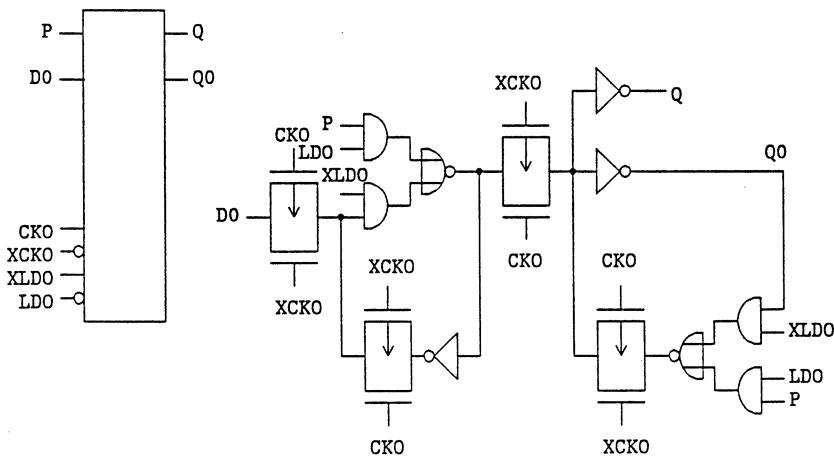
Inputs				Output
L	P	SD	CK	Q
L	L	X	X	L
L	H	X	X	H
H	X	L	↑	L
H	X	H	↑	H

Cell Name	FS3
-----------	-----



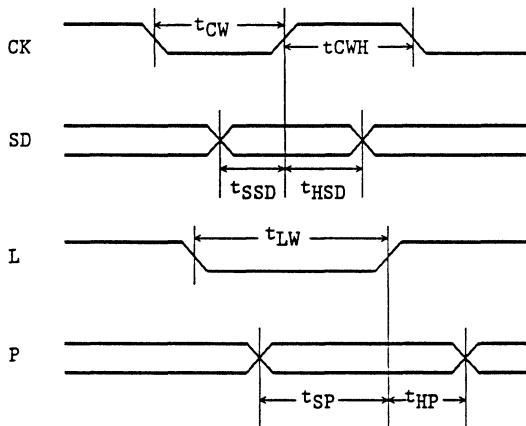
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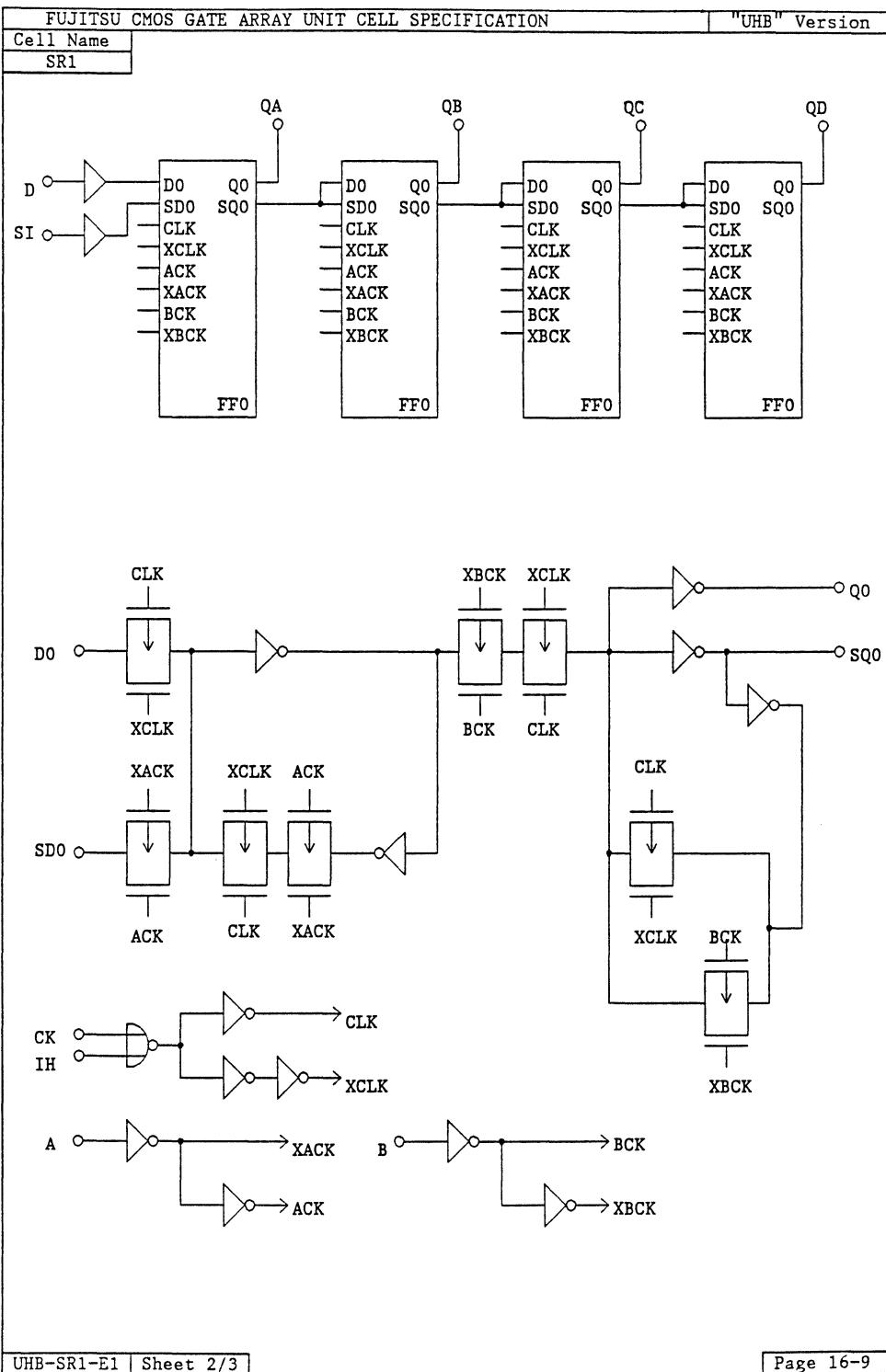
Equivalent Circuit of FF0



Cell Name
FS3

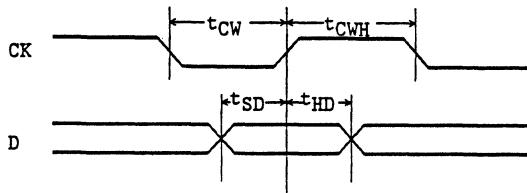
Definition of Parameters





Cell Name
SR1

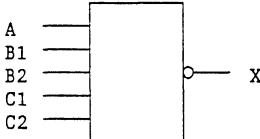
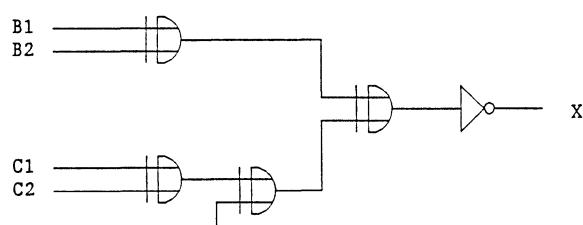
Definitions of Parameters

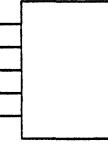
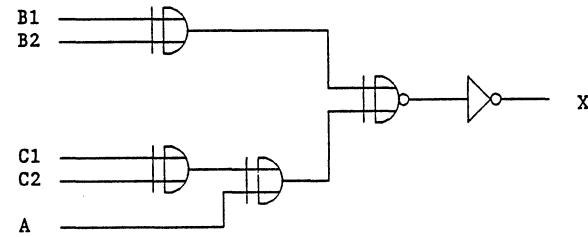


Parity Generator/Selector/Decoder Family

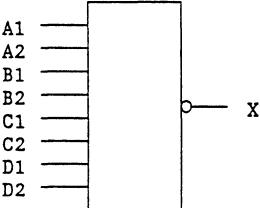
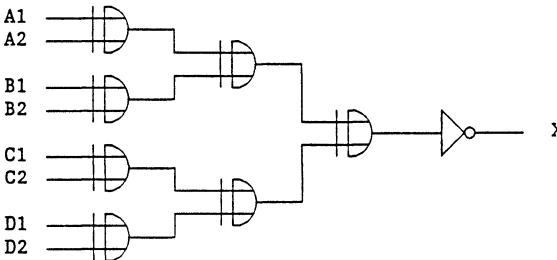
Page	Unit Cell Name	Function	Basic Cells
Parity Generators/Checkers			
2-257	PE5	Even Parity Generator/Checker	12
2-258	PO5	Odd Parity Generator/Checker	12
2-259	PE8	Even Parity Generator/Checker	18
2-260	PO8	Odd Parity Generator/Checker	18
2-261	PE9	Even Parity Generator/Checker	22
2-262	PO9	Odd Parity Generator/Checker	22
Data Selector			
2-263	P24	2:1 Data Selector	12
Decoders			
2-264	DE2	2:4 Decoder	5
2-265	DE3	3:8 Decoder	15
2-267	DE4	2:4 Decoder	8
2-268	DE6	3:8 Decoder	30
Selectors			
2-270	T2B	2:1 Selector	2
2-272	T2C	2:1 Selector	4
2-273	T2D	2:1 Selector	2
2-274	T2E	2:1 Selector	5
2-275	T2F	2:1 Selector	8
2-277	T5A	4:1 Selector	4
2-279	V3A	1:2 Selector	2
2-280	V3B	1:2 Selector	4
Magnitude Comparator			
2-281	MC4	Magnitude Comparator	42

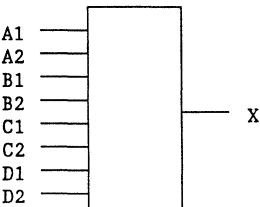
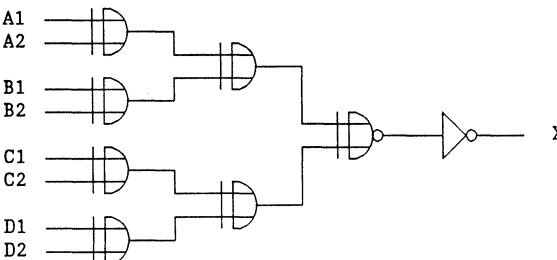
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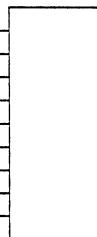
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version								
Cell Name	Function				Number of BC								
PE5	5-bit Even Parity Generator/Checker												
Cell Symbol		Propagation Delay Parameter											
		t _{up}	t _{dn}										
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	Path					
		2.62	0.08	3.41	0.04			A → X					
		2.62	0.08	3.27	0.04			B → X					
		4.14	0.08	4.83	0.04			C → X					
		Parameter			Symbol	Typ(ns)*							
Pin Name	Input Loading Factor (lu)												
	A	2											
	B	2											
Pin Name	Output Driving Factor (lu)												
	X	36											
			* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Function Table			Equivalent Circuit										
<table border="1"> <tr> <td>Σinput</td><td>X</td></tr> <tr> <td>Odd</td><td>L</td></tr> <tr> <td>Even</td><td>H</td></tr> </table>		Σ input	X	Odd	L			Even	H				
Σ input	X												
Odd	L												
Even	H												
UHB-PE5-E1 Sheet 1/1			Page 17-1										

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version							
Cell Name	Function	Number of BC									
Cell Symbol	Propagation Delay Parameter										
	t_{up}	t_{dn}									
	t ₀	KCL	t ₀	KCL	KCL2	CDR2	Path				
	2.63	0.08	3.07	0.04			A → X				
	2.86	0.08	3.04	0.04			B → X				
	4.19	0.08	4.56	0.04			C → X				
Parameter				Symbol	Typ(ns)*						
Pin Name	Input Loading Factor (ℓ_u)										
	A	2									
	B	2									
Pin Name	Output Driving Factor (ℓ_u)										
	X	36									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.											
Function Table			Equivalent Circuit								
<table border="1"> <tr> <td>Σinput</td><td>X</td></tr> <tr> <td>Odd</td><td>H</td></tr> <tr> <td>Even</td><td>L</td></tr> </table>			Σ input	X	Odd	H	Even	L			
Σ input	X										
Odd	H										
Even	L										

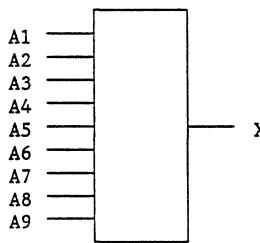
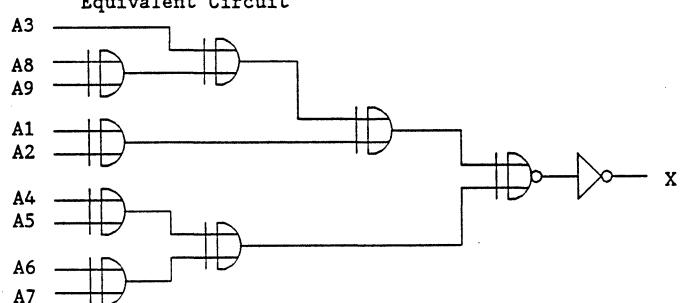
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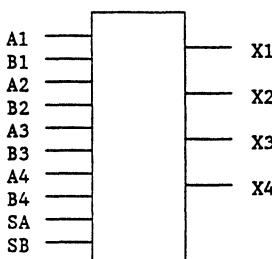
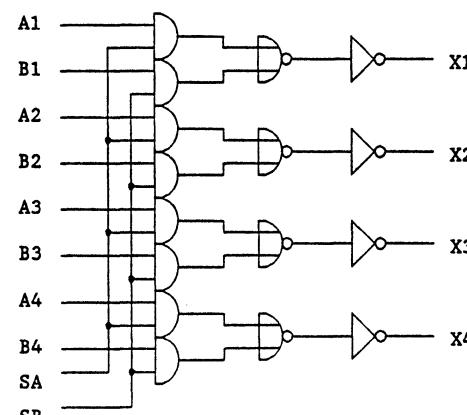
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version								
Cell Name	Function				Number of BC								
PE8	8-bit Even Parity Generator/Checker												
Cell Symbol		Propagation Delay Parameter											
		tup	tdn			Path							
		t0	KCL	t0	KCL	KCL2	CDR2						
		3.85	0.16	4.33	0.08			A → X					
		3.94	0.16	4.42	0.08			B → X					
		3.93	0.16	4.40	0.08			C → X					
		4.02	0.16	4.49	0.08			D → X					
		Parameter			Symbol	Typ(ns)*							
Pin Name		Input Loading Factor (λu)											
A		2											
B		2											
C		2											
D		2											
Pin Name		Output Driving Factor (λu)											
X		18											
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.													
Function Table			Equivalent Circuit										
<table border="1"> <tr> <td>Σinput</td><td>X</td></tr> <tr> <td>Odd</td><td>L</td></tr> <tr> <td>Even</td><td>H</td></tr> </table>		Σ input	X	Odd	L	Even	H						
Σ input	X												
Odd	L												
Even	H												
UHB-PE8-E1 Sheet 1/1			Page 17-3										

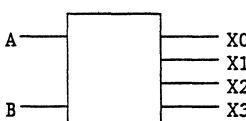
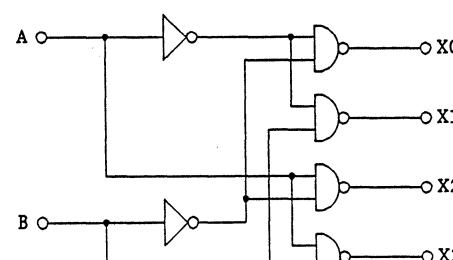
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version							
Cell Name	Function	Number of BC									
P08	8-bit Odd Parity Generator/Checker										
Cell Symbol		Propagation Delay Parameter									
		tup	tdn								
		t0	KCL	t0	KCL						
		3.77	0.16	4.28	0.08						
		3.86	0.16	4.37	0.08						
		3.87	0.16	4.17	0.08						
		3.96	0.16	4.26	0.08						
		Path									
		A → X									
		B → X									
		C → X									
		D → X									
		Parameter									
		Symbol									
		Typ(ns)*									
Pin Name		Input Loading Factor (ℓ_u)									
A		2									
B		2									
C		2									
D		2									
Pin Name		Output Driving Factor (ℓ_u)									
X		18									
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>											
Function Table			Equivalent Circuit								
<table border="1"> <tr> <td>Σinput</td><td>X</td></tr> <tr> <td>Odd</td><td>H</td></tr> <tr> <td>Even</td><td>L</td></tr> </table>		Σ input				X	Odd	H	Even	L	
Σ input	X										
Odd	H										
Even	L										
UHB-P08-E2 Sheet 1/1			Page 17-4								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version	
Cell Name	Function	Number of BC	
PE9	9-bit Even Parity Generator/Checker	22	
Cell Symbol	Propagation Delay Parameter		
	tup	tdn	Path A → X
	t0	KCL	
	5.29	0.16	
		5.71	
		0.08	
		KCL2	
		CDR2	
Parameter		Symbol	
		Typ(ns)*	
Pin Name	Input Loading Factor (ℓu)		
A	2		
Pin Name	Output Driving Factor (ℓu)		
X	18		
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			
Function Table		Equivalent Circuit	
Σ input	X	A3	
Odd	L	A8	
Even	H	A9	
		A1	
		A2	
		A4	
		A5	
		A6	
		A7	

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"UHB" Version																									
Cell Name	Function	Number of BC																									
P09	9-bit Odd Parity Generator/Checker	22																									
Cell Symbol	Propagation Delay Parameter																										
	<table border="1"> <thead> <tr> <th>tup</th> <th>tdn</th> <th></th> <th></th> <th></th> <th></th> <th></th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> <th>KCL2</th> <th>CDR2</th> <th>Path</th> </tr> </thead> <tbody> <tr> <td>5.20</td> <td>0.16</td> <td>5.71</td> <td>0.08</td> <td></td> <td></td> <td>A → X</td> </tr> </tbody> </table>						tup	tdn						t0	KCL	t0	KCL	KCL2	CDR2	Path	5.20	0.16	5.71	0.08			A → X
tup	tdn																										
t0	KCL	t0	KCL	KCL2	CDR2	Path																					
5.20	0.16	5.71	0.08			A → X																					
																											
Pin Name	Input Loading Factor (λ_u)																										
A	2																										
Pin Name	Output Driving Factor (λ_u)																										
X	18																										
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Function Table		Equivalent Circuit																									
<table border="1"> <tr> <td>Σinput</td> <td>X</td> </tr> <tr> <td>Odd</td> <td>H</td> </tr> <tr> <td>Even</td> <td>L</td> </tr> </table>	Σ input	X	Odd	H	Even	L																					
Σ input	X																										
Odd	H																										
Even	L																										

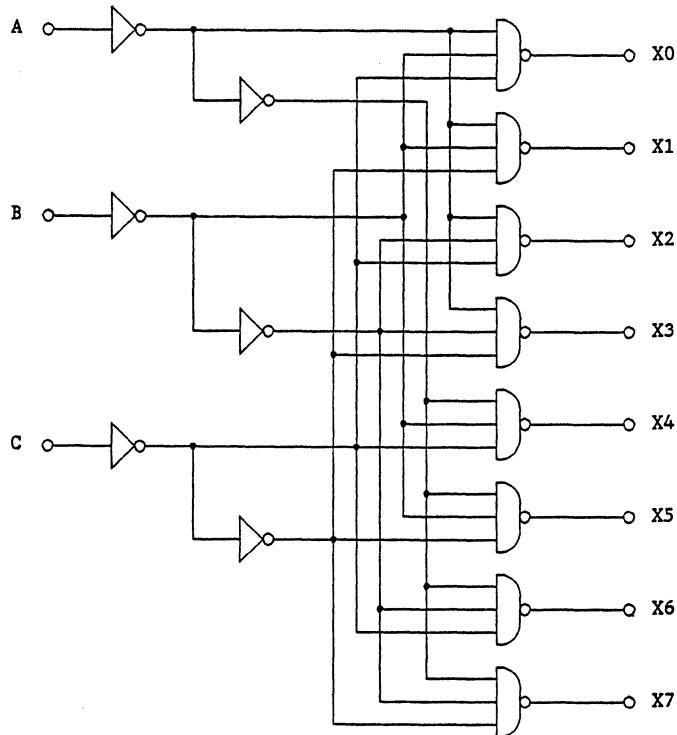
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																		
Cell Name	Function	Number of BC																				
P24	4-wide 2:1 Data Selector																					
Cell Symbol		Propagation Delay Parameter																				
		t _{up}	t _{dn}																			
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	Path														
		0.95	0.08	0.83	0.04			A → X														
		1.16	0.08	0.97	0.04			B → X														
		0.81	0.08	0.95	0.04			SA → X														
		1.00	0.08	1.08	0.04			SB → X														
		Parameter			Symbol	Typ(ns)*																
Pin Name		Input Loading Factor (f <u>u</u>)																				
A		1																				
B		1																				
S		4																				
Pin Name		Output Driving Factor (f <u>u</u>)																				
X		36																				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																						
Function Table			Equivalent Circuit																			
<table border="1"> <tr> <th>SA</th><th>SB</th><th>Xn</th></tr> <tr> <td>L</td><td>L</td><td>L</td></tr> <tr> <td>H</td><td>L</td><td>An</td></tr> <tr> <td>L</td><td>H</td><td>Bn</td></tr> <tr> <td>H</td><td>H</td><td>An+Bn</td></tr> </table>			SA	SB	Xn	L	L	L	H	L	An	L	H	Bn	H	H	An+Bn					
SA	SB	Xn																				
L	L	L																				
H	L	An																				
L	H	Bn																				
H	H	An+Bn																				
UHB-P24-E2 Sheet 1/1			Page 17-7																			

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																																				
Cell Name	Function					Number of BC																																				
DE2	2:4 Decoder					5																																				
Cell Symbol		Propagation Delay Parameter																																								
		tup	tdn	t0	KCL	KCL2	Path																																			
		0.79	0.16	1.08	0.14		A → X0																																			
		0.88	0.16	0.97	0.14		A → X1																																			
		0.37	0.16	0.45	0.14		A → X2, X3																																			
		0.88	0.16	0.97	0.14		B → X0																																			
		0.28	0.16	0.56	0.14		B → X1, X3																																			
		0.79	0.16	1.08	0.14		B → X2																																			
Parameter						Symbol																																				
						Typ(ns)*																																				
Pin Name		Input Loading Factor (ℓ_u)																																								
A		3																																								
B		3																																								
Pin Name		Output Driving Factor (ℓ_u)																																								
X		18																																								
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Function Table																																										
<table border="1"> <thead> <tr> <th colspan="2">Inputs</th> <th colspan="4">Outputs</th> </tr> <tr> <th>A</th> <th>B</th> <th>X3</th> <th>X2</th> <th>X1</th> <th>X0</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>H</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>H</td> <td>H</td> <td>H</td> </tr> </tbody> </table>							Inputs		Outputs				A	B	X3	X2	X1	X0	L	L	H	H	H	L	L	H	H	H	L	H	H	L	H	L	H	H	H	H	L	H	H	H
Inputs		Outputs																																								
A	B	X3	X2	X1	X0																																					
L	L	H	H	H	L																																					
L	H	H	H	L	H																																					
H	L	H	L	H	H																																					
H	H	L	H	H	H																																					
																																										
UHB-DE2-E2 Sheet 1/1																																										
Page 17-8																																										

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version							
Cell Name	Function	Number of BC												
DE3	3:8 Decoder													
Cell Symbol		Propagation Delay Parameter												
		tup			tdn		Path							
		t0	KCL	t0	KCL	KCL2	CDR2							
		1.44	0.16	1.67	0.19			A → X0~X3						
		2.44	0.16	2.44	0.19			A → X4~X7						
		1.33	0.16	1.72	0.19			B → X0~X3						
		2.33	0.16	2.49	0.19			B → X4~X7						
		1.23	0.16	1.78	0.19			C → X0~X3						
		2.23	0.16	2.55	0.19			C → X4~X7						
Parameter							Symbol	Typ(ns)*						
Pin Name	Input Loading Factor (λ_u)													
	A	1												
	B	1												
Pin Name	Output Driving Factor (λ_u)													
	X	14												
	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.													
Function Table														
Inputs			Outputs											
A	B	C	X0	X1	X2	X3	X4	X5	X6	X7				
L	L	L	L	H	H	H	H	H	H	H				
L	L	H	H	L	H	H	H	H	H	H				
L	H	L	H	H	L	H	H	H	H	H				
L	H	H	H	H	H	L	H	H	H	H				
H	L	L	H	H	H	H	L	H	H	H				
H	L	H	H	H	H	H	H	L	H	H				
H	H	L	H	H	H	H	H	H	L	H				
H	H	H	H	H	H	H	H	H	H	L				

Cell Name
DE3

Equivalent Circuit

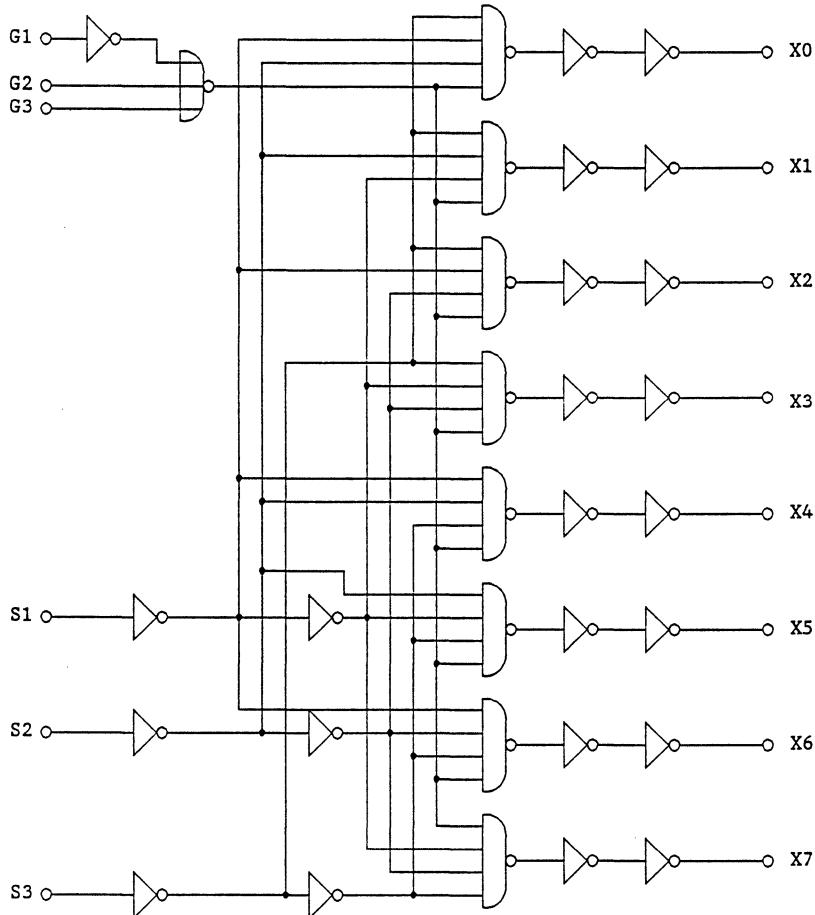


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																																										
Cell Name	Function						Number of BC																																										
DE4	2:4 Decoder with Enable						8																																										
Cell Symbol	Propagation Delay Parameter																																																
		<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="4">tdn</th><th></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th><th>Path</th></tr> </thead> <tbody> <tr> <td>1.19</td><td>0.16</td><td>1.46</td><td>0.19</td><td></td><td></td><td>G → X</td></tr> <tr> <td>0.86</td><td>0.16</td><td>1.11</td><td>0.19</td><td></td><td></td><td>A → X</td></tr> <tr> <td>1.07</td><td>0.16</td><td>1.14</td><td>0.19</td><td></td><td></td><td>B → X</td></tr> </tbody> </table>						tup		tdn					t0	KCL	t0	KCL	KCL2	CDR2	Path	1.19	0.16	1.46	0.19			G → X	0.86	0.16	1.11	0.19			A → X	1.07	0.16	1.14	0.19			B → X							
tup		tdn																																															
t0	KCL	t0	KCL	KCL2	CDR2	Path																																											
1.19	0.16	1.46	0.19			G → X																																											
0.86	0.16	1.11	0.19			A → X																																											
1.07	0.16	1.14	0.19			B → X																																											
		<table border="1"> <thead> <tr> <th colspan="3">Parameter</th><th>Symbol</th><th>Typ(ns)*</th></tr> </thead> <tbody> <tr> <td colspan="3"></td><td></td><td></td></tr> </tbody> </table>					Parameter			Symbol	Typ(ns)*																																						
Parameter			Symbol	Typ(ns)*																																													
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (ℓu)</th></tr> </thead> <tbody> <tr> <td>A</td><td>3</td></tr> <tr> <td>B</td><td>3</td></tr> <tr> <td>G</td><td>1</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓu)	A	3	B	3	G	1																																								
Pin Name	Input Loading Factor (ℓu)																																																
A	3																																																
B	3																																																
G	1																																																
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (ℓu)</th></tr> </thead> <tbody> <tr> <td>X</td><td>14</td></tr> </tbody> </table>		Pin Name	Output Driving Factor (ℓu)	X	14																																												
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Function Table				Equivalent Circuit																																													
<table border="1"> <thead> <tr> <th>G</th><th>A</th><th>B</th><th>X3</th><th>X2</th><th>X1</th><th>X0</th></tr> </thead> <tbody> <tr> <td>H</td><td>X</td><td>X</td><td>H</td><td>H</td><td>H</td><td>H</td></tr> <tr> <td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>L</td></tr> <tr> <td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>L</td><td>H</td></tr> <tr> <td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>H</td></tr> <tr> <td>L</td><td>H</td><td>H</td><td>L</td><td>H</td><td>H</td><td>H</td></tr> </tbody> </table>		G	A					B	X3	X2	X1	X0	H	X	X	H	H	H	H	L	L	L	H	H	H	L	L	L	H	H	H	L	H	L	H	L	H	L	H	H	L	H	H	L	H	H	H		
G	A	B	X3	X2	X1	X0																																											
H	X	X	H	H	H	H																																											
L	L	L	H	H	H	L																																											
L	L	H	H	H	L	H																																											
L	H	L	H	L	H	H																																											
L	H	H	L	H	H	H																																											
UHB-DE4-E2 Sheet 1/1		Page 17-11																																															

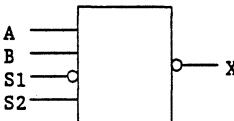
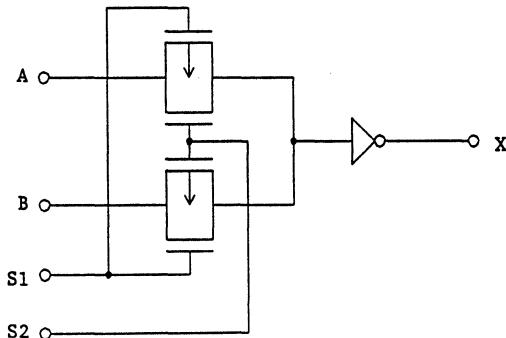
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version							
Cell Name	Function						Number of BC							
DE6	3:8 Decoder with Enable						30							
Cell Symbol		Propagation Delay Parameter												
		tup		tdn			Path							
		t0	KCL	t0	KCL	KCL2	CDR2							
		3.05	0.16	5.95	0.08			G → X						
		2.89	0.16	3.28	0.08			S → X						
		Parameter						Symbol						
								Typ(ns)*						
Pin Name		Input Loading Factor (f <u>u</u>)												
G		1												
S		1												
Pin Name		Output Driving Factor (f <u>u</u>)												
X		18												
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>														
Function Table														
G1	G2+G3	S3	S2	S1	X7	X6	X5	X4	X3	X2	X1	X0		
X	H	X	X	X	H	H	H	H	H	H	H	H		
L	X	X	X	X	H	H	H	H	H	H	H	H		
H	L	L	L	L	H	H	H	H	H	H	L	H		
H	L	L	L	H	H	H	H	H	H	L	H	H		
H	L	L	H	H	H	H	H	H	L	H	H	H		
H	L	H	L	L	H	H	H	L	H	H	H	H		
H	L	H	L	H	H	H	H	L	H	H	H	H		
H	L	H	H	L	H	L	H	H	H	H	H	H		
H	L	H	H	H	L	H	H	H	H	H	H	H		

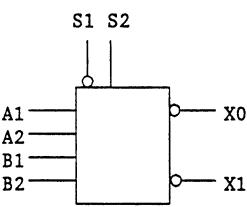
Cell Name
DE6

Equivalent Circuit



2

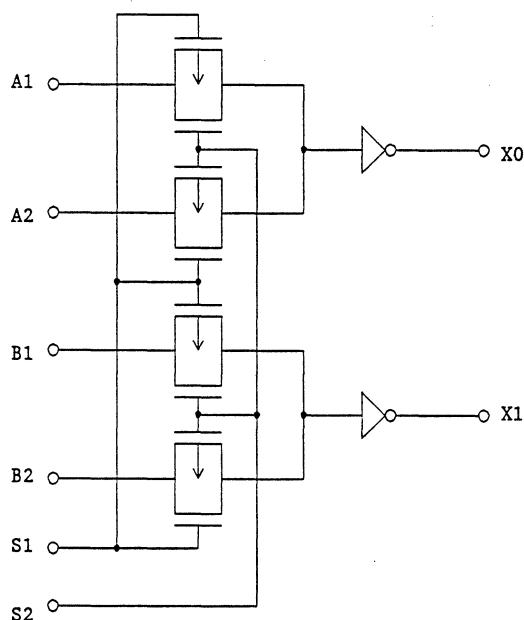
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version																																																		
Cell Name	Function				Number of BC																																																		
T2B	2:1 Selector				2																																																		
Cell Symbol		Propagation Delay Parameter																																																					
		tup	tdn																																																				
		t0	KCL	t0	KCL																																																		
		0.52	0.16	0.78	0.09																																																		
		0.61	0.16	0.99	0.09																																																		
			KCL2		CDR2																																																		
					Path																																																		
					A,B → X S → X																																																		
		Parameter																																																					
		Symbol			Typ(ns)*																																																		
Pin Name		Input Loading Factor (lu)																																																					
A,B		2																																																					
S		1																																																					
Pin Name		Output Driving Factor (lu)																																																					
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Function Table			Equivalent Circuit																																																				
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Inputs				Output																																																			
A	B	S1	S2	X																																																			
L	X	L	H	H																																																			
H	X	L	H	L																																																			
X	L	H	L	H																																																			
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UHB-T2B-E2 Sheet 1/1																																																							
Page 17-14																																																							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																
Cell Name	Function					Number of BC																
T2C	Dual 2:1 Selector					4																
Cell Symbol	Propagation Delay Parameter																					
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tup		tdn																				
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Parameter				Symbol	Typ(ns)*																	
Pin Name		Input Loading Factor (lu)																				
A,B	S	2																				
Pin Name		Output Driving Factor (lu)																				
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Inputs		Outputs																				
A1,B1	A2,B2	S1	S2	X0	X1																	
L	X	L	H	H	H																	
H	X	L	H	L	L																	
X	L	H	L	H	H																	
X	H	H	L	L	L																	
L	H	L	L	Inhibit	Inhibit																	
H	L	L	L	Inhibit	Inhibit																	
L	H	H	H	Inhibit	Inhibit																	
H	L	H	H	Inhibit	Inhibit																	

Cell Name

T2C

Equivalent Circuit



2

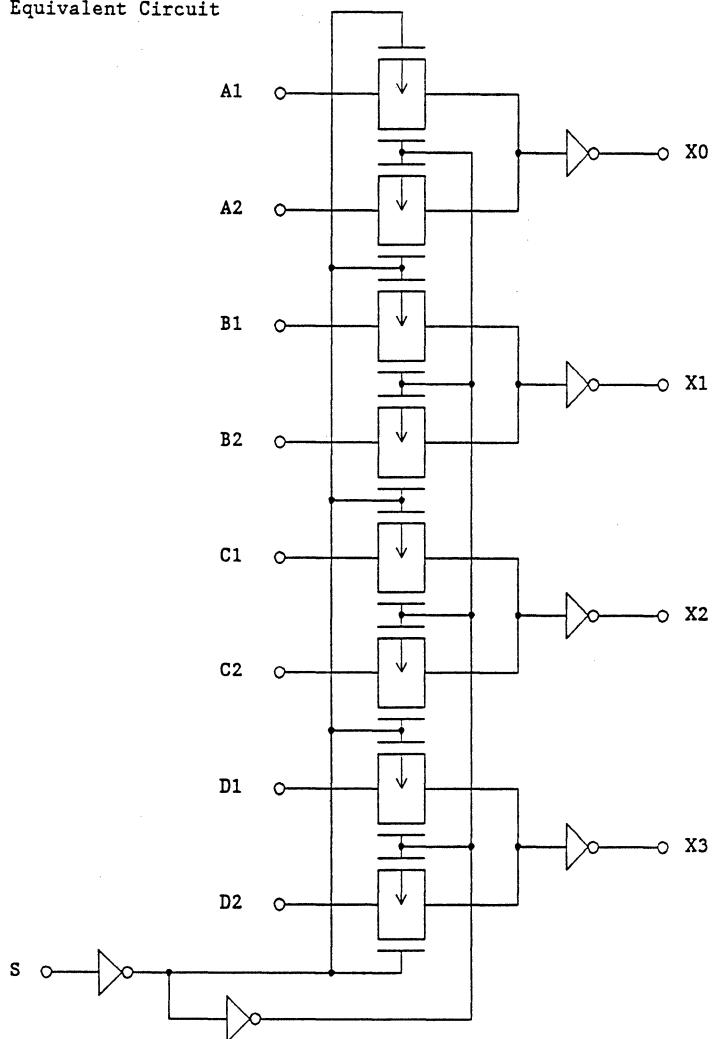
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T2D	2:1 Selector					2																																																																						
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		0.67	0.18	0.51	0.12																																																																							
		Parameter			Symbol	Typ(ns)*																																																																						
Pin Name	Input Loading Factor (ℓu)																																																																											
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Pin Name	Output Driving Factor (ℓu)																																																																											
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version							
Cell Name	Function	Number of BC									
T2E	Dual 2:1 Selector	5									
Cell Symbol	Propagation Delay Parameter										
	tup	tdn									
	t0	KCL	t0	KCL	KCL2	CDR2	Path				
A1 A2 B1 B2 S	0.54 1.64	0.16 0.16	0.54 1.62	0.10 0.10	0.14 0.14	4 4	A,B → X S → X				
Pin Name	Parameter				Symbol	Typ(ns)*					
A,B S											
Pin Name	Output Driving Factor (f <u>u</u>)										
X	18										
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Equivalent Circuit											

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																								
Cell Name	Function						Number of BC																								
T2F	2:1 Selector						8																								
Cell Symbol		Propagation Delay Parameter																													
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UHB-T2F-E1		Sheet 1/2						Page 17-19																							

Cell Name
T2F

Equivalent Circuit



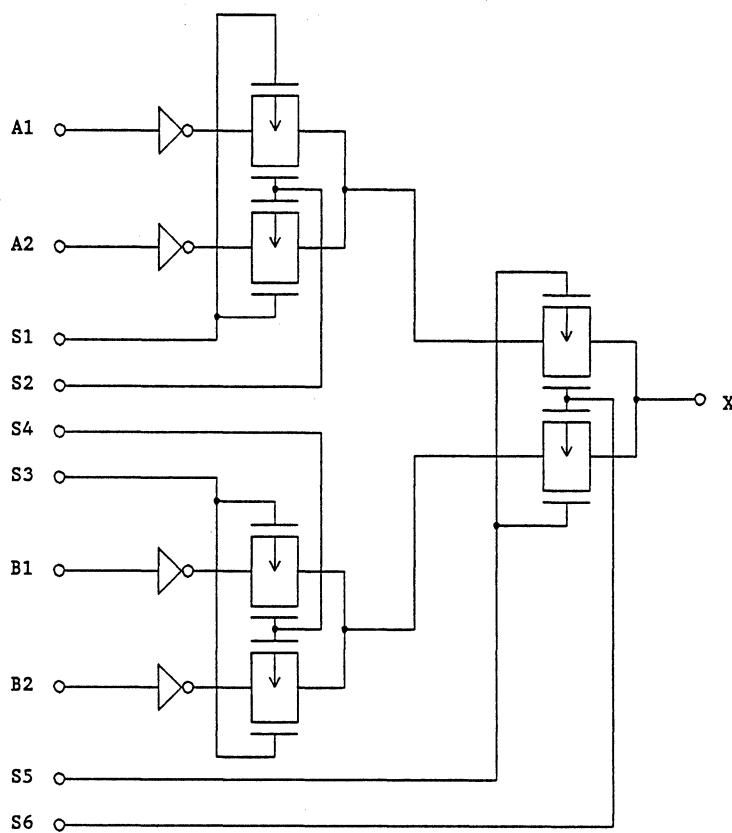
2

Function Table

$A1 \neq A2 \rightarrow S1 = S2$ or $S5 = S6$ Inhibit
 $B1 \neq B2 \rightarrow S3 = S4$ or $S5 = S6$ Inhibit
 $A1, A2 \neq B1, B2$ or $S5 = S6$ Inhibit

Cell Name
T5A

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version																																																				
Cell Name	Function				Number of BC																																																				
V3A	1:2 Selector				2																																																				
Cell Symbol		Propagation Delay Parameter																																																							
		tup	tdn	KCL	KCL2	CDR2	Path																																																		
		0.62 0.55	0.18 0.18	0.70 0.45	0.12 0.12		A → X S → X																																																		
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Pin Name		Input Loading Factor (ℓ_u)																																																							
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION								"UHB" Version																																																																										
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MC4		4-bit Magnitude Comparator						42																																																																										
Cell Symbol		Propagation Delay Parameter																																																																																
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Cell Name

MC4

A3
B3A2
B2

IS

IE

IG

A1
B1A0
B0Equivalent
Circuit

OG

OE

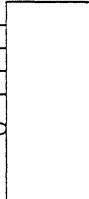
OS

2

Bus Driver

Page	Unit Cell Name	Function	Basic Cells
2-285	B41	4-bit Bus Driver	9

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHE" Version			
Cell Name	Function	Number of BC						
B41	4-bit Bus Driver							
Cell Symbol		Propagation Delay Parameter						
		tup	tdn					
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.58	0.07	1.52	0.06			A → X
		2.50	0.07	1.90	0.06			C → X
Parameter						Symbol	Typ(ns)*	
Pin Name		Input Loading Factor (μ u)						
A		1						
C		1						
Pin Name		Output Loading Factor (μ u)						
X		1						
Pin Name		Output Driving Factor (μ u)						
X		36						
						* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.		

2

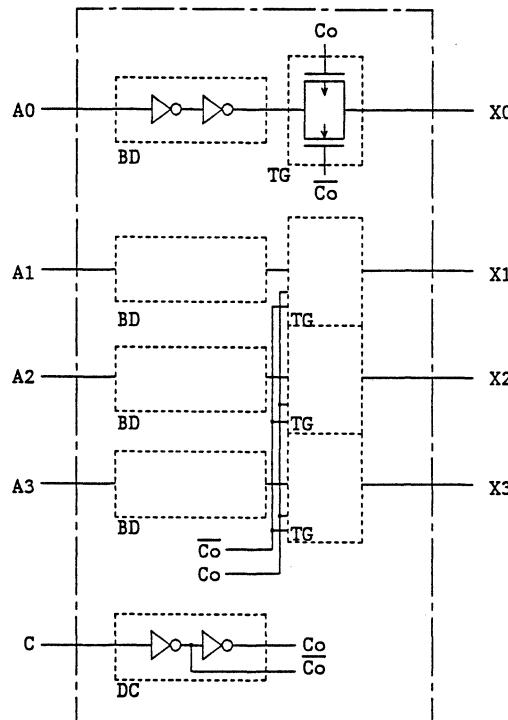
Maximum Number of B41 used in each UHB device

Device Name	Max. B41
C-330UHB	4
C-530UHB	5
C-830UHB	6
C-1200UHB	8
C-1700UHB	12
C-2200UHB	16

Device Name	Max. B41
C-3000UHB	21
C-4100UHB	26
C-6000UHB	50
C-8700UHB	70
C-12000UHB	90

Cell Name	
B41	

Equivalent Circuit



2

Note:

- TG is configured using the special transmission gates buried in the channel area of the UHB devices.
- BD and DC use the regular internal basic cells in the UHB devices.
- A Bus Terminator is invisible to logic designers and is automatically connected to each Bus line, when B41 is used.

Clip Cells

Page	Unit Cell Name	Function	Basic Cells
2-289	Z00	0 Clip	0
2-290	Z01	1 Clip	0
2-291	KD2	Load Gate (Fan-in = 2)	1

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
Z00	0 Clip					0	
Cell Symbol		Propagation Delay Parameter					
		tup	tdn				
		t0	KCL	t0	KCL	KCL2	Path
		Parameter				Symbol	Typ(ns)*
Pin Name	Input Loading Factor (δu)						
Pin Name	Output Driving Factor (δu)						
	X 200						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
Z01	1 Clip					0				
Cell Symbol		Propagation Delay Parameter								
		tup	tdn							
		t0	KCL	t0	KCL	KCL2				
						CDR2				
						Path				
Parameter		Symbol		Typ(ns)*						
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (μu)</th> </tr> </thead> <tbody> <tr> <td></td><td></td></tr> </tbody> </table>		Pin Name	Input Loading Factor (μu)							
Pin Name	Input Loading Factor (μu)									
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (μu)</th> </tr> </thead> <tbody> <tr> <td>X</td><td>200</td></tr> </tbody> </table>		Pin Name	Output Driving Factor (μu)	X	200					
Pin Name	Output Driving Factor (μu)									
X	200									
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								
UHB-Z01-E1 Sheet 1/1				Page 19-2						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
KD2	Load Gate Fan-in = 2					1
Cell Symbol	Propagation Delay Parameter					
		tup	tdn			
		t0	KCL	t0	KCL	KCL2 CDR2
A →						
Parameter						Symbol
						Typ(ns)*
Pin Name		Input Loading Factor (ℓ_u)				
A		2				
Pin Name		Output Driving Factor (ℓ_u)				
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.				

2

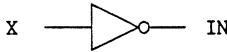
2

I/O Buffer Family

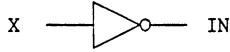
Page	Unit Cell Name	Function	Basic Cells
Input Buffers			
2-295	I1B	Input Buffer	5
2-296	I1BU	I1B with Pull-up Resistance	5
2-297	I1BD	I1B with Pull-down Resistance	5
2-298	I2B	Input Buffer	4
2-299	I2BU	I2B with Pull-up Resistance	4
2-300	I2BD	I2B with Pull-down Resistance	4
2-301	IKB	Clock Input Buffer	4
2-302	IKBU	IKB with Pull-up Resistance	4
2-303	IKBD	IKB with Pull-down Resistance	4
2-304	ILB	Clock Input Buffer	6
2-305	ILBU	ILB with Pull-up Resistance	6
2-306	ILBD	ILB with Pull-down Resistance	6
2-307	I1C	CMOS Interface Input Buffer	5
2-308	I1CU	I1C with Pull-up Resistance	5
2-309	I1CD	I1C with Pull-down Resistance	5
2-310	I2C	CMOS Interface Input Buffer	4
2-311	I2CU	I2C with Pull-up Resistance	4
2-312	I2CD	I2C with Pull-down Resistance	4
2-313	I1S	Schmitt Trigger Input Buffer	8
2-314	I1SU	I1S with Pull-up Resistance	8
2-315	I1SD	I1S with Pull-down Resistance	8
2-316	I2S	Schmitt Trigger Input Buffer	8
2-317	I2SU	I2S with Pull-up Resistance	8
2-318	I2SD	I2S with Pull-down Resistance	8
2-319	I1R	Schmitt Trigger Input Buffer	6
2-320	I1RU	I1R with Pull-up Resistance	6
2-321	I1RD	I1R with Pull-down Resistance	6
2-322	I2R	Schmitt Trigger Input Buffer	8
2-323	I2RU	I2R with Pull-up Resistance	8
2-324	I2RD	I2R with Pull-down Resistance	8
Output Buffers			
2-325	O1B	Output Buffer	3
2-326	O1L	Power Output Buffer	3
2-327	O1R	Output Buffer	5
2-328	O1S	Power Output Buffer	5
2-329	O2B	Output Buffer	2
2-330	O2L	Power Output Buffer	2
2-331	O2R	Output Buffer	4
2-332	O2S	Power Output Buffer	4
2-333	O2S2	High Power Output Buffer	6
2-334	O4R	Output Buffer	5
2-335	O4S	Power 3-state Output Buffer	5
2-336	O4S2	High Power Output Buffer	7
2-337	O4T	Output Buffer	4
2-338	O4W	Power 3-state Output Buffer	4
2-339	O1BF	Output Buffer	3
2-340	O1RF	Output Buffer	5
2-341	O2BF	Output Buffer	2
2-342	O2RF	Output Buffer	4
2-343	O4RF	3-state Output Buffer	5
2-344	O4TF	3-state Output Buffer	4
Bidirectional I/O Buffers (Buses)			
2-345	H6T	3-state Output and Input Buffer	8
2-346	H6TU	H6T with Pull-up Resistance	8
2-347	H6TD	H6T with Pull-down Resistance	8

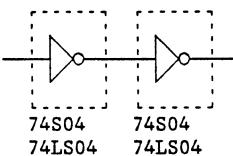
I/O Buffer Family (Continued)

2-348	H6W	Power 3-state Output and Input Buffer	8
2-349	H6WU	H6W with Pull-up Resistance	8
2-350	H6WD	H6W with Pull-down Resistance	8
2-351	H6C	3-state Output and CMOS Interface Input Buffer	8
2-352	H7CU	H6C with Pull-up Resistance	8
2-353	H6CD	H6C with Pull-down Resistance	8
Output Buffers			
2-354	H6E	Power 3-state Output and CMOS Interface Input Buffer	8
2-355	H6EU	H6E with Pull-up Resistance	8
2-356	H6ED	H6E with Pull-down Resistance	8
2-357	H6S	3-state Output and Schmitt Trigger Input Buffer	12
2-358	H6SU	H6S with Pull-up Resistance	12
2-359	H6SD	H6S with Pull-down Resistance	12
2-360	H6R	3-state Output and Schmitt Trigger Input Buffer	12
2-361	H6RU	H6R with Pull-up Resistance	12
2-362	H6RD	H6R with Pull-down Resistance	12
2-363	H8T	3-state Output and Input Buffer	9
2-364	H8TU	H8T with Pull-up Resistance	9
2-365	H8TD	H8T with Pull-down Resistance	9
2-366	H8W	Power 3-state Output and Input Buffer	9
2-367	H8WU	H8W with Pull-up Resistance	9
2-368	H8WD	H8W with Pull-down Resistance	9
2-369	H8W2	High Power 3-state Output and Input Buffer	11
2-370	H8W1	H8W2 with Pull-up Resistance	11
2-371	H8W0	H8W2 with Pull-down Resistance	11
2-372	H8C	3-state Output and CMOS Interface Input Buffer	9
2-373	H8CU	H8C with Pull-up Resistance	9
2-374	H8CD	H8C with Pull-down Resistance	9
2-375	H8E	Power 3-state Output and CMOS Interface Input Buffer	9
2-376	H8EU	H8E with Pull-up Resistance	9
2-377	H8ED	H8E with Pull-down Resistance	9
2-378	H8E2	High Power 3-state Output and Input Buffer	11
2-379	H8E1	H8E2 with Pull-up Resistance	11
2-380	H8E0	H8E2 with Pull-down Resistance	11
2-381	H8S	3-state Output and Schmitt Trigger Input Buffer	13
2-382	H8SU	H8S with Pull-up Resistance	13
2-383	H8SD	H8S with Pull-down Resistance	13
2-384	H8R	3-state Output and Schmitt Trigger Input Buffer	13
2-385	H8RU	H8R with Pull-up Resistance	13
2-386	H8RD	H8R with Pull-down Resistance	13
2-387	H6TF	3-state Output and Schmitt Trigger Input Buffer	8
2-388	H6TFU	H6TF with Pull-up Resistance	8
2-389	H6TFD	H6TF with Pull-down Resistance	8
2-390	H6CF	3-state Output and Input Buffer	8
2-391	H6CFU	H6CF with Pull-up Resistance	8
2-392	H6CFD	H6CF with Pull-down Resistance	8
2-393	H8TF	3-state Output and Input Buffer	9
2-394	H8TFU	H8TF with Pull-up Resistance	9
2-395	H8TFD	H8TF with Pull-down Resistance	9
2-396	H8CF	3-state Output and Input Buffer	9
2-397	H8CFU	H8CF with Pull-up Resistance	9
2-398	H8CFD	H8CF with Pull-down Resistance	9
Oscillator Circuits			
2-399	IT1O	Input Buffer for Oscillator	0
2-400	HOC	Output Buffer for Oscillator and Input Buffer	8
2-401	HOS	Output Buffer for Oscillator and Schmitt Trigger Input Buffer	8
2-402	HOGR	Output Buffer for Oscillator	8

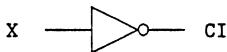
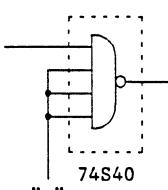
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
I1B	Input Buffer (Inverter)					5
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0	KCL	t0	KCL	KCL2 CDR2
		1.60	0.04	1.54	0.04	
						Path X → IN
		Parameter				Symbol Typ(ns)*
Pin Name	Input Loading Factor (λ_u)					
Pin Name	Output Driving Factor (λ_u)					
	IN 36					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

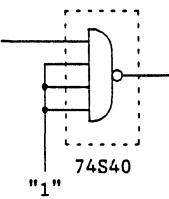
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
I1BU	Input Buffer (Inverter) with Pull-up Resistance					5				
Cell Symbol	Propagation Delay Parameter									
		tup	tdn							
		t0	KCL	t0	KCL	KCL2				
		1.60	0.04	1.54	0.04	CDR2				
						Path X → IN				
	X —————— ▽ —————— IN									
Pin Name	Input Loading Factor (λ_u)									
Pin Name	Output Driving Factor (λ_u)									
IN	36									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
UHB-I1BU-E1 Sheet 1/1						Page 20-2				

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version			
Cell Name	Function	Number of BC					
I1BD	Input Buffer (Inverter) with Pull-down Resistance						
Cell Symbol		Propagation Delay Parameter					
		tup	tdn				
		t0	KCL	t0	KCL		
		1.60	0.04	1.54	0.04		
		KCL2	CDR2				
					Path X → IN		
		Parameter			Symbol		
					Typ(ns)*		
Pin Name	Input Loading Factor (λ_u)						
Pin Name	Output Driving Factor (λ_u)						
	IN 36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							
UHB-I1BD-E1		Sheet 1/1					
Page 20-3							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																					
Cell Name	Function						Number of BC																					
I2B	Input Buffer (True)						4																					
Cell Symbol	Propagation Delay Parameter																											
X —————— IN	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="4">tdn</th><th></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th><th>Path</th></tr> </thead> <tbody> <tr> <td>1.06</td><td>0.04</td><td>1.84</td><td>0.04</td><td></td><td></td><td>X → IN</td></tr> </tbody> </table>						tup		tdn					t0	KCL	t0	KCL	KCL2	CDR2	Path	1.06	0.04	1.84	0.04			X → IN	
tup		tdn																										
t0	KCL	t0	KCL	KCL2	CDR2	Path																						
1.06	0.04	1.84	0.04			X → IN																						
	<table border="1"> <thead> <tr> <th>Parameter</th><th>Symbol</th><th>Typ(ns)*</th></tr> </thead> <tbody> <tr> <td></td><td></td><td></td></tr> </tbody> </table>						Parameter	Symbol	Typ(ns)*																			
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Pin Name	Input Loading Factor (μ u)																											
Pin Name	Output Driving Factor (μ u)																											
IN	36																											
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																												
TTL Equivalent Circuit																												
 74S04 74S04 74LS04 74LS04																												

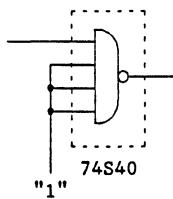
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
I2BU	Input Buffer (True) with Pull-up Resistance				4			
Cell Symbol		Propagation Delay Parameter						
		tup	tdn					
		t0	KCL	t0	KCL			
		1.06	0.04	1.84	0.04			
			KCL2	CDR2				
					Path $X \rightarrow IN$			
Parameter					Symbol			
					Typ(ns)*			
Pin Name		Input Loading Factor (λ_u)						
Pin Name		Output Driving Factor (λ_u)						
IN		36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								
UHB-I2BU-E1 Sheet 1/1								
Page 20-5								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version				
Cell Name	Function				Number of BC				
IKB	Clock Input Buffer (Inverter)				4				
Cell Symbol		Propagation Delay Parameter							
		tup	tdn						
		t0	KCL	t0	KCL				
		2.37	0.02	1.82	0.02				
			KCL2		CDR2				
					Path X → CI				
		Parameter		Symbol	Typ(ns)*				
Pin Name		Input Loading Factor (ℓ_u)							
Pin Name		Output Driving Factor (ℓ_u)							
CI		150							
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
TTL Equivalent Circuit									
									

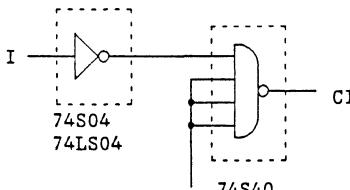
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version				
Cell Name	Function						Number of BC				
IKBU	Clock Input Buffer (Inverter) with Pull-up Resistance						4				
Cell Symbol	Propagation Delay Parameter										
		tup		tdn							
		t0	KCL	t0	KCL	KCL2	Path				
		2.37	0.02	1.82	0.02		X → CI				
		Parameter				Symbol	Typ(ns)*				
Pin Name	Input Loading Factor (λ_u)										
Pin Name	Output Driving Factor (λ_u)										
CI	150										
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.											
TTL Equivalent Circuit											
											
UHB-IKBU-E2 Sheet 1/1				Page 20-8							

2

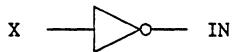
TTL Equivalent Circuit



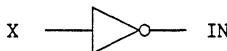
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																		
Cell Name	Function						Number of BC																		
ILB	Clock Input Buffer (True)																								
Cell Symbol	Propagation Delay Parameter																								
	<table border="1"> <thead> <tr> <th>tup</th><th>tdn</th><th colspan="4"></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th></tr> </thead> <tbody> <tr> <td>2.03</td><td>0.02</td><td>2.56</td><td>0.02</td><td></td><td></td></tr> </tbody> </table>						tup	tdn					t0	KCL	t0	KCL	KCL2	CDR2	2.03	0.02	2.56	0.02			Path X → CI
tup	tdn																								
t0	KCL	t0	KCL	KCL2	CDR2																				
2.03	0.02	2.56	0.02																						
X	CI																								
Pin Name	Input Loading Factor (lu)																								
Pin Name	Output Driving Factor (lu)																								
CI	150																								
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.																									
UHB-ILB-E2 Sheet 1/1				Page 20-10																					

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version			
Cell Name	Function					Number of BC			
ILBU	Clock Input Buffer (True) with Pull-up Resistance					6			
Cell Symbol		Propagation Delay Parameter							
		tup		tdn		Path X → CI			
		t0	KCL	t0	KCL		KCL2	CDR2	
		2.03	0.02	2.56	0.02				
		Parameter			Symbol	Typ(ns)*			
Pin Name	Input Loading Factor (λ_u)								
Pin Name	Output Driving Factor (λ_u)								
	CI 150								
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>									
TTL Equivalent Circuit									
									
<small>UHB-ILBU-E2 Sheet 1/1</small>									

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
ILBD	Clock Input Buffer (True) with Pull-down Resistance					6
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
		2.03	0.02	2.56	0.02	CDR2
						Path X → CI
		Parameter				Symbol
						Typ(ns)*
Pin Name	Input Loading Factor (λ_u)					
Pin Name	Output Driving Factor (λ_u)					
	CI	150				
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>						
UHB-ILBD-E2 Sheet 1/1				Page 20-12		

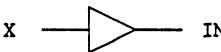
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																				
Cell Name	Function					Number of BC																				
I1C	CMOS Interface Input Buffer (Inverter)					5																				
Cell Symbol		Propagation Delay Parameter																								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2" style="text-align: center;">tup</th><th colspan="3" style="text-align: center;">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th></tr> </thead> <tbody> <tr> <td>1.32</td><td>0.04</td><td>1.44</td><td>0.04</td><td></td></tr> <tr> <td></td><td></td><td></td><td></td><td>CDR2</td></tr> </tbody> </table>				tup		tdn			t0	KCL	t0	KCL	KCL2	1.32	0.04	1.44	0.04						CDR2	Path
tup		tdn																								
t0	KCL	t0	KCL	KCL2																						
1.32	0.04	1.44	0.04																							
				CDR2																						
						X → IN																				
Parameter						Symbol																				
						Typ(ns)*																				
Pin Name	Input Loading Factor (ℓ_u)																									
Pin Name	Output Driving Factor (ℓ_u)																									
IN	36																									
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																										

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
I1CD	CMOS Interface Input Buffer (Inverter) with Pull-down Resistance					5	
Cell Symbol		Propagation Delay Parameter					
		t _{up}	t _{dn}				
		t ₀	KCL	t ₀	KCL	KCL2	Path
		1.35	0.04	1.44	0.04		X → IN
Parameter						Symbol	
						Typ(ns)*	
Pin Name	Input Loading Factor (ℓ_u)						
Pin Name	Output Driving Factor (ℓ_u)						
	IN 36						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
I2C	CMOS Interface Input Buffer (True)					4				
Cell Symbol	Propagation Delay Parameter									
		tup	tdn							
		t0	KCL	t0	KCL	KCL2				
X	IN	0.92	0.04	1.33	0.04	CDR2				
Parameter	Symbol	Typ(ns)*								
Pin Name	Input Loading Factor (ℓ_u)									
Pin Name	Output Driving Factor (ℓ_u)									
IN	36									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										

2

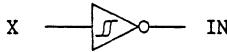
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function						Number of BC
I2CU	CMOS Interface Input Buffer with Pull-up Resistance (True)						4
Cell Symbol		Propagation Delay Parameter					
		t _{up}	t _{dn}				
		t ₀	KCL	t ₀	KCL	KCL2	CDR2
		0.92	0.04	1.33	0.04		
							Path
							X → IN
		Parameter			Symbol	Typ(ns)*	
Pin Name	Input Loading Factor (λ_u)						
Pin Name	Output Driving Factor (λ_u)						
	IN 36						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
I2CD	CMOS Interface Input Buffer with Pull-down Resistance (True)					4
Cell Symbol	Propagation Delay Parameter					
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
	X ————— IN	0.92	0.04	1.33	0.04	CDR2
Parameter				Symbol	Typ(ns)*	
Pin Name	Input Loading Factor (ℓ_u)					
IN	Output Driving Factor (ℓ_u)					
IN	36					
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
I1S	Schmitt Trigger Input Buffer (CMOS Type, Inverter)							8
Cell Symbol		Propagation Delay Parameter						
		tup		tdn				
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.90	0.16	2.68	0.08			X → IN
		Parameter						Symbol
								Typ(ns)*
Pin Name		Input Loading Factor (λu)						
Pin Name		Output Driving Factor (λu)						
IN		18						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>								

UHR-T1SU-E1 | Sheet 1/1

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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
I1SD	Schmitt Trigger Input Buffer (CMOS Type, Inverter) with Pull-down Resistance				8			
Cell Symbol		Propagation Delay Parameter						
		tup	tdn					
		t0	KCL	t0	KCL			
		3.90	0.16	2.68	0.08			
			KCL2	CDR2				
					Path			
					X → IN			
		Parameter			Symbol			
					Typ(ns)*			
Pin Name	Input Loading Factor (ℓ_u)							
Pin Name	Output Driving Factor (ℓ_u)							
	IN 18							
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								
UHB-I1SD-E1 Sheet 1/1			Page 20-21					

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version						
Cell Name	Function					Number of BC						
I2S	Schmitt Trigger Input Buffer (CMOS Type, True)					8						
Cell Symbol	Propagation Delay Parameter											
	tup	tdn										
	t0	KCL	t0	KCL	KCL2	Path						
	2.48	0.16	3.08	0.10		X → IN						
	Parameter											
	Symbol											
	Typ(ns)*											
Pin Name	Input Loading Factor (λ_u)											
Pin Name	Output Driving Factor (λ_u)											
IN	18											
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.												
UHB-I2S-E1 Sheet 1/1												
Page 20-22												

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version
Cell Name	Function						Number of BC
I2SU	Schmitt Trigger Input Buffer (CMOS Type, True) with Pull-up Resistance						8
Cell Symbol	Propagation Delay Parameter						
		tup	tdn				Path
		t0	KCL	t0	KCL	KCL2	CDR2
		2.48	0.16	3.08	0.10		X → IN
		Parameter	Symbol	Typ(ns)*			
Pin Name	Input Loading Factor (ℓ_u)						
Pin Name	Output Driving Factor (ℓ_u)						
IN	18						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version
Cell Name	Function						Number of BC
I2SD	Schmitt Trigger Input Buffer (CMOS Type, True) with Pull-down Resistance						8
Cell Symbol	Propagation Delay Parameter						
			tup	tdn			
	t0	KCL	t0	KCL	KCL2	CDR2	Path
	2.48	0.16	3.08	0.10			X → IN
	Parameter					Symbol	Typ(ns)*
Pin Name	Input Loading Factor (μ u)						
Pin Name	Output Driving Factor (μ u)						
IN	18						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

2

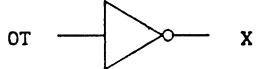
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2

2

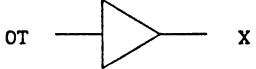
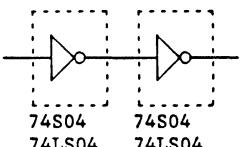
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version
Cell Name	Function						Number of BC
I2R	Schmitt Trigger Input Buffer (TTL Type, True)						8
Cell Symbol	Propagation Delay Parameter						
		tup	tdn				Path
		t0	KCL	t0	KCL	KCL2	CDR2
		2.24	0.16	3.72	0.13		X → IN
		Parameter				Symbol	Typ(ns)*
Pin Name	Input Loading Factor (ℓ_u)						
Pin Name	Output Driving Factor (ℓ_u)						
IN	18						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							
UHB-I2R-E1 Sheet 1/1							
Page 20-28							

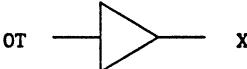
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version
Cell Name	Function				Number of BC
I2RU	Schmitt Trigger Input Buffer (TTL Type, True) with Pull-up Resistance				
Cell Symbol		Propagation Delay Parameter			
		tup	tdn		
		t0	KCL	t0	KCL
		2.24	0.16	3.72	0.13
				KCL2	CDR2
					Path
					X → IN
		Parameter			Symbol
					Typ(ns)*
Pin Name	Input Loading Factor (ℓ_u)				
Pin Name	Output Driving Factor (ℓ_u)				
	IN 18				
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version						
Cell Name	Function					Number of BC					
01B	Output Buffer(IOL=3.2mA, Inverter)										
Cell Symbol		Propagation Delay Parameter									
		tup	tdn								
		t0 1.93 (5.29)	KCL 0.056	t0 2.24 (9.68)	KCL 0.124	KCL2 CDR2					
		Parameter			Symbol	Typ(ns)*					
Pin Name	Input Loading Factor (lu)										
	OT	2									
Pin Name	Output Driving Factor (lu)										
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>											
<p>Note: 1. The unit of KCL is ns/pF.</p> <p>2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.</p> <p>3. The parameters in parentheses are the values applied to the simulation.</p>											
UHB-01B-E4 Sheet 1/1			Page 20-31								

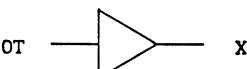
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
O1L	Output Buffer(IOL=12mA, Inverter)							
Cell Symbol	Propagation Delay Parameter							
		tup	tdn		Path			
		t0	KCL	t0	KCL	KCL2	CDR2	OT → X
		2.29 (4.51)	0.037	2.47 (4.93)	0.041			
		Parameter	Symbol	Typ(ns)*				
Pin Name	Input Loading Factor (λ_u)							
OT	2							
Pin Name	Output Driving Factor (λ_u)							
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
Note: 1. The unit of KCL is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.								
UHB-01L-E3		Sheet 1/1		Page 20-32				

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
O1R	Output Buffer(IOL=3.2mA, Inverter) with Noise Limit Resistance					5		
Cell Symbol	Propagation Delay Parameter							
		tup	tdn			Path		
		t0	KCL	t0	KCL	KCL2	CDR2	OT → X
		3.30 (6.66)	0.056	5.18 (12.98)	0.13			
Parameter						Symbol	Typ(ns)*	
Pin Name	Input Loading Factor (ℓu)							
OT	1							
Pin Name	Output Driving Factor (ℓu)							
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
<p>Note: 1. The unit of K_{CL} is ns/pF.</p> <p>2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.</p> <p>3. The parameters in parentheses are the values applied to the simulation.</p>								

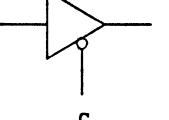
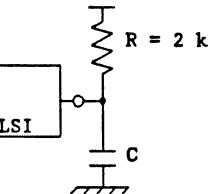
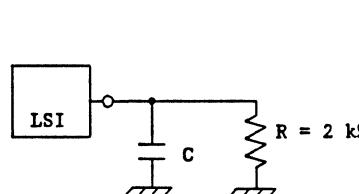
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																			
Cell Name		Function					Number of BC																			
O2B		Output Buffer (IOL=3.2mA, True)					2																			
Cell Symbol		Propagation Delay Parameter																								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">tup</th><th colspan="3">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th></tr> </thead> <tbody> <tr> <td>1.70 (5.09)</td><td>0.056</td><td>1.75 (9.19)</td><td>0.124</td><td></td></tr> <tr> <td></td><td></td><td></td><td></td><td>CDR2</td></tr> </tbody> </table>					tup		tdn			t0	KCL	t0	KCL	KCL2	1.70 (5.09)	0.056	1.75 (9.19)	0.124						CDR2
tup		tdn																								
t0	KCL	t0	KCL	KCL2																						
1.70 (5.09)	0.056	1.75 (9.19)	0.124																							
				CDR2																						
							Path OT → X																			
Pin Name		Parameter					Symbol																			
OT							Typ(ns)*																			
Pin Name		Input Loading Factor (λ_u)																								
OT		4																								
Pin Name		Output Driving Factor (λ_u)																								
		<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																								
TTL Equivalent Circuit																										
																										
<p>Note: 1. The unit of K_{CL} is ns/pF.</p> <p>2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.</p> <p>3. The parameters in parentheses are the values applied to the simulation.</p>																										

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version			
Cell Name	Function	Number of BC					
O2L	Output Buffer(IOL=12mA, True)						
Cell Symbol		Propagation Delay Parameter					
		tup	tdn				
		t0 2.09 (4.31)	KCL 0.037	t0 1.98 (4.44)	KCL 0.041		
			KCL2	CDR2	Path OT → X		
		Parameter		Symbol	Typ(ns)*		
Pin Name	Input Loading Factor (lu)						
	OT 4						
Pin Name	Output Driving Factor (lu)						
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					
Note: 1. The unit of KCL is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.							
UHB-02L-E3 Sheet 1/1			Page 20-36				

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
O2R	Output Buffer(IOL=3.2mA, True) with Noise Limit Resistance					4		
Cell Symbol		Propagation Delay Parameter						
		tup	tdn			Path		
		t0	KCL	t0'	KCL	KCL2	CDR2	OT → X
		2.99 (6.35)	0.056	4.69 (12.49)	0.13			
Parameter						Symbol	Typ(ns)*	
Pin Name		Input Loading Factor (f <u>)</u>						
OT		2						
Pin Name		Output Driving Factor (f <u>)</u>						
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>								
<p>Note: 1. The unit of K_{CL} is ns/pF.</p> <p>2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.</p> <p>3. The parameters in parentheses are the values applied to the simulation.</p>								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version				
Cell Name	Function				Number of BC				
O2S	Output Buffer(IOL=12mA, True) with Noise Limit Resistance				4				
Cell Symbol	Propagation Delay Parameter								
	tup		tdn						
	t0	KCL	t0	KCL	KCL2				
		3.71 (5.99)	0.038	5.87 (9.11)	0.054				
					Path				
					OT → X				
Parameter					Symbol				
					Typ(ns)*				
Pin Name	Input Loading Factor (ℓ_u)								
	OT	2							
Pin Name	Output Driving Factor (ℓ_u)								
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>									
<p>Note: 1. The unit of KCL is ns/pF.</p> <p>2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.</p> <p>3. The parameters in parentheses are the values applied to the simulation.</p>									
UHB-O2S-E3 Sheet 1/1			Page 20-38						

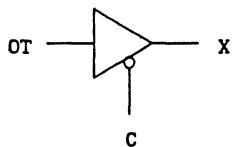
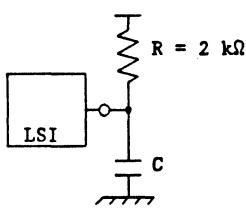
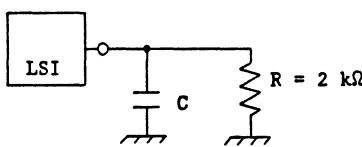
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
O2S2	Output Buffer(IOL=24mA, True) with Noise Limit Resistance					6
Cell Symbol	Propagation Delay Parameter					
		tup	tdn			Path
		t0	KCL	t0	KCL	KCL2 CDR2
		5.27 (7.19)	0.032	9.51 (13.11)	0.06	
						OT → X
Parameter	Symbol	Typ(ns)*				
Pin Name	Input Loading Factor (ℓ_u)					
OT	2					
Pin Name	Output Driving Factor (ℓ_u)					
			<p>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</p>			
<p>Note: 1. The unit of K_{CL} is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>						

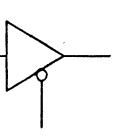
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version														
Cell Name	Function	Number of BC																
O4R	Tri-state Output Buffer(IOL=3.2mA, True) with Noise Limit Resistance	5																
Cell Symbol		Propagation Delay Parameter																
		<i>t_{up}</i>	<i>t_{dn}</i>	<i>t₀</i>	KCL													
OT C		3.12 (6.76)	0.056	5.66 (14.11)	0.13	KCL2	CDR2	Path OT → X										
<table border="1"> <thead> <tr> <th colspan="2">L → Z</th> <th colspan="2">Z → L</th> </tr> <tr> <th><i>t₀</i></th> <th>KCL</th> <th><i>t₀</i></th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>2.22 (13.44)</td> <td>*</td> <td>6.47 (14.92)</td> <td>0.13</td> </tr> </tbody> </table>						L → Z		Z → L		<i>t₀</i>	KCL	<i>t₀</i>	KCL	2.22 (13.44)	*	6.47 (14.92)	0.13	C → X
L → Z		Z → L																
<i>t₀</i>	KCL	<i>t₀</i>	KCL															
2.22 (13.44)	*	6.47 (14.92)	0.13															
<table border="1"> <thead> <tr> <th colspan="2">H → Z</th> <th colspan="2">Z → H</th> </tr> <tr> <th><i>t₀</i></th> <th>KCL</th> <th><i>t₀</i></th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>3.07 (13.44)</td> <td>*</td> <td>3.20 (14.92)</td> <td>0.056</td> </tr> </tbody> </table>							H → Z		Z → H		<i>t₀</i>	KCL	<i>t₀</i>	KCL	3.07 (13.44)	*	3.20 (14.92)	0.056
H → Z		Z → H																
<i>t₀</i>	KCL	<i>t₀</i>	KCL															
3.07 (13.44)	*	3.20 (14.92)	0.056															
<table border="1"> <thead> <tr> <th colspan="2">Z → L</th> <th colspan="2">L → Z</th> </tr> <tr> <th><i>t₀</i></th> <th>KCL</th> <th><i>t₀</i></th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>6.47 (14.92)</td> <td>*</td> <td>2.22 (13.44)</td> <td>0.13</td> </tr> </tbody> </table>							Z → L		L → Z		<i>t₀</i>	KCL	<i>t₀</i>	KCL	6.47 (14.92)	*	2.22 (13.44)	0.13
Z → L		L → Z																
<i>t₀</i>	KCL	<i>t₀</i>	KCL															
6.47 (14.92)	*	2.22 (13.44)	0.13															
<table border="1"> <thead> <tr> <th colspan="2">Z → H</th> <th colspan="2">H → Z</th> </tr> <tr> <th><i>t₀</i></th> <th>KCL</th> <th><i>t₀</i></th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>0.13</td> <td>*</td> <td>3.07 (13.44)</td> <td>3.20 (14.92)</td> </tr> </tbody> </table>							Z → H		H → Z		<i>t₀</i>	KCL	<i>t₀</i>	KCL	0.13	*	3.07 (13.44)	3.20 (14.92)
Z → H		H → Z																
<i>t₀</i>	KCL	<i>t₀</i>	KCL															
0.13	*	3.07 (13.44)	3.20 (14.92)															
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>																		
																		
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.															
<p>Note: 1. The unit of K_{CL} is ns/pF.</p> <p>2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.</p> <p>3. The parameters in parentheses are the values applied to the simulation.</p>																		

Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

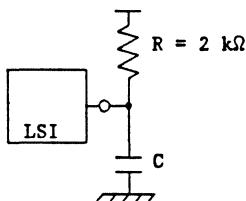
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version
Cell Name	Function				Number of BC
O4S	Tri-state Output Buffer(IOL=12mA, True) with Noise Limit Resistance				
Cell Symbol		Propagation Delay Parameter			
		tup	tdn		
		t0 3.96 (6.43)	KCL 0.038	t0 7.25 (10.76)	KCL 0.054
				KCL2	CDR2
					Path OT → X
		L → Z		Z → L	
		t0 3.65 (17.83)	KCL *	t0 7.40 (10.91)	KCL 0.054
		H → Z		Z → H	
		t0 3.75 (17.83)	KCL *	t0 3.69 (10.91)	KCL 0.038
Pin Name		Input Loading Factor (lu)			
OT	2				
C	2				
Pin Name		Output Driving Factor (lu)			
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>					
					
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.		
<p>Note: 1. The unit of K_{CL} is ns/pF. 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>					

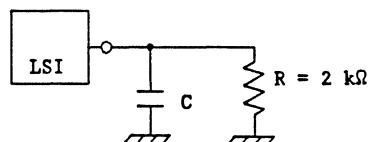
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version
Cell Name	Function	Number of BC		
O4S2	Tri-state Output Buffer(IOL=24mA, True) with Noise Limit Resistance			
Cell Symbol		Propagation Delay Parameter		
		tup	tdn	Path OT → X
		t0 5.61 (7.69)	KCL 0.032	
		t0 11.62 (15.52)	KCL 0.06	C → X
		KCL2	CDR2	
		L → Z	Z → L	
		t0 5.36 (19.23)	KCL *	
		t0 11.18 (15.08)	KCL 0.06	
		H → Z	Z → H	
Pin Name	Input Loading Factor (f <u>u</u>)	t0 6.37 (19.23)	KCL *	
	OT 2	t0 5.25 (15.08)	KCL 0.032	
		C 2		
Pin Name		Output Driving Factor (f <u>u</u>)		

* These values are subject to external loading condition.

Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

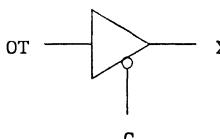
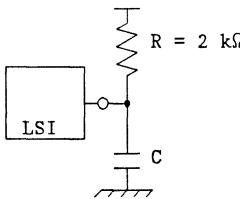
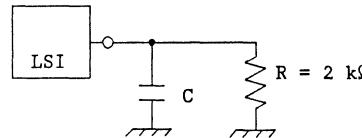


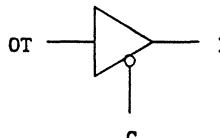
(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} is ns/pF.

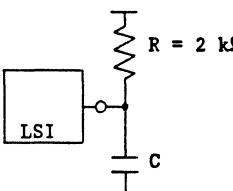
2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

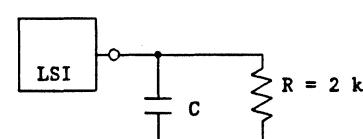
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version				
Cell Name	Function	Number of BC						
04T	Tri-state Output Buffer(IOL=3.2mA, True)	4						
Cell Symbol		Propagation Delay Parameter						
		t _{up}	t _{dn}					
		t ₀ 2.42 (6.06)	KCL 0.056	t ₀ 2.52 (10.97)	KCL 0.13	KCL2	CDR2	Path OT → X
		L → Z Z → L					C → X	
		t ₀ 2.07 (12.35)	KCL	t ₀ 2.55 (11.00)	KCL 0.13			
		H → Z Z → H						
		t ₀ 3.41 (12.35)	KCL	t ₀ 2.31 (11.00)	KCL 0.056			
Pin Name		Input Loading Factor (f <u>u</u>)						
OT		4						
C		2						
Pin Name		Output Driving Factor (f <u>u</u>)						
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>								
								
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.					
<p>Note: 1. The unit of K_{CL} is ns/pF. 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
O4W	Tri-state Output Buffer(IOL=12mA, True)					
Cell Symbol		Propagation Delay Parameter				
		t _{up}	t _{dn}			
		t ₀ 3.02 (5.49)	KCL 0.038	t ₀ 4.12 (7.17)	KCL 0.047	KCL2 CDR2
						Path OT → X
		L → Z		Z → L		C → X
		t ₀ 2.96 (16.35)	KCL *	t ₀ 3.69 (6.75)	KCL 0.047	
		H → Z		Z → H		
		t ₀ 4.03 (16.35)	KCL *	t ₀ 2.72 (6.75)	KCL 0.038	
Pin Name		Input Loading Factor (f _{lu})				
OT	C	4	2			
Pin Name		Output Driving Factor (f _{lu})				

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:

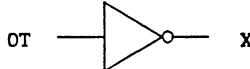


(a) Measurement of tpd at LZ and ZL.

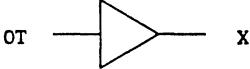
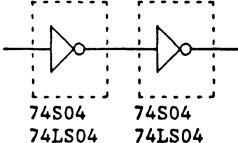


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} is ns/pF.
2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version					
Cell Name	Function			Number of BC					
Cell Symbol	Propagation Delay Parameter								
	tup			tdn					
	t0	KCL	t0	KCL	KCL2	CDR2	Path		
	1.96 (5.32)	0.056	2.01 (5.79)	0.063			OT → X		
Parameter				Symbol	Typ(ns)*				
Pin Name	Input Loading Factor (ℓ_u)								
OT	2								
Pin Name	Output Driving Factor (ℓ_u)								
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>									
<p>Note: 1. The unit of K_{CL} is ns/pF.</p> <p>2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.</p> <p>3. The parameters in parentheses are the values applied to the simulation.</p>									

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version						
Cell Name	Function						Number of BC						
O1RF	Output Buffer (IOL=8mA, Inverter) with Noise Limit Resistance						5						
Cell Symbol	Propagation Delay Parameter												
	t _{up}		t _{dn}										
	t ₀	KCL	t ₀	KCL	KCL2	CDR2	Path						
	3.39 (6.75)	0.056	5.60 (9.38)	0.063			OT → X						
Parameter							Symbol						
							Typ(ns)*						
Pin Name	Input Loading Factor (μ u)												
OT	1												
Pin Name	Output Driving Factor (μ u)												
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.													
<p>Note: 1. The unit of K_{CL} is ns/pF.</p> <p>2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.</p> <p>3. The parameters in parentheses are the values applied to the simulation.</p>													
UHB-O1RF-E1 Sheet 1/1				Page 20-88									

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
O2BF	Output Buffer (IOL=8mA, True)							
2		Propagation Delay Parameter						
Cell Symbol		tup	tdn			Path		
		t0	KCL	t0	KCL	KCL2	CDR2	OT → X
1.76 (5.12)				1.52 (5.30)	0.063			
Parameter						Symbol	Typ(ns)*	
Pin Name	Input Loading Factor (ℓ_u)							
	OT	4						
Pin Name	Output Driving Factor (ℓ_u)							
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								
TTL Equivalent Circuit								
								
Note: 1. The unit of K_{CL} is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.								

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version						
Cell Name	Function					Number of BC						
O2RF	Output Buffer (IOL=8mA, True) with Noise Limit Resistance					4						
Cell Symbol	Propagation Delay Parameter											
	tup		tdn									
	t0	KCL	t0	KCL	KCL2	CDR2						
	3.08 (6.44)	0.056	5.11 (8.89)	0.063								
Parameter						Symbol						
						Typ(ns)*						
Pin Name	Input Loading Factor (f_u)											
OT	2											
Pin Name	Output Driving Factor (f_u)											
	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.											
Note: 1. The unit of K _{CL} is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.												
UHB-O2RF-E1 Sheet 1/1												
Page 20-90												

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
O4RF	Tri-state Output Buffer (IOL=8mA, True) with Noise Limit Resistance				5			
Cell Symbol	Propagation Delay Parameter							
		t _{up}	t _{dn}		Path			
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	OT → X
		3.21 (6.85)	0.056	5.96 (10.51)	0.070			
		L → Z		Z → L		C → X		
		t ₀	KCL	t ₀	KCL			
		2.62 (15.89)	*	6.82 (11.37)	0.070			
		H → Z		Z → H				
		t ₀	KCL	t ₀	KCL			
		3.30 (15.89)	*	3.21 (11.37)	0.056			
Pin Name	Input Loading Factor (f <u>u</u>)							
OT	2							
C	2							
Pin Name	Output Driving Factor (f <u>u</u>)							

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:

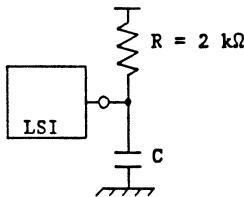
(a) Measurement of tpd at LZ and ZL.

(b) Measurement of tpd at HZ and ZH.

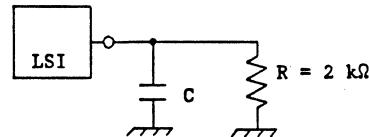
Note: 1. The unit of K_{CL} is ns/pF.
2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																			
Cell Name	Function	Number of BC																					
04TF	Tri-state Output Buffer (IOL=8mA, True)																						
Cell Symbol	Propagation Delay Parameter																						
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="2">tdn</th><th colspan="2"></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th></tr> </thead> <tbody> <tr> <td>2.51 (6.15)</td><td>0.056</td><td>3.27 (7.37)</td><td>0.063</td><td></td><td></td></tr> </tbody> </table>				tup		tdn				t0	KCL	t0	KCL	KCL2	CDR2	2.51 (6.15)	0.056	3.27 (7.37)	0.063			Path
tup		tdn																					
t0	KCL	t0	KCL	KCL2	CDR2																		
2.51 (6.15)	0.056	3.27 (7.37)	0.063																				
					OT → X																		
	<table border="1"> <thead> <tr> <th colspan="2">L → Z</th><th colspan="2">Z → L</th><th colspan="2"></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th colspan="2"></th></tr> </thead> <tbody> <tr> <td>2.29 (14.80)</td><td>*</td><td>3.35 (7.45)</td><td>0.063</td><td colspan="2"></td></tr> </tbody> </table>				L → Z		Z → L				t0	KCL	t0	KCL			2.29 (14.80)	*	3.35 (7.45)	0.063			C → X
L → Z		Z → L																					
t0	KCL	t0	KCL																				
2.29 (14.80)	*	3.35 (7.45)	0.063																				
Pin Name	Input Loading Factor (f <u>u</u>)																						
OT	4																						
C	2																						
Pin Name	Output Driving Factor (f <u>u</u>)																						

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL is ns/pF.

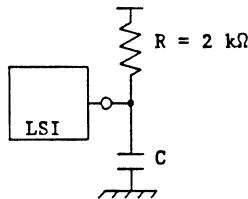
2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

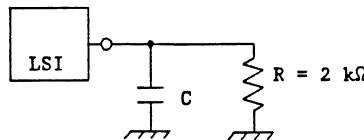
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																				
Cell Name	Function					Number of BC																				
H6T	Tri-state Output ($I_{OL}=3.2\text{mA}$) & Input Buffer (True)					8																				
Cell Symbol	Propagation Delay Parameter																									
		<table border="1"> <thead> <tr> <th colspan="2">t_{up}</th><th colspan="3">t_{dn}</th></tr> <tr> <th>t₀</th><th>KCL</th><th>t₀</th><th>KCL</th><th>KCL2</th></tr> </thead> <tbody> <tr> <td>1.06 (7.18)</td><td>0.04</td><td>1.84 (13.57)</td><td>0.04</td><td>0.13</td></tr> <tr> <td>2.42</td><td>0.056</td><td>2.52</td><td></td><td></td></tr> </tbody> </table>				t _{up}		t _{dn}			t ₀	KCL	t ₀	KCL	KCL2	1.06 (7.18)	0.04	1.84 (13.57)	0.04	0.13	2.42	0.056	2.52			Path X → IN OT → X
t _{up}		t _{dn}																								
t ₀	KCL	t ₀	KCL	KCL2																						
1.06 (7.18)	0.04	1.84 (13.57)	0.04	0.13																						
2.42	0.056	2.52																								
		<table border="1"> <thead> <tr> <th colspan="2">L → Z</th><th colspan="2">Z → L</th></tr> <tr> <th>t₀</th><th>KCL</th><th>t₀</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>2.07 (15.35)</td><td>*</td><td>2.55 (13.60)</td><td>0.13</td></tr> </tbody> </table>				L → Z		Z → L		t ₀	KCL	t ₀	KCL	2.07 (15.35)	*	2.55 (13.60)	0.13	C → X								
L → Z		Z → L																								
t ₀	KCL	t ₀	KCL																							
2.07 (15.35)	*	2.55 (13.60)	0.13																							
<table border="1"> <thead> <tr> <th colspan="2">H → Z</th><th colspan="2">Z → H</th></tr> <tr> <th>t₀</th><th>KCL</th><th>t₀</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>3.41 (15.35)</td><td>*</td><td>2.31 (13.60)</td><td>0.056</td></tr> </tbody> </table>				H → Z		Z → H		t ₀	KCL	t ₀	KCL	3.41 (15.35)	*	2.31 (13.60)	0.056											
H → Z		Z → H																								
t ₀	KCL	t ₀	KCL																							
3.41 (15.35)	*	2.31 (13.60)	0.056																							
Pin Name	Input Loading Factor (ℓ_u)																									
OT	4																									
C	2																									
Pin Name	Output Driving Factor (ℓ_u)																									
IN	36																									

* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

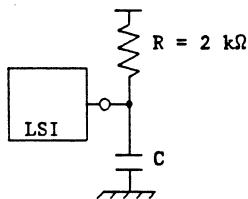
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

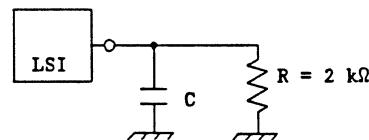
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function				Number of BC			
H6TU	Tri-state Output($I_{OL}=3.2\text{mA}$) & Input Buffer (True) with Pull-up Resistance				8			
Cell Symbol	Propagation Delay Parameter							
		t_{up}	t_{dn}			Path		
		t_0	KCL	t_0	KCL	KCL2	CDR2	
		1.06 (7.18)	0.04	1.84 (13.57)	0.04			X → IN
		2.42	0.056	2.52	0.13			OT → X
		$L \rightarrow Z$		$Z \rightarrow L$		$C \rightarrow X$		
		t_0	KCL	t_0	KCL			
		2.07 (15.35)	*	2.55 (13.60)	0.13			
		$H \rightarrow Z$		$Z \rightarrow H$				
		t_0	KCL	t_0	KCL			
		3.41 (15.35)	*	2.31 (13.60)	0.056			
		Input Loading Factor (μu)						
OT		4						
C		2						
		Output Driving Factor (μu)						
IN		36						

* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

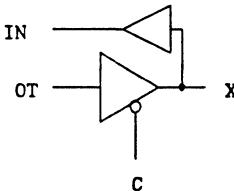


(b) Measurement of tpd at HZ and ZH.

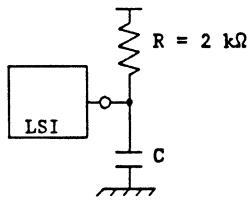
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

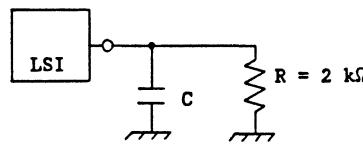
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version						
Cell Name	Function					Number of BC						
H6TD	Tri-state Output($I_{OL}=3.2\text{mA}$) & Input Buffer (True) with Pull-down Resistance					8						
Cell Symbol		Propagation Delay Parameter										
		t_{up}	t_{dn}	K_{CL}	K_{CL2}	Path						
		1.06 2.42 (7.18)	1.84 2.52 (13.57)	0.04 0.13		X → IN OT → X						
		$L \rightarrow Z$		$Z \rightarrow L$		$C \rightarrow X$						
		t_0	K_{CL}	t_0	K_{CL}							
		2.07 (15.35)	*	2.55 (13.60)	0.13							
		$H \rightarrow Z$		$Z \rightarrow H$								
		t_0	K_{CL}	t_0	K_{CL}							
		3.41 (15.35)	*	2.31 (13.60)	0.056							
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (ℓu)</th> </tr> </thead> <tbody> <tr> <td>OT</td> <td>4</td> </tr> <tr> <td>C</td> <td>2</td> </tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓu)	OT	4		C	2				
Pin Name	Input Loading Factor (ℓu)											
OT	4											
C	2											
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (ℓu)</th> </tr> </thead> <tbody> <tr> <td>IN</td> <td>36</td> </tr> </tbody> </table>		Pin Name	Output Driving Factor (ℓu)	IN	36							
Pin Name	Output Driving Factor (ℓu)											
IN	36											

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time
 at LZ, ZL, HZ and ZH are as follows:

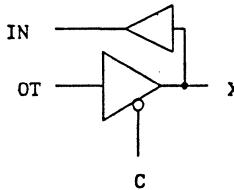
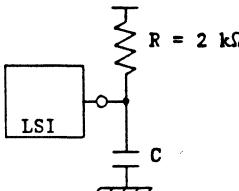
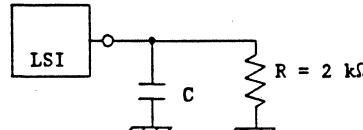


(a) Measurement of tpd at LZ and ZL.



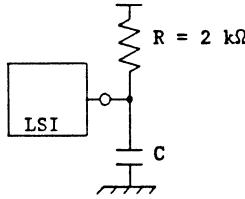
(b) Measurement of tpd at HZ and ZH.

- Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

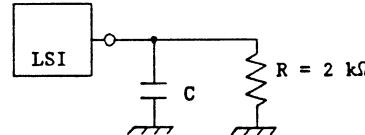
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version			
Cell Name	Function	Number of BC					
H6W	Tri-state Output ($I_{OL}=12mA$) & Input Buffer (True)	8					
Cell Symbol		Propagation Delay Parameter					
		tup		tdn			
		t0	KCL	t0	KCL		
		1.06 3.02 (6.25)	0.04 0.038	1.84 4.12 (8.12)	0.04 0.047		
		KCL2		CDR2			
		Path					
		X → IN					
		OT → X					
		C → X					
		L → Z		Z → L			
		t0	KCL	t0	KCL		
		2.96 (20.25)	*	3.69 (7.69)	0.047		
		H → Z					
		Z → H		KCL			
		t0	KCL	t0	KCL		
		4.03 (20.25)	*	2.72 (7.69)	0.038		
		Output Driving Factor (λ_u)					
		Input Loading Factor (λ_u)					
		Pin Name					
		OT					
		C					
		IN					
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>							
							
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.				
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version							
Cell Name	Function	Number of BC									
H6WU	Tri-state Output($I_{OL}=12mA$) & Input Buffer (True) with Pull-up Resistance										
Cell Symbol		Propagation Delay Parameter									
		t_{up}		t_{dn}							
		t ₀	KCL	t ₀	KCL						
		1.06 (6.25)	0.04	1.84	0.04						
		3.02	0.038	4.12 (8.12)	0.047						
		L → Z		Z → L							
		t ₀	KCL	t ₀	KCL						
		2.96 (20.25)	*	3.69 (7.69)	0.047						
		H → Z		Z → H							
		t ₀	KCL	t ₀	KCL						
		4.03 (20.25)	*	2.72 (7.69)	0.038						
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="padding: 2px;">Pin Name</td> <td style="padding: 2px;">Input Loading Factor (ℓu)</td> </tr> <tr> <td style="padding: 2px;">OT</td> <td style="padding: 2px;">4</td> </tr> <tr> <td style="padding: 2px;">C</td> <td style="padding: 2px;">2</td> </tr> </table>		Pin Name	Input Loading Factor (ℓu)	OT	4	C	2				
Pin Name	Input Loading Factor (ℓu)										
OT	4										
C	2										
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="padding: 2px;">Pin Name</td> <td style="padding: 2px;">Output Driving Factor (ℓu)</td> </tr> <tr> <td style="padding: 2px;">IN</td> <td style="padding: 2px;">36</td> </tr> </table>		Pin Name	Output Driving Factor (ℓu)	IN	36						
Pin Name	Output Driving Factor (ℓu)										
IN	36										

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of t_{pd} at LZ and ZL.



(b) Measurement of t_{pd} at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

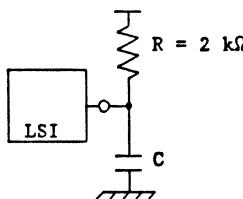
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

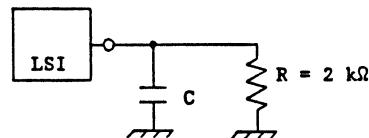
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version						
Cell Name	Function						Number of BC						
H6WD	Tri-state Output(IOL=12mA) & Input Buffer (True) with Pull-down Resistance												
Cell Symbol		Propagation Delay Parameter											
		tup		tdn			Path						
		t0	KCL	t0	KCL	KCL2	CDR2	X → IN OT → X					
		1.06 (6.25)	0.04	1.84 (8.12)	0.04 0.047								
		3.02	0.038	4.12									
		L → Z		Z → L		C → X							
		t0	KCL	t0	KCL								
		2.96 (20.25)	*	3.69 (7.69)	0.047								
		H → Z		Z → H									
		t0	KCL	t0	KCL								
		4.03 (20.25)	*	2.72 (7.69)	0.038								
<table border="1"> <tr> <td>Pin Name</td> <td>Input Loading Factor (ℓ_u)</td> </tr> <tr> <td>OT</td> <td>4</td> </tr> <tr> <td>C</td> <td>2</td> </tr> </table>		Pin Name	Input Loading Factor (ℓ_u)	OT	4	C	2						
Pin Name	Input Loading Factor (ℓ_u)												
OT	4												
C	2												
<table border="1"> <tr> <td>Pin Name</td> <td>Output Driving Factor (ℓ_u)</td> </tr> <tr> <td>IN</td> <td>36</td> </tr> </table>		Pin Name	Output Driving Factor (ℓ_u)	IN	36								
Pin Name	Output Driving Factor (ℓ_u)												
IN	36												

* These values are subject to external loading condition.

Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

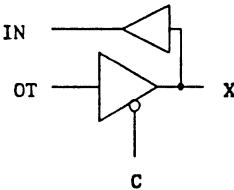
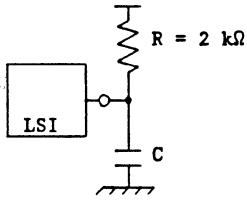
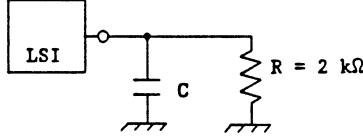


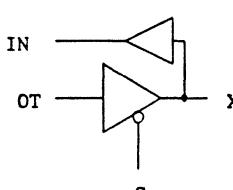
(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

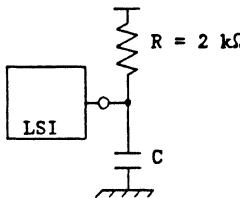
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

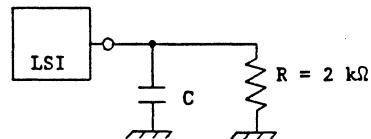
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version											
Cell Name	Function	Number of BC													
H6C	Tri-state Output ($I_{OL}=3.2\text{mA}$) & CMOS Interface Input Buffer (True)														
Cell Symbol		Propagation Delay Parameter													
		t _{up}		t _{dn}		Path $X \rightarrow IN$ $OT \rightarrow X$									
		t ₀	KCL	t ₀	KCL										
		0.92 2.42 (7.18)	0.04 0.056	1.33 2.52 (13.57)	0.04 0.13	C → X									
		L → Z		Z → L											
		t ₀	KCL	t ₀	KCL										
		2.07 (15.35)	*	2.55 (13.60)	0.13										
		H → Z		Z → H		C → X									
		t ₀	KCL	t ₀	KCL										
		3.41 (15.35)	*	2.31 (13.60)	0.056										
		Output Driving Factor (λ_u)		Input Loading Factor (λ_u)											
<table border="1"> <tr> <td>Pin Name</td> <td>OT</td> <td>4</td> </tr> <tr> <td></td> <td>C</td> <td>2</td> </tr> </table>		Pin Name	OT	4			C	2	<table border="1"> <tr> <td>Pin Name</td> <td>IN</td> <td>36</td> </tr> </table>		Pin Name	IN	36		
Pin Name	OT	4													
	C	2													
Pin Name	IN	36													
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>						2									
															
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.												
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>															
UHB-H6C-E4 Sheet 1/1			Page 20-51												

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version																											
Cell Name	Function	Number of BC																														
H6CU	Tri-state Output ($I_{OL}=3.2\text{mA}$) & CMOS Interface Input Buffer (True) with Pull-up Resistance																															
Cell Symbol		Propagation Delay Parameter																														
		<table border="1"> <thead> <tr> <th colspan="2">t_{up}</th><th colspan="3">t_{dn}</th></tr> <tr> <th>t_0</th><th>KCL</th><th>t_0</th><th>KCL</th><th>KCL2</th></tr> </thead> <tbody> <tr> <td>0.92 2.42 (7.18)</td><td>0.04 0.056</td><td>1.33 2.52 (13.57)</td><td>0.04 0.13</td><td></td></tr> <tr> <td></td><td></td><td></td><td></td><td>CDR2</td></tr> </tbody> </table>				t_{up}		t_{dn}			t_0	KCL	t_0	KCL	KCL2	0.92 2.42 (7.18)	0.04 0.056	1.33 2.52 (13.57)	0.04 0.13						CDR2	Path						
t_{up}		t_{dn}																														
t_0	KCL	t_0	KCL	KCL2																												
0.92 2.42 (7.18)	0.04 0.056	1.33 2.52 (13.57)	0.04 0.13																													
				CDR2																												
							$X \rightarrow IN$ $OT \rightarrow X$																									
		<table border="1"> <thead> <tr> <th colspan="2">$L \rightarrow Z$</th><th colspan="3">$Z \rightarrow L$</th></tr> <tr> <th>t_0</th><th>KCL</th><th>t_0</th><th>KCL</th><th></th></tr> </thead> <tbody> <tr> <td>2.07 (15.35)</td><td>*</td><td>2.55 (13.60)</td><td>0.13</td><td></td></tr> <tr> <td></td><td></td><td></td><td></td><td></td></tr> </tbody> </table>					$L \rightarrow Z$		$Z \rightarrow L$			t_0	KCL	t_0	KCL		2.07 (15.35)	*	2.55 (13.60)	0.13							$C \rightarrow X$					
$L \rightarrow Z$		$Z \rightarrow L$																														
t_0	KCL	t_0	KCL																													
2.07 (15.35)	*	2.55 (13.60)	0.13																													
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (ℓ_u)</th></tr> </thead> <tbody> <tr> <td>OT</td><td>4</td></tr> <tr> <td>C</td><td>2</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓ_u)	OT	4	C	2	<table border="1"> <thead> <tr> <th colspan="2">$H \rightarrow Z$</th><th colspan="3">$Z \rightarrow H$</th></tr> <tr> <th>t_0</th><th>KCL</th><th>t_0</th><th>KCL</th><th></th></tr> </thead> <tbody> <tr> <td>3.41 (15.35)</td><td>*</td><td>2.31 (13.60)</td><td>0.056</td><td></td></tr> <tr> <td></td><td></td><td></td><td></td><td></td></tr> </tbody> </table>					$H \rightarrow Z$		$Z \rightarrow H$			t_0	KCL	t_0	KCL		3.41 (15.35)	*	2.31 (13.60)	0.056						
Pin Name	Input Loading Factor (ℓ_u)																															
OT	4																															
C	2																															
$H \rightarrow Z$		$Z \rightarrow H$																														
t_0	KCL	t_0	KCL																													
3.41 (15.35)	*	2.31 (13.60)	0.056																													
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (ℓ_u)</th></tr> </thead> <tbody> <tr> <td>IN</td><td>36</td></tr> </tbody> </table>		Pin Name	Output Driving Factor (ℓ_u)	IN	36																											
Pin Name	Output Driving Factor (ℓ_u)																															
IN	36																															

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

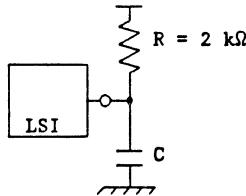
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

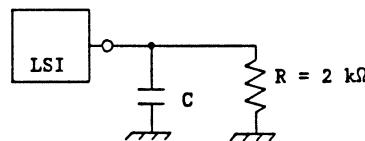
2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H6CD	Tri-state Output ($I_{OL}=3.2\text{mA}$) & CMOS Interface Input Buffer (True) with Pull-down Resistance					8	
Cell Symbol	Propagation Delay Parameter						
		t_{up}	t_{dn}			Path	
		t_0	KCL	t_0	KCL	$KCL2$	$CDR2$
		0.92 2.42 (7.18)	0.04 0.056	1.33 2.52 (13.57)	0.04 0.13		
						X → IN OT → X	
		$L \rightarrow Z$		$Z \rightarrow L$		$C \rightarrow X$	
		t_0	KCL	t_0	KCL		
		2.07 (15.35)	*	2.55 (13.60)	0.13		
		$H \rightarrow Z$		$Z \rightarrow H$			
		t_0	KCL	t_0	KCL		
		3.41 (15.35)	*	2.31 (13.60)	0.056		
Pin Name	Input Loading Factor (μu)						
OT	4						
C	2						
Pin Name	Output Driving Factor (μu)						
IN	36						

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of t_{pd} at LZ and ZL.

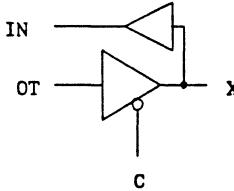
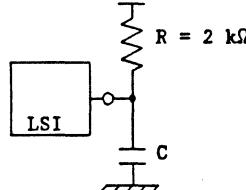
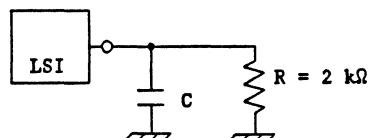


(b) Measurement of t_{pd} at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

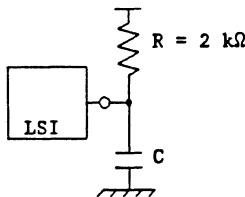
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

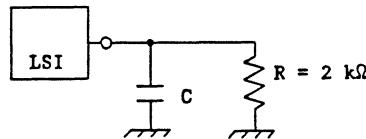
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version		
Cell Name	Function				Number of BC		
H6E	Tri-state Output(IOL=12mA) & CMOS Interface Input Buffer (True)				8		
Cell Symbol		Propagation Delay Parameter					
		tup	tdn		Path		
		t0 0.92 3.02 (6.25)	KCL 0.04 0.038	t0 1.33 4.12 (8.12)	KCL 0.04 0.047	X → IN OT → X	
		L → Z		Z → L		C → X	
		t0 2.96 (20.25)	KCL *	t0 3.69 (7.69)	KCL 0.047		
		H → Z		Z → H			
		t0 4.03 (20.25)	KCL *	t0 2.72 (7.69)	KCL 0.038		
Pin Name		Input Loading Factor (λ_u)					
OT		4					
C		2					
Pin Name		Output Driving Factor (λ_u)					
IN		36					
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>							
							
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.				
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H6EU	Tri-state Output(IOL=12mA) & CMOS Interface Input Buffer (True) with Pull-up Resistance					8	
Cell Symbol	Propagation Delay Parameter						
		tup	tdn	KCL	KCL2	CDR2	Path
		t0 0.92 3.02 (6.25)	KCL 0.04 0.038	t0 1.33 4.12 (8.12)	0.04 0.047		X → IN
							OT → X
		L → Z		Z → L		C → X	
		t0 2.96 (20.25)	KCL *	t0 3.69 (7.69)	KCL 0.047		
					<td data-kind="ghost"></td>		
		H → Z		Z → H		C → X	
		t0 4.03 (20.25)	KCL *	t0 2.72 (7.69)	KCL 0.038		
			<th></th> <td><td data-kind="ghost"></td></td>		<td data-kind="ghost"></td>		
Pin Name	Input Loading Factor (f <u>u</u>)						
OT	4						
C	2						
Pin Name	Output Driving Factor (f <u>u</u>)						
IN	36						

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

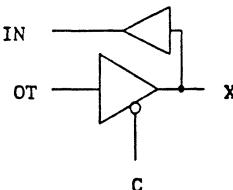


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

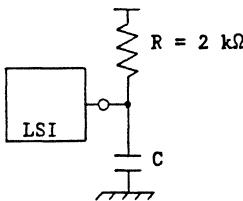
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

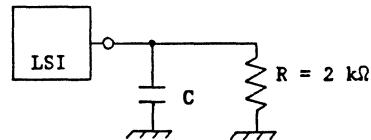
Cell Name	Function	Number of BC												
H6ED	Tri-state Output($I_{OL}=12mA$) & CMOS Interface Input Buffer (True) with Pull-down Resistance	8												
Cell Symbol	Propagation Delay Parameter						Path $X \rightarrow IN$ $OT \rightarrow X$							
	t_{up}		t_{dn}											
	t_0	KCL	t_0	KCL	KCL2	CDR2								
0.92 3.02 (6.25)	0.04 0.038	1.33 4.12 (8.12)	0.04 0.047				C \rightarrow X							
$L \rightarrow Z$														
t_0 2.96 (20.25)	KCL *	t_0 3.69 (7.69)	KCL 0.047											
$Z \rightarrow L$														
t_0 4.03 (20.25)	KCL *	t_0 2.72 (7.69)	KCL 0.038											
Pin Name	Input Loading Factor (μu)													
OT	4													
C	2													
Pin Name	Output Driving Factor (μu)													
IN	36													

* These values are subject to external loading condition.

Measurement circuits of propagation delay time at LZ, ZL, HZ andZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

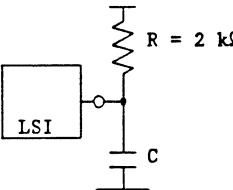
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

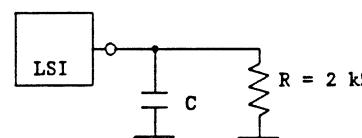
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version		
Cell Name	Function				Number of BC		
H6S	Tri-state Output(IOL=3.2mA) & Schmitt Trigger Input Buffer(CMOS Type, True)				12		
Cell Symbol	Propagation Delay Parameter						
		t _{up}	t _{dn}				
		t ₀	KCL	t ₀	KCL	KCL2	Path
		2.48 2.42 (7.18)	0.16 0.056	3.08 2.52 (13.57)	0.10 0.13		X → IN OT → X
		L → Z		Z → L		C → X	
		t ₀	KCL	t ₀	KCL		
		2.07 (15.35)	*	2.55 (13.60)	0.13		
		H → Z		Z → H		C → X	
		t ₀	KCL	t ₀	KCL		
		3.41 (15.35)	*	2.31 (13.60)	0.056		
Pin Name	Input Loading Factor (f <u>u</u>)						
OT	4						
C	2						
Pin Name	Output Driving Factor (f <u>u</u>)						
IN	18						

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

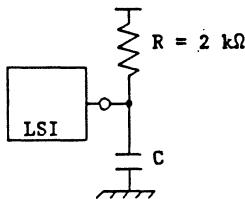


(b) Measurement of tpd at HZ and ZH.

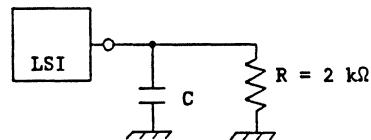
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version	
Cell Name	Function					Number of BC
H6SU	Tri-state Output($I_{OL}=3.2\text{mA}$) & Schmitt Trigger Input Buffer(CMOS Type, True) with Resistance					
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0 KCL	t0 KCL	KCL2	CDR2	Path
		2.48 0.16 (7.18)	3.08 0.10			X → IN
		2.42 0.056	2.52 0.13 (13.57)			OT → X
		L → Z		Z → L		C → X
		t0 KCL	t0 KCL			
		2.07 (15.35)	*	2.55 (13.60)	0.13	
		H → Z		Z → H		
		t0 KCL	t0 KCL			
		3.41 (15.35)	*	2.31 (13.60)	0.056	
Pin Name		Input Loading Factor (f_u)				
OT		4				
C		2				
Pin Name		Output Driving Factor (f_u)				
IN		18				

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



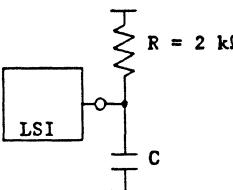
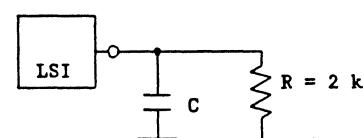
(b) Measurement of tpd at HZ and ZH.

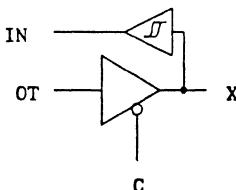
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

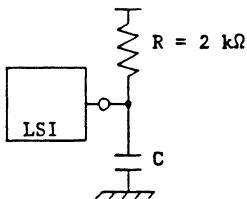
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H6SD	Tri-state Output($I_{OL}=3.2\text{mA}$) & Schmitt Trigger Input Buffer(CMOS Type, True) with Resistance					12	
Cell Symbol		Propagation Delay Parameter					
		t _{up}		t _{dn}		Path X → IN OT → X	
		t ₀	KCL	t ₀	KCL		
		2.48 (7.18)	0.16	3.08	0.10	C → X	
		2.42	0.056	2.52 (13.57)	0.13		
Pin Name Input Loading Factor (ℓu)		L → Z Z → L					
OT 4		t ₀	KCL	t ₀	KCL	C → X	
C 2		2.07 (15.35)	*	2.55 (13.60)	0.13		
Pin Name Output Driving Factor (ℓu)		H → Z Z → H					
IN 18		t ₀	KCL	t ₀	KCL	C → X	
IN 18		3.41 (15.35)	*	2.31 (13.60)	0.056		
* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:							
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.				
Note: 1. The unit of K _{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.							

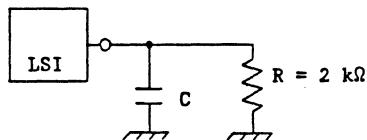
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H6R	Tri-state Output($I_{OL}=3.2\text{mA}$) & Schmitt Trigger Input Buffer (TTL Type, True)					12	
Cell Symbol	Propagation Delay Parameter						
		tup	tdn	KCL	KCL2	CDR2	Path
		t0 2.24 2.42 (7.18)	KCL 0.16 0.056	t0 3.72 2.52 (13.57)	0.13 0.13		X → IN OT → X
		L → Z	Z → L	KCL	t0 2.55 (13.60)	KCL 0.13	C → X
		t0 2.07 (15.35)	*				
Pin Name	Input Loading Factor (ℓu)						
OT	4						
C	2						
Pin Name	Output Driving Factor (ℓu)						
IN	18						
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>							
							
(a) Measurement of tpd at LZ and ZL.				(b) Measurement of tpd at HZ and ZH.			
<p>Note: 1. The unit of KCL for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>							
UHB-H6R-E2 Sheet 1/1				Page 20-60			

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H6RU	Tri-state Output($I_{OL}=3.2\text{mA}$) & Schmitt Trigger Input Buffer (TTL Type, True) with Pull-up Resistance					12	
Cell Symbol	Propagation Delay Parameter						
	tup	tdn				Path	
	t0 KCL	t0 KCL	KCL2	CDR2			
	2.24 2.42 (7.18)	0.16 0.056 (13.57)	3.72 2.52 (13.57)	0.13 0.13		X → IN OT → X	
	L → Z		Z → L			C → X	
	t0 KCL		t0 KCL				
	2.07 (15.35)	*	2.55 (13.60)	0.13			
	H → Z		Z → H				
	t0 KCL		t0 KCL				
	3.41 (15.35)	*	2.31 (13.60)	0.056			
Pin Name	Input Loading Factor (ℓu)						
OT	4						
C	2						
Pin Name	Output Driving Factor (ℓu)						
IN	18						

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

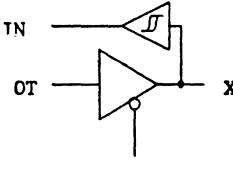


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

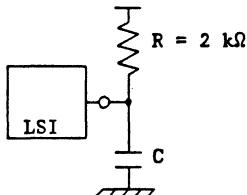
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

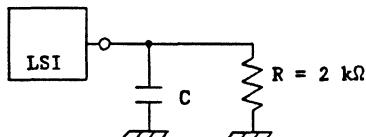
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version				
Cell Name	Function	Number of BC							
H6RD	Tri-state Output($I_{OL}=3.2\text{mA}$) & Schmitt Trigger Input Buffer (TTL Type, True) with Pull-down Resistance								
Cell Symbol		Propagation Delay Parameter							
		t _{up}		t _{dn}		Path			
		t ₀	KCL	t ₀	KCL	KCL2	CDR2		
		2.24 (7.18)	0.16 0.056	3.72 2.52 (13.57)	0.13 0.13				
		L → Z		Z → L		C → X			
		t ₀	KCL	t ₀	KCL	C → X			
		2.07 (15.35)	*	2.55 (13.60)	0.13	C → X			
		H → Z		Z → H		C → X			
		t ₀	KCL	t ₀	KCL	C → X			
		3.41 (15.35)	*	2.31 (13.60)	0.056	C → X			

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version		
Cell Name	Function						Number of BC		
H8T	Tri-state Output($I_{OL}=3.2\text{mA}$) with Noise Limit Resistance & Input Buffer (True)						9		
Cell Symbol	Propagation Delay Parameter								
		t _{up}		t _{dn}		Path			
		t ₀	KCL	t ₀	KCL	KCL2	CDR2		
		1.06 (7.88)	0.04	1.84	0.04				
		3.12	0.056	5.66 (16.71)	0.13				
		$L \rightarrow Z$		$Z \rightarrow L$		$C \rightarrow X$			
		t ₀	KCL	t ₀	KCL				
		2.22 (16.44)	*	6.47 (17.52)	0.13				
		$H \rightarrow Z$		$Z \rightarrow H$					
		t ₀	KCL	t ₀	KCL				
		3.07 (16.44)	*	3.20 (17.52)	0.056				
Pin Name	Input Loading Factor (ℓ_u)								
OT	2								
C	2								
Pin Name	Output Driving Factor (ℓ_u)								
IN	36								

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

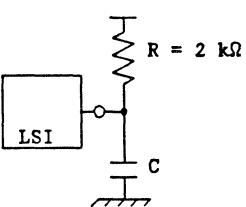
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

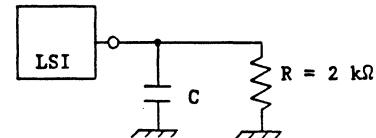
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
H8TU	Tri-state Output($I_{OL}=3.2\text{mA}$) with Noise Limit Resistance & Input Buffer (True) with Pull-up Resistance					9
Cell Symbol	Propagation Delay Parameter					
		t _{up}	t _{dn}			
		t ₀	KCL	t ₀	KCL	KCL2
		1.06 3.12 (7.88)	0.04 0.056	1.84 5.66 (16.71)	0.04 0.13	CDR2
						Path
						X → IN OT → X
		L → Z		Z → L		C → X
		t ₀	KCL	t ₀	KCL	
		2.22 (16.44)	*	6.47 (17.52)	0.13	
		H → Z		Z → H		
		t ₀	KCL	t ₀	KCL	
		3.07 (16.44)	*	3.20 (17.52)	0.056	
Pin Name	Input Loading Factor (ℓ_u)					
OT	2					
C	2					
Pin Name	Output Driving Factor (ℓ_u)					
IN	36					

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



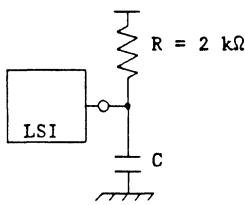
(a) Measurement of tpd at LZ and ZL.



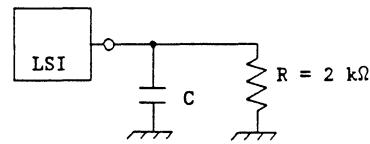
(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

2



(a) Measurement of tpd at LZ and ZL.

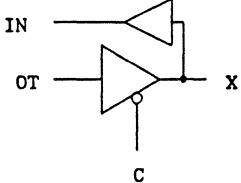
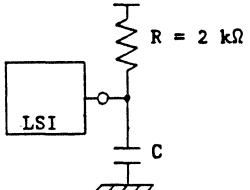
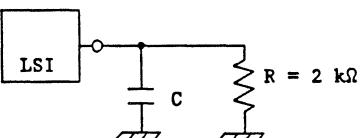


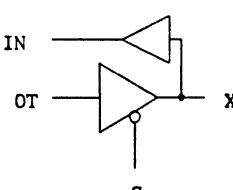
(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

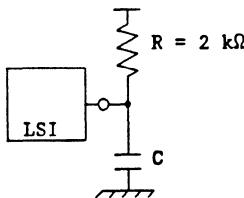
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

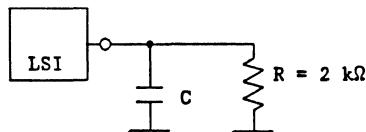
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version							
Cell Name	Function					Number of BC							
H8W	Tri-state Output($I_{OL}=12mA$) with Noise Limit Resistance & Input Buffer (True)					9							
Cell Symbol		Propagation Delay Parameter											
		t_{up} t ₀ 1.06 3.96 (7.19)	t_{dn} t ₀ 1.84 7.25 (11.84)	KCL	KCL2	CDR2	Path						
				0.04	0.04		X → IN OT → X						
		$L \rightarrow Z$ t ₀ 3.65 (21.73)	$Z \rightarrow L$ t ₀ 7.40 (11.99)	KCL	KCL		C → X						
				*	0.054								
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (μu)</th></tr> </thead> <tbody> <tr> <td>OT</td><td>2</td></tr> <tr> <td>C</td><td>2</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (μu)	OT	2	C	2	$H \rightarrow Z$ t ₀ 3.75 (21.73)	$Z \rightarrow H$ t ₀ 3.69 (11.99)	KCL	KCL		
Pin Name	Input Loading Factor (μu)												
OT	2												
C	2												
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (μu)</th></tr> </thead> <tbody> <tr> <td>IN</td><td>36</td></tr> </tbody> </table>				Pin Name	Output Driving Factor (μu)	IN	36	*	0.038				
Pin Name	Output Driving Factor (μu)												
IN	36												
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>													
													
(a) Measurement of tpd at LZ and ZL.				(b) Measurement of tpd at HZ and ZH.									
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.</p> <p>2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.</p> <p>3. The parameters in parentheses are the values applied to the simulation.</p>													
UHB-H8W-E2 Sheet 1/1				Page 20-66									

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H8WU	Tri-state Output(IOL=12mA) with Noise Limit Resistance & Input Buffer (True) with Pull-up Resistance					9	
Cell Symbol		Propagation Delay Parameter					
		t _{up}	t _{dn}				
		t ₀	KCL	t ₀	KCL	KCL2	
		1.06 3.96 (7.19)	0.04 0.038	1.84 7.25 (11.84)	0.04 0.054		X → IN OT → X
		L → Z		Z → L		C → X	
		t ₀	KCL	t ₀	KCL		
		3.65 (21.73)	*	7.40 (11.99)	0.054		
		H → Z		Z → H			
		t ₀	KCL	t ₀	KCL	2	
		3.75 (21.73)	*	3.69 (11.99)	0.038		
		Pin Name		Output Driving Factor (lu)			
		OT	2			2	
		C	2				
		Pin Name		Input Loading Factor (lu)			
		IN	36				

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time
 at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

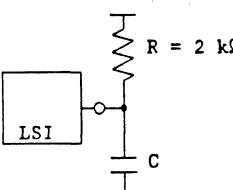
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

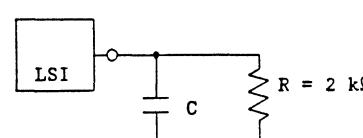
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
H8WD	Tri-state Output($I_{OL}=12\text{mA}$) with Noise Limit Resistance & Input Buffer (True) with Pull-down Resistance					9		
Cell Symbol	Propagation Delay Parameter							
		t _{up}	t _{dn}	KCL	KCL2	CDR2	Path	
		t ₀ 1.06 3.96 (7.19)	KCL 0.04 0.038	t ₀ 1.84 7.25 (11.84)	0.04 0.054		X → IN OT → X	
		L → Z		Z → L			C → X	
		t ₀ 3.65 (21.73)	KCL *	t ₀ 7.40 (11.99)	KCL 0.054			
		H → Z		Z → H				
		t ₀ 3.75 (21.73)	KCL *	t ₀ 3.69 (11.99)	KCL 0.038			
Pin Name	Input Loading Factor (ℓ_u)							
OT	2							
C	2							
Pin Name	Output Driving Factor (ℓ_u)							
IN	36							

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:

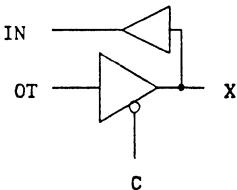


(a) Measurement of tpd at LZ and ZL.

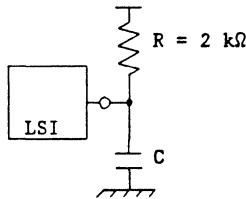


(b) Measurement of tpd at HZ and ZH.

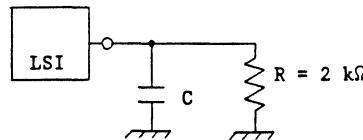
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version																				
Cell Name	Function					Number of BC																			
H8W2	Tri-state Output ($I_{OL}=24\text{mA}$) with Noise Limit Resistance & Input Buffer (TTL, True)																								
Cell Symbol		Propagation Delay Parameter																							
		<table border="1"> <thead> <tr> <th>t_{up}</th> <th colspan="3">t_{dn}</th> <th rowspan="2">Path</th> </tr> <tr> <th>t₀</th> <th>KCL</th> <th>t₀</th> <th>KCL</th> <th>KCL2</th> <th>CDR2</th> </tr> </thead> <tbody> <tr> <td>1.06 5.61 (8.33)</td><td>0.04 0.032</td><td>1.84 11.62 (16.72)</td><td>0.04 0.06</td><td></td><td></td><td>X → IN OT → X</td></tr> </tbody> </table>					t _{up}	t _{dn}			Path	t ₀	KCL	t ₀	KCL	KCL2	CDR2	1.06 5.61 (8.33)	0.04 0.032	1.84 11.62 (16.72)	0.04 0.06			X → IN OT → X	
t _{up}	t _{dn}			Path																					
t ₀	KCL	t ₀	KCL		KCL2	CDR2																			
1.06 5.61 (8.33)	0.04 0.032	1.84 11.62 (16.72)	0.04 0.06			X → IN OT → X																			
		<table border="1"> <thead> <tr> <th colspan="2">L → Z</th> <th colspan="2">Z → L</th> <th rowspan="2">C → X</th> </tr> <tr> <th>t₀</th> <th>KCL</th> <th>t₀</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>5.36 (23.23)</td><td>*</td><td>11.18 (16.28)</td><td>0.06</td><td></td></tr> </tbody> </table>					L → Z		Z → L		C → X	t ₀	KCL	t ₀	KCL	5.36 (23.23)	*	11.18 (16.28)	0.06						
L → Z		Z → L		C → X																					
t ₀	KCL	t ₀	KCL																						
5.36 (23.23)	*	11.18 (16.28)	0.06																						
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (ℓ_u)</th> </tr> </thead> <tbody> <tr> <td>OT</td> <td>2</td> </tr> <tr> <td>C</td> <td>2</td> </tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓ_u)	OT	2	C	2	<table border="1"> <thead> <tr> <th colspan="2">H → Z</th> <th colspan="2">Z → H</th> <th rowspan="2">C → X</th> </tr> <tr> <th>t₀</th> <th>KCL</th> <th>t₀</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>6.37 (23.23)</td><td>*</td><td>5.25 (16.28)</td><td>0.032</td><td></td></tr> </tbody> </table>				H → Z		Z → H		C → X	t ₀	KCL	t ₀	KCL	6.37 (23.23)	*	5.25 (16.28)	0.032	
Pin Name	Input Loading Factor (ℓ_u)																								
OT	2																								
C	2																								
H → Z		Z → H		C → X																					
t ₀	KCL	t ₀	KCL																						
6.37 (23.23)	*	5.25 (16.28)	0.032																						
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (ℓ_u)</th> </tr> </thead> <tbody> <tr> <td>IN</td> <td>36</td> </tr> </tbody> </table>		Pin Name	Output Driving Factor (ℓ_u)	IN	36																				
Pin Name	Output Driving Factor (ℓ_u)																								
IN	36																								

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time
 at LZ, ZL, HZ andZH are as follows:



(a) Measurement of tpd at LZ and ZL.

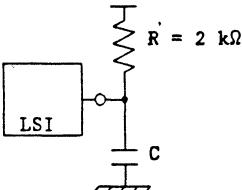


(b) Measurement of tpd at HZ and ZH.

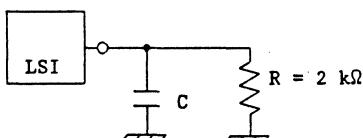
- Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
H8W1	Tri-state Output($I_{OL}=24\text{mA}$) with Noise Limit Resistance & Input Buffer (TTL, True) with Pull-up Resistance					11
Cell Symbol	Propagation Delay Parameter					
		tup	tdn	KCL2	CDR2	Path
		t0	KCL	t0	KCL	
		1.06 (8.33)	0.04	1.84 (16.72)	0.04 0.06	X → IN OT → X
		L → Z		Z → L		C → X
		t0	KCL	t0	KCL	
		5.36 (23.23)	*	11.18 (16.28)	0.06	
		H → Z		Z → H		
		t0	KCL	t0	KCL	
		6.37 (23.23)	*	5.25 (16.28)	0.032	
Pin Name	Input Loading Factor (ℓ_u)					
OT	2					
C	2					
Pin Name	Output Driving Factor (ℓ_u)					
IN	36					

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



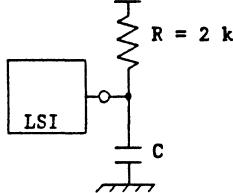
(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

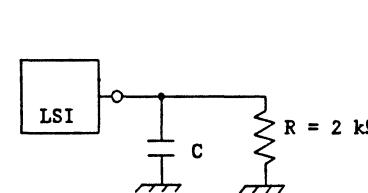
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version			
Cell Name	Function	Number of BC					
H8W0	Tri-state Output($I_{OL}=24\text{mA}$) with Noise Limit Resistance & Input Buffer (TTL, True) with Pull-down Resistance						
Cell Symbol		Propagation Delay Parameter					
		tup		tdn			
		t0	KCL	t0	KCL		
		1.06 5.61 (8.33)	0.04 0.032	1.84 11.62 (16.72)	0.04 0.06		
		KCL2		CDR2			
		Path					
		$X \rightarrow IN$ $OT \rightarrow X$					
		L \rightarrow Z		Z \rightarrow L			
		t0	KCL	t0	KCL		
		5.36 (23.23)	*	11.18 (16.28)	0.06		
		H \rightarrow Z		Z \rightarrow H			
		t0	KCL	t0	KCL		
		6.37 (23.23)	*	5.25 (16.28)	0.032		
		$C \rightarrow X$					
Pin Name	Input Loading Factor (μA)						
	OT	2					
Pin Name	Output Driving Factor (μA)						
	IN	36					
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>							
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.				
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H8C	Tri-state Output($I_{OL}=3.2mA$) with Noise Limit Resistance & CMOS Interface Input Buffer (True)					9	
Cell Symbol	Propagation Delay Parameter						
		tup		tdn		Path X → IN OT → X	
		t0	KCL	t0	KCL		KCL2
		0.92 (7.88)	0.04	1.33 (16.71)	0.04		
		3.12	0.056	5.66	0.13		
		L → Z		Z → L		C → X	
		t0	KCL	t0	KCL		
		2.22 (16.44)	*	6.47 (17.52)	0.13		
		H → Z		Z → H			
		t0	KCL	t0	KCL		
		3.07 (16.44)	*	3.20 (17.52)	0.056		
Pin Name	Input Loading Factor (λ_L)						
OT	2						
C	2						
Pin Name	Output Driving Factor (λ_O)						
IN	36						

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

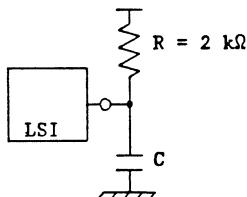
Note: 1. The unit of K_{SI} for paths OT, C to X is ns/pE.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

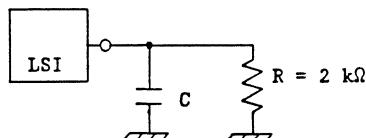
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
H8CU	Tri-state Output(IOL=3.2mA) w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-up Resistance					9
Cell Symbol	Propagation Delay Parameter					
		tup	tdn			
		t0 KCL	t0' KCL	KCL2	CDR2	Path
		0.92 0.04 3.12 0.056 (7.88)	1.33 0.04 5.66 0.13 (16.71)			X → IN OT → X
		L → Z		Z → L		C → X
		t0 KCL	t0' KCL			
		2.22 (16.44)	*	6.47 (17.52)	0.13	
		H → Z		Z → H		
		t0 KCL	t0' KCL			
		3.07 (16.44)	*	3.20 (17.52)	0.056	
Pin Name	Input Loading Factor (ℓu)					
OT	2					
C	2					
Pin Name	Output Driving Factor (ℓu)					
IN	36					

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

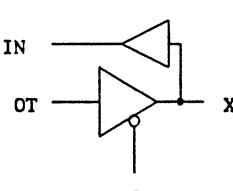


(b) Measurement of tpd at HZ and ZH.

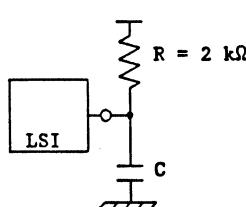
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

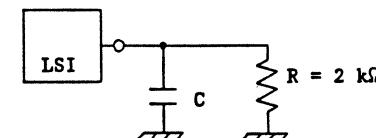
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version						
Cell Name	Function						Number of BC						
H8CD	Tri-state Output(IOL=3.2mA) w/ Noise Limit Resistance & CMOS Interface Input Buffer(True) w/ Pull-down Resistance												
Cell Symbol		Propagation Delay Parameter											
		t _{up}	td _n	KCL	KCL2	CDR2	Path						
		t ₀ 0.92 3.12 (7.88)	t ₀ 1.33 5.66 (16.71)	KCL 0.04 0.056	KCL2	CDR2	X → IN OT → X						
		L → Z		Z → L									
		t ₀ 2.22 (16.44)	KCL *	t ₀ 6.47 (17.52)	KCL 0.13	C → X							
		H → Z		Z → H									
		t ₀ 3.07 (16.44)	KCL *	t ₀ 3.20 (17.52)	KCL 0.056								
<table border="1"> <tr> <th>Pin Name</th> <th>Input Loading Factor (μu)</th> </tr> <tr> <td>OT</td> <td>2</td> </tr> <tr> <td>C</td> <td>2</td> </tr> </table>		Pin Name	Input Loading Factor (μ u)	OT	2	C	2						
Pin Name	Input Loading Factor (μ u)												
OT	2												
C	2												
<table border="1"> <tr> <th>Pin Name</th> <th>Output Driving Factor (μu)</th> </tr> <tr> <td>IN</td> <td>36</td> </tr> </table>		Pin Name	Output Driving Factor (μ u)	IN	36								
Pin Name	Output Driving Factor (μ u)												
IN	36												

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:

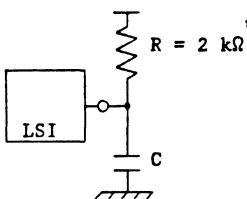
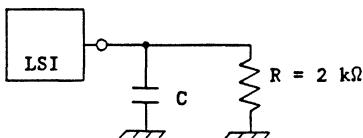


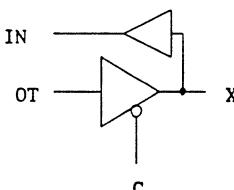
(a) Measurement of tpd at LZ and ZL.



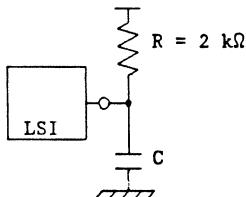
(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.

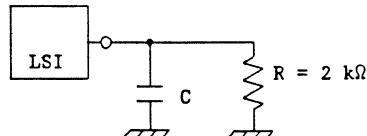
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version			
Cell Name	Function					Number of BC			
H8E	Tri-state Output($I_{OL}=12mA$) with Noise Limit Resistance & CMOS Interface Input Buffer (True)					9			
Cell Symbol	Propagation Delay Parameter								
		t _{up}	t _{dn}			Path			
		t ₀	KCL	t ₀	KCL	KCL2	CDR2		
		0.92 3.96 (7.19)	0.04 0.038	1.33 7.25 (11.84)	0.04 0.054			X → IN OT → X	
		L → Z		Z → L		C → X			
		t ₀	KCL	t ₀	KCL				
		3.65 (21.73)	*	7.40 (11.99)	0.054				
		H → Z		Z → H					
		t ₀	KCL	t ₀	KCL				
		3.75 (21.73)	*	3.69 (11.99)	0.038				
Pin Name	Input Loading Factor (ℓu)								
OT	2								
C	2								
Pin Name	Output Driving Factor (ℓu)								
IN	36								
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>									
									
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.						
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>									

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version						
Cell Name	Function					Number of BC						
H8EU	Tri-state Output(IOL=12mA) with Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-up Resistance					9						
Cell Symbol		Propagation Delay Parameter										
		<i>t_{up}</i>	<i>t_{dn}</i>									
		<i>t₀</i>	KCL	<i>t₀</i>	KCL	KCL2						
		0.92 3.96 (7.19)	0.04 0.038	1.33 7.25 (11.84)	0.04 0.054	CDR2	Path					
						X → IN OT → X						
		<i>L → Z</i>		<i>Z → L</i>		C → X						
		<i>t₀</i>	KCL	<i>t₀</i>	KCL							
		3.65 (21.73)	*	7.40 (11.99)	0.054							
		<i>H → Z</i>		<i>Z → H</i>								
		<i>t₀</i>	KCL	<i>t₀</i>	KCL							
		3.75 (21.73)	*	3.69 (11.99)	0.038							
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (μu)</th></tr> </thead> <tbody> <tr> <td>OT</td><td>2</td></tr> <tr> <td>C</td><td>2</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (μ u)	OT	2		C	2				
Pin Name	Input Loading Factor (μ u)											
OT	2											
C	2											
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (μu)</th></tr> </thead> <tbody> <tr> <td>IN</td><td>36</td></tr> </tbody> </table>		Pin Name	Output Driving Factor (μ u)	IN	36							
Pin Name	Output Driving Factor (μ u)											
IN	36											

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time
 at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

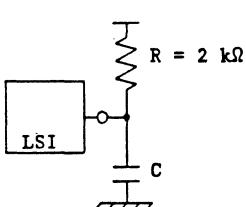
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

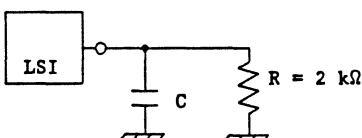
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
H8ED	Tri-state Output(IOL=12mA) with Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-down Resistance					9		
Cell Symbol	Propagation Delay Parameter							
		t _{up}	t _{dn}			Path		
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	X → IN OT → X
		0.92 3.96 (7.19)		1.33 7.25 (11.84)	0.04 0.054			
		L → Z		Z → L		C → X		
		t ₀	KCL	t ₀	KCL			
		3.65 (21.73)	*	7.40 (11.99)	0.054			
		H → Z		Z → H		3.75 (21.73)	0.038	
		t ₀	KCL	t ₀	KCL			
			*	3.69 (11.99)				
Pin Name	Input Loading Factor (lu)							
OT	2							
C	2							
Pin Name	Output Driving Factor (lu)							
IN	36							

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:

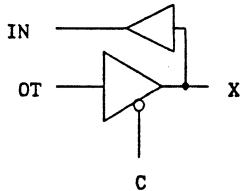


(a) Measurement of tpd at LZ and ZL.

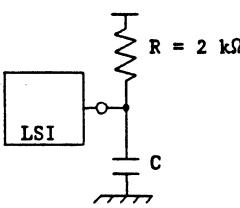


(b) Measurement of tpd at HZ and ZH.

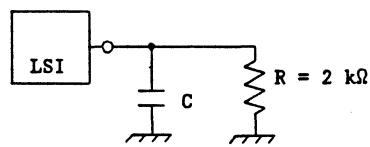
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H8E2	Tri-state Output(IOL=24mA) w/ Noise Limit Resistance & Input Buffer (CMOS, True)					11	
Cell Symbol		Propagation Delay Parameter					
		t _{up}	t _{dn}				
		t ₀	KCL	t ₀	KCL	KCL2	
		0.92 5.61 (8.33)	0.04 0.032	1.33 11.62 (16.72)	0.04 0.06	CDR2	Path X → IN OT → X
		L → Z		Z → L		C → X	
		t ₀	KCL	t ₀	KCL		
		5.36 (23.23)	*	11.18 (16.28)	0.06		
		H → Z		Z → H			
		t ₀	KCL	t ₀	KCL		
		6.37 (23.23)	*	5.25 (16.28)	0.032		
Pin Name		Output Driving Factor (f _u)					
OT	2						
C	2						
Pin Name		Input Loading Factor (f _u)					
IN	36						

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

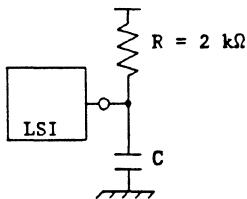


(b) Measurement of tpd at HZ and ZH.

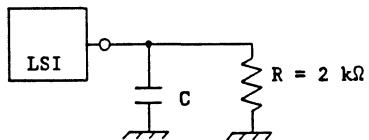
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version		
Cell Name	Function				Number of BC		
H8E1	Tri-state Output($I_{OL}=24\text{mA}$) w/ Noise Limit Resistance & Input Buffer(CMOS, True) w/ Pull-up Resistance				11		
Cell Symbol	Propagation Delay Parameter						
		tup	tdn			Path	
		t0	KCL	t0	KCL		KCL2
		0.92 5.61 (8.33)	0.04 0.032	1.33 11.62 (16.72)	0.04 0.06		
		X → IN OT → X					
		L → Z Z → L				C → X	
		t0	KCL	t0	KCL		
		5.36 (23.23)	*	11.18 (16.28)	0.06		
		H → Z Z → H					
		t0	KCL	t0	KCL		
		6.37 (23.23)	*	5.25 (16.28)	0.032		
Pin Name	Input Loading Factor (ℓu)						
OT	2						
C	2						
Pin Name	Output Driving Factor (ℓu)						
IN	36						

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

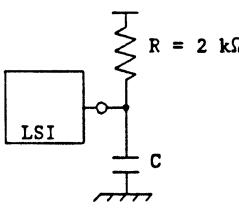
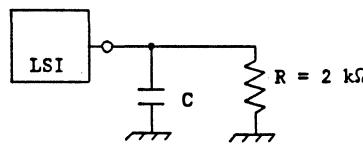


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

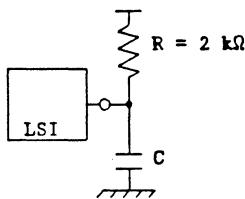
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
H8E0	Tri-state Output(IOL=24mA) w/ Noise Limit Resistance & Input Buffer(CMOS, True) w/ Pull-down Resistance					11
Cell Symbol	Propagation Delay Parameter					
		tup	tdn			
		t0	KCL	t0	KCL	KCL2
		0.92 5.61 (8.33)	0.04 0.032	1.33 11.62 (16.72)	0.04 0.06	CDR2
		X → IN OT → X				
		L → Z		Z → L		C → X
		t0	KCL	t0	KCL	
		5.36 (23.23)	*	11.18 (16.28)	0.06	
		H → Z		Z → H		
		t0	KCL	t0	KCL	
		6.37 (23.23)	*	5.25 (16.28)	0.032	
Pin Name	Input Loading Factor (ℓ_u)					
OT	2					
C	2					
Pin Name	Output Driving Factor (ℓ_u)					
IN	36					
* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:						
						
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.			
Note: 1. The unit of K _{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.						

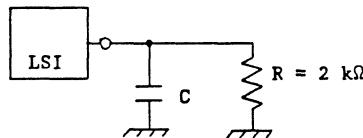
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function					Number of BC		
H8S	Tri-State Output ($I_{OL}=3.2\text{mA}$) & Schmitt Trigger Input Buffer (CMOS Type, True) w/ Noise Limit Resistance					13		
Cell Symbol	Propagation Delay Parameter							
		t _{up}	td _n			Path		
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	X → IN OT → X
		2.48 3.12 (7.88)	0.16 0.056	3.08 5.66 (16.71)	0.10 0.13			
		L → Z		Z → L		C → X		
		t ₀	KCL	t ₀	KCL			
		2.22 (16.44)	*	6.47 (17.52)	0.13			
		H → Z		Z → H				
		t ₀	KCL	t ₀	KCL			
		3.07 (16.44)	*	3.20 (17.52)	0.056			
Pin Name	Input Loading Factor (ℓ_u)							
OT	2							
C	2							
Pin Name	Output Driving Factor (ℓ_u)							
IN	18							

* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

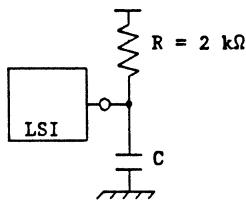
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

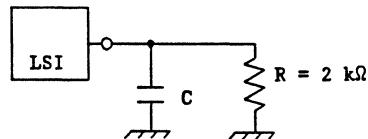
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
H8SU	Tri-state Output($I_{OL}=3.2\text{mA}$) & Schmitt Trigger Input Buffer(CMOS Type,True) w/ Noise Limit Resistance w/ Pull-up Resistance					13
Cell Symbol	Propagation Delay Parameter					
		t _{up}	t _{dn}			
		t ₀	KCL	t ₀	KCL	KCL2
		2.48 3.12 (7.88)	0.16 0.056	3.08 5.66 (16.71)	0.10 0.13	CDR2
						Path
						X → IN OT → X
		L → Z		Z → L		C → X
		t ₀	KCL	t ₀	KCL	
		2.22 (16.44)	*	6.47 (17.52)	0.13	
		H → Z		Z → H		C → X
		t ₀	KCL	t ₀	KCL	
		3.07 (16.44)	*	3.20 (17.52)	0.056	
Pin Name	Input Loading Factor (ℓu)					
OT	2					
C	2					
Pin Name	Output Driving Factor (ℓu)					
IN	18					

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

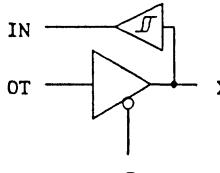
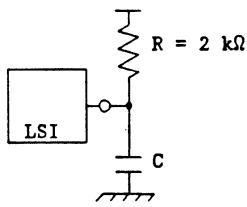
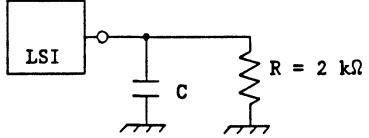


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H8SD	Tri-state Output(IOL=3.2mA) & Schmitt Trigger Input Buffer(CMOS Type ,True) w/ Noise Limit Resistance w/ Pull-down Resistance					13	
Cell Symbol		Propagation Delay Parameter					
		t _{up}	t _{dn}	KCL2	CDR2	Path	
		t ₀ 2.48 3.12 (7.88)	KCL 0.16 0.056	t ₀ 3.08 5.66 (16.71)	KCL 0.10 0.13	X → IN OT → X	
		L → Z		Z → L		C → X	
		t ₀ 2.22 (16.44)	KCL *	t ₀ 6.47 (17.52)	KCL 0.13		
		H → Z		Z → H			
		t ₀ 3.07 (16.44)	KCL *	t ₀ 3.20 (17.52)	KCL 0.056		
Pin Name		Input Loading Factor (f <u>u</u>)					
OT	2						
C	2						
Pin Name		Output Driving Factor (f <u>u</u>)					
IN	18						
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>							
							
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.				
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.</p>							

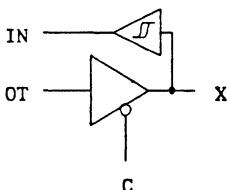
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version		
Cell Name	Function					Number of BC		
H8R	Tri-state Output ($I_{OL}=3.2\text{mA}$) & Schmitt Trigger Input Buffer (TTL Type, True) w/ Noise Limit Resistance					13		
Cell Symbol	Propagation Delay Parameter							
		tup	tdn			Path		
		t0	KCL	t0	KCL	KCL2	CDR2	X → IN OT → X
		2.24 (7.88)	0.16 0.056	3.72 (16.71)	0.13 0.13			
		L → Z		Z → L			C → X	
		t0	KCL	t0	KCL			
		2.22 (16.44)	*	6.47 (17.52)	0.13			
		H → Z		Z → H				
		t0	KCL	t0	KCL			
		3.07 (16.44)	*	3.20 (17.52)	0.056			
Pin Name	Input Loading Factor (f <u>u</u>)							
OT	2							
C	2							
Pin Name	Output Driving Factor (f <u>u</u>)							
IN	18							

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ andZH are as follows:

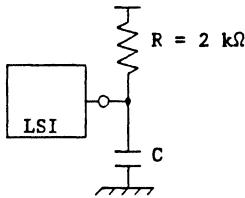
(a) Measurement of tpd at LZ and ZL.

(b) Measurement of tpd at HZ and ZH.

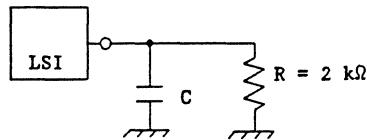
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H8RU	Tri-state Output(IOL=3.2mA) & Schmitt Trigger Input Buffer(TTL Type, True) w/ Noise Limit Resistance w/ Pull-up Resistance					13	
Cell Symbol		Propagation Delay Parameter					
		tup	tdn	KCL	KCL2	CDR2	
		t0 2.24 3.12 (7.88)	KCL 0.16 0.056	t0 3.72 5.66 (16.71)	0.13		Path $X \rightarrow IN$ $OT \rightarrow X$
		L → Z		Z → L		C → X	
		t0 2.22 (16.44)	KCL *	t0 6.47 (17.52)	KCL 0.13		
		H → Z		Z → H			
		t0 3.07 (16.44)	KCL *	t0 3.20 (17.52)	KCL 0.056		
Pin Name		Input Loading Factor (ℓu)					
OT		2					
C		2					
Pin Name		Output Driving Factor (ℓu)					
IN		18					

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:

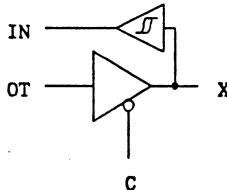


(a) Measurement of tpd at LZ and ZL.

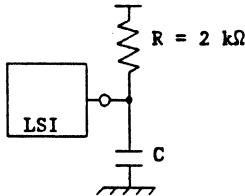


(b) Measurement of tpd at HZ and ZH.

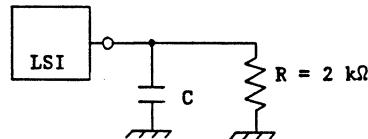
- Note:
1. The unit of K_{CL} for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																															
Cell Name	Function	Number of BC																																	
H8RD	Tri-state Output(IOL=3.2mA) & Schmitt Trigger Input Buffer(TTL Type, True) w/ Noise Limit Resistance w/ Pull-down Resistance																																		
Cell Symbol		Propagation Delay Parameter																																	
		<table border="1"> <thead> <tr> <th>t_{up}</th> <th colspan="4">t_{dn}</th> <th rowspan="2">Path</th> </tr> <tr> <th>t₀</th> <th>KCL</th> <th>t₀</th> <th>KCL</th> <th>KCL2</th> <th>CDR2</th> </tr> </thead> <tbody> <tr> <td>2.24 (7.88)</td> <td>0.16</td> <td>3.72</td> <td>0.13</td> <td></td> <td>X → IN</td> </tr> <tr> <td>3.12</td> <td>0.056</td> <td>5.66</td> <td>0.13</td> <td></td> <td>OT → X</td> </tr> <tr> <td></td> <td></td> <td>(16.71)</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>				t _{up}	t _{dn}				Path	t ₀	KCL	t ₀	KCL	KCL2	CDR2	2.24 (7.88)	0.16	3.72	0.13		X → IN	3.12	0.056	5.66	0.13		OT → X			(16.71)			
t _{up}	t _{dn}				Path																														
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* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

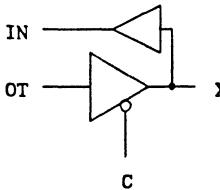


(b) Measurement of tpd at HZ and ZH.

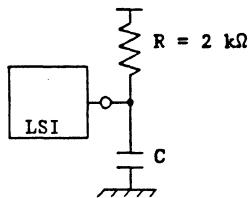
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

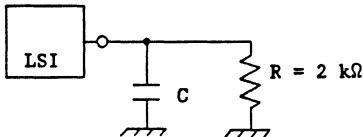
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version						
Cell Name	Function	Number of BC								
H6TF	Tri-state Output ($I_{OL}=8mA$) & Input Buffer (True)									
Cell Symbol		Propagation Delay Parameter								
		t_{up}	t_{dn}							
		t_0	KCL	t_0	KCL					
		1.06 (7.27)	0.04	1.84 (8.63)	0.04					
		2.51	0.056	3.27	0.063					
				KCL2	CDR2					
					Path					
					X → IN OT → X					
		$L \rightarrow Z$		$Z \rightarrow L$						
		t_0	KCL	t_0	KCL					
		2.29 (18.62)	*	3.35 (8.71)	0.063					
		$H \rightarrow Z$		$Z \rightarrow H$						
		t_0	KCL	t_0	KCL					
		3.12 (18.62)	*	2.37 (8.71)	0.056					
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (ℓu)</th></tr> </thead> <tbody> <tr> <td>OT</td><td>4</td></tr> <tr> <td>C</td><td>2</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓu)	OT	4	C	2			
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C	2									
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Pin Name	Output Driving Factor (ℓu)									
IN	36									

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time
 at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

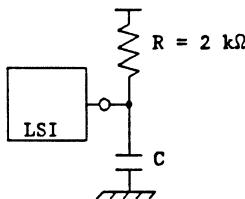


(b) Measurement of tpd at HZ and ZH.

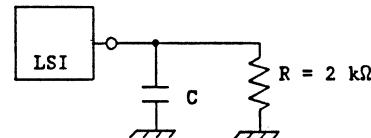
- Note:
1. The unit of KCL for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version																												
Cell Name	Function						Number of BC																												
H6TFU	Tri-state Output($I_{OL}=8mA$) & Input Buffer (True) with Pull-up Resistance						8																												
Cell Symbol	Propagation Delay Parameter																																		
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="5">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th><th>Path</th></tr> </thead> <tbody> <tr> <td>1.06 (7.27)</td><td>0.04</td><td>1.84</td><td>0.04</td><td></td><td></td><td>X → IN</td></tr> <tr> <td>2.51</td><td>0.056</td><td>3.27 (8.63)</td><td>0.063</td><td></td><td></td><td>OT → X</td></tr> </tbody> </table>							tup		tdn					t0	KCL	t0	KCL	KCL2	CDR2	Path	1.06 (7.27)	0.04	1.84	0.04			X → IN	2.51	0.056	3.27 (8.63)	0.063			OT → X
tup		tdn																																	
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(a) Measurement of tpd at LZ and ZL.

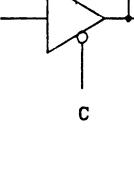


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

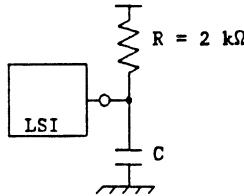
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

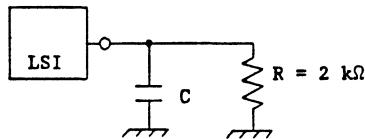
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																																				
Cell Name	Function	Number of BC																																						
H6TFD	Tri-state Output ($I_{OL}=8mA$) & Input Buffer (True) with Pull-down Resistance																																							
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2

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time
 at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

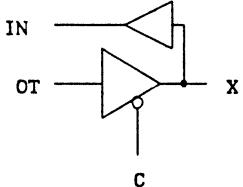


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

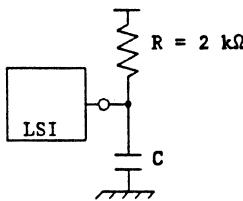
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3. The parameters in parentheses are the values applied to the simulation.

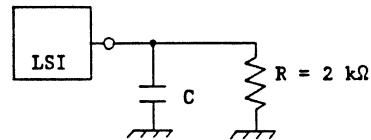
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version						
Cell Name	Function						Number of BC						
H6CF	Tri-state Output(IOL=8mA) & CMOS Interface Input Buffer (True)						8						
Cell Symbol		Propagation Delay Parameter											
		t _{up}	t _{dn}			Path							
		t ₀ 0.92 (7.27)	KCL 0.04 0.056	t ₀ 1.33 (8.63)	KCL 0.04 0.063	KCL2	CDR2	X → IN OT → X					
		$L + Z$		$Z \rightarrow L$		C → X							
		t ₀ 2.29 (18.62)	KCL *	t ₀ 3.35 (8.71)	KCL 0.063								
		$H \rightarrow Z$		$Z \rightarrow H$									
		t ₀ 3.12 (18.62)	KCL *	t ₀ 2.37 (8.71)	KCL 0.056								
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Measurement circuits of propagation delay time at LZ, ZL, HZ andZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

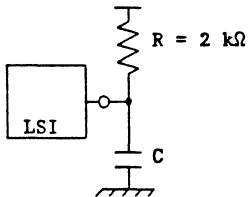
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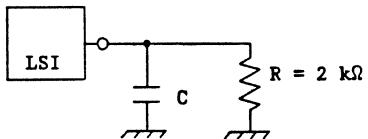
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version							
Cell Name	Function				Number of BC						
H6CFU	Tri-state Output ($I_{OL}=8mA$) & CMOS Interface Input Buffer (True) with Pull-up Resistance										
Cell Symbol		Propagation Delay Parameter									
		tup	tdn	KCL	Path						
		t0 0.92 2.51 (7.27)	t0 1.33 3.27 (8.63)	KCL 0.04 0.056	X → IN OT → X						
		L → Z		Z → L							
		t0 2.29 (18.62)	KCL *	t0 3.35 (8.71)	KCL 0.063						
		H → Z		Z → H							
		t0 3.12 (18.62)	KCL *	t0 2.37 (8.71)	KCL 0.056						
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Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



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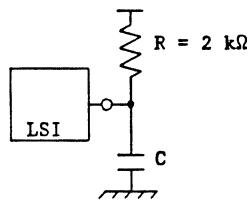
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3. The parameters in parentheses are the values applied to the simulation.

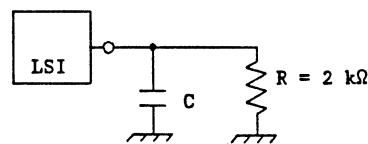
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version		
Cell Name	Function					Number of BC	
H6CFD	Tri-state Output($I_{OL}=8mA$) & CMOS Interface Input Buffer (True) with Pull-down Resistance						
Cell Symbol		Propagation Delay Parameter					
		t_{up}	t_{dn}				
		t₀	KCL	t₀	KCL	KCL2	
		0.92 (7.27)	0.04 0.056	1.33 (8.63)	0.04 0.063	CDR2	
		L + Z		Z + L		C → X	
		t₀	KCL	t₀	KCL		
		2.29 (18.62)	*	3.35 (8.71)	0.063		
		H → Z		Z → H		C → X	
		t₀	KCL	t₀	KCL		
		3.12 (18.62)	*	2.37 (8.71)	0.056		
		Pin Name		Input Loading Factor (λ_u)		C → X	
		OT	4				
		C	2				
		Pin Name		Output Driving Factor (λ_u)		C → X	
		IN	36				

* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

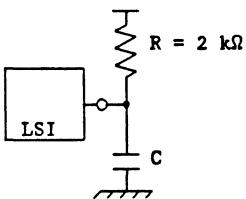
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

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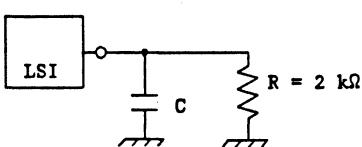
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version	
Cell Name	Function					Number of BC	
H8TF	Tri-state Output($I_{OL}=8mA$) with Noise Limit Resistance & Input Buffer (True)					9	
Cell Symbol	Propagation Delay Parameter						
		t _{up}	td _n				
		t ₀	KCL	t ₀	KCL	KCL2	
		1.06 3.21 (7.97)	0.04 0.056	1.84 5.96 (11.91)	0.04 0.070	CDR2	
						Path	
						X → IN OT → X	
		L → Z		Z → L		C → X	
		t ₀	KCL	t ₀	KCL		
		2.62 (19.71)	*	6.82 (12.77)	0.070		
		H → Z		Z → H			
		t ₀	KCL	t ₀	KCL		
		3.30 (19.71)	*	3.21 (12.77)	0.056		
		Input Loading Factor (ℓ_u)					
OT	2						
C	2						
		Output Driving Factor (ℓ_u)					
Pin Name							
IN	36						

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



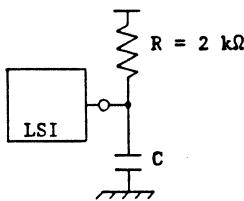
(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
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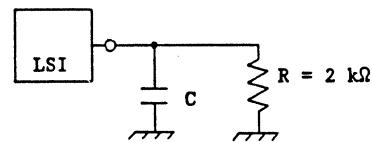
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version
Cell Name	Function					Number of BC
H8TFU	Tri-state Output($I_{OL}=8mA$) with Noise Limit Resistance & Input Buffer (True) with Pull-up Resistance					9
Cell Symbol	Propagation Delay Parameter					
		t _{up}	t _{dn}			
		t ₀	KCL	t ₀	KCL	KCL2
		1.06 (7.97)	0.04 0.056	1.84 (11.91)	0.04 0.070	CDR2
						Path
						X → IN OT → X
		L → Z		Z → L		C → X
		t ₀	KCL	t ₀	KCL	
		2.62 (19.71)	*	6.82 (12.77)	0.070	
		H → Z		Z → H		
		t ₀	KCL	t ₀	KCL	
		3.30 (19.71)	*	3.21 (12.77)	0.056	
Pin Name	Input Loading Factor (ℓ_u)					
OT	2					
C	2					
Pin Name	Output Driving Factor (ℓ_u)					
IN	36					

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Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

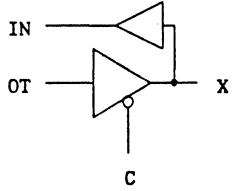


(b) Measurement of tpd at HZ and ZH.

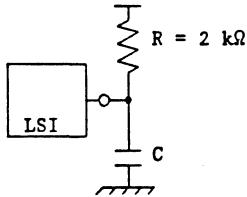
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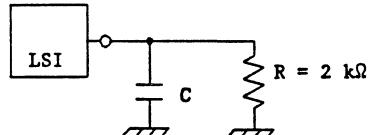
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							"UHB" Version							
Cell Name	Function						Number of BC							
H8TFD	Tri-state Output($I_{OL}=8mA$) with Noise Limit Resistance & Input Buffer (True) with Pull-down Resistance													
Cell Symbol		Propagation Delay Parameter												
		t_{up}	t_{dn}				Path $X \rightarrow IN$ $OT \rightarrow X$							
		t_0	KCL	t_0	KCL	KCL2	CDR2							
		1.06 (7.97)	0.04	1.84 (11.91)	0.04			$C \rightarrow X$						
		3.21	0.056	5.96	0.070									
		$L \rightarrow Z$		$Z \rightarrow L$										
		t_0	KCL	t_0	KCL									
		2.62 (19.71)	*	6.82 (12.77)	0.070									
		$H \rightarrow Z$		$Z \rightarrow H$										
		t_0	KCL	t_0	KCL									
		3.30 (19.71)	*	3.21 (12.77)	0.056									
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Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:

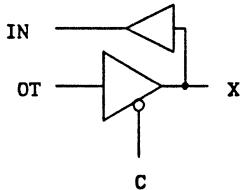


(a) Measurement of tpd at LZ and ZL.



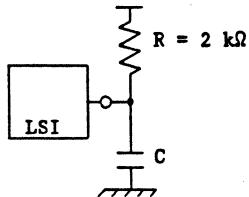
(b) Measurement of tpd at HZ and ZH.

- Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
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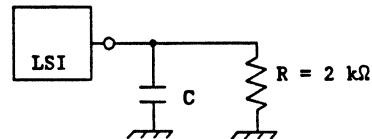
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"UHB" Version																		
Cell Name	Function	Number of BC																				
H8CF	Tri-state Output($I_{OL}=8mA$) with Noise Limit Resistance & CMOS Interface Input Buffer (True)																					
Cell Symbol		Propagation Delay Parameter																				
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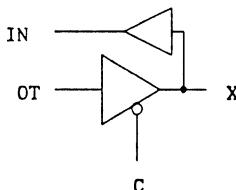


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Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

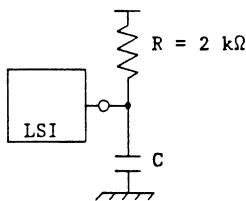
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

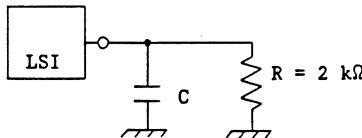
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																
Cell Name	Function					Number of BC																
H8CFU	Tri-state Output(IOL=8mA) w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-up Resistance					9																
Cell Symbol		Propagation Delay Parameter																				
		<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="2">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>0.92 (7.97)</td><td>0.04</td><td>1.33 (11.91)</td><td>0.04</td></tr> <tr> <td>3.21</td><td>0.056</td><td>5.96</td><td>0.070</td></tr> </tbody> </table>				tup		tdn		t0	KCL	t0	KCL	0.92 (7.97)	0.04	1.33 (11.91)	0.04	3.21	0.056	5.96	0.070	Path
tup		tdn																				
t0	KCL	t0	KCL																			
0.92 (7.97)	0.04	1.33 (11.91)	0.04																			
3.21	0.056	5.96	0.070																			
						X → IN OT → X																
		<table border="1"> <thead> <tr> <th colspan="2">L → Z</th><th colspan="2">Z → L</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>2.62 (19.71)</td><td>*</td><td>6.82 (12.77)</td><td>0.070</td></tr> </tbody> </table>				L → Z		Z → L		t0	KCL	t0	KCL	2.62 (19.71)	*	6.82 (12.77)	0.070	C → X				
L → Z		Z → L																				
t0	KCL	t0	KCL																			
2.62 (19.71)	*	6.82 (12.77)	0.070																			
		<table border="1"> <thead> <tr> <th colspan="2">H → Z</th><th colspan="2">Z → H</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>3.30 (19.71)</td><td>*</td><td>3.21 (12.77)</td><td>0.056</td></tr> </tbody> </table>				H → Z		Z → H		t0	KCL	t0	KCL	3.30 (19.71)	*	3.21 (12.77)	0.056					
H → Z		Z → H																				
t0	KCL	t0	KCL																			
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<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (f<u>u</u>)</th></tr> </thead> <tbody> <tr> <td>OT</td><td>2</td></tr> <tr> <td>C</td><td>2</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (f <u>u</u>)	OT	2	C	2															
Pin Name	Input Loading Factor (f <u>u</u>)																					
OT	2																					
C	2																					
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (f<u>u</u>)</th></tr> </thead> <tbody> <tr> <td>IN</td><td>36</td></tr> </tbody> </table>		Pin Name	Output Driving Factor (f <u>u</u>)	IN	36																	
Pin Name	Output Driving Factor (f <u>u</u>)																					
IN	36																					

* These values are subject to external loading condition.

Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

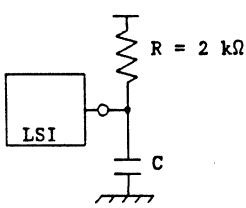
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

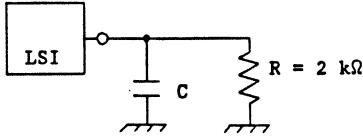
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION					"UHB" Version			
Cell Name	Function					Number of BC		
H8CFD	Tri-state Output(IOL=8mA) w/ Noise Limit Resistance & CMOS Interface Input Buffer(True) w/ Pull-down Resistance					9		
Cell Symbol	Propagation Delay Parameter							
		t _{up}	t _{dn}			Path		
		t ₀	KCL	t ₀	KCL	KCL2	CDR2	X → IN OT → X
		0.92 3.21 (7.97)	0.04 0.056	1.33 5.96 (11.91)	0.04 0.070			
		L → Z		Z → L		C → X		
		t ₀	KCL	t ₀	KCL			
		2.62 (19.71)	*	6.82 (12.77)	0.070			
		H → Z		Z → H				
		t ₀	KCL	t ₀	KCL			
		3.30 (19.71)	*	3.21 (12.77)	0.056			
Pin Name	Input Loading Factor (f _u)							
OT	2							
C	2							
Pin Name	Output Driving Factor (f _u)							
IN	36							

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:

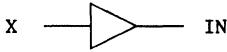


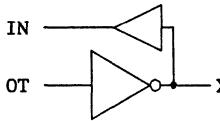
(a) Measurement of tpd at LZ and ZL.



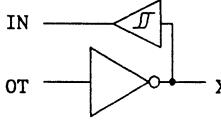
(b) Measurement of tpd at HZ and ZH.

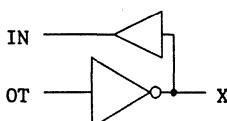
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version				
Cell Name	Function					Number of BC				
IT10	Input Buffer for Oscillator Circuit							0		
Cell Symbol		Propagation Delay Parameter								
		tup	tdn							
		t0	KCL	t0	KCL	KCL2	CDR2	Path $X \rightarrow IN$		
		0	0	0	0					
		Parameter				Symbol	Typ(ns)*			
Pin Name	Input Loading Factor (λ_u)									
Pin Name	Output Driving Factor (λ_u)									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
<p>This cell is for the oscillator circuit only. Please refer to the document Fujitsu CMOS Gate Array 'UHB' Version User's Manual for I/O Cell for Oscillator Circuit GATI0281A for the details.</p>										
UHB-IT10-E1		Sheet 1/1			Page 20-105					

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version					
Cell Name	Function					Number of BC					
HOC	Output Buffer for Oscillator with CMOS Interface Input Buffer					8					
Cell Symbol	Propagation Delay Parameter										
	tup	tdn				Path					
	t0 0.92	KCL 0.04	t0 1.33	KCL 0.04	KCL2	CDR2					
						X → IN					
Parameter	Symbol		Typ(ns)*								
Pin Name	Input Loading Factor (ℓ_u)										
Pin Name	Output Driving Factor (ℓ_u)										
IN	36										
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.											
This cell is for the oscillator circuit only. Please refer to the document "Fujitsu CMOS Gate Array 'UHB' Version User's Manual for I/O Cell for Oscillator Circuit (GATI0281A)" for the details.											

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB" Version																
Cell Name	Function					Number of BC																
HOS	Output Buffer for Oscillator with Schmitt Trigger Input Buffer																					
Cell Symbol		Propagation Delay Parameter																				
		<table border="1"> <thead> <tr> <th>tup</th> <th>tdn</th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> <th>KCL2</th> <th>CDR2</th> <th>Path</th> </tr> </thead> <tbody> <tr> <td>2.48</td> <td>0.16</td> <td>3.08</td> <td>0.10</td> <td></td> <td></td> <td>X → IN</td> </tr> </tbody> </table>					tup	tdn	t0	KCL	t0	KCL	KCL2	CDR2	Path	2.48	0.16	3.08	0.10			X → IN
tup	tdn																					
t0	KCL	t0	KCL	KCL2	CDR2	Path																
2.48	0.16	3.08	0.10			X → IN																
<table border="1"> <thead> <tr> <th>Parameter</th> <th>Symbol</th> <th>Typ(ns)*</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td></td> </tr> </tbody> </table>		Parameter	Symbol	Typ(ns)*																		
Parameter	Symbol	Typ(ns)*																				
Pin Name	Input Loading Factor (ℓ_u)																					
Pin Name	Output Driving Factor (ℓ_u)																					
IN	18																					
<small>* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.</small>																						
<small>This cell is for the oscillator circuit only. Please refer to the document "Fujitsu CMOS Gate Array 'UHB' Version User's Manual for I/O Cell for Oscillator Circuit (GATI0281Δ)" for the details.</small>																						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"UHB"	sion																					
Cell Name	Function					Nu.	z of BC																					
HOCR	Output Buffer for Oscillator w/ CMOS Interface Input Buffer w/ Feedback Resistance																											
Cell Symbol	Propagation Delay Parameter																											
	<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="4">tdn</th><th></th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th><th>KCL2</th><th>CDR2</th><th>Path</th></tr> </thead> <tbody> <tr> <td>0.92</td><td>0.04</td><td>1.33</td><td>0.04</td><td></td><td></td><td>X → IN</td></tr> </tbody> </table>						tup		tdn					t0	KCL	t0	KCL	KCL2	CDR2	Path	0.92	0.04	1.33	0.04			X → IN	
tup		tdn																										
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Pin Name	Input Loading Factor (ℓu)																											
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UHB-HOCR-E1 Sheet 1/1				Page 20-108																								

APPENDIX A: General AC Specifications

Simulation Delay Specifications
(Recommended Operating Conditions, Ta = 0 to 70°C, VDD = 5V±5%

Delay Multipliers	Min.	Max.
Pre-layout Simulation	0.35	1.65
Post-layout Simulation	0.40	1.60

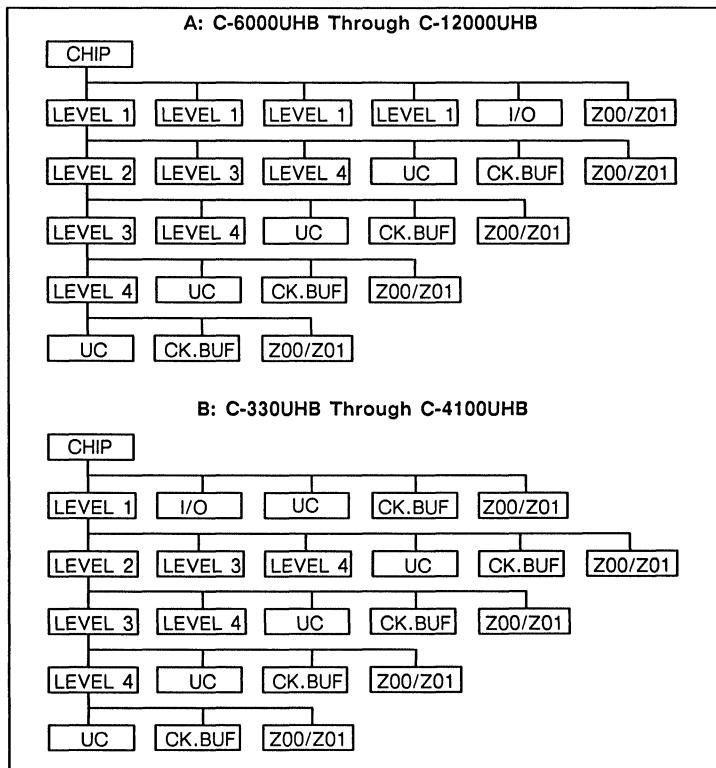
2

APPENDIX B: Hierarchical Structure

Hierarchical blocks (or Functional Logic Blocks) within other hierarchical blocks are user-defined groups of cells laid out in close proximity to each other in both X and Y dimensions of the array.

The hierarchical method of design allows circuit sections to be placed within the array at positions relative to each other. This is made possible by the designer's defining and placing functional logic blocks within the hierarchy and thus controlling path lengths.

There are five levels of hierarchy, also referred to as Functional Logic Blocks (FLBs). Certain design rules regarding what may and what must appear at certain levels are condensed in the diagram below.



Use of the hierarchical design method is mandatory for partitioned arrays and optional for non-partitioned arrays. Section A of the figure above addresses partitioned arrays C-6000UHB through C-12000UHB. Section B of the figure above addresses non-partitioned arrays C330UHB through C4100UHB. Immediately below the chip level, four Level 1 (FLB1) blocks must be defined, giving identity to each of the four partitioned quadrants of the array.

APPENDIX B: Hierarchical Structure (Continued)

All I/O buffers and their associated circuitry must be defined immediately beneath the chip level with the FLB1 blocks. Nothing but I/O buffers may be so defined. If pull-up or pull-down cells (A01s or X00s) are required for unused inputs of the I/O buffers, they must also be defined at this level. Unit cells (UC) may be defined at each level.

For optimum delay characteristics, Level 2 blocks should be defined under each of the Level 1 blocks, Level 3 Blocks under Level 2 blocks, and so on. Unit cells should be defined under Level 4.

APPENDIX C: Estimation Tables for Metal Loading

C-330UHB

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	1.0	10	5.0
2	2.2	11	5.0
3	3.0	12	5.1
4	3.5	13	5.2
5	3.9	14	5.3
6	4.2	15	5.3
7	4.6	16-30	5.7
8	4.8	31-50	6.6
9	4.9	51-75	6.7
		76-100	7.4

C-530UHB

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	1.1	10	5.6
2	2.5	11	5.6
3	3.4	12	5.7
4	3.9	13	5.8
5	4.4	14	5.9
6	4.7	15	5.9
7	5.1	16-30	6.4
8	5.4	31-50	7.4
9	5.5	51-75	7.5
		76-100	8.3

C-830UHB

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	1.3	10	6.7
2	3.0	11	6.7
3	4.0	12	6.8
4	4.7	13	6.9
5	5.2	14	7.1
6	5.6	15	7.1
7	6.1	16-30	7.7
8	6.4	31-50	8.8
9	6.6	51-75	9.0
		76-100	9.9

C-1200UHB

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	1.7	10	8.2
2	3.6	11	8.2
3	4.9	12	8.3
4	5.7	13	8.4
5	6.3	14	8.6
6	6.8	15	8.6
7	7.4	16-30	9.3
8	7.8	31-50	10.6
9	8.0	51-75	10.9
		76-100	12.0

C-1700UHB

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	1.8	10	8.8
2	3.9	11	8.8
3	5.3	12	9.0
4	6.2	13	9.1
5	6.8	14	9.3
6	7.4	15	9.3
7	8.1	16-30	10.1
8	8.4	31-50	11.5
9	8.6	51-75	11.8
		76-100	13.0

APPENDIX C: Estimation Tables for Metal Loading (Continued)

C-2200UHB

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	2.2	10	10.7
2	4.7	11	10.7
3	6.4	12	10.8
4	7.4	13	10.9
5	8.2	14	11.2
6	8.9	15	11.2
7	9.7	16-30	12.1
8	10.1	31-50	13.9
9	10.4	51-75	14.3
		76-100	15.7

C-3000UHB

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	2.6	10	12.9
2	5.7	11	12.9
3	7.7	12	13.1
4	9.0	13	13.2
5	10.0	14	13.6
6	10.8	15	13.6
7	11.8	16-30	14.7
8	12.3	31-50	16.8
9	12.6	51-75	17.3
		76-100	19.0

C-4100UHB

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	3.0	10	14.8
2	6.6	11	14.8
3	8.8	12	15.0
4	10.3	13	15.2
5	11.4	14	15.5
6	12.4	15	15.5
7	13.5	16-30	16.8
8	14.0	31-50	19.3
9	14.4	51-75	19.8
		76-100	21.8

2

C-6000UHB (Within Block)

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	1.6	10	7.9
2	3.5	11	7.9
3	4.7	12	8.0
4	5.5	13	8.2
5	6.1	14	8.4
6	6.6	15	8.4
7	7.2	16-30	9.1
8	7.5	31-50	10.4
9	7.7	51-75	10.6
		76-100	11.7

C-6000UHB (Inter-Block)

NDI	CL(ℓ_u)	NDI	CL(ℓ_u)
1	3.5	10	17.2
2	7.6	11	17.2
3	10.2	12	17.4
4	12.0	13	17.6
5	13.3	14	18.1
6	14.4	15	18.1
7	15.7	16-30	19.6
8	16.3	31-50	22.4
9	16.8	51-75	23.0
		76-100	25.3

Inter-Block tables must be applied to a net which has an inter-block connection. If a net, for example, has 3 NDI in a block and 1 NDI in a different block, NDI = 4 of the Inter-Block table must be applied.

APPENDIX C: Estimation Tables for Metal Loading (Continued)

C-8700UHB (Within Block)

NDI	CL (ft u)	NDI	CL (ft u)
1	2.2	10	10.7
2	4.7	11	10.7
3	6.4	12	10.8
4	7.4	13	10.9
5	8.2	14	11.2
6	8.9	15	11.2
7	9.7	16-30	12.1
8	10.1	31-50	13.9
9	10.4	51-75	14.3
		76-100	15.7

C-8700UHB (Inter-Block)

NDI	CL (ft u)	NDI	CL (ft u)
1	4.2	10	20.8
2	9.2	11	20.8
3	12.4	12	21.0
4	14.5	13	21.3
5	16.0	14	21.8
6	17.3	15	21.8
7	18.9	16-30	23.6
8	19.7	31-50	27.1
9	20.2	51-75	27.8
		76-100	30.5

C-12000UHB (Within Block)

NDI	CL (ft u)	NDI	CL (ft u)
1	2.6	10	12.9
2	5.7	11	12.9
3	7.7	12	13.1
4	9.0	13	13.2
5	10.0	14	13.6
6	10.8	15	13.6
7	11.8	16-30	14.7
8	12.3	31-50	16.8
9	12.6	51-75	17.3
		76-100	19.0

C-12000UHB (Inter-Block)

NDI	CL (ft u)	NDI	CL (ft u)
1	4.9	10	24.3
2	10.8	11	24.3
3	14.5	12	24.6
4	17.0	13	25.0
5	18.8	14	25.6
6	20.3	15	25.6
7	22.2	16-30	27.7
8	23.1	31-50	31.7
9	23.7	51-75	32.6
		76-100	35.8

Inter-Block tables must be applied to a net which has an inter-block connection. If a net, for example, has 3 NDI in a block and 1 NDI in a different block, NDI = 4 of the Inter-Block table must be applied.

APPENDIX C: Estimation Tables for Metal Loading for Clock Nets

C-330UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 – 2	5.1	11 – 12	12.7
3 – 4	9.5	13 – 15	13.0
5 – 6	11.9	16 – 30	13.3
7 – 8	12.2	31 – 50	15.4
9 – 10	12.4	51 – 80	18.1

C-330UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 – 2	7.0	11 – 12	17.6
3 – 4	13.4	13 – 15	17.9
5 – 6	16.7	16 – 30	18.1
7 – 8	17.0	31 – 50	20.2
9 – 10	17.3	51 – 80	23.0

C-530UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 – 2	5.1	11 – 12	14.9
3 – 4	9.6	13 – 15	15.1
5 – 6	14.1	16 – 30	15.4
7 – 8	14.4	31 – 50	17.3
9 – 10	14.6	51 – 80	19.8

C-530UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 – 2	7.3	11 – 12	21.4
3 – 4	14.0	13 – 15	21.7
5 – 6	20.7	16 – 30	21.9
7 – 8	20.9	31 – 50	23.8
9 – 10	21.2	51 – 80	26.4

C-830UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 – 2	5.6	11 – 12	18.5
3 – 4	10.5	13 – 15	18.8
5 – 6	15.4	16 – 30	19.1
7 – 8	18.0	31 – 50	21.2
9 – 10	18.2	51 – 80	24.1

C-830UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 – 2	8.1	11 – 12	27.3
3 – 4	15.5	13 – 15	27.6
5 – 6	22.9	16 – 30	27.8
7 – 8	26.7	31 – 50	30.0
9 – 10	27.0	51 – 80	32.8

C-1200UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 – 2	6.2	11 – 12	23.3
3 – 4	11.7	13 – 15	23.7
5 – 6	17.2	16 – 30	24.0
7 – 8	22.7	31 – 50	26.3
9 – 10	23.0	51 – 80	29.3

C-1200UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 – 2	9.3	11 – 12	36.0
3 – 4	18.0	13 – 15	36.3
5 – 6	26.7	16 – 30	36.6
7 – 8	35.4	31 – 50	38.9
9 – 10	35.7	51 – 80	41.9

Estimation Tables for Metal Loading for Clock Nets (Continued)

C-1700UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	6.6	11 - 12	28.0
3 - 4	12.6	13 - 15	28.3
5 - 6	18.6	16 - 30	28.6
7 - 8	24.5	31 - 50	31.0
9 - 10	27.7	51 - 80	34.2

C-1700UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	10.3	11 - 12	44.4
3 - 4	19.9	13 - 15	44.7
5 - 6	29.5	16 - 30	45.0
7 - 8	39.1	31 - 50	47.4
9 - 10	44.1	51 - 80	50.6

C-2200UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	7.1	11 - 12	33.1
3 - 4	13.5	13 - 15	33.4
5 - 6	19.9	16 - 30	33.8
7 - 8	26.3	31 - 50	36.3
9 - 10	32.8	51 - 80	39.6

C-2200UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	11.2	11 - 12	53.7
3 - 4	21.8	13 - 15	54.1
5 - 6	32.3	16 - 30	54.4
7 - 8	42.8	31 - 50	56.9
9 - 10	53.4	51 - 80	60.2

C-3000UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	7.7	11 - 12	43.0
3 - 4	14.8	13 - 15	43.3
5 - 6	21.8	16 - 30	43.7
7 - 8	28.9	31 - 50	46.3
9 - 10	35.9	51 - 80	49.8

C-3000UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	12.6	11 - 12	72.1
3 - 4	24.5	13 - 15	72.4
5 - 6	36.4	16 - 30	72.8
7 - 8	48.3	31 - 50	75.4
9 - 10	60.2	51 - 80	78.9

C-4100UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	8.4	11 - 12	47.3
3 - 4	16.2	13 - 15	51.4
5 - 6	24.0	16 - 30	51.7
7 - 8	31.7	31 - 50	54.6
9 - 10	39.5	51 - 80	58.4

C-4100UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	14.0	11 - 12	80.8
3 - 4	27.4	13 - 15	87.6
5 - 6	40.7	16 - 30	88.0
7 - 8	54.1	31 - 50	90.9
9 - 10	67.4	51 - 80	94.6

Estimation Tables for Metal Loading for Clock Nets (Continued)

C-6000UHB (for CK20, CK40)

NDI	CL(ℓu)
1	9.9
2	14.9
3	24.1
4	29.2

C-6000UHB (for CK60, CK80)

NDI	CL(ℓu)
1	13.2
2	24.8
3	37.3
4	48.9

C-8700UHB (for CK20, CK40)

NDI	CL(ℓu)
1	11.8
2	17.8
3	28.9
4	34.9

C-8700UHB (for CK60, CK80)

NDI	CL(ℓu)
1	15.7
2	29.7
3	44.8
4	58.7

C-12000UHB (for CK20, CK40)

NDI	CL(ℓu)
1	13.7
2	20.7
3	33.7
4	40.8

C-12000UHB (for CK60, CK80)

NDI	CL(ℓu)
1	18.3
2	34.7
3	52.3
4	68.7

APPENDIX D: Available Package Types

**UHB CMOS Available Package Types
Plastic**

	C-330 UHB	C-530 UHB	C-830 UHB	C-1200 UHB	C-1700 UHB	C-2200 UHB	C-3000 UHB	C-4100 UHB	C-6000 UHB	C-8700 UHB	C-12000 UHB
DIP											
Standard	(100 mil pin pitch)										
16 DIP	•	—	—	—	—	—	—	—	—	—	—
18 DIP	CH	—	—	—	—	—	—	—	—	—	—
20 DIP	•	•	—	—	—	—	—	—	—	—	—
22 DIP	•	•	•	•	•	—	—	—	—	—	—
24 DIP	•	•	•	•	•	•	•	—	—	—	—
28 DIP	•	•	•	•	•	•	•	•	•	—	—
40 DIP	•	•	•	•	•	•	•	•	•	CH	—
42 DIP	•	•	•	•	•	•	•	•	•	CH	—
48 DIP	•	•	•	•	•	•	•	•	•	CH	—
Shrink	(70 mil pin pitch)										
28 SHDIP	•	•	•	•	•	—	—	—	—	—	—
42 SHDIP	•	•	•	•	•	•	•	•	•	—	—
48 SHDIP	•	•	•	•	•	•	•	•	•	—	—
64 SHDIP	—	•	•	•	•	•	•	•	•	CH	—
Skinny	(300 mil wide body)										
22 SKDIP	•	•	—	—	—	—	—	—	—	—	—
24 SKDIP	CH	CH	—	—	—	—	—	—	—	—	—
28 SKDIP	NW	NW	—	—	—	—	—	—	—	—	—
FPT											
	(leads on two sides)										
16 FPT	•	CH	CH	CH	—	—	—	—	—	—	—
20 FPT	•	CH	CH	CH	—	—	—	—	—	—	—
24 FPT	•	•	•	•	—	—	—	—	—	—	—
28 FPT	•	•	•	•	—	—	—	—	—	—	—
	(leads on all four sides)										
44 FPT	•	•	•	•	•	—	—	—	—	—	—
48 FPT	•	•	•	•	•	•	•	—	—	—	—
48 FPT-S*	•	•	•	•	•	—	—	—	—	—	—
64 FPT	•	•	•	•	•	•	•	•	•	CH	—
80 FPT	—	•	•	•	•	•	•	•	•	—	—
100 FPT	—	—	•	•	•	•	•	•	•	—	—
120 FPT	—	—	—	•	•	•	•	•	•	•	—
160 FPT	—	—	—	—	—	—	•	•	•	•	—
*smaller than the other 48-pin FPT											
PLCC											
28 PLCC	•	•	•	•	•	•	•	—	CH	—	—
44 PLCC	•	•	•	•	•	•	•	•	CH	—	—
68 PLCC	•	•	•	•	•	•	•	•	•	CH	CH
84 PLCC	—	—	—	—	•	•	•	•	•	CH	CH
PPGA											
	100 mil pin pitch)										
64 PGA	•	•	•	•	•	•	•	•	•	•	—
88 PGA	—	•	•	•	•	•	•	•	•	•	—
135 PGA	—	—	—	—	—	—	—	•	•	•	—
NOTES:											
• : Available											
— : Not Available											
UD : Under Development											
NW : Newly Available											
CH : The availability of the package has changed, i.e., become unavailable											

APPENDIX D: Available Package Types (Continued)

UHB CMOS Available Package Types Ceramic

	C-330 UHB	C-530 UHB	C-830 UHB	C-1200 UHB	C-1700 UHB	C-2200 UHB	C-3000 UHB	C-4100 UHB	C-6000 UHB	C-8700 UHB	C-12000 UHB
DIP											
Standard	(100 mil pin pitch)										
20 DIP	•	—	—	—	—	—	—	—	—	—	—
22 DIP	•	•	•	—	—	—	—	—	—	—	—
24 DIP	•	•	•	•	—	•	—	—	—	—	—
28 DIP	•	•	•	•	•	—	—	—	—	—	—
40 DIP	•	•	•	•	•	•	—	—	—	—	—
42 DIP	—	—	—	•	•	—	•	—	—	—	—
48 DIP	—	—	•	•	•	•	—	—	—	—	—
Shrink	(70 mil pin pitch)										
28 SHDIP	•	•	•	—	—	—	—	—	—	—	—
42 SHDIP	—	—	—	•	•	•	—	—	—	—	—
FPT											
(leads on all four sides)											
48 FPT	—	—	•	•	•	•	—	—	—	—	—
80 FPT	—	—	—	—	—	—	—	—	—	UD	—
100 FPT	—	—	—	—	•	—	—	—	—	UD	—
120 FPT	—	—	—	—	—	—	—	•	•	•	UD
160 FPT	—	—	—	—	—	—	—	—	—	—	CH
LCC											
28 LCC	•	•	•	•	—	—	—	—	—	—	—
48 LCC	•	•	•	•	•	•	•	•	—	—	—
64 LCC	•	•	•	•	•	•	•	•	•	•	CH
68 LCC	—	•	•	•	•	•	•	•	•	•	CH
84 LCC	—	—	—	—	—	—	—	—	—	—	CH
PGA											
100 mil pin pitch)											
64 PGA	•	•	•	•	•	•	•	•	•	•	•
88 PGA	—	CH	•	•	•	•	•	•	•	•	UD
135 PGA	—	—	—	—	•	•	•	•	•	•	•
179 PGA	—	—	—	—	—	—	NW	NW	NW	•	•
208 PGA	—	—	—	—	—	—	•	NW	NW	NW	•
256 PGA	—	—	—	—	—	—	—	—	—	•	•
NOTES:											
•	: Available										
—	: Not Available										
UD	: Under Development										
NW	: Newly Available										
CH	: The availability of the package has been changed, i.e., become unavailable										

Appendix E: TTL 7400 Function Conversion Table

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7400	Quad 2-Input NAND	4 x N2N	4
7401	Quad 2-Input NAND, Open Collector Outputs	T24 multiplexer	6
7402	Quad 2-Input NOR	4 x R2N	4
7403	Quad 2-Input NAND, Open Collector Outputs	T24 multiplexer	6
7404	Hex Inverter	6 x VIN	6
7405	Hex Inverter, Open Collector Outputs	R6B	5
7406	Hex Inverter/Buffer, Open Collector Outputs	R6B	5
7407	Hex Buffer, Open Collector Outputs	2 x N3N into R2n	5
7408	Quad 2-Input AND	4 x N2P	8
7409	Quad 2-Input AND, Open Collector Outputs	N8P	6
7410	Triple 3-Input NAND	3 x N3N	6
7411	Triple 3-Input AND	3 x N3P	9
7412	Triple 3-NAND, Open Collector Outputs	T33	7
7413	Dual 4-Input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7414	Hex Schmitt Trigger Inverter	6 x I1R	48
7415	Triple 3-Input AND, Open Collector Outputs	N8P to N2P	8
7418	Dual 4-Input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7419	Hex Schmitt Trigger Inverter	6 x I1R	48
7420	Dual 4-Input NAND	2 x N4N	4
7421	Dual 4-Input AND	2 x N4P	6
7422	Dual 4-Input NAND, Open Collector Outputs	2 x N4N + N2P	6
7423	Expanded Dual 4-Input NOR with Strobe	R4P to D23 + R4P to R2N	9
7424	Quad Schmitt Trigger 2-Input NAND	8 x I2R + 4 x N2N	68
7425	Dual 4-Input NOR with Strobe	2 x (R4P + R2N)	8
7426	Quad 2-Input NAND, High Voltage Output	4 x N2N	4
7427	Triple 3-Input NOR	3 x R3N	6
7428	Quad 2-Input NOR Buffer	4 x R2N	4
7430	8-Input NAND	N8B	6
7432	Quad 2-Input OR	4 x R2P	8
7433	Quad 2-Input NOR Buffer, Open Collector Outputs	4 x R2N + N4P	7
7434	Hex Noninverter	6 x B1N	6
7435	Hex Noninverter with Open Collector Outputs	2 x N3N into R2N	5
7437	Quad 2-Input NAND Buffer	4 x N2B	12
7438/9	Quad 2-Input NAND Buffer, Open Collector Outputs	4 x N2N + N4P 2 x N4B (N4N if not power)	7 8(4)
7440	Dual 4-Input NAND Buffer	4 x V2B + 10 x N4N	24
7442	BCD to Decimal Decoder	4 x V2B + 10 x N4N	24
7443	EX3 to Decimal Decoder	4 x V2B + 10 x N4N	24
7444	4 to 10 Line Decoder	4 x V2B + 10 x N4N	24
7445	BCD to Decimal Decoder/driver (30V)	4 x V2B + 10 x N4N	24
7446	BCD to 7-segment Decoder/Driver (30V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7447	BCD to 7-segment Decoder/Driver (15V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7448	BCD to 7-segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7449	BCD to 7-segment, Open Collector Outputs	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7450	Dual 2-input, 2-wide AOI (One Expandable)	D36 + D24	5
7451	AOI	2 x D24 (LS51 = D24 + T32)	4(7)
7452	Expandable 4-wide AND-OR	N3N + D36 + V1N into N3N	8
7453	Expandable 4-wide AOI	D36 + D23 into N2P	7
7454	4-wide AOI	2 x N3N + 2 x N2N + N4N + V1N	9
7455	2-wide 4-Input AOI	T42	6
7460	Dual 4-Input Expander	2 x N4P	6
7461	Triple 3-Input Expander	3 x N3P	6
7462	4-wide AND-OR Expander	2 x N3N + 2 x N2N + N4N	8
7464	4-2-3-2 AOI	T54	10
7465	4-2-3-2 AOI (Open Collector)	T54	10

TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7470	AND-gated positive-edge JK FF with Preset and Clear or:	$3 \times V1N + 2 \times N3N + N2N + R2N + FJD$ $FD4 + 2 \times N2N + R2N + V1N + R2P + D24(2)$	21 17
7471	AND-gated RS M/S FF with Preset and Clear or:	$FD4 + 2 \times N3N + 2 \times D23 + 2 \times V1N$ $LT1+ 2 \times N4N + N2P$	19 10
7472	AND-gated JK M/S FF with Preset and Clear or:	$V1N + 2 \times N3N + N2N + R2N + FJD$ $FD4 + N3P + N3N + V1N + D24$	19 17
7473	Dual JK FF with Clear	$2 \times FJD$	24
7474	Dual positive-edge D-FF with Preset and Clear	$2 \times FDP$	16
7475	4-bit Bistable Latch	LTM	16
7476	Dual JK FF with Preset and Clear	$2 \times (FJD + N2N + R2N + V1N)$	30
7477	4-bit Bistable Latch	LTM	16
7478	Dual JK FF with Preset and Common Clear and Clock	$2 \times (FJD + N2N + R2N + V1N)$	30
7480	Gated Full Adder	A1N	8
7482	2-bit Binary Full Adder	A2N	16
7483	4-bit Binary Full Adder with Fast Carry	A4H	48
7484	4-bit Magnitude Comparator	MC4	42
7486	Quad 2-input XOR	$4 \times X2N$	12
7487	4-bit True/Complement Zero/One Element	$4 \times N2N + V1N + 4 \times N2N$	17
7489	64-bit (16 x 4) Memory	$2 \times DE6 + V1N + 16 \times LT4$ + $5 \times (V2B + T5A) + 10 \times V1B$	298
7490	Decade Counter (Different Implementation)	$2 \times (FDP + FDO + N2P + N2N + R2N) + V1N$ $4 \times N2P + 2 \times R2P + N2N + C41 + LT1$	39 41
7491	8-bit Shift Register	$2 \times FDS + V1N$	41
7492	Divide-by-12 Counter	$4 \times FDO + 2 \times V1N + 2 \times R2N + N2N$	33
7493	4-bit Binary Counter	C41 + N2N (for the resets)	25
7494	4-bit Shift Register, 2 asynchronous Presets	F53	34
	4-bit Shift Register, 2 asynchronous Presets, Full Implementation	$4 \times FDP + 4 \times D24 + 2 \times V1N$	42
7495	4-bit Parallel-access Shift Register	FS2 + D24 + 2 x V1N	34
7496	5-bit Shift Register	$5 \times FDP + 5 \times N2N + V1N$ (clock)	46
7497	Synch 6-bit Binary Rate Multiplier	$FDR + 2 \times FDO + 3 \times V1N + 2 \times N2N$ + $2 \times N3N + 2 \times N4N + 5 \times N6B + 3 \times N8B$ + $R2B + X2N + 5 \times X1B.$	122
7498	4-bit Data Selector/Storage Register	FDQ + T2F + 4 x V1N	33
7499	4-bit Universal Shift Register	FS2 + LTK + 2 x D24 + 4 x V1N	42
74100	8-bit Bistable Latch	$2 \times YL4 + 2 \times V1N$	30
74101	AO-gated JK Negative-Edge FF, with Preset	FD3 + V1N + 3 x D24	15
74102	AND-gated JK Negative-Edge FF with Preset and Clear	FD4 + D24 + N3P + N3N	16
74103	Dual JK FF with Clear or:	$2 \times FJD + 2 \times V1N$ (for clock) $2 \times (FD5 + D24 + V1N)$	26 22
74106	Dual JK Negative-Edge FF with Preset and Clear	$2 \times (FD4 + D24 + V1N)$	24
74107	Dual JK FF with Clear	$2 \times (FJD + 2 \times V1N)$	22
74108	Dual JK Negative-Edge FF with Preset and Common Clear and Clock	$2 \times (FD4 + D24 + V1N)$	24
74109	Dual JK Positive-Edge FF with Preset and Clear	$2 \times (FDP + V1N + D24)$	22
74110	AND-gated JK M/S FF with Data Lockout	FDP + D24 + N3P + N3N	15
74111	Dual JK M/S FF with Data Lockout	$2 \times (FDP + D24 + V1N)$	22
74112	Dual JK Negative-Edge FF with Preset and Clear	$2 \times (FD4 + D24 + V1N)$	24

TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74113	Dual JK Negative-Edge FF with Preset	$2 \times (FD3 + D24 + V1N)$	22
74114	Dual JK Negative-Edge FF with Preset and Common Clear and Clock	$2 \times (FD4 + D24 + V1N)$	24
74116	Dual 4-bit Latch with Clear	$2 \times LTM$	32
74120	Dual Pulse Synchronizer/Driver	$2 \times (N2P + LT1 + 4 \times N3N + 2 \times N2N + 2 \times V1N)$	36
74125	Quad Bus Buffer with 3-state Output	B41	9
74126	Quad Bus Buffer with 3-state Output	$B41 + 4 \times V1N$	13
74132	Quad 2-Input NAND Schmitt Trigger	$4 \times (2 \times I2R + N2N)$	68
74133	13-Input NAND	$2 \times N4N + N3N + N2N$ into R4P	10
74134	12-Input NAND with 3-state Outputs	NCB + O4R	15
74135	Quad 3-Input EXOR/EXNOR	$4 \times X4N$	20
74136	Quad 2-Input EXOR with Open-Collector Outputs	$4 \times X2N + R4N$	14
74137	3-line to 8-line Decoder with Address Latch	$3 \times LTK$ into DE6	42
74138	3-line to 8-line Decoder with Enable	DE6	30
74139	Dual 2-line to 4-line Decoder	2 \times DE4	16
74141	BCD-to-Decimal Decoder	$4 \times V2B + 10 \times N4N$	24
74145	BCD-to-decimal Decoder	$4 \times V1N + 10 \times N4N$	24
74147	10-line to 4-line BCD Priority Encoder	$3 \times N4N + 3 \times N3N + 2 \times N2N + 2 \times N2P + 3 \times R2N + R4N + 13 \times V1N$	36
74148	8-line to 3-line Octal Priority Encoder	$N9B + 2 \times N2N + R2P + R4N + 4 \times N3N + 2 \times N4N + G44 + 12 \times V1N$	40
74150	1-to-16 Multiplexer	DE3 $+ 2 \times U28 + D24 + 2 \times V1N$	41
74151	1-to-8 Multiplexer with Strobe	DE3 $+ U28 + N2N(1) + V1N$	28
74152	1-to-8 Multiplexers	DE3 $+ U28$	26
74153	Dual 4-line to 1-line Selector/Multiplexer	DE2 $+ 2 \times U24 + 2 \times R2N$)	19
74154	4-line to 16-line Decoder/Demultiplexer or:	$2 \times DE6(+ V1N$	61
74155	Dual 2-line to 4-line Decoder/Demultiplexer (Totem Pole)	$2 \times DE4 + N2P + 16 \times R2P$	50
74156	Dual 2-line to 4-line Decoder/Demultiplexer (Open Collector)	$8 \times N3N + 2 \times R2N + 5 \times V1N$	23
74157	Quad 2-line to 1-line multiplexer	$8 \times N3N + 2 \times R2N + 5 \times V1N$	23
74158	Quad 2-line to 1-line multiplexer (Inverter Data Outputs)	$T2F + 4 \times R2N + B1N$	13
74159	4-line to 16-line Demultiplexer	$4 \times D24 + V1N + 2 \times R2N$	11
74160	Synchronous 4-bit Counter (Decimal with Direct Clear)	$2 \times DE6 + V1N$ (without open collector)	50
74161	Synchronous 4-bit Counter (Binary with Direct Clear)	$4 \times C11 + K1B + 2 \times V1B + V1N + B1N + N2K + 2 \times R3N + R4N + 3 \times R2N + N2N$	62
74162	Synchronous 4-bit Counter (Decimal with Synchronous Clear)	C43	48
74163	Synchronous 4-bit Counter (Binary with Synchronous Clear)	$C45 + D36 + N3P + 2 \times R2N + B1N$	57
74164	8-bit Parallel Output Serial Shift Register, Asynchronous Clear	C45	48
74165	8-bit Shift Register	$2 \times FDR + N2P$	54
74166	8-bit Shift Register	$2 \times FDS + 8 \times D24 + 11 \times V1N + K4B + R2P$	71
74168	4-bit Up/Down Synchronous Counter (Decade)	$2 \times FDR + 8 \times D24 + 10 \times V1N + K4B$	80
74169	4-bit Up/Down Synchronous Counter (Binary)	$4 \times C11 + 4 \times T32 + 7 \times N2N + 2 \times N3N + R2N + 7 \times V1B + K1B$	85
74170	4-by-4 Register File	C47	68
74171	Quad D-FF with Clear	$4 \times (YL4 + B1N + V1N + U24) + 2 \times DE4$	104
74172	16-bit (8 \times 2) Register File	$FDR + 4 \times V1N$	30
		$3 \times DE6 + 4 \times FDS + 16 \times (N2N + G34 + V1N + 2 \times R2P + 4 \times U28) + 2 \times V1N + 2 \times R2P$	348

TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74173	4-bit D-type Register (3-state Output)	$FDR + 2 \times R2N + B41 + 6 \times V1N + K1B + 4 \times D24$	53
74174	Hex D-FF (Single Output)	$FDR + 2 \times FDO$	40
74175	Quad D-FF (with Clear)	$FDR + 4 \times V1N$	30
74176	Presettable Decade/Binary Counter	$4 \times FDP + 2 \times R2N + 5 \times N2N + 4 \times N3N + K1B$	49
74177	Presettable Binary Counter	$4 \times FDP + 5 \times N2N + 4 \times N3N + K1B$	47
74178	4-bit Universal Shift Register	$FS2$	30
74179	4-bit Universal Shift Register (Direct Clear)	$FS2 + 9 \times N2N + B1N$	40
74180	9-bit Odd/Even Parity Checker	$PO8 + 2 \times D24 + V1N$	23
74181	ALU/Function Generator	$5 \times V1N + 5 \times T32 + 4 \times D36 + 8 \times X2N + 3 \times T54 + N6B + N4B + 2 \times N2N + 2 \times N4P$	113
74182	Look-ahead Carry Generator	$R4P + 2 \times V1N + 2 \times T44 + T33 + D24$	36
74183	Dual Carry-save Full Adder	$2 \times A1N$	16
74184	BCD-to-binary Code Converter	These devices are ROM based	
74185	Binary-to-BCD Code Converter	These devices are ROM based	
74190	Synch Up/Down Counter (BCD)	$4 \times FDP + 4 \times X2N + K1B + 3 \times V1N + 3 \times N3N + 9 \times N2N + 2 \times T32 + T43$	
74191	Synch Up/Down Counter (Binary)	C47	68
74192	Up/Down Dual Clock Counter (BCD)	$4 \times C11 + 4 \times V2B + N6B + 2 \times N3N + R2N + T32 + T42 + T43$	79
74193	Up/Down Dual Clock Counter (Binary)	$4 \times C11 + 2 \times N6B + 4 \times V2B + R2N + D24 + T32 + T42$	72
74194	4-bit Bidirectional Universal Shift Register	$FDR + 6 \times V1N + R2N + 4 \times D36 + D23 + B1N$	48
74195	4-bit Parallel Access Shift Register	$FS2 + D24 + 2 \times V1N$	34
74196	Preset Decade/Binary Counter/Latch	$4 \times FDP + 2 \times R2N + 5 \times N2N + 4 \times N3N + K1B$	49
74197	Preset Binary Counter/Latch	$4 \times FDP + 5 \times N2N + 4 \times N3N + K1B$	47
74198	8-bit Bidirectional Universal Shift Register	$2 \times FDR + D24 + 10 \times V1N + R2N + 8 \times D36$	89
74199	8-bit Bidirectional Universal Shift Register (JK Serial Input) or:	$2 \times FS2 + D24 + 3 \times V1N + B1N + R2N + 8 \times N2P$ $2 \times FDR + 7 \times D24 + T33 + 11 \times V1N + R2N$	83 85
74246	BCD-to-7-Segment Decoder/Driver (30V, Active Low Open Collector)	$4 \times V1N + 11 \times N2N + 10 \times N3N + 4 \times N3P + 3 \times N2P$	53
74247	BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector)	$4 \times V1N + 11 \times N2N + 10 \times N3N + 4 \times N3P + 3 \times N2P$	53
74248	BCD-to-7-Segment Decoder/Driver (Internal Pull-up)	$4 \times V1N + 11 \times N2N + 10 \times N3N + 4 \times N3P + 3 \times N2P$	53
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74260	Dual 5-input NOR	$2 \times R6B$	10
74265	Quad Complementary Output Element	$B1N + V1N$	
74266	Quad 2-EXNOR, Open Collector	$4 \times X1N$	12
74273	Octal D-type FF with Clear	$2 \times FDR$	52
74276	Quad J-K FF	$4 \times (FDP + V1N + D24) + 2 \times B1N$	46
74347	BCD-to-7-Segment Decoder/Driver	$4 \times V1N + 11 \times N2N + 10 \times N3N + 4 \times N3P + 3 \times N2P$	53

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Section 3



AV Series CMOS Gate Array Unit Cell Library

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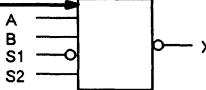
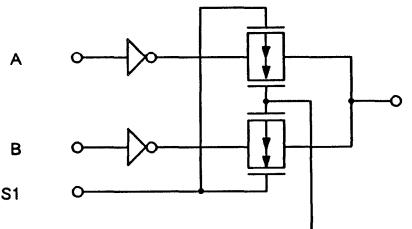
Unit Cell Specification Information

This section contains specifications for all the unit cells available for the AV Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates. A basic cell contains one pair of P-channel and one pair of N-channel transistors.

How to Read a Unit Cell Specification

The following paragraphs numbered 1–10 explain how the information given in the AV Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

1. The unit cell name appears in the upper left corner of the page.
2. The unit cell Function is given on the same line as the unit cell Name.
3. The number of basic cells (BC) or equivalent that make up the unit cell is shown in the upper right corner of the page.
4. Propagation delay parameters for the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t_0) is given in ns. KCL, the delay constant for the cell (delay time per load unit) is given in ns/pF. KCL2 and CDR2 are a delay constant and an output driving factor provided for some unit cells to calculate delay when a unit cell is loaded beyond its published output driving factor (CDR).
5. The cell (logic) symbol is shown in the top left box under the cell name box.
6. Clock parameters (in ns) for unit cells such as flip-flops and counters that make use of clock signals are given when applicable in a table directly below the propagation delay parameters.
7. Input loading factors are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
8. The output driving factor is shown directly under the input loading factor. The output driving factor is the maximum number of load units the unit cell can drive while performing at published specifications.
9. The function (truth) table, if applicable, is shown in a box at the lower left side of the page.
10. The unit cell schematic, or equivalent circuit, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.

Cell Name		Function		Number of BC																																														
1	T2D	2:1 Selector		2																																														
Cell Symbol		Propagation Delay Parameter																																																
2		tup		tdn																																														
3		t0	KCL	t0	KCL																																													
4		6.63	0.12	4.14	0.07																																													
		6.63	0.12	4.14	0.07																																													
		6.63	0.12	4.14	0.07																																													
Path		CK→Q,XQ		CL→Q,XQ																																														
5		PR→Q,XQ																																																
		Parameter																																																
6		Symbol	Min.	Typ.	Max.																																													
7	Pin Name																																																	
	A,B	1 f <u>s</u>																																																
	S1,S2	1 f <u>s</u>																																																
8	Pin Name																																																	
	X	14 f <u>s</u>																																																
Function Table			Equivalent Circuit																																															
9	<table border="1"> <thead> <tr> <th colspan="3">Inputs</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>S1</th> <th>S2</th> <th>X</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>X</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>X</td> <td>L</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>X</td> <td>H</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>H</td> <td>INHIBIT</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>H</td> <td>INHIBIT</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>H</td> <td>INHIBIT</td> </tr> </tbody> </table>			Inputs			Output	A	B	S1	S2	X	L	X	L	H	H	H	X	L	H	L	X	L	H	L	H	X	H	H	L	L	L	H	L	H	INHIBIT	H	L	L	H	INHIBIT	H	H	H	H	INHIBIT			
Inputs			Output																																															
A	B	S1	S2	X																																														
L	X	L	H	H																																														
H	X	L	H	L																																														
X	L	H	L	H																																														
X	H	H	L	L																																														
L	H	L	H	INHIBIT																																														
H	L	L	H	INHIBIT																																														
H	H	H	H	INHIBIT																																														
10	S2																																																	

3

Inverter, Clock Buffer Family

Page	Unit Cell Name	Function	Basic Cells
3-7	V1N	Inverter	1
3-8	V2B	Power Inverter	1
3-9	K1B	Clock Buffer	2
3-10	K2B	Power Clock Buffer	3
3-11	K3B	Gated Clock Buffer (AND)	3
3-12	K4B	Gated Clock Buffer (OR)	3
3-13	KCB	Gated Clock Buffer	11

3

3

3

3

3

NAND Family

Page	Unit Cell Name	Function	Basic Cells
3-17	N2N	2-input NAND	1
3-18	N3N	3-input NAND	2
3-19	N4N	4-input NAND	2
3-20	N2B	Power 2-input NAND	3
3-21	N3B	Power 3-input NAND	3
3-22	N4B	Power 4-input NAND	4
3-23	N6B	Power 6-input NAND	5
3-24	N8B	Power 8-input NAND	6
3-25	N9B	Power 9-input NAND	7
3-26	NCB	Power 12-input NAND	9
3-27	NGB	Power 16-input NAND	11

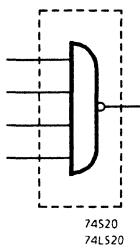
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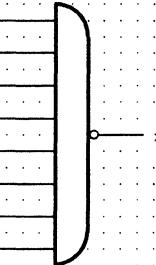
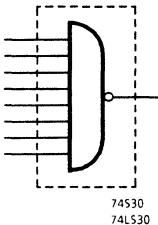
TTL Equivalent Circuit



AV-N4B-E1

N4B Sheet 1/1

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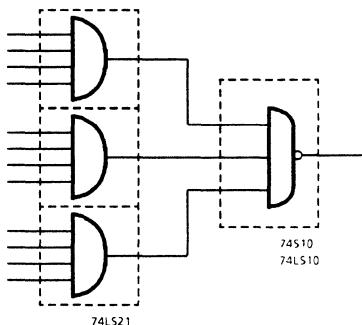
Cell Name	Function					Number of BC	
N8B	Power 8-input NAND					6	
Cell Symbol		Propagation Delay Parameters				Path	
		t_{up}		t_{dn}			
		t_o	K_{CL}	t_o	K_{CL}		
		2.29	0.12	3.09	0.07	A → X	
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX	
1 ℓu						UNIT	
Output Driving Factor		Pin Name					
36 ℓu		X					
TTL Equivalent Circuit							
							
AV-N8B-E1					N8B	Sheet 1/1	

3

Cell Name	Function	Propagation Delay Parameters				Number of BC
Cell Symbol		t_{up}		t_{dn}		Path
		t_o	K_{CL}	t_o	K_{CL}	
A1		2.26	0.12	5.38	0.07	A → X
A2						
A3						
A4						
A5						
A6						
A7						
A8						
A9						
A10						
A11						
A12						
Input Loading Factor		Pin Name				
1 ℓu		A				
Output Driving Factor		Pin Name				
36 ℓu		X				

3

TTL Equivalent Circuit



AV-NCB-E1

Sheet 1/1

3

3

AND Family

Page	Unit Cell Name	Function	Basic Cells
3-31	N2P	Power 2-input AND	2
3-32	N3P	Power 3-input AND	3
3-33	N4P	Power 4-input AND	3

3

3

3

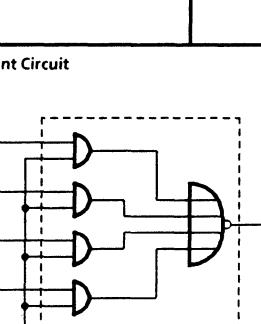
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NOR Family

Page	Unit Cell Name	Function	Basic Cells
2-37	R2N	2-input NOR	1
2-38	R3N	3-input NOR	2
2-39	R4N	4-input NOR	2
2-40	R2B	Power 2-input NOR	3
2-41	R3B	Power 3-input NOR	3
2-42	R4B	Power 4-input NOR	4
2-43	R6B	Power 6-input NOR	5
2-44	R8B	Power 8-input NOR	6
2-45	R9B	Power 9-input NOR	7
2-46	RCB	Power 12-input NOR	9
2-47	RGB	Power 16-input NOR	11

3

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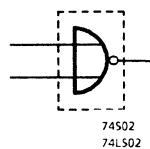
Cell Name	Function	Propagation Delay Parameters				Number of BC
R4N	4-input NOR	t_{up}	t_{dn}	t_o	K_{CL}	2
Cell Symbol		Propagation Delay Parameters				Path
		t_o	K_{CL}	t_o	K_{CL}	
A1		2.74	0.76	0.39	0.16	A → X
A2						
A3						
A4						
		Parameter	Symbol	MIN	TYP	MAX
						UNIT
Input Loading Factor						
1 ℓu	A					
Output Driving Factor						
6 ℓu	X					
TTL Equivalent Circuit						
						
"1"		7453				

3

Cell Name	Function	Propagation Delay Parameters				Number of BC
						3
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}	t_{dn}	t_o	K_{CL}	
		2.38	0.12	1.54	0.07	A → X
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX
1 ℓu						
Output Driving Factor		Pin Name				
36 ℓu		X				

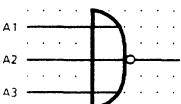
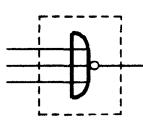
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TTL Equivalent Circuit



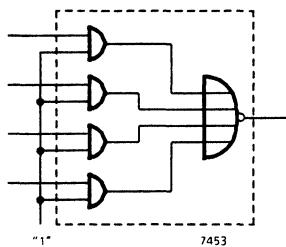
AV-R2B-E1

R2B Sheet 1/1

Cell Name	Function					Number of BC				
R3B	Power 3-input NOR					3				
Cell Symbol		Propagation Delay Parameters				Path				
		t_{up}		t_{dn}						
		t_o	KCL	t_o	KCL	A → X				
		3.65	0.12	1.61	0.07					
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX				
						UNIT				
Output Driving Factor		Pin Name								
1 ℓ u		A								
TTL Equivalent Circuit										
 74LS27										
AV-R3B-E1										
			R3B	Sheet 1/1						

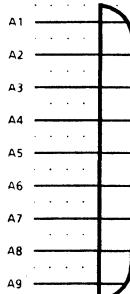
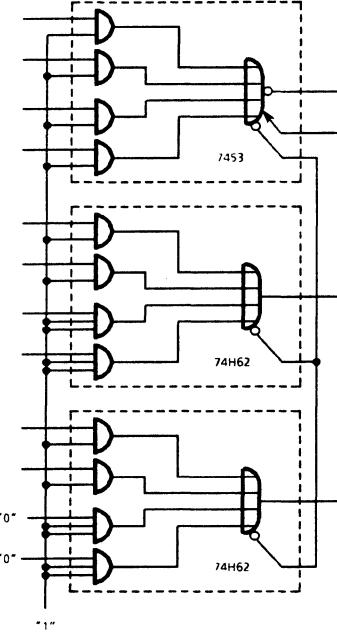
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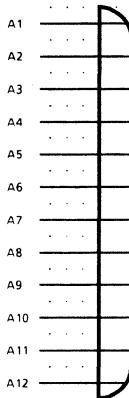
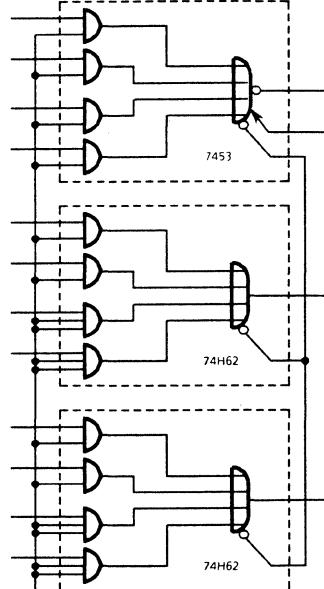
TTL Equivalent Circuit



AV-R4B-E1

R4B Sheet 1/1

Cell Name	Function	Number of BC			
R9B	Power 9-input NOR	7			
Cell Symbol	Propagation Delay Parameters			Path	
	t_{up}	t_{dn}			
	4.30	0.12	1.99	0.07	A → X
TTL Equivalent Circuit					
					
Input Loading Factor	Pin Name				
1 ℓ_u	A				
Output Driving Factor	Pin Name				
36 ℓ_u	X				
AV-R9B-E1					
R9B			Sheet 1/1		

Cell Name	Function	Propagation Delay Parameters				Number of BC
RCB	Power 12-input NOR					9
Cell Symbol		t_{up}	t_{dn}	t_o	KCL	Path
						
						A → X
TTL Equivalent Circuit						
Input Loading Factor						
1 ℓ_u	A					
Output Driving Factor						
36 ℓ_u	X					
AV-RCB-E1						
				RCB	Sheet 1/1	

Cell Name	Function	Number of BC											
RGB	Power 16-input NOR	11											
Cell Symbol	Propagation Delay Parameters			Path									
	t_{up}	t_{dn}											
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16	5.64	0.12	2.10	0.07	A → X								
TTL Equivalent Circuit													
<table border="1"> <thead> <tr> <th>Input Loading Factor</th> <th>Pin Name</th> </tr> </thead> <tbody> <tr> <td>1 ℓu</td> <td>A</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Output Driving Factor</th> <th>Pin Name</th> </tr> </thead> <tbody> <tr> <td>36 ℓu</td> <td>X</td> </tr> </tbody> </table>					Input Loading Factor	Pin Name	1 ℓu	A	Output Driving Factor	Pin Name	36 ℓu	X	
Input Loading Factor	Pin Name												
1 ℓu	A												
Output Driving Factor	Pin Name												
36 ℓu	X												

3

3

OR Family

Page	Unit Cell Name	Function	Basic Cells
3-51	R2P	Power 2-input OR	2
3-52	R3P	Power 3-input OR	3
3-53	R4P	Power 4-input OR	3

3

3

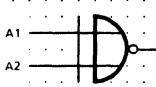
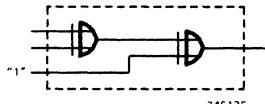
Cell Name	Function					Number of BC
R4P	Power 4-input OR					3
Cell Symbol	Propagation Delay Parameters				Path	
	t_{up}		t_{dn}			
	t_o	K _{CL}	t_o	K _{CL}	A → X	
	1.16	0.12	4.52	0.07		
	Parameter		Symbol	MIN	TYP	MAX
						UNIT
Input Loading Factor	Pin Name					
1 ℓ_u	A					
Output Driving Factor	Pin Name					
36 ℓ_u	X					
TTL Equivalent Circuit						
 7453 74S04 74LS04						
AV-R4P-E1				R4P	Sheet 1/1	

3

EXNOR/EXOR Family

Page	Unit Cell Name	Function	Basic Cells
3-57	X1B	Power EXNOR	4
3-58	X2B	Power EXOR	4

3

Cell Name	Function				Number of BC		
X1B	Power ENOR				4		
Cell Symbol		Propagation Delay Parameters				Path	
		t_{up}		t_{dn}			
		t_0	K _{CL}	t_0	K _{CL}	A → X	
		2.41	0.12	3.24	0.07		
Input Loading Factor		Parameter					
		Symbol	MIN	TYP	MAX	UNIT	
Output Driving Factor		Pin Name					
		A					
TTL Equivalent Circuit							
 74S135							
AV-X1B-E1		X1B		Sheet 1/1			

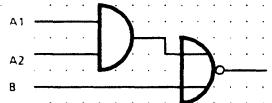
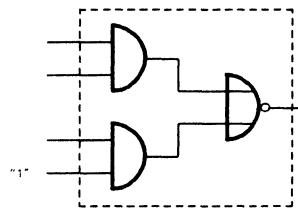
AV-X2B-E1

X2B Sheet 1/1

AND-OR-Inverter Family

Page	Unit Cell Name	Function	Basic Cells
3-61	D14	2-wide 3-AND 4-input AND-OR inverter	2
3-62	D23	2-wide 2-AND 3-input AND-OR inverter	2
3-63	D24	2-wide 2-AND 4-input AND-OR inverter	2
3-64	D34	3-wide 2-AND 4-input AND-OR inverter	2
3-65	D44	2-wide 2-OR 2-AND 4-input AND-OR inverter	2
3-66	D36	3-input AND-OR Inverter	3

3

Cell Name	Function					Number of BC					
D23	2-wide 2-AND 3-input AND-OR-Inverter					2					
Cell Symbol		Propagation Delay Parameters				Path					
		t_{up}	t_{dn}								
		t_o	K_{CL}	t_o	K_{CL}	A,B → X					
		1.41	0.54	0.48	0.24						
		Parameter	Symbol	MIN	TYP	MAX	UNIT				
Input Loading Factor		Pin Name									
1 ℓu		A,B									
Output Driving Factor		Pin Name									
10 ℓu		X									
TTL Equivalent Circuit											
 74LS51 74LS551											
AV-D23-E1		D23		Sheet 1/1							

3

3

3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AV" Version													
Cell Name	Function	Number of BC													
D36	3-input AND-OR-Inverter	3													
Cell Symbol		Propagation Delay Parameter													
		<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="2">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>2.92</td><td>0.77</td><td>0.72</td><td>0.30</td></tr> </tbody> </table>	tup		tdn		t0	KCL	t0	KCL	2.92	0.77	0.72	0.30	Path
tup		tdn													
t0	KCL	t0	KCL												
2.92	0.77	0.72	0.30												
		A,B,C → X													
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (λ_u)</th></tr> </thead> <tbody> <tr> <td>A, B, C</td><td>1</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (λ_u)	A, B, C	1										
Pin Name	Input Loading Factor (λ_u)														
A, B, C	1														
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Output Driving Factor (λ_u)</th></tr> </thead> <tbody> <tr> <td>X</td><td>8</td></tr> </tbody> </table>		Pin Name	Output Driving Factor (λ_u)	X	8										
Pin Name	Output Driving Factor (λ_u)														
X	8														
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.													

OR-AND-Inverter Family

Page	Unit Cell Name	Function	Basic Cells
3-69	G14	2-wide 3-OR 4-input OR-AND Inverter	2
3-70	G23	2-wide 2-OR 3-input OR-AND Inverter	2
3-71	G24	2-wide 2-OR 4-input OR-AND Inverter	2
3-72	G34	3-wide 2-OR 4-input OR-AND Inverter	2
3-73	G44	2-wide 2-AND 2-OR 4-input OR-AND Inverter	2

3

Cell Name	Function					Number of BC
G14	2-wide 3-OR 4-input OR-AND-Inverter					2
Cell Symbol	Propagation Delay Parameters				Path	
	t_{up}		t_{dn}			
	t_0	K_{CL}	t_0	K_{CL}	A,B → X	
	2.23	0.69	0.54	0.27		
	Parameter	Symbol	MIN	TYP	MAX	UNIT
Input Loading Factor	Pin Name					
1 ℓ_u	A,B					
Output Driving Factor	Pin Name					
10 ℓ_u	X					
TTL Equivalent Circuit						
AV-G14-E1				G14	Sheet 1/1	

3

3

Multiplexer Family

Page	Unit Cell Name	Function	Basic Cells
3-77	T24	Power 2-AND 4-wide Multiplexer	6
3-78	T26	Power 2-AND 6-wide Multiplexer	9
3-79	T28	Power 2-AND 8-wide Multiplexer	11
3-80	T32	Power 3-AND 2-wide Multiplexer	5
3-81	T33	Power 3-AND 3-wide Multiplexer	7
3-82	T34	Power 3-AND 4-wide Multiplexer	9
3-83	T42	Power 4-AND 2-wide Multiplexer	6
3-84	T43	Power 4-AND 3-wide Multiplexer	9
3-85	T44	Power 4-AND 4-wide Multiplexer	11
3-86	U24	Power 2-OR 4-wide Multiplexer	6
3-87	U26	Power 2-OR 6-wide Multiplexer	9
3-88	U28	Power 2-OR 8-wide Multiplexer	11
3-89	U32	Power 3-OR 2-wide Multiplexer	5
3-90	U33	Power 3-OR 3-wide Multiplexer	7
3-91	U34	Power 3-OR 4-wide Multiplexer	9
3-92	U42	Power 4-OR 2-wide Multiplexer	6
3-93	U43	Power 4-OR 3-wide Multiplexer	9
3-94	U44	Power 4-OR 4-wide Multiplexer	11

3

Cell Name	Function	Number of BC							
T24	Power 2-AND 4-wide Multiplexer								
Cell Symbol		Propagation Delay Parameters							
		t_{up}		t_{dn}					
		t _o	K _{CL}	t _o	K _{CL}				
		3.51	0.12	2.10	0.07				
		Any → X Input							
Input Loading Factor		Parameter							
1 ℓ u		Symbol							
Any Input		MIN							
Output Driving Factor		TYP							
36 ℓ u		MAX							
X		UNIT							
TTL Equivalent Circuit									

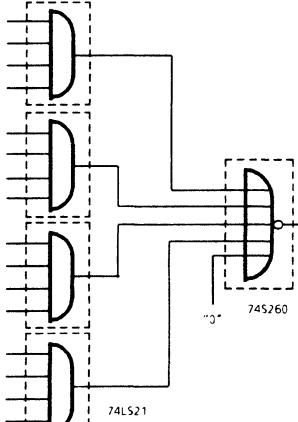
3

Cell Name	Function					Number of BC
T26	Power 2-AND 6-wide Multiplexer					9
Cell Symbol		Propagation Delay Parameters				Path
A1		t _{up}		t _{dn}		
A2		t ₀	K _{CL}	t ₀	K _{CL}	
B1		4.01	0.12	2.30	0.07	Any → X Input
B2						
C1						
C2						
D1						
D2						
E1						
E2						
F1						
F2						
Input Loading Factor		Parameter				
1 ℓu		Symbol	MIN	TYP	MAX	UNIT
Any Input						
Output Driving Factor		Pin Name				
36 ℓu		X				
TTL Equivalent Circuit						
AV-T26-E1						
					T26	Sheet 1/1

Cell Name	Function					Number of BC		
T28	Power 2-AND 8-wide Multiplexer					11		
Cell Symbol	Propagation Delay Parameters				Path			
	t_{up}	t_{dn}	t_0	K_{CL}				
A1					Any \rightarrow X Input			
A2								
B1					Any \rightarrow X Input			
B2								
C1					Any \rightarrow X Input			
C2								
D1					Any \rightarrow X Input			
D2								
E1					Any \rightarrow X Input			
E2								
F1					Any \rightarrow X Input			
F2								
G1					Any \rightarrow X Input			
G2								
H1					Any \rightarrow X Input			
H2								
Input Loading Factor	Pin Name							
1 ℓu	Any Input							
Output Driving Factor	Pin Name							
36 ℓu	X							
TTL Equivalent Circuit								
AV-T28-E1		T28		Sheet 1/1				

3

Cell Name	Function					Number of BC
T43	Power 4-AND 3-wide Multiplexer					9
Cell Symbol	Propagation Delay Parameters				Path	
	t_{up}		t_{dn}			
A1	t_o	KCL	t_o	KCL	Any \rightarrow X Input	
A2	3.03	0.12	2.73	0.07		
A3						
A4						
B1	Parameter	Symbol	MIN	TYP	MAX	UNIT
B2						
B3						
B4						
C1						
C2						
C3						
C4						
Input Loading Factor	Pin Name					
1 ℓu	Any Input					
Output Driving Factor	Pin Name					
36 ℓu	X					
TTL Equivalent Circuit						
AV-T43-E1				T43	Sheet 1/1	

Cell Name	Function	Number of BC							
T44	Power 4-AND 4-wide Multiplexer	11							
Cell Symbol		Propagation Delay Parameters							
A1		t_{up}		t_{dn}					
		t_o	K _{CL}	t_o	K _{CL}				
A2		3.36	0.12	2.84	0.07				
A3									
A4									
B1		Parameter		Symbol	MIN				
B2					TYP				
B3					MAX				
B4					UNIT				
C1									
C2									
C3									
C4									
D1									
D2									
D3									
D4									
Input Loading Factor	Pin Name								
1 ℓu	Any Input								
Output Driving Factor	Pin Name								
36 ℓu	X								
TTL Equivalent Circuit									
									
AV-T44-E1									
T44		Sheet 1/1							

3

Cell Name	Function	Number of BC					
U26	Power 2-OR 6-wide Multiplexer	9					
Cell Symbol		Propagation Delay Parameters				Path	
		t _{up}		t _{dn}			
A1		t ₀	K _{CL}	t ₀	K _{CL}		
A2		3.21	0.12	4.14	0.07	Any → X Input	
		Parameter	Symbol	MIN	TYP	MAX	UNIT
B1							
B2							
C1							
C2							
D1							
D2							
E1							
E2							
F1							
F2							
Input Loading Factor		Pin Name					
1 ℓ u	Any Input						
Output Driving Factor		Pin Name					
36 ℓ u	X						
TTL Equivalent Circuit							
		<p>The TTL equivalent circuit diagram illustrates the internal logic of the U26 cell. It shows a 6-wide multiplexer structure built from smaller logic components. The inputs A1-A2, B1-B2, C1-C2, D1-D2, E1-E2, and F1-F2 are processed by six 2-to-1 multiplexers (74LS32). The outputs of these multiplexers are then fed into three OR gates (74LS10) to produce the final output X.</p>					
		<p>This detailed TTL equivalent circuit diagram provides a clearer view of the internal logic. It shows the 6-wide multiplexer implemented using 74LS32 and 74LS10 logic gates. The inputs A1-A2, B1-B2, C1-C2, D1-D2, E1-E2, and F1-F2 are processed by six 2-to-1 multiplexers (74LS32). The outputs of these multiplexers are then fed into three OR gates (74LS10) to produce the final output X.</p>					
AV-U26-E1		74LS32	74LS10				
U26		Sheet 1/1					

3

Cell Name	Function					Number of BC	
						11	
Cell Symbol		Propagation Delay Parameters				Path	
		t _{up}		t _{dn}			
		t ₀	K _{CL}	t ₀	K _{CL}		
		3.19	0.12	5.28	0.07	Any → X Input	
TTL Equivalent Circuit							
Input Loading Factor		Pin Name					
1 ℓ u		Any Input					
Output Driving Factor		Pin Name					
36 ℓ u		X					
AV-U28-E1							
U28				Sheet 1/1			

Cell Name	Function					Number of BC
U32	Power 3-OR 2-wide Multiplexer					5
Cell Symbol	Propagation Delay Parameters				Path	
	t_{up}		t_{dn}			
	t_0	KCL	t_0	KCL	Any \rightarrow X Input	
	3.56	0.12	2.35	0.07		
	Parameter	Symbol	MIN	TYP	MAX	UNIT
A1						
A2						
A3						
B1						
B2						
B3						
Input Loading Factor	Pin Name					
1 ℓ u	Any Input					
Output Driving Factor	Pin Name					
36 ℓ u	X					
TTL Equivalent Circuit						
7427 74LS27	74S04 74LS04	74500 74LS00				
AV-U32-E1				U32	Sheet 1/1	

Cell Name	Function	Propagation Delay Parameters				Number of BC
U33	Power 3-OR 3-wide Multiplexer					7
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}	t_{dn}		Any → X Input	
A1		t_o	K _{CL}	t_o	K _{CL}	
A2		3.66	0.12	3.76	0.07	
A3						
Input Loading Factor		Parameter				
1 ℓu		Symbol	MIN	TYP	MAX	UNIT
Any Input						
Output Driving Factor		Parameter				
36 ℓu		Symbol	MIN	TYP	MAX	UNIT
X						
TTL Equivalent Circuit						
7427		74S04	74LS10			
74LS27		74S04	74LS10			

3

Cell Name	Function	Propagation Delay Parameters				Number of BC
U44	Power 4-OR 4-wide Multiplexer					11
Cell Symbol		t_{up}	t_{dn}	t_o	K_{CL}	Path
TTL Equivalent Circuit						
A1		4.65	0.12	4.90	0.07	Any → X Input
A2						
A3						
A4						
B1						
B2						
B3						
B4						
C1						
C2						
C3						
C4						
D1						
D2						
D3						
D4						
Input Loading Factor	Pin Name					
1 ℓu	Any Input					
Output Driving Factor	Pin Name					
36 ℓu	X					
AV-U44-E1						
U44						
Sheet 1/1						

Selector Family

Page	Unit Cell Name	Function	Basic Cells
3-97	T2B	2:1 Selector	2
3-98	T2C	Dual 2:1 Selector	4
3-99	T2D	2:1 Selector	2
3-100	V3A	1:2 Selector	2
3-101	V3B	Dual 1:2 Selector	3
3-102	T5A	4:1 Selector	5

3

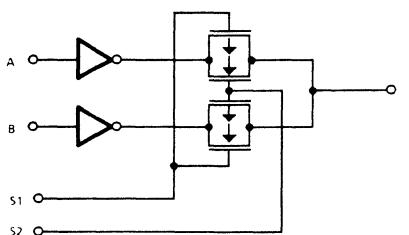
3

3

Function Table



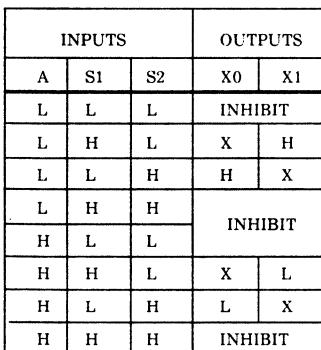
INPUTS			OUTPUT	
A	B	S1	S2	X
L	X	L	H	H
H	X	L	H	L
X	L	H	L	H
X	H	H	L	L
L	H	L	L	IN-HIBIT
L	H	H	H	
H	L	L	L	
H	L	H	H	



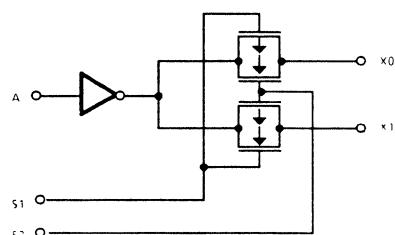
Cell Name	Function	Propagation Delay Parameters				Number of BC
V3A	1 : 2 Selector					2
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}	t_{dn}	t_o	K_{CL}	
A		0.77 2.34	0.19 0.19	1.18 0.42	0.20 0.20	$A \rightarrow X$ $S1, S2 \rightarrow X$
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX
1 ℓ_u						
1 ℓ_u						
Output Driving Factor		Pin Name				
14 ℓ_u		A S1, S2	X			
Output Loading Factor		Pin Name				
1 ℓ_u		X				

3

Function Table



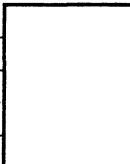
Equivalent Circuit

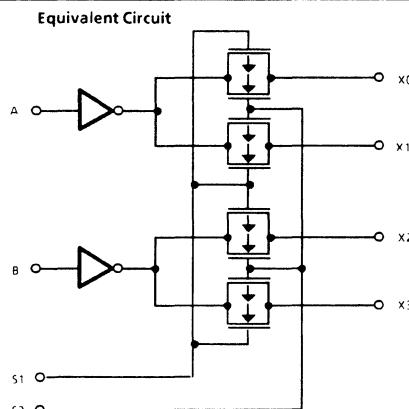


AV-V3A-E1

VRA

Sheet 1/1

Cell Name	Function					Number of BC
V3B	Dual 1 : 2 Selector					3
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}		t_{dn}		
		t_0	K_{CL}	t_0	K_{CL}	
		0.77 2.34	0.19 0.19	1.18 0.42	0.20 0.20	A,B → X S1,S2 → X
		Parameter	Symbol	MIN	TYP	MAX
						UNIT
Input Loading Factor		Pin Name				
1 ℓ_u 2 ℓ_u		A,B S1,S2				
Output Driving Factor		Pin Name				
14 ℓ_u		X				
Output Loading Factor		Pin Name				
1 ℓ_u		X				
Function Table						
INPUTS		OUTPUTS				
A,B	S1	S2	X0,X2	X1,X3		
L	L	L	INHIBIT			
L	H	L	X	H		
L	L	H	H	X		
L	H	H	INHIBIT			
H	L	L				
H	H	L	X	L		
H	L	H	L	X		
H	H	H	INHIBIT			
AV-V3B-E1						
				V3B	Sheet 1/1	



Cell Name	Function	Propagation Delay Parameters				Number of BC
T5A	4:1 Selector					5
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}		t_{dn}		
		t_o	K_{CL}	t_o	K_{CL}	
S1	S2	1.48	0.19	1.13	0.20	A,B → X
		3.22	0.19	1.25	0.20	S1 ~ S4 → X
		2.63	0.19	0.70	0.20	S5 ~ S6 → X
Parameter		Symbol	MIN	TYP	MAX	UNIT
A1						
A2						
B1						
B2						
S5	S6					
Input Loading Factor		Pin Name				
1 ℓ_u	1 ℓ_u	A,B S1 ~ S6				
Output Driving Factor		Pin Name				
9 ℓ_u	X					

Function Table

INPUTS										OUTPUT
A1	A2	B1	B2	S1	S2	S0	S1	S5	S6	X
L	H	L	H	L	H			L	H	H
				L	H			L	H	L
H	L	H	L	H	L			L	H	H
				H	L			L	H	L
L	H	L	H			L	H	H	L	H
						L	H	H	L	L
H	L	H	L			H	L	H	L	H
						H	L	H	L	L

$A_1 \neq A_2 \rightarrow S_1 = S_2$ or $S_5 = S_6$ Inhibit

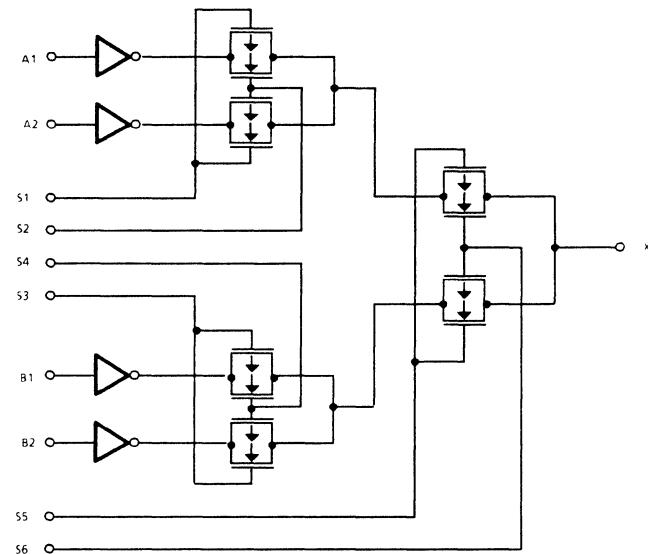
$B_1 \neq B_2 \rightarrow S_3 = S_4$ or $S_5 = S_6$ Inhibit

A1, A2 ≠ B1, B2 or S5 = S6 Inhibit

A.V.T5A.E1

T5A

Sheet 1/2

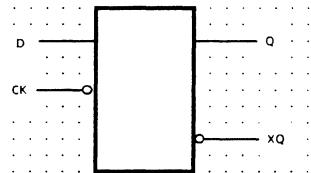
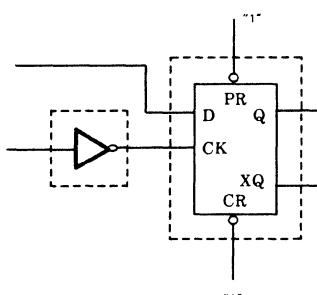
Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Equivalent Circuit	
	
AV-T5A-E1	T5A Sheet 2/2

3

Flip-Flop Family

Page	Unit Cell Name	Function	Basic Cells
3-107	FD2	Power D FF	8
3-109	FD3	Power D FF with Preset	9
3-111	FD4	Power D FF with Clear and Preset	10
3-113	FD5	Power D FF with Clear	9
3-115	FD6	D FF	7
3-117	FD7	D FF with Clear	8
3-119	FD8	D FF and Latch	9
3-121	FDD	Positive Edge Clocked Power D FF with Clear and Preset	11
3-123	FDE	Positive Edge Clocked Power D FF with Clear	10
3-125	FDG	Positive Edge Clocked D FF with Clear	9
3-127	FDM	D FF	6
3-129	FDN	D FF with Set	7
3-131	FDO	D FF with Reset	7
3-133	FDP	D FF with Set and Reset	8
3-135	FDQ	4-bit D FF	21
3-137	FDR	4-bit D FF with Clear	26
3-139	FDS	4-bit D FF	20
3-141	FJ4	Power J-K FF with Clear	11
3-143	FJ5	Power J-K FF with Clear and Preset	12
3-145	FJD	Positive Edge Clocked Power J-K FF with Clear	12

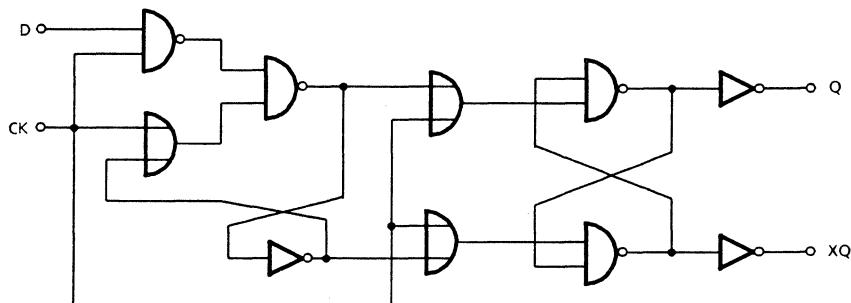
3

Cell Name	Function					Number of BC
FD2	Power DFF					8
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}		t_{dn}		
		t_o	K _{CL}	t_o	K _{CL}	
		4.83	0.12	3.24	0.07	CK → Q, XQ
Parameter	Symbol	MIN	TYP	MAX	UNIT	
Clock Pulse Width	t_{CW}		4		ns	
Data Set Up Time	t_{SD}		4		ns	
Data Hold Time	t_{HD}		1		ns	
Clock Pause Time	t_{CWL}		3		ns	
Input Loading Factor						
1 ℓ_u 4 ℓ_u						
		D CK				
Output Loading Factor						
36 ℓ_u		Q,XQ				
TTL Equivalent Circuit						
						
74S04 74LS04						
74S74 74LS74A						
Function Table						
		Inputs		Outputs		
		CK	D	Q	XQ	
		↓	H L	H L	L H	
AV-FD2-E1		FD2		Sheet 1/2		

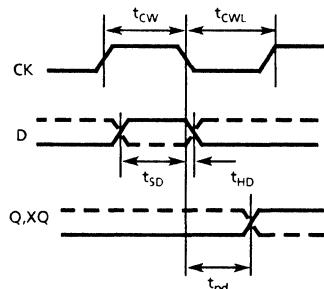
Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

Equivalent Circuit

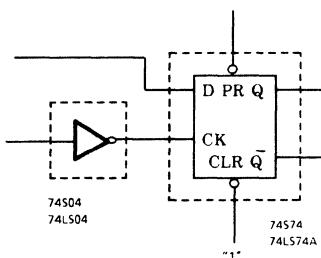


Definition of Parameters



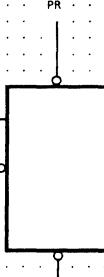
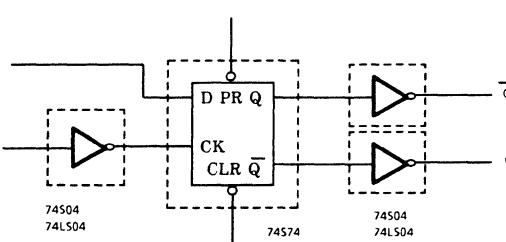
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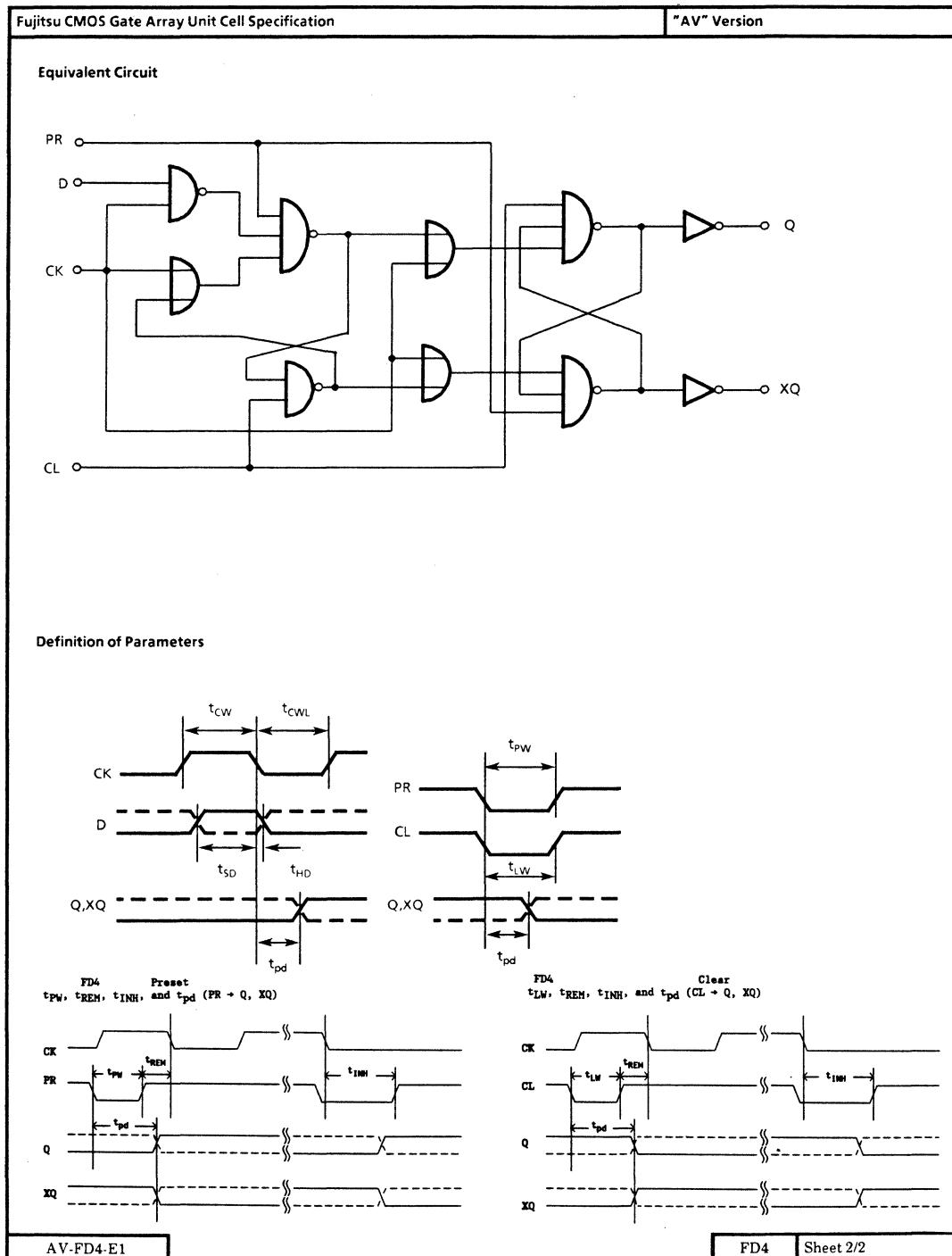
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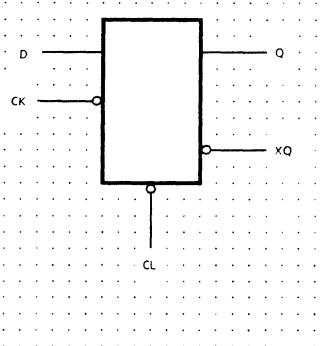
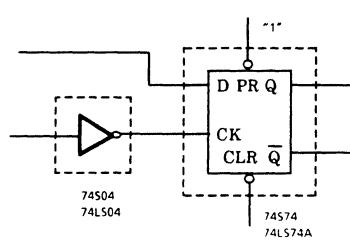


Inputs			Outputs	
PR	CK	D	Q	XQ
L	X	X	H	L
H		H	H	L
H	↓	L	L	H

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Equivalent Circuit	
Definition of Parameters	
FD3 Preset t_{PW} , t_{REM} , t_{INH} , and t_{pd} ($PR + Q, XQ$)	
AV-FD3-E1	FD3 Sheet 2/2

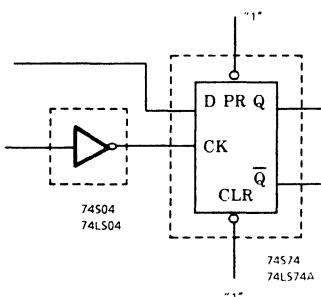
Cell Name	Function					Number of BC
FD4	Power DFF with CLEAR and PRESET					10
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}		t_{dn}		
		t_o	K_{CL}	t_o	K_{CL}	
		5.63 5.63 5.63	0.12 0.12 0.12	3.54 3.54 3.54	0.07 0.07 0.07	$CK \rightarrow Q, XQ$ $CL \rightarrow Q, XQ$ $PR \rightarrow Q, XQ$
		Parameter				
		Symbol	MIN	TYP	MAX	UNIT
Clock Pulse Width		t_{CW}		4		ns
Preset Pulse Width		t_{PW}		5		ns
Clear Pulse Width		t_{LW}		5		ns
Data Set Up Time		t_{SD}		4		ns
Data Hold Time		t_{HD}		1		ns
Clock Pause Time		t_{CWL}		4		ns
Input Loading Factor		Pin Name				
16u 48u 26u 26u		D CK CL PR				
Output Driving Factor		Pin Name				
368u		Q,XQ				
TTL Equivalent Circuit						
						
Function Table						
		Inputs		Outputs		
		PR	CL	CK	D	Q XQ
		L	H	X	X	H L
		H	L	X	X	L H
		H	H	↓	H	H L
		H	H	↓	L	L H
AV-FD4-E1		FD4				Sheet 1/2



Cell Name	Function					Number of BC																						
FD5	Power DFF with CLEAR					9																						
Cell Symbol		Propagation Delay Parameters				Path																						
		t_{up}	t_{dn}																									
		t_o	K_{CL}	t_o	K_{CL}	$CK \rightarrow Q, XQ$ $CL \rightarrow Q, XQ$																						
		5.33 5.13	0.12 0.12	3.54 3.54	0.07 0.07																							
Parameter	Symbol	MIN	TYP	MAX	UNIT																							
Clock Pulse Width	t_{CW}		4		ns																							
Clear Pulse Width	t_{LW}		5		ns																							
Data Set Up Time	t_{SD}		4		ns																							
Data Hold Time	t_{HD}		1		ns																							
Clock Pause Time	t_{CWL}		4		ns																							
Input Loading Factor																												
1 ℓ_u 4 ℓ_u 2 ℓ_u		D	CK	CL																								
Output Driving Factor																												
36 ℓ_u		Q, XQ																										
TTL Equivalent Circuit			Function Table																									
			<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> <tr> <th>CL</th><th>CK</th><th>D</th><th>Q</th><th>XQ</th></tr> </thead> <tbody> <tr> <td>L</td><td>X</td><td>X</td><td>L</td><td>H</td></tr> <tr> <td>H</td><td></td><td></td><td>H</td><td>L</td></tr> <tr> <td>H</td><td>↓</td><td>L</td><td>L</td><td>H</td></tr> </tbody> </table>				Input	Output	CL	CK	D	Q	XQ	L	X	X	L	H	H			H	L	H	↓	L	L	H
Input	Output																											
CL	CK	D	Q	XQ																								
L	X	X	L	H																								
H			H	L																								
H	↓	L	L	H																								
AV-FD5-E1		FD5 Sheet 1/2																										

Cell Name	Function	Number of BC										
FD6	DFF	7										
Cell Symbol		Propagation Delay Parameters				Path						
		t_{up}		t_{dn}								
		t_o	K _{CL}	t_o	K _{CL}							
		3.94	0.25	2.69	0.14	CK → Q, XQ						
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX						
1 ℓu 4 ℓu		Clock Pulse Width	t_{CW}		4	ns						
		Data Set Up Time	t_{SD}		4	ns						
		Data Hold Time	t_{HD}		1	ns						
		Clock Pause Time	t_{CWL}		3	ns						
Output Driving Factor		Pin Name										
18 ℓu		D CK										
Output Driving Factor		Pin Name										
18 ℓu		Q,XQ										
TTL Equivalent Circuit				Function Table								
				<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> </thead> <tbody> <tr> <td>CK D ↓ H</td><td>Q XQ H L</td></tr> <tr> <td>↓ L</td><td>L H</td></tr> </tbody> </table>			Input	Output	CK D ↓ H	Q XQ H L	↓ L	L H
Input	Output											
CK D ↓ H	Q XQ H L											
↓ L	L H											

3



Function Table

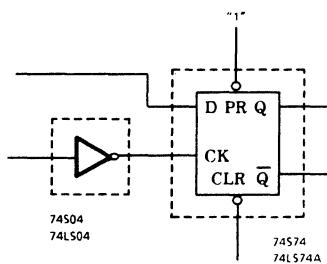
Input		Output
CK	D	Q XQ
↓	H	H L
↓	L	L H

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Equivalent Circuit	
Definition of Parameters	
AV-FD6-E1	FD6 Sheet 2/2

Cell Name	Function	Propagation Delay Parameters				Number of BC
Cell Symbol		t_{up}		t_{dn}		Path
		t_o	K_{CL}	t_o	K_{CL}	
		4.34 4.34	0.25 0.25	2.89 2.89	0.14 0.14	$CK \rightarrow Q, XQ$ $CL \rightarrow Q, XQ$
Parameter	Symbol	MIN	TYP	MAX	UNIT	
Clock Pulse Width	t_{CW}		4			ns
Clear Pulse Width	t_{LW}		4			ns
Data Set Up Time	t_{SD}		4			ns
Data Hold Time	t_{HD}		1			ns
Clock Pause Time	t_{CWL}		4			ns
Input Loading Factor	Pin Name					
1 ℓu 4 ℓu 2 ℓu	D CK CL					
Output Driving Factor	Pin Name					
18 ℓu	Q, XQ					

3

TTL Equivalent Circuit



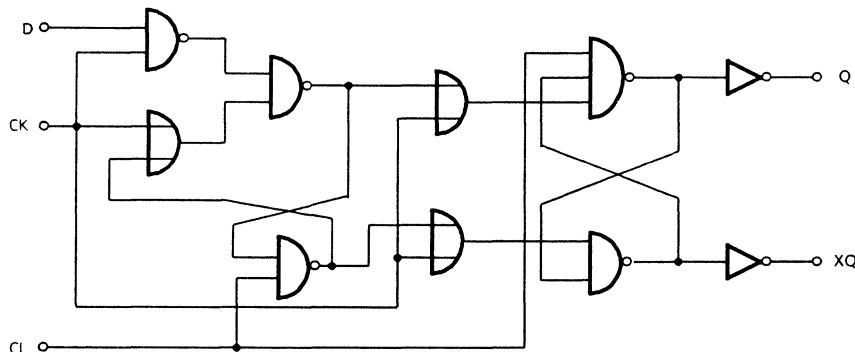
Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

Function Table

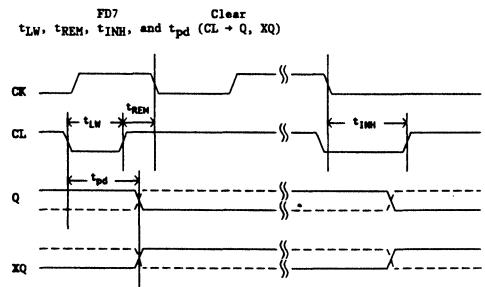
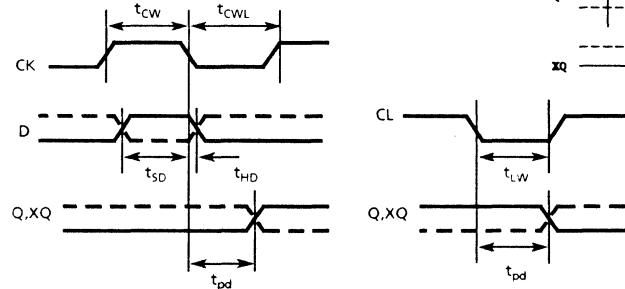
Input	Output			
CL	CK	D	Q	XQ
L	X	X	L	H
H	↓	H	H	L
H	↓	L	L	H

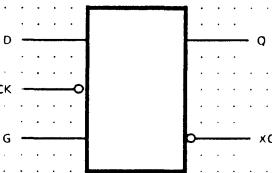
Equivalent Circuit



3

Definition of Parameters



Cell Name	Function					Number of BC	
FD8	DFF & Latch					9	
Cell Symbol		Propagation Delay Parameters				Path	
		t_{up}	t_{dn}				
		t_0	K _{CL}	t_0	K _{CL}		
		3.94 10.14 10.14	0.25 0.25 0.25	2.69 8.89 8.89	0.14 0.14 0.14	CK → Q, XQ D → Q, XQ G → Q, XQ	
		Parameter	Symbol	MIN	TYP	MAX	UNIT
		DFF Operation					
		Clock Pulse Width	t_{CW}	7			ns
		Data Set Up Time	t_{SD}	7			ns
		Data Hold Time	t_{HD}	1			ns
		Clock Pause Time	t_{CWL}	4			ns
		Latch Operation					
		G Pulse Width	t_{GW}	7			ns
		Data Set Up Time	t_{SDG}	7			ns
		Data Hold Time	t_{HDG}	1			ns
Input Loading Factor							
4 ℓu 2 ℓu		CK D,G					
Output Driving Factor		Pin Name					
18 ℓu		Q,XQ					

Fujitsu CMOS Gate Array Unit Cell Specification

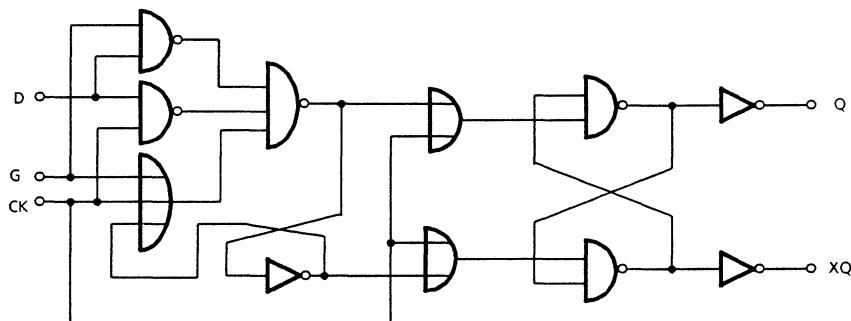
"AV" Version

Function Table

Inputs			Outputs	
G	CK	D	Q	XQ
L	↓	L	L	H
L	↓	H	H	L
H	L	L	L	H
H	L	H	H	L
L	L	X	Q ₀	XQ ₀
H	H	X	Q ₀	XQ ₀

←Inhibited

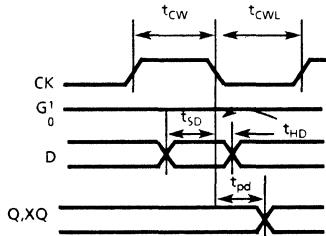
Equivalent Circuit



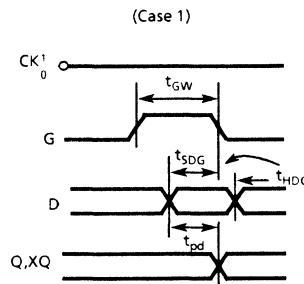
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Definition of Parameters

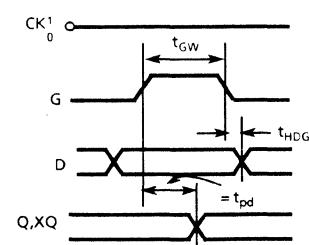
(1) DFF Operation



(2) Latch Operation



(Case 2)

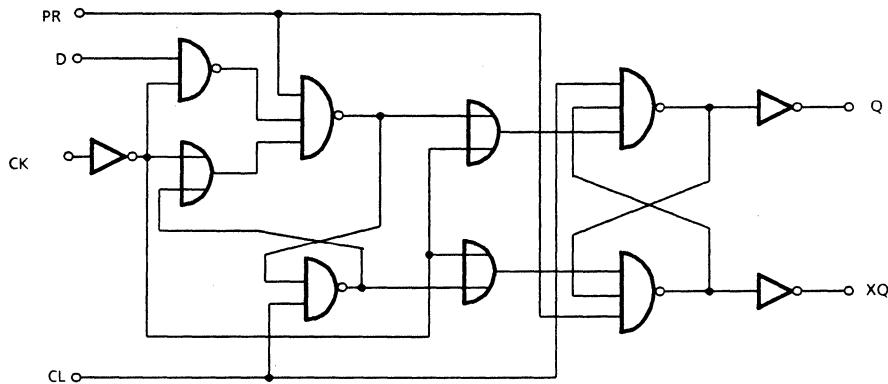


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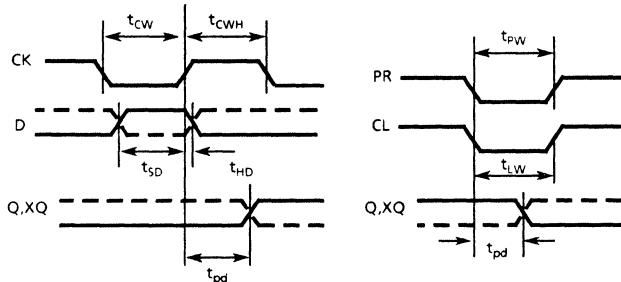
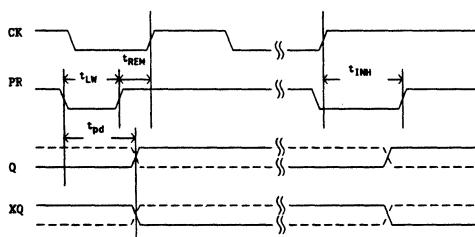
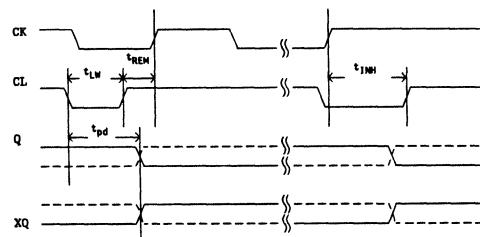
Fujitsu CMOS Gate Array Unit Cell Specification

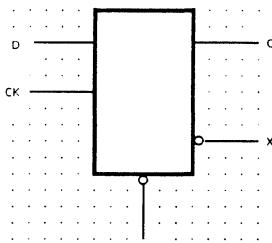
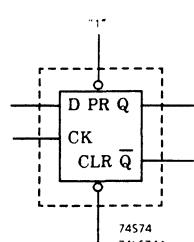
"AV" Version

Equivalent Circuit

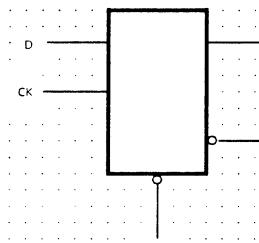
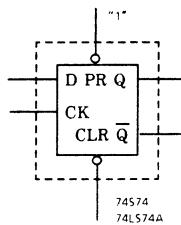


Definition of Parameters

FDD Preset
 t_{PW} , t_{REM} , t_{INH} , and t_{pd} ($PR \rightarrow Q, XQ$)FDD Clear
 t_{LW} , t_{REM} , t_{INH} , and t_{pd} ($CL \rightarrow Q, XQ$)

Cell Name	Function					Number of BC
FDE	Positive Edge Clocked Power DFF with CLEAR					10
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}	t_{dn}			
		t_o	K_{CL}	t_o	K_{CL}	
		6.23 5.13	0.12 0.12	4.44 3.54	0.07 0.07	CK → Q, XQ CL → Q, XQ
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX
1 ℓu 1 ℓu 2 ℓu		Clock Pulse Width	t_{CW}		6	
		Clear Pulse Width	t_{LW}		5	
		Data Set Up Time	t_{SD}		4	
		Data Hold Time	t_{HD}		1	
		Clock Pause Time	t_{CWH}		4	
Output Driving Factor		Pin Name				
36 ℓu		Q,XQ	D CK CL			
TTL Equivalent Circuit						
						
Function Table						
			Inputs	Outputs		
CL	CK	D		Q	XQ	
L	X	X		L	H	
H	↑	H		H	L	
H	↑	L		L	H	

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Equivalent Circuit	
Definition of Parameters	
<p style="text-align: center;">FDE Clear t_{LW}, t_{REM}, t_{INH}, and t_{pd} ($CL + Q$, XQ)</p>	
AV-FDE-E1	FDE Sheet 2/2

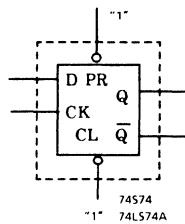
Cell Name	Function					Number of BC					
FDG	Positive Edge Clocked DFF with CLEAR					9					
Cell Symbol		Propagation Delay Parameters				Path					
		t_{up}		t_{dn}							
		t_o	KCL	t_o	KCL						
		5.24 4.14	0.25 0.25	3.79 2.89	0.14 0.14	CK \rightarrow Q, XQ CL \rightarrow Q, XQ					
		Parameter	Symbol	MIN	TYP	MAX					
		Clock Pulse Width	t_{CW}		6	ns					
		Clear Pulse Width	t_{LW}		4	ns					
		Data Set Up Time	t_{SD}		4	ns					
		Data Hold Time	t_{HD}		1	ns					
		Clock Pause Time	t_{CWH}		4	ns					
Input Loading Factor		Pin Name									
1 ℓu 1 ℓu 2 ℓu		D CK CL									
Output Driving Factor		Pin Name									
18 ℓu		Q, XQ									
TTL Equivalent Circuit											
											
AV-FDG-E1		FDG		Sheet 1/2							

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version																									
Function Table																										
<table border="1"> <thead> <tr> <th colspan="3">Inputs</th> <th colspan="2">Outputs</th> </tr> <tr> <th>CL</th> <th>CK</th> <th>D</th> <th>Q</th> <th>XQ</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>X</td> <td>X</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>↑</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>↑</td> <td>L</td> <td>L</td> <td>H</td> </tr> </tbody> </table>		Inputs			Outputs		CL	CK	D	Q	XQ	L	X	X	L	H	H	↑	H	H	L	H	↑	L	L	H
Inputs			Outputs																							
CL	CK	D	Q	XQ																						
L	X	X	L	H																						
H	↑	H	H	L																						
H	↑	L	L	H																						
Equivalent Circuit																										
<p style="text-align: right;">Clear t_{LW}, t_{REM}, t_{INH}, and t_{pd} ($CL + Q, XQ$)</p>																										
Definition of Parameters																										
AV-FDG-E1	FDG Sheet 2/2																									

Cell Name	Function	Number of BC									
FDM	DFF	6									
Cell Symbol		Propagation Delay Parameters				Path					
		t_{up}		t_{dn}							
		t_o	K _{CL}	t_o	K _{CL}						
		3.46 5.96	0.25 0.25	5.16 4.22	0.14 0.14	CK \rightarrow Q CK \rightarrow XQ					
Input Loading Factor		Parameter									
2 ℓ_u 1 ℓ_u		t_{CW}									
D CK		6									
Output Driving Factor		ns									
18 ℓ_u		2									
Pin Name		Data Set Up Time									
Q,XQ		t_{SD}									
Pin Name		Data Hold Time									
Q,XQ		t_{HD}									
Pin Name		Clock Pause Time									
Q,XQ		t_{CWH}									
TTL Equivalent Circuit											
Function Table											
Inputs		Outputs									
D CK		Q XQ									
H L		H L H									

3

Function Table

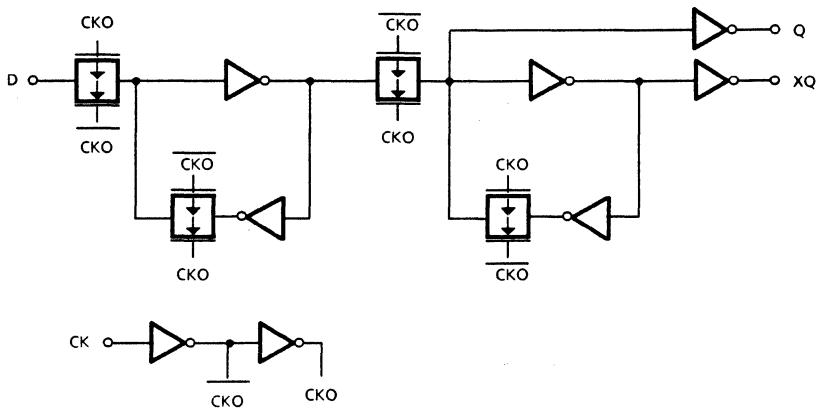


Inputs	Outputs		
D	CK	Q	XQ
H L	↑ ↑	H L	L H

Fujitsu CMOS Gate Array Unit Cell Specification

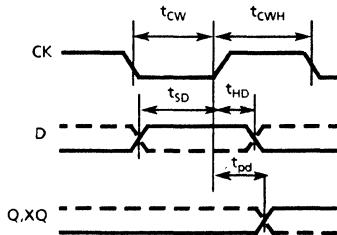
"AV" Version

Equivalent Circuit



Definition of Parameters

3

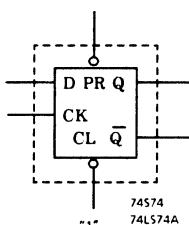


Cell Name	Function	Propagation Delay Parameters				Number of BC
Cell Symbol		t_{up}		t_{dn}		Path
		t_o	K _{CL}	t_o	K _{CL}	
		3.46 6.10 2.82	0.25 0.25 0.25	5.16 4.42 1.40	0.14 0.14 0.14	CK → Q CK → XQ S → Q, XQ
Parameter	Symbol	MIN	TYP	MAX	UNIT	
Clock Pulse Width	t_{CW}		6			ns
Data Set Up Time	t_{SD}		2			ns
Data Hold Time	t_{HD}		2			ns
Set Pulse Width	t_{SW}		3			ns
Clock Pause Time	t_{CWH}		6			ns
Set Release Time	t_{REM}		1			ns
Set Hold Time	t_{INH}		4			ns
Input Loading Factor	Pin Name					
2 ℓ_u 1 ℓ_u	D, S CK					
Output Driving Factor	Pin Name					
18 ℓ_u	Q, XQ					

3

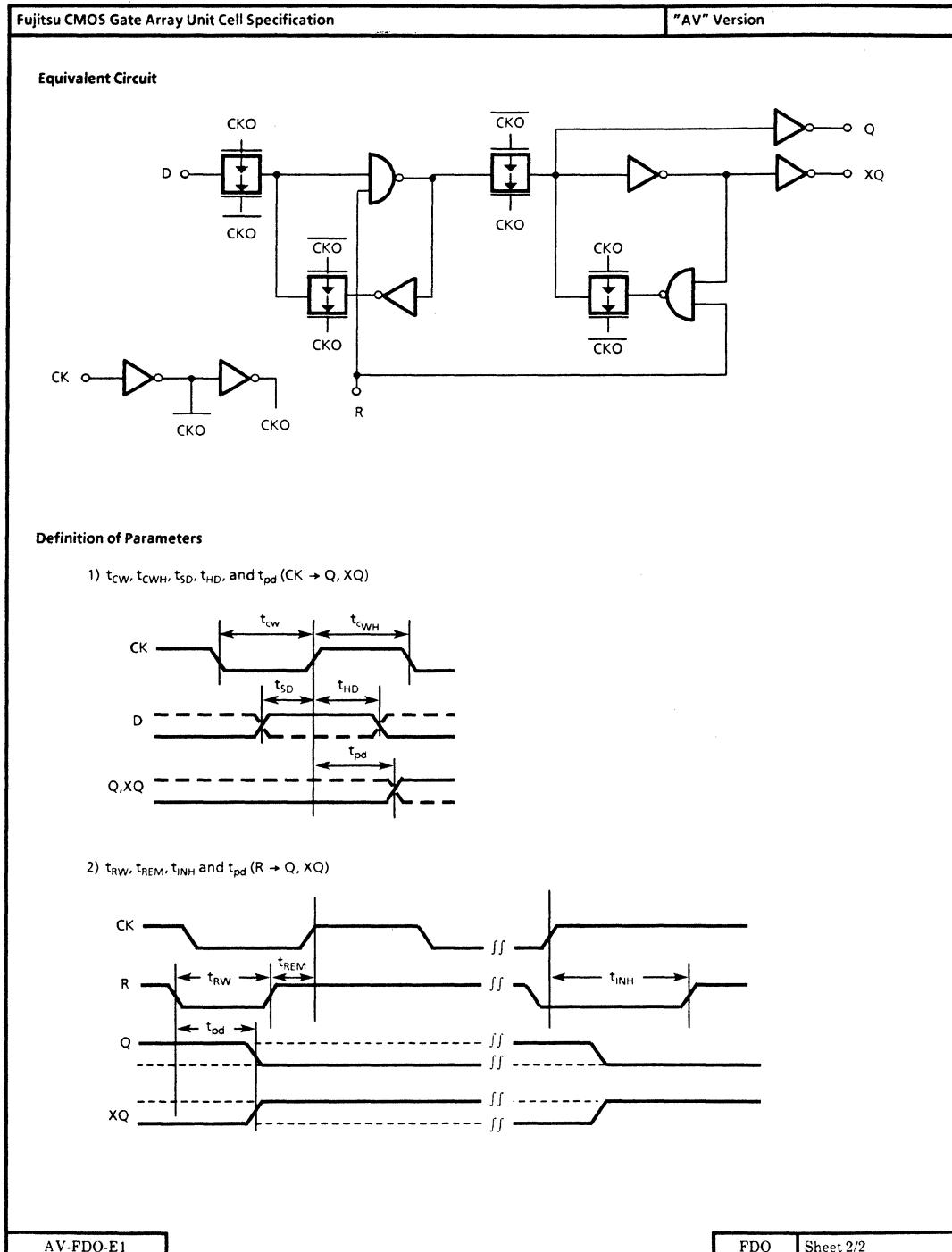
TTL Equivalent Circuit

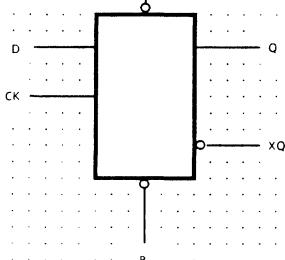
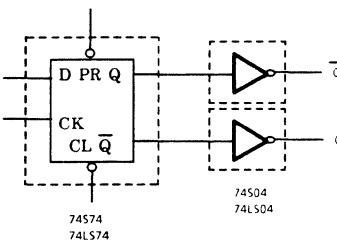
Function Table

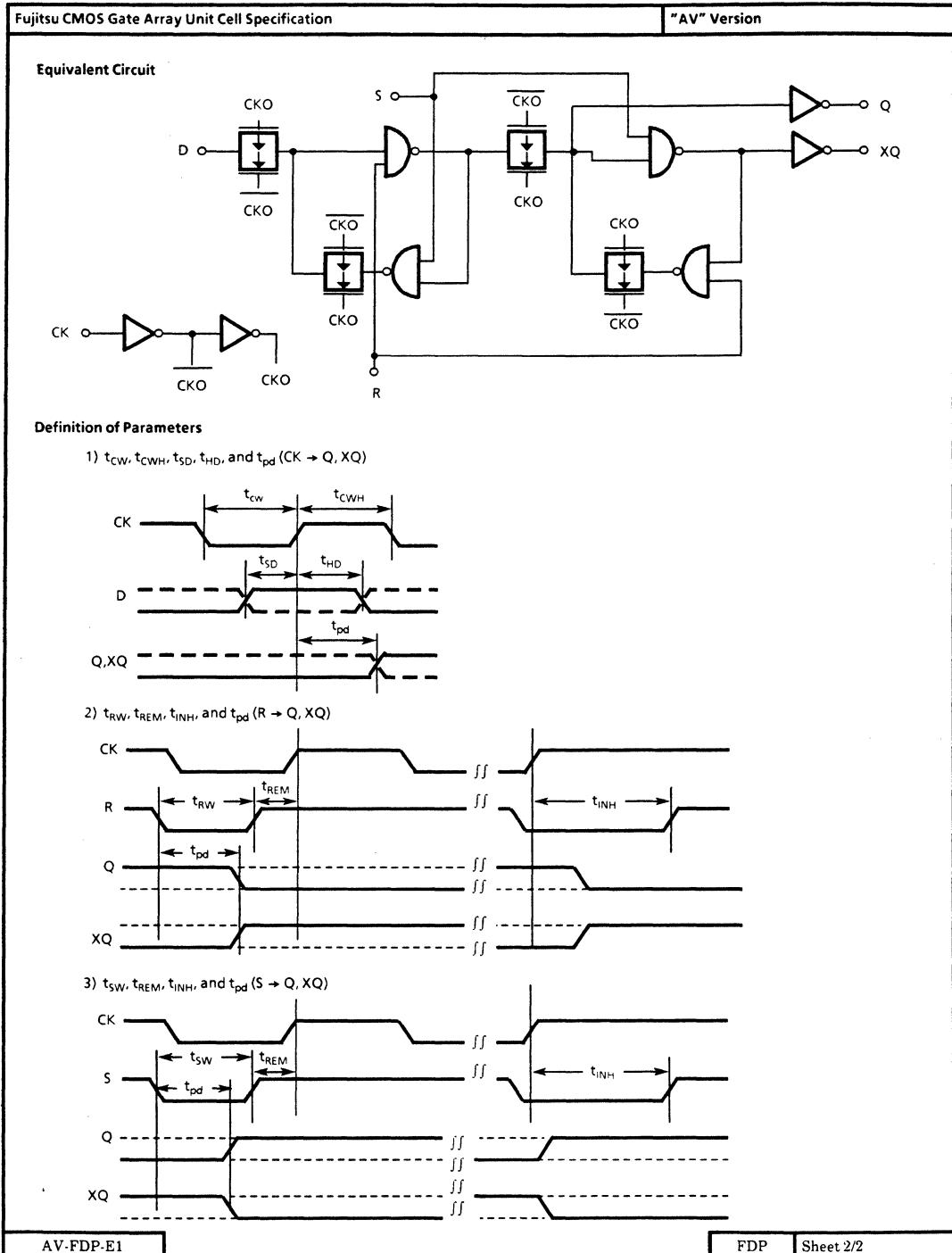


Inputs			Outputs	
S	D	CK	Q	XQ
L	X	X	H	L
H	H	↑	H	L
H	L	↓	L	H

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Equivalent Circuit	
Definition of Parameters	
1) t_{CW} , t_{CWH} , t_{SD} , t_{HD} , and t_{pd} ($CK \rightarrow Q, XQ$)	
2) t_{SW} , t_{REM} , t_{INH} , and t_{pd} ($S \rightarrow Q, XQ$)	
AV-FDN-E1	FDN Sheet 2/2



Cell Name	Function				Number of BC						
FDP	DFF with SET and RESET				8						
Cell Symbol		Propagation Delay Parameters									
		t_{up}		t_{dn}							
		t_o	K_{CL}	t_o	K_{CL}						
		3.46 6.10 2.96 2.86	0.25 0.25 0.25 0.25	5.16 4.42 1.40 1.92	0.14 0.14 0.14 0.14	$CK \rightarrow Q$ $CK \rightarrow XQ$ $S \rightarrow Q, XQ$ $R \rightarrow Q, XQ$					
		Parameter	Symbol	MIN	TYP	MAX	UNIT				
		Clock Pulse Width	t_{CW}		6		ns				
		Data Set Up Time	t_{SD}		2		ns				
		Data Hold Time	t_{HD}		2		ns				
		Set Pulse Width	t_{SW}		3		ns				
		Reset Pulse Width	t_{RW}		3		ns				
		Clock Pause Time	t_{CWH}		6		ns				
		Reset Release Time	t_{REM}		1		ns				
		Set Release Time	t_{REM}		1		ns				
		Reset Hold Time	t_{INH}		4		ns				
		Set Hold Time	t_{INH}		4		ns				
Input Loading Factor		Pin Name									
2 ℓu		D, S, R									
1 ℓu		CK									
Output Driving Factor		Pin Name									
18 ℓu		Q, XQ									
TTL Equivalent Circuit						Function Table					
						Inputs					
						S	R	D	CK	Q	XQ
						H	L	X	X	L	H
						L	H	X	X	H	L
						L	L	X	X	INHIBITED	
						H	H	H	X	H	L
						H	H	L	↑	L	H
AV-FDP-E1						FDP		Sheet 1/2			



Cell Name	Function					Number of BC					
FDQ	4-bit DFF					21					
Cell Symbol	Propagation Delay Parameters				Path						
	t_{up}		t_{dn}								
	t_o	KCL	t_o	KCL							
	8.32	0.25	6.58	0.14	CK \rightarrow Q						
	Parameter		Symbol	MIN	TYP	MAX					
	Clock Pulse Width		t_{CW}		6						
	Data Set Up Time		t_{SD}		1						
	Data Hold Time		t_{HD}		5						
	Clock Pause Time		t_{CWL}		7						
Input Loading Factor	Pin Name										
1 ℓ u	D, CK										
Output Driving Factor	Pin Name										
18 ℓ u	Q										
TTL Equivalent Circuit											
AV-FDQ-E1				FDQ	Sheet 1/2						

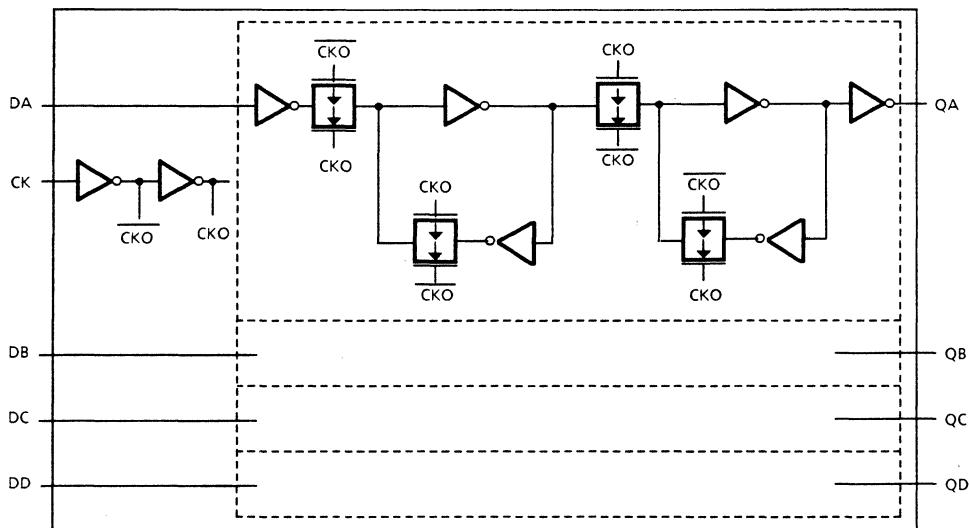
Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

Function Table

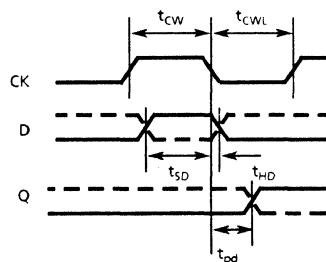
Input	Output	
CK	D	Q
↓	H L	H L

Equivalent Circuit



3

Definition of Parameters



Cell Name	Function					Number of BC					
FDR	4-bit DFF with CLEAR					26					
Cell Symbol	Propagation Delay Parameters				Path						
	t_{up}		t_{dn}								
	t_o	K _{CL}	t_o	K _{CL}							
	8.36	0.25	6.68 3.52	0.14 0.14	CK → Q CL → Q						
	Parameter		Symbol	MIN	TYP	MAX					
	Clock Pulse Width		t_{CW}		8						
	Data Set Up Time		t_{SD}		1						
	Data Hold Time		t_{HD}		5						
	Clear Pulse Width		t_{LW}		5						
	Clear Release Time		t_{REM}		3						
	Clear Hold Time		t_{INH}		3						
	Clock Pause Time		t_{CWH}		6						
Input Loading Factor	Pin Name										
1 ℓu	D, CK, CL										
Output Driving Factor	Pin Name										
18 ℓu	Q										
TTL Equivalent Circuit											
AV-FDR-E1				FDR	Sheet 1/2						

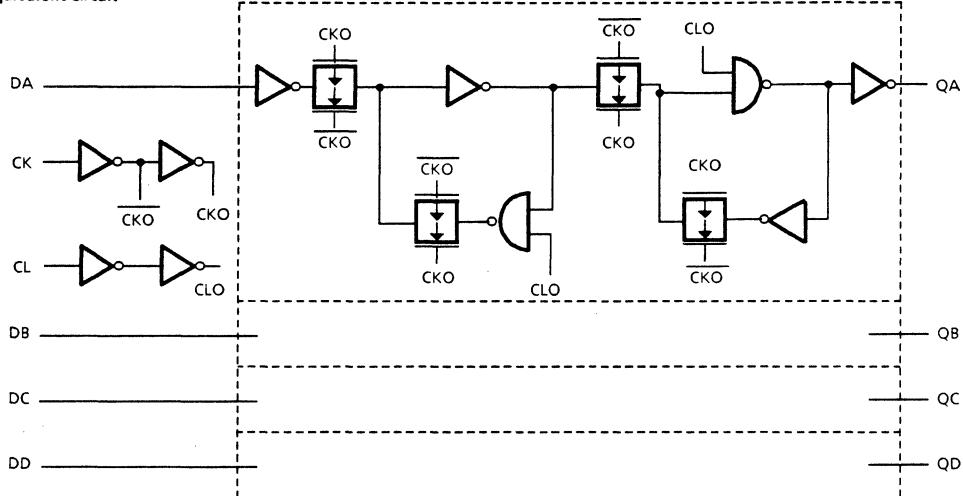
Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

Function Table

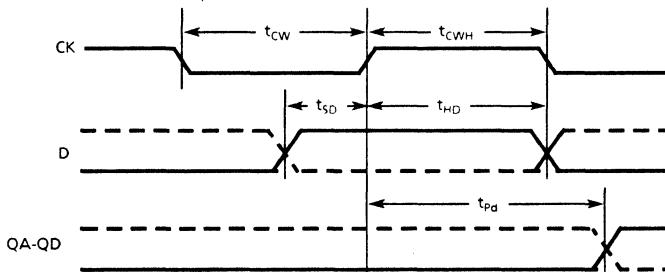
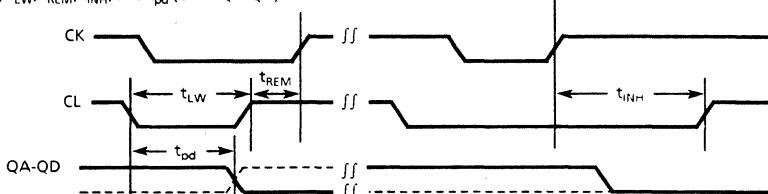
Inputs			Outputs
CK	D	CL	Q
X ↑ L H	X L H	L H	L H

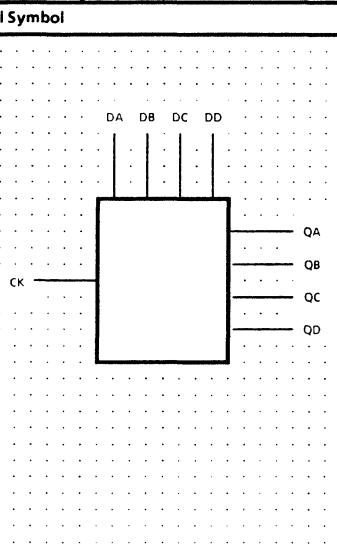
Equivalent Circuit



3

Definition of Parameters

1) t_{CW} , t_{CWH} , t_{SD} , t_{HD} , and t_{pd} (CK \rightarrow QA-QD)2) t_{LW} , t_{REM} , t_{INH} , and t_{pd} (CL \rightarrow QA-QD)

Cell Name	Function				Number of BC
FDS	Positive Edge Clocked 4-bit DFF				20
Cell Symbol	Propagation Delay Parameters				
	t_{up}		t_{dn}		Path
	t_0	K_{CL}	t_0	K_{CL}	
	5.96	0.25	7.66	0.14	CK → Q
Parameter	Symbol	MIN	TYP	MAX	UNIT
Clock Pulse Width (Low)	t_{CW}		8		ns
Data Set Up Time	t_{SD}		1		ns
Data Hold Time	t_{HD}		5		ns
Clock Pause Time	t_{CWH}		6		ns
Input Loading Factor	Pin Name				
2 ℓ_u	DA~DD CK				
Output Driving Factor	Pin Name				
18 ℓ_u	QA~QD				
AV-FDS-E1		FDS	Sheet 1/2		

Fujitsu CMOS Gate Array Unit Cell Specification		"AV" Version						
Function Table								
<table border="1"> <thead> <tr> <th>Inputs</th><th>Outputs</th></tr> </thead> <tbody> <tr> <td>CK D</td><td>Q</td></tr> <tr> <td>↑ L H</td><td>L H</td></tr> </tbody> </table>			Inputs	Outputs	CK D	Q	↑ L H	L H
Inputs	Outputs							
CK D	Q							
↑ L H	L H							
Equivalent Circuit								
Timing Diagram								
AV-FDS-E1	FDS	Sheet 2/2						

3

Fujitsu CMOS Gate Array Unit Cell Specification

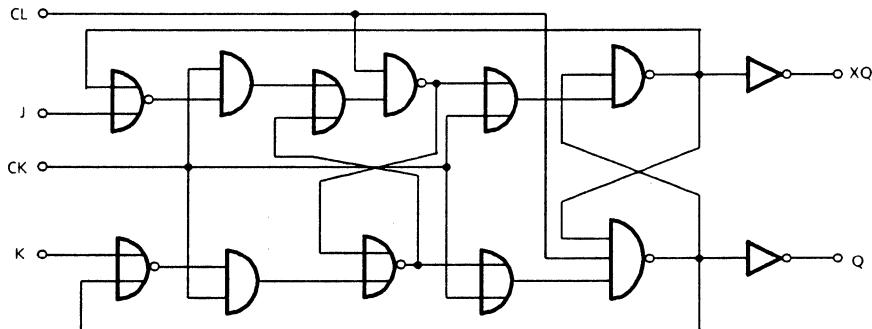
"AV" Version

Function Table

Inputs				Outputs	
CL	CK	J	K	Q	XQ
L	X	X	X	L	H
H		H	H	Q0	XQ0
H		H	L	L*	H*
H		L	H	H*	L*
H		L	L	XQ0	Q0

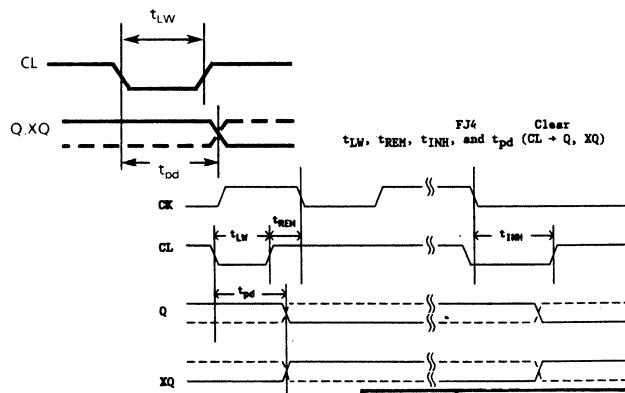
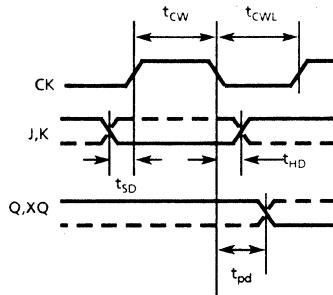
*Note:
In a logic simulation, this Flip-Flop must be initialized by "CL" input in order to achieve these outputs. If not, the outputs remain "X" (unknown state).

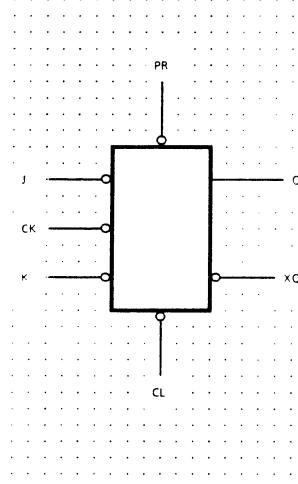
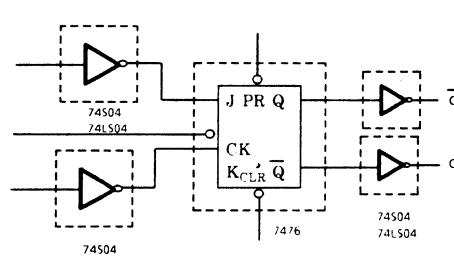
Equivalent Circuit



3

Definition of Parameters



Cell Name	Function					Number of BC
FJ5	Power JKFF with CLEAR and PRESET					12
Cell Symbol	Propagation Delay Parameters				Path	
	t_{up}		t_{dn}			
	t_o	KCL	t_o	KCL		
	6.63 6.63 6.63	0.12 0.12 0.12	4.14 4.14 4.14	0.07 0.07 0.07	CK → Q, XQ CL → Q, XQ PR → Q, XQ	
Parameter	Symbol	MIN	TYP	MAX	UNIT	
Clock Pulse Width	t_{CW}		5		ns	
Preset Pulse Width	t_{PW}		6		ns	
Clear Pulse Width	t_{LW}		6		ns	
J, K Set Up Time	t_{SD}		2		ns	
J, K Hold Time	t_{HD}		1		ns	
Clock Pause Time	t_{CWL}		5		ns	
Input Loading Factor	Pin Name					
4 ℓu 2 ℓu 2 ℓu 1 ℓu	CK CL PR J, K					
Output Driving Factor	Pin Name					
36 ℓu	Q,XQ					
TTL Equivalent Circuit						
						
AV-FJ5-E1					FJ5	Sheet 1/2

Fujitsu CMOS Gate Array Unit Cell Specification

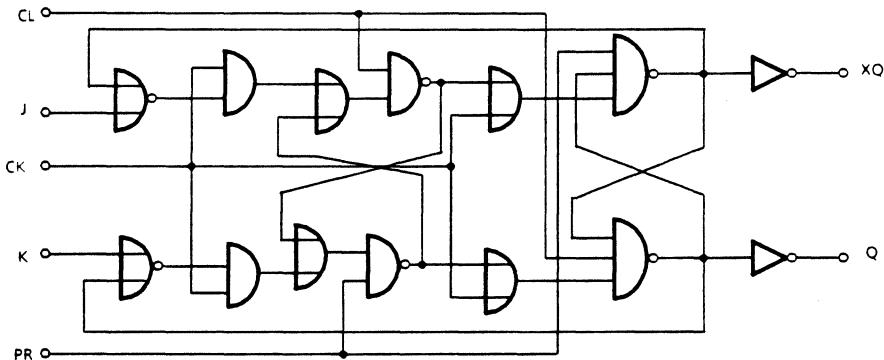
"AV" Version

Function Table

Inputs					Outputs	
PR	CL	CK	J	K	Q	XQ
L	L	X	X	X	Inhibited	
L	H	X	X	X	H	L
H	L	X	X	X	L	H
H	H		H	H	Q ₀	XQ ₀
H	H		H	L	L*	H*
H	H		L	H	H*	L*
H	H		L	L	XQ ₀	Q ₀

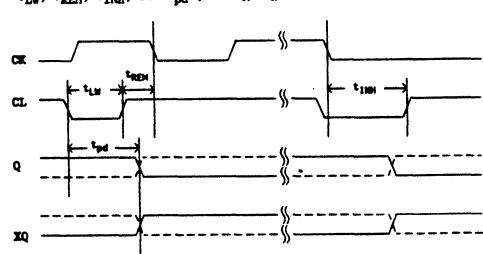
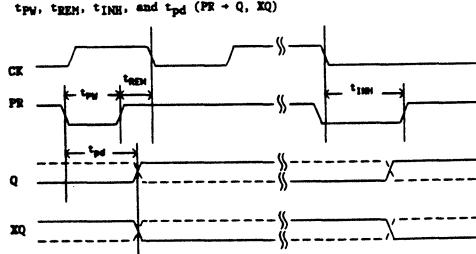
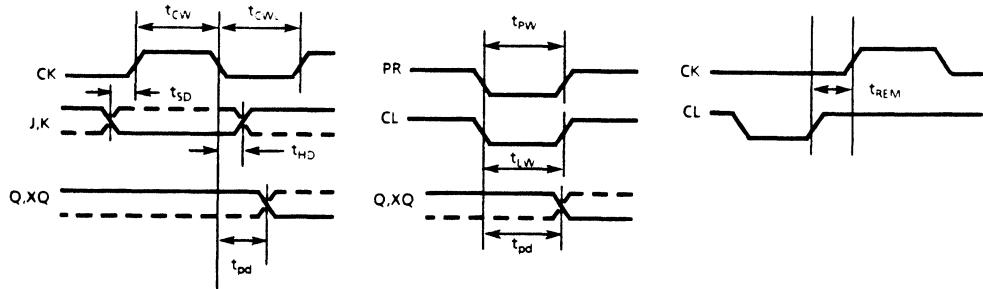
*Note:
In a logic simulation, this Flip-Flop must
be initialized by "CL" or "PR" input in
order to achieve these outputs. If not,
the outputs remain "X" (unknown state).

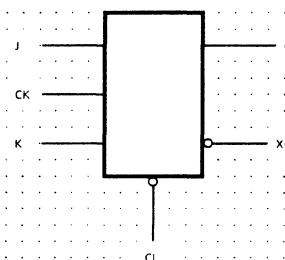
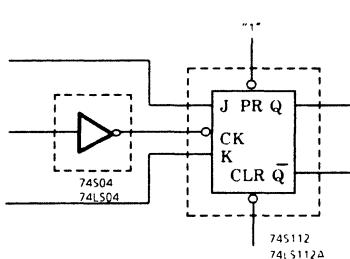
Equivalent Circuit



Definition of Parameters

3



Cell Name	Function					Number of BC					
FJD	Positive Edge Clocked Power JKFF with CLEAR					12					
Cell Symbol		Propagation Delay Parameters				Path					
		t_{up}		t_{dn}							
		t_o	K_{CL}	t_o	K_{CL}	CK → Q, XQ CL → Q, XQ					
		7.83 5.03	0.12 0.12	4.34 3.44	0.07 0.07						
Parameter	Symbol	MIN	TYP	MAX	UNIT						
Clock Pulse Width	t _{CW}		6			ns					
Clear Pulse Width	t _{LW}		5			ns					
J, K Set Up Time	t _{SD}		6			ns					
J, K Hold Time	t _{HD}		1			ns					
Clock Pause Time	t _{CWH}		6			ns					
Input Loading Factor		Pin Name									
2 ℓ_u 1 ℓ_u 1 ℓ_u		CL CK J, K									
Output Driving Factor		Pin Name									
36 ℓ_u		Q, XQ									
TTL Equivalent Circuit											
											
AV-FJD-E1		FJD		Sheet 1/2							

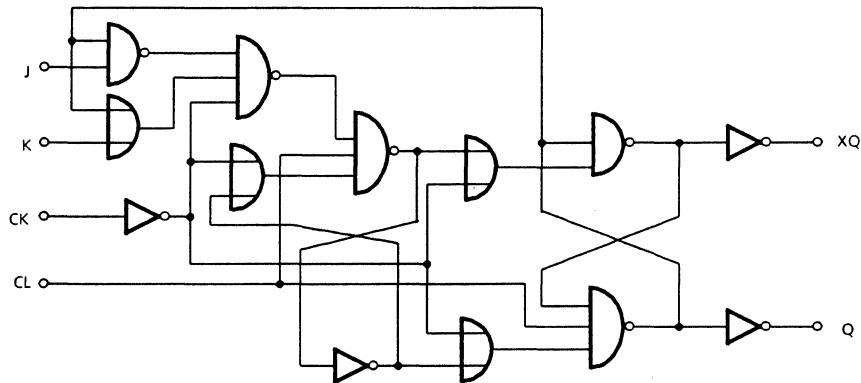
Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

Function Table

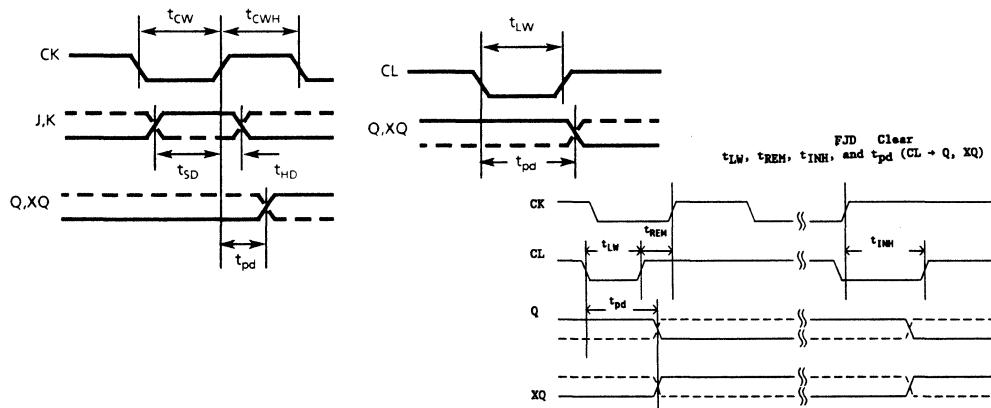
Inputs				Outputs	
CL	CK	J	K	Q	XQ
L	X	X	X	L	H
H	+	L	L	Q ₀	XQ ₀
H	+	L	H	L	H
H	+	H	L	H	L
H	+	H	H	XQ ₀	Q ₀

Equivalent Circuit



3

Definition of Parameters



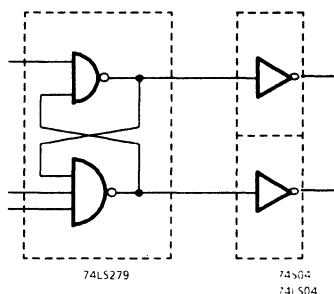
Data Latch Family

Page	Unit Cell Name	Function	Basic Cells
3-149	LT1	S-R Latch with Clear	4
3-151	LT2	1-bit Data Latch	4
3-153	LT2	4-bit Data Latch	15
3-155	LT4	4-bit Data Latch	13
3-157	LTK	Data Latch	4
3-159	LTL	Data Latch with Clear	5
3-161	LTM	4-bit Data Latch with Clear	15

3

3

TTL Equivalent Circuit



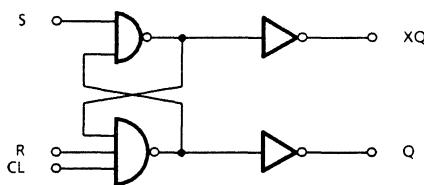
Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

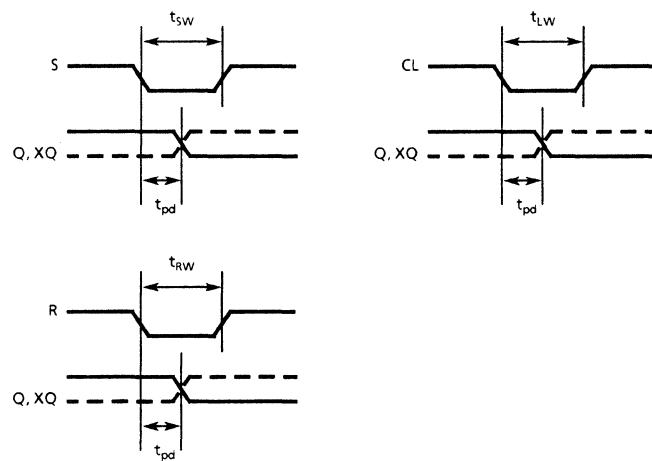
Function Table

Inputs			Outputs	
CL	S	R	Q	XQ
L	H	H	L	H
H	H	H	Q ₀	XQ ₀
H	H	L	L	H
H	L	H	H	L
H	L	L	Inhibited	

Equivalent Circuit



Definition of Parameters



Cell Name	Function	Propagation Delay Parameters				Number of BC
LT2	1-bit DATA Latch					4
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}	t_{dn}	t_o	K_{CL}	
1.84	0.25	3.09	0.14	G → Q		
3.94	0.25	2.59	0.14	G → XQ		
1.44	0.25	3.09	0.14	D → Q		
3.94	0.25	2.19	0.14	D → XQ		
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX
2 ℓu 1 ℓu		G Input Pulse Width	t_{GW}	5		ns
Data Set Up Time		t_{SD}		4		ns
Data Hold Time		t_{HD}		1		ns
Output Driving Factor		Pin Name				
18 ℓu		G				
		D				
TTL Equivalent Circuit						
		74LS51	74LS51	74LS04	74LS04	

3

Fujitsu CMOS Gate Array Unit Cell Specification		"AV" Version																								
Function Table																										
<table border="1"> <thead> <tr> <th colspan="2">Inputs</th><th colspan="2">Outputs</th></tr> <tr> <th>D</th><th>G</th><th>Q</th><th>XQ</th></tr> </thead> <tbody> <tr> <td>H</td><td>H</td><td>Q₀</td><td>XQ₀</td></tr> <tr> <td>L</td><td>H</td><td>Q₀</td><td>XQ₀</td></tr> <tr> <td>H</td><td>L</td><td>H</td><td>L</td></tr> <tr> <td>L</td><td>L</td><td>L</td><td>H</td></tr> </tbody> </table>			Inputs		Outputs		D	G	Q	XQ	H	H	Q ₀	XQ ₀	L	H	Q ₀	XQ ₀	H	L	H	L	L	L	L	H
Inputs		Outputs																								
D	G	Q	XQ																							
H	H	Q ₀	XQ ₀																							
L	H	Q ₀	XQ ₀																							
H	L	H	L																							
L	L	L	H																							
Equivalent Circuit																										
Definition of Parameters																										
<p>(Case 1)</p>																										
<p>(Case 2)</p>																										
<p>Note: When Data input is high level and G input transfers from high to low level, a spike noise occurs as below</p>																										
AV-LT2-E1	Spike (Several nano seconds: 1 Inverter Gate Delay time)																									
LT2		Sheet 2/2																								

Cell Name	Function					Number of BC																							
LT3	4-bit Data Latch					15																							
Cell Symbol	Propagation Delay Parameters				Path																								
	t_{up}		t_{dn}																										
	t_o	K _{CL}	t_o	K _{CL}																									
DA	3.04 5.54 1.44 3.94	0.25 0.25 0.25 0.25	4.69 3.79 3.09 2.19	0.14 0.14 0.14 0.14	G → P G → N D → P D → N																								
DB																													
DC																													
DD																													
G																													
Input Loading Factor	Pin Name																												
5 ℓ u 1 ℓ u	G D																												
Output Driving Factor	Pin Name																												
18 ℓ u	Any Output																												
TTL Equivalent Circuit	Function Table																												
<p>74LS04 74L504</p> <p>74L75 74LS75</p>	<table border="1"> <thead> <tr> <th>INPUTS</th><th colspan="2">OUTPUTS</th></tr> <tr> <th>D</th><th>G</th><th>P</th><th>N</th></tr> </thead> <tbody> <tr> <td>H</td><td>H</td><td>P_o</td><td>No</td></tr> <tr> <td>L</td><td>H</td><td>P_o</td><td>No</td></tr> <tr> <td>H</td><td>L</td><td>H</td><td>L</td></tr> <tr> <td>L</td><td>L</td><td>L</td><td>H</td></tr> </tbody> </table>						INPUTS	OUTPUTS		D	G	P	N	H	H	P _o	No	L	H	P _o	No	H	L	H	L	L	L	L	H
INPUTS	OUTPUTS																												
D	G	P	N																										
H	H	P _o	No																										
L	H	P _o	No																										
H	L	H	L																										
L	L	L	H																										
AV-LT3-E1																													
	LT3	Sheet 1/2																											

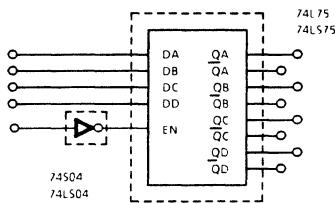
Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Equivalent Circuit	
Definition of Parameters	
<p>(Case 1)</p>	
<p>(Case 2)</p>	
<p>Note: When Data input is high level and G input transfers from high to low level, a spike noise occurs as below.</p>	
AV-LT3-E1	LT3 Sheet 2/2

Cell Name	Function	Number of BC															
LT4	4-bit Data Latch	13															
Cell Symbol	Propagation Delay Parameters																
	t_{up}		t_{dn}		Path												
	t_o	K _{CL}	t_o	K _{CL}													
DA	6.74 5.80 1.42 2.43	0.25 0.25 0.25 0.25	5.00 7.50 1.63 2.18	0.14 0.14 0.14 0.14	G → P G → N D → P D → N												
DB																	
DC																	
DD																	
G																	
PA																	
NA																	
PB																	
NB																	
PC																	
NC																	
PD																	
ND																	
Input Loading Factor																	
1 ℓu	G																
2 ℓu	D																
Output Driving Factor																	
18 ℓu	Any Output																
TTL Equivalent Circuit																	
Function Table																	
<table border="1"> <thead> <tr> <th>Inputs</th> <th>Outputs</th> </tr> <tr> <th>D G</th> <th>P N</th> </tr> </thead> <tbody> <tr> <td>H H</td> <td>Po No</td> </tr> <tr> <td>L H</td> <td>Po No</td> </tr> <tr> <td>H L</td> <td>H L</td> </tr> <tr> <td>L L</td> <td>L H</td> </tr> </tbody> </table>						Inputs	Outputs	D G	P N	H H	Po No	L H	Po No	H L	H L	L L	L H
Inputs	Outputs																
D G	P N																
H H	Po No																
L H	Po No																
H L	H L																
L L	L H																

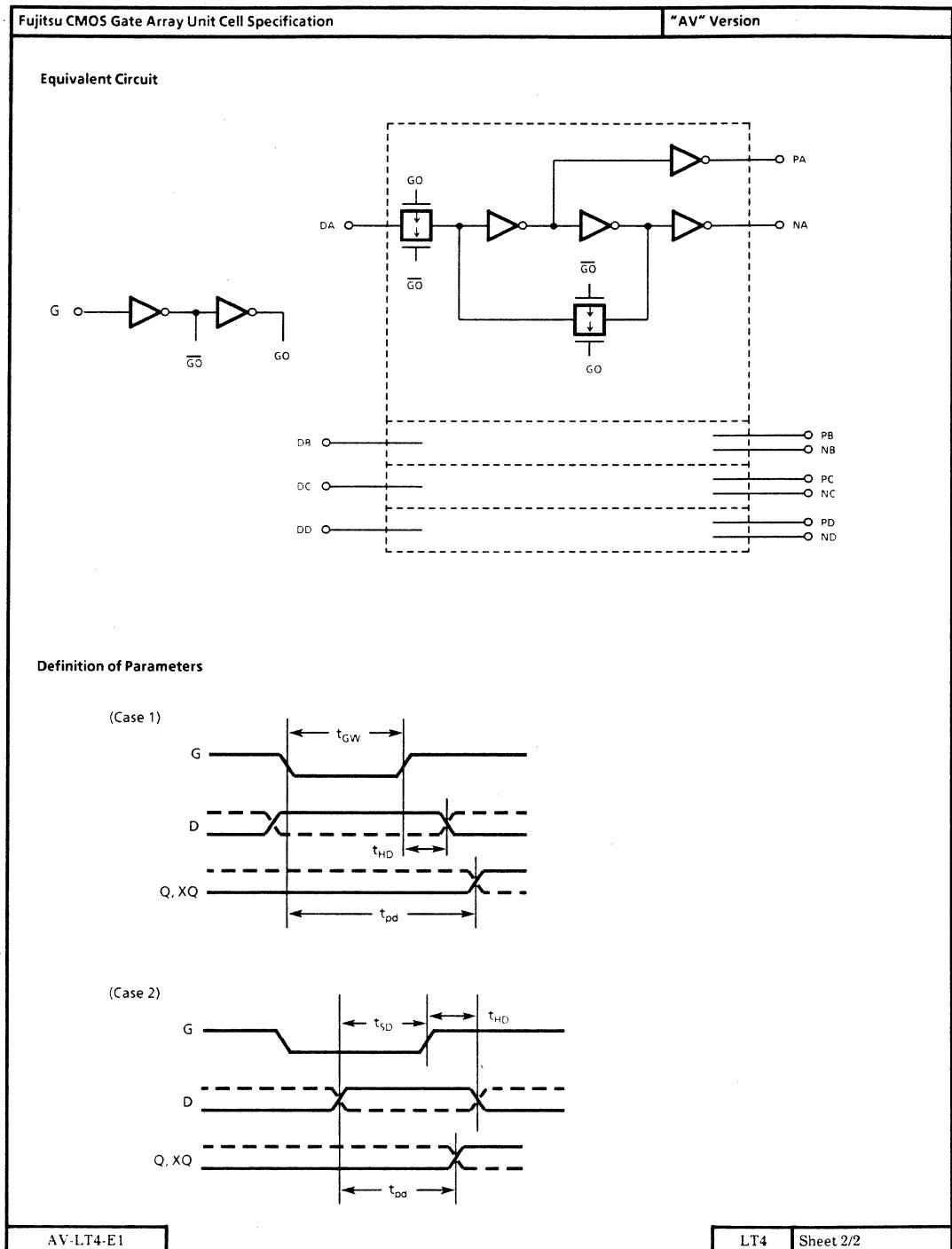
3

TTL Equivalent Circuit

Function Table



Inputs		Outputs	
D	G	P	N
H	H	Po	No
L	H	Po	No
H	L	H	L
L	L	L	H



Cell Name	Function	Propagation Delay Parameters				Number of BC
LTK	1-bit Data Latch					4
Cell Symbol		t_{up}		t_{dn}		Path
		t_o	K_{CL}	t_o	K_{CL}	
		1.42	0.25	1.63	0.14	D → Q
		2.43	0.25	2.18	0.14	D → XQ
		5.35	0.25	3.61	0.14	G → Q
		4.41	0.25	6.11	0.14	G → XQ
Parameter	Symbol	MIN	TYP	MAX	UNIT	
G Input Pulse Width	t_{GW}		6			ns
Data Set Up Time	t_{SD}		2			ns
Data Hold Time	t_{HD}		2			ns
Input Loading Factor	Pin Name					
2 ℓ_u 1 ℓ_u	D G					
Output Driving Factor	Pin Name					
18 ℓ_u 18 ℓ_u	Q XQ					

3

Function Table

Inputs		Outputs	
D	G	Q	XQ
X	H	Q ₀	XQ ₀
H	L	H	L
L	L	L	H

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Equivalent Circuit	
Definition of Parameters	
<p>3</p> <p>(Case 1)</p>	
<p>(Case 2)</p>	
AV-LTK-E1	LTK Sheet 2/2

3

Function Table

Inputs			Outputs	
CL	D	G	Q	XQ
L	X	H	L	H
H	X	H	Q ₀	XQ ₀
H	H	L	H	L
H	L	L	L	H

Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

Equivalent Circuit

Definition of Parameters

(Case 1)

(Case 2)

(Case 3)

Note*:

G input must be high level at the time this latch is cleared.
If Clear is input, while G-input is low, the spike may be caused on the output or this latch may oscillate.

Cell Name	Function	Propagation Delay Parameters				Number of BC
Cell Symbol		t_{up}		t_{dn}		Path
		t_o	K_{CL}	t_o	K_{CL}	
DA	PA	2.20	0.25	1.40	0.14	CL → P,N
DB	NA	1.56	0.25	1.83	0.14	D → P
DC	PB	2.63	0.25	2.32	0.14	D → N
DD	NB	6.88	0.25	5.20	0.14	G → P
G	PC	6.00	0.25	7.64	0.14	G → N
	NC					
	PD					
	ND					
	CL					
Input Loading Factor	Pin Name					
2 ℓu 1 ℓu 4 ℓu	DA ~ DD G CL					
Output Driving Factor	Pin Name					
18 ℓu 18 ℓu	PA ~ PD NA ~ ND					

3

Function Table

Inputs			Outputs	
CL	D	G	P	N
L	X	H	L	H
H	X	H	P ₀	N ₀
H	H	L	H	L
H	L	L	L	H

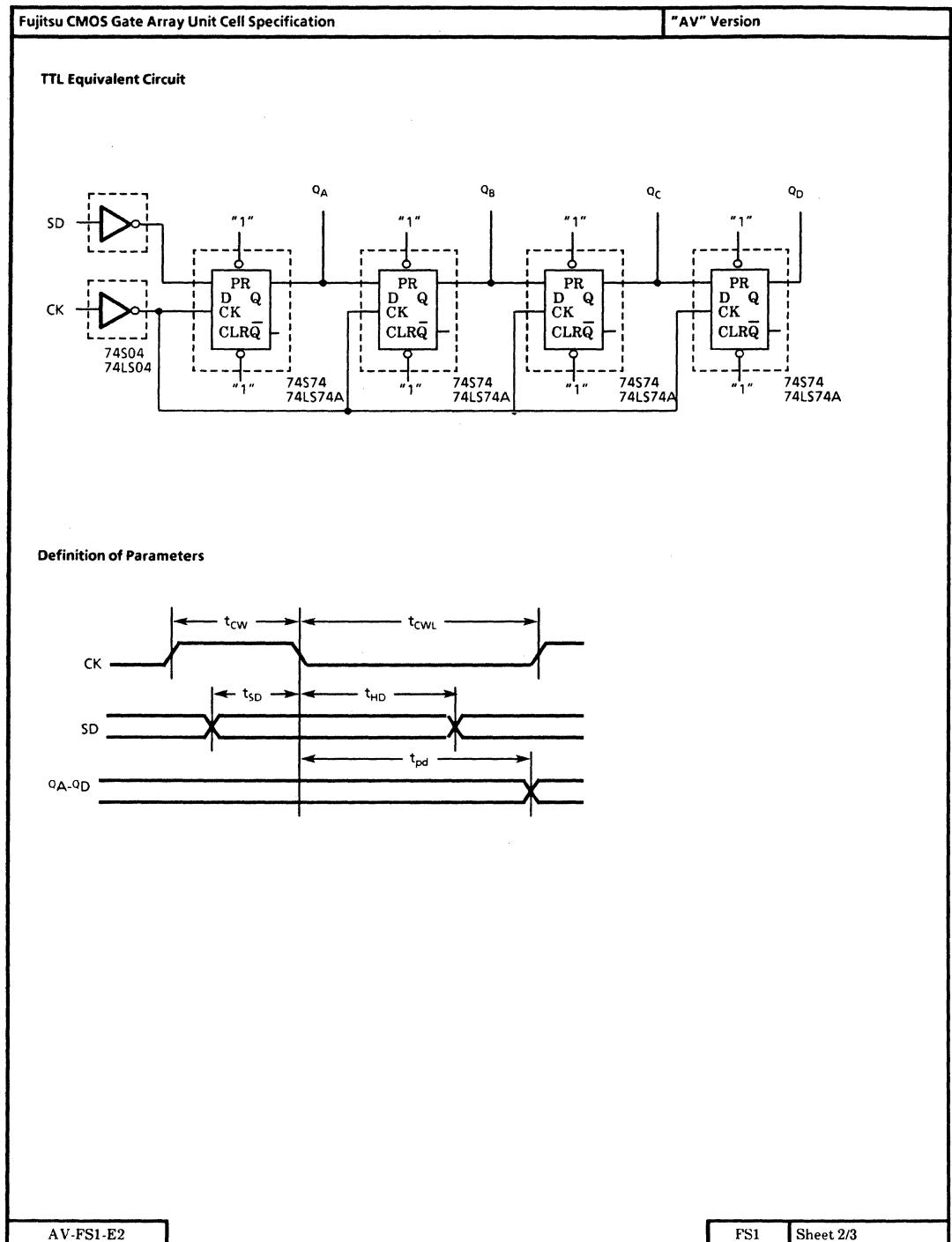
Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Equivalent Circuit	
Definition of Parameters	
<p>(Case 1)</p>	<p>(Case 3)</p>
<p>(Case 2)</p>	<p>Note*:</p> <p>G input must be high level at the time this latch is cleared.</p> <p>If Clear is inputted while G-input is low, the spike may be caused on the output or this latch may oscillate.</p>
AV-LTM-E1	LTM Sheet 2/2

Shift Register Family

Page	Unit Cell Name	Function	Basic Cells
3-165	FS1	4-bit Serial-in Parallel-out Shift Register	18
3-168	FS2	4-bit Shift Register with Synchronous Load	30
2-171	FS3	4-bit Shift Register with Asynchronous Load	34

3

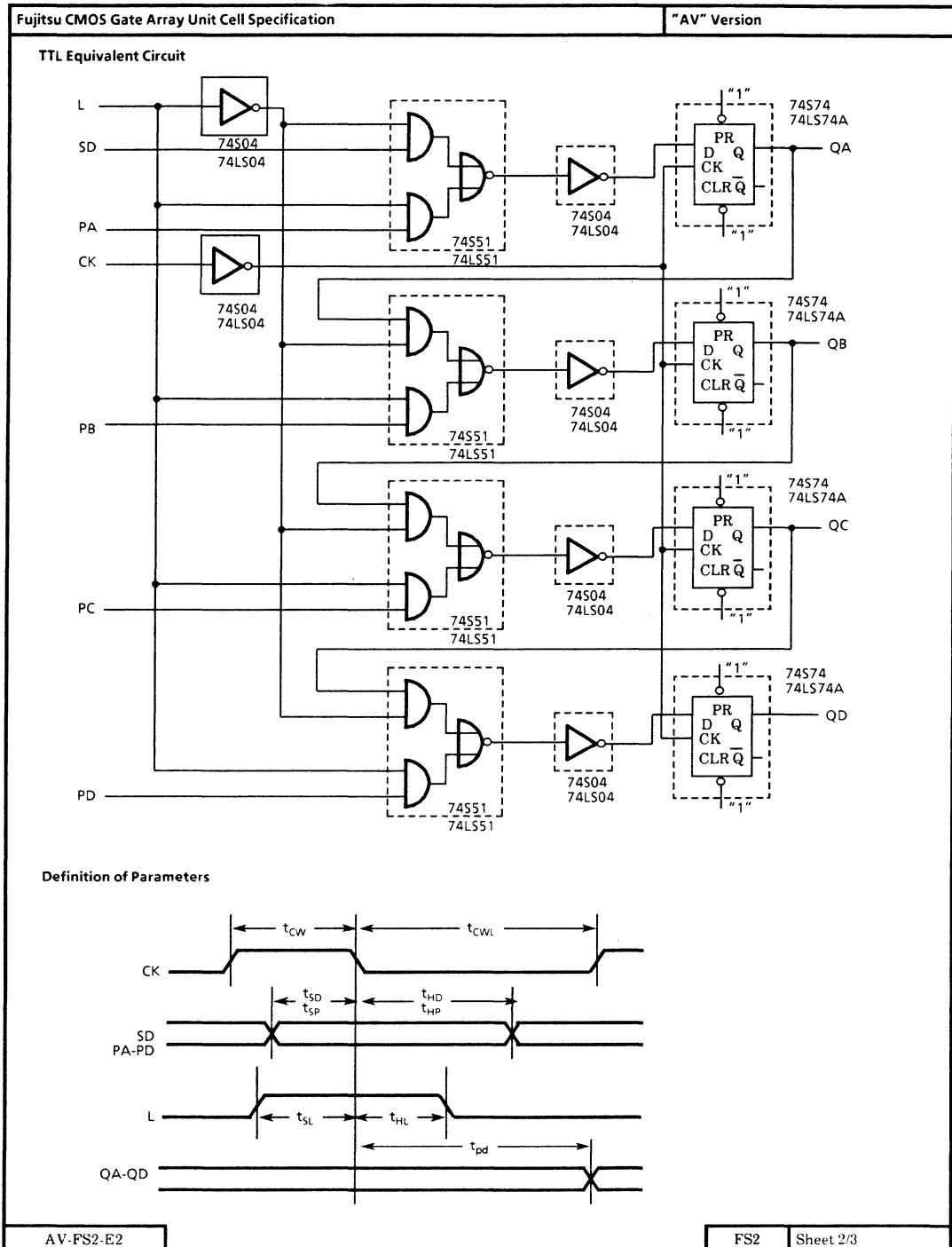
Cell Name	Function					Number of BC
FS1	4-bit Serial-in Parallel-out Shift Register					18
Cell Symbol	Propagation Delay Parameters				Path	
	t_{up}		t_{dn}			
	t_o	K_{CL}	t_o	K_{CL}	CK → Q	
	6.39	0.25	7.88	0.14		
	Parameter		Symbol	MIN	TYP	MAX
	Clock Pulse Width		t_{CW}		6	
	S-Data Set Up Time		t_{SD}		1	
	S-Data Hold Time		t_{HD}		5	
	Clock Pause Time	C = 16 ℓu	t_{CWL}^*		9	
		C = 32 ℓu	t_{CWL}^*		15	
		C = 64 ℓu	t_{CWL}^*		39	
Input Loading Factor	Pin Name					
1 ℓu 1 ℓu	SD CK					
Output Driving Factor	Pin Name					
16 ℓu	Q					
* The value of t_{CWL} depends on the load (C) connected to the output terminals, QA, QB, QC, and QD.						
Equivalent Circuit						
AV-FS1-E2	FS1 Sheet 1/3					



Fujitsu CMOS Gate Array Unit Cell Specification						"AV" Version
Function Table						
FS1						
Inputs		Outputs				
SD	CK	QA	QB	QC	QD	
SD	↓	SD	QAn	QBn	QCn	

Note:

- SD = H or L
- QAn, QBn, and QCn are levels of QA, QB, and QC, respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.



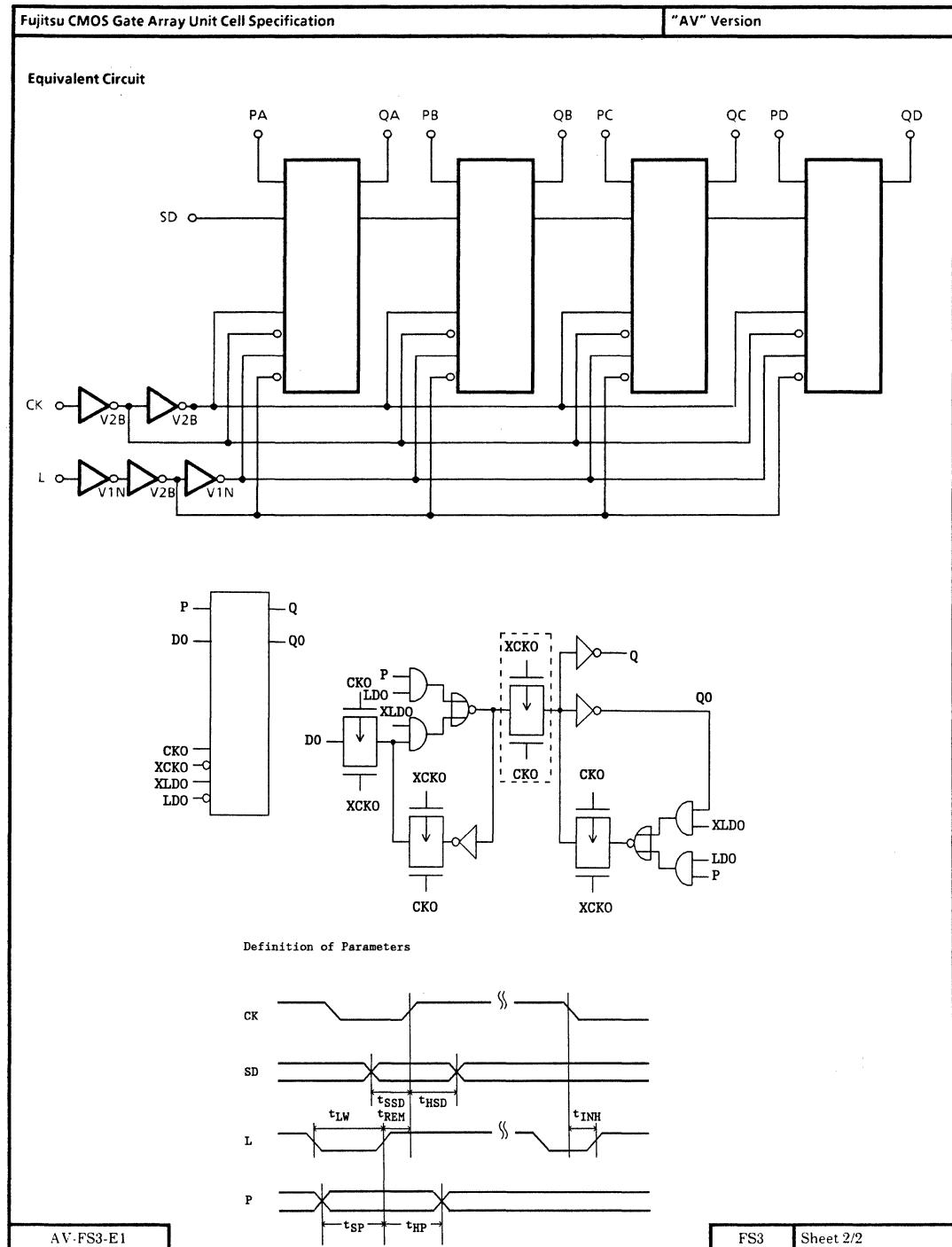
Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
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FS2 Function Table

Inputs				Outputs			
SD	L	P	CK	QA	QB	QC	QD
SD	L	X	↓	SD	QAn	QBn	QCn
X	H	P	↓	PA	PB	PC	PD

- Note:
- SD = H or L
 - QAn, QBn, and QCn are levels of QA, QB, and QC, respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.
 - P represents PA, PB, PC, and PD.

Cell Name	Function					Number of BC	
FS3	4-bit Shift Register With Asynchronous Load					34	
Cell Symbol	Propagation Delay Parameters				Path		
	t_{up}		t_{dn}				
	t_0	KCL	t_0	KCL	$CK \rightarrow Q$ $L \rightarrow Q$ $P \rightarrow Q$		
	4.34 6.36 1.98	0.25 0.25 0.25	6.04 8.01 3.63	0.14 0.14 0.14			
Parameter	Symbol	MIN	TYP	MAX	UNIT		
Clock Pulse Width	t_{CW}		6		ns		
Load Pulse Width	t_{LW}		8		ns		
S-Data Set Up Time	t_{SD}		3		ns		
S-Data Hold Time	t_{HD}		3		ns		
P Set Up Time (Load)	t_{SP}		1		ns		
P Hold Time (Load)	t_{HP}		4		ns		
Load Release Time	t_{REM}		3		ns		
Load Hold Time	t_{INH}		3		ns		
Input Loading Factor							
2 ℓ_u 1 ℓ_u 2 ℓ_u		CK L PA~PD SD					
Output Driving Factor							
18 ℓ_u		QA~QD					
Function Table							
INPUTS			OUTPUT				
L	P	SD	CK	Q			
L	L	X	X	L			
L	H	X	X	H			
H	X	L	↑	L			
H	X	H	↑	H			

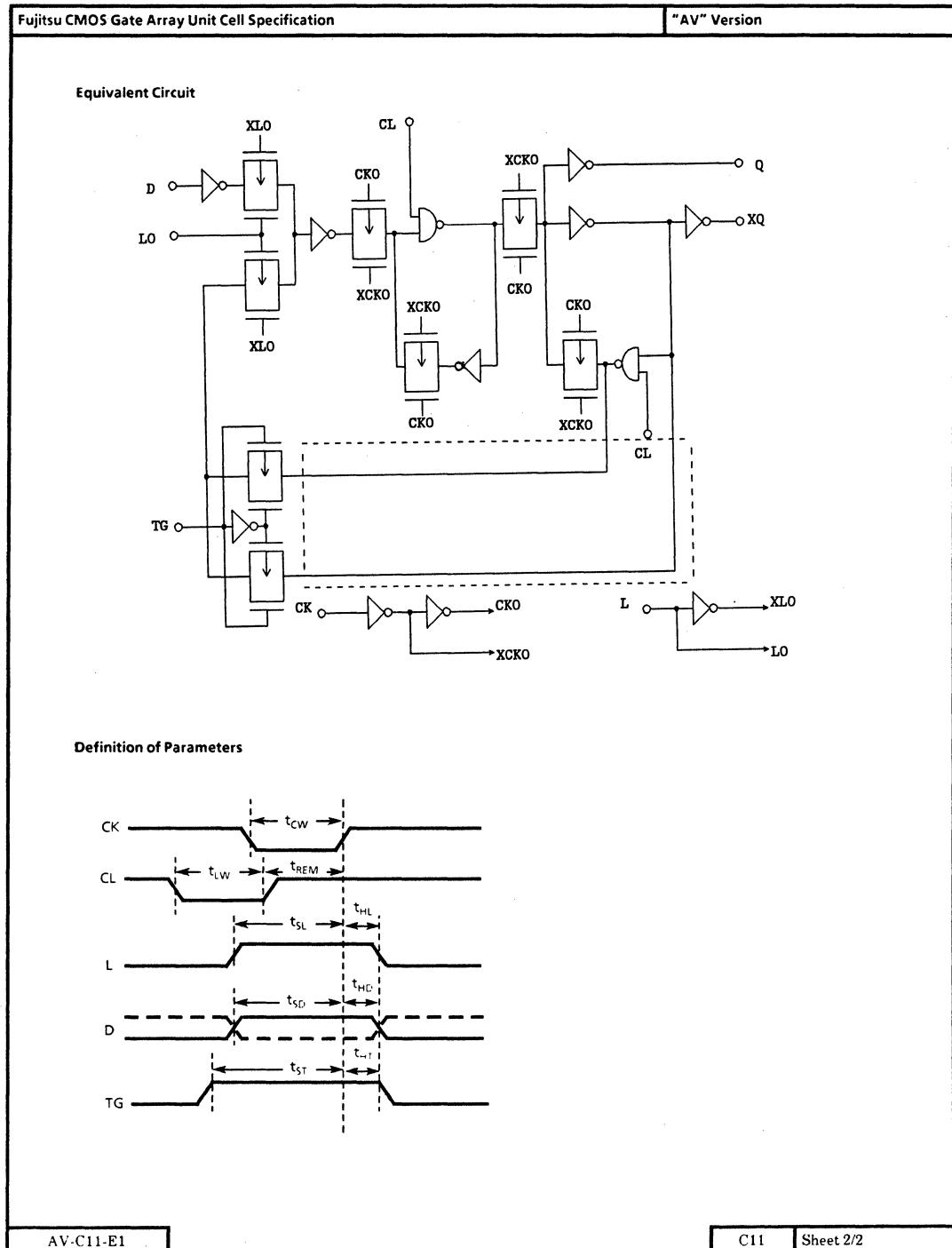


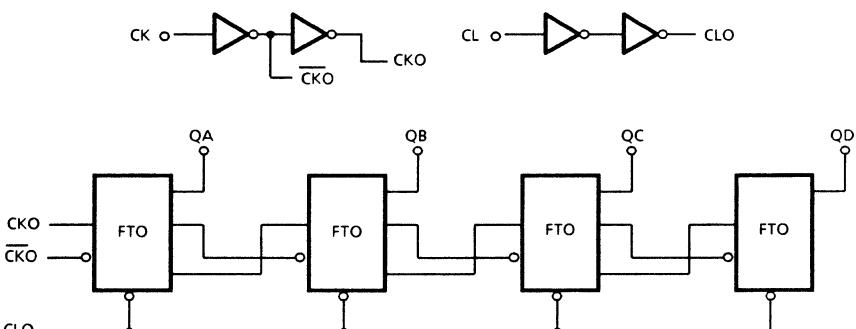
Counter Family

Page	Unit Cell Name	Function	Basic Cells
3-175	C11	Flip-Flop for Counter	11
3-177	C41	4-bit Binary Asynchronous Counter	24
3-180	C42	4-bit Binary Synchronous Counter	32
3-183	C43	4-bit Binary Synchronous Up Counter	48
3-186	C45	4-bit Binary Synchronous Up Counter	48
3-189	C47	4-bit Binary Synchronous Up/Down Counter	68

3

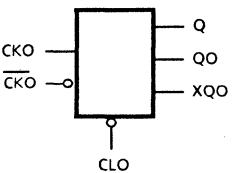
Cell Name	Function					Number of BC	
C11	Flip-Flop for Counter					11	
Cell Symbol	Propagation Delay Parameters					Path	
	t_{up}		t_{dn}				
	t_0	K_{CL}	t_0	K_{CL}			
	3.23 5.90 1.58 2.80	0.25 0.25 0.25 0.25	4.93 4.30 1.83 2.65	0.14 0.14 0.14 0.14	$CK \rightarrow Q$ $CK \rightarrow XQ$ $CL \rightarrow Q$ $CL \rightarrow XQ$		
Parameter		Symbol	MIN	TYP	MAX	UNIT	
Clock Pulse Width		t_{CPW}		6		ns	
Clear Pulse Width		t_{CPW}		3		ns	
Clear Release Time		t_{REM}		1		ns	
Load Set Up Time (CK)		t_{SL}		5		ns	
Load Hold Time (CK)		t_{HL}		1		ns	
Data Set Up Time (CK)		t_{SD}		3		ns	
Data Hold Time (CK)		t_{HD}		2		ns	
TG Set Up Time (CK)		t_{ST}		6		ns	
TG Hold Time (CK)		t_{HT}		1		ns	
Input Loading Factor		Pin Name					
1 ℓu 2 ℓu		D, CK L, TG, CL					
Output Driving Factor		Pin Name					
18 ℓu		Q, XQ					
Function Table							
L	D	TG	CL	CK	Q(Q ₀)		
X	X	X	L	X	L		
H	H	X	H	↑	H		
H	L	X	H	↑	L		
L	X	L	H	↑	Q(Q ₀)		
L	X	H	H	↑	$\bar{Q}(\bar{Q}_0)$		
AV-C11-E1		C11		Sheet 1/2			



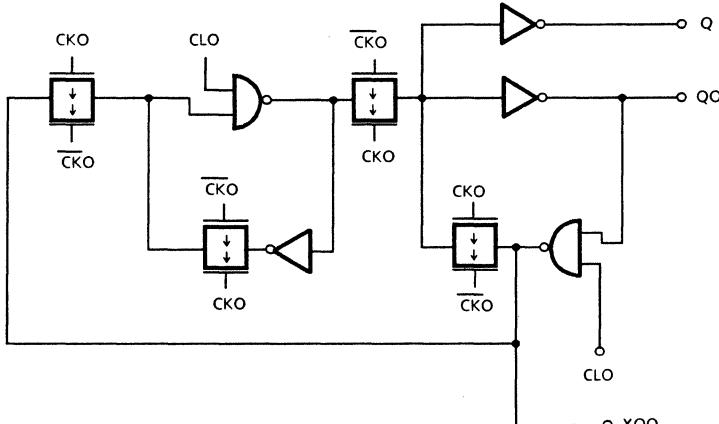
Cell Name	Function					Number of BC
C41	4-bit Binary Asynchronous Counter					24
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}		t_{dn}		
		t_o	K_{CL}	t_o	K_{CL}	
		QA 9.23 14.98 20.73	0.25 0.25 0.25	5.18 10.93 16.68 22.43 4.70	0.14 0.14 0.14 0.14 0.14	CK → QA CK → QB CK → QC CK → QD CL → Q
		Parameter				
		Clock Pulse Width	t_{CW}		5	ns
		Clear Pulse Width	t_{LW}		5	ns
		Clear Release Time	t_{REM}		4	ns
		Clear Hold Time	t_{INH}		3	ns
		Clock Pause Time	t_{CWH}		7	ns
Input Loading Factor		Pin Name				
1 ℓu		CK, CL				
Output Driving Factor		Pin Name				
18 ℓu		Any Output				
Equivalent Circuit						
AV-C41-E2		C41		Sheet 1/3		

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
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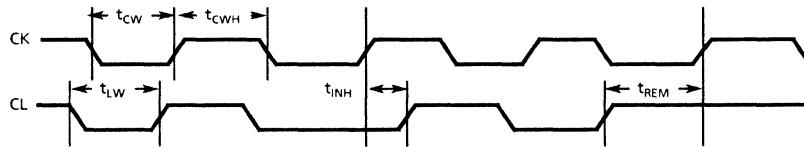
FTO (Flip-Flop for Counter) (not Unit Cell)

Symbol 	Function Table <table border="1" style="border-collapse: collapse; text-align: center;"> <tr> <th>CLO</th> <th>CKO</th> <th>Q</th> </tr> <tr> <td>L</td> <td>X</td> <td>L</td> </tr> <tr> <td>H</td> <td>↑</td> <td>$\overline{Q_{n-1}}$</td> </tr> </table>	CLO	CKO	Q	L	X	L	H	↑	$\overline{Q_{n-1}}$
CLO	CKO	Q								
L	X	L								
H	↑	$\overline{Q_{n-1}}$								

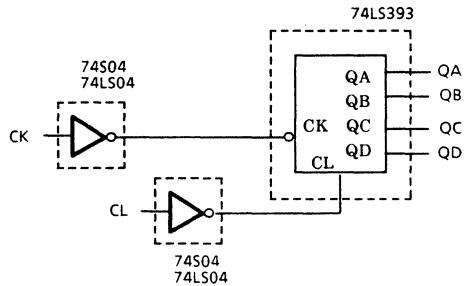
Internal Circuit Diagram



Definition of Parameters

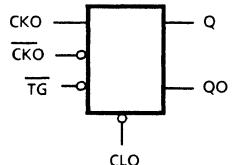
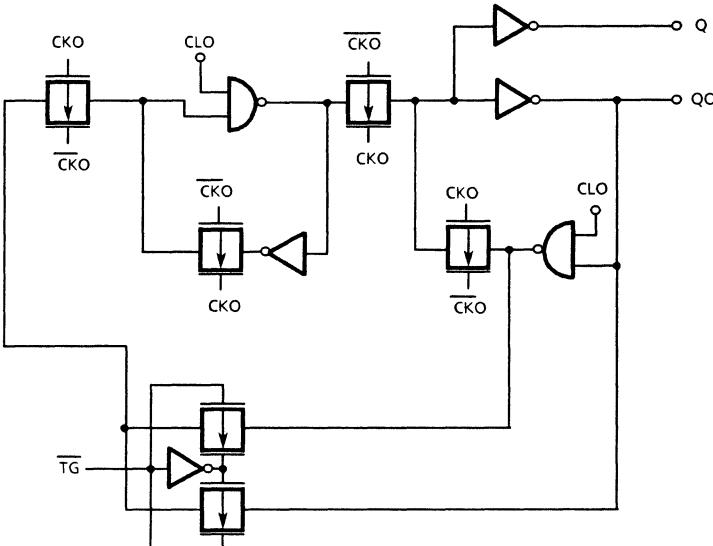
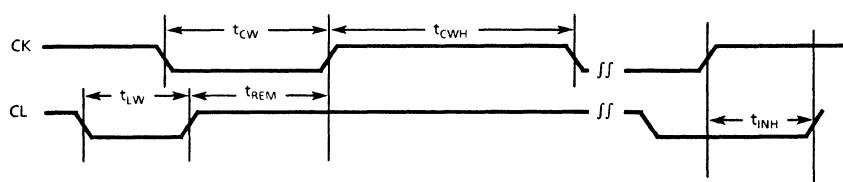


TTL Equivalent Circuit



Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version								
C41 Function Table									
<table border="1"><thead><tr><th>Inputs</th><th>Outputs</th></tr></thead><tbody><tr><td>CL</td><td>CK</td></tr><tr><td>H</td><td>↑</td></tr><tr><td>L</td><td>X</td></tr></tbody></table>	Inputs	Outputs	CL	CK	H	↑	L	X	(QA - QD) Count up L
Inputs	Outputs								
CL	CK								
H	↑								
L	X								

Cell Name	Function	Propagation Delay Parameters				Number of BC	
C42	4-bit Binary Synchronous Counter					32	
Cell Symbol		Propagation Delay Parameters				Path	
		t_{up}	t_{dn}	t_o	K_{CL}		
		6.55	0.25	8.25 4.06	0.14 0.14	$CK \rightarrow Q$ $CL \rightarrow Q$	
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX	UNIT
1 ℓu		Clock Pulse Width	t_{CPW}		8		ns
		Clear Pulse Width	t_{CPW}		5		ns
		Clear Release Time	t_{CREM}		3		ns
		Clock Pause Time	t_{CWH}		6		ns
		Clear Hold Time	t_{CHH}		4		ns
Output Driving Factor		Pin Name					
18 ℓu		CK, CL					
Equivalent Circuit							

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version																
FT2 (Flip-Flop for Counter) (not Unit Cell)																	
Symbol	Function Table																
	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>CLO</th> <th>\overline{TG}</th> <th>CKO</th> <th>Q(QO)</th> </tr> <tr> <td>L</td> <td>X</td> <td>X</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>\uparrow</td> <td>Q_{n-1}</td> </tr> <tr> <td>H</td> <td>L</td> <td>\uparrow</td> <td>$\overline{Q_{n-1}}$</td> </tr> </table>	CLO	\overline{TG}	CKO	Q(QO)	L	X	X	L	H	H	\uparrow	Q_{n-1}	H	L	\uparrow	$\overline{Q_{n-1}}$
CLO	\overline{TG}	CKO	Q(QO)														
L	X	X	L														
H	H	\uparrow	Q_{n-1}														
H	L	\uparrow	$\overline{Q_{n-1}}$														
																	
Definition of Parameters																	
																	
AV-C42-E2	C42 Sheet 2/3																

Fujitsu CMOS Gate Array Unit Cell Specification

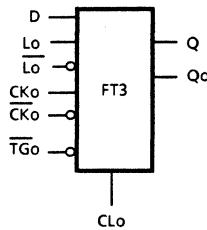
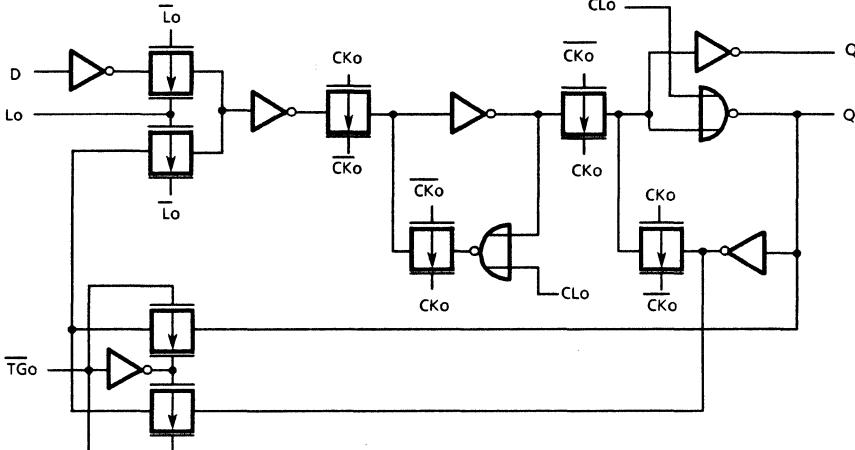
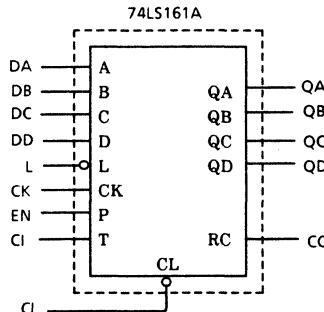
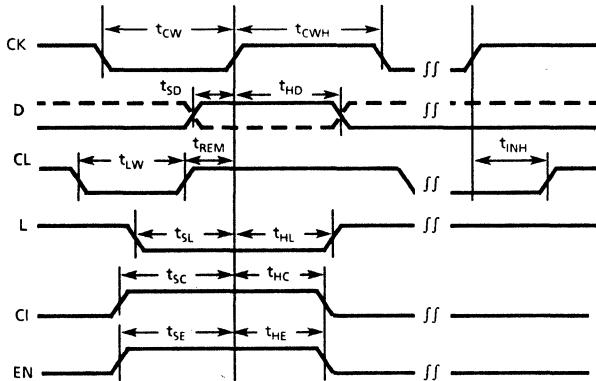
"AV" Version

C42
Function Table

Inputs		Outputs
CL	CK	(QA - QD)
H	↑	Count up
L	X	L

3

Cell Name	Function					Number of BC		
C43	4-bit Binary Synchronous Up Counter					48		
Cell Symbol	Propagation Delay Parameters				Path			
	t_{up}		t_{dn}					
	t_o	K_{CL}	t_o	K_{CL}				
DA	6.67	0.25	8.37	0.14	$CK \rightarrow Q$			
DB	13.40	0.25	12.44	0.14	$CK \rightarrow CO$			
DC	2.94	0.25	3.04	0.14	$CI \rightarrow CO$			
DD			5.54	0.14	$CL \rightarrow Q$			
L			9.61	0.14	$CL \rightarrow CO$			
CK								
EN								
CI								
CO								
Parameter	Symbol	MIN	TYP	MAX	UNIT			
Clock Pulse Width	t_{CW}		8		ns			
Data Set Up Time	t_{SD}		2		ns			
Data Hold Time	t_{HD}		4		ns			
Load Set Up Time	t_{SL}		4		ns			
Load Hold Time	t_{HL}		4		ns			
CI Set Up Time	t_{SC}		6		ns			
CI Hold Time	t_{HC}		1		ns			
EN Set Up Time	t_{SE}		6		ns			
EN Hold Time	t_{HE}		1		ns			
Clear Pulse Width	t_{LW}		7		ns			
Clear Release Time	t_{REM}		5		ns			
Clear Hold Time	t_{INH}		8		ns			
Clock Pause Time	t_{CWH}		8		ns			
Input Loading Factor	Pin Name							
1 ℓu	D							
1 ℓu	L, EN							
1 ℓu	CK, CL							
2 ℓu	CI							
Output Driving Factor	Pin Name							
18 ℓu	Any Output							
Equivalent Circuit	DA	QA	DB	QB	DC	QC	DD	QD
	CL	Clo	Lo	Lo	Lo	Lo	Lo	Lo
L	Lo	Lo	Lo	Lo	Lo	Lo	Lo	Lo
CK	CKo	CKo	CKo	CKo	CKo	CKo	CKo	CKo
CI								
EN								
	FT3		FT3		FT3		FT3	
AV-C43-E2					C43	Sheet 1/3		

Fujitsu CMOS Gate Array Unit Cell Specification		"AV Version																																					
FT3 (Flip-Flop for Counter) (not Unit Cell) 9B.C.																																							
Symbol 		Function Table <table border="1"> <thead> <tr> <th>Lo</th><th>D</th><th>\overline{TGo}</th><th>CLo</th><th>CK</th><th>Q(Qo)</th></tr> </thead> <tbody> <tr> <td>X</td><td>X</td><td>X</td><td>H</td><td>X</td><td>L</td></tr> <tr> <td>H</td><td>H</td><td>X</td><td>L</td><td>\uparrow</td><td>H</td></tr> <tr> <td>H</td><td>L</td><td>X</td><td>L</td><td>\uparrow</td><td>L</td></tr> <tr> <td>L</td><td>X</td><td>H</td><td>L</td><td>\uparrow</td><td>$Q(Qo)$</td></tr> <tr> <td>L</td><td>X</td><td>L</td><td>L</td><td>\uparrow</td><td>$\overline{Q}(Qo)$</td></tr> </tbody> </table>		Lo	D	\overline{TGo}	CLo	CK	Q(Qo)	X	X	X	H	X	L	H	H	X	L	\uparrow	H	H	L	X	L	\uparrow	L	L	X	H	L	\uparrow	$Q(Qo)$	L	X	L	L	\uparrow	$\overline{Q}(Qo)$
Lo	D	\overline{TGo}	CLo	CK	Q(Qo)																																		
X	X	X	H	X	L																																		
H	H	X	L	\uparrow	H																																		
H	L	X	L	\uparrow	L																																		
L	X	H	L	\uparrow	$Q(Qo)$																																		
L	X	L	L	\uparrow	$\overline{Q}(Qo)$																																		
																																							
TTL Equivalent Circuit 		Definition of Parameters 																																					
AV-C43-E2		C43	Sheet 2/3																																				

Fujitsu CMOS Gate Array Unit Cell Specification							"AV Version
C43							
Function Table							
Inputs						Outputs (QA - QD)	
CL	L	D	EN	CI	CK		
L	X	X	X	X	X	L	
H	L	H	X	X	↑	H	
H	L	L	X	X	↑	L	
H	H	X	X	L	X	No Counting	
H	H	X	L	X	X	No Counting	
H	H	X	H	H	↑	Count up	

Note: The CO output produces a high level output data when the counter overflows.

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version																																				
FT1 (Flip-Flop for COUNTER -- NOT UNIT CELL)																																					
Symbol 	Function Table <table border="1"> <thead> <tr> <th>Lo</th> <th>D</th> <th>TGo</th> <th>CLo</th> <th>CKo</th> <th>Q(Qo)</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>X</td> <td>X</td> <td>H</td> <td>↑</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>X</td> <td>L</td> <td>↑</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>X</td> <td>L</td> <td>↑</td> <td>L</td> </tr> <tr> <td>L</td> <td>X</td> <td>H</td> <td>L</td> <td>↑</td> <td>Q(Qo)</td> </tr> <tr> <td>L</td> <td>X</td> <td>L</td> <td>L</td> <td>↑</td> <td>Q(Qo)</td> </tr> </tbody> </table>	Lo	D	TGo	CLo	CKo	Q(Qo)	L	X	X	H	↑	L	H	H	X	L	↑	H	H	L	X	L	↑	L	L	X	H	L	↑	Q(Qo)	L	X	L	L	↑	Q(Qo)
Lo	D	TGo	CLo	CKo	Q(Qo)																																
L	X	X	H	↑	L																																
H	H	X	L	↑	H																																
H	L	X	L	↑	L																																
L	X	H	L	↑	Q(Qo)																																
L	X	L	L	↑	Q(Qo)																																
Definition of Parameters 																																					
TTL Equivalent Circuit 																																					
AV-C45-E2	C45 Sheet 2/3																																				

Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

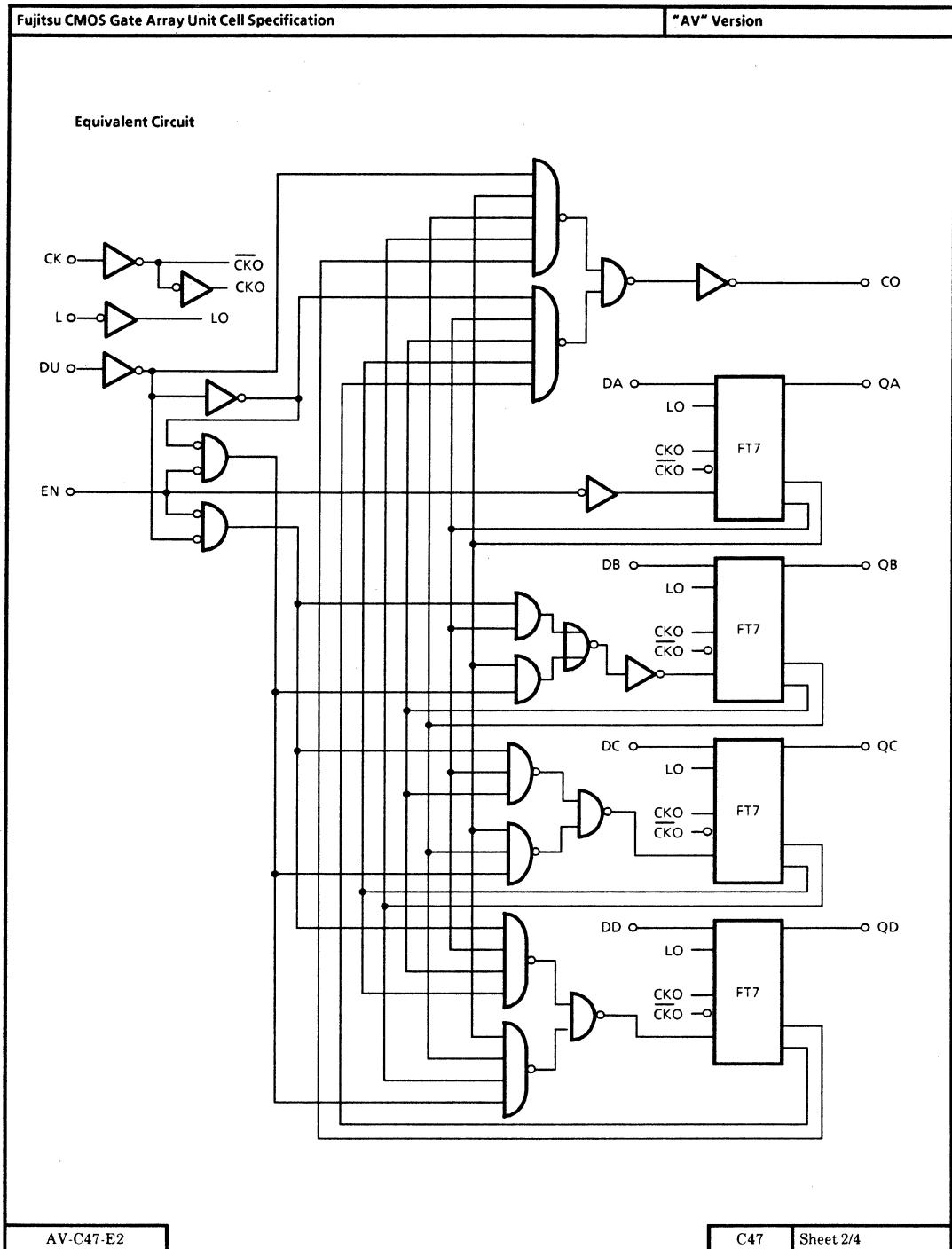
C45**Function Table**

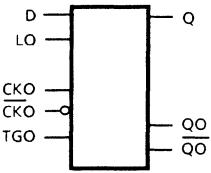
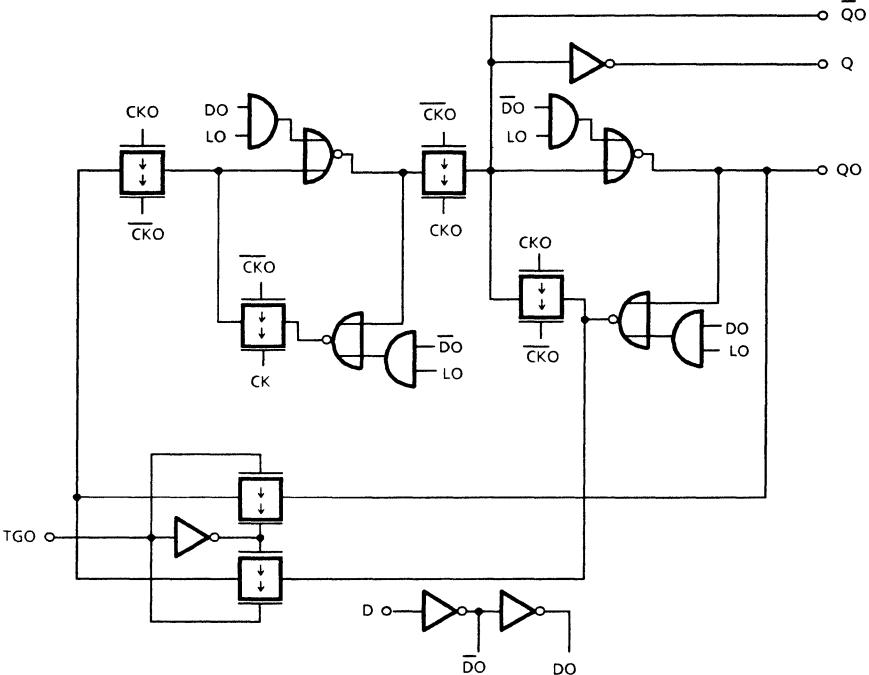
Inputs						Outputs (QA - QD)
CL	L	D	EN	CI	CK	
L	X	X	X	X	↑	L
H	L	H	X	X	↑	H
H	L	L	X	X	↑	L
H	H	X	X	L	X	No Counting
H	H	X	L	X	X	No Counting
H	H	X	H	H	↑	Count up

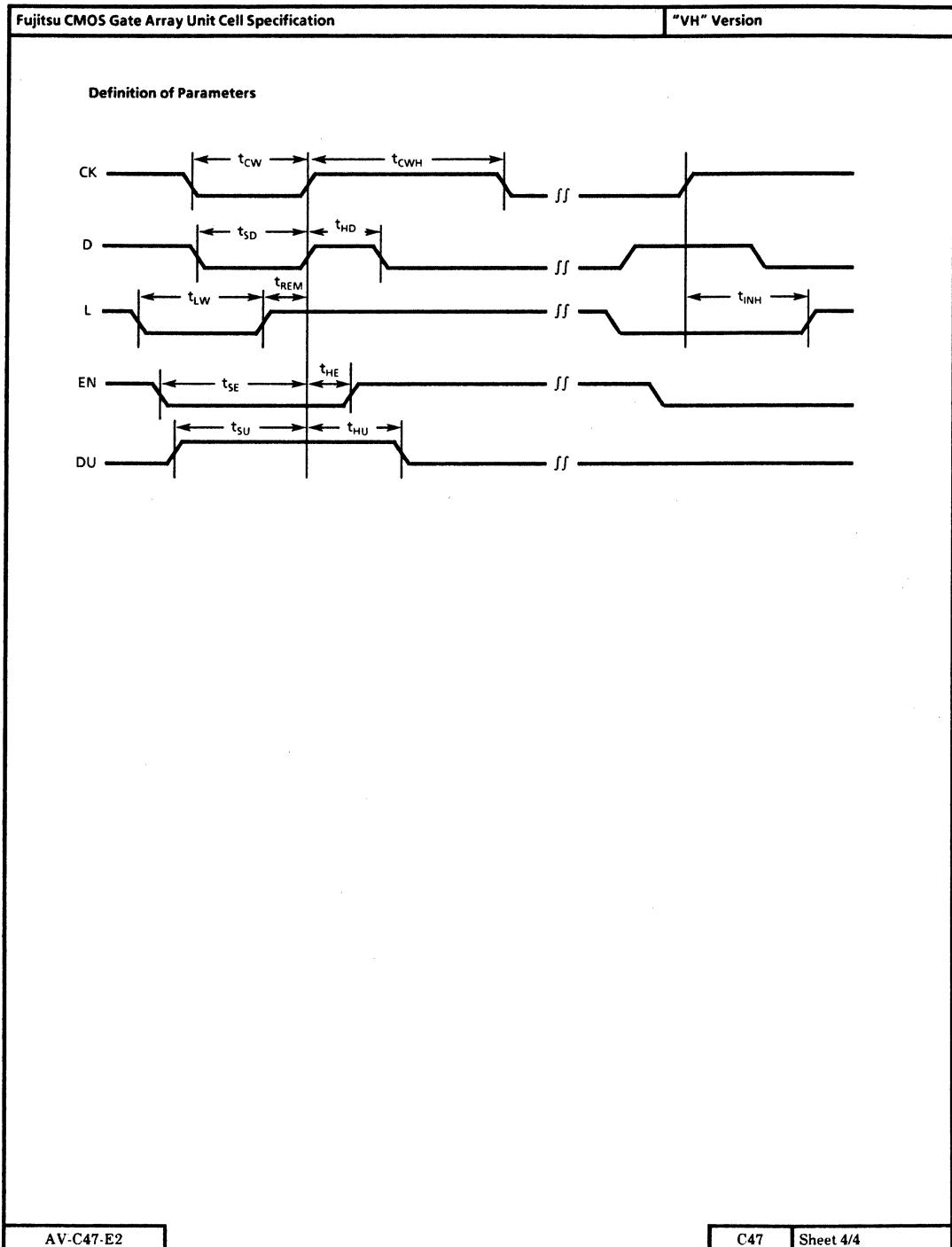
Note: The CO output produces a high level output data when the counter overflows.

3

Cell Name	Function					Number of BC* see note																																				
C47	4-bit Binary Synchronous Up/Down Counter					68																																				
Cell Symbol		Propagation Delay Parameters				Path																																				
		t_{up}		t_{dn}																																						
		t_0	K_{CL}	t_0	K_{CL}																																					
		6.82 9.65 4.96 6.07	0.25 0.25 0.25 0.25	8.52 9.41 4.43 5.76	0.14 0.14 0.14 0.14	$CK \rightarrow Q$ $CK \rightarrow CO$ $L \rightarrow Q$ $DU \rightarrow CO$																																				
		Parameter																																								
		Clock Pulse Width	t_{CPW}		10	ns																																				
		Load Pulse Width	t_{LPW}		5	ns																																				
		Data Set Up Time (L)	t_{SD}		7	ns																																				
		Data Hold Time (L)	t_{HD}		3	ns																																				
		EN Set Up Time (CK)	t_{SE}		9	ns																																				
		EN Hold Time (CK)	t_{HE}		3	ns																																				
		DU Set Up Time (CK)	t_{SU}		11	ns																																				
		DU Hold Time (CK)	t_{HU}		2	ns																																				
		Clear Release Time	t_{REM}		3	ns																																				
		Clear Hold Time	t_{DH}		8	ns																																				
		Clock Pause Time	t_{CPH}		10	ns																																				
Input Loading Factor		Pin Name																																								
1 ℓu		D CK, DU																																								
1 ℓu		L																																								
2 ℓu		EN																																								
3 ℓu																																										
Output Driving Factor		Pin Name																																								
18 ℓu		Any Output																																								
Function Table																																										
Inputs					TTL Equivalent Circuit																																					
<table border="1"> <thead> <tr> <th>DA\cupDD</th> <th>L</th> <th>EN</th> <th>DU</th> <th>CK</th> <th>Outputs (QA\cupQD)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>L</td> <td>X</td> <td>X</td> <td>X</td> <td>H</td> </tr> <tr> <td>0</td> <td>L</td> <td>X</td> <td>X</td> <td>X</td> <td>L</td> </tr> <tr> <td>X</td> <td>H</td> <td>H</td> <td>X</td> <td>↑</td> <td>No Counting</td> </tr> <tr> <td>X</td> <td>H</td> <td>L</td> <td>L</td> <td>↑</td> <td>Count Up</td> </tr> <tr> <td>X</td> <td>H</td> <td>L</td> <td>H</td> <td>↑</td> <td>Count Down</td> </tr> </tbody> </table>					DA \cup DD	L	EN	DU	CK	Outputs (QA \cup QD)	1	L	X	X	X	H	0	L	X	X	X	L	X	H	H	X	↑	No Counting	X	H	L	L	↑	Count Up	X	H	L	H	↑	Count Down		
DA \cup DD	L	EN	DU	CK	Outputs (QA \cup QD)																																					
1	L	X	X	X	H																																					
0	L	X	X	X	L																																					
X	H	H	X	↑	No Counting																																					
X	H	L	L	↑	Count Up																																					
X	H	L	H	↑	Count Down																																					
<p>Note: The CO output produces a low level output pulse when the counter overflows or underflows.</p>					<p>74LS191 MAX/MIN 74504 74LS04</p>																																					
<p>Note*: C47 is not available for C350AVB or C540AVB.</p>																																										
AV-C47-E2					C47	Sheet 1/4																																				



Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version																																				
FT7 (Flip-Flop for Counter) (not Unit Cell)																																					
Symbol	Function Table																																				
	<table border="1"> <thead> <tr> <th colspan="4">Inputs</th> <th colspan="2">Outputs</th> </tr> <tr> <th>LO</th> <th>D</th> <th>TGO</th> <th>CKO</th> <th>QO(Q)</th> <th>$\bar{Q}O$</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>X</td> <td>X</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>X</td> <td>X</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>X</td> <td>L</td> <td>↑</td> <td>Q_{n-1}</td> <td>Q_{n-1}</td> </tr> <tr> <td>L</td> <td>X</td> <td>H</td> <td>↑</td> <td>Q_{n-1}</td> <td>Q_{n-1}</td> </tr> </tbody> </table>	Inputs				Outputs		LO	D	TGO	CKO	QO(Q)	$\bar{Q}O$	H	H	X	X	H	L	H	L	X	X	L	H	L	X	L	↑	Q_{n-1}	Q_{n-1}	L	X	H	↑	Q_{n-1}	Q_{n-1}
Inputs				Outputs																																	
LO	D	TGO	CKO	QO(Q)	$\bar{Q}O$																																
H	H	X	X	H	L																																
H	L	X	X	L	H																																
L	X	L	↑	Q_{n-1}	Q_{n-1}																																
L	X	H	↑	Q_{n-1}	Q_{n-1}																																
																																					



Adder Family

Page	Unit Cell Name	Function	Basic Cells
3-195	A1N	1-bit Full Adder	8
3-197	A2N	2-bit Full Adder	16
3-199	A4H	4-bit Full Adder	50

3

Cell Name	Function	Propagation Delay Parameters				Number of BC																																									
A1N	1-bit Full Adder	t_{up}				8																																									
Cell Symbol		t_o	K_{CL}	t_o	K_{CL}	Path																																									
		2.03 5.23 1.75 1.85	0.61 0.61 0.54 0.54	1.36 2.96 1.33 2.13	0.26 0.26 0.24 0.24																																										
						CI → S																																									
						A,B → S																																									
						CI → CO																																									
						A,B → CO																																									
Input Loading Factor	Pin Name	Parameter	Symbol	MIN	TYP	MAX	UNIT																																								
2 ℓu	A,B,CI																																														
Output Driving Factor	Pin Name																																														
10 ℓu	S,CO																																														
TTL Equivalent Circuit				Function Table																																											
				<table border="1"> <thead> <tr> <th colspan="3">Inputs</th> <th colspan="2">Outputs</th> </tr> <tr> <th>A</th> <th>B</th> <th>CI</th> <th>S</th> <th>CO</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>L</td> <td>H</td> </tr> </tbody> </table>				Inputs			Outputs		A	B	CI	S	CO	L	L	L	L	L	H	L	H	H	L	L	H	H	L	L	H	L	L	H	L	L	H	H	H	L	H	H	H	L	H
Inputs			Outputs																																												
A	B	CI	S	CO																																											
L	L	L	L	L																																											
H	L	H	H	L																																											
L	H	H	L	L																																											
H	L	L	H	L																																											
L	H	H	H	L																																											
H	H	H	L	H																																											

3

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Equivalent Circuit	
AV-A1N-E1	A1N Sheet 2/2

Cell Name	Function	Propagation Delay Parameters				Number of BC
A2N	2-bit Full Adder					16
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}	t_{dn}	t_o	K_{CL}	
B2		4.93 5.23 4.65 4.75	3.06 2.96 3.03 3.83	0.61 0.61 0.54 0.54	0.26 0.26 0.24 0.24	CI \rightarrow S1,S2 A,B \rightarrow S1,S2 CI \rightarrow CO A,B \rightarrow CO
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX
2 ℓu						
Output Driving Factor		Pin Name				
10 ℓu		A,B,CI				
		S,CO				
TTL Equivalent Circuit						
7482						
AV-A2N-E1						
				A2N	Sheet 1/2	

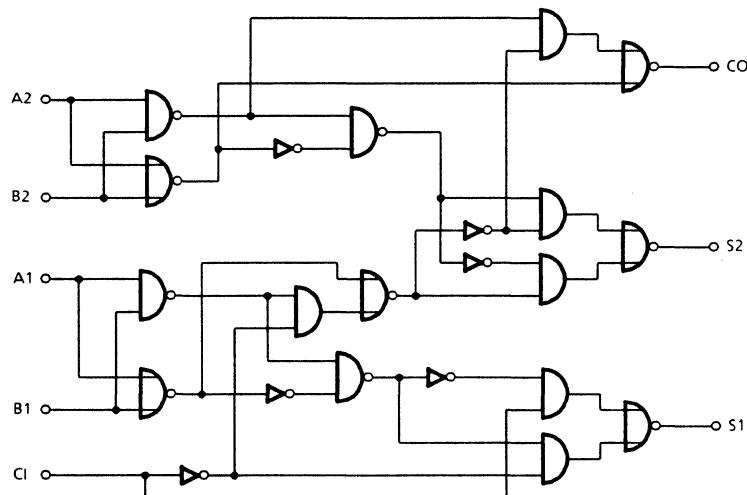
Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

Function Table

Inputs				Outputs					
				CI=L			CI=H		
A1	B1	A2	B2	S1	S2	\bar{CO}	S1	S2	\bar{CO}
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	H	L	H
L	H	H	H	H	H	L	H	H	H
H	H	H	H	L	H	H	H	H	H

Equivalent Circuit



3

Fujitsu CMOS Gate Array Unit Cell Specification

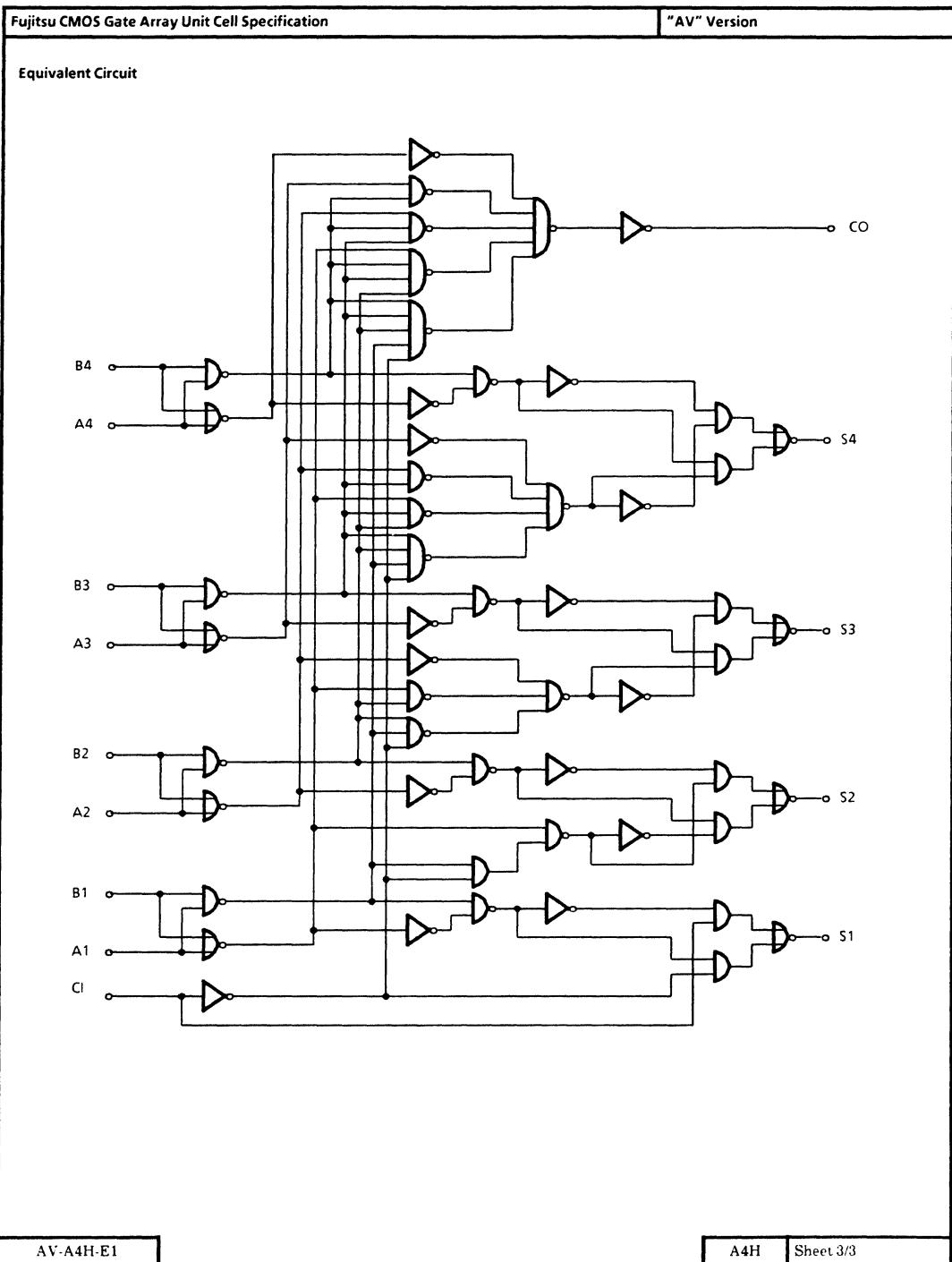
"AV" Version

Function Table

Inputs					Outputs							
					$C_1 = L$		$C_2 = L$		$C_1 = H$		$C_2 = H$	
A1 A3	B1 B3	A2 A4	B2 B4	S1 S3	S2 S4	C2 CO	S1 S3	S2 S4	C2 CO	S1 S3	S2 S4	C2 CO
L	L	L	L	L	L	L	H	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	H	L	L
L	H	L	L	H	L	L	L	H	L	H	L	L
H	H	L	L	L	H	L	H	H	H	H	L	L
L	L	H	L	L	H	L	H	H	H	H	L	L
H	L	H	L	H	H	L	L	L	L	L	H	
L	H	H	L	H	H	L	L	L	L	L	H	
H	H	H	L	L	L	H	H	L	H	L	H	
L	L	L	H	L	H	L	H	H	H	H	L	L
H	L	L	H	H	H	L	L	L	L	H	L	H
L	H	L	H	H	H	L	L	L	L	H	L	H
H	H	L	H	L	L	H	H	L	H	L	H	H
L	L	H	H	L	L	H	H	H	L	H	L	H
H	L	H	H	H	L	H	L	H	L	H	H	
L	H	H	H	H	L	H	L	H	L	H	H	
H	H	H	H	L	H	H	H	H	H	H	H	

Note:

Input conditions at A1, B1, B2 and C1 are used to determine outputs S1 and S2 and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4, and CO.



3

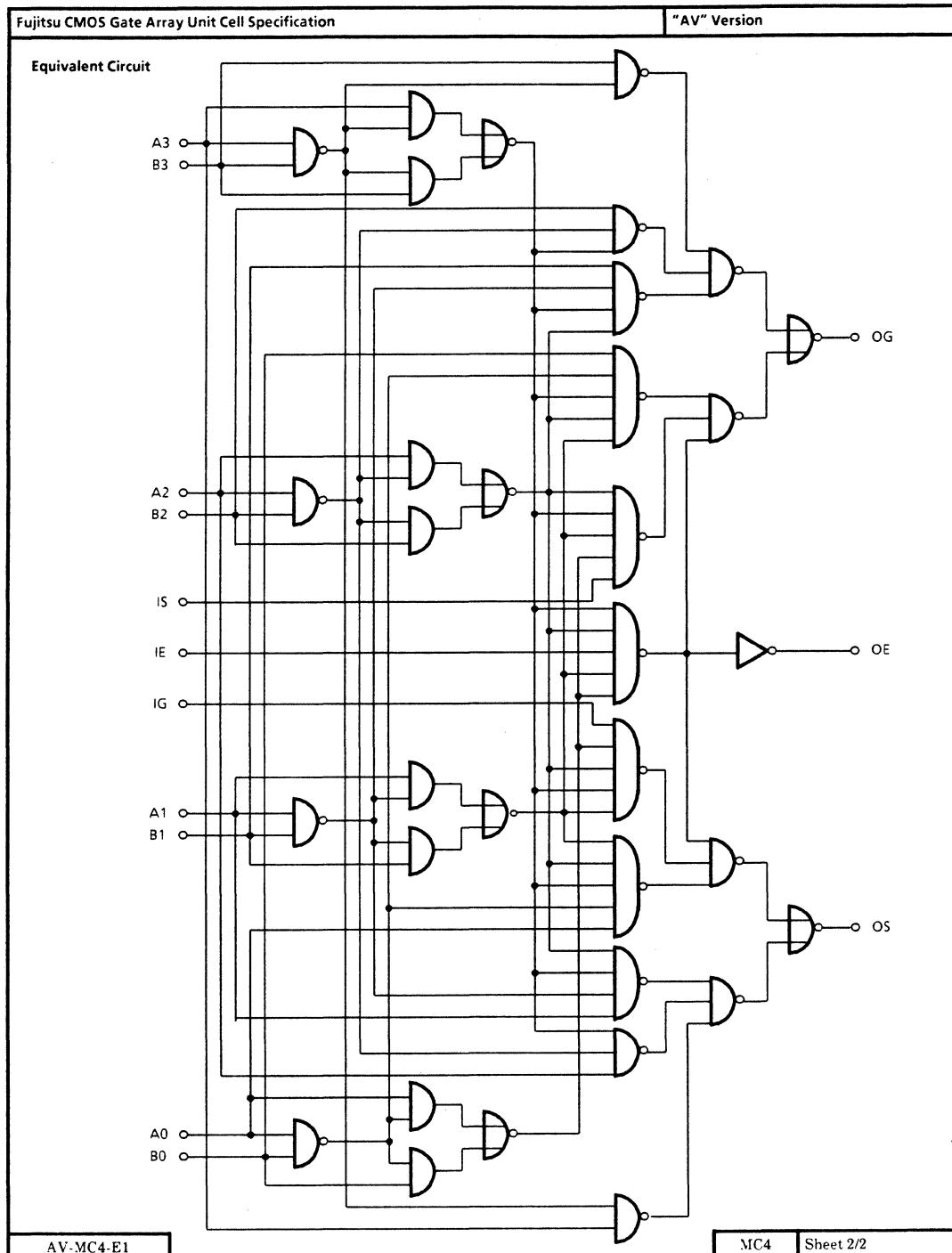
Miscellaneous Functions

Page	Unit Cell Name	Function	Basic Cells
3-205	MC4	4-bit Magnitude Comparator	42
3-207	DE2	2:4 Decoder	5
3-208	DE3	3:8 Decoder	15
3-209	SM1	Schmitt Trigger Input	8
3-211	SM2	Schmitt Trigger Input	7
3-213	BD3	Buffer (Delay Cell)	5
3-214	BD5	Buffer (Delay Cell)	9
3-215	BD6	Buffer (Delay Cell)	17

3

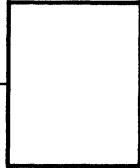
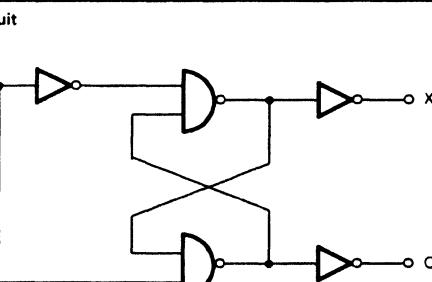
Cell Name	Function					Number of BC			
MC4	4-bit Magnitude Comparator					42			
Cell Symbol		Propagation Delay Parameters				Path			
		t_{up}	t_{dn}	t_o	K_{CL}				
B3 A3 B2 A2 B1 A1 B0 A0	IG IE IS	9.25 8.77 4.75 4.67 6.07	0.25 0.46 0.25 0.46 0.46	8.70 8.33 4.60 3.83 5.53	0.14 0.13 0.14 0.13 0.13	A or B → OE A or B → OG,OS IE → OE IS → OG, IG → OS IE → OS or OG			
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX	UNIT		
3 ℓu 1 ℓu	A,B IS,IE,IG								
Output Driving Factor		Pin Name							
18 ℓu 10 ℓu	OE OG,OS								
Function Table 74LS85 Compatible		Comparing Inputs		Cascading Inputs		Outputs			
A3, B3	A2, B2	A1, B1	A0, B0	IG (A > B)	IS (A < B)	IE (A = B)	OG (A > B)	OS (A < B)	OE (A = B)
A3 > B3 A3 < B3	X X	X X	X X	X X	X X	X X	H L	L H	L L
A3 = B3 A3 = B3	A2 > B2 A2 < B2	X X	X X	X X	X X	X X	H L	L H	L L
A3 = B3 A3 = B3	A2 = B2 A2 = B2	A1 > B1 A1 < B1	X X	X X	X X	X X	H L	L H	L L
A3 = B3 A3 = B3	A2 = B2 A2 = B2	A1 = B1 A1 = B1	A0 > B0 A0 < B0	X	X	X	H L	L H	L L
A3 = B3 A3 = B3	A2 = B2 A2 = B2	A1 = B1 A1 = B1	A0 > B0 A0 = B0	X	X	H	L H	L L	H L
A3 = B3 A3 = B3	A2 = B2 A2 = B2	A1 = B1 A1 = B1	A0 = B0 A0 = B0	H	H	L	L H	L L	L L
A3 = B3 A3 = B3	A2 = B2 A2 = B2	A1 = B1 A1 = B1	A0 = B0 A0 = B0	L	L	L	H L	H L	L L

3



3

Cell Name	Function	Number of BC								
DE3	3 : 8 Decoder	15								
Cell Symbol	Propagation Delay Parameters									
	t_{up}	t_{dn}	Path							
	t_o	K_{CL}	t_o	K_{CL}						
	3.68	0.27	3.29	0.28	A,B,C → X					
	Equivalent Circuit									
Input Loading Factor	Pin Name									
1 ℓ_u	A,B,C									
Output Driving Factor	Pin Name									
14 ℓ_u	X									
Function Table										
Inputs		Outputs								
A	B	C	X0	X1	X2	X3	X4	X5	X6	X7
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

Cell Name	Function	Propagation Delay Parameters				Number of BC								
SM1	Schmitt-Trigger Input					8								
Cell Symbol	Propagation Delay Parameters													
	t_{up}		t_{dn}		Path $D \rightarrow Q$ $D \rightarrow XQ$									
	t_o	K_{CL}	t_o	K_{CL}										
	7.70 12.7	0.16 0.16	10.6 7.40	0.10 0.11										
Parameter	Symbol	MIN	TYP	MAX	UNIT									
Positive-going Threshold Voltage*	$V_T +$	2.5	3.3	4.0	V									
Negative-going Threshold Voltage*	$V_T -$	0.7	1.4	2.0	V									
Hysteresis*	$V_T^+ - V_T^-$	1.1	1.9	2.7	V									
Data Pulse Width (Positive Pulse, Negative Pulse)	t_{DW}			25**										
Input Loading Factor	Pin Name													
Output Driving Factor	Pin Name													
18 μ u	Q,XQ													
Equivalent Circuit	Function Table													
	<table border="1"> <thead> <tr> <th>Input</th><th>Outputs</th></tr> </thead> <tbody> <tr> <td>D</td><td>Q XQ</td></tr> <tr> <td>L</td><td>L H</td></tr> <tr> <td>H</td><td>H L</td></tr> </tbody> </table>						Input	Outputs	D	Q XQ	L	L H	H	H L
Input	Outputs													
D	Q XQ													
L	L H													
H	H L													
Note: SM1 must not be used with SM2 in one chip. Also, the rule of usage on the next page should be observed.														

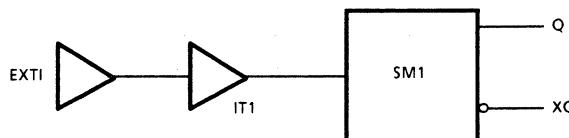
Note: SM1 must not be used with SM2 in one chip.
Also, the rule of usage on the next page should be observed.

Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

Rule of Usage

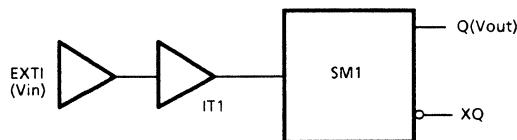
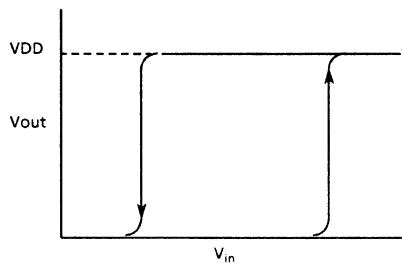
SM1 must be used with IT1, I/O cell for only protection circuit, as shown below.
 IT1 is available only for SM1.



AC Spec Condition

$V_{IL} = 0.6\text{ V}$, $V_{IH} = 4.0\text{ V}$
 $t_s = t_f = 10\text{ ns}$
 $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

Hysteresis Characteristics



Note*: The specification is expressed as follows:

Values of V_{T+} , V_{T-} and $V_{T+} - V_{T-}$ are for reference only.

$$V_{IH(\min)} = V_{DD} \times 0.8\text{ (V)}$$

$$V_{IL(\max)} = 0.6\text{ (V)}$$

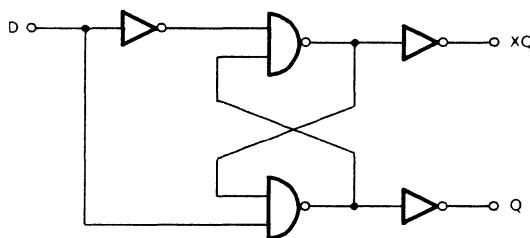
($V_{DD} = 5\text{V} \pm 5\%$, $T_A = 0\text{--}70^\circ\text{C}$)

*minimum value with typical operation conditions.

Cell Name	Function	Propagation Delay Parameters				Number of BC	
Cell Symbol		Propagation Delay Parameters					
		t_{up}	t_{dn}				Path
		t_o	K_{CL}	t_o	K_{CL}		
		7.30 13.8	0.16 0.14	11.6 6.50	0.13 0.07		$D \rightarrow Q$ $D \rightarrow XQ$
Input Loading Factor	Pin Name						
5 ℓu	D						
Output Driving Factor	Pin Name						
18 ℓu	Q,XQ						

3

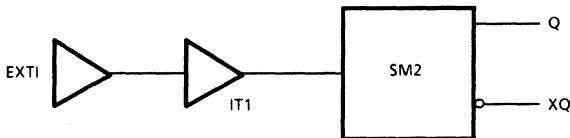
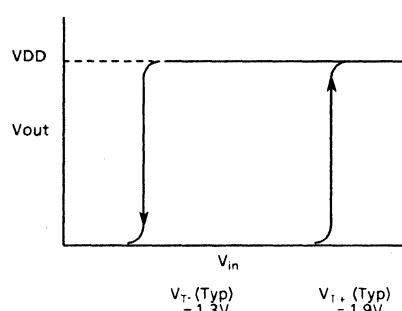
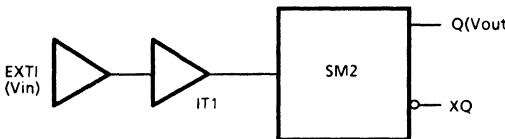
Equivalent Circuit



Function Table

Input	Outputs	
D	Q	XQ
L	L	H
H	H	L

Note: SM2 must not be used with SM1 in one chip.
Also, the rule of usage on the next page should be observed.

Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
Rule of Usage	
SM2 must be used with IT1, I/O cell for only protection circuit, as shown below. IT1 is available only for Schmitt-Trigger Input.	
	
AC Spec Condition	
$V_{IL} = 0.6 \text{ V}$, $V_{IH} = 2.6 \text{ V}$ $t_f = t_r = 10 \text{ ns}$ $V_{DD} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$	
Hysteresis Characteristics	
	
	
<p>Note*: The specification is expressed as follows:</p> <p>Values of V_{T-}, V_{T+} and $V_{T+} - V_{T-}$ are for reference only.</p> <p>$V_{IH(\min)} = V_{DD} \times 0.5 \text{ (V)}$</p> <p>$V_{IL(\max)} = 0.8 \text{ (V)}$</p> <p>($V_{DD} = 5 \text{ V} \pm 5\%$, $T_A = 0 \sim 70^\circ\text{C}$)</p>	
<p>* minimum value with typical operation conditions.</p>	
AV-SM2-E2	SM2
Sheet 2/2	

3

Cell Name	Function					Number of BC				
BD5	Buffer (Delay Cell)					9				
Cell Symbol		Propagation Delay Parameters				Path				
		t_{up}		t_{dn}						
		t_o	K_{CL}	t_o	K_{CL}					
		22.18	0.16	18.78	0.10	A → X				
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX				
						UNIT				
Output Driving Factor		Pin Name								
1 ℓu		A								
Output Driving Factor		Pin Name								
18 ℓu		X								
TTL Equivalent Circuit (Logic Function Equivalent only. The propagation delay time is not equivalent.)										
 74S04 74LS04										
AV-BD5-E1			BD5 Sheet 1/1							

Cell Name	Function	Propagation Delay Parameters				Number of BC
BD6	Buffer (Delay Cell)					17
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}	K_{CL}	t_{dn}	K_{CL}	
		43.10	0.16	32.60	0.10	A → X
Input Loading Factor		Parameter	Symbol	MIN	TYP	MAX
Output Driving Factor		Pin Name				
1 ℓu		A				
TTL Equivalent Circuit (Logic Function Equivalent only. The propagation delay time is not equivalent.)						
		74S04 74LS04	74S04 74LS04			

3

3

I/O Cell Family

Page	Unit Cell Name	Function
Input Buffers		
3-219	I2B	Input Buffer (True)
3-220	I2BU	I2B with Pull-up Resistance
3-221	I2BD	I2B with Pull-down Resistance
3-222	ILB	Clock Input Buffer (True)
3-223	ILBU	ILB with Pull-up Resistance
3-224	ILBD	ILB with Pull-down Resistance
3-225	IKB	Clock Input Buffer (Inverter)
3-226	IKBU	IKB with Pull-up Resistance
3-227	IKBD	IKB with Pull-down Resistance
3-228	I2C	CMOS Interface Input Buffer
3-229	I2CU	I2C with Pull-up Resistance
3-230	I2CD	I2C with Pull-down Resistance
3-231	IT1	Input Buffer for Schmitt Trigger Input
3-232	IT1U	IT1 with Pull-up Resistance
3-233	IT1D	IT1 with Pull-down Resistance
Output Buffers		
3-234	O2B	Output Buffer (True)
3-235	O2L	Power Output Buffer (True)
3-236	O4T	3-state Output Buffer (True)
3-237	O4W	Power 3-state Output Buffer (True)

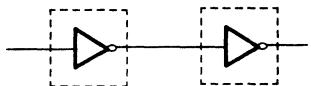
I/O Cell Family (Continued)

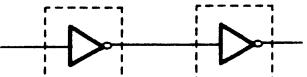
3-state Output and Input Buffers

3-238	H6T	3-state Output and Input Buffer (True)
3-239	H6TU	H6T with Pull-up Resistance
3-240	H6TD	H6T with Pull-down Resistance
3-241	H6W	Power 3-state Output and Input Buffer (True)
3-242	H6WU	H6W with Pull-up Resistance
3-243	H6WD	H6W with Pull-down Resistance
3-244	H6C	3-state Output and CMOS Interface Input Buffer (True)
3-245	H6CU	H6C with Pull-up Resistance
3-246	H6CD	H6C with Pull-down Resistance
3-247	H6E	Power 3-state Output and CMOS Interface Input Buffer (True)
3-248	H6EU	H6E with Pull-up Resistance
3-249	H6ED	H6E with Pull-down Resistance
3-250	H6D	3-state Input and Output Buffer for SM1, SM2
3-251	H6DU	H6D with Pull-up Resistance
3-252	H6DD	H6D with Pull-down Resistance

High-Drive Buffers

3-253	O2L2	O2L with 20mA Drive
3-254	O4W2	O4W with 20mA Drive
3-255	H6W2	H6W with 20mA Drive
3-256	H6W1	H6WU with 20mA Drive
3-257	H6W0	H6WD with 20mA Drive
3-258	H6E2	H6E with 20mA Drive
3-259	H6E1	H6EU with 20mA Drive
3-260	H6E0	H6ED with 20mA Drive
3-261	O2B2	O2B with 10mA Drive
3-262	O2B3	O2B with 15mA Drive
3-263	O4T2	O4T with 10mA Drive
3-264	O4T3	O4T with 15mA Drive
3-265	H6T2	H6T with 10mA Drive
3-266	H6T3	H6T with 15mA Drive
3-267	H6C2	H6C with 10mA Drive
3-268	H6C3	H6C with 15mA Drive
3-269	O1T	Crystal Oscillator CMOS Interface Input Buffer with Schmitt Trigger
3-270	OT1	Output Buffer with Protection Circuit Only

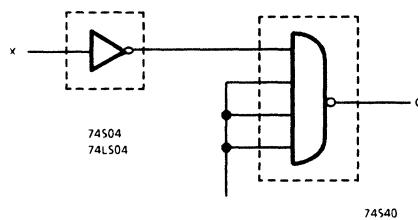
Cell Name	Function					Number of BC					
I2BU	Input Buffer with Pull Up Resistance (True)					-					
Cell Symbol		Propagation Delay Parameters				Path					
		t_{up}	t_{dn}								
		t_0	K_{CL}	t_0	K_{CL}						
		2.06	0.06	3.08	0.08	X → IN					
		Parameter	Symbol	MIN	TYP	MAX					
						UNIT					
Input Loading Factor		Pin Name									
Output Driving Factor		Pin Name									
36 ℓ_u		IN									
TTL Equivalent Circuit											
											
74504 74LS04		74504 74LS04									
Note: This cell is available for AVB Series only.											
AV-I2BU-E1		I2BU		Sheet 1/1							

Cell Name	Function							Number of BC							
I2BD	Input Buffer with Pull Down Resistance (True)							-							
Cell Symbol	Propagation Delay Parameters						Path								
	t_{up}		t_{dn}												
	t_0	K_{CL}	t_0	K_{CL}											
	2.06	0.06	3.08	0.08	X → IN										
	Parameter	Symbol	MIN	TYP	MAX	UNIT									
Input Loading Factor	Pin Name														
Output Driving Factor	Pin Name														
36 μ A	IN														
TTL Equivalent Circuit															
 74S04 74S04 74LS04 74LS04															
Note: This cell is available for AVB Series only.															
AV-I2BD-E1							I2BD	Sheet 1/1							

Cell Name	Function	Propagation Delay Parameters				Number of BC	
Cell Symbol		Propagation Delay Parameters				Path	
		t_{up}	t_{dn}				
		t_0	K _{CL}	t_0	K _{CL}		
	x	3.14	0.02	5.30	0.01	X → CI	
Input Loading Factor	Pin Name						
Output Driving Factor	Pin Name						
360 f <u>A</u>	CI						

3

TTL Equivalent Circuit



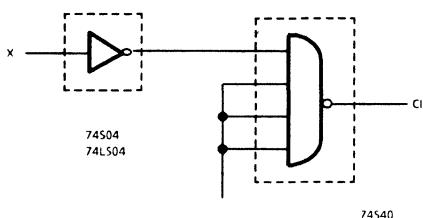
AV-II.B-E1

JL-B Sheet 1/1

Cell Name	Function	Propagation Delay Parameters				Number of BC
Cell Symbol		t_{up}	t_{dn}			Path
		t_o	K_{CL}	t_o	K_{CL}	
	x ————— CI	3.14	0.02	5.30	0.01	X → CI
Input Loading Factor	Pin Name					
Output Driving Factor	Pin Name					
360 f <u>u</u>	CI					

3

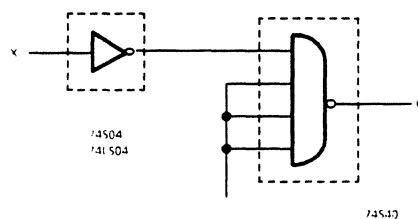
TTL Equivalent Circuit



Note: This cell is available for AVB Series only.

Cell Name	Function	Propagation Delay Parameters				Number of BC	
Cell Symbol		Propagation Delay Parameters				Path	
		t_{up}	t_{dn}				
		t_0	K _{CL}	t_0	K _{CL}		
	x ————— CI	3.14	0.02	5.30	0.01	X → CI	
Input Loading Factor	Pin Name						
Output Driving Factor	Pin Name						
360 f <u>A</u>	CI						

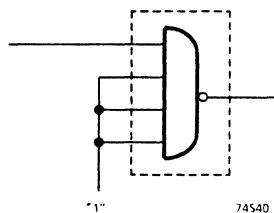
TTL Equivalent Circuit



Note: This cell is available for AVB Series only.

3

TTI Equivalent Circuit



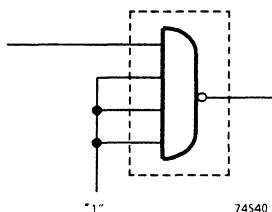
Note: This cell is available for AVB Series only.

Note: This cell is available for AVB Series only.

Cell Name	Function	Propagation Delay Parameters				Number of BC
Cell Symbol		Propagation Delay Parameters				Path
		t_{up}	t_{dn}	Path		
		t_o	K_{CL}	t_o	K_{CL}	
		4.91	0.02	3.03	0.01	X → Cl
Input Loading Factor	Pin Name					
Output Driving Factor	Pin Name					
360 f <u>u</u>	Cl					

3

TTL Equivalent Circuit

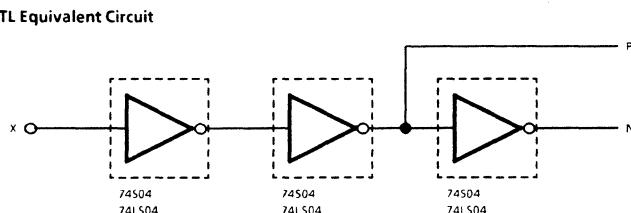


Note: This cell is available for AVB Series only.

Cell Name	Function	Propagation Delay Parameters				Number of BC
Cell Symbol		t_{up}		t_{dn}		Path
		t_o	K _{CL}	t_o	K _{CL}	
		2.29 $t_{dp}(PI)^*$ + 0.48	0.08 0.13	2.41 $t_{dp}(PI)^*$ + 0.35	0.05 0.07	X → PI X → NI
Parameter	Symbol	MIN	TYP	MAX	UNIT	
High-level Input Voltage	V _{IH}	V _{DD} × 0.7				V
Low-level Input Voltage	V _{IL}			V _{DD} × 0.3		V
Input Loading Factor	Pin Name					
Output Driving Factor	Pin Name					
36 ℓ u 18 ℓ u	PI NI					
TTL Equivalent Circuit						
Function Table						
INPUT	OUTPUTS					
X	PI	NI				
L	L	H				
H	H	L				

NOTE*: $t_{dn}(\text{PI}) = t_0(\text{dn}) + K_{CL}(\text{dn}) \times C_L(f_u)$
 $t_{up}(\text{PI}) = t_0(\text{up}) + K_{CL}(\text{up}) \times C_L(f_u)$

Cell Name	Function	Number of BC																	
I2CU	CMOS Interface Input Buffer with Pull Up Resistance (True & Invert)																		
Cell Symbol		Propagation Delay Parameters																	
		t_{up}		t_{dn}		Path													
		t_0	K_{CL}	t_0	K_{CL}														
		2.29 $t_{dn}(\text{PI})^*$ +0.48	0.08 0.13	2.41 $t_{up}(\text{PI})^*$ +0.35	0.05 0.07	X → CI X → NI													
Parameter		Symbol	MIN	TYP	MAX	UNIT													
Input High Voltage		V_{IH}	$V_{DD} \times 0.7$			V													
Input Low Voltage		V_{IL}			$V_{DD} \times 0.3$	V													
Input Loading Factor		Pin Name																	
Output Driving Factor		Pin Name																	
36 ℓ_u 18 ℓ_u		PI NI																	
TTL Equivalent Circuit																			
Function Table <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>INPUT</th><th colspan="2">OUTPUTS</th></tr> <tr> <td>X</td><td>PI</td><td>NI</td></tr> <tr> <td>L</td><td>L</td><td>H</td></tr> <tr> <td>H</td><td>H</td><td>L</td></tr> </table>								INPUT	OUTPUTS		X	PI	NI	L	L	H	H	H	L
INPUT	OUTPUTS																		
X	PI	NI																	
L	L	H																	
H	H	L																	
<small>NOTE*: $t_{dn}(\text{PI}) = t_0(t_{dn}) + K_{CL}(t_{dn}) \times CL \cdot f_{in}$ $t_{up}(\text{PI}) = t_0(t_{up}) + K_{CL}(t_{up}) \times CL \cdot f_{in}$</small>																			
<small>Note: This cell is available for AVB Series only.</small>																			
AV-I2CU-E1		I2CU		Sheet 1/1															



INPUT	OUTPUTS	
X	P1	N1
L	L	H
H	H	L

NOTE*: $t_{dn}(\text{PI}) = t_0(\text{dn}) + K_{CL}(\text{dn}) \times C_L(\text{fu})$
 $t_{up}(\text{PI}) = t_0(\text{up}) + K_{CL}(\text{up}) \times C_L(\text{fu})$

Note: This cell is available for AVB Series only.

3

Cell Name	Function	Propagation Delay Parameters				Number of BC	
Cell Symbol		Propagation Delay Parameters				Path	
		t_{up}	t_{dn}				
		t_o	K_{CL}	t_o	K_{CL}		
		0	0	0	0	X → IN	
Input Loading Factor	Pin Name						
Output Driving Factor	Pin Name						

Note: IT1U is the input protection circuit only for SM1, SM2.

Note: This cell is available for AVB Series only.

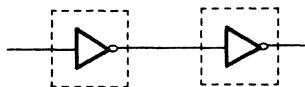
3

Note: 1: The unit of K_{CL} is ns/pF.

2: Output load capacitance of 60pF is used for Fujitsu's logic simulation.

3: The parameters in parentheses are the values applied to the simulation.

TTL Equivalent Circuit



74504

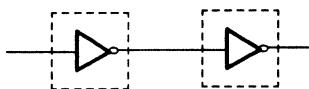
14504
74LS04

Note: This cell is available for AVB Series only.

Cell Name	Function					Number of BC		
O2L	Power Output Buffer (True)					-		
Cell Symbol		Propagation Delay Parameters				Path		
		t_{up}		t_{dn}				
		t_0	K_{CL}	t_0	K_{CL}	OT → X		
		2.20 (4.60)	0.04	4.30 (6.70)	0.04			
		Parameter	Symbol	MIN	TYP	MAX	UNIT	
Input Loading Factor		Pin Name	OT					
2 ℓu								
Output Driving Factor								

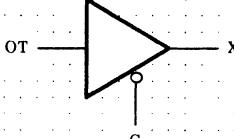
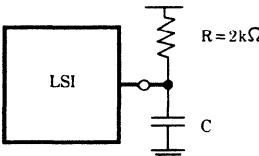
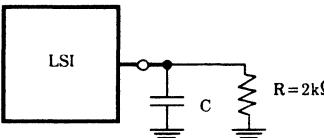
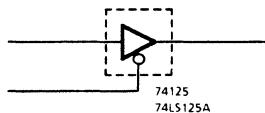
- Note:
- 1: The unit of K_{CL} is ns/pF.
 - 2: Output load capacitance of 60pF is used for Fujitsu's logic simulation.
 - 3: The parameters in parentheses are the values applied to the simulation.
 - 4: $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0\text{--}70^\circ C$, $V_{DD} = 5V \pm 5\%$

TTL Equivalent Circuit

74504
74LS0474504
74LS04

Note: This cell is available for AVB Series only.

Cell Name	Function	Number of BC							
O4T	Tri-State Output Buffer (True)	-							
Cell Symbol		Propagation Delay Parameters							
		t_{up}				t_{dn}			
		t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}	Path	
		2.46 (7.66)	0.08	6.47 (11.67)	0.08	OT → X			
		$L \rightarrow Z$		$Z \rightarrow L$		$H \rightarrow Z$		$Z \rightarrow H$	
		t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}
		1.60 (24.95)	*	5.72 (10.92)	0.08	2.85 (24.95)	*	3.55 (10.92)	0.08
* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.									
(a) Measurement of t_{pd} at LZ and ZL									
(b) Measurement of t_{pdi} at HZ and ZH									
<p>Note:</p> <ol style="list-style-type: none"> The unit of K_{CL} is ns/pF. Output load capacitance of 65pF is used for Fujitsu's logic simulation. The parameters in parentheses are the values applied to the simulation. 									
TTL Equivalent Circuit									
AV-O4T-E1			O4T			Sheet 1/1			

Cell Name	Function	Number of BC																															
O4W	Power Tri-State Output Buffer (True)	-																															
Cell Symbol	Propagation Delay Parameters																																
		Path																															
<table border="1"> <thead> <tr> <th colspan="2">t_{up}</th> <th colspan="2">t_{dn}</th> </tr> <tr> <th>t_o</th> <th>K_{CL}</th> <th>t_o</th> <th>K_{CL}</th> </tr> </thead> <tbody> <tr> <td>2.80 (6.07)</td> <td>0.05</td> <td>6.60 (10.50)</td> <td>0.06</td> </tr> <tr> <td colspan="2">L → Z</td> <td colspan="2">Z → L</td> </tr> <tr> <td colspan="2">H → Z</td> <td colspan="2">Z → H</td> </tr> <tr> <th>t_o</th><th>K_{CL}</th><th>t_o</th><th>K_{CL}</th></tr> <tr> <td>3.00 (31.3)</td><td>*</td><td>7.00 (11.55)</td><td>0.07</td> </tr> <tr> <td>6.70 (31.3)</td><td>*</td><td>3.80 (11.55)</td><td>0.05</td> </tr> </tbody> </table>		t_{up}		t_{dn}		t_o	K_{CL}	t_o	K_{CL}	2.80 (6.07)	0.05	6.60 (10.50)	0.06	L → Z		Z → L		H → Z		Z → H		t_o	K_{CL}	t_o	K_{CL}	3.00 (31.3)	*	7.00 (11.55)	0.07	6.70 (31.3)	*	3.80 (11.55)	0.05
t_{up}		t_{dn}																															
t_o	K_{CL}	t_o	K_{CL}																														
2.80 (6.07)	0.05	6.60 (10.50)	0.06																														
L → Z		Z → L																															
H → Z		Z → H																															
t_o	K_{CL}	t_o	K_{CL}																														
3.00 (31.3)	*	7.00 (11.55)	0.07																														
6.70 (31.3)	*	3.80 (11.55)	0.05																														
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.</p>																																	
																																	
(a) Measurement of t_{pd} at LZ and ZL																																	
																																	
(b) Measurement of t_{pd} at HZ and ZH																																	
<p>Note:</p> <ol style="list-style-type: none"> The unit of K_{CL} is ns/pF. Output load capacitance of 65pF is used for Fujitsu's logic simulation. The parameters in parentheses are the values applied to the simulation. $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $V_{DD} = 5V \pm 5\%$ 																																	
<h4>TTL Equivalent Circuit</h4> 																																	
<p>Note: This cell is available for AVB Series only.</p>																																	
AV-O4W-E1	O4W	Sheet 1/1																															

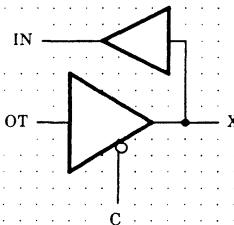
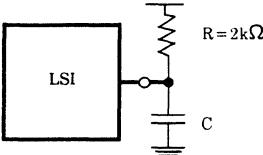
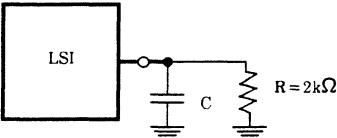
Cell Name	Function					Number of BC						
H6T	Tri-State Output and Input Buffer (True)					-						
Cell Symbol		Propagation Delay Parameters				Path						
		t_{up}		t_{dn}		OT → X						
		t_o	K_{CL}	t_o	K_{CL}							
		2.46 (9.26)		6.47 (13.27)								
		L → Z		Z → L		C → X						
		t_o	K_{CL}	t_o	K_{CL}							
		1.60 (31.75)	*	5.72 (12.52)	0.08							
		H → Z		Z → H		X → IN						
		t_o	K_{CL}	t_o	K_{CL}							
		2.85 (31.75)	*	3.55 (12.52)	0.08							
		t_{up}		t_{dn}								
		t_o	K_{CL}	t_o	K_{CL}							
		2.06	0.06	3.08	0.08							
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.</p>												
Input Loading Factor		Pin Name										
2 ℓu 3 ℓu		OT C										
Output Driving Factor		Pin Name										
36 ℓu		IN										
<p>(a) Measurement of t_{pd} at LZ and ZL</p>												
<p>(b) Measurement of t_{pd} at HZ and ZH</p>												
<p>Note:</p> <ol style="list-style-type: none"> The unit of K_{CL} for paths OT, C to X is ns/pF. Output load capacitance of 85pF is used for Fujitsu's logic simulation. The parameters in parentheses are the values applied to the simulation. 												
		AV-H6T-E1										
				H6T Sheet 1/1								

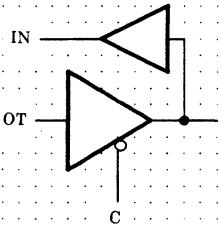
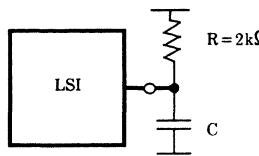
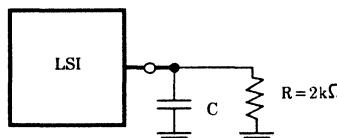
Cell Name	Function					Number of BC						
H6TU	Tri-State Output and Input Buffer with Pull Up Resistance (True)					-						
Cell Symbol		Propagation Delay Parameters										
		t_{up}		t_{dn}		Path OT → X						
		t_o	K_{CL}	t_o	K_{CL}							
		2.46 (9.26)	0.08	6.47 (13.27)	0.08	C → X						
		$L \rightarrow Z$		$Z \rightarrow L$								
		t_o	K_{CL}	t_o	K_{CL}	X → IN						
		1.60 (31.75)	*	5.72 (12.52)	0.08							
		2.85 (31.75)	*	3.55 (12.52)	0.08	X → IN						
		t_{up}		t_{dn}								
		t_o	K_{CL}	t_o	K_{CL}	X → IN						
		2.06	0.06	3.08	0.08							
* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.												
Input Loading Factor												
		(a) Measurement of t_{pd} at LZ and ZL										
Output Driving Factor												
		(b) Measurement of t_{pd} at HZ and ZH										
TTL Equivalent Circuit 												
Note: 1: The unit of K_{CL} for paths OT, C to X is ns/pF. 2: Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3: The parameters in parentheses are the values applied to the simulation.												
Note: This cell is available for AVB Series only.												
AV-H6TU-E1		H6TU			Sheet 1/1							

Cell Name	Function					Number of BC													
H6TD	Tri-State Output and Input Buffer with Pull Down Resistance (True)					-													
Cell Symbol	Propagation Delay Parameters					Path													
	t_{up}		t_{dn}		OT → X														
	t_o	K_{CL}	t_o	K_{CL}		C → X													
2.46 (9.26)		0.08		6.47 (13.27)		X → IN													
$L \rightarrow Z$		$Z \rightarrow L$		$H \rightarrow Z$															
t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}														
1.60 (31.75)	*	5.72 (12.52)	0.08	2.85 (31.75)	*	3.55 (12.52)													
t_{up}		t_{dn}																	
t_o	K_{CL}	t_o	K_{CL}																
2.06	0.06	3.08	0.08																
* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.																			
Input Loading Factor	Pin Name																		
2 ℓ_u 3 ℓ_u	OT C																		
Output Driving Factor	Pin Name																		
36 ℓ_u	IN																		
TTL Equivalent Circuit	<p>(a) Measurement of t_{pd} at LZ and ZL</p> <p>(b) Measurement of t_{pd} at HZ and ZH</p>																		
Note: 1: The unit of K_{CL} for paths OT, C to X is ns/pF. 2: Output load capacitance of 85pF is used for Fujitsu's logic simulation. 3: The parameters in parentheses are the values applied to the simulation.																			
Note: This cell is available for AVB Series only.																			
AV-H6TD-E1			H6TD	Sheet 1/1															

Cell Name	Function					Number of BC	
H6W	Power Tri-State Output and Input Buffer (True)					-	
Cell Symbol	Propagation Delay Parameters					Path	
	t_{up}		t_{dn}				
	t_o	K _{CL}	t_o	K _{CL}			
	2.80 (7.05)	0.05	6.60 (11.70)	0.06			
	L → Z		Z → L		H → Z		
t_o 3.00 (41.55)		K _{CL} *	t_o 7.00 (12.95)	K _{CL} 0.07	t_o 6.70 (41.55)	K _{CL} *	
t_o 2.06		K _{CL} 0.06	t_o 3.08		t_o 0.08		
		t_{up}		t_{dn}			
		t_o	K _{CL}	t_o	K _{CL}		
		2.06	0.06	3.08	0.08	X → IN	
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.</p>							
<p>(a) Measurement of t_{pd} at LZ and ZL</p>							
<p>(b) Measurement of t_{pd} at HZ and ZH</p>							
<p>Note:</p> <ol style="list-style-type: none"> The unit of K_{CL} for paths OT, C to X is ns/pF. Output load capacitance of 85pF is used for Fujitsu's logic simulation. The parameters in parentheses are the values applied to the simulation. $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $V_{DD} = 5V \pm 5\%$ 							
<p>Note: This cell is available for AVB Series only.</p>							
AV-H6W-E1		H6W	Sheet 1/1				

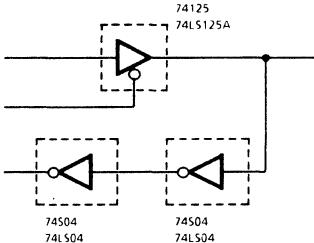
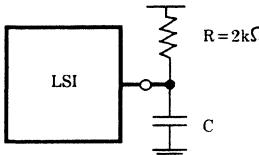
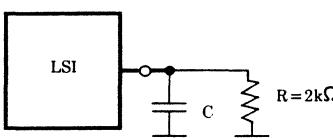
Cell Name	Function					Number of BC							
H6WU	Tri-State Output and Input Buffer with Pull Up Resistance (True)					-							
Cell Symbol	Propagation Delay Parameters				Path								
	t_{up}		t_{dn}										
	t_o	K_{CL}	t_o	K_{CL}	OT → X								
	2.80 (7.05)	0.05	6.60 (11.70)	0.06									
	$L \rightarrow Z$		$Z \rightarrow L$		$H \rightarrow Z$								
	t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}							
	3.00 (41.55)	*	7.00 (12.95)	0.07	6.70 (41.55)	*							
	$Z \rightarrow H$		$H \rightarrow Z$		$Z \rightarrow H$								
	t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}							
	2.06	0.06	3.08	0.08	C → X								
	t_{up}		t_{dn}		X → IN								
	t_o	K_{CL}	t_o	K_{CL}									
	2.06	0.06	3.08	0.08									
* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.													
Input Loading Factor													
		(a) Measurement of t_{pd} at LZ and ZL											
Output Driving Factor													
		(b) Measurement of t_{pd} at HZ and ZH											
TTL Equivalent Circuit													
<p>Note:</p> <ol style="list-style-type: none"> 1: The unit of K_{CL} for paths OT, C to X is ns/pF. 2: Output load capacitance of 85pF is used for Fujitsu's logic simulation. 3: The parameters in parentheses are the values applied to the simulation. 4: $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $V_{DD} = 5V \pm 5\%$ 													
Note: This cell is available for AVB Series only.													
AV-H6WU-E1		H6WU		Sheet 1/1									

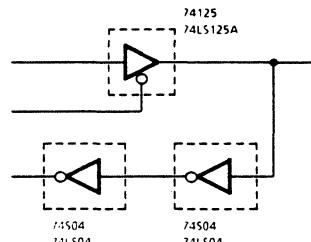
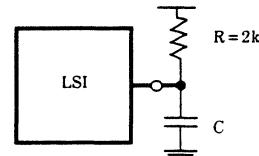
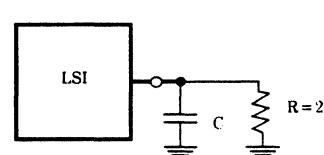
Cell Name	Function	Number of BC																								
H6WD	Tri-State Output and Input Buffer with Pull Down Resistance (True)	-																								
Cell Symbol	Propagation Delay Parameters																									
																										
<table border="1"> <thead> <tr> <th colspan="2">t_{up}</th> <th colspan="2">t_{dn}</th> </tr> <tr> <th>t_o</th> <th>KCL</th> <th>t_o</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>2.80 (7.05)</td> <td>0.05</td> <td>6.60 (11.70)</td> <td>0.06</td> </tr> </tbody> </table>		t_{up}		t_{dn}		t_o	KCL	t_o	KCL	2.80 (7.05)	0.05	6.60 (11.70)	0.06	Path												
t_{up}		t_{dn}																								
t_o	KCL	t_o	KCL																							
2.80 (7.05)	0.05	6.60 (11.70)	0.06																							
<table border="1"> <thead> <tr> <th colspan="2">$L \rightarrow Z$</th> <th colspan="2">$Z \rightarrow L$</th> <th colspan="2">$H \rightarrow Z$</th> <th colspan="2">$Z \rightarrow H$</th> </tr> <tr> <th>t_o</th> <th>KCL</th> <th>t_o</th> <th>KCL</th> <th>t_o</th> <th>KCL</th> <th>t_o</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>3.00 (41.55)</td> <td>*</td> <td>7.00 (12.95)</td> <td>0.07</td> <td>6.70 (41.55)</td> <td>*</td> <td>3.80 (12.95)</td> <td>0.05</td> </tr> </tbody> </table>		$L \rightarrow Z$		$Z \rightarrow L$		$H \rightarrow Z$		$Z \rightarrow H$		t_o	KCL	t_o	KCL	t_o	KCL	t_o	KCL	3.00 (41.55)	*	7.00 (12.95)	0.07	6.70 (41.55)	*	3.80 (12.95)	0.05	OT → X
$L \rightarrow Z$		$Z \rightarrow L$		$H \rightarrow Z$		$Z \rightarrow H$																				
t_o	KCL	t_o	KCL	t_o	KCL	t_o	KCL																			
3.00 (41.55)	*	7.00 (12.95)	0.07	6.70 (41.55)	*	3.80 (12.95)	0.05																			
<table border="1"> <thead> <tr> <th colspan="2">t_{up}</th> <th colspan="2">t_{dn}</th> </tr> <tr> <th>t_o</th> <th>KCL</th> <th>t_o</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>2.06</td> <td>0.06</td> <td>3.08</td> <td>0.08</td> </tr> </tbody> </table>		t_{up}		t_{dn}		t_o	KCL	t_o	KCL	2.06	0.06	3.08	0.08	C → X												
t_{up}		t_{dn}																								
t_o	KCL	t_o	KCL																							
2.06	0.06	3.08	0.08																							
<table border="1"> <thead> <tr> <th colspan="2">$L \rightarrow Z$</th> <th colspan="2">$Z \rightarrow L$</th> <th colspan="2">$H \rightarrow Z$</th> <th colspan="2">$Z \rightarrow H$</th> </tr> <tr> <th>t_o</th> <th>KCL</th> <th>t_o</th> <th>KCL</th> <th>t_o</th> <th>KCL</th> <th>t_o</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>2.06</td> <td>0.06</td> <td>3.08</td> <td>0.08</td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>		$L \rightarrow Z$		$Z \rightarrow L$		$H \rightarrow Z$		$Z \rightarrow H$		t_o	KCL	t_o	KCL	t_o	KCL	t_o	KCL	2.06	0.06	3.08	0.08					X → IN
$L \rightarrow Z$		$Z \rightarrow L$		$H \rightarrow Z$		$Z \rightarrow H$																				
t_o	KCL	t_o	KCL	t_o	KCL	t_o	KCL																			
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<p>(a) Measurement of t_{pd} at LZ and ZL</p>																										
																										
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<p>Note:</p> <ol style="list-style-type: none"> The unit of K_{CL} for paths OT, C to X is ns/pF. Output load capacitance of 85pF is used for Fujitsu's logic simulation. The parameters in parentheses are the values applied to the simulation. $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $V_{DD} = 5V \pm 5\%$ 																										
<p>Note: This cell is available for AVB Series only.</p>																										
AV-H6WD-E1	H6WD	Sheet 1/1																								

Cell Name	Function					Number of BC		
H6C	Tri-State Output and CMOS Interface Input Buffer (True)					-		
Cell Symbol	Propagation Delay Parameters				Path			
	t_{up}		t_{dn}					
	t_o	K_{CL}	t_o	K_{CL}				
	2.46 (9.26)	0.08	6.47 (13.27)	0.08				
	$L \rightarrow Z$		$Z \rightarrow L$					
	t_o	K_{CL}	t_o	K_{CL}				
	1.60 (31.75)	*	5.72 (12.52)	0.08				
	$H \rightarrow Z$		$Z \rightarrow H$					
	t_o	K_{CL}	t_o	K_{CL}				
	2.85 (31.75)	*	3.55 (12.52)	0.08				
	t_{up}		t_{dn}					
Input Loading Factor	t_o	K_{CL}	t_o	K_{CL}	X → IN			
	2.29	0.08	2.41	0.05				
Parameter		Symbol	MIN	TYP	MAX	UNIT		
Input High Voltage		V_{IH}	$V_{DD} \times 0.7$			V		
Input Low Voltage		V_{IL}			$V_{DD} \times 0.3$	V		
* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.								
								
(a) Measurement of t_{pd} at LZ and ZL								
								
(b) Measurement of t_{pd} at HZ and ZH								
Note: 1: The unit of K_{CL} for paths OT, C to X is ns/pF. 2: Output load capacitance of 85pF is used for Fujitsu's logic simulation. 3: The parameters in parentheses are the values applied to the simulation.								
Note: This cell is available for AVB Series only.								
AV-H6C-E1				H6C	Sheet 1/1			

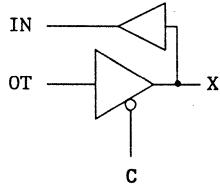
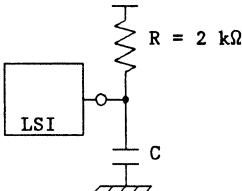
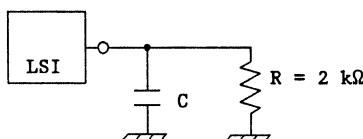
Cell Name	Function					Number of BC									
H6CU	Tri-State Output and CMOS Interface Input Buffer with Pull Up Resistance (True)					-									
Cell Symbol		Propagation Delay Parameters													
		t_{up}		t_{dn}		Path									
		t_o	K _{CL}	t_o	K _{CL}										
			2.46 (9.26)	0.08	6.47 (13.27)	0.08	OT → X								
		L → Z		Z → L		H → Z		Z → H	C → X						
		t_o	K _{CL}	t_o	K _{CL}	t_o	K _{CL}	t_o	K _{CL}						
		1.60 (31.75)	*	5.72 (12.52)	0.08	2.85 (31.75)	*	3.55 (12.52)	0.08						
		t_{up}		t_{dn}		X → IN									
		t_o	K _{CL}	t_o	K _{CL}										
		2.29	0.08	2.41	0.05										
		Parameter		Symbol	MIN	TYP	MAX	UNIT							
		Input High Voltage		V _{IH}	V _{DD} × 0.7				V						
		Input Low Voltage		V _{IL}					V _{DD} × 0.3		V				
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.</p>							3								
<p>(a) Measurement of t_{pd} at LZ and ZL</p>															
<p>(b) Measurement of t_{pd} at HZ and ZH</p>															
<p>Note: 1: The unit of K_{CL} for paths OT, C to X is ns/pF. 2: Output load capacitance of 85pF is used for Fujitsu's logic simulation. 3: The parameters in parentheses are the values applied to the simulation.</p>															
<p>Note: This cell is available for AVB Series only.</p>															
AV-H6CU-E1			H6CU				Sheet 1/1								

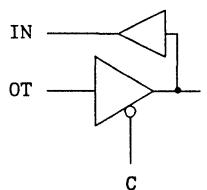
Cell Name	Function					Number of BC		
H6CD	Tri-State Output and CMOS Interface Input Buffer with Pull Down Resistance (True)					-		
Cell Symbol		Propagation Delay Parameters				Path		
		t_{up}		t_{dn}				
		t_o	K_{CL}	t_o	K_{CL}	OT → X		
		2.46 (9.26)		0.08				
		$L \rightarrow Z$		$Z \rightarrow L$		C → X		
		t_o	K_{CL}	t_o	K_{CL}			
		1.60 (31.75)	*	5.72 (12.52)	0.08			
		$H \rightarrow Z$		$Z \rightarrow H$		X → IN		
		t_o	K_{CL}	t_o	K_{CL}			
		2.85 (31.75)	*	3.55 (12.52)	0.08			
		t_{up}		t_{dn}				
		t_o	K_{CL}	t_o	K_{CL}			
		2.29	0.08	2.41	0.05			
		Parameter		Symbol	MIN	TYP		
		Input High Voltage		V_{IH}	$V_{DD} \times 0.7$			
		Input Low Voltage		V_{IL}		$V_{DD} \times 0.3$		
						V		
Input Loading Factor		Pin Name						
2 ℓu 3 ℓu		OT C						
Output Driving Factor		Pin Name						
36 ℓu		IN						
TTL Equivalent Circuit								

Cell Name	Function							Number of BC						
H6E	Power Tri-State Output and CMOS Interface Input Buffer (True)							-						
Cell Symbol	Propagation Delay Parameters							Path OT → X C → X X → IN						
			t_{up}		t_{dn}									
	t_o		K_{CL}		t_o		K_{CL}							
	2.80 (7.05)		0.05		6.60 (11.70)		0.06							
	$L \rightarrow Z$		$Z \rightarrow L$		$H \rightarrow Z$		$Z \rightarrow H$							
	t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}						
	3.00 (41.55)	*	7.00 (12.95)	0.07	6.70 (41.55)	*	3.80 (12.95)	0.05						
	t_{up}		t_{dn}											
	t_o		K_{CL}		t_o		K_{CL}							
	2.29		0.08		2.41		0.05							
Input Loading Factor	Parameter	Symbol	MIN	TYP	MAX	UNIT								
	Input High Voltage	V_{IH}	$V_{DD} \times 0.7$				V							
	Input Low Voltage	V_{IL}					$V_{DD} \times 0.3$	V						
Output Driving Factor	Pin Name													
	2 ℓu 3 ℓu	OT C												
	36 ℓu	IN												
TTL Equivalent Circuit														
														
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.</p>														
														
(a) Measurement of t_{pd} at LZ and ZL														
														
(b) Measurement of t_{pd} at HZ and ZH														
<p>Note: 1: The unit of K_{CL} for paths OT, C to X is ns/pF. 2: Output load capacitance of 85pF is used for Fujitsu's logic simulation. 3: The parameters in parentheses are the values applied to the simulation. 4: $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $V_{DD} = 5V \pm 5\%$</p>														
Note: This cell is available for AVB Series only.						H6E	Sheet 1/1							

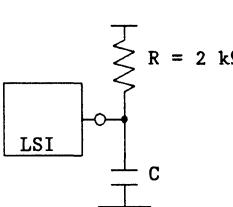
Cell Name	Function									Number of BC												
H6EU	Power Tri-State Output and CMOS Interface Input Buffer with Pull Up Resistance (True)									-												
Cell Symbol	Propagation Delay Parameters									Path												
	t_{up}				t_{dn}				OT → X													
	t_o	K_{CL}			t_o	K_{CL}																
	2.80 (7.05)	0.05			6.60 (11.70)	0.06			C → X													
	L → Z		Z → L		H → Z		Z → H															
	t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}	X → IN													
	3.00 (41.55)	*	7.00 (12.95)	0.07	6.70 (41.55)	*	3.80 (12.95)	0.05														
	t_{up}				t_{dn}				Parameter													
	t_o	K_{CL}			t_o	K_{CL}																
	2.29	0.08			2.41	0.05			Symbol													
					MIN	TYP	MAX	UNIT	Input High Voltage													
					V_{IH}	$V_{DD} \times 0.7$			Input Low Voltage													
Input Loading Factor	Pin Name																					
2 ℓ u	OT																					
3 ℓ u	C																					
Output Driving Factor	Pin Name																					
36 ℓ u	IN																					
TTL Equivalent Circuit																						
																						
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.</p>																						
																						
(a) Measurement of t_{pz} at LZ and ZL																						
																						
(b) Measurement of t_{pz} at HZ and ZH																						
<p>Note: 1: The unit of K_{CL} for paths OT, C to X is ns/pF. 2: Output load capacitance of 85pF is used for Fujitsu's logic simulation. 3: The parameters in parentheses are the values applied to the simulation. 4: $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $V_{DD} = 5V \pm 5\%$</p>																						
Note: This cell is available for AVB Series only.																						
AV-H6EU-E1										H6EU Sheet 1/1												

Cell Name	Function	Propagation Delay Parameters								Number of BC							
H6ED	Power Tri-State Output and CMOS Interface Input Buffer with Pull Down Resistance (True)									-							
Cell Symbol		Propagation Delay Parameters								Path							
		t_{up}		t_{dn}						OT → X							
		t_o	K_{CL}	t_o	K_{CL}					C → X							
		2.80 (7.05)		0.05		6.60 (11.70)		0.06		X → IN							
		$L \rightarrow Z$		$Z \rightarrow L$		$H \rightarrow Z$		$Z \rightarrow H$		X → IN							
		t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}	t_o	K_{CL}	X → IN							
		3.00 (41.55)	*	7.00 (12.95)	0.07	6.70 (41.55)	*	3.80 (12.95)	0.05	X → IN							
		t_{up}		t_{dn}						X → IN							
		t_o	K_{CL}	t_o	K_{CL}					X → IN							
		2.29	0.08	2.41		0.05				X → IN							
		Parameter		Symbol		MIN		TYP		UNIT							
		Input High Voltage		V_{IH}		$V_{DD} \times 0.7$				V							
		Input Low Voltage		V_{IL}				$V_{DD} \times 0.3$		V							
Input Loading Factor		<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows.</p>															
Output Driving Factor																	
TTL Equivalent Circuit		<p>Note:</p> <ol style="list-style-type: none"> The unit of K_{CL} for paths OT, C to X is ns/pF. Output load capacitance of 85pF is used for Fujitsu's logic simulation. The parameters in parentheses are the values applied to the simulation. $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $V_{DD} = 5V \pm 5\%$ 															
AV-H6ED-E1		<p>Note: This cell is available for AVB Series only.</p>															
		<p>H6ED Sheet 1/1</p>															

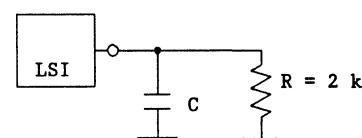
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AV" Version																						
Cell Name	Function	Number of BC																						
H6D	Tri-state Output and Input Buffer for SM1, SM2																							
Cell Symbol		Propagation Delay Parameter																						
		<table border="1"> <thead> <tr> <th>tup</th> <th>tdn</th> <th></th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>2.46 (9.26) 0</td> <td>0.08</td> <td>6.47 (13.27) 0</td> <td>0.08</td> </tr> <tr> <td></td> <td>0</td> <td></td> <td>0</td> </tr> </tbody> </table>	tup	tdn		t0	KCL	t0	KCL	2.46 (9.26) 0	0.08	6.47 (13.27) 0	0.08		0		0	Path OT → X X → IN C → X						
tup	tdn																							
t0	KCL	t0	KCL																					
2.46 (9.26) 0	0.08	6.47 (13.27) 0	0.08																					
	0		0																					
		<table border="1"> <thead> <tr> <th>L → Z</th> <th>Z → L</th> <th></th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>1.60 (31.75)</td> <td>*</td> <td>5.72 (12.52)</td> <td>0.08</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>		L → Z	Z → L		t0	KCL	t0	KCL	1.60 (31.75)	*	5.72 (12.52)	0.08										
L → Z	Z → L																							
t0	KCL	t0	KCL																					
1.60 (31.75)	*	5.72 (12.52)	0.08																					
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (f<u>u</u>)</th> </tr> </thead> <tbody> <tr> <td>OT</td> <td>2</td> </tr> <tr> <td>C</td> <td>3</td> </tr> </tbody> </table>		Pin Name	Input Loading Factor (f <u>u</u>)	OT	2	C	3	<table border="1"> <thead> <tr> <th>H → Z</th> <th>Z → H</th> <th></th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>2.85 (31.75)</td> <td>*</td> <td>3.55 (12.52)</td> <td>0.08</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>		H → Z	Z → H		t0	KCL	t0	KCL	2.85 (31.75)	*	3.55 (12.52)	0.08				
Pin Name	Input Loading Factor (f <u>u</u>)																							
OT	2																							
C	3																							
H → Z	Z → H																							
t0	KCL	t0	KCL																					
2.85 (31.75)	*	3.55 (12.52)	0.08																					
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (f<u>u</u>)</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> </tr> </tbody> </table>		Pin Name	Output Driving Factor (f <u>u</u>)																					
Pin Name	Output Driving Factor (f <u>u</u>)																							
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>																								
																								
(a) Measurement of tpd at LZ and ZL.		(b) Measurement of tpd at HZ and ZH.																						
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation. 4. H6D is the bidirectional protection circuit only for SM1, SM2.</p>																								
AV-H6D-E1		Sheet 1/1																						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version		
Cell Name	Function			Number of BC		
H6DU	Tri-state Output and Input Buffer for SM1, SM2 with Pull Up Resistance					
Cell Symbol		Propagation Delay Parameter				
		tup	tdn			
		t0 2.46 (9.26) 0	KCL 0.08 0	t0 6.47 (13.27) 0	KCL 0.08 0	Path OT → X X → IN
		L → Z Z → L				
		t0 1.60 (31.75)	KCL *	t0 5.72 (12.52)	KCL 0.08	C → X
		H → Z Z → H				
		t0 2.85 (31.75)	KCL *	t0 3.55 (12.52)	KCL 0.08	
Pin Name		Input Loading Factor (λ_u)				
OT	2					
C	3					
Pin Name		Output Driving Factor (λ_u)				

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:

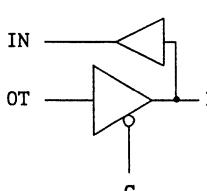
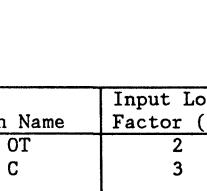
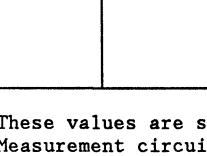
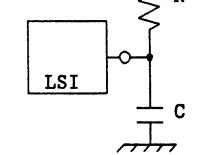
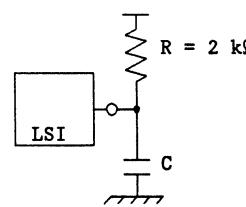
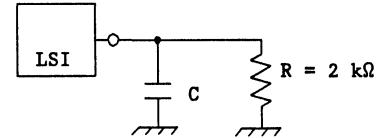


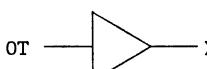
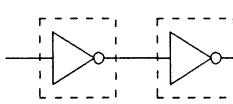
(a) Measurement of tpd at LZ and ZL.

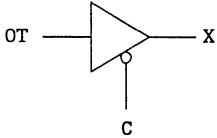
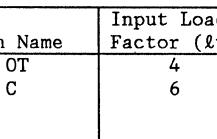


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.
4. H6DU is the bidirectional protection circuit only for SM1, SM2.

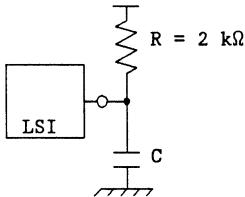
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version
Cell Name	Function			Number of BC
H6DD	Tri-state Output and Input Buffer for SM1, SM2 with Pull Down Resistance			
Cell Symbol		Propagation Delay Parameter		
		tup	tdn	
		t0	KCL	Path
		2.46 (9.26) 0	0.08	OT → X
		6.47 (13.27) 0	0.08	X → IN
		L → Z Z → L		
		t0	KCL	t0 KCL
		1.60 (31.75)	*	5.72 (12.52) 0.08
		H → Z Z → H		
		t0	KCL	t0 KCL
		2.85 (31.75)	*	3.55 (12.52) 0.08
				
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>				
				
(a) Measurement of tpd at LZ and ZL.		(b) Measurement of tpd at HZ and ZH.		
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation. 4. H6DU is the bidirectional protection circuit only for SM1, SM2.</p>				

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version				
Cell Name	Function			Number of BC				
O2L2	High Power Output Buffer(True) (O2L with 20mA drive)							
Cell Symbol		Propagation Delay Parameter						
		t _{up}	t _{dn}	Path OT → X				
t_0 2.11 (3.01)		KCL 0.015	t_0 4.04 (5.12)					
Parameter				Symbol				
				Typ(ns)*				
Pin Name								
OT	Input Loading Factor (λu) 4							
Pin Name		Output Driving Factor (λu)						
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						
TTL Equivalent Circuit								
 74S04 74S04 74LS04 74LS04								
Note: 1. The unit of KCL is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation. 4. $V_{OL} = 0.5V$ at $I_{OL} = 20mA$, $T_A = 0 \sim 70^\circ C$, $VDD = 5V \pm 5\%$ 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.								
This cell is available for AVB series only.								
AV-02L2-E1		Sheet 1/1						

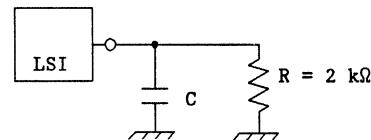
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version																
Cell Name	Function			Number of BC																
04W2 (04W with 20mA drive)				-																
Cell Symbol		Propagation Delay Parameter																		
		<table border="1"> <thead> <tr> <th>tup</th> <th>tdn</th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>3.09 (4.07)</td> <td>0.015</td> <td>6.17 (7.54)</td> <td>0.021</td> </tr> </tbody> </table>		tup	tdn	t0	KCL	t0	KCL	3.09 (4.07)	0.015	6.17 (7.54)	0.021	Path OT → X						
tup	tdn																			
t0	KCL	t0	KCL																	
3.09 (4.07)	0.015	6.17 (7.54)	0.021																	
		<table border="1"> <thead> <tr> <th>L → Z</th> <th>Z → L</th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>5.00 (18.8)</td> <td>*</td> <td>6.10 (7.47)</td> <td>0.021</td> </tr> </tbody> </table>		L → Z	Z → L	t0	KCL	t0	KCL	5.00 (18.8)	*	6.10 (7.47)	0.021	C → X						
L → Z	Z → L																			
t0	KCL	t0	KCL																	
5.00 (18.8)	*	6.10 (7.47)	0.021																	
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (lu)</th> </tr> </thead> <tbody> <tr> <td>OT</td> <td>4</td> </tr> <tr> <td>C</td> <td>6</td> </tr> </tbody> </table>		Pin Name	Input Loading Factor (lu)	OT	4	C	6	<table border="1"> <thead> <tr> <th>H → Z</th> <th>Z → H</th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>6.00 (18.8)</td> <td>*</td> <td>3.30 (7.47)</td> <td>0.016</td> </tr> </tbody> </table>		H → Z	Z → H	t0	KCL	t0	KCL	6.00 (18.8)	*	3.30 (7.47)	0.016	
Pin Name	Input Loading Factor (lu)																			
OT	4																			
C	6																			
H → Z	Z → H																			
t0	KCL	t0	KCL																	
6.00 (18.8)	*	3.30 (7.47)	0.016																	
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (lu)</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> </tr> </tbody> </table>		Pin Name	Output Driving Factor (lu)																	
Pin Name	Output Driving Factor (lu)																			

3

* These values are subject to external loading condition.
 Measurement circuits of propagation delay time
 at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

- Note:
1. The unit of K_{CL} for paths OT, C to X is ns/pF.
 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. V_{OOL} = 0.5V at I_{OOL} = 20mA, T_A = 0 ~ 70°C, V_{DD} = 5V±5%
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

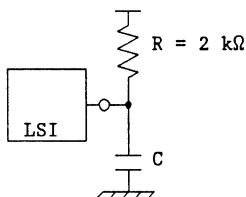
This cell is available for AVB series only.

3

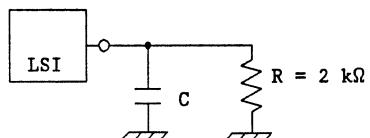
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version	
Cell Name	Function			Number of BC	
H6W2	High Power Tri-State Output and Input Buffer (True) (H6W with 20mA drive)				
Cell Symbol		Propagation Delay Parameter			
		tup	tdn	Path	
IN	OT	t0 2.06	KCL 0.06		
		3.09 (4.37)	0.015	t0 3.08 KCL 0.08	
OT	X	6.17 (7.96)	0.021	Path X → IN	
		L → Z	Z → L	C → X	
OT	C	t0 5.00 (22.6)	KCL *		
		6.10 (7.89)	0.021		
Pin Name	Input Loading Factor (ℓu)				
	OT	4			
Pin Name	C	6			
	Output Driving Factor (ℓu)				
Pin Name	IN	36			

* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

- Note:
1. The unit of KCL for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. $V_{OL} = 0.5V$ at $I_{OL} = 20mA$, $T_A = 0 \sim 70^\circ C$, $V_{DD} = 5V \pm 5\%$
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AVB series only.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version	
Cell Name	Function	Number of BC			
H6W1	High Power Tri-State Output and Input Buffer with Pull Up Resistance(True) (H6WU with 20mA drive)	-			
Cell Symbol	Propagation Delay Parameter				
		t _{up}	t _{dn}	Path	
		t ₀	KCL	X → IN	
		2.06	0.06		
		3.09 (4.37)	0.015	OT → X	
		L → Z	Z → L	C → X	
		t ₀	KCL	t ₀	KCL
		5.00 (22.6)	*	6.10 (7.89)	0.021
		H → Z	Z → H		
		t ₀	KCL	t ₀	KCL
		6.00 (22.6)	*	3.30 (7.89)	0.016
Pin Name	Input Loading Factor (Ωu)				
OT	4				
C	6				
Pin Name	Output Driving Factor (Ωu)				
IN	36				

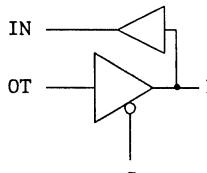
* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:

(a) Measurement of tpd at LZ and ZL.

(b) Measurement of tpd at HZ and ZH.

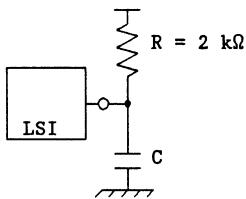
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.
4. V_{OOL} = 0.5V at I_{OOL} = 20mA, T_A = 0 ~ 70°C, V_{DD} = 5V±5%
5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

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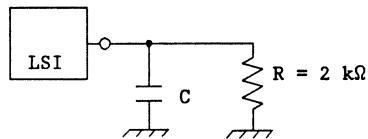
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version																				
Cell Name	Function	Number of BC																						
H6W0	High Power Tri-State Output and Input Buffer with Pull Down Resistance(True) (H6WD with 20mA drive)	-																						
Cell Symbol	Propagation Delay Parameter																							
	<table border="1"> <thead> <tr> <th></th> <th>t_{up}</th> <th></th> <th>t_{dn}</th> <th></th> </tr> <tr> <th></th> <th>t₀</th> <th>KCL</th> <th>t₀</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>IN → X</td> <td>2.06</td> <td>0.06</td> <td>3.08</td> <td>0.08</td> </tr> <tr> <td>OT → X</td> <td>3.09 (4.37)</td> <td>0.015</td> <td>6.17 (7.96)</td> <td>0.021</td> </tr> </tbody> </table>		t _{up}		t _{dn}			t ₀	KCL	t ₀	KCL	IN → X	2.06	0.06	3.08	0.08	OT → X	3.09 (4.37)	0.015	6.17 (7.96)	0.021	Path	X → IN	
	t _{up}		t _{dn}																					
	t ₀	KCL	t ₀	KCL																				
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	L → Z		Z → L																					
	t ₀	KCL	t ₀	KCL																				
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<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (f<u>u</u>)</th> </tr> </thead> <tbody> <tr> <td>OT</td> <td>4</td> </tr> <tr> <td>C</td> <td>6</td> </tr> </tbody> </table>	Pin Name	Input Loading Factor (f <u>u</u>)	OT	4	C	6	<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (f<u>u</u>)</th> </tr> </thead> <tbody> <tr> <td>IN</td> <td>36</td> </tr> </tbody> </table>				Pin Name	Output Driving Factor (f <u>u</u>)	IN	36										
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	H → Z		Z → H																					
	t ₀	KCL	t ₀	KCL																				
C → X	6.00 (22.6)	*	3.30 (7.89)	0.016																				

* These values are subject to external loading condition.

Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

- Note:
1. The unit of KCL for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. $V_{OL} = 0.5V$ at $I_{OL} = 20mA$, $T_A = 0 \sim 70^\circ C$, $V_{DD} = 5V \pm 5\%$
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

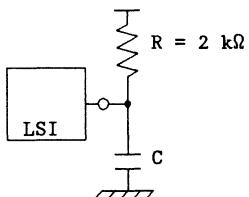
This cell is available for AVB series only.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version																		
Cell Name	Function			Number of BC																		
H6E2	Power Tri-State Output and CMOS Interface Input Buffer (True) (H6E with 20mA drive)																					
Cell Symbol		Propagation Delay Parameter																				
		<table border="1"> <thead> <tr> <th colspan="2">t_{up}</th><th colspan="2">t_{dn}</th></tr> <tr> <th>t₀</th><th>KCL</th><th>t₀</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>2.29</td><td>0.08</td><td>2.41</td><td>0.05</td></tr> <tr> <td>3.09 (4.37)</td><td>0.015</td><td>6.17 (7.96)</td><td>0.021</td></tr> </tbody> </table>			t _{up}		t _{dn}		t ₀	KCL	t ₀	KCL	2.29	0.08	2.41	0.05	3.09 (4.37)	0.015	6.17 (7.96)	0.021		
t _{up}		t _{dn}																				
t ₀	KCL	t ₀	KCL																			
2.29	0.08	2.41	0.05																			
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		<table border="1"> <thead> <tr> <th colspan="2">L → Z</th><th colspan="2">Z → L</th></tr> <tr> <th>t₀</th><th>KCL</th><th>t₀</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>5.00 (22.6)</td><td>*</td><td>6.10 (7.89)</td><td>0.021</td></tr> </tbody> </table>			L → Z		Z → L		t ₀	KCL	t ₀	KCL	5.00 (22.6)	*	6.10 (7.89)	0.021						
L → Z		Z → L																				
t ₀	KCL	t ₀	KCL																			
5.00 (22.6)	*	6.10 (7.89)	0.021																			
<table border="1"> <thead> <tr> <th>Pin Name</th><th>Input Loading Factor (λu)</th></tr> </thead> <tbody> <tr> <td>OT</td><td>4</td></tr> <tr> <td>C</td><td>6</td></tr> </tbody> </table>		Pin Name	Input Loading Factor (λu)	OT	4	C	6	<table border="1"> <thead> <tr> <th colspan="2">H → Z</th><th colspan="2">Z → H</th></tr> <tr> <th>t₀</th><th>KCL</th><th>t₀</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>6.00 (22.6)</td><td>*</td><td>3.30 (7.89)</td><td>0.016</td></tr> </tbody> </table>			H → Z		Z → H		t ₀	KCL	t ₀	KCL	6.00 (22.6)	*	3.30 (7.89)	0.016
Pin Name	Input Loading Factor (λu)																					
OT	4																					
C	6																					
H → Z		Z → H																				
t ₀	KCL	t ₀	KCL																			
6.00 (22.6)	*	3.30 (7.89)	0.016																			
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<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>																						
<p>(a) Measurement of tpd at LZ and ZL.</p>		<p>(b) Measurement of tpd at HZ and ZH.</p>																				
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation. 4. V_{OL} = 0.5V at I_{OL} = 20mA, T_A = 0 ~ 70°C, V_{DD} = 5V±5% 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.</p>																						
<p>This cell is available for AVB series only.</p>																						

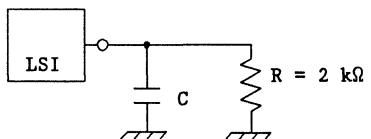
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version	
Cell Name	Function	Number of BC			
H6E1	High Power Tri-State Output and CMOS Interface Input Buffer w/ Pull Up Resistance(True) (H6EU w/ 20mA drive)	-			
Cell Symbol	Propagation Delay Parameter				
		tup	tdn	Path X → IN OT → X	
		t0 2.29 3.09 (4.37)	KCL 0.08 0.015		
		t0 2.41 6.17 (7.96)	KCL 0.05 0.021	C → X	
		L → Z Z → L			
		t0 5.00 (22.6)	KCL *		
		H → Z Z → H			
		t0 6.00 (22.6)	KCL *		
Pin Name	Input Loading Factor (lu)				
OT	4				
C	6				
Pin Name	Output Driving Factor (lu)				
IN	36				

* These values are subject to external loading condition.

Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



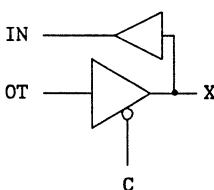
(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

- Note:
1. The unit of K_{CL} for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. V_{OOL} = 0.5V at I_{OOL} = 20mA, T_A = 0 ~ 70°C, V_{DD} = 5V±5%
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

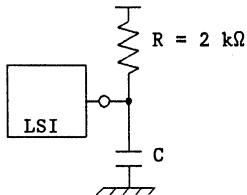
This cell is available for AVB series only.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version	
Cell Name	Function	Number of BC			
H6E0	High Power Tri-State Output and CMOS Interface Input Buffer w/ Pull Down Resistance(True)(H6ED w/ 20mA drive)				
Cell Symbol		Propagation Delay Parameter			
		tup		tdn	
		t0	KCL	t0	
		2.29	0.08	2.41	
		3.09 (4.37)	0.015	6.17 (7.96)	
		Path			
		$X \rightarrow IN$			
		$OT \rightarrow X$			
		L → Z		Z → L	
		t0	KCL	t0	
		5.00 (22.6)	*	6.10 (7.89)	
		0.021			
		H → Z		Z → H	
		t0	KCL	t0	
		6.00 (22.6)	*	3.30 (7.89)	
		0.016			
		Output Driving Factor (lu)			
		Pin Name		Input Loading Factor (lu)	
		OT		4	
		C		6	
		Pin Name		IN	
		36			

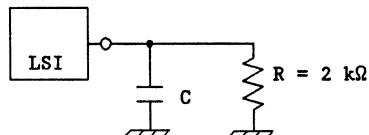
3

* These values are subject to external loading condition.

Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



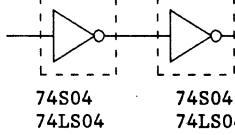
(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. $V_{OL} = 0.5V$ at $I_{OL} = 20mA$, $T_A = 0 \sim 70^\circ C$, $VDD = 5V \pm 5\%$
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

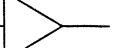
This cell is available for AVB series only.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version			
Cell Name	Function	Number of BC					
O2B2	Power Output Buffer(True) (O2B with 10mA drive)	-					
Cell Symbol		Propagation Delay Parameter					
OT		t _{up}	td _n				
X		t ₀	KCL	Path			
1.40 (3.20)		2.82 (4.80)		0.033 OT → X			
Parameter				Symbol			
				Typ(ns)*			
Pin Name		Input Loading Factor (ℓ_u)					
OT		4					
Pin Name		Output Driving Factor (ℓ_u)					
		* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					
TTL Equivalent Circuit							
 74S04 74S04 74LS04 74LS04							
Note: 1. The unit of KCL is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation. 4. V _{OL} = 0.5V at I _{OL} = 10mA, T _A = 0 ~ 70°C, V _{DD} = 5V±5% 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.							
This cell is available for AV & AVM series only.							

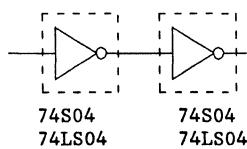
3

Note: 1. The unit of KCL is ns/pF.
 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $VDD = 5V \pm 5\%$
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

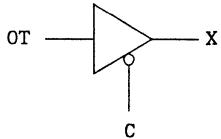
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AV" Version		
Cell Name	Function	Number of BC		
O2B3	High Power Output Buffer(True) (O2B with 15mA drive)	-		
Cell Symbol		Propagation Delay Parameter		
		tup tdn		
t0	KCL	t0	KCL	Path
1.39 (2.59)	0.020	2.59 (3.97)	0.023	OT → X
Parameter		Symbol	Typ(ns)*	
Pin Name	Input Loading Factor (ℓu)			
OT	6			
Pin Name	Output Driving Factor (ℓu)			

TTL Equivalent Circuit



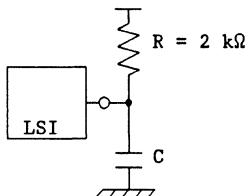
Note: 1. The unit of KCL is ns/pF.
 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. $V_{OL} = 0.5V$ at $I_{OL} = 15mA$, $T_A = 0 \sim 70^\circ C$, $VDD = 5V \pm 5\%$
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

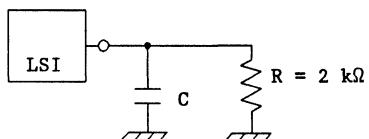
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version										
Cell Name	Function			Number of BC										
04T2	Power Tri-State Output Buffer (True) (04T with 10mA drive)													
Cell Symbol		Propagation Delay Parameter												
		<table border="1"> <thead> <tr> <th>tup</th> <th>tdn</th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>2.03 (3.98)</td> <td>0.030</td> <td>4.48 (6.69)</td> <td>0.034</td> </tr> </tbody> </table>		tup	tdn	t0	KCL	t0	KCL	2.03 (3.98)	0.030	4.48 (6.69)	0.034	Path
tup	tdn													
t0	KCL	t0	KCL											
2.03 (3.98)	0.030	4.48 (6.69)	0.034											
				OT → X										
		<table border="1"> <thead> <tr> <th>L → Z</th> <th>Z → L</th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>3.00 (16.00)</td> <td>*</td> <td>4.41 (6.62)</td> <td>0.034</td> </tr> </tbody> </table>		L → Z	Z → L	t0	KCL	t0	KCL	3.00 (16.00)	*	4.41 (6.62)	0.034	C → X
L → Z	Z → L													
t0	KCL	t0	KCL											
3.00 (16.00)	*	4.41 (6.62)	0.034											
		<table border="1"> <thead> <tr> <th>H → Z</th> <th>Z → H</th> </tr> <tr> <th>t0</th> <th>KCL</th> <th>t0</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>3.50 (16.00)</td> <td>*</td> <td>2.57 (6.62)</td> <td>0.030</td> </tr> </tbody> </table>		H → Z	Z → H	t0	KCL	t0	KCL	3.50 (16.00)	*	2.57 (6.62)	0.030	
H → Z	Z → H													
t0	KCL	t0	KCL											
3.50 (16.00)	*	2.57 (6.62)	0.030											
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (l<u>u</u>)</th> </tr> </thead> <tbody> <tr> <td>OT</td> <td>4</td> </tr> <tr> <td>C</td> <td>6</td> </tr> </tbody> </table>		Pin Name	Input Loading Factor (l <u>u</u>)	OT	4	C	6							
Pin Name	Input Loading Factor (l <u>u</u>)													
OT	4													
C	6													
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (l<u>u</u>)</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> </tr> </tbody> </table>		Pin Name	Output Driving Factor (l <u>u</u>)											
Pin Name	Output Driving Factor (l <u>u</u>)													

* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



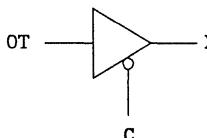
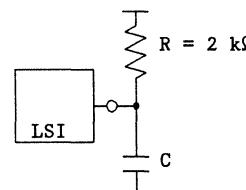
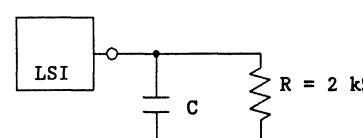
(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

- Note:
1. The unit of K_{CL} for paths OT, C to X is ns/pF.
 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. V_{OL} = 0.5V at I_{OL} = 10mA, T_A = 0 ~ 70°C, V_{DD} = 5V±5%
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

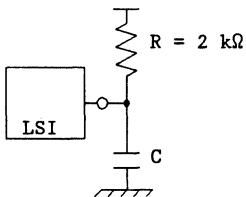
This cell is available for AV & AVM series only.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version						
Cell Name	Function	Number of BC								
04T3	High Power Tri-State Output Buffer(True) (04T with 15mA drive)									
Cell Symbol		Propagation Delay Parameter								
		t _{up}	t _{dn}	Path						
		t ₀ 2.01 (3.31)	KCL 0.020	t ₀ 4.16 (5.72)	KCL 0.024	OT → X				
		L → Z		Z → L		C → X				
		t ₀ 3.50 (16.8)	KCL *	t ₀ 4.33 (5.83)	KCL 0.023					
		H → Z		Z → H						
		t ₀ 4.46 (16.8)	KCL *	t ₀ 2.52 (5.83)	KCL 0.020					
Pin Name		Input Loading Factor (ℓ_u)								
OT	6									
C	9									
Pin Name		Output Driving Factor (ℓ_u)								
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>										
										
(a) Measurement of tpd at LZ and ZL.			(b) Measurement of tpd at HZ and ZH.							
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation. 4. V_{OL} = 0.5V at I_{OL} = 15mA, T_A = 0 ~ 70°C, V_{DD} = 5V±5% 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.</p>										
This cell is available for AV & AVM series only.										
AV-04T3-E1 Sheet 1/1										

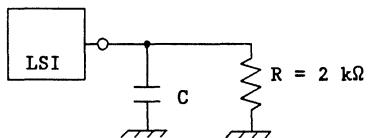
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version						
Cell Name	Function			Number of BC						
H6T2	Power Tri-State Output and Input Buffer(True) (H6T with 10mA drive)									
Cell Symbol		Propagation Delay Parameter								
		tup	tdn							
		t0 2.06 2.03 (4.58)	KCL 0.06 0.030	t0 3.08 4.48 (7.37)						
		KCL 0.08 0.034		Path X → IN OT → X						
		L → Z		Z → L						
		t0 3.00 (20.00)	KCL *	t0 4.41 (7.30)						
				KCL 0.034						
		H → Z		Z → H						
		t0 3.50 (20.00)	KCL *	t0 2.57 (7.30)						
				KCL 0.030						
				C → X						
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Input Loading Factor (ℓu)</th> </tr> </thead> <tbody> <tr> <td>OT</td> <td>4</td> </tr> <tr> <td>C</td> <td>6</td> </tr> </tbody> </table>		Pin Name	Input Loading Factor (ℓu)	OT	4	C	6			
Pin Name	Input Loading Factor (ℓu)									
OT	4									
C	6									
<table border="1"> <thead> <tr> <th>Pin Name</th> <th>Output Driving Factor (ℓu)</th> </tr> </thead> <tbody> <tr> <td>IN</td> <td>36</td> </tr> </tbody> </table>		Pin Name	Output Driving Factor (ℓu)	IN	36					
Pin Name	Output Driving Factor (ℓu)									
IN	36									

* These values are subject to external loading condition.

Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

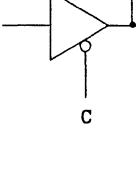


(b) Measurement of tpd at HZ and ZH.

- Note:
1. The unit of K_{CL} for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $VDD = 5V \pm 5\%$
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

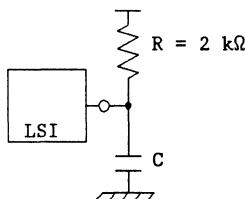
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version			
Cell Name	Function			Number of BC			
H6T3	High Power Tri-State Output and Input Buffer(True) (H6T with 15mA drive)						
Cell Symbol		Propagation Delay Parameter					
		t _{up}	t _{dn}				
		t ₀	KCL	Path			
		2.06	0.06	X → IN			
		2.01 (3.71)	0.020	OT → X			
		3.08	0.08				
		4.16 (6.20)	0.024				
		L → Z					
		t ₀	KCL	Z → L			
		3.50 (20.9)	*	0.023			
		4.33 (6.29)					
		H → Z					
		t ₀	KCL	Z → H			
		4.46 (20.9)	*	0.020			
		2.52 (6.29)					
Pin Name		Output Driving Factor (l _u)					
OT		6					
C		9					
Pin Name		Input Loading Factor (l _u)					
IN		36					
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>							
		(a) Measurement of tpd at LZ and ZL.					
		(b) Measurement of tpd at HZ and ZH.					
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation. 4. V_{OL} = 0.5V at I_{OL} = 15mA, T_A = 0 ~ 70°C, V_{DD} = 5V±5% 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.</p>							
This cell is available for AV & AVM series only.							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version	
Cell Name	Function			Number of BC	
H6C2	Power Tri-State Output and CMOS Interface Input Buffer (True) (H6C with 10mA drive)				
Cell Symbol		Propagation Delay Parameter			
		t _{up}	t _{dn}		
		t ₀	KCL	Path	
		2.29	0.08	X → IN	
		2.03 (4.58)	0.030	OT → X	
		L → Z		Z → L	
		t ₀	KCL		
		3.00 (20.00)	*	0.034	
				C → X	
		H → Z		Z → H	
		t ₀	KCL		
		3.50 (20.00)	*	0.030	
Pin Name		Input Loading Factor (f <u>lu</u>)			
OT	C	4			
		6			
		H → Z			
		t ₀	KCL		
		3.50 (20.00)	*	0.030	
Pin Name		Output Driving Factor (f <u>lu</u>)			
IN		36			

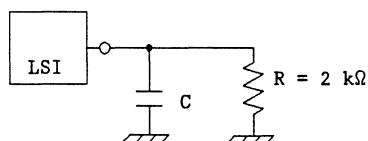
3

* These values are subject to external loading condition.

Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



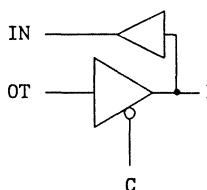
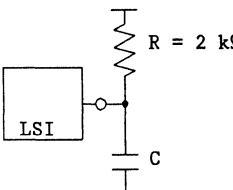
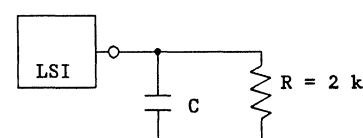
(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.
 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
 3. The parameters in parentheses are the values applied to the simulation.
 4. $V_{OL} = 0.5V$ at $I_{OL} = 10mA$, $T_A = 0 \sim 70^\circ C$, $VDD = 5V \pm 5\%$
 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version								
Cell Name	Function			Number of BC								
H6C3	High Power Tri-State Output and CMOS Interface Input Buffer(True) (H6C with 15mA drive)											
Cell Symbol		Propagation Delay Parameter										
		t _{up}	KCL	t _{dn}								
		2.29	0.08	t ₀								
		2.01 (3.71)	0.020	4.16 (6.20)								
				0.05								
				0.024								
		X → IN										
		OT → X										
L → Z												
<table border="1"> <thead> <tr> <th>t₀</th> <th>KCL</th> <th>t₀</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>3.50 (20.7)</td> <td>*</td> <td>4.33 (6.29)</td> <td>0.023</td> </tr> </tbody> </table>		t ₀	KCL	t ₀	KCL	3.50 (20.7)	*	4.33 (6.29)	0.023	Z → L		C → X
t ₀	KCL	t ₀	KCL									
3.50 (20.7)	*	4.33 (6.29)	0.023									
H → Z												
<table border="1"> <thead> <tr> <th>t₀</th> <th>KCL</th> <th>t₀</th> <th>KCL</th> </tr> </thead> <tbody> <tr> <td>4.46 (20.9)</td> <td>*</td> <td>2.52 (6.29)</td> <td>0.020</td> </tr> </tbody> </table>		t ₀	KCL	t ₀	KCL	4.46 (20.9)	*	2.52 (6.29)	0.020	Z → H		
t ₀	KCL	t ₀	KCL									
4.46 (20.9)	*	2.52 (6.29)	0.020									
Pin Name		Output Driving Factor (f _{lu})										
OT	C	4										
		6										
Pin Name		Input Loading Factor (f _{lu})										
IN		36										
<p>* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:</p>												
												
(a) Measurement of tpd at LZ and ZL.		(b) Measurement of tpd at HZ and ZH.										
<p>Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation. 4. V_{OL} = 0.5V at I_{OL} = 15mA, T_A = 0 ~ 70°C, V_{DD} = 5V±5% 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.</p>												
This cell is available for AV & AVM series only.												

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version			
Cell Name	Function			Number of BC			
I5C	Crystal Oscillator CMOS Interface Input Buffer with Schmitt Trigger						
Cell Symbol		Propagation Delay Parameter					
		t _{up}	t _{dn}	Path			
		t ₀ 84.18 1.00	KCL 0.12 1.123		t ₀ 72.39 0.91	KCL 0.05 0.990	
		Parameter		Symbol	Typ(ns)*		
Pin Name	Input Loading Factor (lu)						
Pin Name	Output Driving Factor (lu)						
PI	18 lu						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							
Equivalent circuit							
Crystal Oscillator Amp							
Schmitt trigger							
I5C cell should be used with OT1. I5C is designed for low frequency oscillation.							
Note:							
*1 The unit of K _{CL} is ns/pF.							
*2 Output load capacitance of 60pF is used for Fujitsu's logic simulation.							
AV-I5C-E1	Sheet 1/1						

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AV" Version			
Cell Name	Function			Number of BC			
OT1	Output Buffer with Protection Circuit Only			0			
Cell Symbol	Propagation Delay Parameter						
		tup	tdn				
		t0	KCL				
		0	0	Path OT → X			
Parameter				Symbol Typ(ns)*			
Pin Name	Input Loading Factor (λ_u)						
OT	0						
Pin Name	Output Driving Factor (λ_u)						
	-						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							
Note :							
OT1 cell should be used with I5C.							
AV-OT1-E1 Sheet 1/1							

RAM Family for C-2301AVM

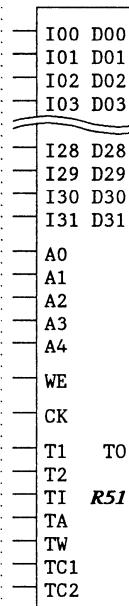
Page	Unit Cell Name	Function
3-273	R51	32w x 32b Single Port Static RAM
3-274	R51A	32w x 28b plus 32w x 4b Single Port Static RAM
3-275	R51B	32w x 24b plus 32w x 8b Single Port Static RAM
3-276	R51C	32w x 20b plus 32w x 12b Single Port Static RAM
3-277	R51D	32w x 16b plus 32w x 16b Single Port Static RAM
3-278	R61	64w x 16b Single Port Static RAM
3-279	R61A	64w x 12b plus 6w x 4b Single Port Static RAM
3-280	R61B	64w x 8b plus 64w x 8b Single Port Static RAM
3-281	R71	128w x 8b Single Port Static RAM
3-282	R71A	128w x 4b plus 128w x 4b Single Port Static RAM
3-283	R83	256w x 4b Single Port Static RAM
3-284	R83A	256w x 2b plus 256w x 2b Single Port Static RAM

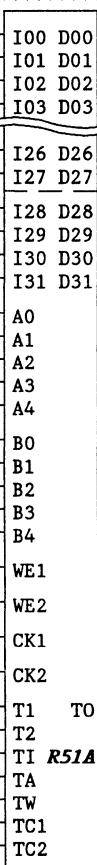
RAM Family for C1502AVM/C4002AVM

3

Page	Unit Cell Name	Function
3-285	R610	64w x 36b Single Port Static RAM
3-286	R611	64w x 20b plus 64w x 16b Single Port Static RAM
3-287	R711	128w x 18b Single Port Static RAM
3-288	R712	128w x 9b plus 128w x 9b Single Port Static RAM
3-289	R87	256w x 9b Single Port Static RAM

3

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version		
RAM Name	Function			
R51	32w x 32b Single Port Static RAM			
RAM Symbol		Propagation Delay Parameter		
		tup	tdn	
		t0	KCL	t0
		9	0.12	21
				0.07
				Path
				CK to D
Parameter			Symbol	Typ(ns)*
Clock Pulse Width (High)			tCWH	25
Clock Pulse Width (Low)			tCWL	20
Clock Pulse Width (Low)			tCWM	5000
Address Setup Time			tSA	5
Address Hold Time			tHA	5
Data Output Hold Time			tHDO	5
Input Data Setup Time			tSDI	20
Input Data Hold Time			tHDI	10
WE Setup Time			tSEH	3
WE Hold Time			tHEH	3
WE Setup Time (Inhibition Mode)			tSEL	5
WE Hold Time (Inhibition Mode)			tHEL	5
* Minimum values (or maximum value for tCWM) for typical operation condition.				
Pin Name		Input Loading Factor (μ u)		
I00 ~ I31		1 μ u		
A0 ~ A4		1 μ u		
WE		1 μ u		
CK		1 μ u		
Pin Name		Output Driving Factor (μ u)		
D00 ~ D31		36 μ u		
Note:				
I00 - I31	: Data Inputs			D00 - D31 : Data Outputs
A0 - A4	: Address Inputs			T1, T2, TI, TA, TW, TC1, TC2 : Inputs for RAM Test
WE	: Write Enable			TO : Output for RAM Test
CK	: Clock			** AO : LSB, A4 : MSB

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version			
RAM Name	Function	Propagation Delay Parameter			
R51A	32w x 28b + 32w x 4b Single Port Static RAM				
RAM Symbol		tup		tdn	
		t0	KCL	t0	KCL
		9	0.12	21	0.07
		Parameter		Symbol	Typ(ns)*
		Clock Pulse Width (High)		tCWH	25
		Clock Pulse Width (Low)		tCWL	20
		Clock Pulse Width (Low)		tCWM	5000
		Address Setup Time		tSA	5
		Address Hold Time		tHA	5
		Data Output Hold Time		tHDO	5
		Input Data Setup Time		tSDI	20
		Input Data Hold Time		tHDI	10
		WE Setup Time		tSEH	3
		WE Hold Time		tHEH	3
		WE Setup Time (Inhibition Mode)		tSEL	5
		WE Hold Time (Inhibition Mode)		tHEL	5
		* Minimum values (or maximum value for tCWM) for typical operation condition.			
		Pin Name		Input Loading Factor (μ u)	
		I00 ~ I31		1 μ u	
		A0 ~ A4		1 μ u	
		B0 ~ B4		1 μ u	
		WE1, WE2		1 μ u	
		CK1, CK2		1 μ u	
		Pin Name		Output Driving Factor (μ u)	
		D00 ~ D31		36 μ u	
Note:					
I00 - I31 : Data Inputs		D00 - D31 : Data Outputs			
A0 - A4 : Address Inputs		T1, T2, TI, TA, TW, TC1, TC2 : Inputs for RAM Test			
B0 - B4 : Write Enable		TO : Output for RAM Test			
CK1, CK2 : Clock		** A0, B0 : LSB A4, B4 : MSB			
R51A	Sheet 1/1				

Note -

T00 = T31 : Data Inputs

A0 = A4

A0 = A4 : Address Inputs
B0 = B4

WE1 WE2 : Write Enable

WE1, WE2 : Write
CK1 CK2 : Clock

CR1, CR2 : Clock

D00 = D31 : Data Outputs

D00 - D51 : Data Outputs

T1, T2, T1,
TW TG1 TG2

TO : Output for RAM Test

** A0 B0 : TS

** AU, BU : LSI
A4 B4 : MSI

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version																																								
RAM Name	Function																																									
R51C 32w x 20b + 32w x 12b Single Port Static RAM																																										
RAM Symbol		Propagation Delay Parameter																																								
		<table border="1"> <thead> <tr> <th colspan="2">tup</th><th colspan="2">tdn</th></tr> <tr> <th>t0</th><th>KCL</th><th>t0</th><th>KCL</th></tr> </thead> <tbody> <tr> <td>9</td><td>0.12</td><td>21</td><td>0.07</td></tr> </tbody> </table>		tup		tdn		t0	KCL	t0	KCL	9	0.12	21	0.07																											
tup		tdn																																								
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R51C		Sheet 1/1																																								

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version		
RAM Name	Function			
R51D	32w x 16b + 32w x 16b Single Port Static RAM			
RAM Symbol	Propagation Delay Parameter			
	tup	tdn		
	t0	KCL	t0	KCL
I00 D00 I01 D01 I02 D02 I03 D03	9	0.12	21	0.07
I14 D14 I15 D15 I16 D16 I17 D17				
I30 D30 I31 D31				
A0 A1 A2 A3 A4				
B0 B1 B2 B3 B4				
WE1 WE2				
CK1 CK2				
T1 T0 T2 TI R51D TA TW TC1 TC2				
* Minimum values (or maximum value for tCWM) for typical operation condition.				
Pin Name	Input Loading Factor (lu)	Output Driving Factor (lu)		
I00 ~ I31	1 lu			
A0 ~ A4	1 lu			
B0 ~ B4	1 lu			
WE1, WE2	1 lu			
CK1, CK2	1 lu			
D00 ~ D31	36 lu			

3

Note:

I00 - I31 : Data Inputs

A0 = A4

A0 = A4 : Address Inputs

WE1 WE2 : Write Enable

WE1, WE2 : Wfil
CK1 CK2 : Clos

D00 = D31 : Data Outputs

D60 D51 : Data outputs

T1, T2, T1,
TW TC1 TC

TW, 101, 102
TO

** A0 BO + TSB

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version				
RAM Name	Function	Propagation Delay Parameter				
R61	64w x 16b Single Port Static RAM	t _{up}	t _{dn}	t ₀	KCL	Path
I00 D00 I01 D01 I02 D02 I03 D03 I04 D04 I05 D05 I06 D06 I07 D07 I08 D08 I09 D09 I10 D10 I11 D11 I12 D12 I13 D13 I14 D14 I15 D15 A0 A1 A2 A3 A4 A5 WE CK T1 T2 TI TA TW TC1 TC2	R61	9	0.12	21	0.07	CK to D
		Parameter	Symbol	Typ(ns)*		
		Clock Pulse Width (High)	tCWH	25		
		Clock Pulse Width (Low)	tCWL	20		
		Clock Pulse Width (Low)	tCWM	5000		
		Address Setup Time	tSA	5		
		Address Hold Time	tHA	5		
		Data Output Hold Time	tHDO	5		
		Input Data Setup Time	tSDI	20		
		Input Data Hold Time	tHDI	10		
		WE Setup Time	tSEH	3		
		WE Hold Time	tHEH	3		
		WE Setup Time (Inhibition Mode)	tSEL	5		
		WE Hold Time (Inhibition Mode)	tHEL	5		
		* Minimum values (or maximum value for CWM) for typical operation condition.				
		Pin Name	Input Loading Factor (f <u>A</u>)			
		I00 ~ I15	1 f <u>A</u>			
		A0 ~ A5	1 f <u>A</u>			
		WE	1 f <u>A</u>			
		CK	1 f <u>A</u>			
		Pin Name	Output Driving Factor (f <u>A</u>)			
		D00 ~ D15	36 f <u>A</u>			
Note:						
I00 ~ I15 : Data Inputs		D00 ~ D15 : Data Outputs				
A0 ~ A5 : Address Inputs		T1, T2, TI, TA, TW, TC1, TC2 : Inputs for RAM Test				
WE : Write Enable		TO : Output for RAM Test				
CK : Clock		** A0 : LSB, A5 : MSB				

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version																																								
RAM Name	Function																																									
R61A	64w x 12b + 64w x 4b Single Port Static RAM																																									
RAM Symbol	Propagation Delay Parameter																																									
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R61A	Sheet 1/1																																									

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version			
RAM Name	Function				
R61B	64w x 8b + 64w x 8b Single Port Static RAM				
RAM Symbol	Propagation Delay Parameter				
	tup	tdn			
	t0	KCL	t0	KCL	Path
I00 D00 I01 D01 I02 D02 I03 D03 I04 D04 I05 D05 I06 D06 I07 D07 I08 D08 I09 D09 I10 D10 I11 D11 I12 D12 I13 D13 I14 D14 I15 D15	9	0.12	21	0.07	CK to D
A0 A1 A2 A3 A4 A5 B0 B1 B2 B3 B4 B5 WE1 WE2 CK1 CK2 T1 T0 T2 TI R61B TA TW TC1 TC2	Parameter			Symbol	Typ(ns)*
	Clock Pulse Width (High)	tCWH	25		
	Clock Pulse Width (Low)	tCWL	20		
	Clock Pulse Width (Low)	tCWM	5000		
	Address Setup Time	tSA	5		
	Address Hold Time	tHA	5		
	Data Output Hold Time	tHDO	5		
	Input Data Setup Time	tSDI	20		
	Input Data Hold Time	tHDI	10		
	WE Setup Time	tSEH	3		
	WE Hold Time	tHEH	3		
	WE Setup Time (Inhibition Mode)	tSEL	5		
	WE Hold Time (Inhibition Mode)	tHEL	5		
	* Minimum values (or maximum value for CWM) for typical operation condition.				
	Pin Name	Input Loading Factor (lu)			
I00 ~ I15 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2	1 lu 1 lu 1 lu 1 lu 1 lu				
	Pin Name	Output Driving Factor (lu)			
	D00 ~ D15	36 lu			
Note:					
I00 - I15 : Data Inputs	D00 - D15				: Data Outputs
A0 - A5 : Address Inputs	T1, T2, TI, TA,				: Inputs for RAM Test
B0 - B5	TW, TC1, TC2				
WE1, WE2 : Write Enable	TO				: Output for RAM Test
CK1, CK2 : Clock	** A0, B0 : LSB				
	A5, B5 : MSB				

Note:

T00 = T15 : Data Inputs

A0 = A5

A0 = A5 : Address Input
B0 = B5

WE1, WE2 : Write

WE1, WE2 : Write Enable
CK1 CK2 : Clock

R61B Sheet 1

D00 = D15 : Data Outputs

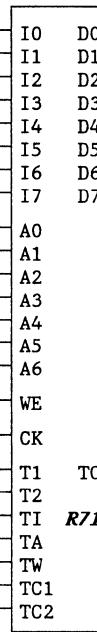
T1, T2, T3, TA, TB, TC, TD, TE, TF, TG, TH, TI, TII, TIII

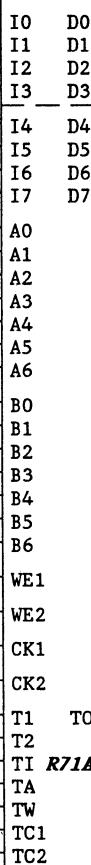
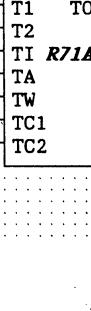
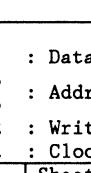
11, 12, 11,
TW, TG1, TG2

TQ

** A0 B0 : LSP

A0, B0 : LSI
A5 B5 : MSI

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version			
RAM Name	Function				
R71	128w x 8b Single Port Static RAM				
RAM Symbol		Propagation Delay Parameter			
		t _{up}	t _{dn}		
		t ₀	KCL		
		9	0.12		
		t ₀	KCL		
		22	0.07		
		Path			
		CK to D			
Parameter					
Symbol					
Clock Pulse Width (High)	tCWH	Typ(ns)*			
Clock Pulse Width (Low)	tCWL	25			
Clock Pulse Width (Low)	tCWM	20			
Address Setup Time	tSA	5000			
Address Hold Time	tHA	5			
Data Output Hold Time	tHDO	5			
Input Data Setup Time	tSDI	5			
Input Data Hold Time	tHDI	20			
WE Setup Time	tSEH	10			
WE Hold Time	tHEH	3			
WE Setup Time (Inhibition Mode)	tSEL	3			
WE Hold Time (Inhibition Mode)	tHEL	5			
* Minimum values (or maximum value for tCWM) for typical operation condition.					
Pin Name		Input Loading Factor (l <u>u</u>)			
I0 ~ I7		1 l <u>u</u>			
A0 ~ A6		1 l <u>u</u>			
WE		1 l <u>u</u>			
CK		1 l <u>u</u>			
Pin Name		Output Driving Factor (l <u>u</u>)			
D0 ~ D7		36 l <u>u</u>			
Note:					
I0 ~ I7	: Data Inputs	D0 ~ D7	: Data Outputs		
A0 ~ A6	: Address Inputs	T1, T2, TI, TA,	: Inputs for RAM Test		
WE	: Write Enable	TW, TC1, TC2	: Inputs for RAM Test		
CK	: Clock	TO	: Output for RAM Test		
** A0 : LSB, A6 : MSB					

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version							
RAM Name	Function	Propagation Delay Parameter							
RAM Symbol		t _{up}	t _{dn}	t ₀	KCL	Path			
		9	0.12	22	0.07	CK to D			
			Parameter			Symbol			
Clock Pulse Width (High)			tCWH	Typ(ns)*					
Clock Pulse Width (Low)			tCWL	25					
Clock Pulse Width (Low)			tCWM	5000					
Address Setup Time			tSA	5					
Address Hold Time			tHA	5					
Data Output Hold Time			tHDO	5					
Input Data Setup Time			tSDI	20					
Input Data Hold Time			tHDI	10					
WE Setup Time			tSEH	3					
WE Hold Time			tHEH	3					
WE Setup Time (Inhibition Mode)			tSEL	5					
WE Hold Time (Inhibition Mode)			tHEL	5					
<small>* Minimum values (or maximum value for tCWM) for typical operation condition.</small>									
	Pin Name	Input Loading Factor (μ A)							
	I0 ~ I7	1 μ A							
	A0 ~ A6	1 μ A							
	B0 ~ B6	1 μ A							
	WE1, WE2	1 μ A							
	CK1, CK2	1 μ A							
	Pin Name	Output Driving Factor (μ A)							
	D0 ~ D7	36 μ A							
Note: I0 - I7 : Data Inputs D0 - D7 : Data Outputs A0 - A6 : Address Inputs T1, T2, TI, TA, : Inputs for RAM Test B0 - B6 : TW, TC1, TC2 : Output for RAM Test WE1, WE2 : Write Enable TO : Output for RAM Test CK1, CK2 : Clock ** A0, B0 : LSB R71A Sheet 1/1 A6, B6 : MSB									

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version																																								
RAM Name	Function																																									
R83	256w x 4b Single Port Static RAM																																									
RAM Symbol	Propagation Delay Parameter																																									
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D0 ~ D3	36 μ u																																									
Note:																																										
I0 - I3 : Data Inputs	D0 - D3 : Data Outputs																																									
A0 - A7 : Address Inputs	T1, T2, TI, TA, TW, TC1, TC2 : Inputs for RAM Test																																									
WE : Write Enable	TO : Output for RAM Test																																									
CK : Clock	** A0 : LSB, A7 : MSB																																									

8

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION				"AVM" Version		
RAM Name	Function					
R83A	256w x 2b + 256w x 2b Single Port Static RAM					
RAM Symbol	Propagation Delay Parameter					
	tup	tdn				
	t0	KCL	t0	KCL		
	9	0.12	22	0.07		
	Parameter	Symbol	Typ(ns)*			
	Clock Pulse Width (High)	tCWH	25			
	Clock Pulse Width (Low)	tCWL	20			
	Clock Pulse Width (Low)	tCWM	5000			
	Address Setup Time	tSA	5			
	Address Hold Time	tHA	5			
	Data Output Hold Time	tHDO	5			
	Input Data Setup Time	tSDI	20			
	Input Data Hold Time	tHDI	10			
	WE Setup Time	tSEH	3			
	WE Hold Time	tHEH	3			
	WE Setup Time (Inhibition Mode)	tSEL	5			
	WE Hold Time (Inhibition Mode)	tHEL	5			
	* Minimum values (or maximum value for tCWM) for typical operation condition.					
	Pin Name	Input Loading Factor (l <u>u</u>)				
	IO ~ I3	1 l <u>u</u>				
	A0 ~ A7	1 l <u>u</u>				
	B0 ~ B7	1 l <u>u</u>				
	WE1, WE2	1 l <u>u</u>				
	CK1, CK2	1 l <u>u</u>				
	Pin Name	Output Driving Factor (l <u>u</u>)				
	D0 ~ D3	36 l <u>u</u>				
Note:						
IO - I3 : Data Inputs	D0 - D3 : Data Outputs					
A0 - A7 : Address Inputs	T1, T2, TI, TA, TW, TC1, TC2 : Inputs for RAM Test					
B0 - B7 : Write Enable	TO : Output for RAM Test					
WE1, WE2 : Clock	** A0, B0 : LSB A7, B7 : MSB					
R83A	Sheet 1/1	Page				

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version		
RAM Name	Function			
R610	64w x 36b Single Port Static RAM			
RAM Symbol	Propagation Delay Parameter			
	tup	tdn		
	t0	KCL	t0	KCL
I00 D00 I01 D01 I02 D02 I03 D03 I04 D04 I05 D05 I06 D06 I07 D07 I08 D08 I09 D09 I10 D10	12	0.12	26	0.07
I30 D30 I31 D31 I32 D32 I33 D33 I34 D34 I35 D35	Parameter			Symbol Typ(ns)*
A0 A1 A2 A3 A4 A5	Clock Pulse Width (High)	tCWH	25	
WE	Clock Pulse Width (Low)	tCWL	20	
CK	Clock Pulse Width (Low)	tCWM	5000	
T1 TO T2 TI R610	Address Setup Time	tSA	5	
TA TW TC1 TC2	Address Hold Time	tHA	5	
	Data Output Hold Time	tHDO	5	
	Input Data Setup Time	tSDI	20	
	Input Data Hold Time	tHDI	10	
	WE Setup Time	tSEH	3	
	WE Hold Time	tHEH	3	
	WE Setup Time (Inhibition Mode)	tSEL	5	
	WE Hold Time (Inhibition Mode)	tHEL	5	
	* Minimum values (or maximum value for tCWM) for typical operation condition.			
	Pin Name	Input Loading Factor (μ u)		
I00 ~ I35 A0 ~ A5 WE CK	1 μ u 1 μ u 1 μ u 1 μ u			
	Pin Name	Output Driving Factor (μ u)		
D00 ~ D35	36 μ u			
Note:				
I00 - I35 : Data Inputs	D00 - D35	: Data Outputs		
A0 - A5 : Address Inputs	T1, T2, TI, TA,	: Inputs for RAM Test		
WE : Write Enable	TW, TC1, TC2			
CK : Clock	TO	: Output for RAM Test		
	** A0 : LSB, A5 : MSB			

3

Note:

Note:
I00 - I35 : Data Inputs
A0 - A5 : Address Inputs
WE : Write Enable
CK : Clock

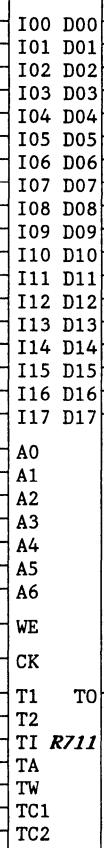
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D00 - D35      : Data Outputs
T1, T2, TI, TA, : Inputs for RAM Test
TW, TC1, TC2   :
TO             : Output for RAM Test
** A0 : LSB. A5 : MSB

```

B610 Sheet 1/1

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version			
RAM Name	Function				
R611	64w x 20b + 64w x 16b Single Port Static RAM				
RAM Symbol	Propagation Delay Parameter				
	tup	tdn		Path	
	t0	KCL	t0	KCL	
I00 D00 I01 D01 I02 D02 I03 D03	12	0.12	26	0.07	
I17 D17 I18 D18 I19 D19				CK to D	
I20 D20 I21 D21 I22 D22					
I33 D33 I34 D34 I35 D35					
Parameter	Symbol	Typ(ns)*			
Clock Pulse Width (High)	tCWH	25			
Clock Pulse Width (Low)	tCWL	20			
Clock Pulse Width (Low)	tCWM	5000			
A0	tSA	5			
A1	tHA	5			
A2	tHDO	5			
A3	tSDI	20			
A4	tHDI	10			
A5	tSEH	3			
B0	tHEH	3			
B1	tSEL	5			
B2	tHEL	5			
B3					
B4					
B5					
WE1					
CK1					
WE2					
CK2					
T1 T0					
TI R611					
TA					
TW					
TC1					
TC2					
Note:					
I00 - I35 : Data Inputs	D00 - D35	: Data Outputs			
A0 - A5 : Address Inputs	T1, T2, TI, TA,	: Inputs for RAM Test			
B0 - B5 : Write Enable	TW, TC1, TC2				
CK1, CK2 : Clock	TO	: Output for RAM Test			
	** A0, B0 : LSB				
	A5, B5 : MSB				

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version				
RAM Name	Function					
R711	128w x 18b Single Port Static RAM					
RAM Symbol		Propagation Delay Parameter				
		t _{up}	t _{dn}			
		t ₀	KCL	t ₀		
		12	0.12	26		
				0.07		
				Path		
				CK to D		
Parameter			Symbol	Typ(ns)*		
Clock Pulse Width (High)			t _{CWH}	25		
Clock Pulse Width (Low)			t _{CWL}	20		
Clock Pulse Width (Low)			t _{CWM}	5000		
Address Setup Time			t _{SA}	5		
Address Hold Time			t _{HA}	5		
Data Output Hold Time			t _{HD0}	5		
Input Data Setup Time			t _{SDI}	20		
Input Data Hold Time			t _{HD1}	10		
WE Setup Time			t _{SEH}	3		
WE Hold Time			t _{HEH}	3		
WE Setup Time (Inhibition Mode)			t _{SEL}	5		
WE Hold Time (Inhibition Mode)			t _{HEL}	5		
WE						
CK						
T1 T0						
T2						
TI R711						
TA						
TW						
TC1						
TC2						
* Minimum values (or maximum value for t _{CWM}) for typical operation condition.						
Pin Name		Input Loading Factor (f <u>u</u>)				
I00 ~ I17		1 f <u>u</u>				
A0 ~ A6		1 f <u>u</u>				
WE		1 f <u>u</u>				
CK		1 f <u>u</u>				
Pin Name		Output Driving Factor (f <u>u</u>)				
D00 ~ D17		36 f <u>u</u>				
Note:						
I00 - I17 : Data Inputs		D00 - D17 : Data Outputs				
A0 - A6 : Address Inputs		T1, T2, TI, TA, TW, TC1, TC2 : Inputs for RAM Test				
WE : Write Enable		TO : Output for RAM Test				
CK : Clock		** A0 : LSB, A6 : MSB				

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version		
RAM Name	Function			
RAM Symbol	Propagation Delay Parameter			
	tup	tdn		
	t0	KCL	t0	KCL
I00 D00 I01 D01 I02 D02 I03 D03 I04 D04 I05 D05 I06 D06 I07 D07 I08 D08 I09 D09 I10 D10	12	0.12	26	0.07
I16 D16 I17 D17				CK to D
A0 A1 A2 A3 A4 A5 A6				
B0 B1 B2 B3 B4 B5 B6				
WE1 CK1 WE2 CK2 T1 T0 T2 TI R712 TA TW TC1 TC2				
Parameter				
Clock Pulse Width (High)	tCWH	25		
Clock Pulse Width (Low)	tCWL	20		
Clock Pulse Width (Low)	tCWM	5000		
Address Setup Time	tSA	5		
Address Hold Time	tHA	5		
Data Output Hold Time	tHDO	5		
Input Data Setup Time	tSDI	20		
Input Data Hold Time	tHDI	10		
WE Setup Time	tSEH	3		
WE Hold Time	tHEH	3		
WE Setup Time (Inhibition Mode)	tSEL	5		
WE Hold Time (Inhibition Mode)	tHEL	5		
* Minimum values (or maximum value for tCWM) for typical operation condition.				
Pin Name	Input Loading Factor (μ u)			
	I00 ~ I17	1 μ u		
	A0 ~ A6	1 μ u		
	B0 ~ B6	1 μ u		
	WE1, WE2	1 μ u		
	CK1, CK2	1 μ u		
Pin Name	Output Driving Factor (μ u)			
	D00 ~ D17	36 μ u		
Note:				
I00 - I17 : Data Inputs	D00 - D17	: Data Outputs		
A0 - A6 : Address Inputs	T1, T2, TI, TA,	: Inputs for RAM Test		
B0 - B6 : Write Enable	TW, TC1, TC2			
WE1, WE2 : Clock	TO	: Output for RAM Test		
	** A0, B0 : LSB			
	A6, B6 : MSB			

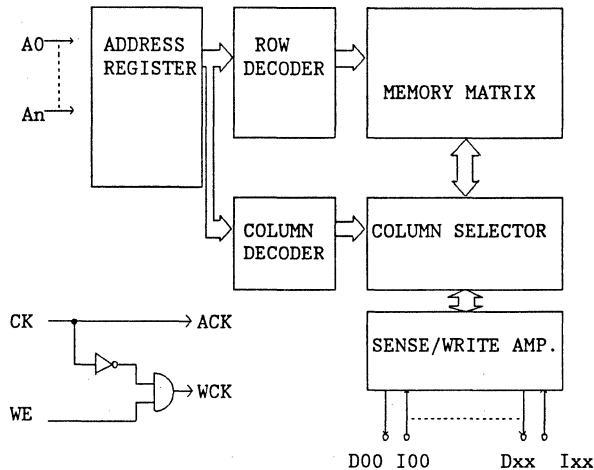
R712 | Sheet 1/1 |

C-1502AVM/C-4002AVM-R712(128w x 9b + 128w x 9b)-E2

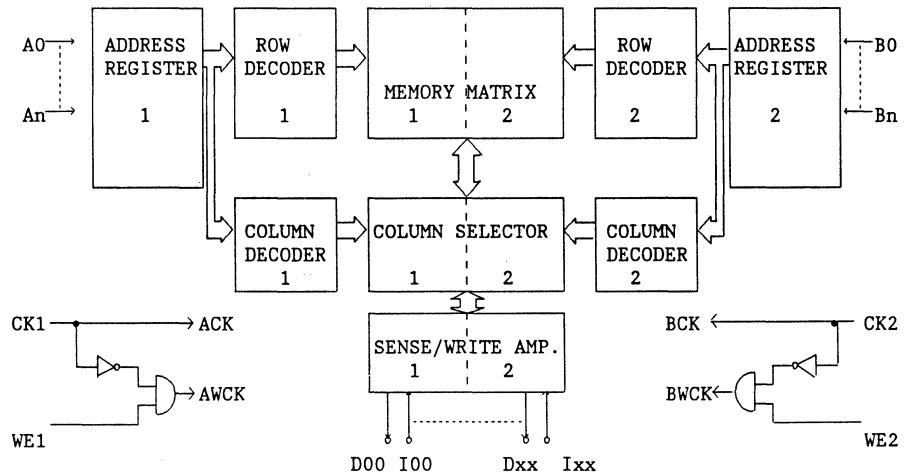
Preliminary

FUJITSU CMOS GATE ARRAY CELL SPECIFICATION		"AVM" Version					
RAM Name	Function						
R87	256w x 9b Single Port Static RAM						
RAM Symbol		Propagation Delay Parameter					
		tup	tdn				
		t0	KCL	t0	KCL		
		12	0.12	26	0.07		
		Path					
		CK to D					
		Parameter		Symbol	Typ(ns)*		
		Clock Pulse Width (High)		tCWH	25		
		Clock Pulse Width (Low)		tCWL	20		
		Clock Pulse Width (Low)		tCWM	5000		
		Address Setup Time		tSA	5		
		Address Hold Time		tHA	5		
		Data Output Hold Time		tHD0	5		
		Input Data Setup Time		tSDI	20		
		Input Data Hold Time		tHDI	10		
		WE Setup Time		tSEH	3		
		WE Hold Time		tHEH	3		
		WE Setup Time (Inhibition Mode)		tHEL	5		
		WE Hold Time (Inhibition Mode)		tHEL	5		
		* Minimum values (or maximum value for tCWM) for typical operation condition.					
		Pin Name	Input Loading Factor (μ u)				
		I0 ~ I8	1 μ u				
		A0 ~ A7	1 μ u				
		WE	1 μ u				
		CK	1 μ u				
		Output Driving Factor (μ u)					
		Pin Name					
		D0 ~ D8	36 μ u				
Note:							
I0 ~ I8 : Data Inputs		D0 ~ D8 : Data Outputs					
A0 ~ A7 : Address Inputs		T1, T2, TI, TA, : Inputs for RAM Test					
WE : Write Enable		TW, TC1, TC2 : RAM Test					
CK : Clock		TO : Output for RAM Test					
** A0 : LSB, A7 : MSB							
R87	Sheet 1/1						

Block Diagram of RAM (Case 1): R51, R61, R71, R83, R610, R710, R87

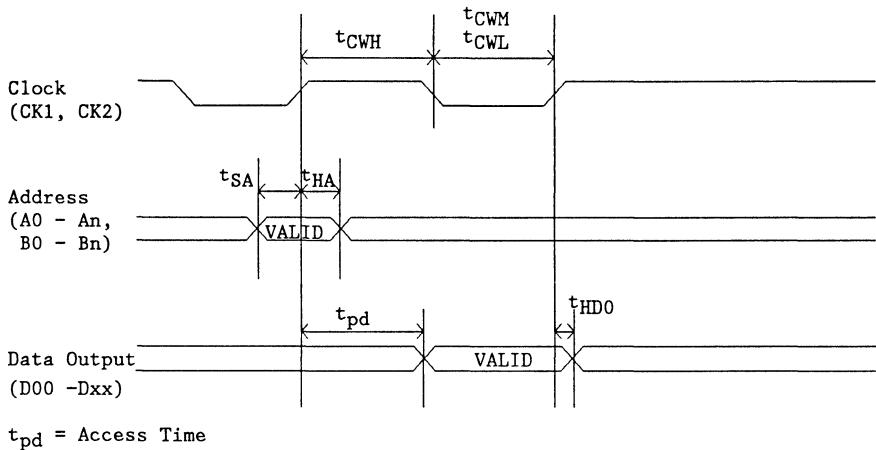


Block Diagram of RAM (Case 2): R51A, R51B, R51C, R51D, R61A, R61B, R71A
R83A, R611, R712

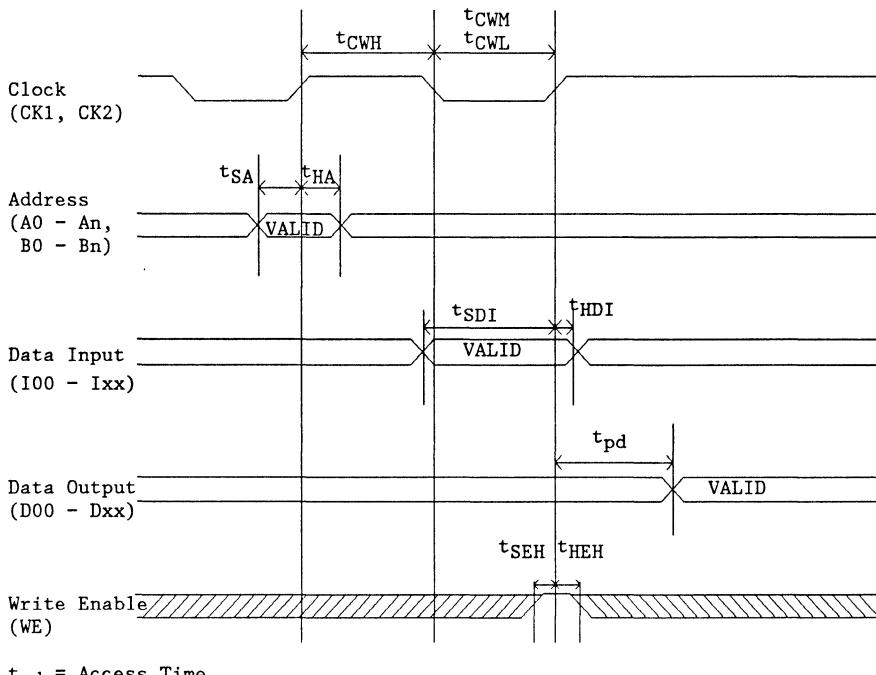


Definition of Parameters for RAM

i) Read mode

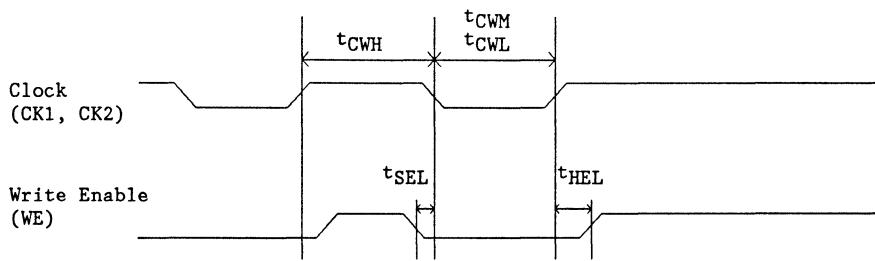


ii) Write mode



Definition of Parameters for RAM (cont'd)

iii) Write Inhibit mode



ROM Family for C-2301AVM

Page	Unit Cell Name	Function
3-295	YRn	256w x 8b ROM

ROM Family for C-1502AVM/C-4002AVM

Page	Unit Cell Na64	Function
3-296	YRn	256w x 18b ROM
3-297	YRn	128w x 36b ROM

3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AVM" Version					
ROM Name	Function	YRn 256w x 8b Read Only Memory					
ROM Symbol	Propagation Delay Parameter						
	tup	tdn					
	t0	KCL	t0	KCL	Path		
A0 ~ A7	15	0.16	30	0.12	CK to D		
CK							
T1	T0						
T2							
TA	YRn						
TC1							
TC2							
Parameter			Symbol	Typ(ns)*			
Clock Pulse Width (High)			tCWH	35			
Clock Pulse Width (Low)			tCWL	25			
Clock Pulse Width (Low)			tCWM	5000			
Address Setup Time			tSA	5			
Address Hold Time			tHA	5			
Data Output Hold Time			tHD0	5			
* Minimum values (or maximum value for tCWM) for typical operation condition.							
Pin Name	Input Loading Factor (μ u)						
	A0 ~ A7	1 μ u					
CK		1 μ u					
Pin Name	Output Driving Factor (μ u)						
	D0 ~ D7	36 μ u					
Note:							
A0 ~ A7 : Address Inputs		T1, T2, TA, TC1, TC2: Inputs for ROM Test					
** A0: LSB, A7: MSB		T0 : Output for ROM Test					
CK : Clock							
D0 ~ D7 : Data Outputs							

3

Note:

A0 - A7 : Address Inputs

A0 - A7 : Address
** A0: LSB, A7: MSB

CK : Clock

D0 = D7 : Data Outputs

T1, T2, TA, TC1, TC2: Inputs for ROM Test

TO : Output for ROM Test

YRn(256x8) | Sheet 1/1

Preliminary

Note:

A0 - A7 : Address Inputs T1, T2, TA, TC1, TC2: Inputs for ROM Test

** A0: LSB, A7: MSB TO : Output for ROM Test

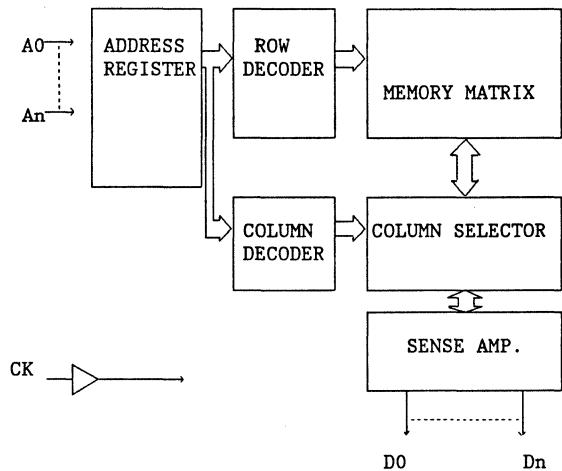
CK : Clock

D00 - D17: Data Outputs

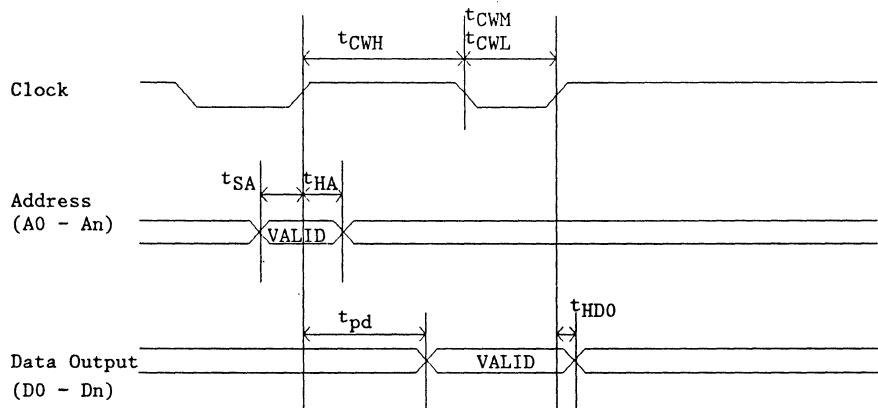
YRn(256x18) Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION				"AVM" Version
ROM Name	Function			
YRn	128w x 36b Read Only Memory			
ROM Symbol	Propagation Delay Parameter			
	tup	tdn		
	t0	KCL	t0	KCL
A0 A1 A2 A3 A4 A5 A6 D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31 D32 D33 D34 D35 CK T1 T0 T2 TA YRn TC1 TC2	15	0.12	29	0.07
	Parameter	Symbol	Typ(ns)*	
	Clock Pulse Width (High)	tCWH	30	
	Clock Pulse Width (Low)	tCWL	25	
	Clock Pulse Width (Low)	tCWM	5000	
	Address Setup Time	tSA	5	
	Address Hold Time	tHA	5	
	Data Output Hold Time	tHDO	5	
	* Minimum values (or maximum value for tCWM) for typical operation condition.			
	Pin Name	Input Loading Factor (μ u)		
	A0 ~ A6	1 μ u		
	CK	1 μ u		
	Pin Name	Output Driving Factor (μ u)		
	D00 ~ D35	36 μ u		
Note:				
A0 ~ A6 : Address Inputs	T1, T2, TA, TC1, TC2:	Inputs for ROM Test		
** A0: LSB, A6: MSB	T0	Output for ROM Test		
CK : Clock				
D00 ~ D35: Data Outputs				
YRn(128x36)	Sheet 1/1			

Block Diagram of ROM



Definition of Parameters for ROM



3

APPENDIX A: General AC Specifications

Pre-layout Simulation Delay Specifications

(Recommended Operating Conditions unless otherwise noted)

Rating	Symbol	Min.	Max.	Unit
Propagation Delay Time	tPLH	(Typ)x0.45	(Typ)x1.6	ns
	tPHL			
Enable Time	tPZL	(Typ)x0.45	(Typ)x1.6	ns
	tPZH			
Disable time	tPLZ	(Typ)x0.45	(Typ)x1.6	ns
	tPHZ			

Post-layout Simulation Delay Specifications

(Recommended Operating Conditions unless otherwise noted)

3

Rating	Symbol	Min.	Max.	Unit
Propagation Delay Time	tPLH	(Typ)x0.5	(Typ)x1.55	ns
	tPHL			
Enable Time	tPZL	(Typ)x0.5	(Typ)x1.55	ns
	tPZH			
Disable time	tPLZ	(Typ)x0.5	(Typ)x1.55	ns
	tPHZ			

3

APPENDIX B: Estimation Tables for Metal Loading

Master Table

Device	Table for CL Estimation						
	1	2	3	4	5	6	7
C-8000AV	• ¹			• ²			
C-6600AV	• ¹			• ²			
C-5000AV					•		
C-3900AV							•
C-2600AV	•						
C-4002AVM							
C-2301AVM	• ³					• ⁴	
C-1502AVM	• ³					• ⁴	
C-2000AVB	•						
C-1600AVB	•						
C-1200AVB		•					
C-850AVB		•					
C-540AVB			•				
C-350AVB			•				

Notes:

1. Internal block routing only.
2. Between-block routing only. (One I/O is regarded as one block.)
3. I/O cell not in the net.
4. I/O cell in the net.

APPENDIX B: Estimation Tables for Metal Loading (Continued)

Table 1

NDI	CL (ℓu)	NDI	CL (ℓu)
1	1.2	11	7.9
2	3.5	12	8.0
3	4.7	13	8.1
4	5.5	14	8.3
5	6.1	15	8.3
6	6.6	16–30	9.0
7	7.2	31–50	10.3
8	7.5	51–75	12.3
9	7.7	76–100	14.4
10	7.9	100 and up	Prohibited

Table 2

3

NDI	CL (ℓu)	NDI	CL (ℓu)
1	1.1	11	5.2
2	2.3	12	5.3
3	3.1	13	5.3
4	3.6	14	5.5
5	4.0	15	5.5
6	4.4	16–30	5.9
7	4.8	31–50	6.8
8	5.0	51–75	8.1
9	5.1	76–100	9.5
10	5.2	100 and up	Prohibited

APPENDIX B: Estimation Tables for Metal Loading (Continued)

Table 3

NDI	CL (ℓu)	NDI	CL (ℓu)
1	1.0	11	3.5
2	1.5	12	3.5
3	2.1	13	3.6
4	2.4	14	3.7
5	2.7	15	3.7
6	2.9	16–30	4.0
7	3.2	31–50	4.5
8	3.3	51–75	5.4
9	3.4	76–100	6.3
10	3.5	100 and up	Prohibited

Table 4

NDI	CL (ℓu)
1	22
2	27.5
3	33
4 and up	38.5
100 and up	Prohibited

APPENDIX B: Estimation Tables for Metal Loading (Continued)

Table 5

NDI	CL (ℓu)	NDI	CL (ℓu)
1	1.9	11	11.9
2	5.3	12	12.1
3	7.2	13	12.2
4	8.3	14	12.4
5	9.1	15	12.4
6	9.9	16–30	13.5
7	10.8	31–50	15.5
8	11.2	51–75	18.5
9	11.6	76–100	21.7
10	11.9	100 and up	Prohibited

Table 6

NDI	CL (ℓu)	NDI	CL (ℓu)
1	18.7	11	26.6
2	19.9	12	26.6
3	22.2	13	26.7
4	23.4	14	26.8
5	24.2	15	27.0
6	24.8	16–30	27.0
7	25.3	31–50	28.1
8	25.9	51–75	29.0
9	26.2	76–100	31.0
10	26.4	100 and up	Prohibited

APPENDIX B: Estimation Tables for Metal Loading (Continued)

Table 7

NDI	CL (ℓu)	NDI	CL (ℓu)
1	1.5	11	10.1
2	4.5	12	10.2
3	6.0	13	10.4
4	7.0	14	10.6
5	7.8	15	10.6
6	8.4	16–30	11.5
7	9.2	31–50	13.2
8	9.6	51–75	15.7
9	9.9	76–100	18.4
10	10.1	100 and up	Prohibited

3

APPENDIX C: AV CMOS Gate Array Available Package Types

		C-2600AV (MB654K)	C-3900AV (MB653K)	C-5000AV (MB652K)	C-6600AV (MB651K)	C-8000AV (MB650K)
Dual In-line Packages (Standard type)						
DIP-24	Plastic	●	●	—	—	—
DIP-28	Ceramic	●	—	—	—	—
DIP-40	Plastic	●	—	—	—	—
	Ceramic	●	●	—	—	—
	Plastic	●	●	●	—	—
DIP-42	Ceramic	●	●	—	—	—
	Plastic	●	●	—	—	—
DIP-48	Ceramic	●	●	—	—	—
	Plastic	●	●	—	—	—
DIP-64	Ceramic	—	—	—	●	—
Dual In-line Packages (Shrink type: 70 mil pin pitch)						
DIP-42SH	Ceramic	●	—	—	—	—
	Plastic	●	—	—	—	—
DIP-48SH	Plastic	●	●	—	—	—
DIP-64SH	Plastic	●	●	●	●	—
Flat Packages (with leads on all four sides of the package)						
FPT-48	Plastic	●	●	—	—	—
FPT-64	Plastic	●	●	●	●	—
FPT-80	Plastic	●	●	●	●	—
FPT-100	Plastic	●	●	●	●	—
FPT-120	Ceramic	—	—	●	●	●
	Plastic	*	●	●	●	●
FPT-160	Plastic	—	—	*	●	●
Pin Grid Array Packages						
PGA-64	Ceramic	●	●	●	●	●
	Plastic	●	●	●	●	●
PGA-88	Ceramic	●	●	●	●	●
	Plastic	●	●	●	●	●
PGA-135	Ceramic	●	●	●	●	●
	Plastic	●	●	●	●	●
PGA-179	Ceramic	—	—	—	●	●

● = Available

* = For these devices, standard pin assignment is not available; only the U version is available.

— = Not available

APPENDIX C: AV CMOS Gate Array Available Package Types 316(Continued)

	C-2600AV (MB654K)	C-3900AV (MB653K)	C-5000AV (MB652K)	C-6600AV (MB651K)	C-8000AV (MB650K)
Leadless Chip Carriers					
LCC-48	Ceramic	●	●	●	—
LCC-64	Ceramic	●	●	●	●
LCC-68	Ceramic	●	●	●	●
LCC-84	Ceramic	—	—	—	●
Plastic Leaded Chip Carrier					
PLCC-28	Plastic	●	—	—	—
PLCC-44	Plastic	●	●	—	—
PLCC-68	Plastic	●	●	●	—
PLCC-84	Plastic	●	●	●	—

● = Available

— = Not available

APPENDIX C: AV CMOS Gate Array Available Package Types with U Type VSS and VDD Pin Assignment

		C-2600AV (MB654K)	C-3900AV (MB653K)	C-5000AV (MB652K)	C-6600AV (MB651K)	C-8000AV (MB650K)
Dual In-line Packages (Standard type)						
DIP-24	Plastic	●	●	—	—	—
DIP-28	Ceramic	●	—	—	—	—
DIP-40	Plastic	●	—	—	—	—
	Ceramic	●	●	—	—	—
	Plastic	●	●	●	—	—
DIP-42	Ceramic	●	●	—	—	—
	Plastic	●	●	—	—	—
DIP-48	Ceramic	●	●	—	—	—
	Plastic	●	●	—	—	—
Dual In-line Packages (Shrink type: 70 mil pin pitch)						
DIP-42S	Ceramic	●	—	—	—	—
	Plastic	●	—	—	—	—
DIP-48S	Plastic	●	●	—	—	—
DIP-64S	Plastic	●	●	●	●	—
Flat Packages (with leads on all four sides of the package)						
FPT-48	Plastic	●	●	—	—	—
FPT-64	Plastic	●	●	●	●	—
FPT-80	Plastic	●	●	●	●	—
FPT-100	Plastic	●	●	●	●	—
FPT-120	Ceramic	—	—	●	●	●
	Plastic	●	●	●	●	●
FPT-160	Plastic	—	—	●	●	●
Pin Grid Array Packages						
PGA-64	Ceramic	●	●	●	●	●
	Plastic	●	●	●	●	●
PGA-88	Ceramic	●	●	●	●	●
	Plastic	●	●	●	●	●
PGA-135	Ceramic	●	●	●	●	●
	Plastic	●	●	●	●	●

● = Available

— = Not available

* = The U type pinout has the same number of VSS pins as the AVB version; that is, it has more VSS pins than the standard AV type. The part number of the device using this type of pinout is suffixed with U; e.g., MB652xxxU.

APPENDIX C: AV CMOS Gate Array Available Package Types with U Type VSS and VDD Pin Assignment (Continued)

		C-2600AV (MB654K)	C-3900AV (MB653K)	C-5000AV (MB652K)	C-6600AV (MB651K)	C-8000AV (MB650K)
Leadless Chip Carriers						
LCC-48	Ceramic	●	●	●	—	—
LCC-64	Ceramic	●	●	●	●	●
LCC-68	Ceramic	●	●	●	●	●
Plastic Leaded Chip Carrier						
PLCC-28	Plastic	●	—	—	—	—
PLCC-44	Plastic	●	●	—	—	—
PLCC-68	Plastic	●	●	●	—	—
PLCC-84	Plastic	●	●	●	—	—

● = Available

— = Not available

		C-350AVB (MB675K)	C-540AVB (MB674K)	C-850AVB (MB673K)	C-1200AVB (MB672K)	C-1600AVB (MB671K)	C-2000AVB (MB670K)
Dual In-line Packages (Standard type)							
DIP-16	Ceramic	●	●	—	—	—	—
	Plastic	●	●	—	—	—	—
DIP-18	Ceramic	●	●	—	—	—	—
	Plastic	●	●	—	—	—	—
DIP-20	Ceramic	●	●	—	—	—	—
	Plastic	●	●	●	—	—	—
DIP-22	Ceramic	●	●	●	●	●	—
	Plastic	●	●	●	●	●	—
DIP-24	Ceramic	●	●	●	●	●	—
	Plastic	●	●	●	●	●	●
DIP-28	Ceramic	●	●	●	●	●	●
	Plastic	●	●	●	●	●	●
DIP-40	Ceramic	●	●	●	●	●	●
	Plastic	●	●	●	●	●	●
DIP-42	Ceramic	—	—	—	●	●	●
	Plastic	●	●	●	●	●	●
DIP-48	Ceramic	—	—	—	●	●	●
	Plastic	—	●	●	●	●	●
Dual In-line Packages (Shrink type: 70 mil pin pitch)							
DIP-28SH	Ceramic	—	●	●	●	—	—
	Plastic	●	●	●	●	●	—
DIP-42SH	Ceramic	—	—	—	●	●	●
	Plastic	●	●	●	●	●	●
DIP-48SH	Plastic	●	●	●	●	●	●
DIP-64SH	Plastic	—	●	●	●	●	●
Dual In-line Packages (Skinny type: 300 mil row space)							
DIP-22SK	Plastic	●	●	●	—	—	—
DIP-24SK	Plastic	●	●	●	—	—	—
DIP-28SK	Plastic	●	●	●	—	—	—
Flat Packages (with leads on two sides of the packages)							
FPT-16	Plastic	●	●	—	—	—	—
FPT-20	Plastic	●	●	—	—	—	—
FPT-24	Plastic	●	●	●	●	—	—
FPT-28	Plastic	●	●	●	●	—	—
Flat Packages (with leads on all four sides of the packages)							
FPT-44	Plastic	●	●	●	●	●	●
FPT-48	Plastic	●	●	●	●	●	●
FPT-64	Plastic	—	●	●	●	●	●
FPT-80	Plastic	—	—	—	●	●	●
FPT-100	Plastic	—	—	—	—	—	●

● = Available

— = Not available

AV CMOS Gate Array AVB Version Available Packages (Continued)

		C-350AVB (MB675K)	C-540AVB (MB674K)	C-850AVB (MB673K)	C-1200AVB (MB672K)	C-1600AVB (MB671K)	C-2000AVB (MB670K)
Repeated In-line Packages (Pin Grid Array Packages)							
PGA-64	Ceramic	—	●	●	●	●	●
	Plastic	—	●	●	●	●	●
PGA-88	Ceramic	—	—	—	—	●	●
	Plastic	—	—	—	—	●	●
Leadless Chip Carriers							
LCC-28	Ceramic	●	●	●	●	●	—
LCC-48	Ceramic	●	●	●	●	●	—
LCC-64	Ceramic	—	●	●	●	●	●
LCC-68	Ceramic	—	—	—	—	●	●
Plastic Leaded Chip Carriers							
PLCC-28	Plastic	●	●	●	●	●	—
PLCC-44	Plastic	●	●	●	●	●	●
PLCC-68	Plastic	—	—	—	●	●	●
PLCC-84	Plastic	—	—	—	—	—	●

● = Available

— = Not available

APPENDIX C: AV CMOS Gate Array AVB Version Available Packages (U-type Pinout Configuration)*

		C-350AVB (MB675K)	C-540AVB (MB674K)	C-850AVB (MB673K)	C-1200AVB (MB672K)	C-1600AVB (MB671K)	C-2000AVB (MB670K)
Dual In-line Packages (Standard type)							
DIP-16	Ceramic	●	●	—	—	—	—
	Plastic	●	●	—	—	—	—
DIP-18	Ceramic	●	●	—	—	—	—
	Plastic	●	●	—	—	—	—
DIP-20	Ceramic	●	●	—	—	—	—
	Plastic	●	●	●	—	—	—
DIP-22	Ceramic	●	●	●	●	●	—
	Plastic	●	●	●	●	●	—
DIP-24	Ceramic	●	●	●	●	●	—
	Plastic	●	●	●	●	●	●
DIP-28	Ceramic	●	●	●	●	●	●
	Plastic	●	●	●	●	●	●
DIP-40	Ceramic	●	●	●	●	●	●
	Plastic	●	●	●	●	●	●
DIP-42	Ceramic	—	—	—	●	●	●
	Plastic	●	●	●	●	●	●
DIP-48	Ceramic	—	—	—	●	●	●
	Plastic	—	●	●	●	●	●
Dual In-line Packages (Shrink type: 70 mil pin pitch)							
DIP-28SH	Ceramic	—	●	●	●	—	—
	Plastic	●	●	●	●	●	—
DIP-42SH	Ceramic	—	—	—	●	●	●
	Plastic	●	●	●	●	●	●
DIP-48SH	Plastic	●	●	●	●	●	●
DIP-64SH	Plastic	—	●	●	●	●	●
Dual In-line Packages (Skinny type: 300 mil row space)							
DIP-22SK	Plastic	●	●	●	—	—	—
DIP-24SK	Plastic	●	●	●	—	—	—
DIP-28SK	Plastic	●	●	●	—	—	—
Flat Packages (with leads on two sides of the packages)							
FPT-16	Plastic	●	●	—	—	—	—
FPT-20	Plastic	●	●	—	—	—	—
FPT-24	Plastic	●	●	●	●	—	—
FPT-28	Plastic	●	●	●	●	—	—

* The U-type pinout configurations have fewer VSS pins and are for designs that use no high-drive output buffers and need more signal pins than those specified for standard pinout. If a design does not require more signal pins than defined for standard pinout, the standard pinout is preferred.

- = Available
- = Not available

APPENDIX C: AV CMOS Gate Array AVB Version Available Packages (U-type Pinout Configuration)* (Continued)

		C-350AVB (MB675K)	C-540AVB (MB674K)	C-850AVB (MB673K)	C-1200AVB (MB672K)	C-1600AVB (MB671K)	C-2000AVB (MB670K)
Flat Packages (with leads on all four sides of the packages)							
FPT-44	Plastic	●	●	●	●	●	●
FPT-48	Plastic	●	●	●	●	●	●
FPT-64	Plastic	—	●	●	●	●	●
FPT-80	Plastic	—	—	—	● **	●	●
FPT-100	Plastic	—	—	—	—	—	●
Repeated In-line Packages (Pin Grid Array Packages)							
PGA-64	Ceramic	—	●	●	●	●	●
	Plastic	—	●	●	●	●	●
PGA-88	Ceramic	—	—	—	—	● **	●
	Plastic	—	—	—	—	● **	●
Leadless Chip Carriers							
LCC-28	Ceramic	●	●	●	●	●	—
LCC-48	Ceramic	●	●	●	●	●	—
LCC-64	Ceramic	—	●	●	●	●	●
LCC-68	Ceramic	—	—	—	—	●	●
Plastic Leaded Chip Carriers							
PLCC-28	Plastic	●	●	●	●	●	—
PLCC-44	Plastic	●	●	●	●	●	●
PLCC-68	Plastic	—	—	—	●	●	●
PLCC-84	Plastic	—	—	—	—	—	●

*The U-type pinout configurations have fewer VSS pins and are for designs that use no high-drive output buffers and need more signal pins than those specified for standard pinout. If a design does not require more signal pins than defined for standard pinout, the standard pinout is preferred.

● = Available

— = Not available

** = U-type version is not available

AV CMOS Gate Array AVM Version Available Package Types (RAM)

		C-1502AVM (MB662K)	C-2301AVM (MB661K)	C-4002AVM (MB660K)
Dual In-line Packages (Standard type)				
DIP-24	Plastic	●	●	—
DIP-28	Plastic	●	—	—
DIP-40	Ceramic	●	●	—
	Plastic	●	●	—
DIP-42	Ceramic	●	●	—
	Plastic	●	●	—
DIP-48	Ceramic	●	●	—
Dual In-line Packages (Shrink type: 70 mil pin pitch)				
DIP-42S	Plastic	●	—	—
DIP-48S	Plastic	●	●	—
DIP-64S	Plastic	●	●	●
Flat Packages				
FPT-48	Plastic	●	●	—
FPT-64	Plastic	●	●	●
FPT-80	Plastic	●	●	●
FPT-100	Plastic	●	●	●
FPT-120	Plastic	●*	●*	●*
FPT-160	Plastic	—	—	●**
Pin Grid Array Packages				
PGA-64	Ceramic	●	●	●
	Plastic	●	●	●
PGA-88	Ceramic	●	●	●
	Plastic	●	●	●
PGA-135	Ceramic	●	●	●
	Plastic	●	●	●
Leadless Chip Carriers				
LCC-48	Ceramic	●	●	—
LCC-64	Ceramic	●	●	●
LCC-68	Ceramic	●	—	●
Plastic Leaded Chip Carriers				
PLCC-44	Plastic	●	●	—
PLCC-68	Plastic	●	●	—
PLCC-84	Plastic	●	●	—

● = Available

— = Not available

* = 8 ground pin option. The part number of the device using this type of pinout is suffixed with "U"; e.g., 662xxxU. Fujitsu recommends the 8 ground pin option for the package.

** = 12 ground pin option. The part number of the device using this type of pinout is suffixed with "U"; e.g., 660xxxU. Fujitsu recommends the 12 ground pin option for the package.

AV CMOS Gate Array AVM Version Available Package Types (ROM)

		C-1502AVM (MB662K)	C-2301AVM (MB661K)	C-4002AVM (MB660K)
Dual In-line Packages (Standard type)				
DIP-24	Plastic	●	●	—
DIP-28	Plastic	●	—	—
DIP-40	Ceramic	●	●	—
	Plastic	●	●	—
DIP-42	Ceramic	●	●	—
	Plastic	●	●	—
DIP-48	Ceramic	●	●	—
Dual In-line Packages (Shrink type: 70 mil pin pitch)				
DIP-42S	Plastic	●	—	—
DIP-48S	Plastic	●	●	—
DIP-64S	Plastic	●	●	●
Flat Packages				
FPT-48	Plastic	●	●	—
FPT-64	Plastic	●	●	●
FPT-80	Plastic	●	●	●
FPT-100	Plastic	●	●	●
FPT-120	Plastic	●*	●*	●*
FPT-160	Plastic	—	—	●**
Pin Grid Array Packages				
PGA-64	Ceramic	●	●	●
	Plastic	●	●	●
PGA-88	Ceramic	●	●	●
	Plastic	●	●	●
PGA-135	Ceramic	●	●	●
	Plastic	●	●	●
Leadless Chip Carriers				
LCC-48	Ceramic	●	●	—
LCC-64	Ceramic	●	●	●
LCC-68	Ceramic	●	—	●
Plastic Leaded Chip Carriers				
PLCC-44	Plastic	●	●	—
PLCC-68	Plastic	●	●	—
PLCC-84	Plastic	●	●	—

● = Available

— = Not available

* = 8 ground pin option. The part number of the device using this type of pinout is suffixed with "U"; e.g., 662xxxU. Fujitsu recommends the 8 ground pin option for the package.

** = 12 ground pin option. The part number of the device using this type of pinout is suffixed with "U"; e.g., 660xxxU. Fujitsu recommends the 12 ground pin option for the package.

APPENDIX D: AV Unit Cell Library Alphanumeric Index

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APPENDIX D: AV Unit Cell Library Alphanumeric Index (Continued)

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* Can be used only with AVB technology

APPENDIX D: AV Unit Cell Library Alphanumeric Index (Continued)

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* Can be used only with AVB technology

APPENDIX D: AV Unit Cell Library Alphanumeric Index (Continued)

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Section 4



Sales Information

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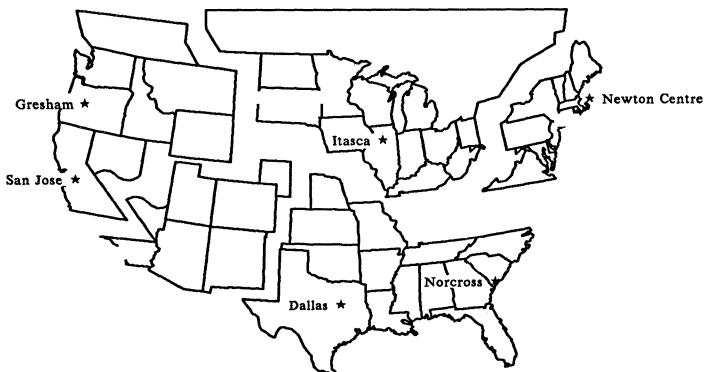
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UHB Series Unit Cell Library

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AV Series Unit Cell Library

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