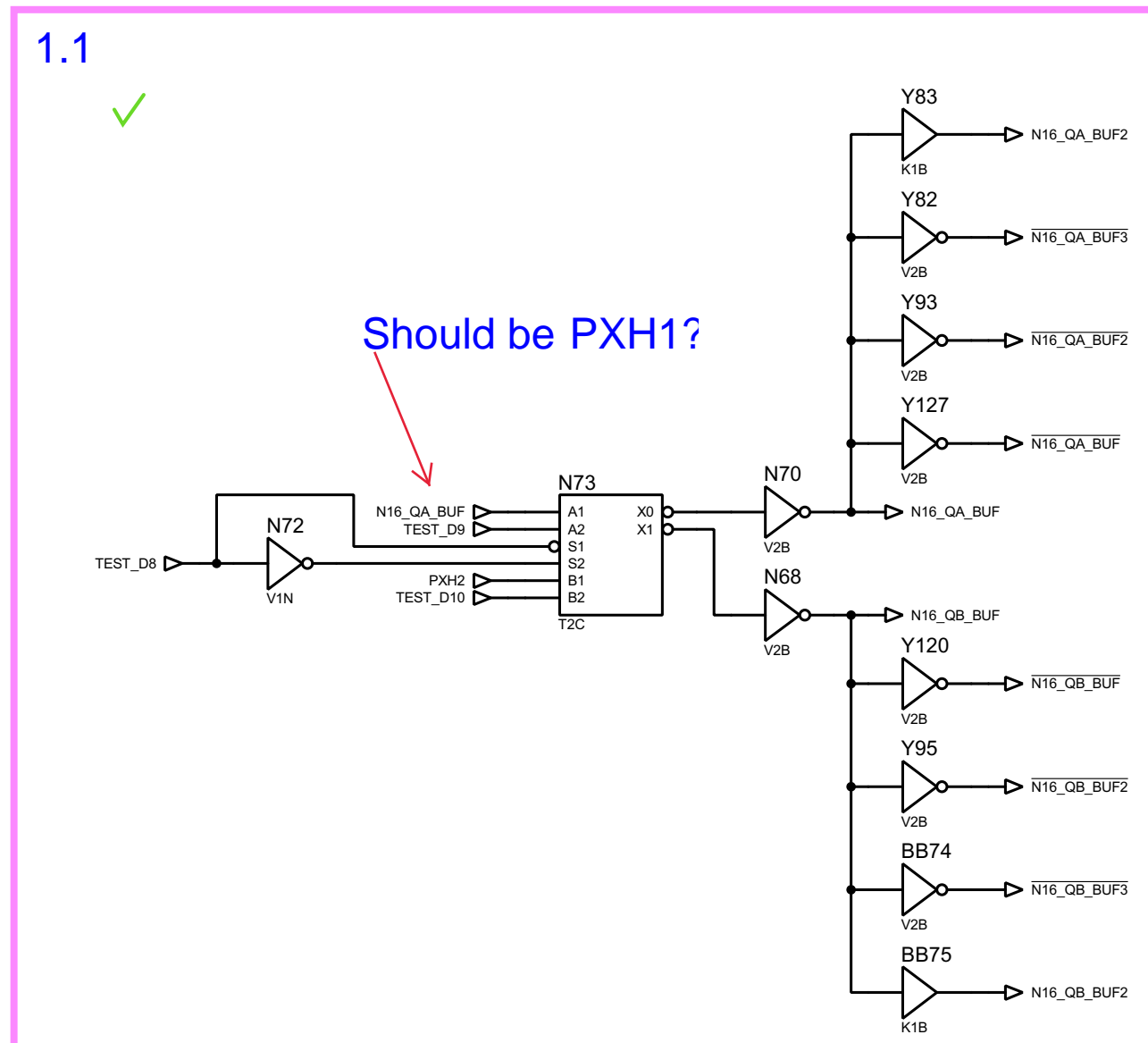


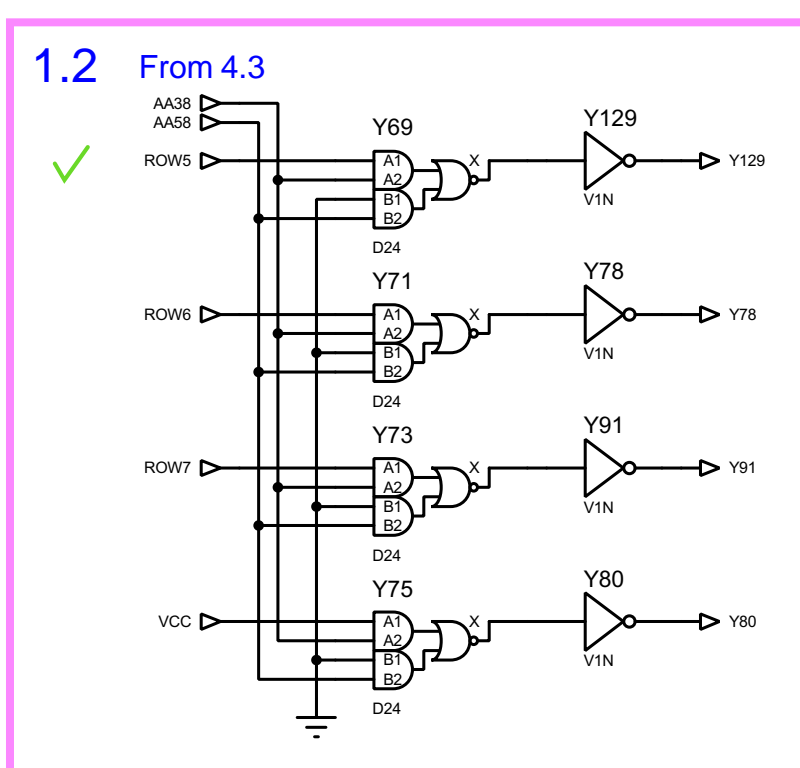
```

VRAM address (1 word per address)
FEDC BA98 7654 3210
0000 01xx xxxxxx Layer FIX tilemap
0000 01xx xxxxxx Layer A tilemap
0000 110x xxxxxx Layer B tilemap
0000 110x xxxxxx B scroll
0000 01xx xxxxxx A X scroll
0001 0xxx xxxxxx Layer FIX codes
0001 01xx xxxxxx Layer A codes
0001 110x xxxxxx Layer B codes
0001 110x xxxxxx B scroll
0001 1101 xxxxxx B X scroll
0001 1101 x xxxxx X tilemaps X
          xxx xxx Tilemaps Y

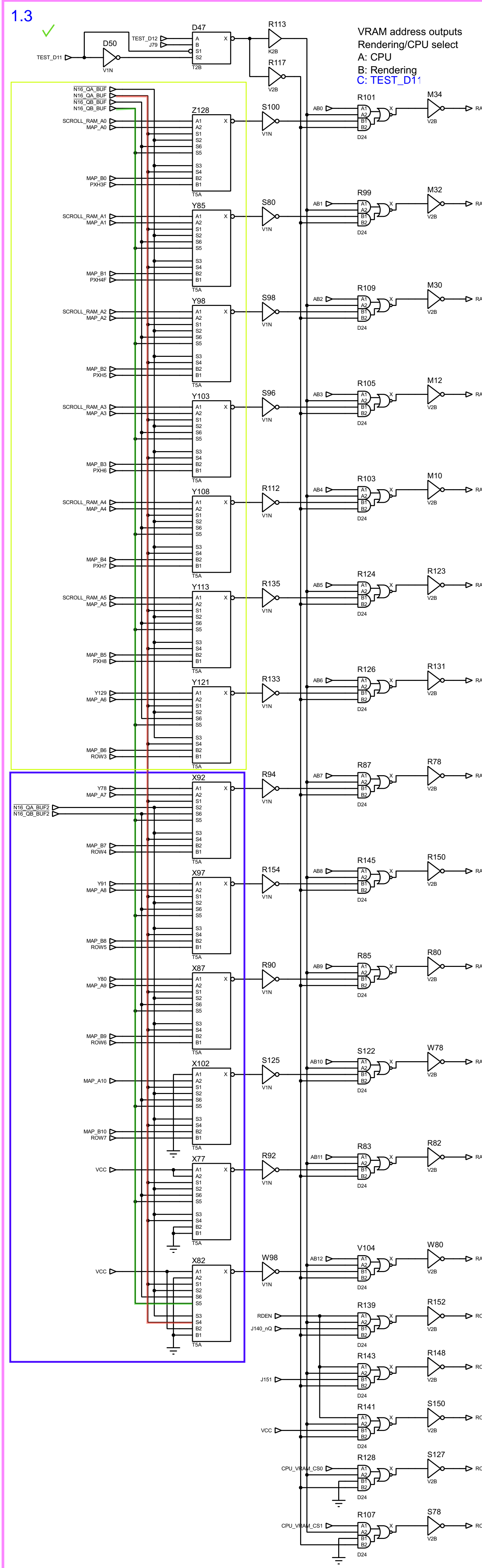
```

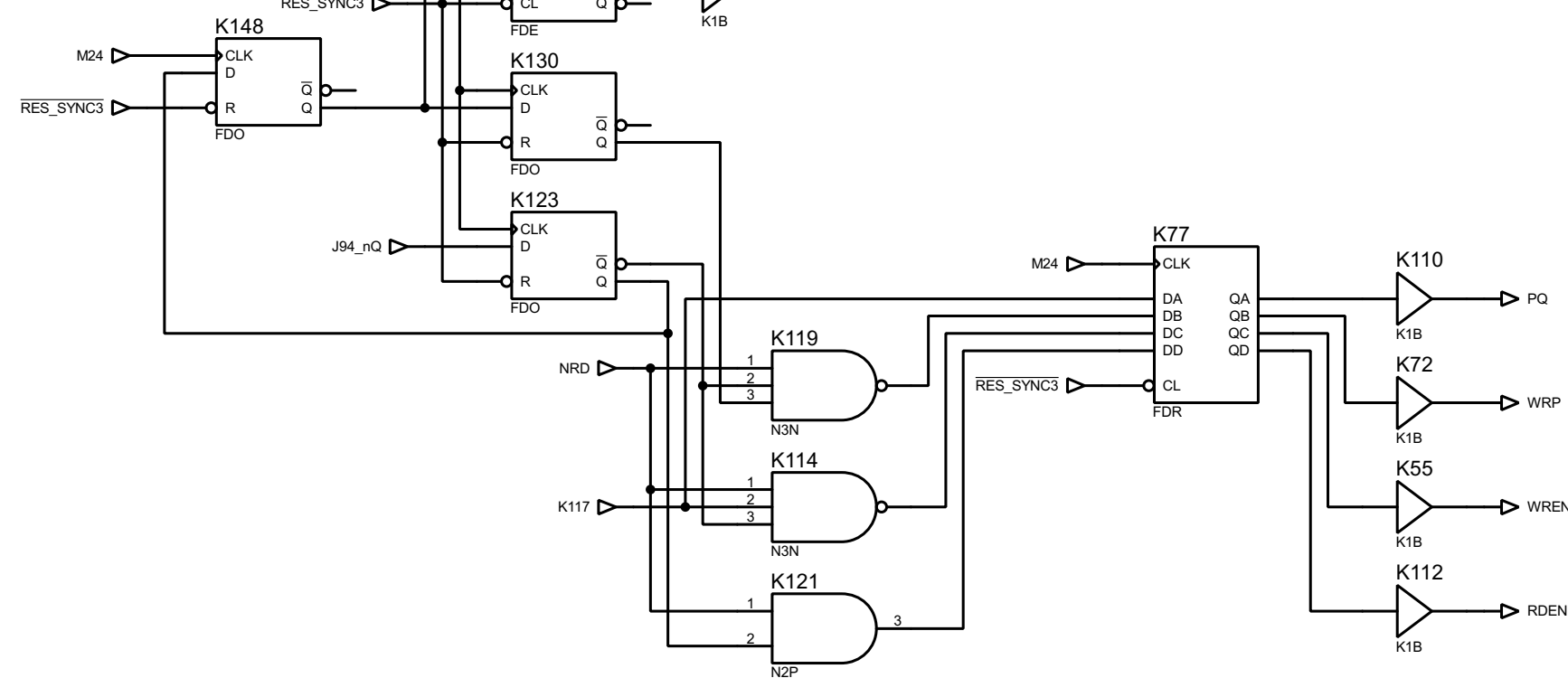
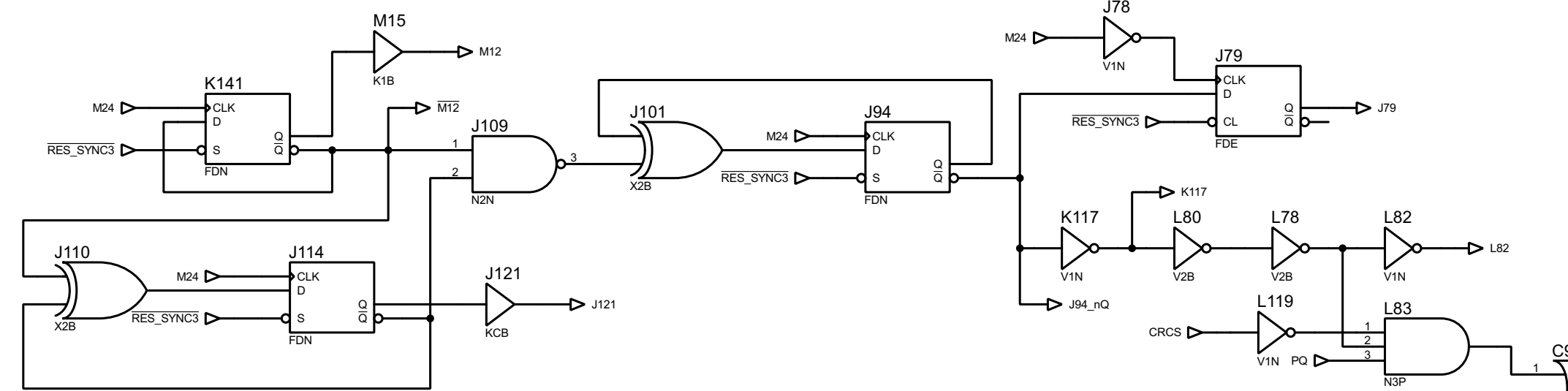


TEST_D13 Addresses Selector



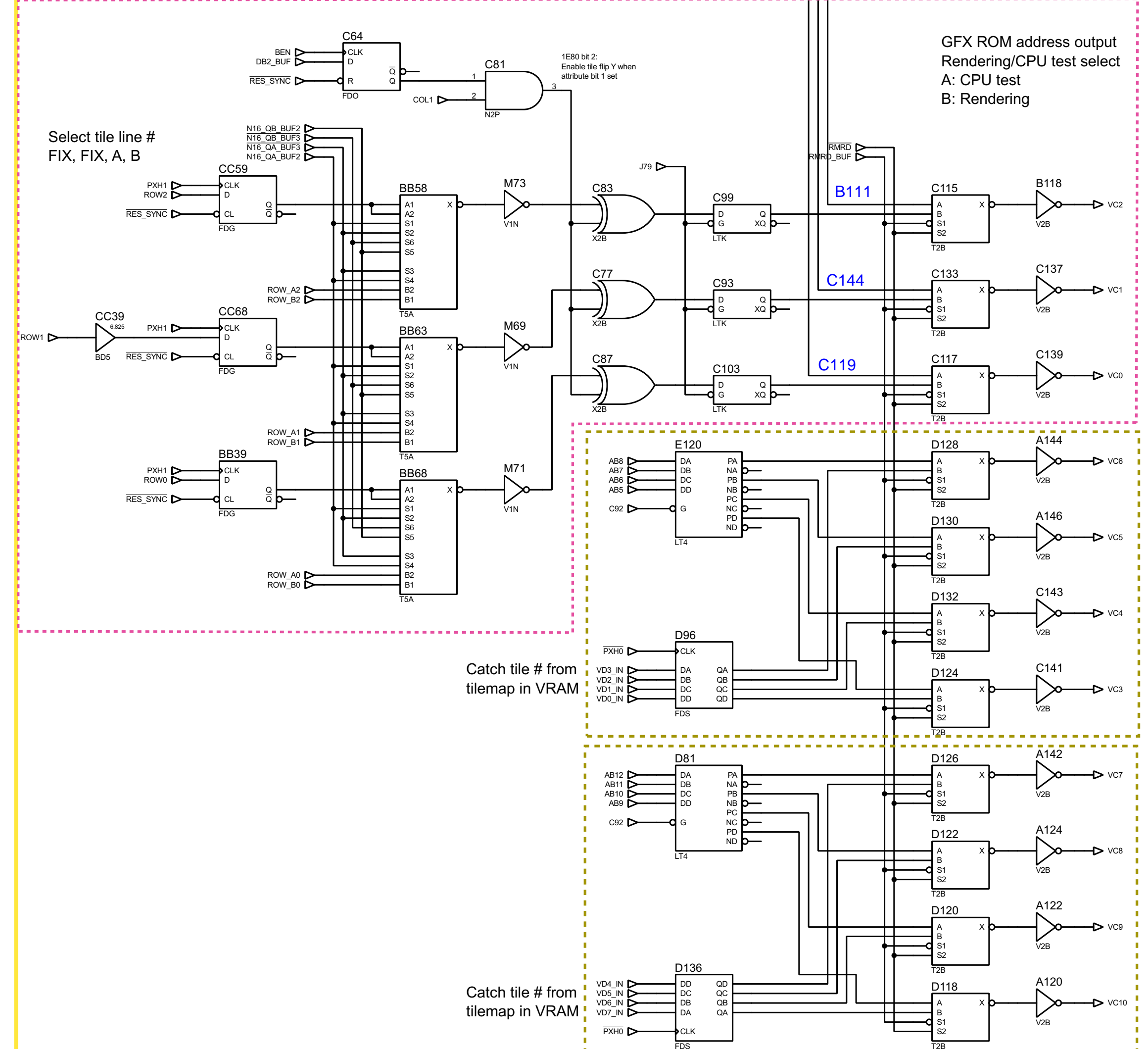
Selection can be simplified using AA38 (and AA38n) only, AA58 always selects 1'b0.





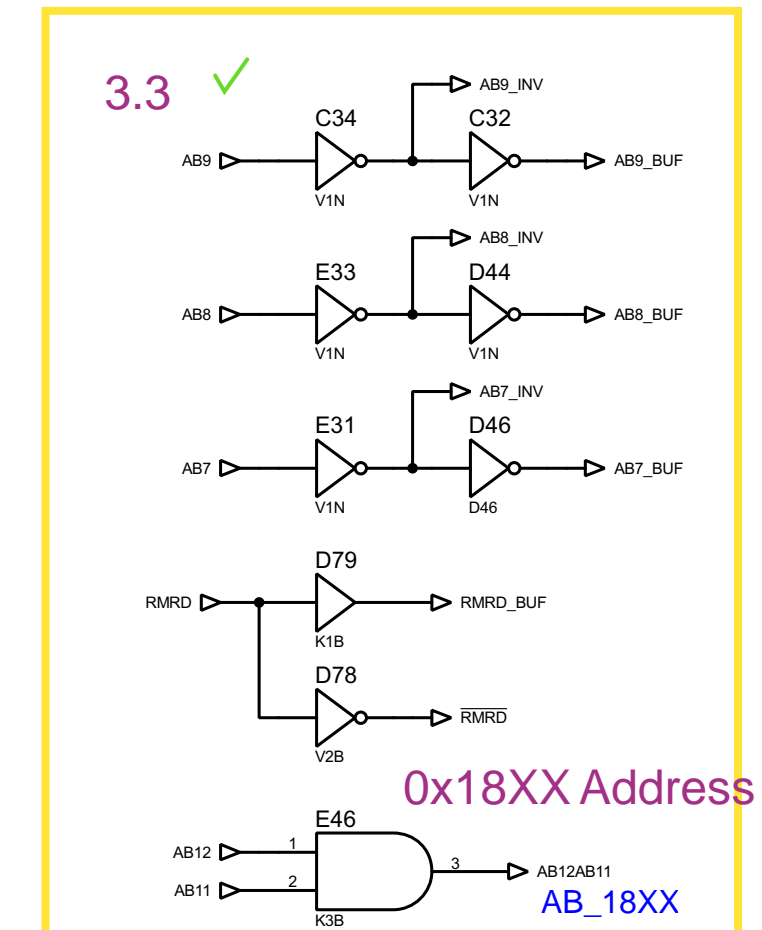
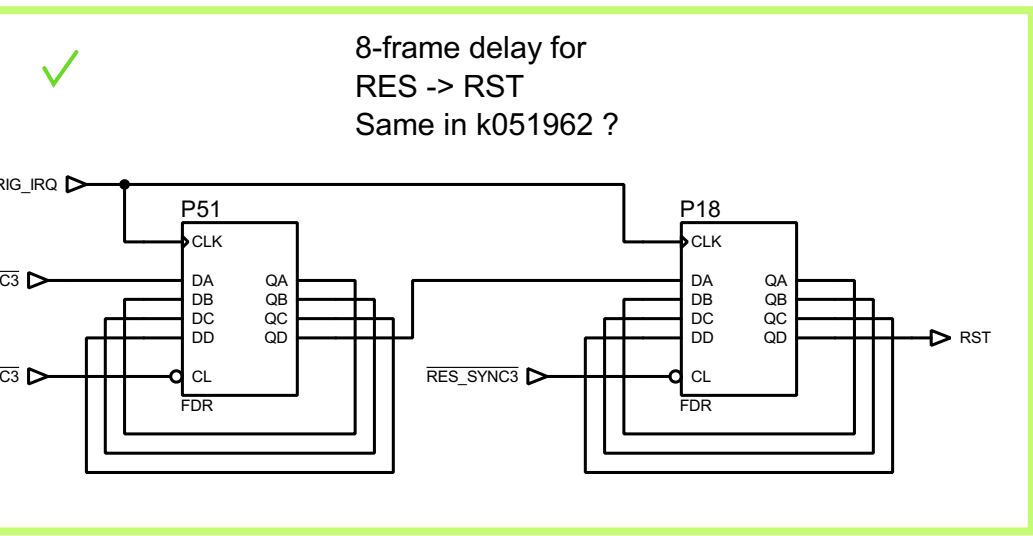
TIMING SIGNALS

SKIP because AB[1:0] used to select byte

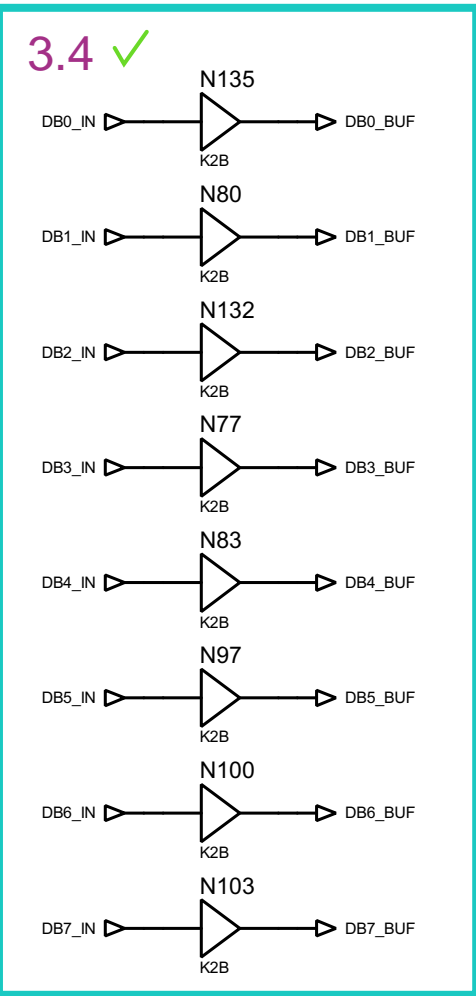


3.1 ✓

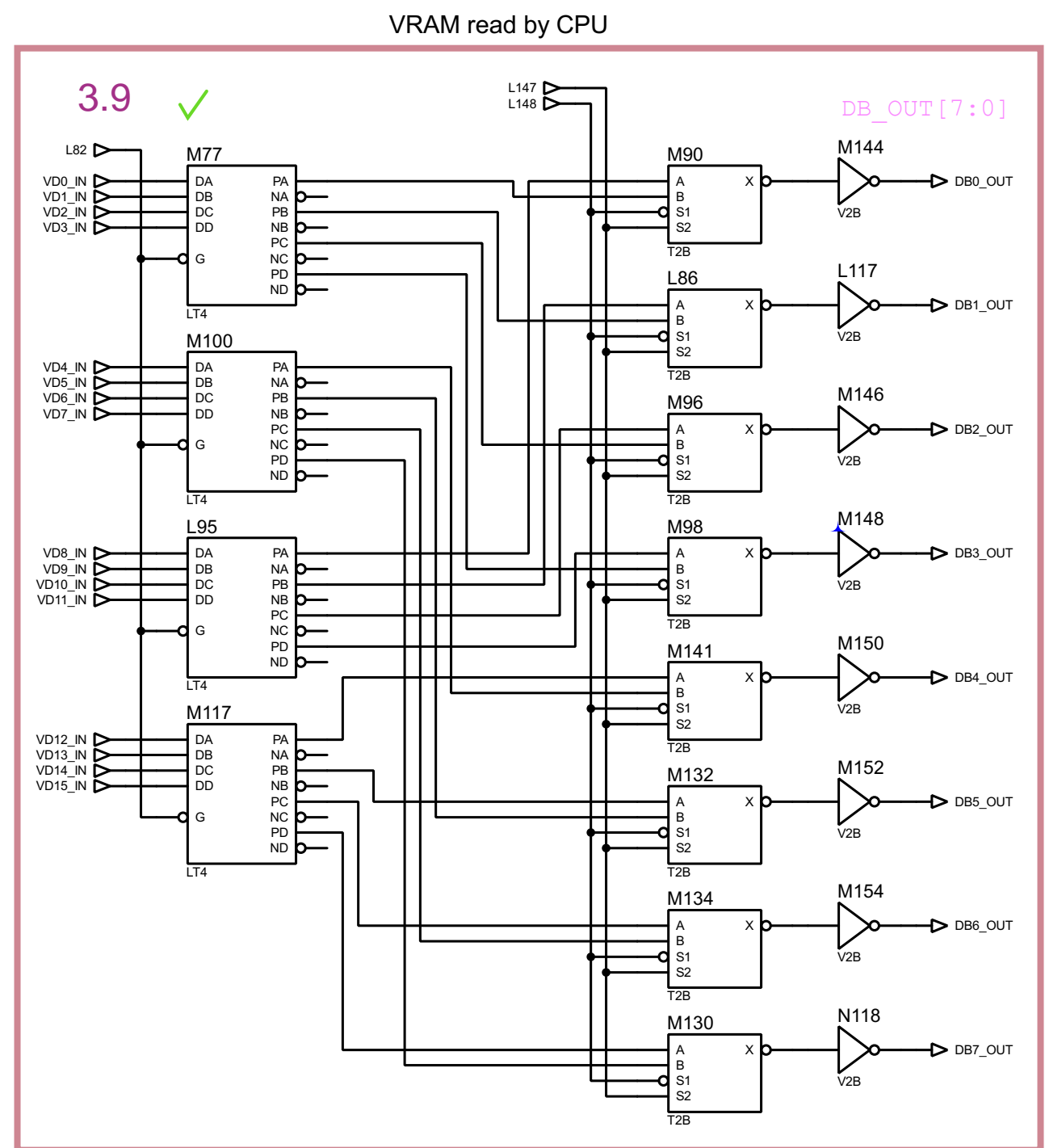
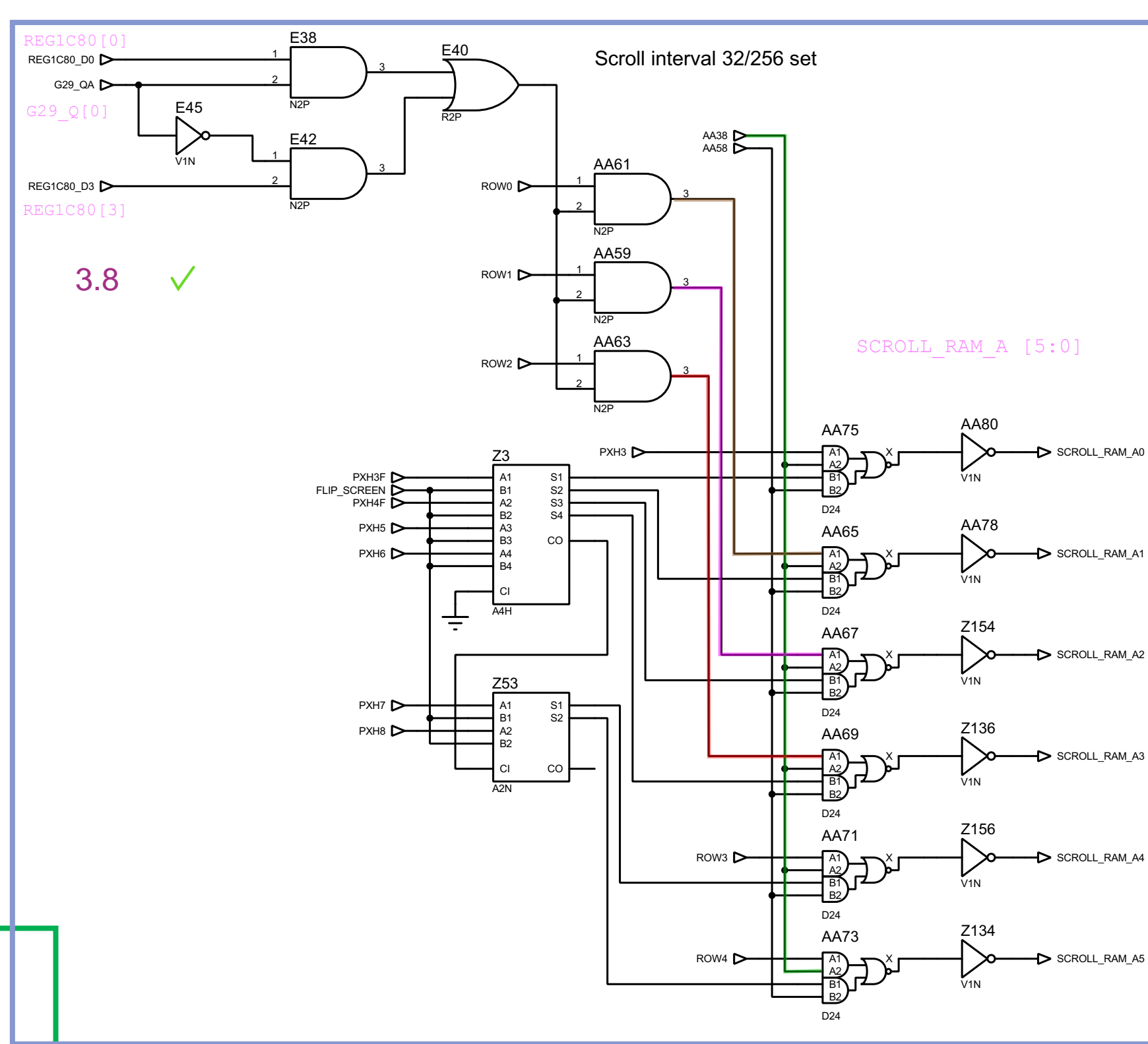
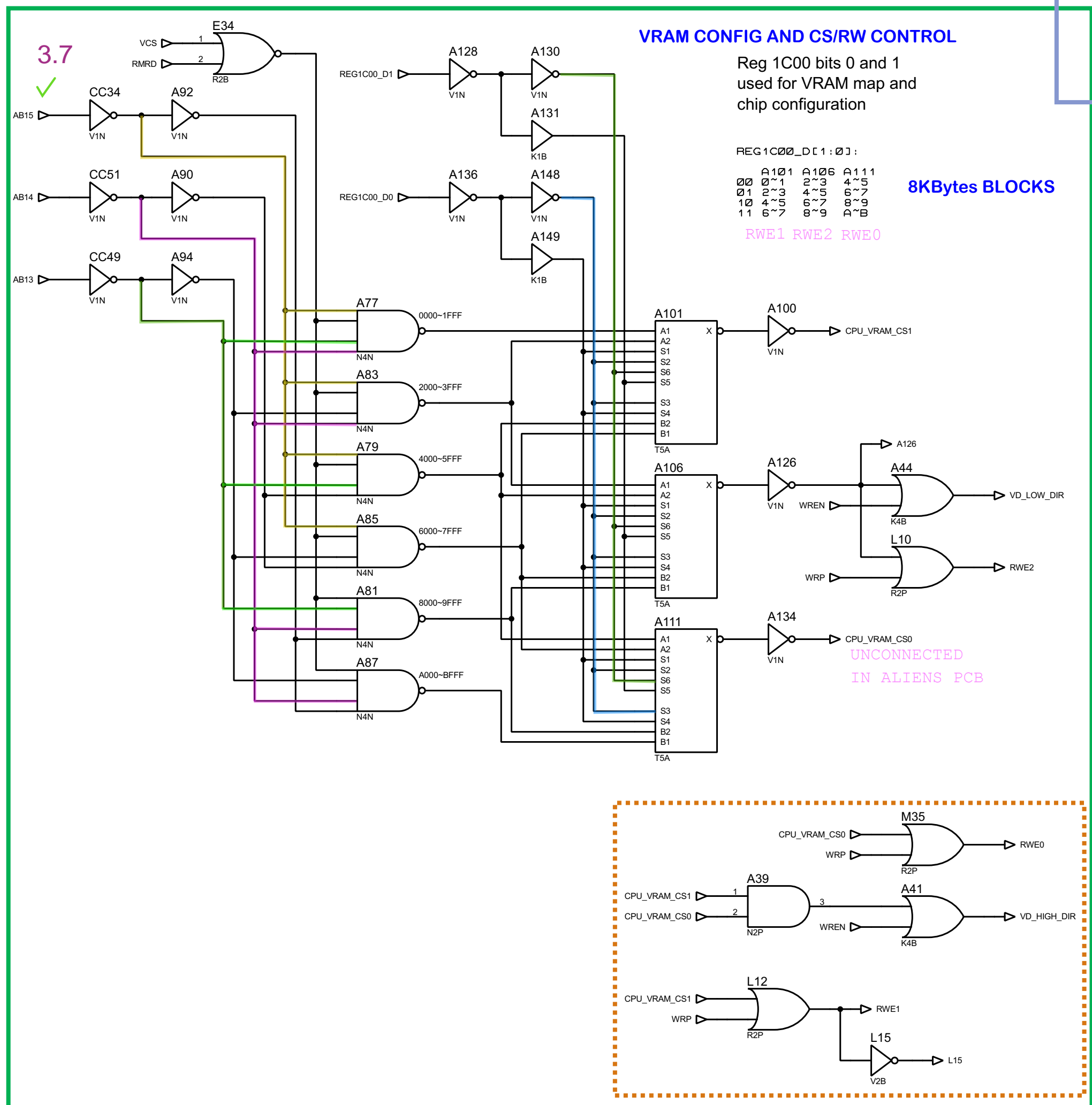
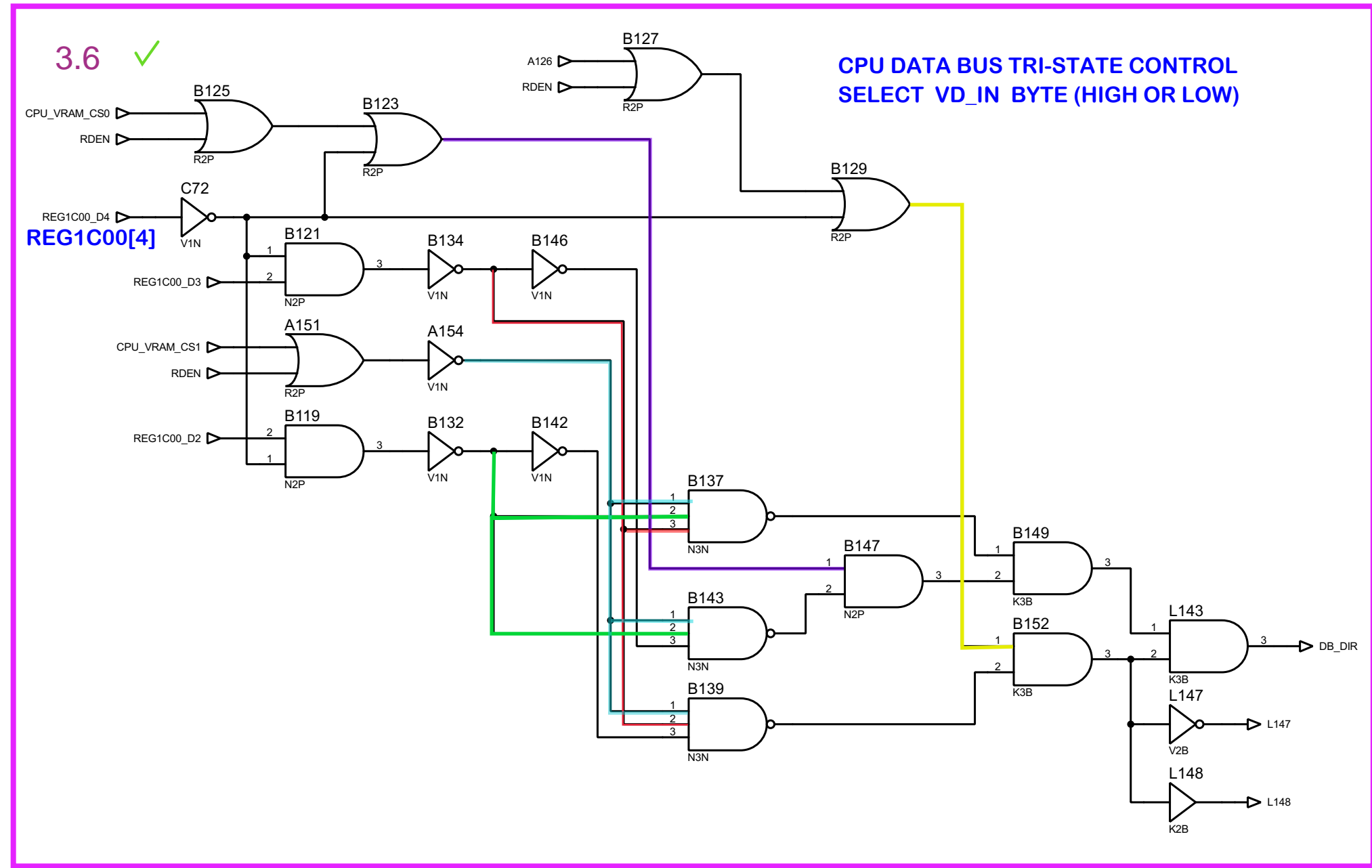
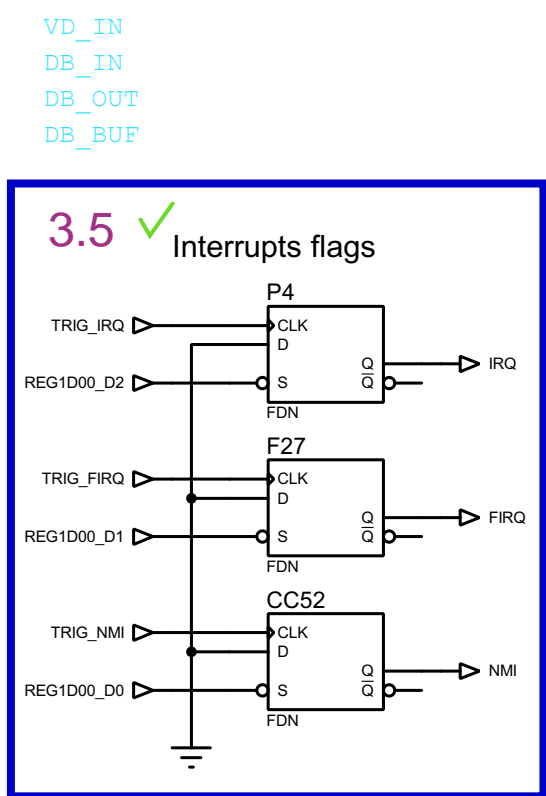
The diagram shows a circuit for a 3-bit counter. It consists of three main components: an N122 flip-flop, an M74 3-to-2 line decoder, and an H12 2-to-1 line multiplexer. The N122 flip-flop has inputs M04 (CLK), V02 (D), and RES (CL), and an output Q. The M74 decoder has a 3-bit input (Q, Q-bar, Q-bar-bar) and two 2-bit outputs, RES_SYNC and RES_SYNC2. The H12 multiplexer has two 2-bit inputs (RES_SYNC and RES_SYNC2) and a 2-bit output (RES_SYNC2).



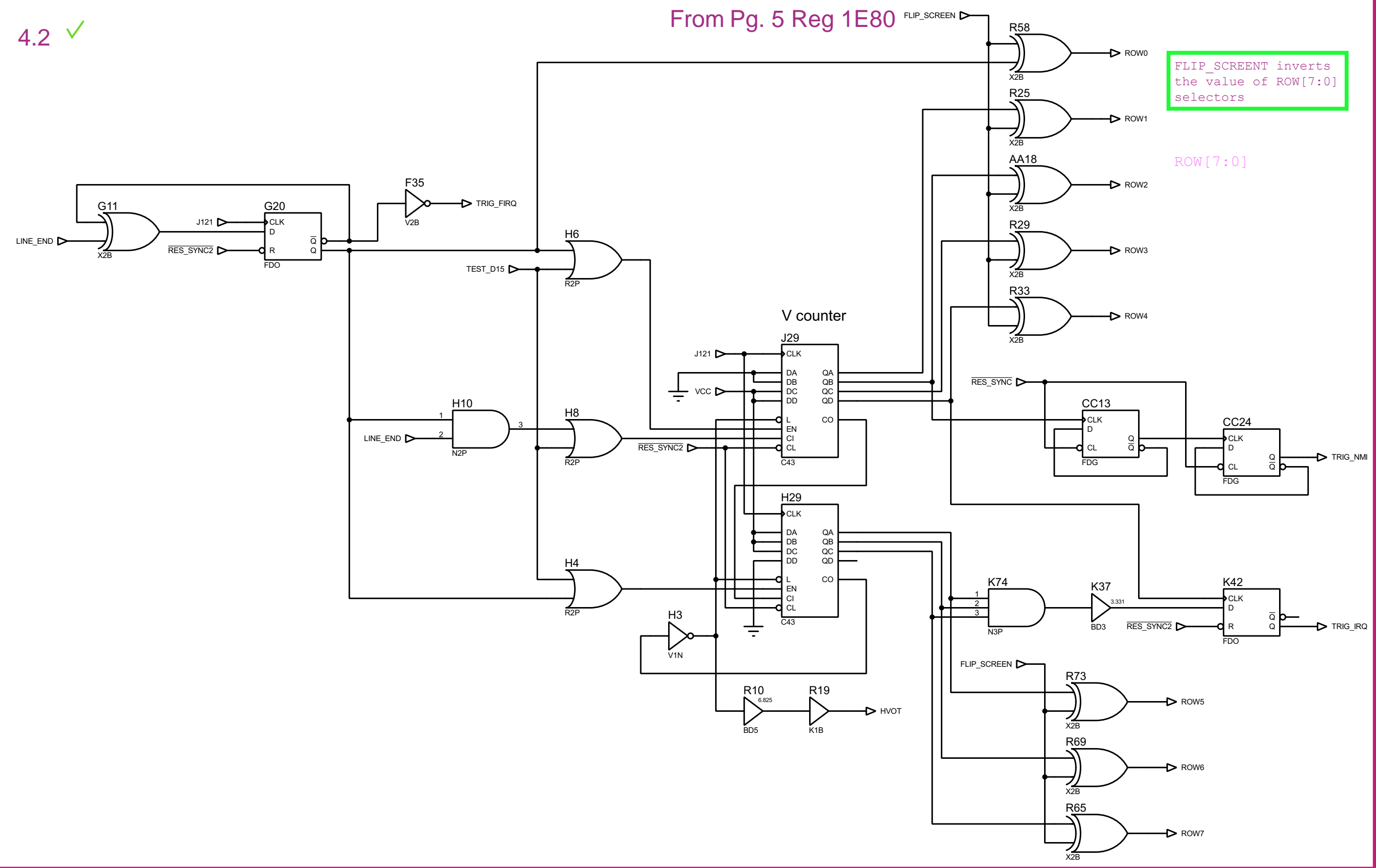
A diagram showing two triangles. The top triangle is oriented with its base on the left and its vertex on the right. A horizontal dashed line extends from the left base to the vertex, and another horizontal dashed line extends from the right vertex to the right. The bottom triangle is oriented with its base on the left and its vertex on the right. A horizontal dashed line extends from the left base to the vertex, and another horizontal dashed line extends from the right vertex to the right. A small circle is located below the bottom triangle.



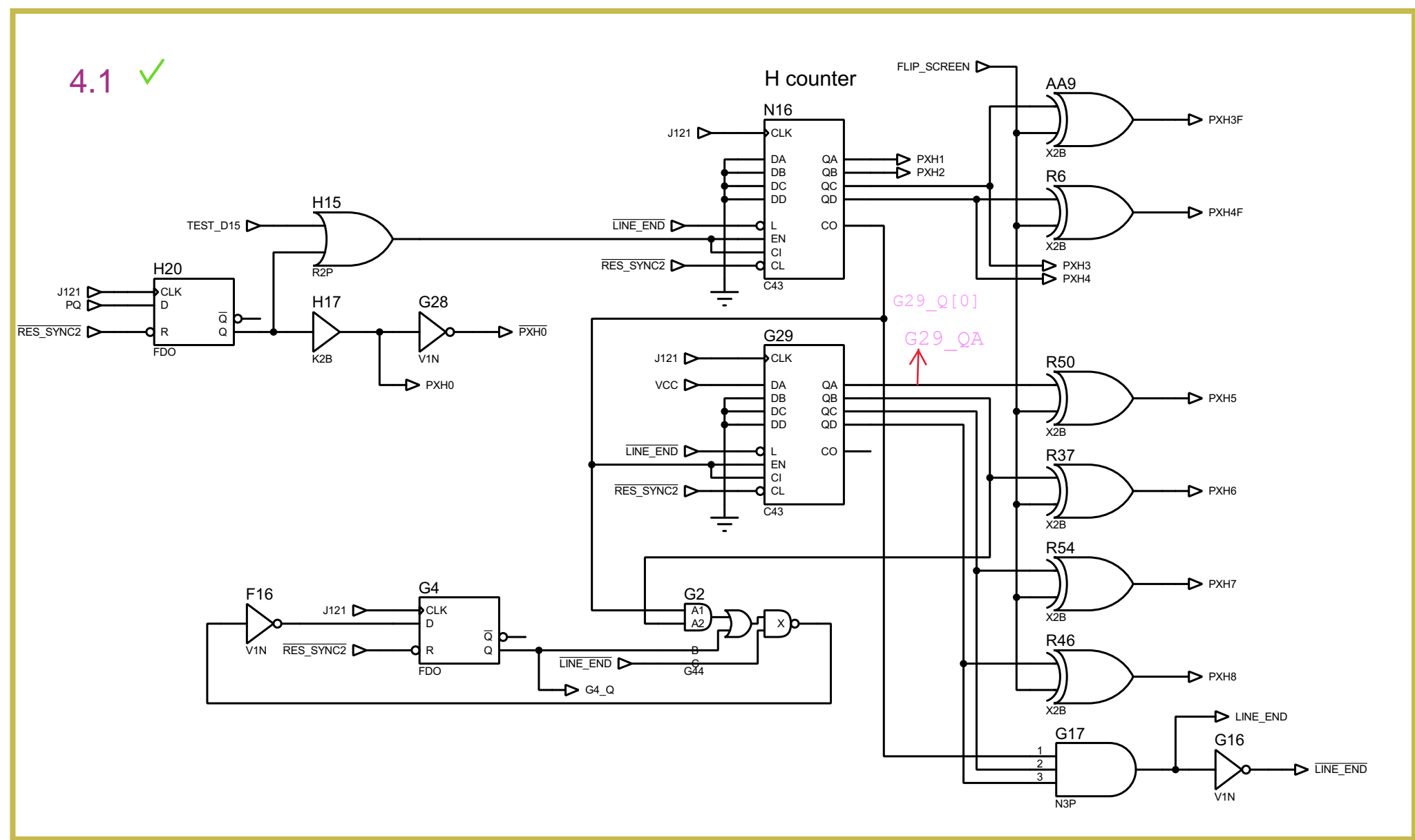
```
wire [7:0] DB_BUF
```



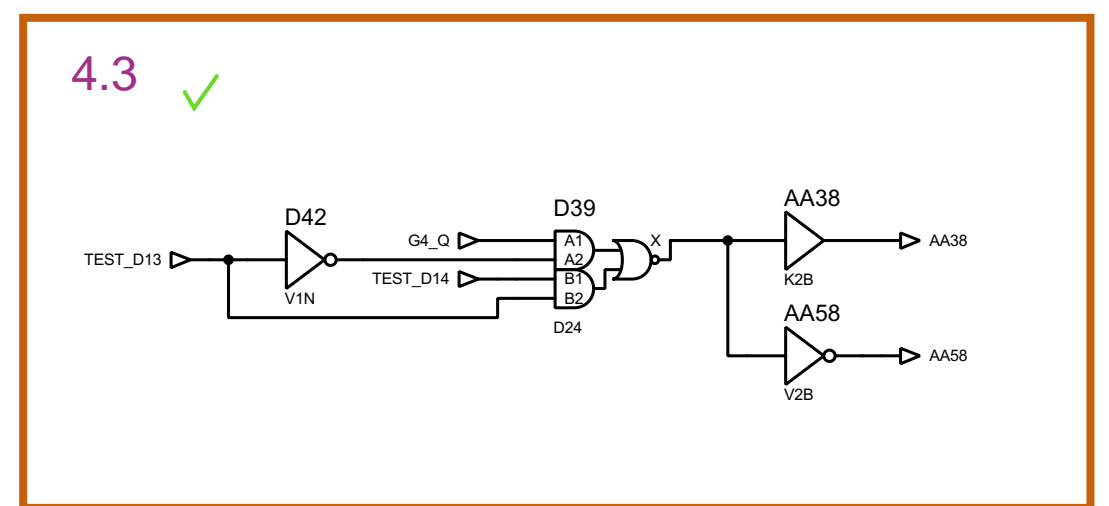
4.2 ✓



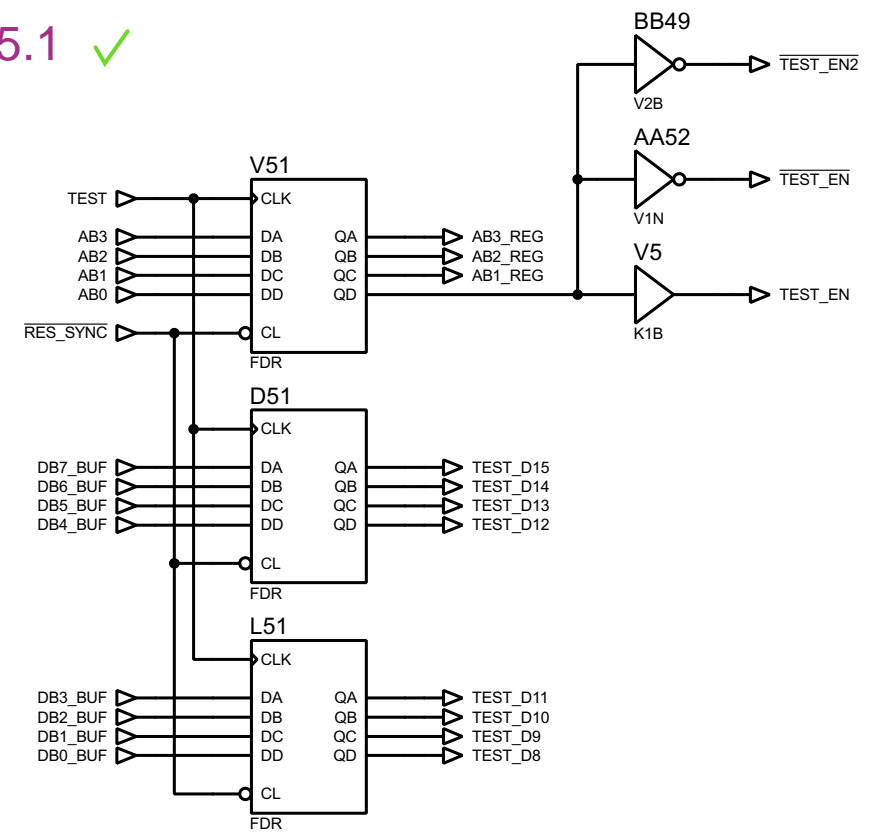
4.1 ✓



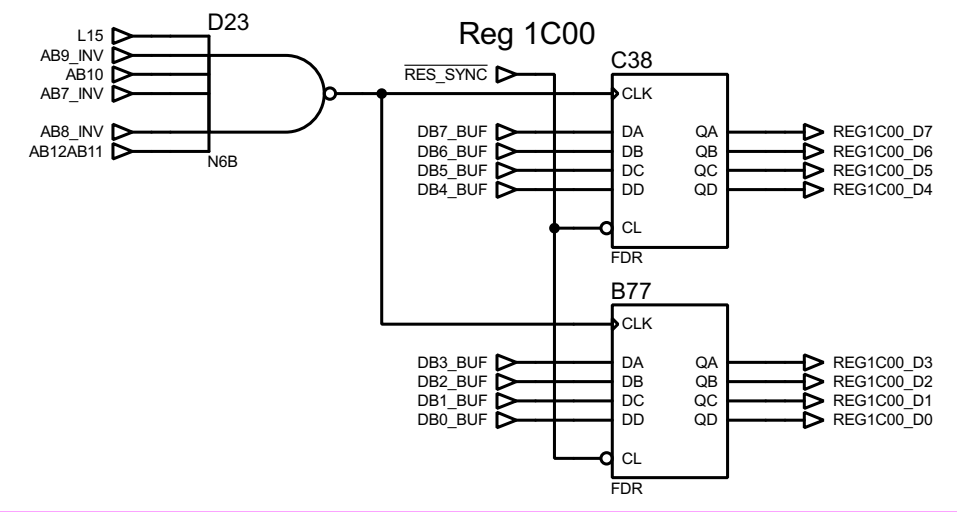
4.3 ✓



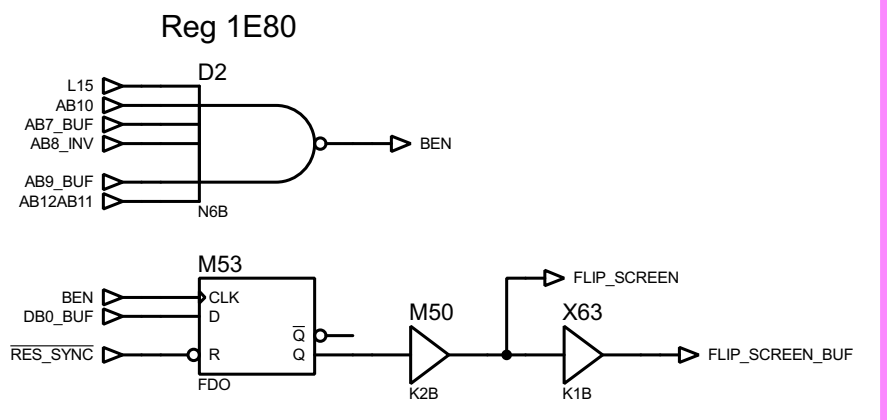
5.1 ✓



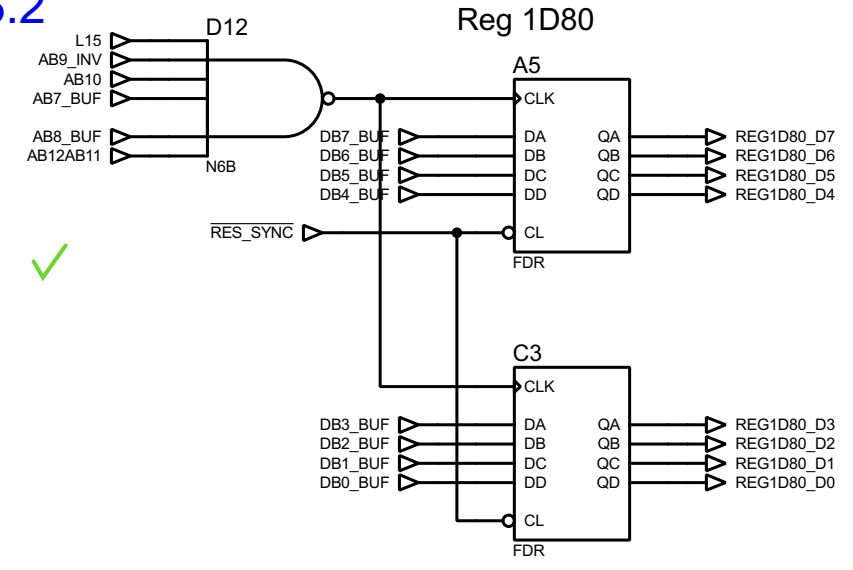
5.4 ✓



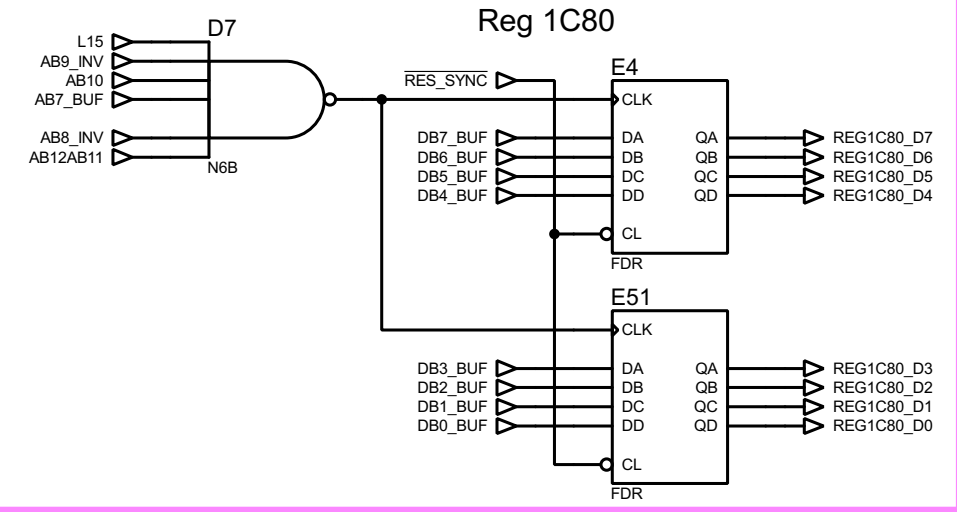
5.7 ✓



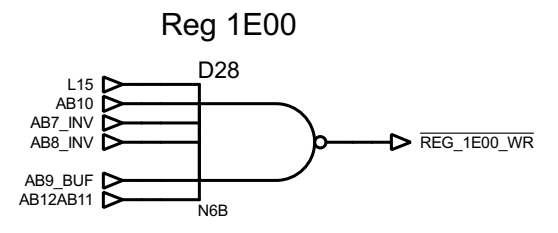
5.2 ✓



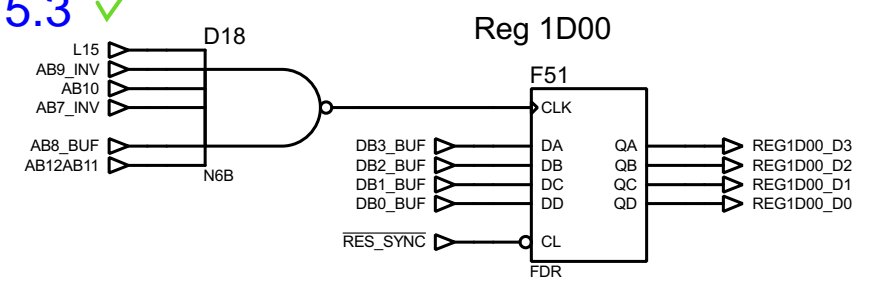
5.5 ✓



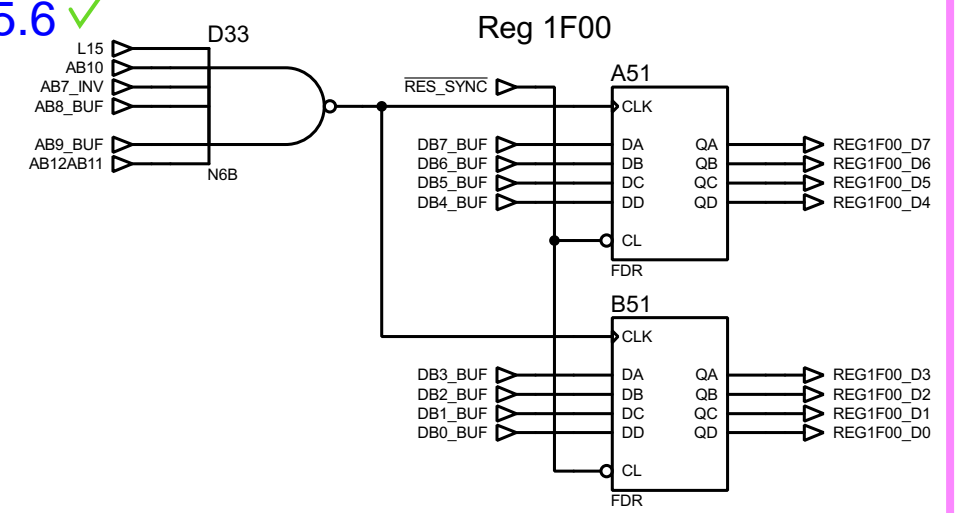
5.8 ✓



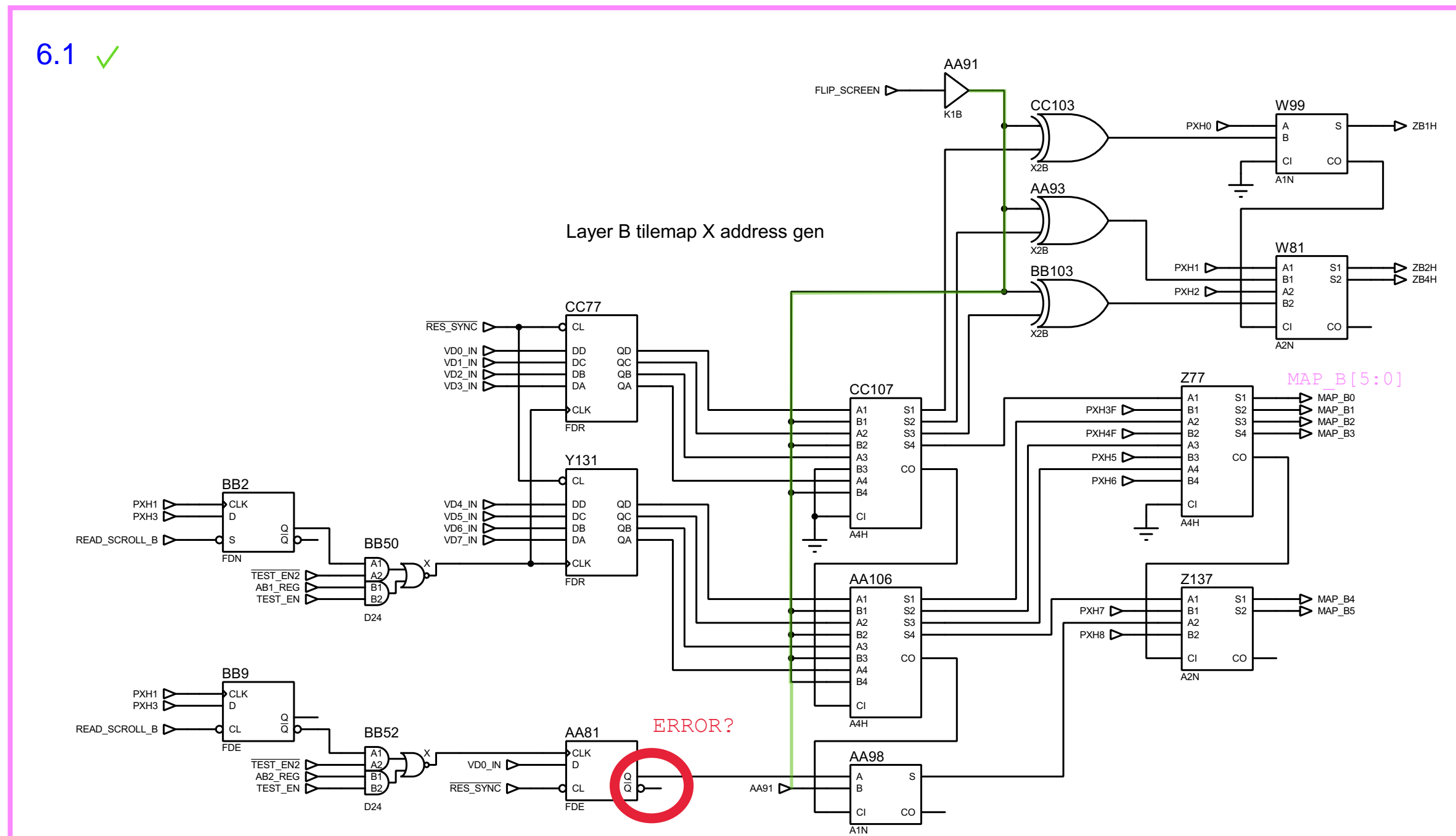
5.3 ✓



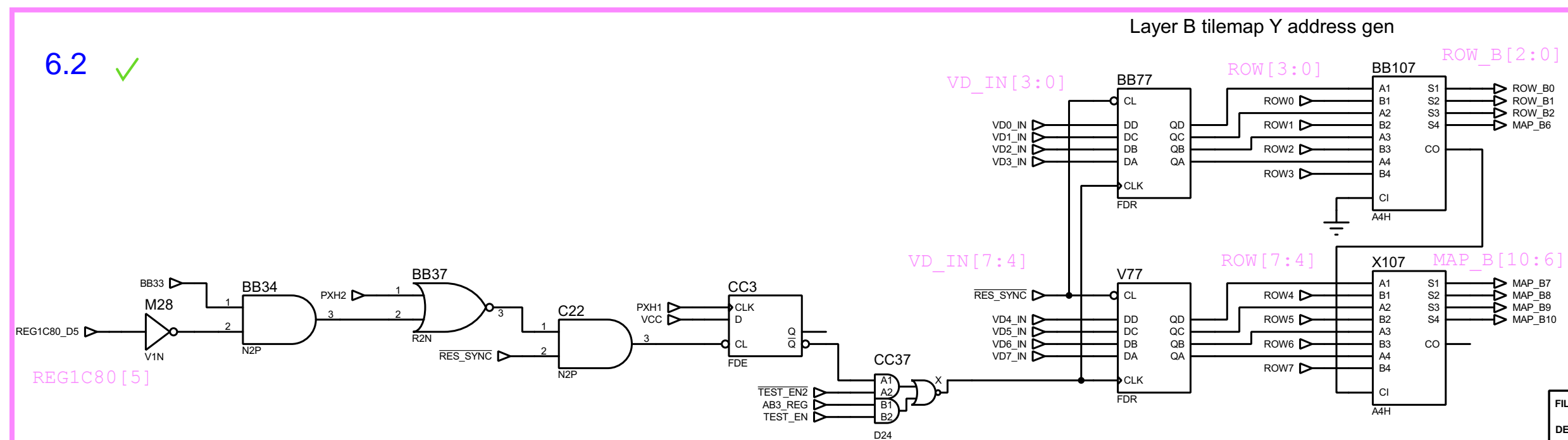
5.6 ✓



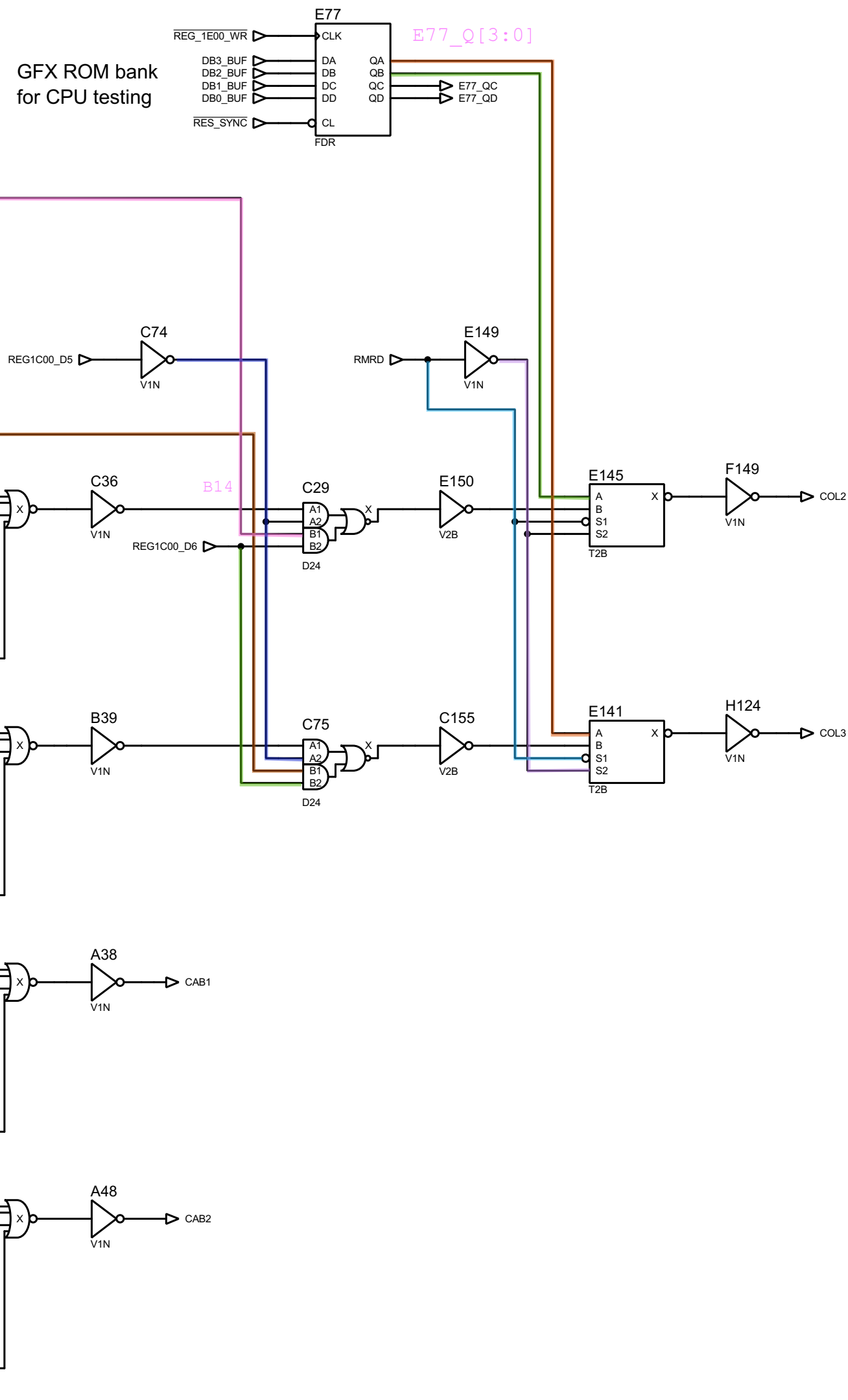
6.1 ✓



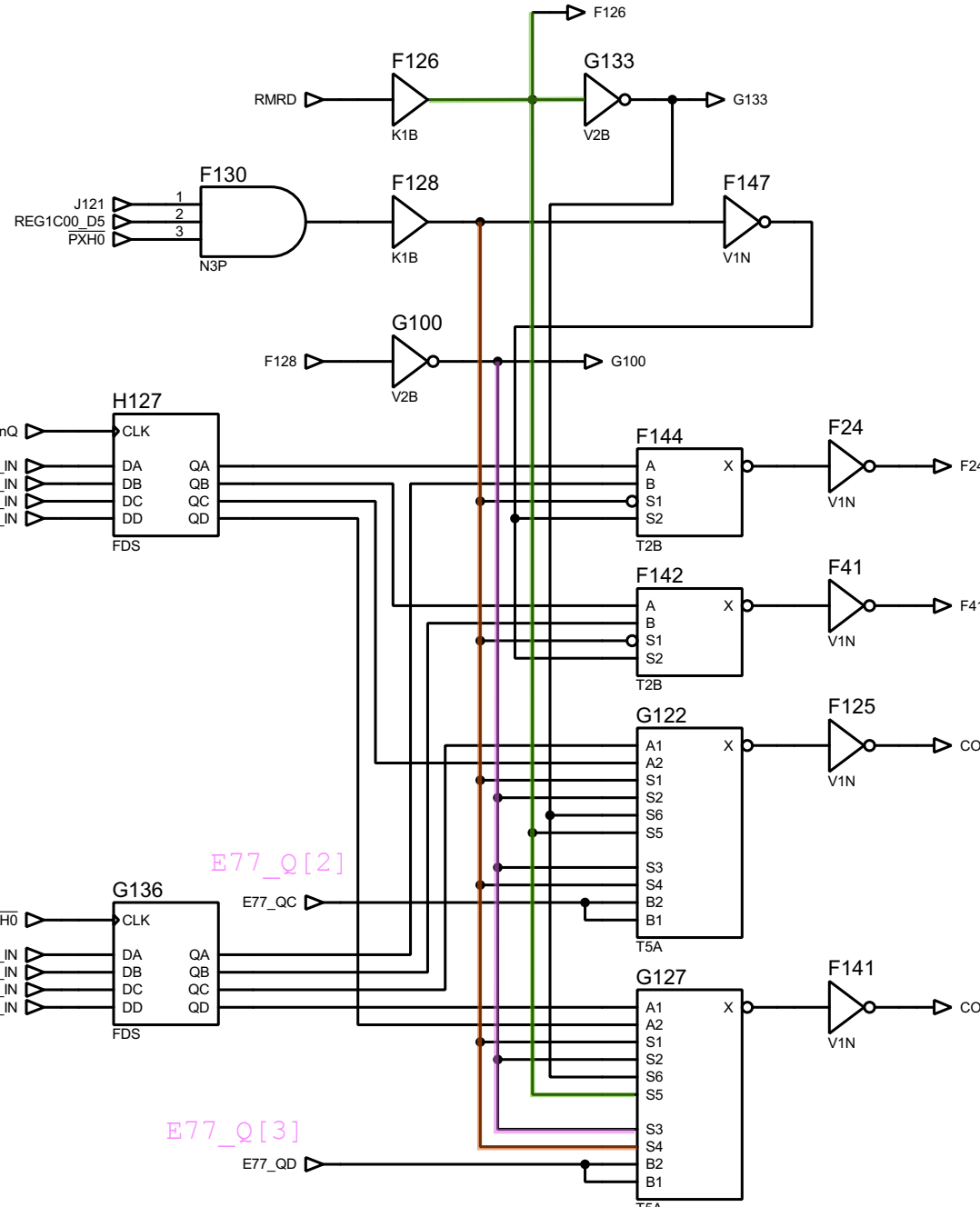
6.2 ✓



7.2

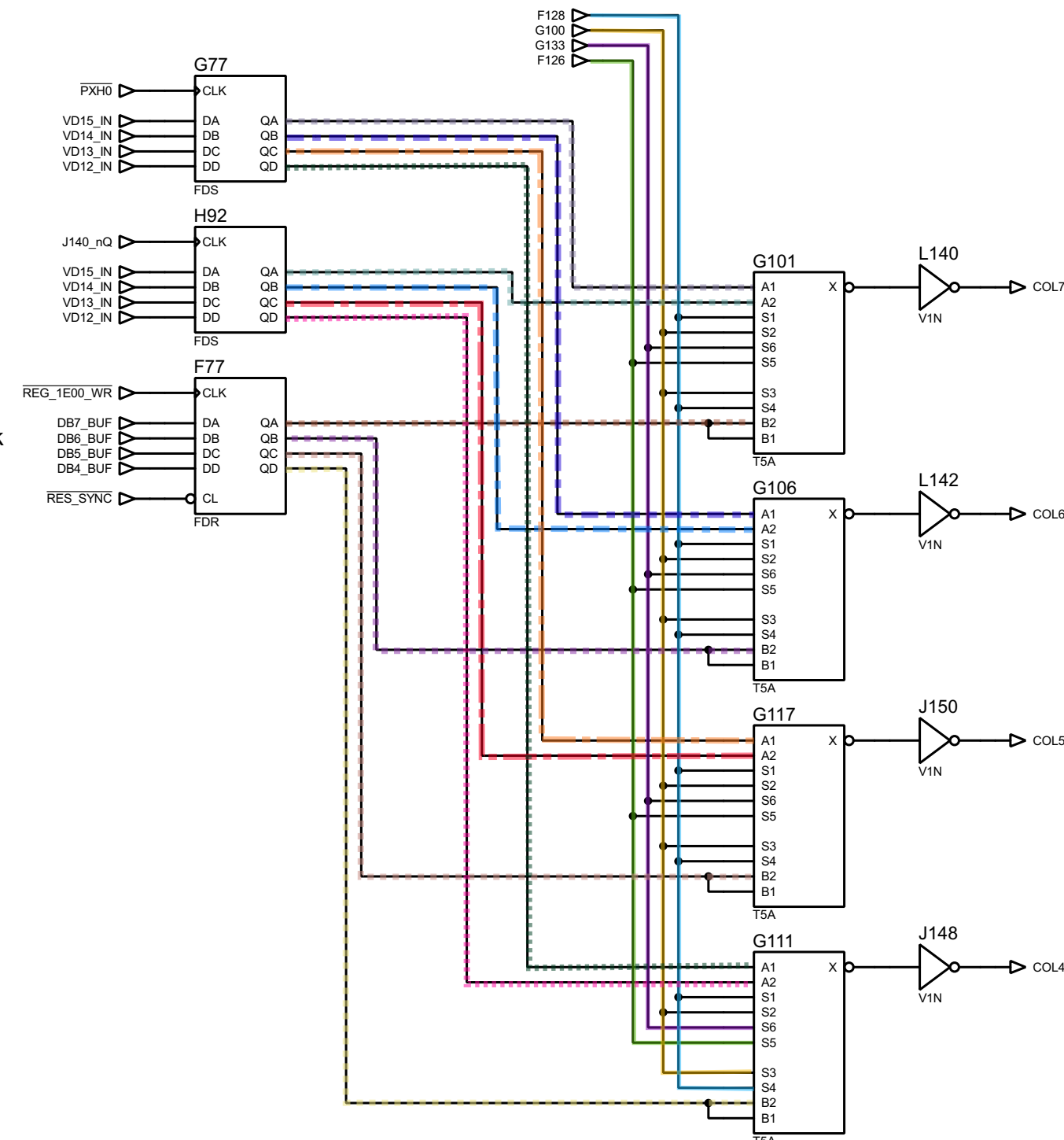


7.1

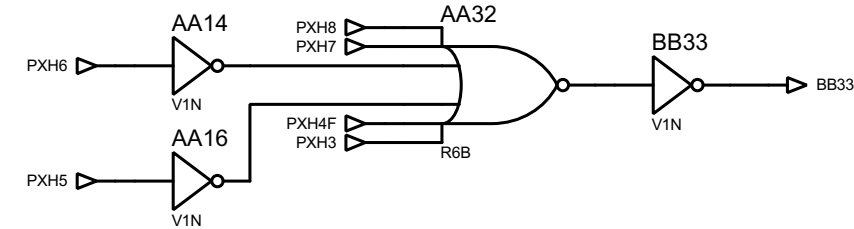


7.3

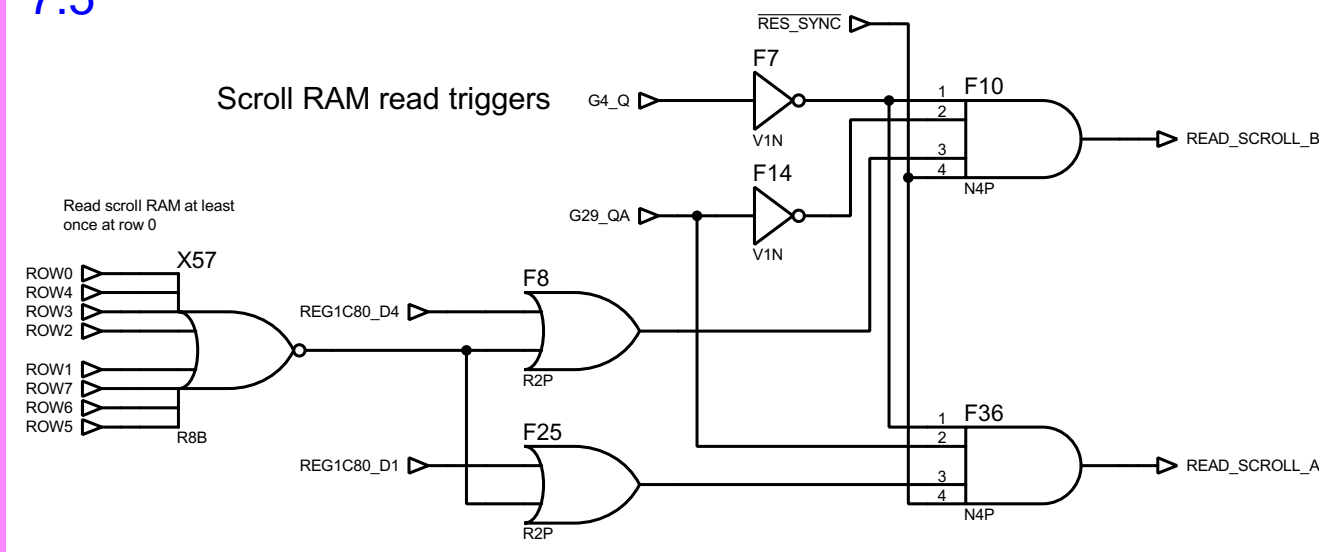
GFX ROM bank for CPU testing



7.4

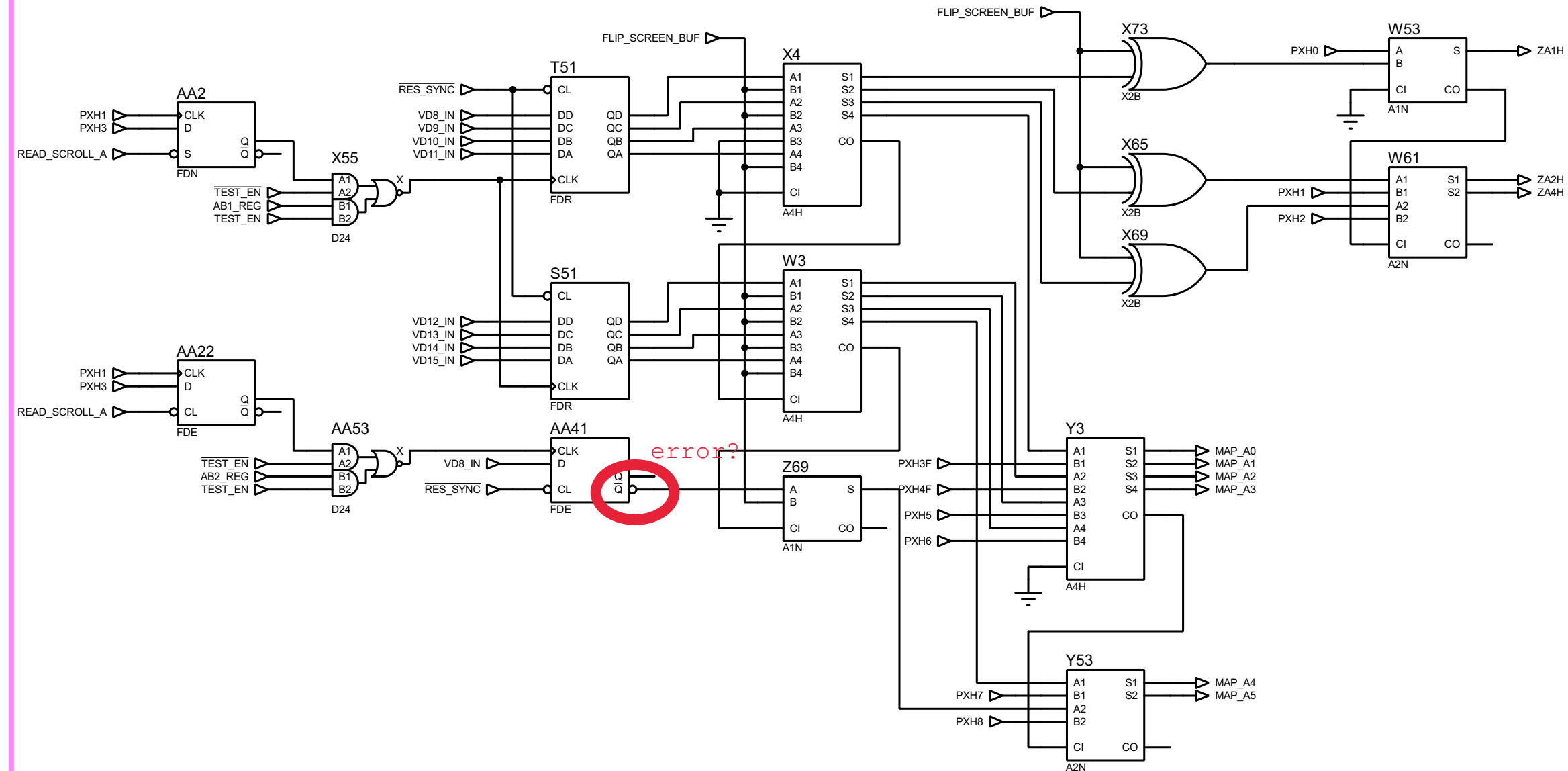


7.5



8.1 ✓

Layer A tilemap X address gen



8.2 ✓

Layer A tilemap Y address gen

