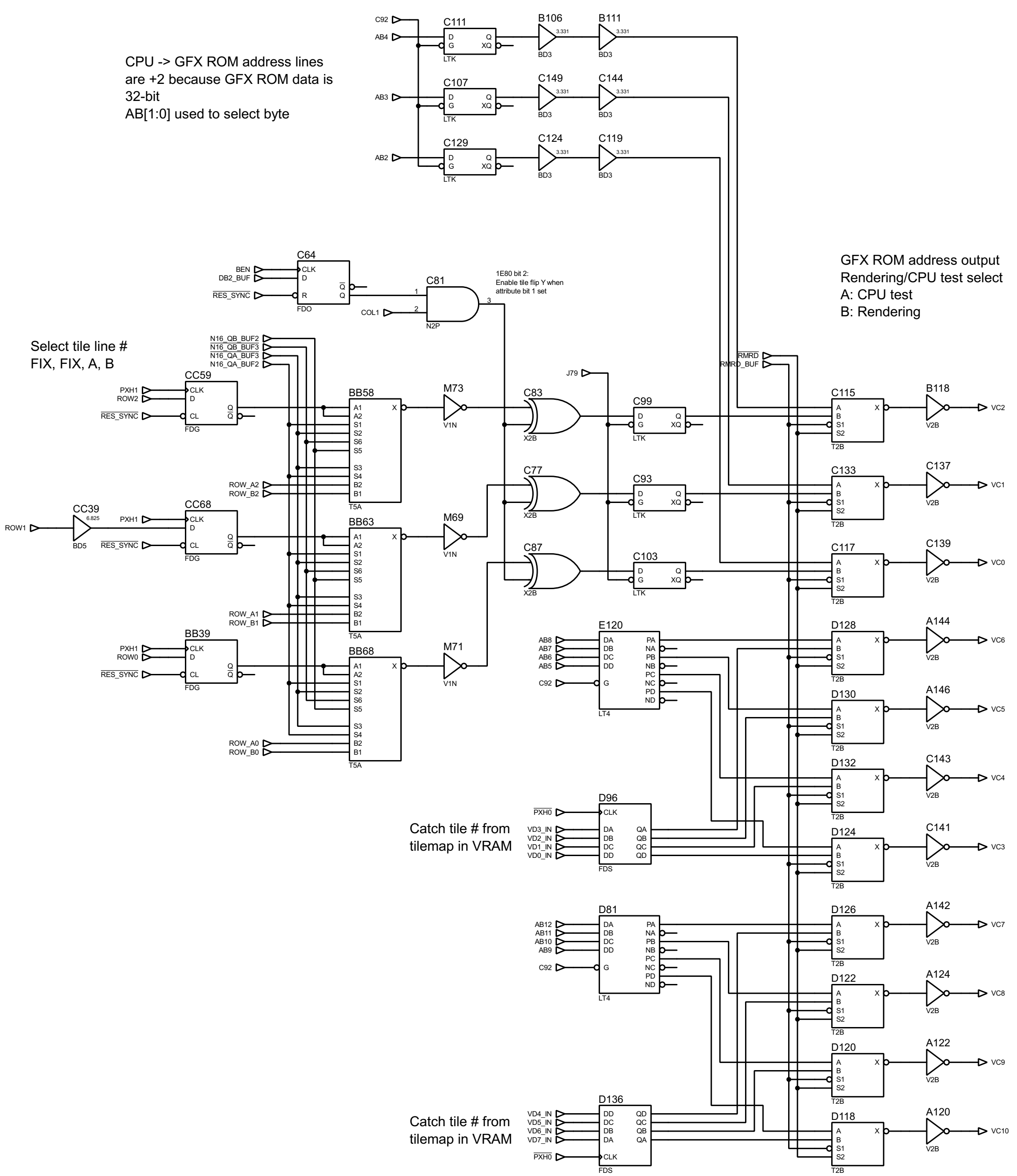
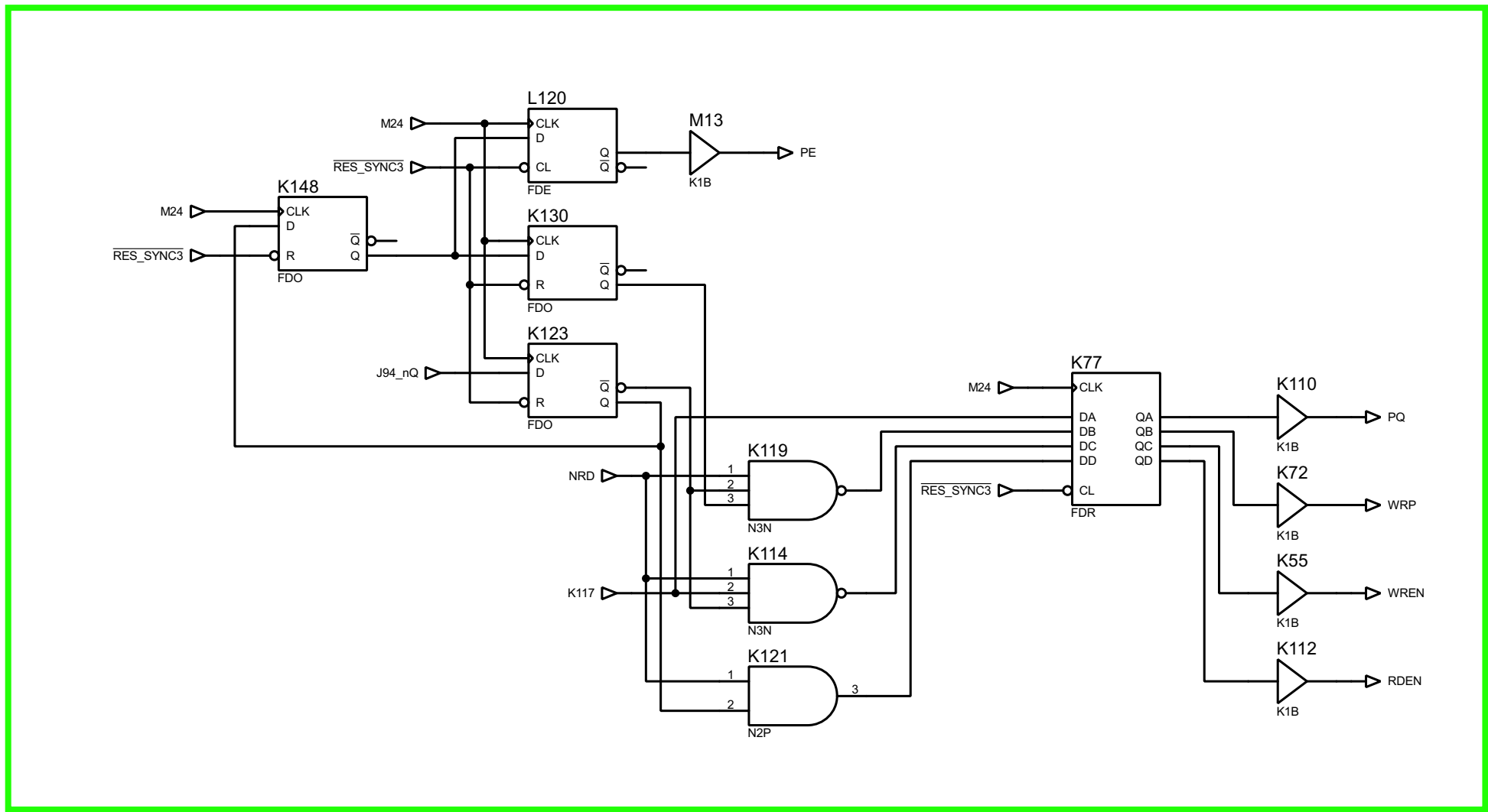
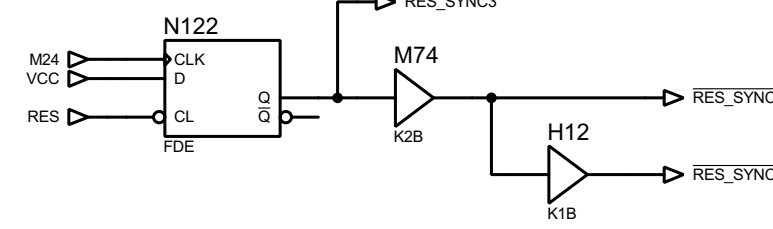


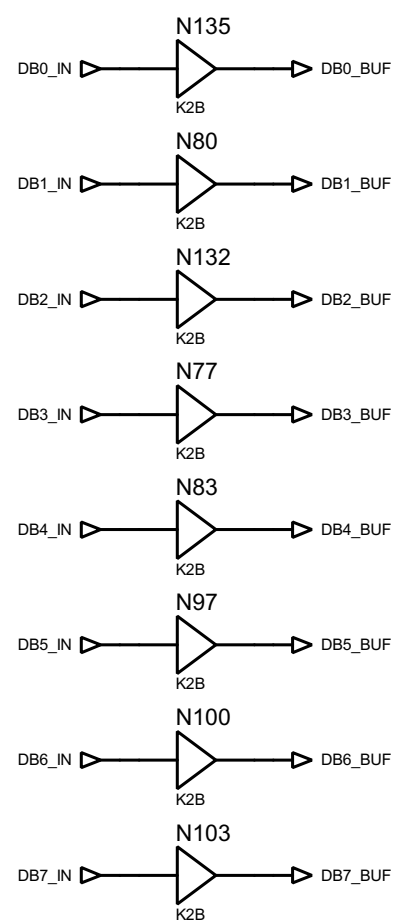
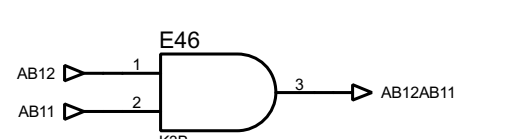
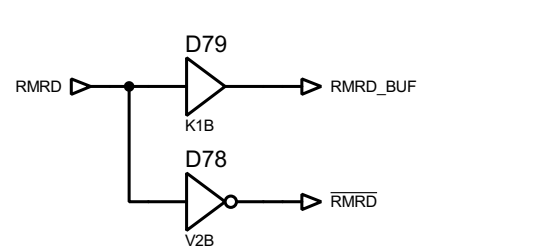
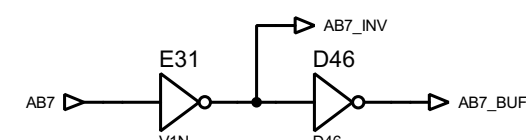
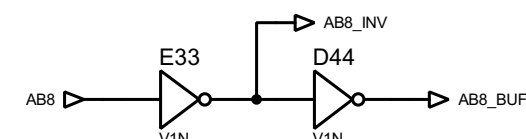
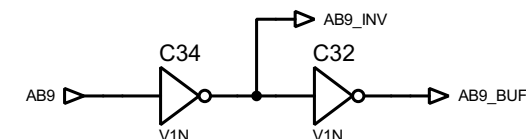
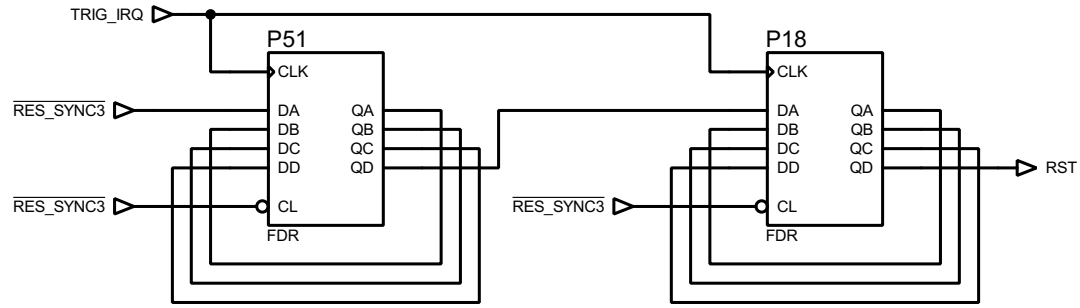
TIMING SIGNALS



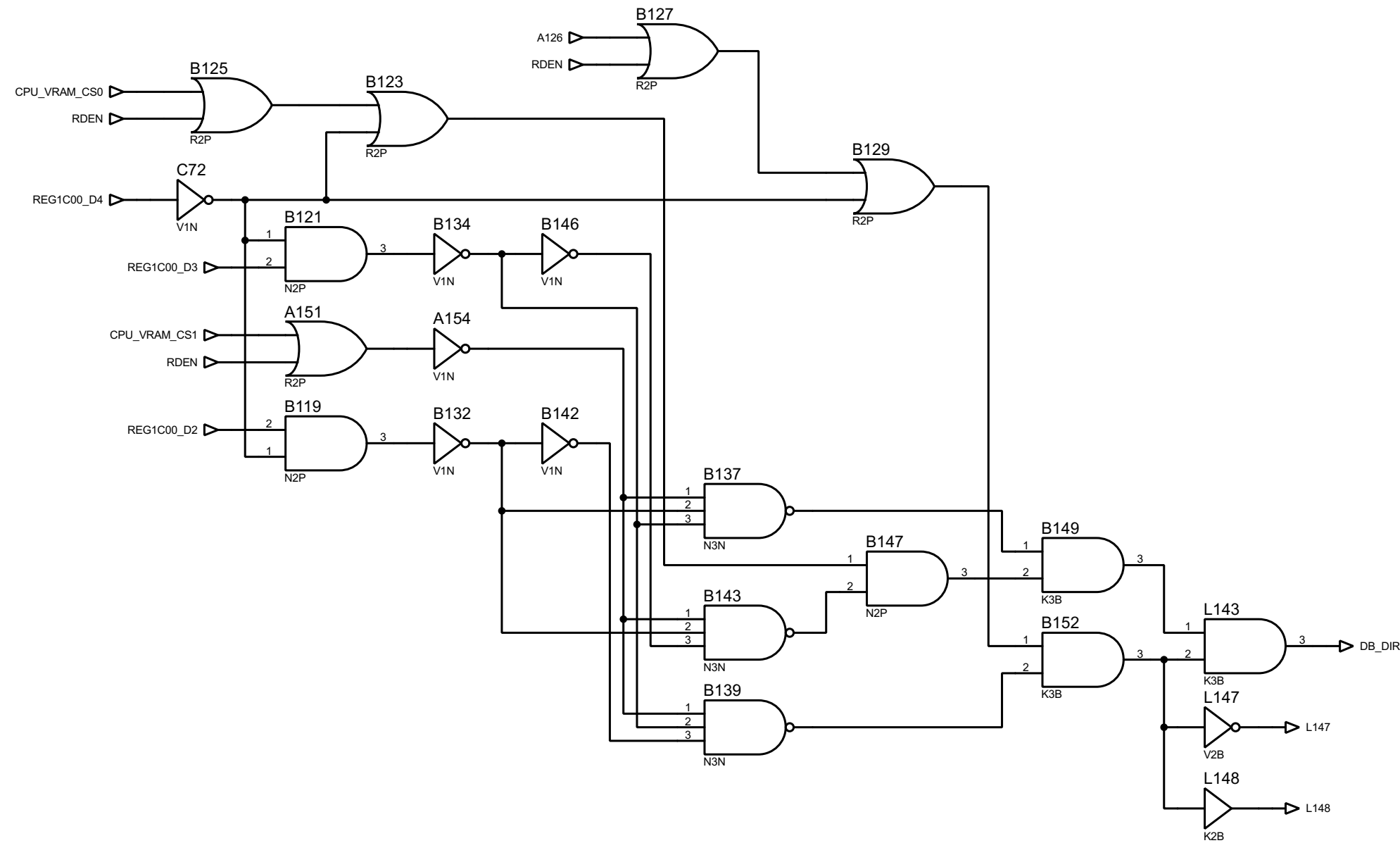
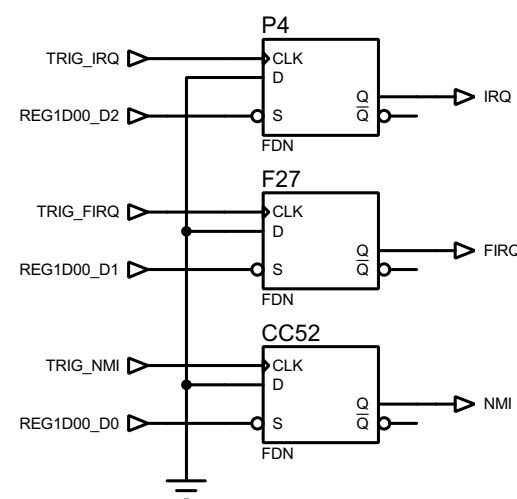
RES_SYNC signals generator



8-frame delay for RES -> RST Same in k051962 ?



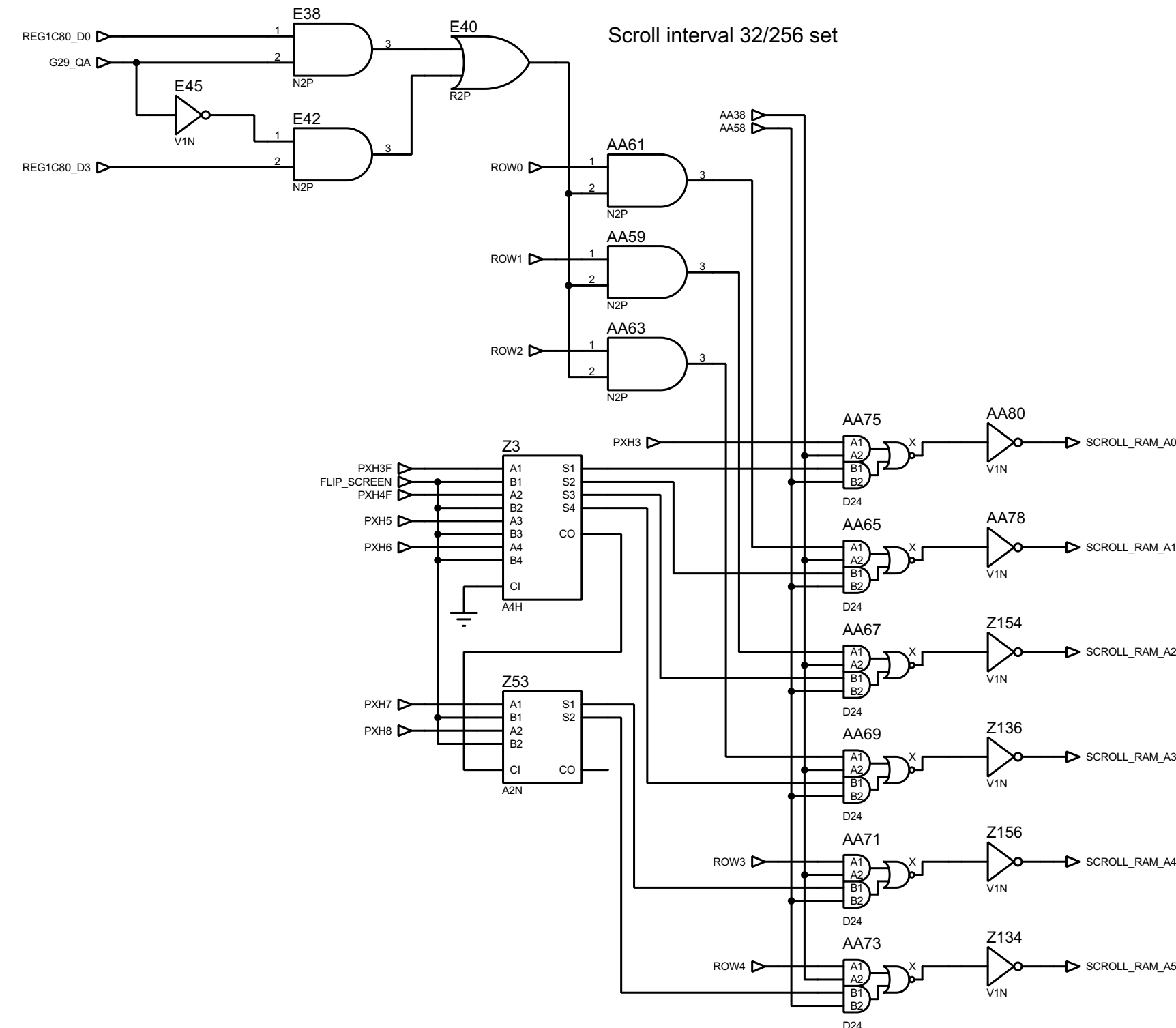
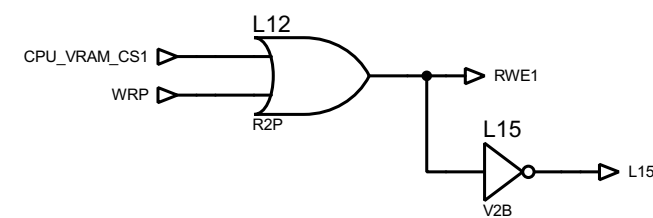
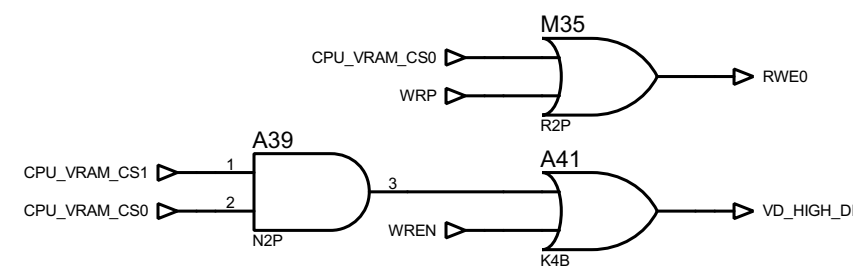
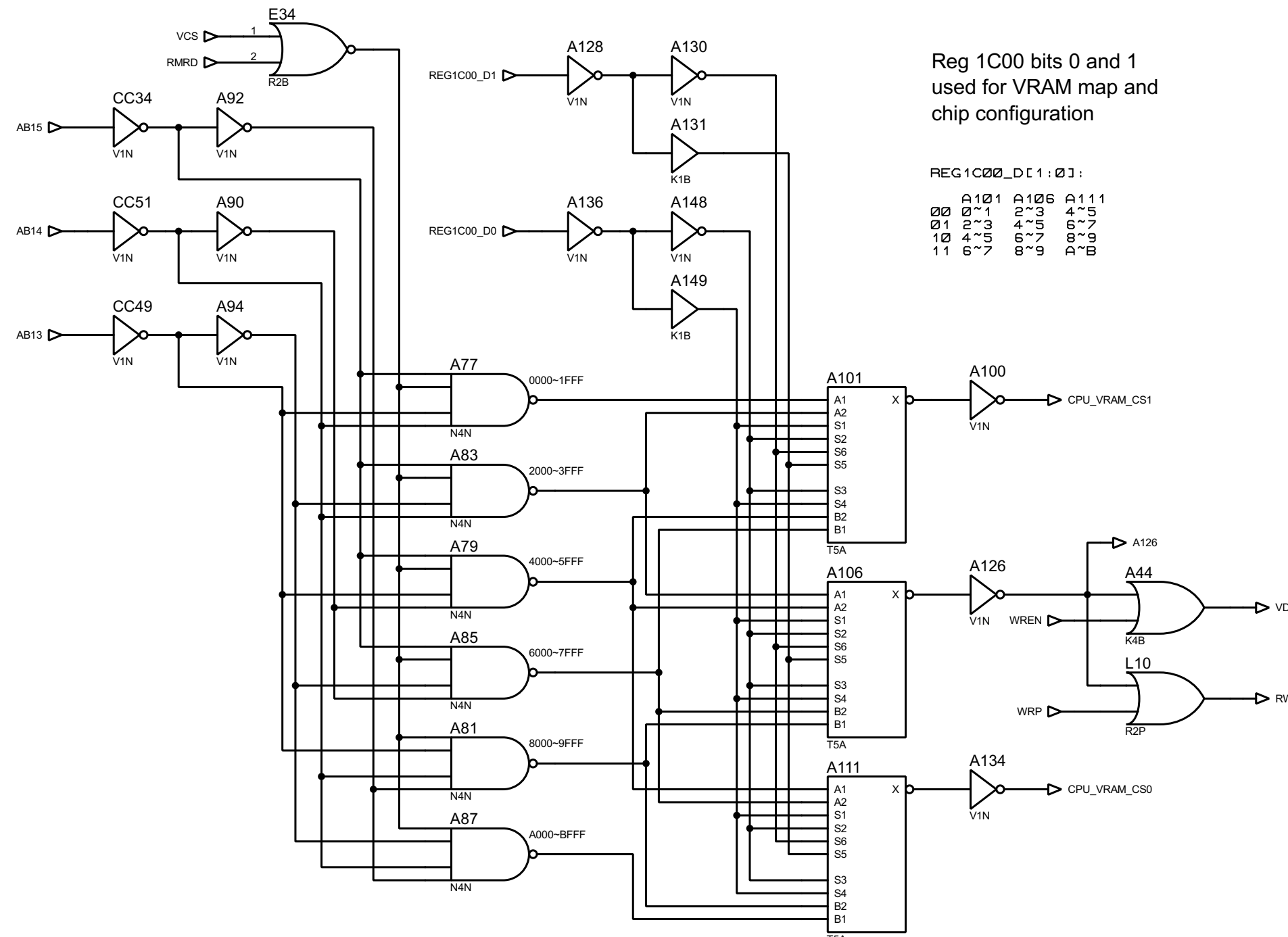
Interrupts flags



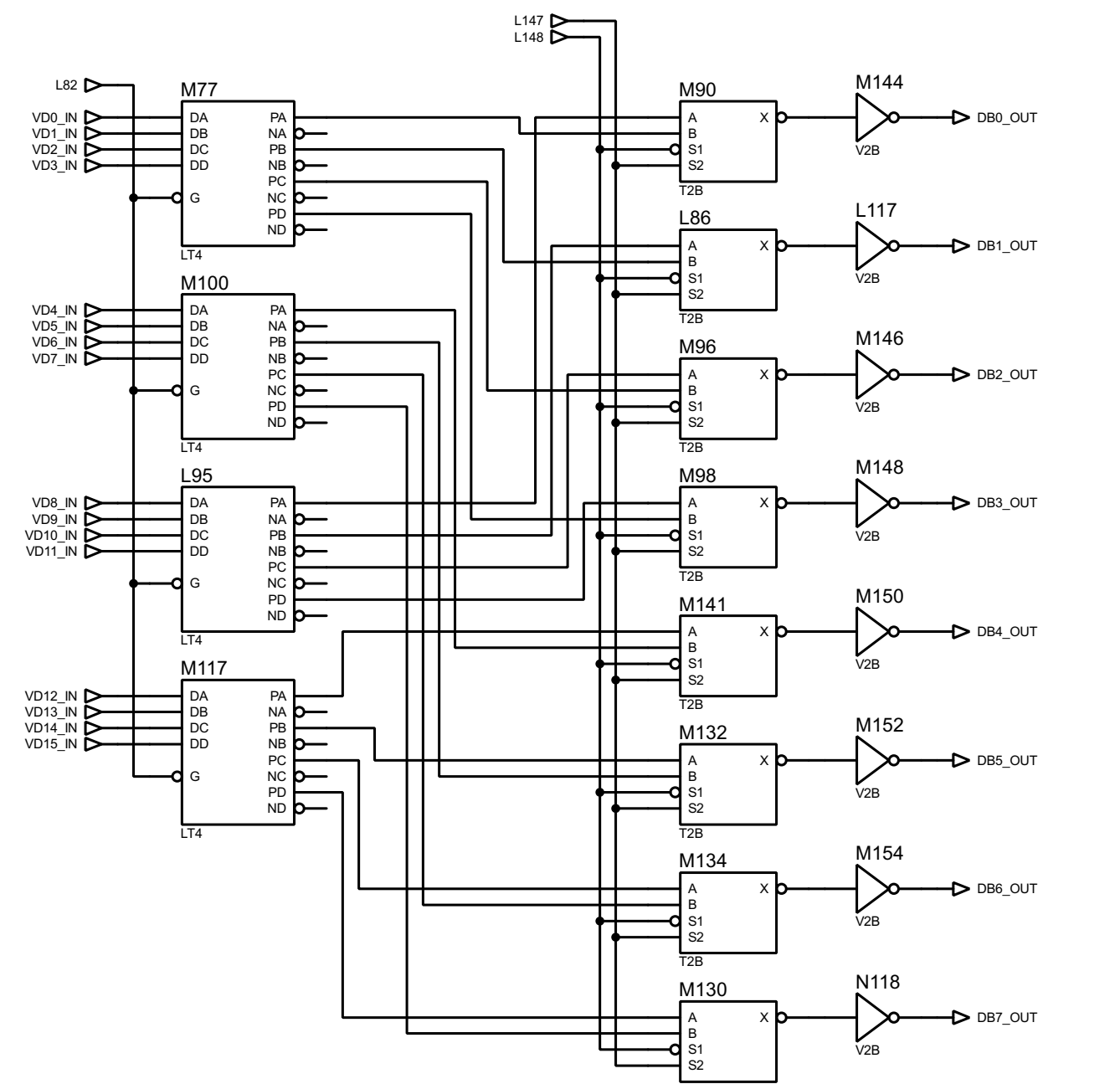
Reg 1C00 bits 0 and 1 used for VRAM map and chip configuration

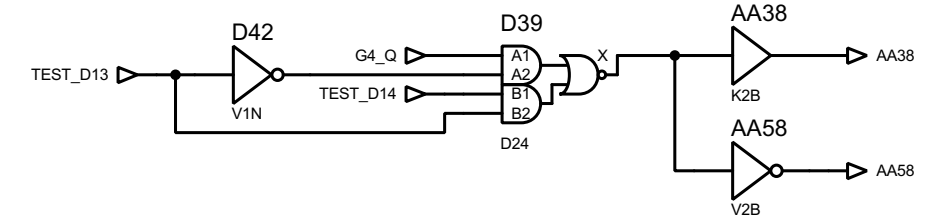
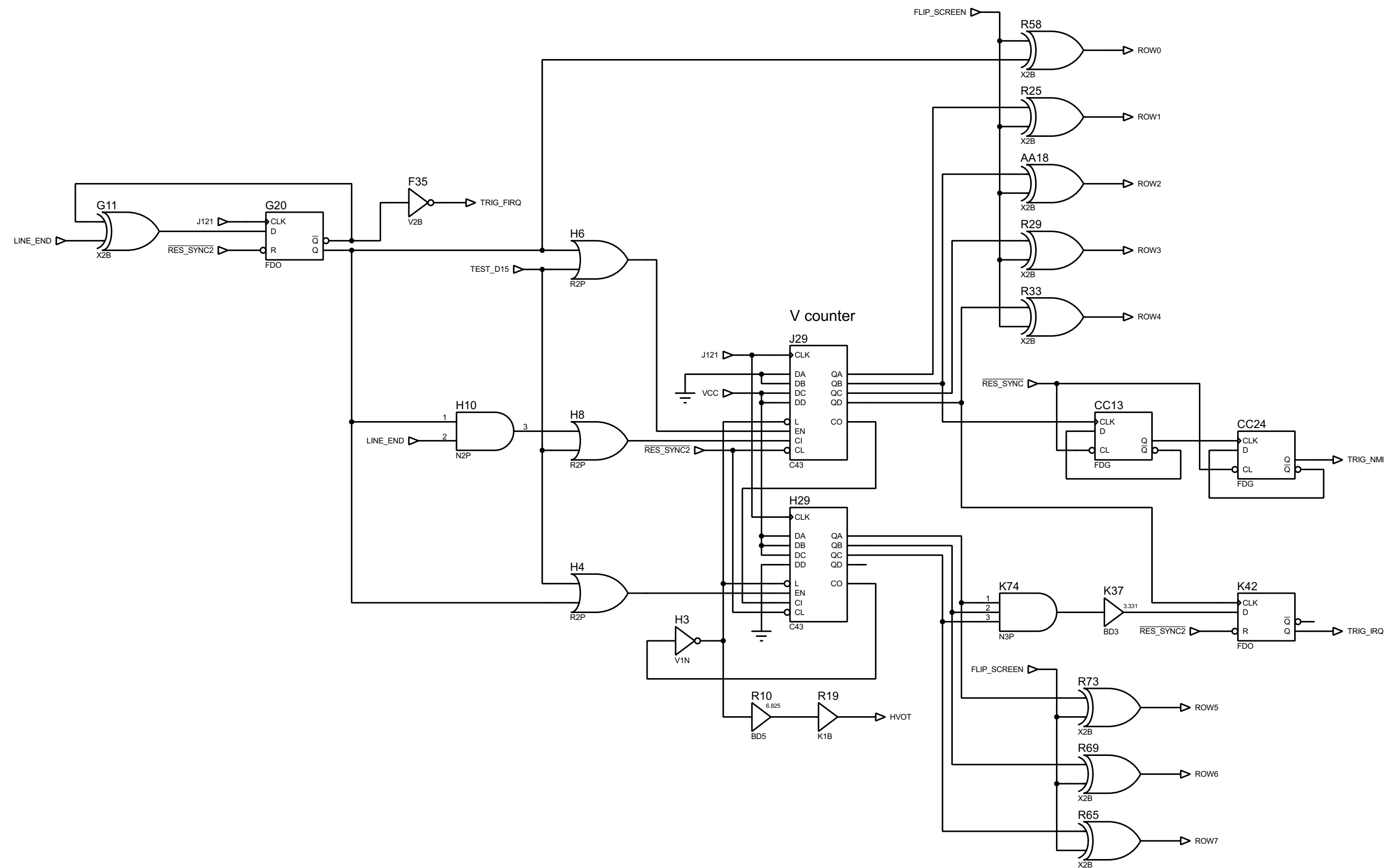
REG1C00_D[1:0] :

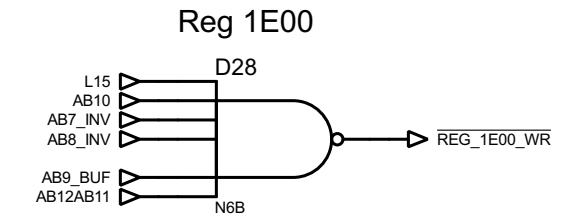
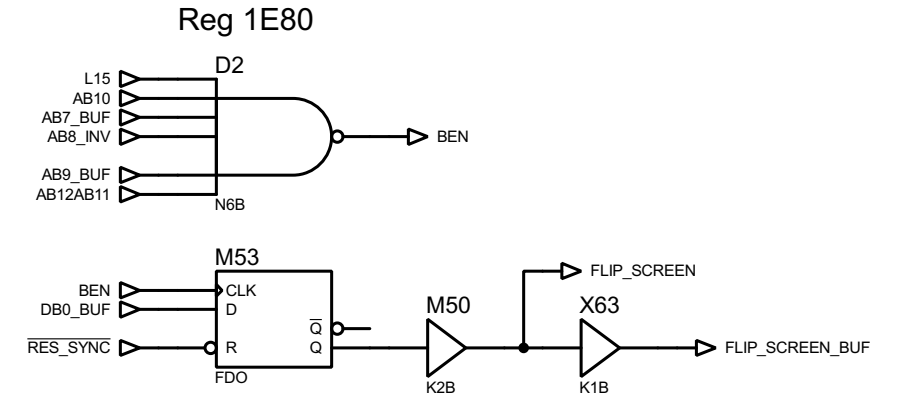
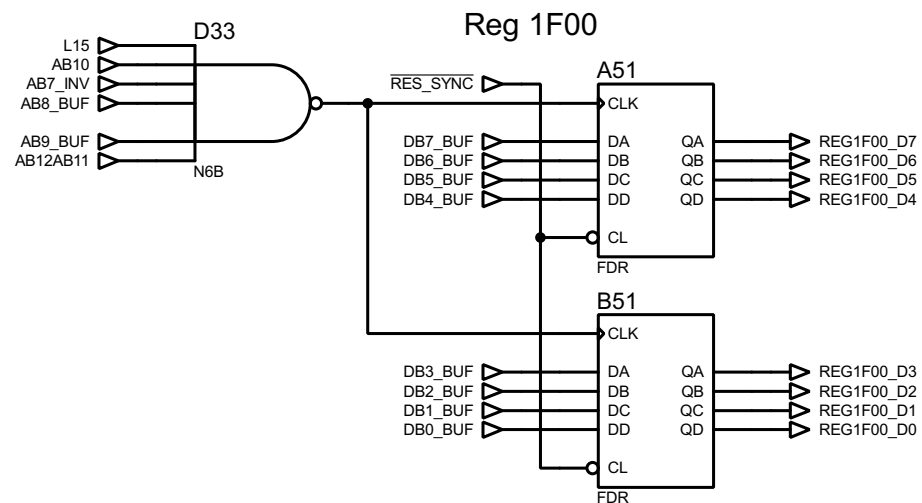
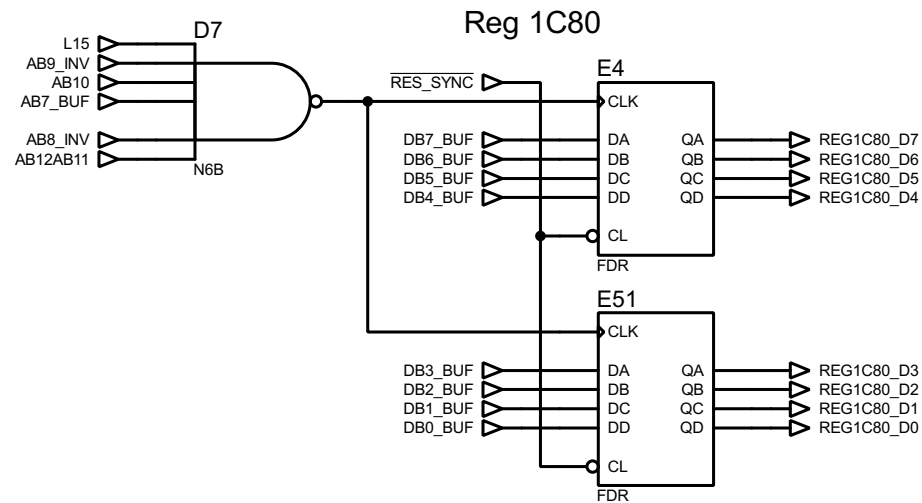
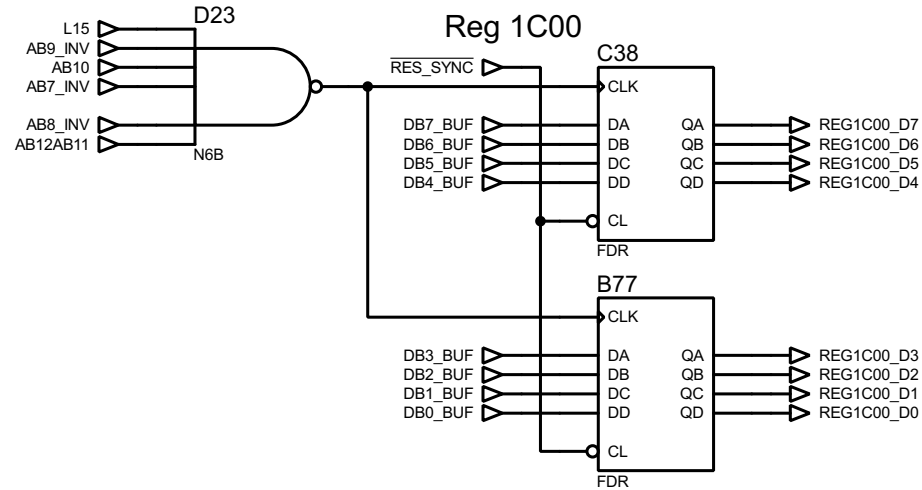
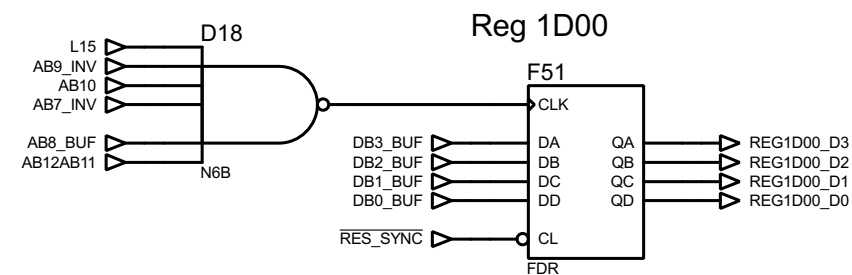
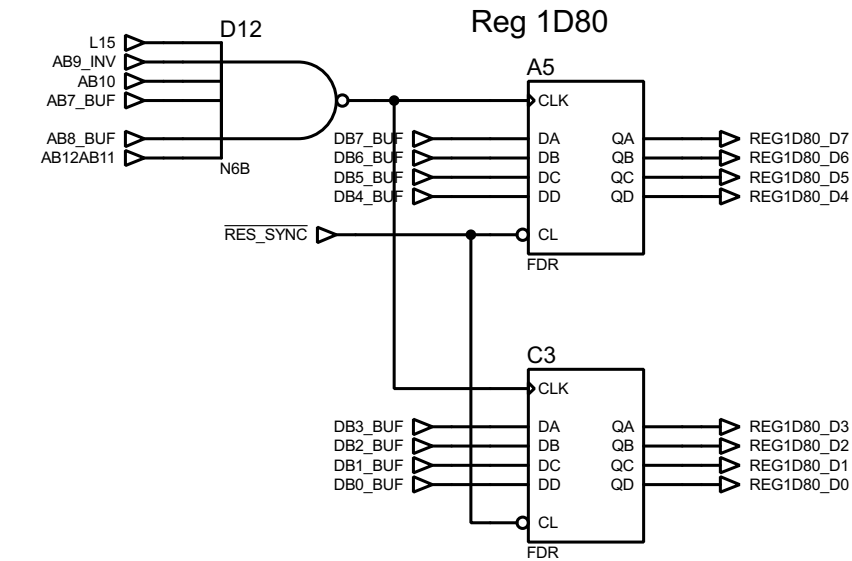
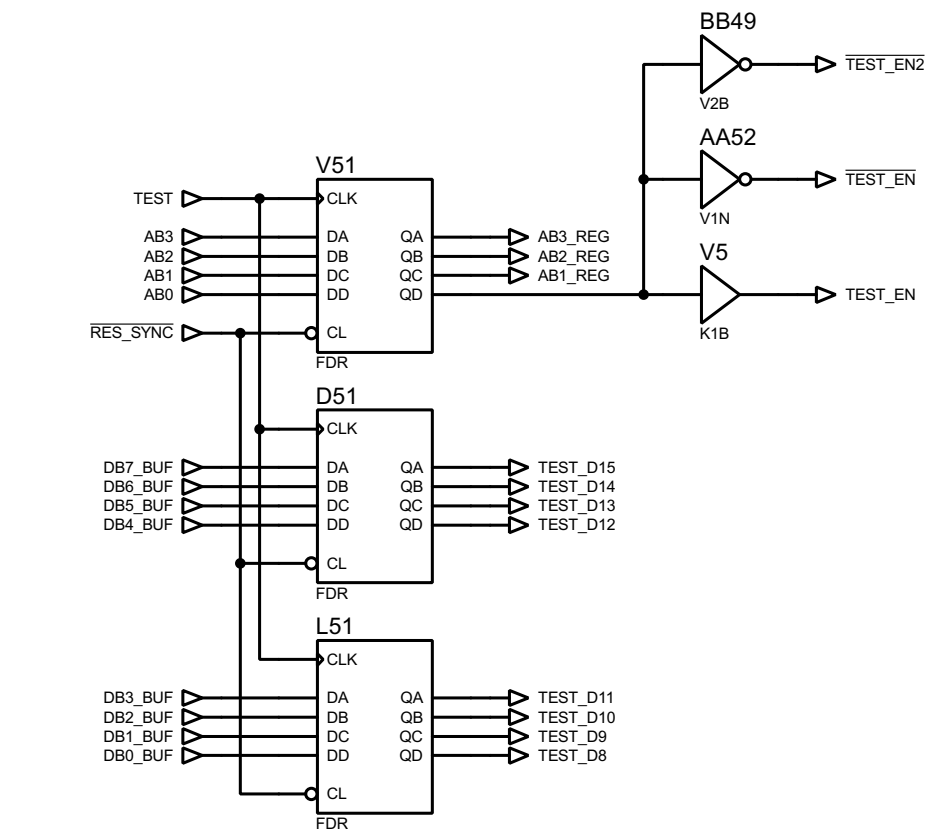
00	0~1	2~3	4~5
01	2~3	4~5	6~7
10	4~5	6~7	8~9
11	6~7	8~9	A~B

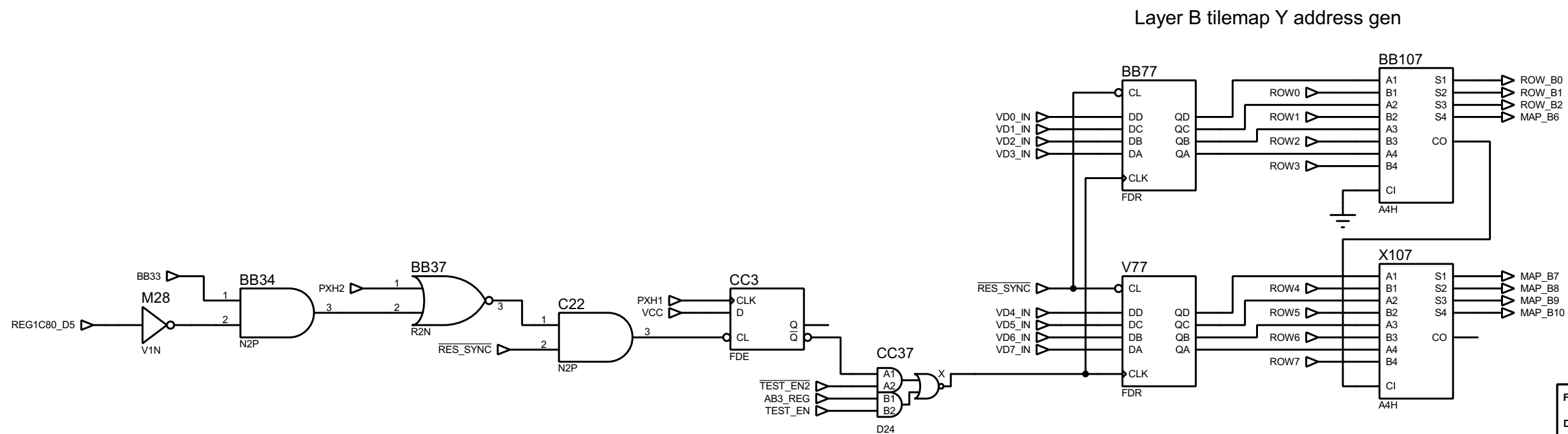
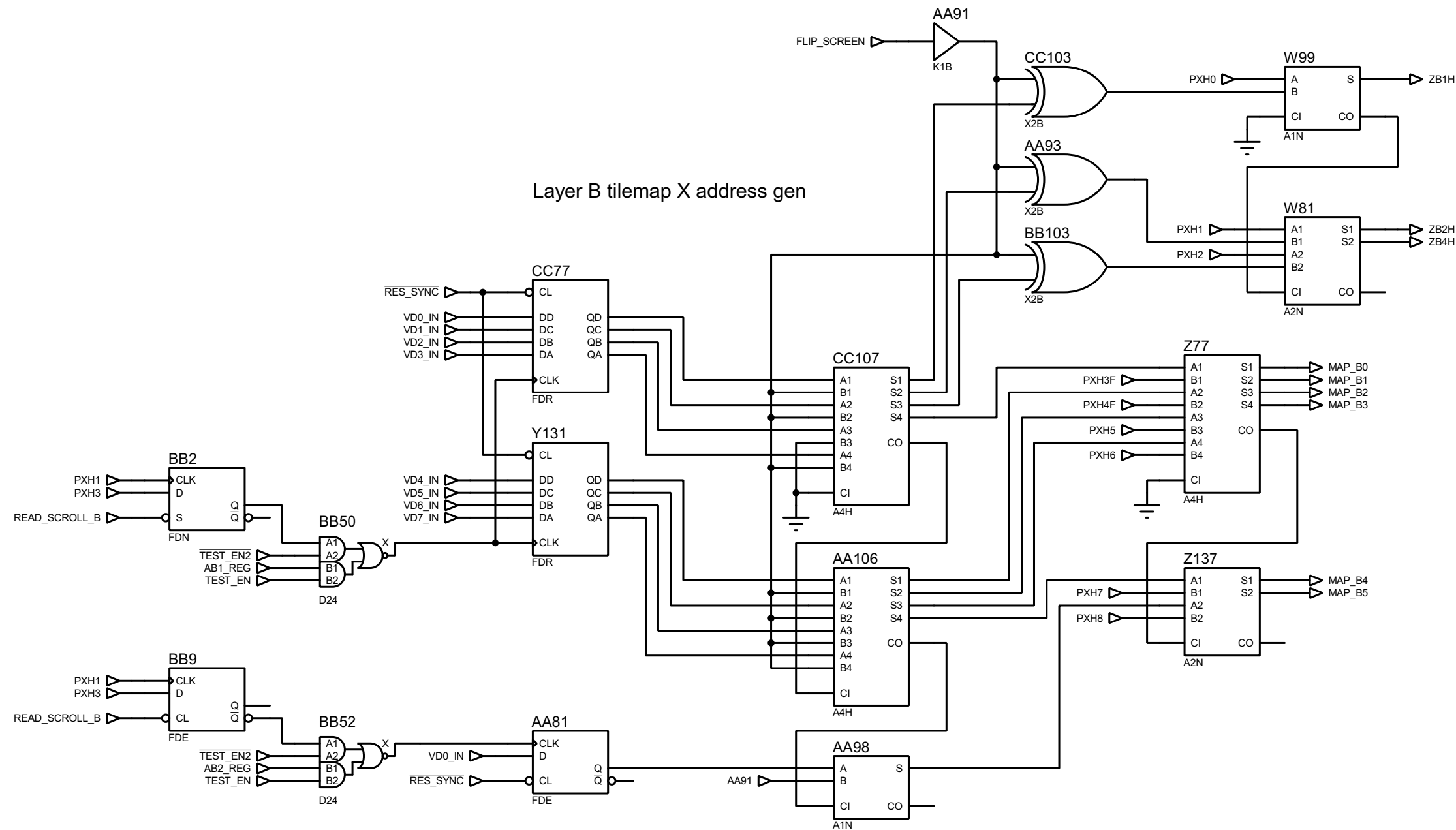


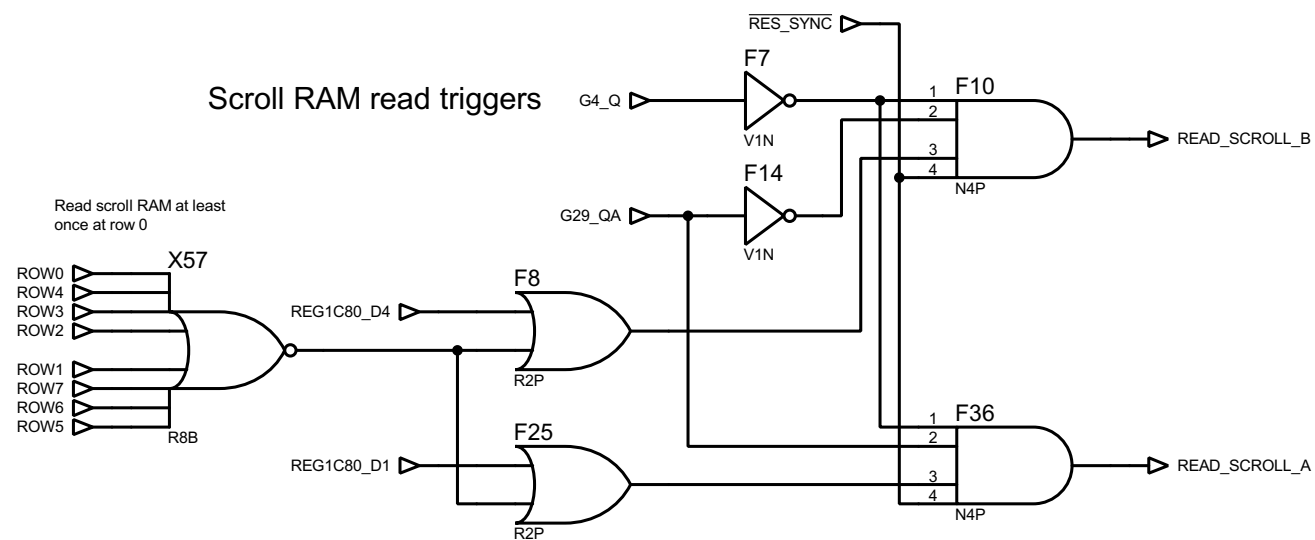
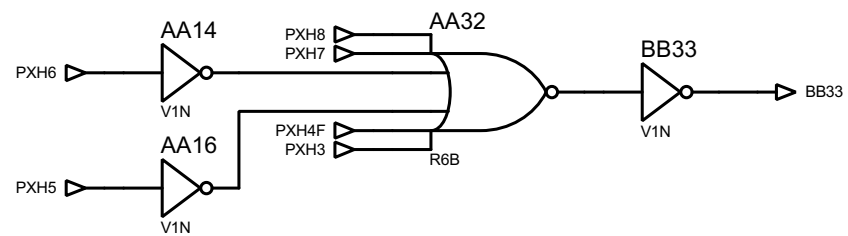
VRAM read by CPU



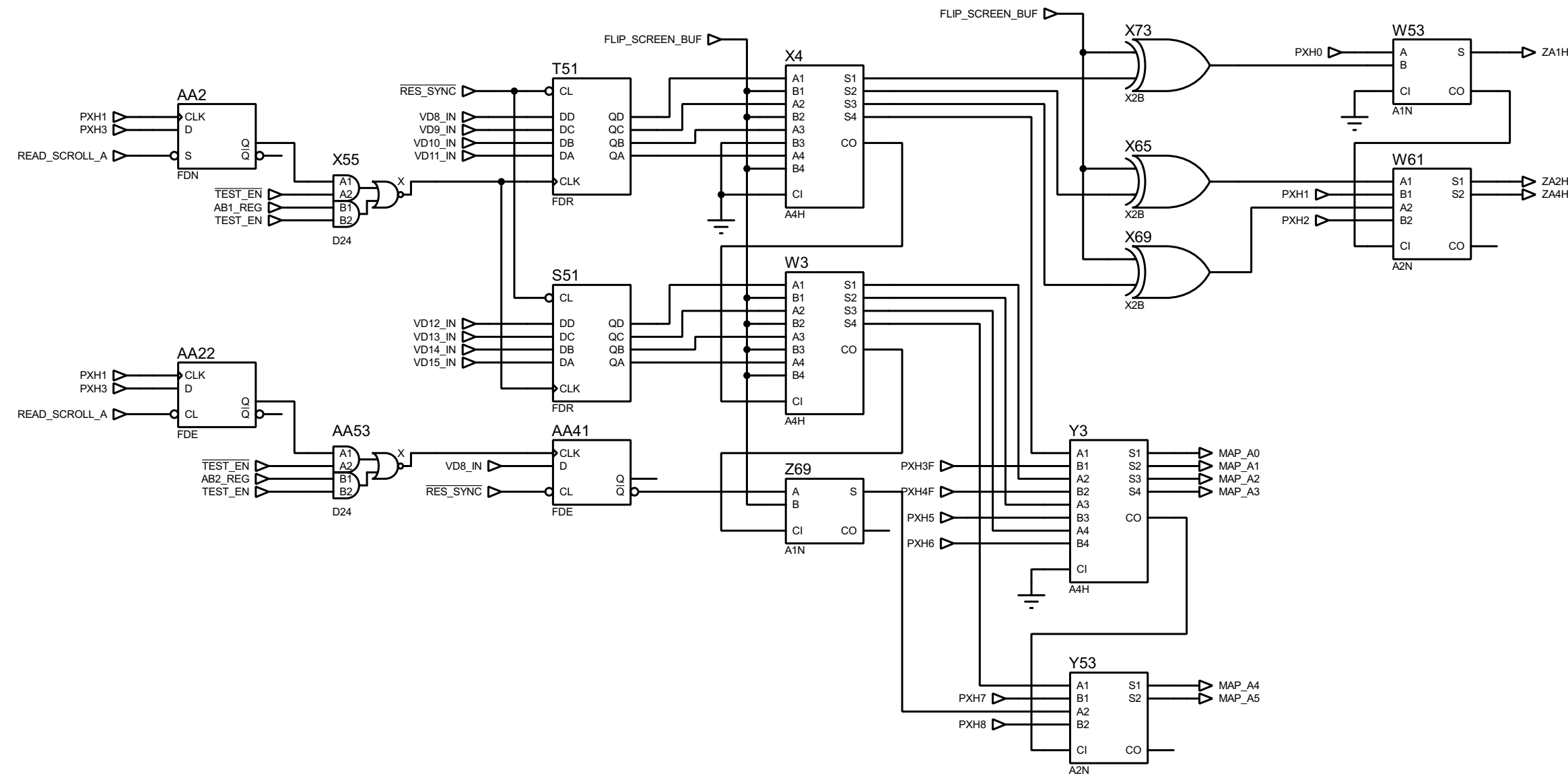








Layer A tilemap X address gen



Layer A tilemap Y address gen

