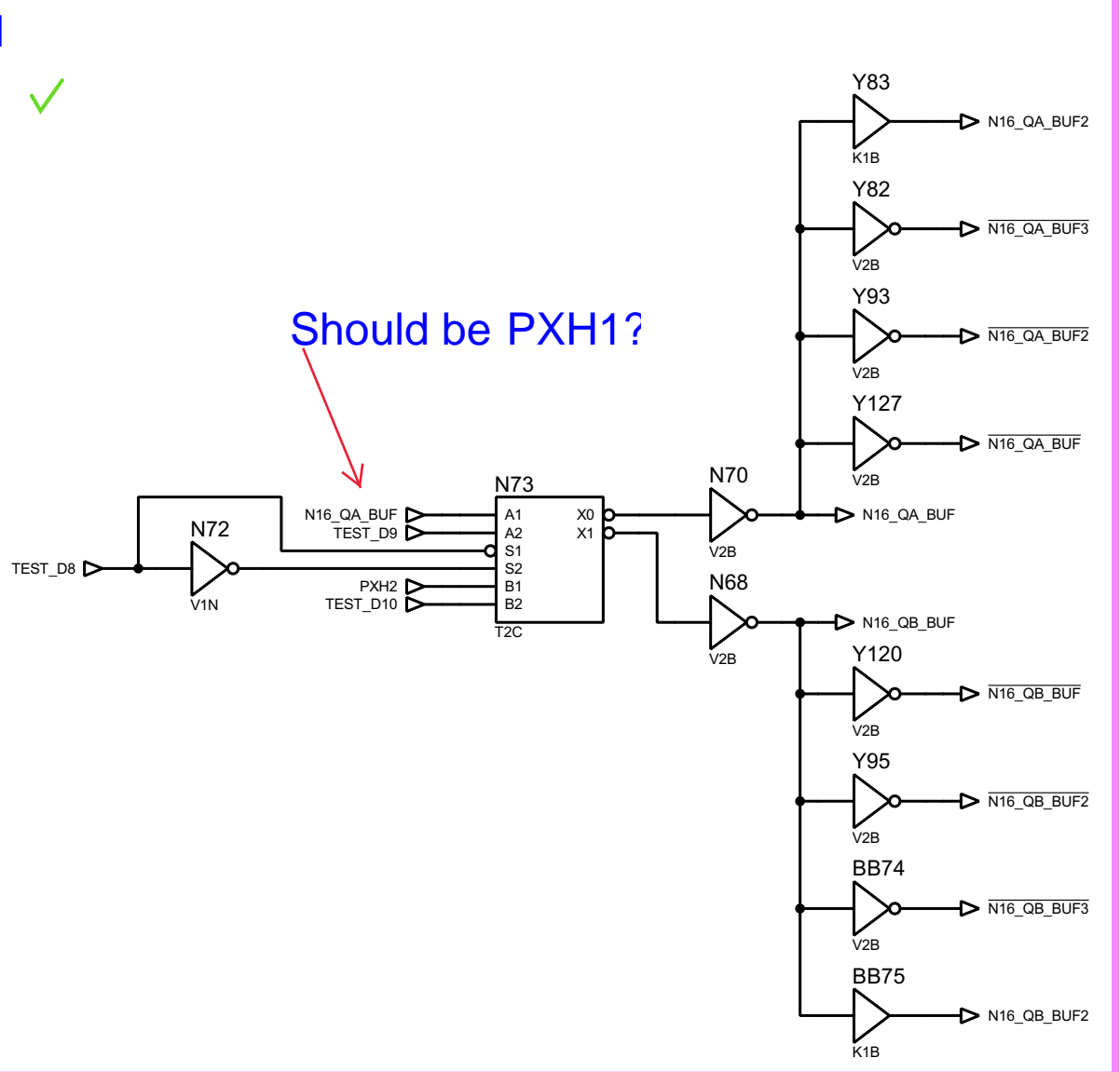


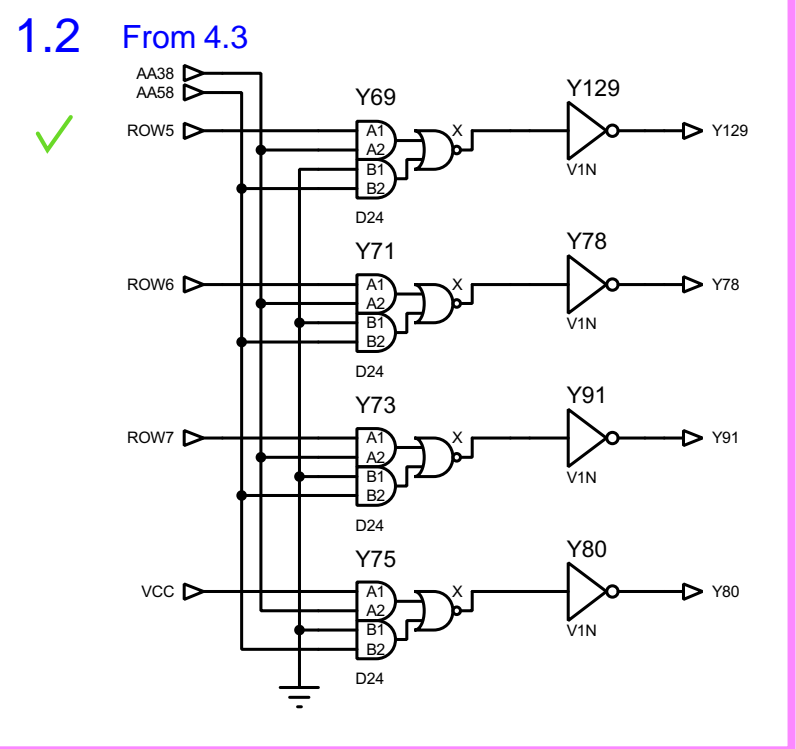
```

VRAM Address (1 word per address)
FEDC BA98 7654 3210
0000 00xx xxxx xxxx Layer FIX tilemap
0000 01xx xxxx xxxx Layer A tilemap
0000 10xx xxxx xxxx Layer B tilemap
0000 11xx xxxx xxxx Layer C tilemap
0000 1101 xxxx xxxx A X scroll
0001 00xx xxxx xxxx Layer FIX codes
0001 01xx xxxx xxxx Layer A codes
0001 10xx xxxx xxxx Layer B codes
0001 1100 xxxx xxxx B Y scroll
0001 1101 x xxxx X tilemaps X
          xx xxx Tilemaps Y

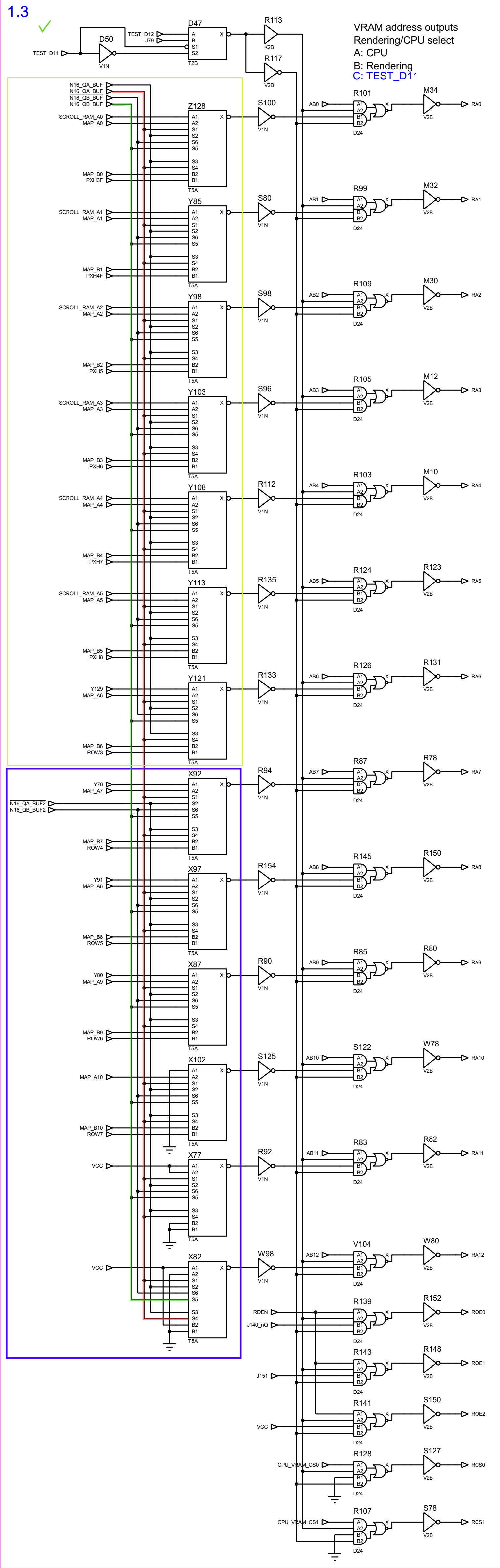
```

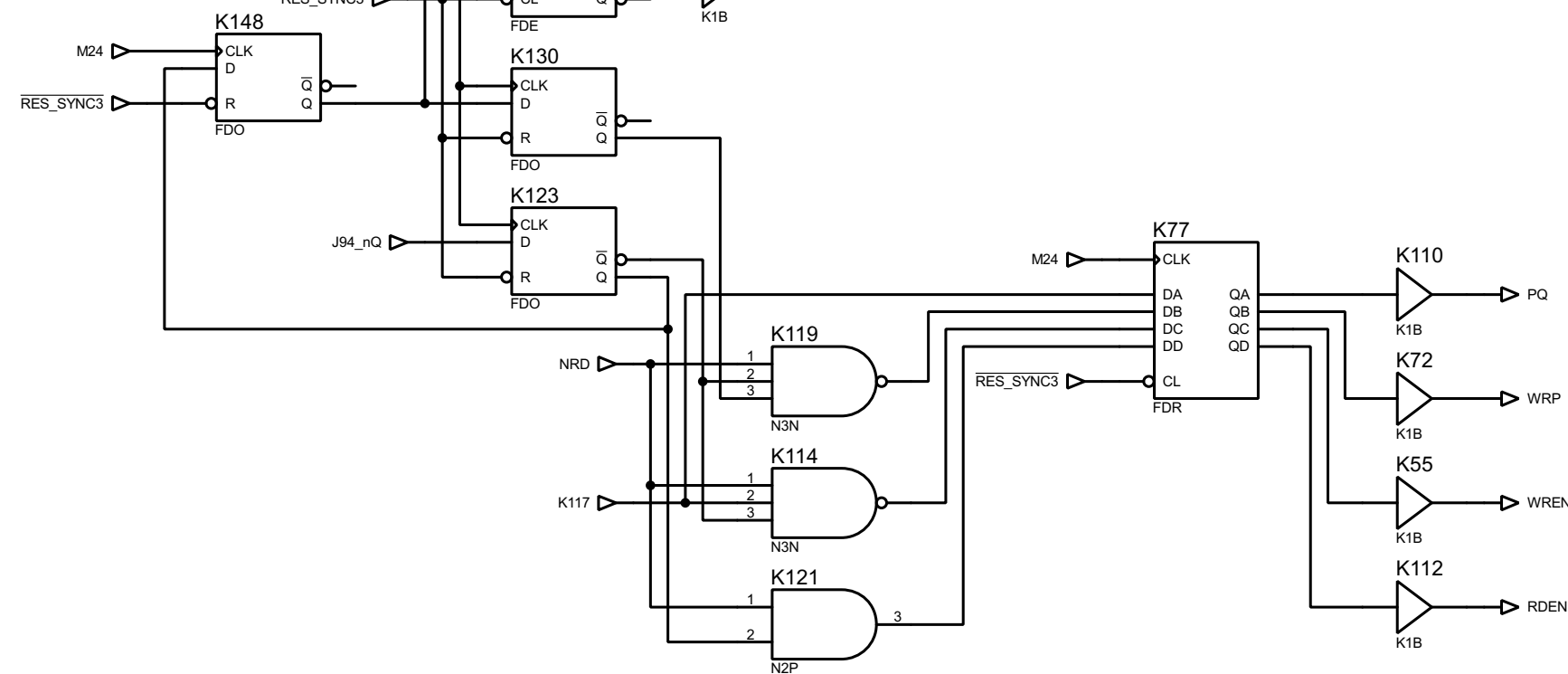
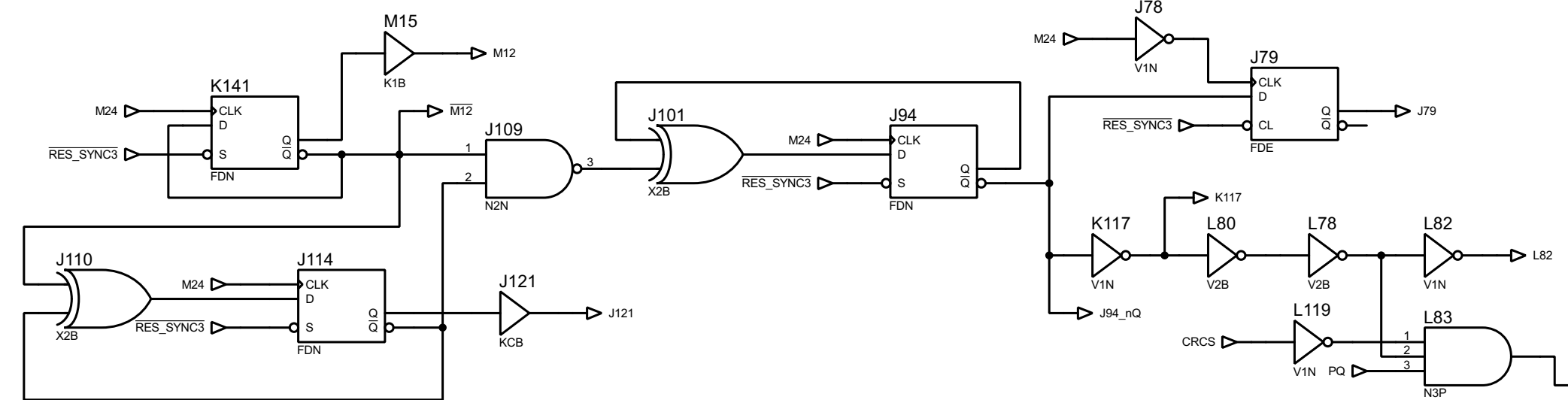


TEST_D13 Addresses Selector



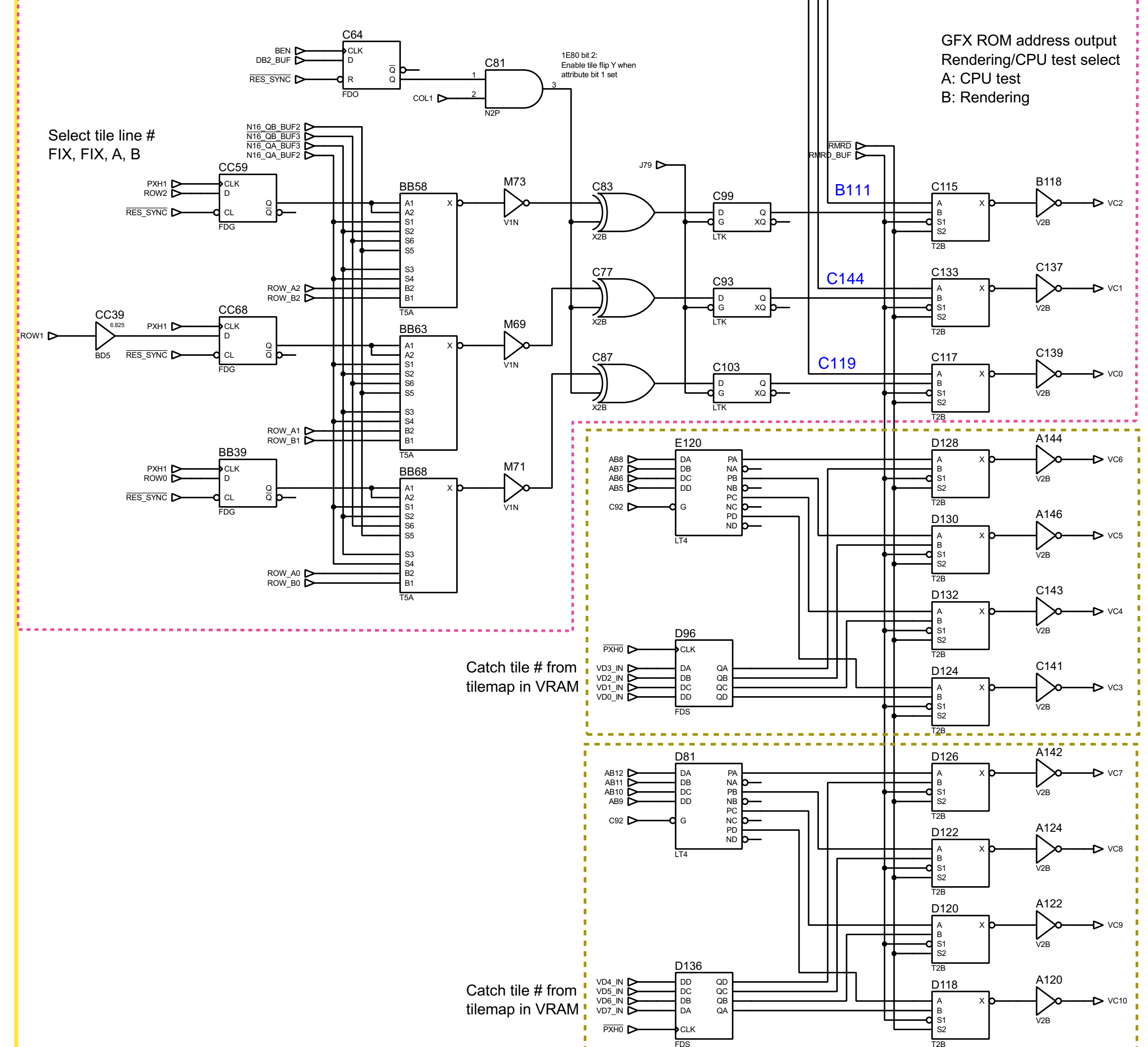
Selection can be simplified using AA38 (and AA38n) only.
AA58 always selects 1'b0.





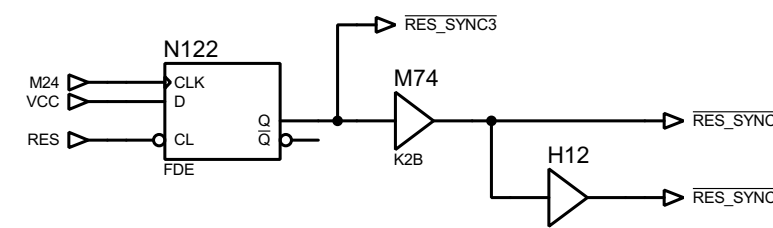
TIMING SIGNALS

SKIP because AB[1:0] used to select byte



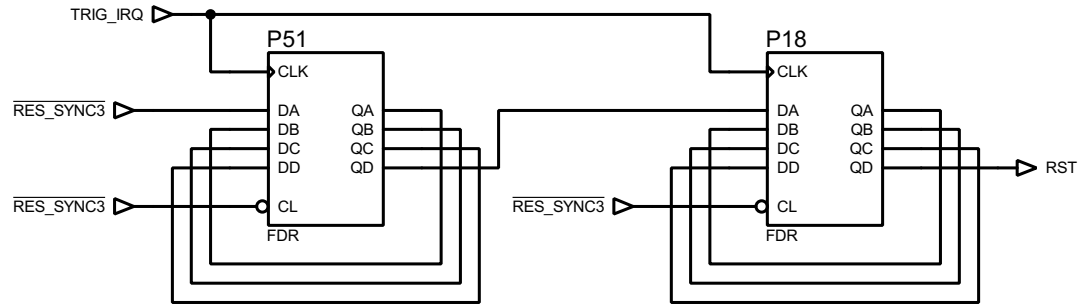
RES_SYNC signals generator

3.1 ✓

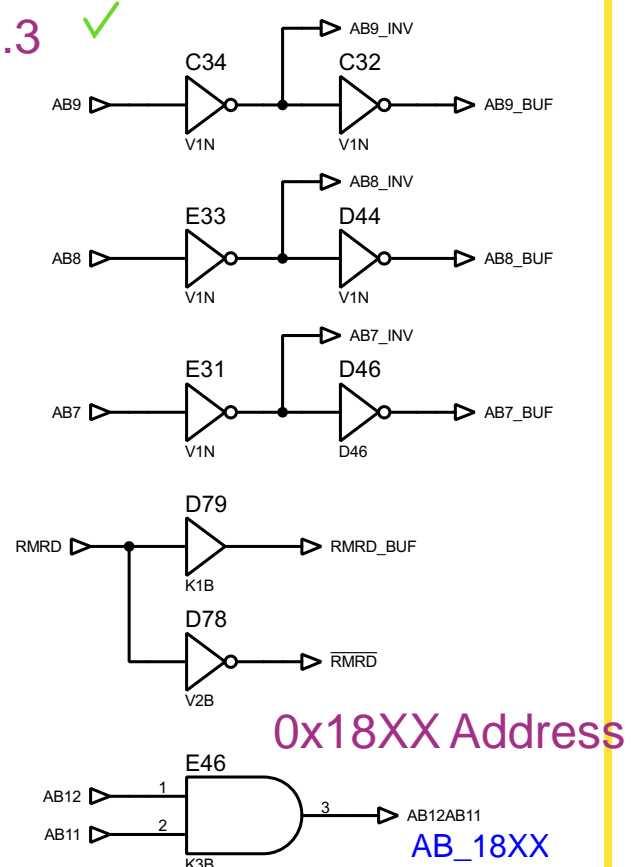


3.2 ✓

8-frame delay for
RES -> RST
Same in k051962 ?



3.3 ✓

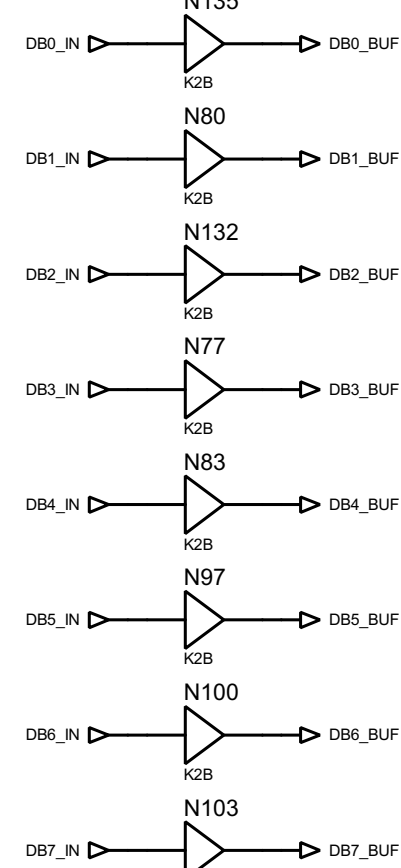


0x18XX Address

AB_18XX

180c-1833: Layer A Y Scroll

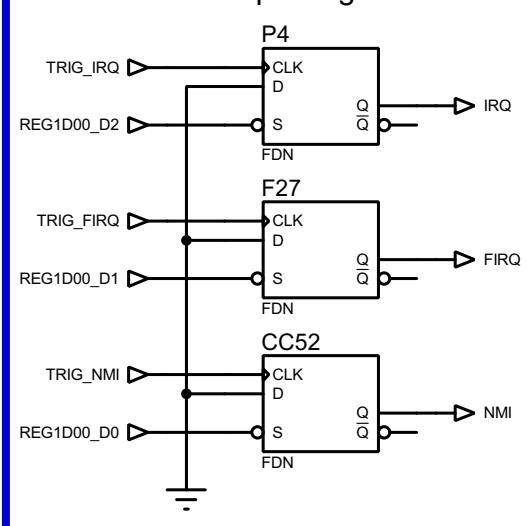
3.4 ✓



wire [7:0] DB_IN

wire [7:0] DB_BUF

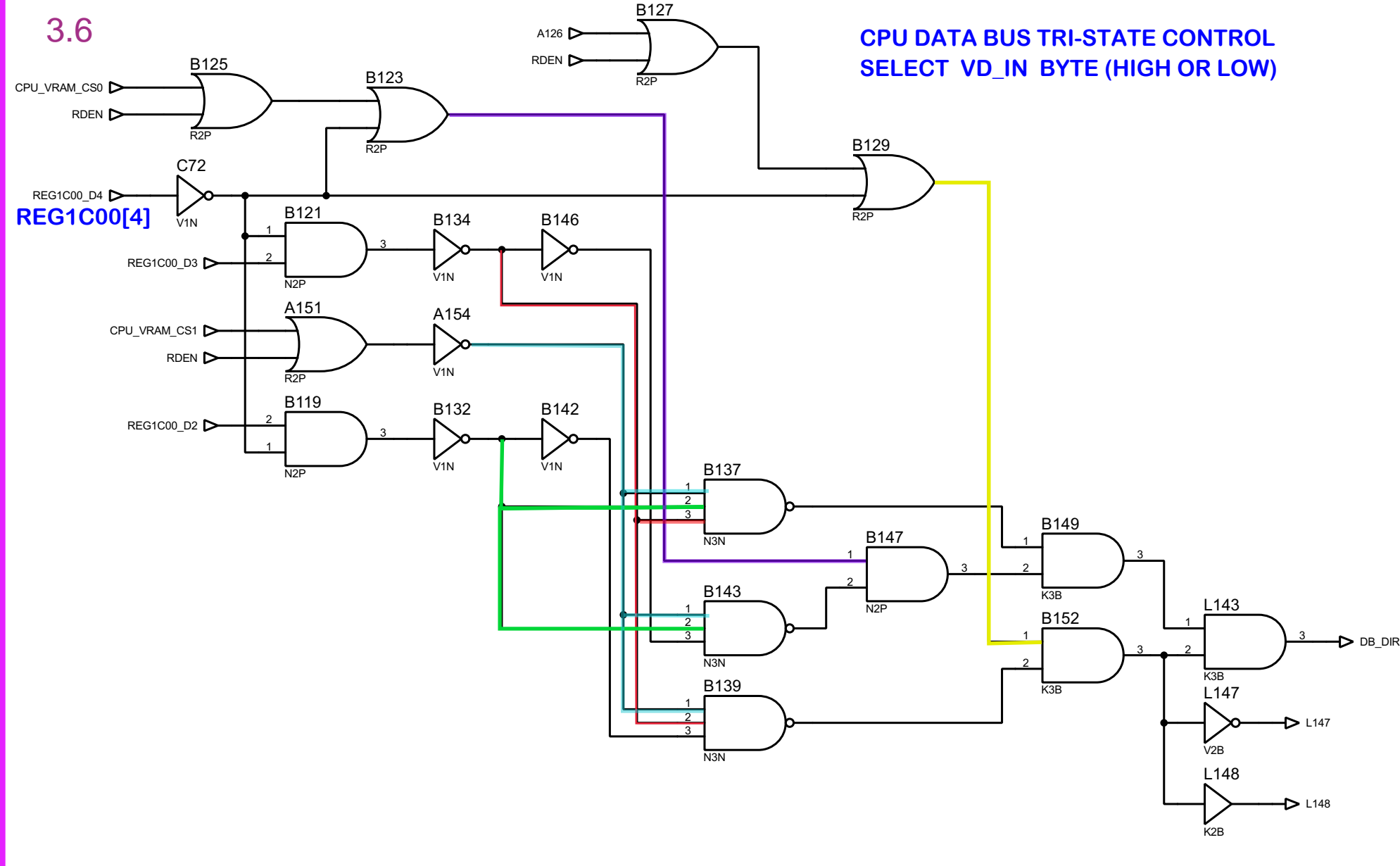
3.5 ✓ Interrupts flags



3.6

REG1C00[4]

CPU DATA BUS TRI-STATE CONTROL
SELECT VD_IN BYTE (HIGH OR LOW)



VRAM CONFIG AND CS/RW CONTROL

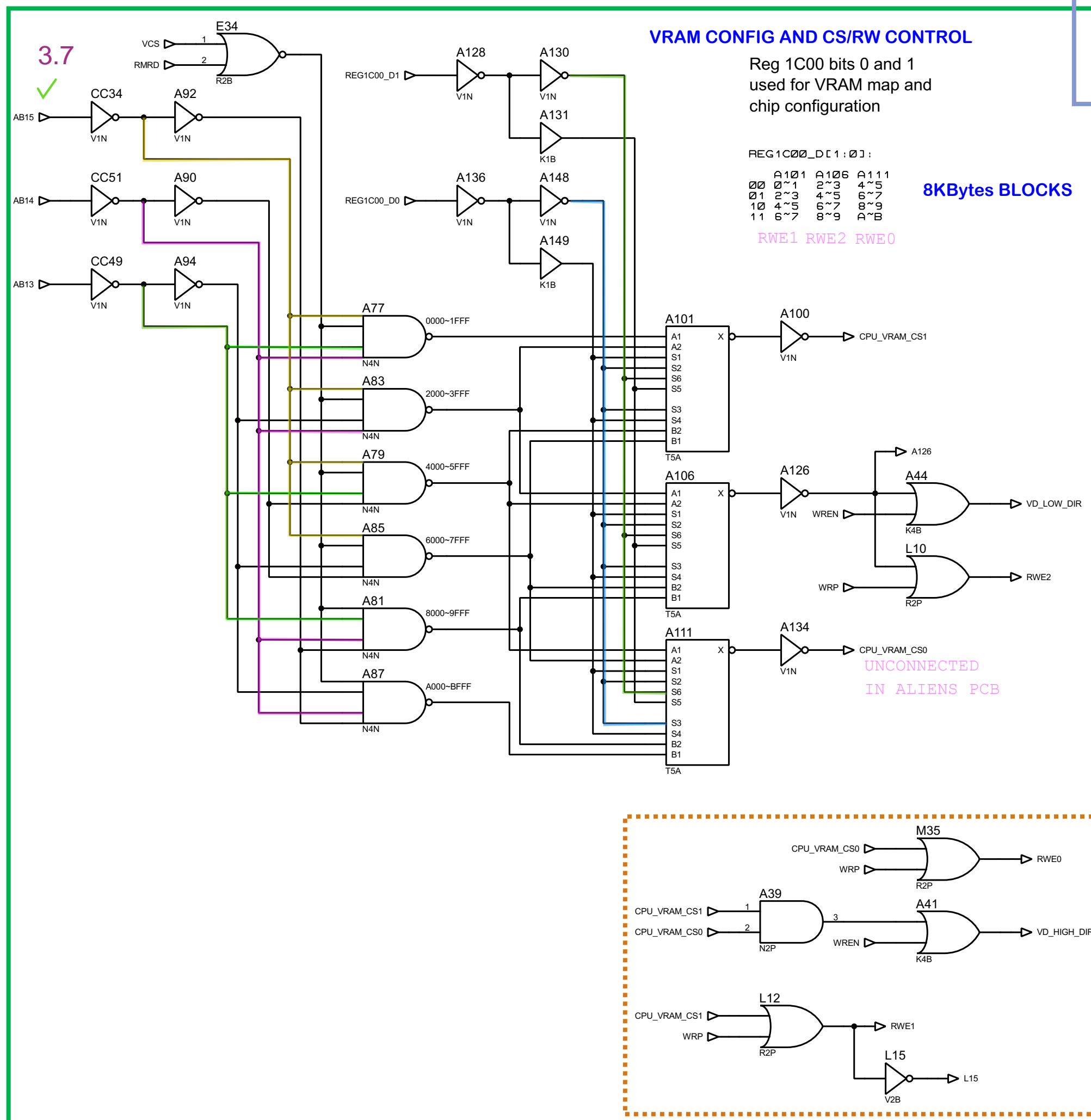
Reg 1C00 bits 0 and 1
used for VRAM map and
chip configuration

REG1C00_D[1:0] :

00 0~1 2~3 4~5 6~7 8~9 A~B
01 2~3 4~5 6~7 8~9 A~B
10 4~5 6~7 8~9 A~B
11 6~7 8~9 A~B

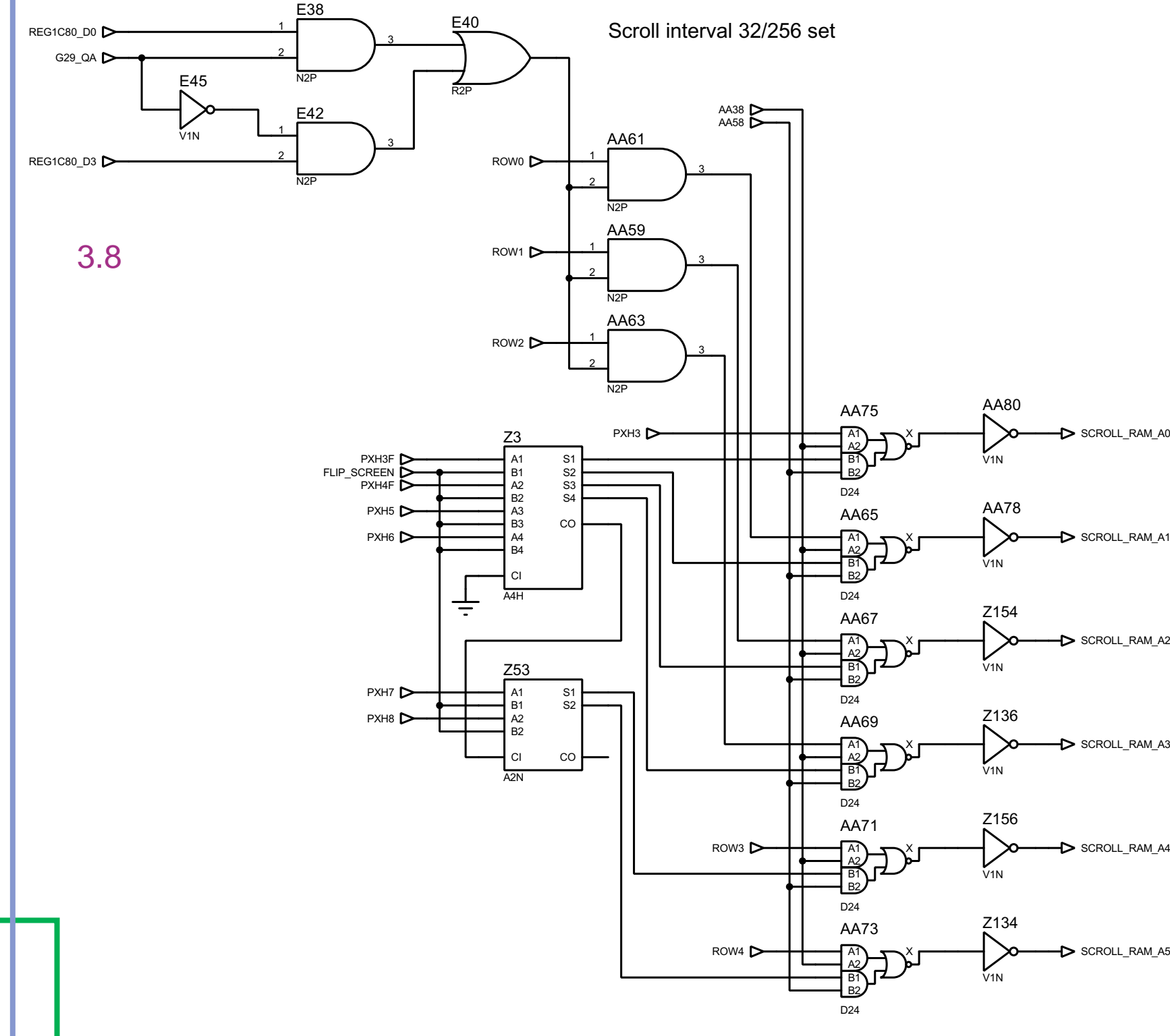
8KBytes BLOCKS

RWE1 RWE2 RWE0



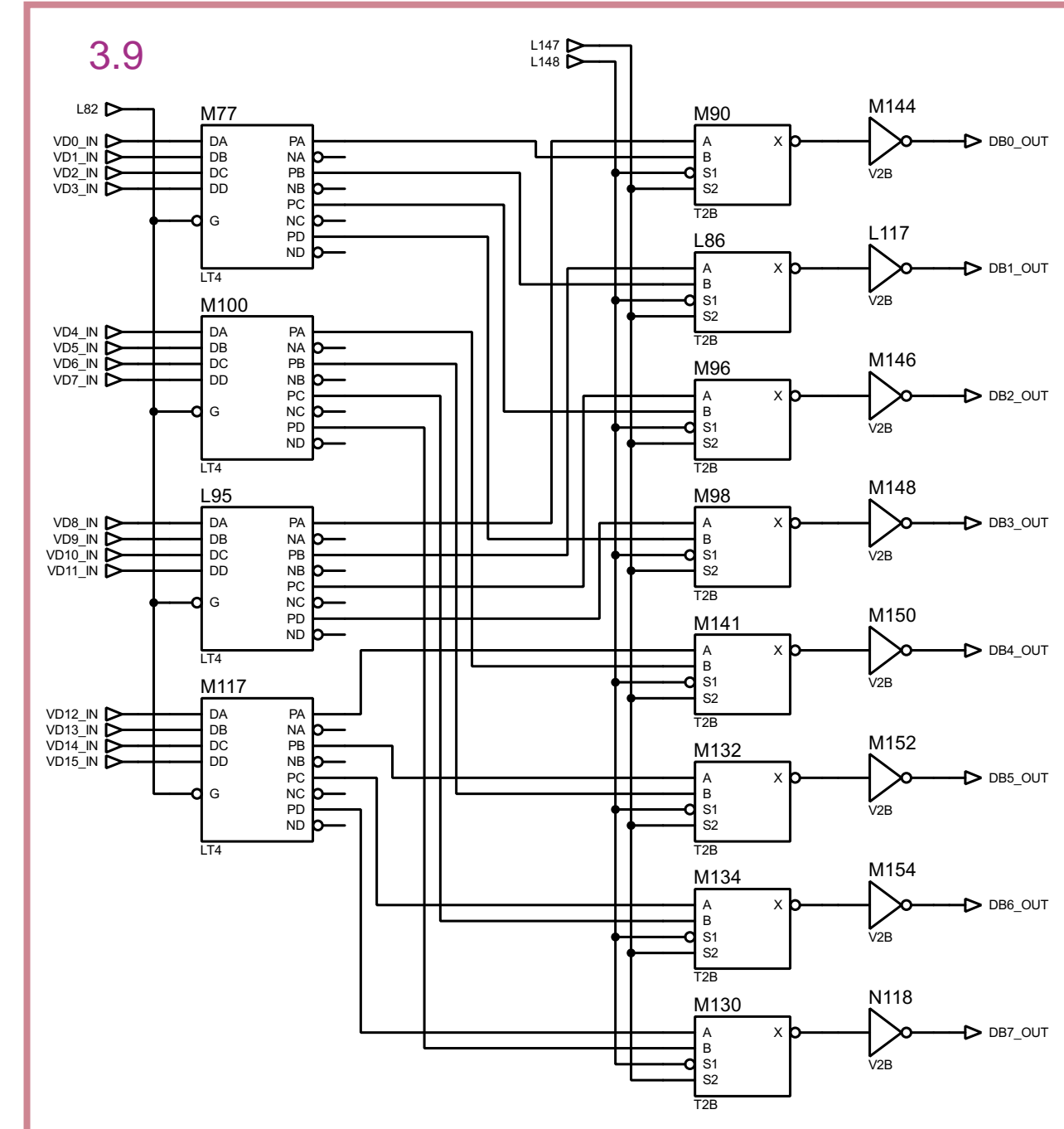
3.8

Scroll interval 32/256 set

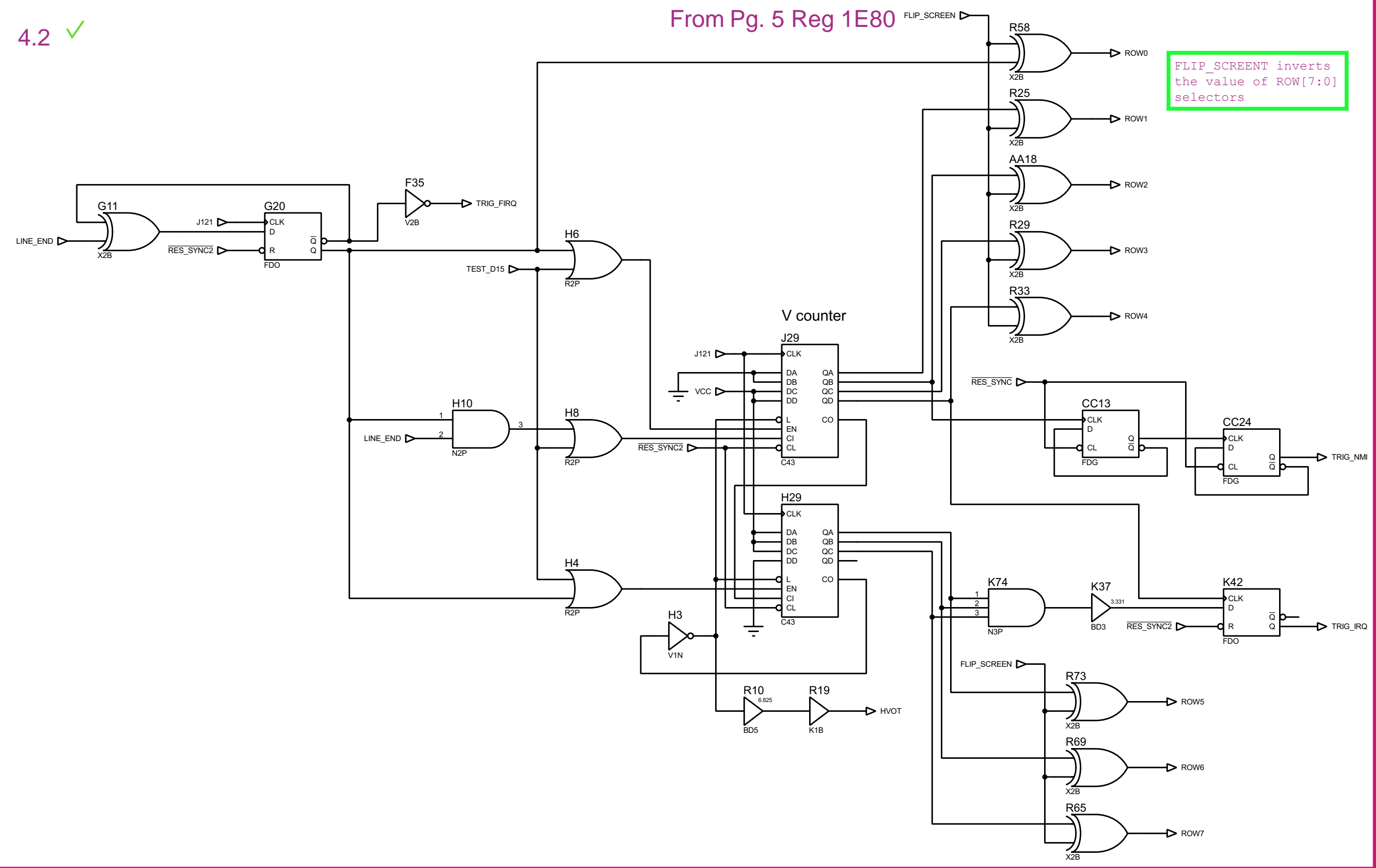


VRAM read by CPU

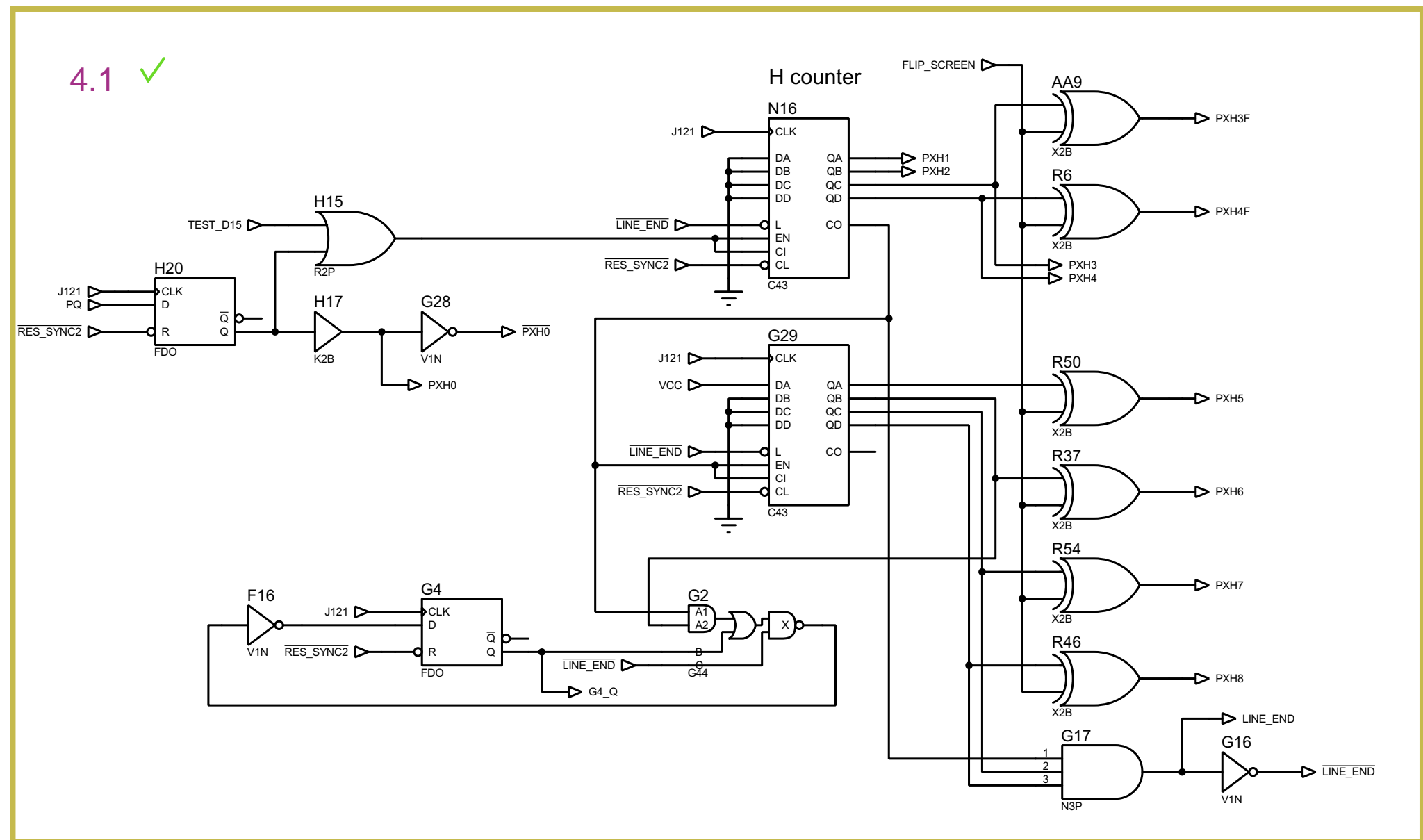
3.9



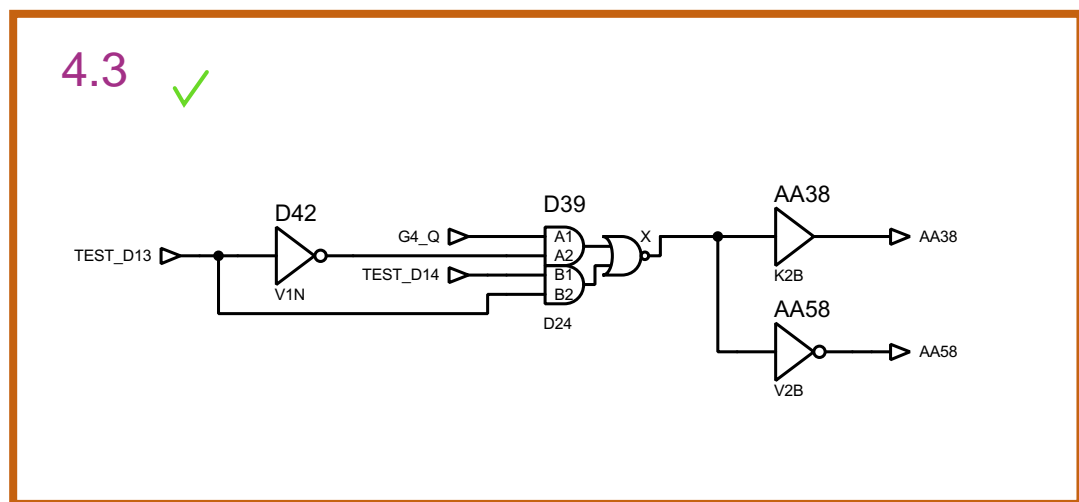
4.2 ✓



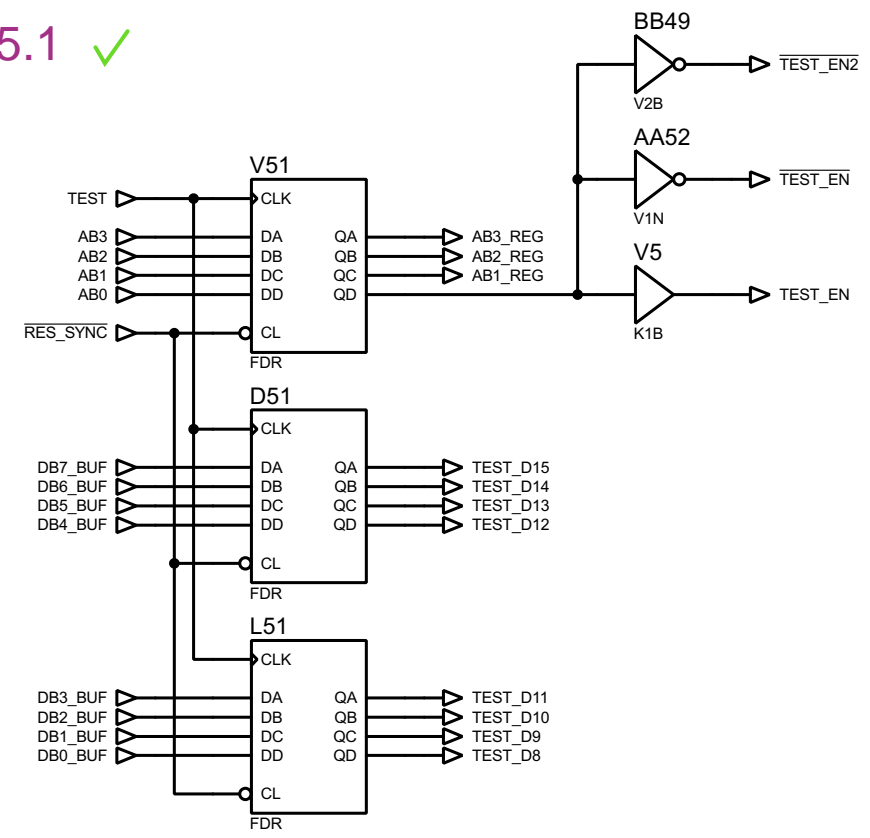
4.1 ✓



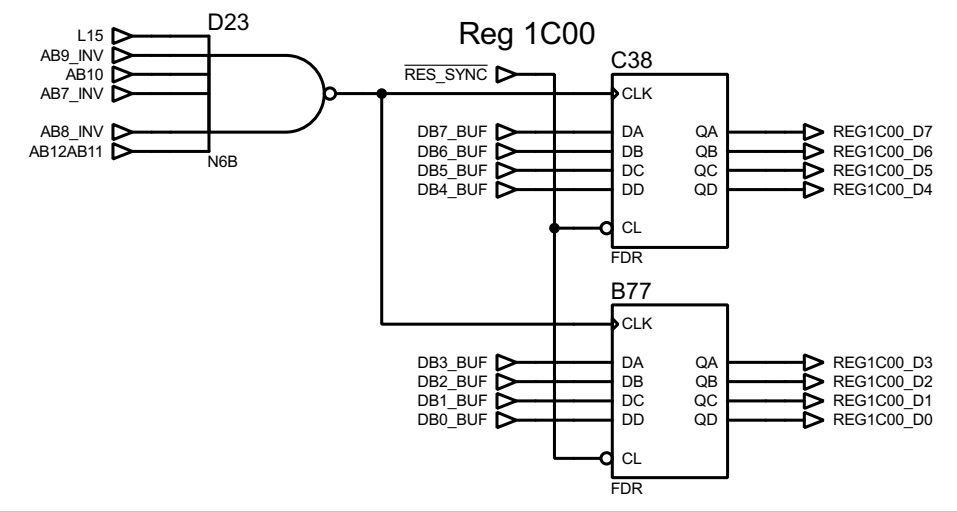
4.3 ✓



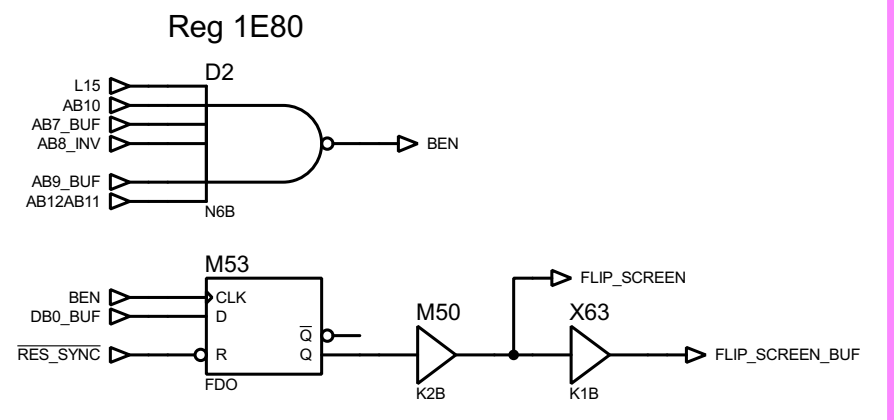
5.1 ✓



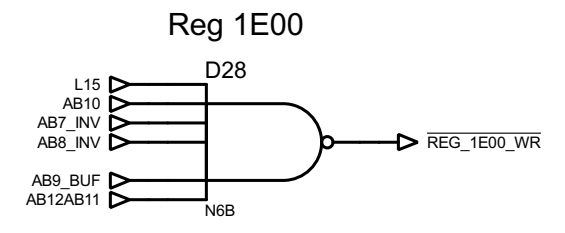
5.4 ✓



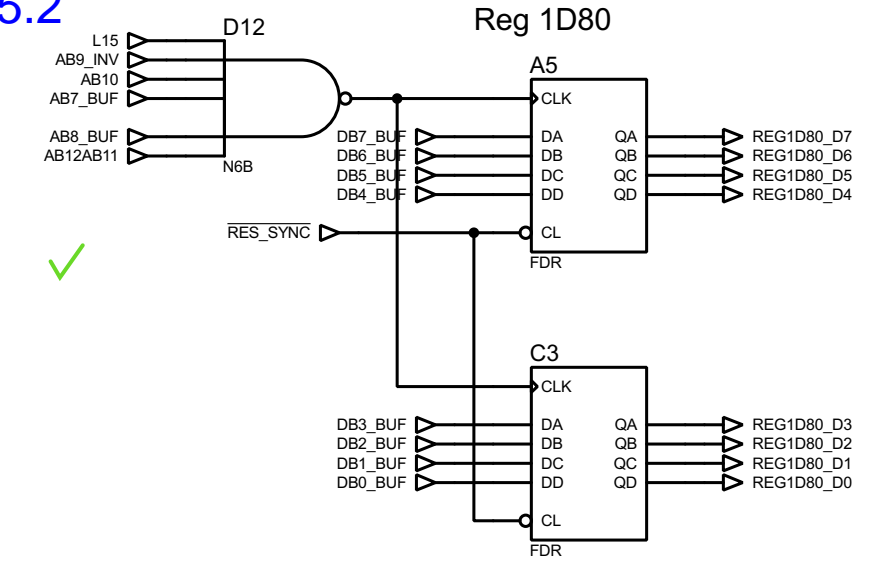
5.7 ✓



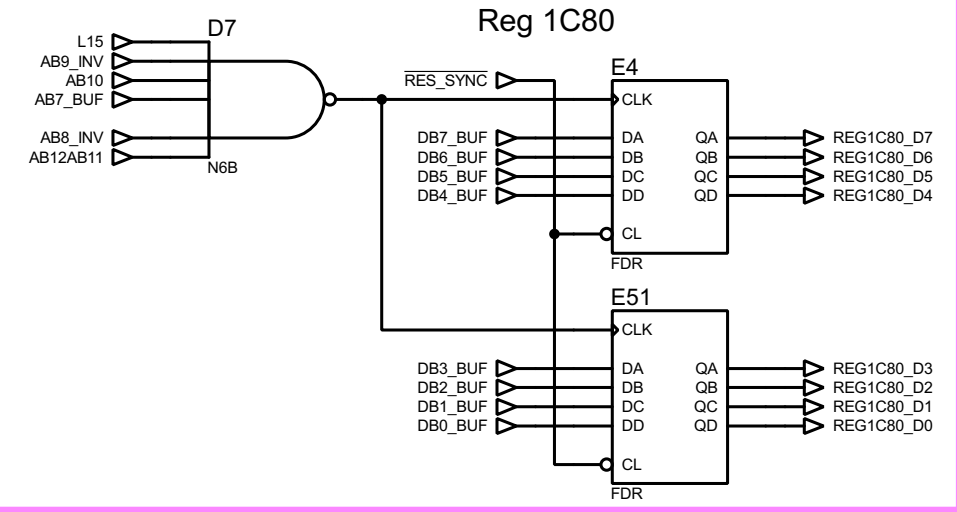
5.8 ✓



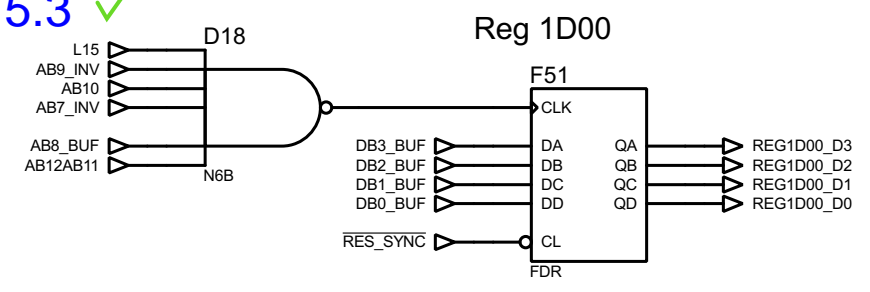
5.2 ✓



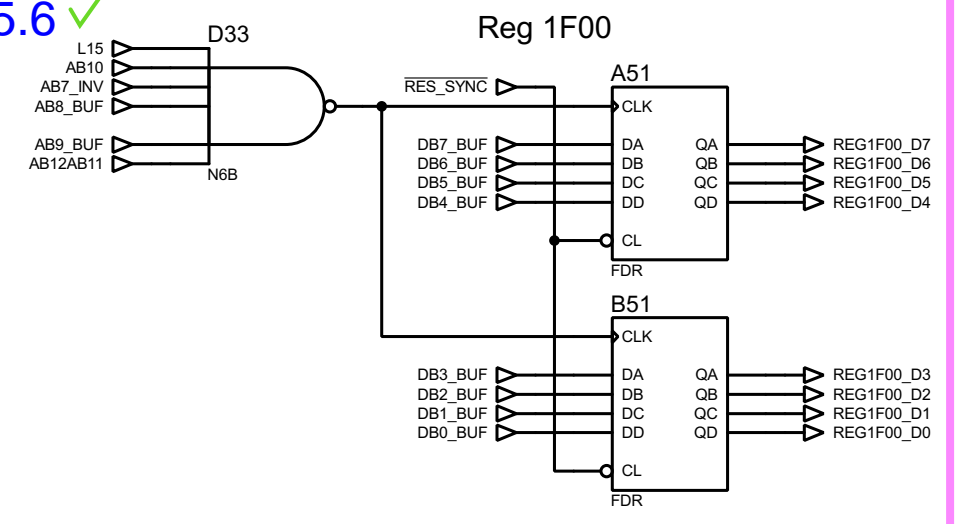
5.5 ✓



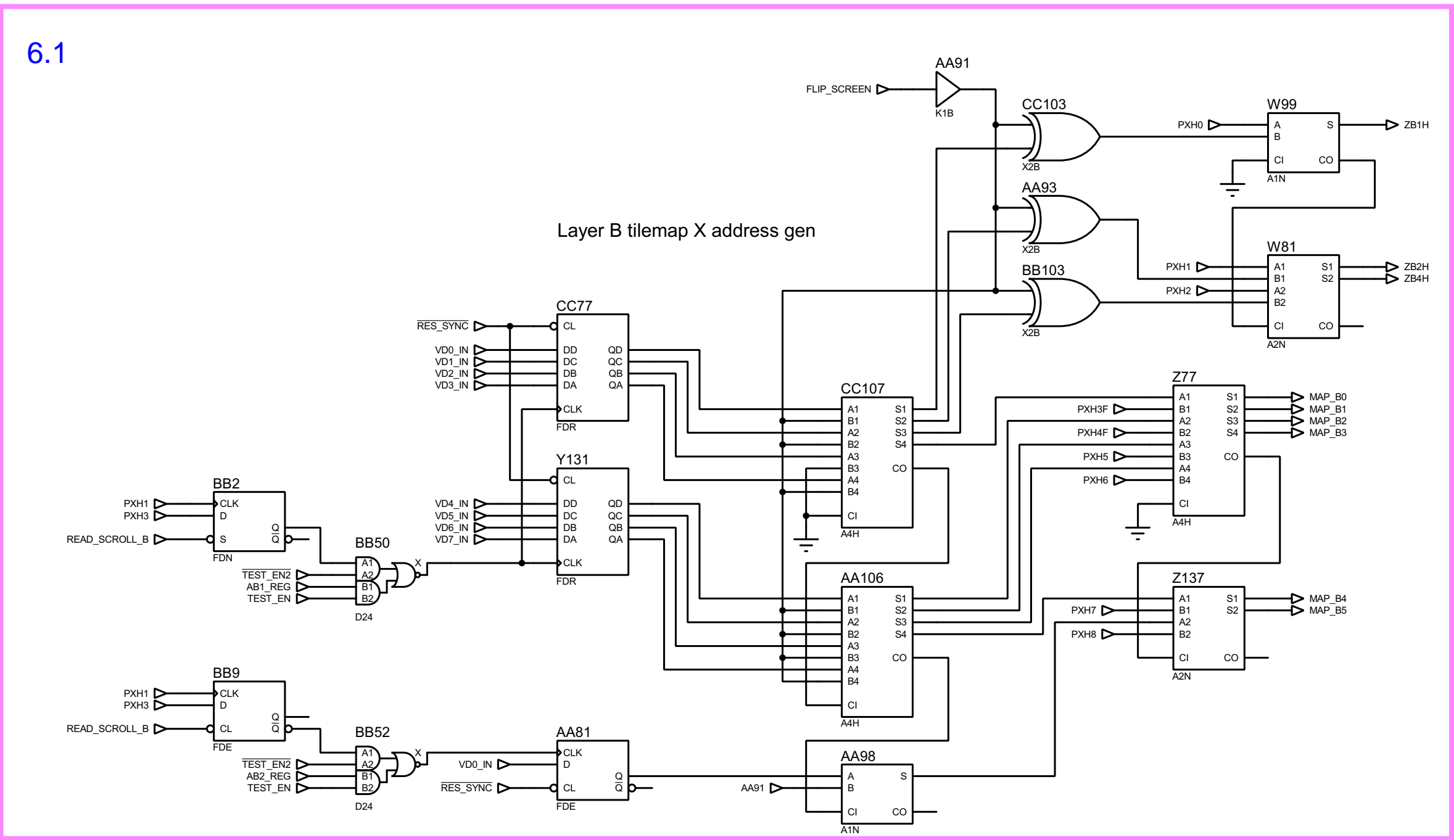
5.3 ✓



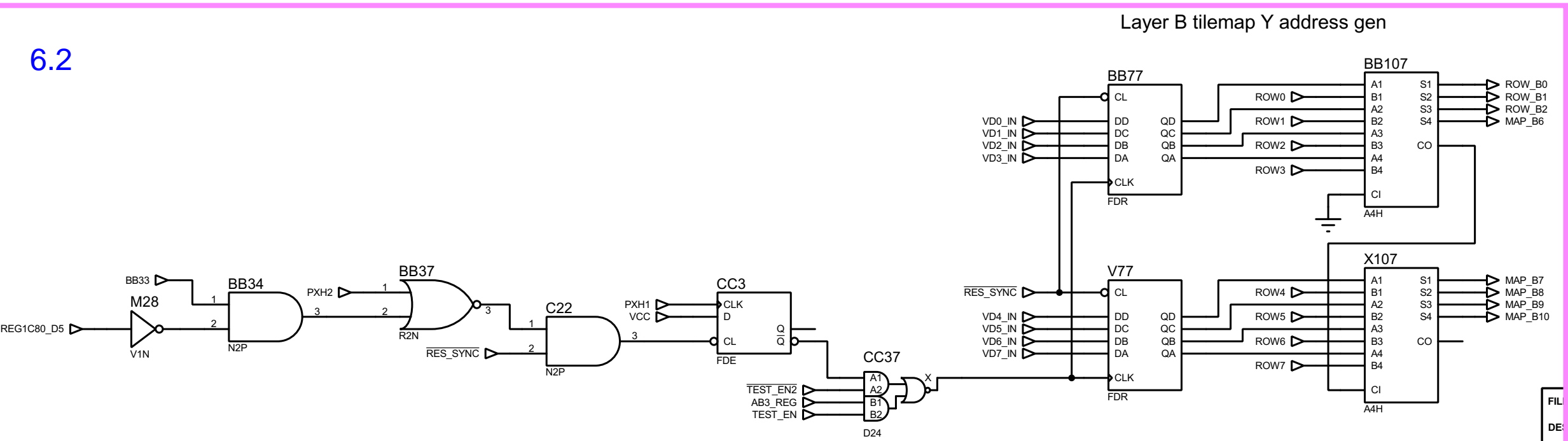
5.6 ✓



6.1



6.2



7.1

GFX ROM bank
for CPU testing

REG_1E00_WR
DB3_BUF
DB2_BUF
DB1_BUF
DB0_BUF
RES_SYNC
CLK
FDR

QA
QB
QC
QD
E77_QC
E77_QD

F41
B14
K2B
B13
V2B
F24
A35
V1N
A31
K2B
REG1D80_D0
REG1D80_D4
REG1F00_D0
REG1F00_D4
REG1D80_D1
REG1D80_D5
REG1F00_D1
REG1F00_D5
REG1D80_D2
REG1D80_D6
REG1F00_D2
REG1F00_D6
REG1D80_D3
REG1D80_D7
REG1F00_D3
REG1F00_D7

B3
A1
A2
A3
B1
B2
B3
C1
C2
C3
D1
D2
D3
T34
B19
A1
A2
A3
B1
B2
B3
C1
C2
C3
D1
D2
D3
T34
B40
A1
A2
A3
B1
B2
B3
C1
C2
C3
D1
D2
D3
T34
B28
A1
A2
A3
B1
B2
B3
C1
C2
C3
D1
D2
D3
T34

C36
V1N
C29
A1
A2
B1
B2
D24
E149
V1N
E150
V2B
E145
A
B
S1
S2
T2B
F149
V1N
COL2
B39
V1N
C75
A1
A2
B1
B2
D24
C155
V2B
E141
A
B
S1
S2
T2B
H124
V1N
COL3
A38
V1N
CAB1
A48
V1N
CAB2

REG1C00_D5
REG1C00_D6
RMRD
V1N

7.2

7.3

The diagram illustrates the logic for the GFX ROM bank during CPU testing. It consists of the following components and connections:

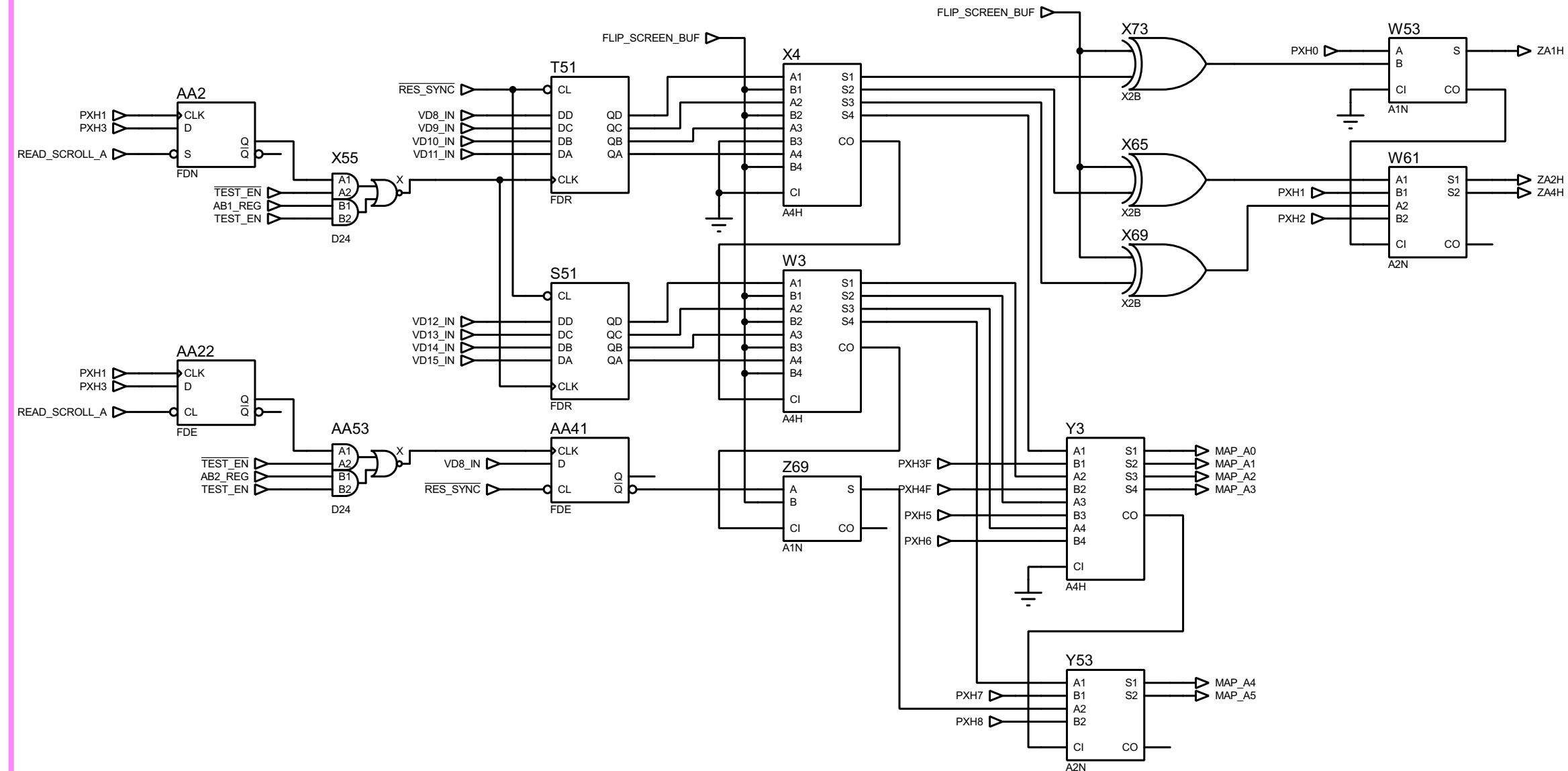
- Decoders:**
 - G77:** A 3-to-8 decoder with clock input `PXH0`. Its data inputs are `VD15_IN`, `VD14_IN`, and `VD13_IN`. Its outputs are `QA`, `QB`, `QC`, and `QD`.
 - H92:** A 3-to-8 decoder with clock input `J140_nQ`. Its data inputs are `VD15_IN`, `VD14_IN`, and `VD13_IN`. Its outputs are `QA`, `QB`, `QC`, and `QD`.
 - F77:** A 3-to-8 decoder with clock input `REG_1E00_WR`. Its data inputs are `DB7_BUF`, `DB6_BUF`, `DB5_BUF`, and `DB4_BUF`. Its outputs are `QA`, `QB`, `QC`, and `QD`.
- Multiplexers:**
 - G101:** An 8-to-1 multiplexer with inputs `A1`, `A2`, `S1`, `S2`, `S6`, `S5`, `S3`, and `S4`. It has control inputs `B2`, `B1`, and `T5A`. Its output is `X`, which is inverted by `L140` to produce `COL7`.
 - G106:** An 8-to-1 multiplexer with inputs `A1`, `A2`, `S1`, `S2`, `S6`, `S5`, `S3`, and `S4`. It has control inputs `B2`, `B1`, and `T5A`. Its output is `X`, which is inverted by `L142` to produce `COL6`.
 - G117:** An 8-to-1 multiplexer with inputs `A1`, `A2`, `S1`, `S2`, `S6`, `S5`, `S3`, and `S4`. It has control inputs `B2`, `B1`, and `T5A`. Its output is `X`, which is inverted by `J150` to produce `COL5`.
 - G111:** An 8-to-1 multiplexer with inputs `A1`, `A2`, `S1`, `S2`, `S6`, `S5`, `S3`, and `S4`. It has control inputs `B2`, `B1`, and `T5A`. Its output is `X`, which is inverted by `J148` to produce `COL4`.
- Other Inputs:**
 - `F128`, `G100`, `G153`, and `F126` are inputs to the multiplexers.
 - `RES_SYNC` is the clock input for the multiplexers.

7.4

7.5

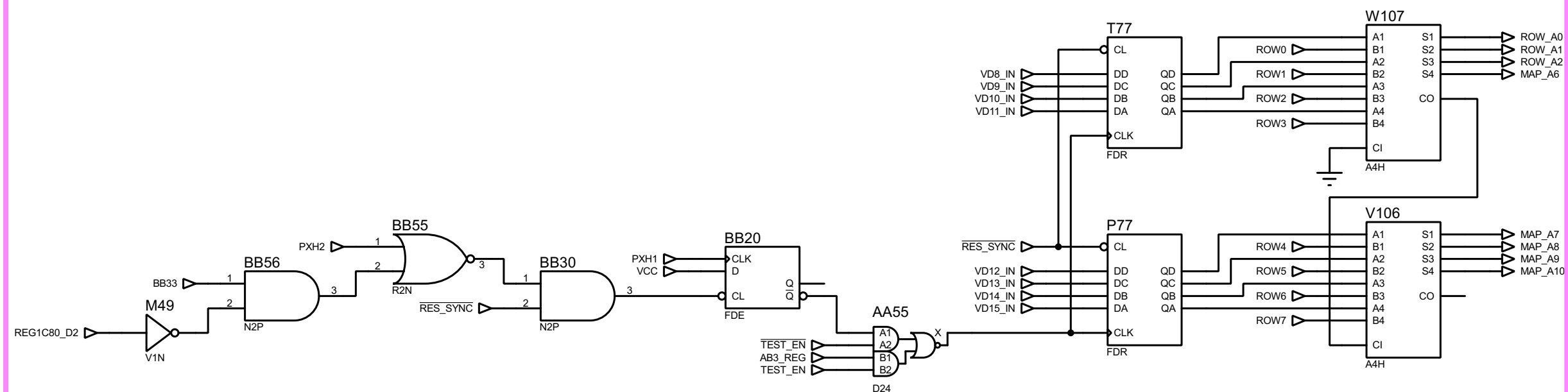
8.1

Layer A tilemap X address gen



8.2

Layer A tilemap Y address gen



FILE NAME: k052109.pdsprj

DESIGN TITLE: Konami 052109
LAYER A SCROLL

BY: Sean Gonsalves

REV: A

DATE: 22/06/2021

PAGE: 8 of 8