Practical 1A

Digital Electronics - Logic Gates and Boolean Laws

Before the practical ensure that you complete the following:

Read and revise:

Chapter 1 and Chapter 2 in the **EEE2046F/EEE2050F course notes**. Please note that the practicals for this course contain a large self-study component and therefore be prepared before the start of the practical.

Bring the following tools to the lab session (see Appendix A.1):[a]

- A breadboard
- Point nose pliers and/or side cutters
- Logic components (HEF4049,HEF4071,HEF4081)

[a] Available from the White Lab store.

1A.1 Introduction

In this practical you will learn to construct digital circuits using 4000 series CMOS logic chips. Additionally, you will simplify Logic Circuits using Boolean Algebra.

You have received the following components at the start of the course, which you can keep for your own use after the practical:

- 1 X CMOS Quad 2-input AND Gate (HEF4081) (**datasheet**)
- 1 X CMOS Quad 2-input OR Gate (HEF4071) (**datasheet**)
- 1 X CMOS Hex buffer inverter (HEF4049) (**datasheet**)

E12 series resistors (see Appendix A.2.1) and capacitors will be available in the Sasol Laboratory for the duration of the practical.

This practical contains both physical experiments as well as a practical report write-up and may take longer than the 2 hour practical session to complete. Please ensure that you take accurate and detailed notes during the physical experiments so that you can compile them into a report after the practical for submission on VULA by the due date.

Please name your practical report as follows:

Prac1A-STUDENTNUMBER1

Call a teaching assistant or tutor if you need assistance at any stage during the practical session and once you have completed the experiments for sign-off.

1A.2 Background: Basic logic gates

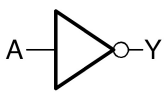
Most real-world signals are continuous or *analogue* in nature and we can describe the behaviour of these variables using continuous mathematical functions. However if we want to represent the value of this signal at some point in time, we approximate and 'encode' the information in its current state using a discrete value or set of symbols. If these values have a finite number of states, the system is known as a *digital* or discrete system. An example of a digital representation is the binary system, which forms the basis of all modern computing. The binary number system provides us with a powerful way to represent information. We can represent any piece of complex information using only a series of 1's and 0's. These binary values can be generated electronically using switches, relays or transistors and therefore form the basis of all modern electrical digital systems. We will examine these basic building blocks in this practical by building basic logic circuits using 4000 series CMOS logic. A *logic gate* is a simple digital circuit used to manipulate logic variables using Boolean algebra. Each gate has one or more inputs and an output.

The state of the output depends on the state of the input(s) and can be described using a *truth table*. A truth table represents all possible output values for any combination of input values. It provides us with a simple graphical representation of the relationship between inputs and outputs for digital circuits.

Input signals to the logic gate are represented by A and B etc., and the output is represented by Y in this course. We will now look at each of the basic logic gates.

1A.2.1 NOT gate

A *NOT gate* has one input A and one output Y. It functions as an inverter, in other words the output is the inverse of the input. If A is TRUE then Y will be FALSE and visa versa. The symbol and truth table for the gate can be seen in figure 1A.1.



(a) NOT gate symbol

Input	Output
A	Y
0	1
1	0

(b) NOT gate truth table

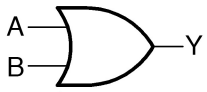
Figure 1A.1: The NOT gate

The NOT operation in Boolean algebra is often represented by a 'bar' above the input. The Boolean equation 1A.2.1 is read as "Y *equals not* A"

$$Y = \bar{A}$$

1A.2.2 OR gate

The *OR gate* is a multi-input, single output gate.[1] The OR gate output is TRUE if any or all of its inputs are TRUE as can be seen in the truth table in figure 1A.2. If all inputs are FALSE, the output will be FALSE.



(a) OR gate symbol

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(b) OR gate truth table

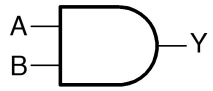
Figure 1A.2: The OR gate

The OR operation in Boolean algebra is often represented by a + sign. The Boolean equation 1A.5 is read as "*Y equals A or B*"

$$Y = A + B$$

1A.2.3 AND gate

The *AND gate* is also a multi-gate, single output gate. The AND gate output is TRUE if and only if all the inputs are TRUE. The output remains FALSE for all other cases as can be seen in the truth table in figure 1A.3.



(a) AND gate symbol

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(b) AND gate truth table

Figure 1A.3: The AND gate

The AND operation in Boolean algebra is represented in a number of ways. The Boolean equation 1A.2.3 is read as "*Y equals A and B*"

$$Y = A \cdot B$$

1A.3 Background: 4000 series CMOS logic gates

Logic gates are constructed using transistors. The arrangement and type of transistor used in the gate construction will determine the electrical characteristics of the logic gates, such as the supply voltage requirements, logic levels, signal switch speeds, propagation times etc. (see pp. 18 to 21 in the **EEE2046F/EEE2050F course notes** for more information). The 4000 series of logic chips were

[1] We will only consider two input gates in this practical, however gates can have more than two inputs and you will need to apply the rules of the basic gates to generate their truth tables and circuits.

originally designed in the 1960's, but are still manufactured today. These logic gates are build with *Complementary Metal-Oxide-Semiconductor* (CMOS) Field Effect Transistors (FETs).

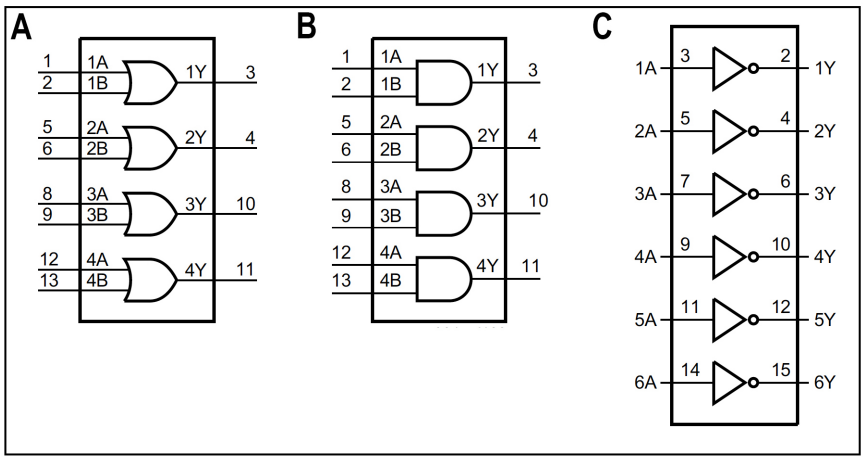


Figure 1A.4: Pin outs for 4000 series CMOS logic chips. (A) Quad 2-input OR-gate (4071); **(B)** Quad 2-input AND-gate (4081); **(C)** Hex buffer inverter (4049). The voltage supply pins for the 4071 and 4081 chips in this figure are V_{DD} (pin 14) and the V_{SS} (pin 7). The voltage supply pins for the 4049 chip are V_{DD} (pin 1) and the V_{SS} (pin 8).Taken from [12–14].

Typically, CMOS logic chips have lower operating currents than Bipolar Junction Transistor based implementations and therefore have lower power consumption. **CMOS chips are highly sensitive to damage from electrostatic discharge (ESD) through their pins, therefore handle the chips with care. Additionally, all unused gates on the chip must have their inputs connected to a known logic state to ensure that their outputs do not drift with input noise.**

1A.4 Setting up

Read through each task carefully and complete the circuit design, construction and question section. Remember to construct your circuits neatly.

1A.4.1 Setting up the breadboard, bench top power supply unit and oscilloscope

We will begin by setting up our breadboard and power supply for our circuits.

1. Set up the bus rails on your breadboard, which will be used as the power supply rails and the logic HIGH and LOW for the circuits. Link the bus rails using a piece of single stranded wire (if required, not all breadboards separate the bus rails along the length of the board). Ensure that the wire is stripped on both ends and is securely fastened in the spring-loaded terminals on the breadboard. Make the connecting wires lie flat to the breadboard so that they are not pulled out accidentally during the practical. Connect the outer top and bottom bus rail as a +5 V rail (**red**), and the two inner bus rails for GND (**black**). Include one 10 nF ceramic decoupling capacitor per rail pair and one 1 μF electrolytic capacitor close to the power supply connections (**(The electrolytic capacitor is polarised and must be connected correctly)**. See Appendix A.3.1 for more details on decoupling capacitors. [2].

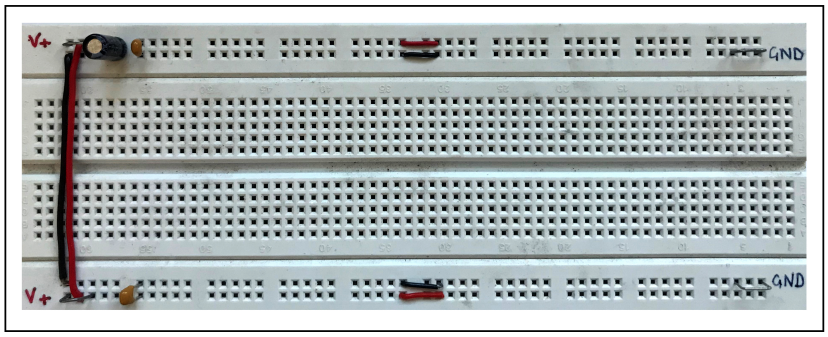


Figure 1A.5: Step 1: The breadboard. Link the bus rail strips using a piece of single stranded wire (if needed). Have two bus rails for +5 V (**red**), and two for GND (**black**).

2. Ensure that you have good connection points on the breadboard to connect the bench top power supply leads. Either secure loops of bare wire or a connect a piece of wire.

3. Switch on your bench top power supply and connect the power supply leads to the power supply unit.

4. Set the output voltage on the bench top supply to +5 V.

5. Now connect the +5 V supply from the bench top power supply unit to your bread board. The red crocodile clip to +5 V and the black crocodile clip to GND.

6. Turn on the oscilloscope. Ensure that your probes are set to 1x and not 10x.

7. Connect the channel 1 probe to the scope. Now connect the channel 1 probe clip and channel 1 probe GND crocodile clip to the test pin on the scope to set your GND level on the display. Ensure that your voltage/division setting on the oscilloscope is correct for measuring the DC voltage over a 0 to +10 V range.

[2]Note that you may use whatever colour wire is available. However, it is good practice to use the same colour wire for the same signal in the circuit.

8. Connect the channel 2 probe to the scope. Now connect the channel 2 probe clip and channel 2 probe GND crocodile clip to the test pin on the scope to set your GND level on the display. Ensure that your voltage/division setting on the oscilloscope is correct.

9. Connect the oscilloscope probe 1 GND crocodile clip to the GND on your breadboard.

10. Connect the oscilloscope probe 1 to the +5 V supply on your breadboard to confirm that it reads +5 V.

11. Disconnect the channel 1 scope probe from your board and switch off the bench top power supply. You are now ready to start building your circuit.

1A.5 Questions and circuit construction

Please answer the following questions in your practical report. All circuit diagrams should be drawn neatly **before you start building you circuit**. Build the circuits on your breadboard, where required, and show the tutor once completed.

Consider the following Boolean equation:

$$Y = (A+B+C)\cdot\left(\overline{A}+C+\overline{A}\cdot(B+C)+(\overline{A}+\overline{B})\cdot C\right)$$

(a) Draw a full circuit diagram of the Boolean equation using 2-input logic gates and include it in your practical report. Assume you only have access to NOT (4049), AND (4081) and OR (4071) gates. Include the chip pin numbers on the gate symbols in your diagram (see figure 1A.4 for pin numbers). Please note that you must use **symbolic** 2-input logic gate symbols in your diagram. Marks will be deducted for messy diagrams. **[16]**

(b) How many logic gates does your circuit use? Name them. **[2]**

(c) How many 4000 series logic chips does your circuit use? Name them. **[2]**

(d) Simplify the equation using Boolean algebra. Show all your workings in your report that you have applied in each step to arrive at the simplified answer. Assume you only have access to 2-input NOT, AND and OR gates. **[10]**

(e) Draw a full circuit diagram of the Boolean equation using logic gates and include it in your practical report. Assume you only have access to 2-input NOT (4049), AND (4081) and OR (4071) gates. Include the chip pin numbers on the gate symbols in your diagram (see figure 1A.4). **[5]**

(f) Now build the circuit on your breadboard using your circuit diagram as reference. Remember to connect all **unused inputs** to a known logic signal, either HIGH (+5 V) or LOW (GND), and to include one 10 nF ceramic decoupling capacitor per chip. Connect the V_{DD} lines to +5 V and the V_{SS} to GND from the bench top power supply unit [3]. Call a tutor and show them your circuit once you are complete.

(g) Draw and complete the truth table for the circuit. Include all possible input combinations in the table. Verify that you circuit produces the same outputs as the truth table. Include a verification table in your report, showing the results of your experiment. **[5]**

[3] Note that DD stands for 'drain' in a FET transistor, if Bipolar Junction Transistors (BJTs) are used in the integrated circuit, the term will be V_{CC} for the 'collector'.

1A.6 Practical Submission

Submit your completed practical report on VULA as a **.pdf**[4] under the correct assignment. Show all your calculations and either take a photo of or scan your circuit diagrams and include them in your report.

Your document must be named as follows so that it is easily identifiable:

Prac1A-STUDENTNUMBER1.pdf

Do **NOT** zip the files together but upload them individually to VULA. Ensure that your name and student number is clearly written in your practical report. Practical reports must be completed and submitted on VULA by 23h55 by the due date on the VULA calendar.

1A.7 Marks Breakdown

Questions	**Marks**
(a)	16
(b)	2
(c)	2
(d)	10
(e)	5
(f)	5
Total	**40 Marks**

Up to 5 marks will be deducted for untidy reports. **5% will be deducted per day for late hand in's for up to one week, after which you will receive 0 and the practical report will no longer be accepted.** Please ensure that you submit the files in the correct place and read the instructions given on VULA with regards to file naming. **NO EMAILED** pracs will be accepted.

[4] **Note** if it is submitted as a **.doc/.docx** or equivalent format file, it will **NOT** be marked.