Practical 3A

Digital Electronics - Combinational Circuits

Before the practical ensure that you complete the following:

Read and revise:

Chapter 2 and 4 in the **EEE2046F/EEE2050F course notes**. Please note that the practicals for this course contain a large self-study component and therefore be prepared before the start of the practical.

Bring the following tools to the lab session (see Appendix A.1):[a]

- A breadboard
- Point nose pliers and/or side cutters
- Logic components (HEF4049,HEF4071,HEF4081,HEF4011)

[a] Available from the White Lab store.

3A.1 Introduction

In this practical you will investigate, design and build basic arithmetic logic circuits using basic logic gates.

You will receive the following components at the start of the practical, which you can keep for your own use after the practical:

- 1 X CMOS Quad 2-input AND Gate (HEF4081) (**datasheet**)
- 1 X CMOS Quad 2-input OR Gate (HEF4071) (**datasheet**)
- 1 X CMOS Quad 2-input XOR Gate (HEF4070)) (**datasheet**)
- 1 X CMOS Hex buffer inverter (HEF4049) (**datasheet**)

E12 series resistors (see Appendix A.2.1) and capacitors will be available in the Sasol Laboratory for the duration of the practical.

This practical contains both physical experiments as well as a practical report write-up and may take longer than the 2 hour practical session to complete. Please ensure that you take accurate and detailed notes during the physical experiments so that you can compile them into a report after the practical for submission on VULA by the due date.

Please name your practical report as follows:

Prac3A-STUDENTNUMBER

Call a teaching assistant or tutor if you need assistance at any stage during the practical session and once you have completed the experiments for sign-off.

3A.2 Arithmetic circuits

There are a number of standard arithmetic operations for binary numbers and as we represent information in logic circuits using binary values, we need to be able to carry out these operations in hardware using standard logic components. These circuits form the basis of the *Arithmetic Logic Unit (ALU)* in the *central processing unit* in a digital processor.

3A.2.1 Addition

Binary addition is fundamental in a digital processor and *adders* are digital circuits which can be used to carry out this arithmetic operation. We will first consider the simplest adders which are designed to add 1-bit binary numbers together followed by multi-bit wide adders with the ability to process carry bits. See Example 3A.1 for an overview of basic binary addition.

Example 3A.1

Add these two unsigned binary numbers together: 1010_2 *and* 0100_2

$$\begin{array}{rcccc} & 1 & 0 & 1 & 0 \\ + & 0 & 1 & 0 & 0 \\ \hline & 1 & 1 & 1 & 0 \end{array}$$

Half Adder:

A *half adder* is a logic circuit which is used to add two 1-bit binary numbers together. It has two binary inputs: A and B and two binary outputs: the sum (S), and the carry out bit (C_{out}) as in figure 3A.1.

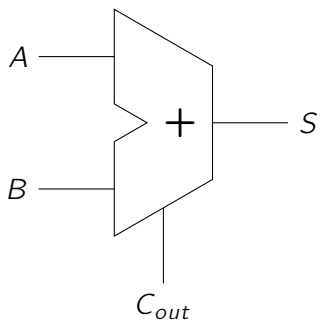

Figure 3A.1: The Half Adder

Full Adder:
We can see that the half-adder circuit is able output the sum of two inputs correctly and produce a carry out bit, however it is unable to incorporate a carry input bit and is therefore known as a half adder circuit. We will now see how we can produce a circuit which can process both the carry in and carry out bits.

The *full adder* has three inputs, one of which is the carry input (C_{in}) and two outputs S and C_{out}. It can be constructed by connecting two half adders together, where the sum output of the first half adder is fed into one input of the second half adder, while the second input of the second half adder is connected to the carry input. It is known as a *carry propagate adder*, which means that the carry output from one bit propagates into the next bit.

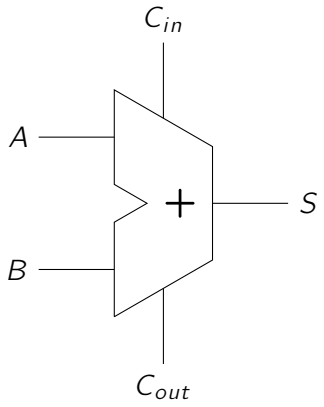

Figure 3A.2: The Full Adder

3A.2.2 Subtraction

We can subtract one binary number from another if we represent the number to be subtracted as its 2's complement.

To convert a number to its 2's complement we need to: (a) invert all bits in the numeral and (b) add one to the result. The output will then be the difference (D) between A and B, and the carry out bit will now represent a borrow in (B_{in}) operation. If the two input numbers are unsigned digits the difference will either be unsigned if ($A \geq B$) or the 2's complement if ($A < B$) and a borrow in operation had to occur.

$$D = \begin{cases} \text{unsigned bit,} & (A \geq B) \\ \text{signed 2's complement bit,} & (A < B) \end{cases}$$

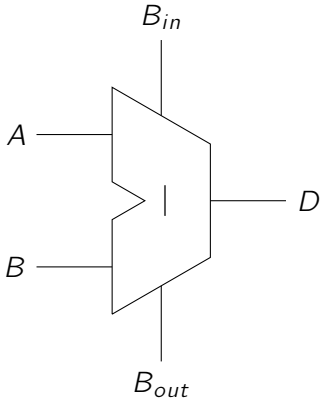

Figure 3A.3: The Full Subtractor

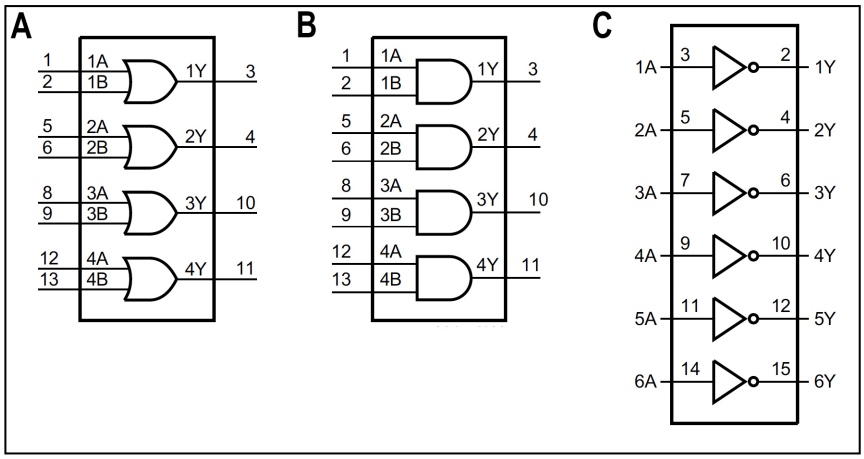

Figure 3A.4: Pin outs for 4000 series CMOS logic chips. (A) Quad 2-input OR-gate (4071); **(B)** Quad 2-input AND-gate (4081); **(C)** Hex buffer inverter (4049). The voltage supply pins for the 4071 and 4081 chips in this figure are V_{DD} (pin 14) and the V_{SS} (pin 7). The voltage supply pins for the 4049 chip are V_{DD} (pin 1) and the V_{SS} (pin 8).Taken from [12–14].

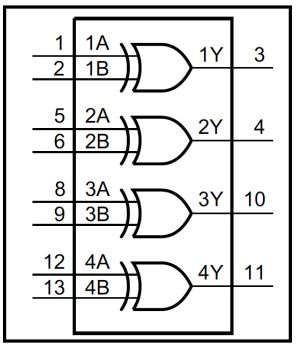

Figure 3A.5: Pin outs for 4070 series CMOS XOR Gate. The voltage supply pins for the 4070 chip are V_{DD} (pin 14) and the V_{SS} (pin 7).

3A.3 Task

In the next section we will design and build basic binary addition circuits on our breadboard, test their performance and answer some questions in your practical report.

Read through each task carefully and then complete the system design, construction and question section. Remember to construct your circuits neatly.

3A.3.1 Setting up the breadboard, bench top power supply unit and oscilloscope

We will begin by setting up our breadboard and power supply for our circuits.

1. Set up the your breadboard as in Practical 1A.
2. Switch on your bench top power supply and set the output voltage on the bench top supply to +5 V.
3. Now connect the +5 V supply from the bench top power supply unit to your bread board.

4. Turn on the oscilloscope and ensure that your setting on the oscilloscope is correct for measuring the DC voltage over a 0 to +5 V range. Check each of your channel probes by connecting them to oscilloscope test pins.

5. Switch off the bench top power supply.

6. You are now ready to start building your circuit.

3A.4 Questions and circuit construction

You will now design a 1-bit half adder and half subtractor, a 1-bit full adder and subtractor circuit and then a 1-bit adder-subtractor circuit. Show all calculations and reasoning in your practical report.

(a) Draw the truth table for a 1-bit half adder with inputs A and B and outputs S and C_{out} circuit in your report. Include all possible input combinations in the table. **[3]**

(b) Write out the Boolean equations for S and C_{out} in terms of the inputs A and B. **[1]**

(c) Draw and complete the truth table for a 1-bit full adder circuit in your report. **[5]**

(d) Find the simplified Boolean equations for S and C_{out} in terms of the inputs A, B and C_{in} from the truth table using Boolean Algebra/Karnaugh Maps. **[2]**

(e) Draw a full circuit diagram of the Boolean equation using 2-input logic gates and include it in your practical report. Assume you only have access to NOT (4049), AND (4081), OR (4071) and XOR (4070) gates. Include the chip pin numbers on the gate symbols in your diagram (see figure 3A.5 for pin numbers). Please note that you must use **symbolic** 2-input logic gate symbols in your diagram. Marks will be deducted for messy diagrams. **[6]**

(f) Draw the truth table for a 1-bit full subtractor in your report. Include all possible input combinations in the table. **[5]**

(g) Find the simplified Boolean equations for D and B_{out} in terms of the inputs A, B and B_{in} from the truth table using Boolean Algebra/Karnaugh Maps. **[2]**

(h) What is the relationship between the full adder and full subtractor circuits? **[1]**

(i) Using the following relationship:

$$B = B \oplus 0$$
$$\overline{B} = B \oplus 1$$

and the relationship determined in (h) design a 1-bit adder/subtractor circuit which has the following **inputs**: A, B, Sel and C_{in}/B_{in} D and **outputs**: S/D and C_{out}/B_{out}. Where Sel is a selection line with the following properties:

Selection	Operation
0	Adder
1	Subtractor

Draw a full circuit diagram of the Boolean equation using 2-input logic gates and include it in your practical report. Assume you only have access to NOT (4049), AND (4081), OR (4071) and XOR (4070) gates. Include the chip pin numbers on the gate symbols in your diagram (see figure 3A.5 for pin numbers). Please note that you must use **symbolic** 2-input logic gate symbols in your diagram. Marks will be deducted for messy diagrams. **[5]**

(j) Now build the 1-bit full adder/subtractor circuit on your breadboard using your circuit diagram as reference. Remember to connect all **unused inputs** to a known logic signal, either HIGH (+5 V) or LOW (GND), and to include one 10 nF ceramic decoupling capacitor per chip. Connect the V_{DD} lines to +5 V and the V_{SS} to GND from the bench top power supply unit. Call a tutor and show them your circuit once you are complete.

(k) Verify that you circuit produces the same outputs as the adder-subtractor circuit described previously. Include a verification table in your report, showing the results of your experiment. **[10]**

3A.5 Practical Submission

Submit your completed practical report on VULA as a **.pdf**[1] under the correct assignment. Show all your calculations and either take a photo of or scan your circuit diagrams and include them in your report.

Your document must be named as follows so that it is easily identifiable:

Prac3A-STUDENTNUMBER.pdf

Do **NOT** zip the files together but upload them individually to VULA. Ensure that your name and student number is clearly written in your practical report. Practical reports must be completed and submitted on VULA by 23h55 by the due date on the VULA calendar.

3A.6 Marks Breakdown

Questions	**Marks**
(a)	3
(b)	1
(c)	5
(d)	2
(e)	6
(f)	5
(g)	2
(h)	1
(i)	5
(k)	10
Total	**40 Marks**

Up to 5 marks will be deducted for untidy reports. **5% will be deducted per day for late hand in's for up to one week, after which you will receive 0 and the practical report will no longer be accepted.** Please ensure that you submit the files in the correct place and read the instructions given on VULA with regards to file naming. **NO EMAILED** pracs will be accepted.

[1] **Note** if it is submitted as a **.doc/.docx** or equivalent format file, it will **NOT** be marked.