Practical 2A

Digital Electronics - NAND Gate representation

Before the practical ensure that you complete the following:

Read and revise:

Chapter 1 and Chapter 2 in the **EEE2046F/EEE2050F course notes**. Please note that the practicals for this course contain a large self-study component and therefore be prepared before the start of the practical.

Bring the following tools to the lab session (see Appendix A.1):[a]

- A breadboard
- Point nose pliers and/or side cutters
- Logic components (HEF4011)

[a] Available from the White Lab store.

2A.1 Introduction

In this practical you will learn to construct digital circuits using 4000 series NAND CMOS logic chips. Additionally, you will simplify Logic Circuits using Karnaugh Maps and NAND gate representation.

You received the following components at the start of the course, which you can keep for your own use after the practical:

- 4 X CMOS Quad 2-input NAND Gate (HEF4011) (**datasheet**)

E12 series resistors (see Appendix A.2.1) and capacitors will be available in the Sasol Laboratory for the duration of the practical.

This practical contains both physical experiments as well as a practical report write-up and may take longer than the 2 hour practical session to complete. Please ensure that you take accurate and detailed

notes during the physical experiments so that you can compile them into a report after the practical for submission on VULA by the due date.

Please name your practical report as follows:

Prac2A-STUDENTNUMBER1

Call a teaching assistant or tutor if you need assistance at any stage during the practical session and once you have completed the experiments for sign-off.

2A.2 Background: Combinational Logic Circuits

A *circuit* is an electrical network or a collection of electrical devices which are connected together in closed loop. We often represent this as a *black box* where the inner workings of the circuit itself are not known, but the circuit's behaviour can be described mathematically or graphically using the relationship between its inputs and outputs over time. A digital circuit is electrical network which processes digital or

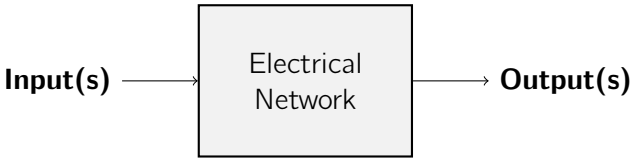

Figure 2A.1: A black box

discrete signals [7]. At its base level it is made up of a combination of various logic gates. These digital circuits are divided into two main groups:

- Combinational circuits
- Sequential circuits

A *combinational circuit's* output is only dependent on the input(s)' value at any moment in time. In other words these circuits are 'memoryless' and their output in the current state does not depend on the value of the output in any previous time period as there is no feedback from the output back to the input in the system. At any point in time the output depends purely on the input(s) to the circuit. If you know or can measure the values of the output for all input combinations you will be able to represent the circuit's behaviour with a truth table. From this we can then *reverse engineer* the circuit or work out what is inside the black box.

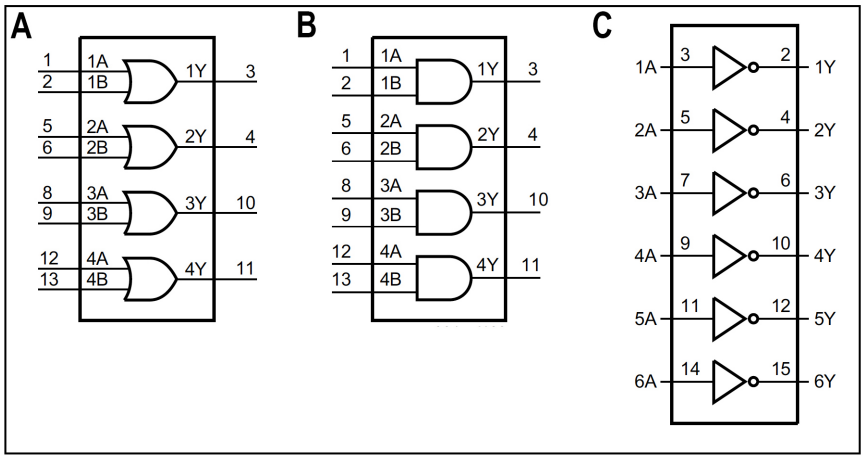

Figure 2A.2: Pin outs for 4000 series CMOS AND, OR and NOT logic chips. (A) Quad 2-input OR-gate (4071); **(B)** Quad 2-input AND-gate (4081); **(C)** Hex buffer inverter (4049). The voltage supply pins for the 4071 and 4081 chips in this figure are V_{DD} (pin 14) and the V_{SS} (pin 7). The voltage supply pins for the 4049 chip are V_{DD} (pin 1) and the V_{SS} (pin 8).Taken from [12–14].

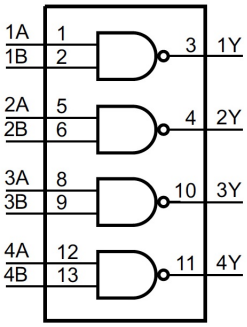

Figure 2A.3: Pin outs for 4000 series CMOS NAND logic chips (4011). The voltage supply pins for the 4011 chip in this figure are V_{DD} (pin 14) and the V_{SS} (pin 7).Taken from [**?**].

In the next section we will build basic combinational logic circuits on our breadboard, test their performance and answer some questions in your practical report.

2A.3 Setting up

Read through each task carefully and complete the circuit design, construction and question section. Remember to construct your circuits neatly.

2A.3.1 Setting up the breadboard, bench top power supply unit and oscilloscope

We will begin by setting up our breadboard and power supply for our circuits.

1. Set up the your breadboard as in Practical 1A.
2. Switch on your bench top power supply and set the output voltage on the bench top supply to +5 V.

3. Now connect the +5 V supply from the bench top power supply unit to your bread board.
4. Turn on the oscilloscope and ensure that your setting on the oscilloscope is correct for measuring the DC voltage over a 0 to +5 V range. Check each of your channel probes by connecting them to oscilloscope test pins.
5. Switch off the bench top power supply.
6. You are now ready to start building your circuit.

2A.4 Questions and circuit construction

A combinational logic circuit can be represented by a Boolean equation. Given the following Boolean equation, complete the following questions:

$$Y = A \cdot B \cdot C \cdot D + \overline{A} \cdot B + A \cdot C + \overline{B} \cdot D + \overline{A} \cdot \overline{C} \cdot D$$

(a) Draw a full circuit diagram of the Boolean equation using 2-input logic gates and include it in your practical report. Assume you only have access to NOT (4049), AND (4081) and OR (4071) gates. Include the chip pin numbers on the gate symbols in your diagram (see figure 2A.2 for pin numbers). Please note that you must use **symbolic** 2-input logic gate symbols in your diagram. Marks will be deducted for messy diagrams. **[8]**

(b) How many 4000 series logic chips does your circuit use? Name them. **[2]**

(c) Draw and complete the truth table for the circuit. Include all possible input combinations in the table. **[9]**

(d) Write out a Boolean equation for the system as a sum of its minterms. **[5]**

(e) Write out a Boolean equation for the system as a product of its maxterms. **[2]**

(f) Simplify the equation using Karnaugh Maps and Boolean Algebra. Show all your workings. **[5]**

(g) Give a NAND Gate only realisation of the **simplified circuit** using De Morgan's laws. Show all your workings. **[5]**

(h) Draw a circuit diagram of the simplified Boolean Equation using 2-input NAND logic gates. Include the pin numbers on the gate symbols in your diagram (see figure 2A.3). Please note that you must use **symbolic** 2-input logic gate symbols in your diagram. Marks will be deducted for messy diagrams. **[5]**

(i) Now build the NAND gate circuit on your breadboard using your circuit diagram as reference. Remember to connect all **unused inputs** to a known logic signal, either HIGH (+5 V) or LOW (GND), and to include one 10 nF ceramic decoupling capacitor per chip. Connect the V_{DD} lines to +5 V and the V_{SS} to GND from the bench top power supply unit. Call a tutor and show them your circuit once you are complete.

(j) Verify that you circuit produces the same outputs as the previous truth table. Include a verification table in your report, showing the results of your experiment. **[9]**

2A.5 Practical Submission

Submit your completed practical report on VULA as a **.pdf**[1] under the correct assignment. Show all your calculations and either take a photo of or scan your circuit diagrams and include them in your report.

Your document must be named as follows so that it is easily identifiable:

Prac2A-STUDENTNUMBER1.pdf

Do **NOT** zip the files together but upload them individually to VULA. Ensure that your name and student number is clearly written in your practical report. Practical reports must be completed and submitted on VULA by 23h55 by the due date on the VULA calendar.

2A.6 Marks Breakdown

Questions	**Marks**
(a)	8
(b)	2
(c)	9
(d)	5
(e)	2
(f)	5
(g)	5
(h)	5
(i)	5
(j)	9
Total	**40 Marks**

Up to 5 marks will be deducted for untidy reports. **5% will be deducted per day for late hand in's for up to one week, after which you will receive 0 and the practical report will no longer be accepted.** Please ensure that you submit the files in the correct place and read the instructions given on VULA with regards to file naming. **NO EMAILED** pracs will be accepted.

[1] **Note** if it is submitted as a **.doc/.docx** or equivalent format file, it will **NOT** be marked.