PLASTIC LOGIC

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Application Note

For Plastic Logic's UC8156 based displays

"Update Modes"

2 Waveform Types

The UC8156 controller is supporting 2 waveform types. Plastic Logic has defined them as:
Type1: "high-quality 4 grey-level waveform" -> update time 0.5sec … 1sec
Type2: "fast 2 grey-level (only black&white) waveform" -> update time 0.2sec … 0.4sec

Waveform Type	Supported grey level	Time needed for an update [1]
Type1	4	0.5sec … 1sec
Type2	2 (black&white only)	0.2sec … 0.4sec

[1] *exact update time is depending on specific waveform design*

Switching between those 2 waveform types can be done using Reg[40h].bit1 (MARS bit):
MARS=0 -> Type1 waveform is selected
MARS=1 -> Type2 waveform is selected

(34) Program WS MTP (Index: 40h) (Default: F0h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Program WS MTP	R/W	PGRS[3:0]				-	-	MARS	PST

Program MTP of Waveform Setting, the contents should be written into RAM before sending this command.

** Don't get confused about the name and description "Program MTP …". This "MARS" bit is also used to decide which waveform inside the MTP is read by the UC8156 controller internally at the beginning of an update.*

The waveform selection using the MARS bit must be done in advance to the update trigger command Reg[14h].bit0 (DWTRG).

In order to trigger the correct update of the waveform from the MTP into the waveform LUT it is necessary to enable the "Read MTP to Update LUT setting" bit which is in (the undocumented) Reg[44h].bit6 -> Reg[44h]=0x60. This needs to be done only once after power-up together with the general register over-writes.

Because the 2GL type2 waveform is optimized for fast updates and not for quality, it is recommended to introduce a 4GL type1 update after 5-10 2GL-type2 update in a sequence depending our your user experience.

“Partial” vs “Normal” update

(21) Display Engine Control Register (Index: 14h) (Default: 00h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display Engine Control Register	R/W	TKV[1:0]		DM[1:0]		TDEN	PART_DISP	WSS	DWTRG

TKV[1:0]: Transparency Key Value.
00:GS0 01:GS1 10:GS2 11:GS3

DM[1:0]: Display Mode Select, these bits select the display mode that is triggered when the DWTRG bit is set(R12H bit0=1b).
00: Full Display Update. The update area of rectangular is defined in R0Ch.
01: Initial Update. The update area of rectangular is defined in R0Ch.
10: Area Display Update. The update area of rectangular is defined in R0Dh.
11: Area Display Update (disable non-select gate line). The update area of rectangular is defined in R0Dh.

TDEN: Transparency Display Enable
0: Transparency Off.
1: Transparency On.

PART_DISP: Partial Display. When Old_data=New_data, the pixel is not updated. The default of the source driver output voltage can be modified by so_other.
0: OFF (Normal Display)
1: Partial Display.

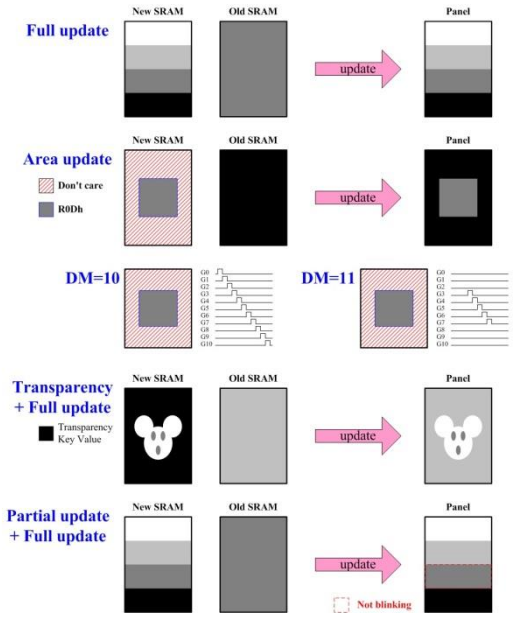
WSS: Waveform source select
0: Read waveform from LUT (R1Ch)
1: Read waveform from MT

DWTRG: Display Write Trigger, This bit can be active only when BUSY_N = “1”. (Write Only)
0: No effect.
1: Triggers a new display operation.

Using the partial mode is compressing the “flickering” during the update for pixels which are not changing their value (e.g. pixel is black in currently displayed image and will stay black at the next image after update as well).
During the use of the partial mode the displays will collect some “ghosting” over several sequential partial update. Therefore it is recommended to introduce a “normal” update (Reg[14h].bit2=0) after 5-10 partial updates depending on your user experience.

Partial update mode can be used combined either with the type1 or type2 waveform update mode (see above).

More information about update modes



The use of the Area Update Mode in combination with “DM=11” is not recommended.