Display Module Datasheet

1.1", 150 ppi,
148x70 pixels

Part-No. 700831

Revision 1

Revision Status	Date	Reason of Modification
1	02-March-2016	Version copied from #700830 and the following changed: - Thickness reduced to 0.46 mm - Product number changed - New drawing -> active border and media overlap added - Updated reference schematic

Contents

1. Introduction

1.1 *Purpose of this document*

This document describes the technical specification of the Plastic Logic 1.1'' display module using the Ultrachip EPD controller/driver UC8156. It defines general characteristics of the display module and the technical information required to integrate the display module into a product.

1.2 *Key features of display module*

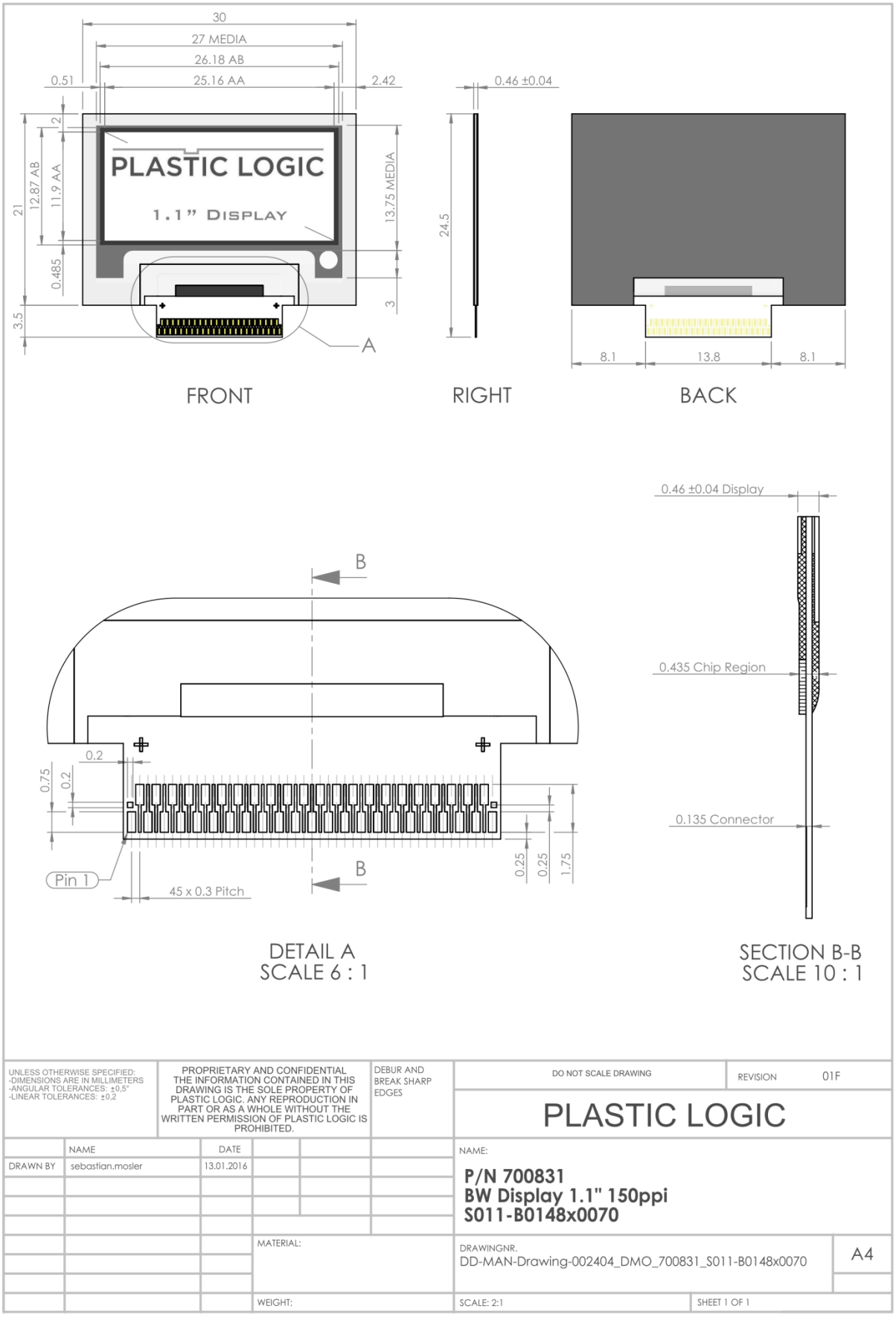
- Consists of an active matrix electrophoretic display which has an integrated EPD controller + source and gate driver IC bonded on the plastic substrate
- Display based on organic TFT active matrix
- 148 x 70 pixels @ 150 ppi equivalent to 170 µm pixel size
- 2 or 4 grey levels
- Incorporates industry-leading bi-stable electrophoretic display technology
- Ultra-wide viewing angle
- Enables robust product design
- Flexible
- SPI interface to customer application

1.3 *General parameters*

Parameter	Value	Comments
Module dimensions	30.0 mm x 24.5 mm	Display with connector
Substrate dimensions	30.0 mm x 21.0 mm	Display without connector
Active screen dimensions	25.16 mm x 11.9 mm	Equivalent to 1.1 inch diagonal
Active/controllable border	0.51 mm	Circumferential
Module thickness	0.460 mm	Tolerance +/-0.040 mm
Active screen resolution	148 x 70 pixels	
Active screen pixel pitch	170 µm (square)	Equivalent to 150 ppi
Bending radius	>= ~30 mm	Depending on product integration
Fully integrated EPD controller/driver	UC8156	Bonded to the plastic substrate (COP)
Surface treatment	Anti-glare, UV protection and hard-coat (2H)	

Table 1: General parameter

2. Mechanical specification – drawing



3. Reliability specifications

3.1 *Maximum ratings*

Parameter	Value	Unit	Comments
Operating Temperature	0 to 40	degC	15%rH to 85%rH*
Storage Temperature Range	-25 to 50	degC	15%rH to 85%rH*

***Longterm exposure of stress close to limits might reduce overall lifetime**

Table 2: Reliability parameters

3.2 *Environmental test conditions*

Test name	Test conditions	Note
HTS – High Temperature Storage	50°C / 23% rH for 240h	(1)
LTS – Low Temperature Storage	-25°C for 240h	(1)
AHS – Advanced Humidity Storage	50°C / 90% rH for 168h	(1)
TST – Temperature Shock Test	-25°C for 30min / 50°C for 30min for 100 cycles	(1)
HTO - High Temperature Operation	50°C for 240h	(1)
LTO – Low Temperature Operation	0°C for 240h	(1)
AHO – Advanced Humidity Operation	40°C / 85%rH for 168h	(1)

Note (1): Functionality and mechanical and optical parameter shall be still satisfied at the end of each test.

4. Electrical interface

4.1 *Connector interface description*

The 1.1'' display has a 45 pad interface which is 2-rows staggered and having a pitch of 0.3mm. Please refer to the detail in the drawing.

Pin/Pad number	Symbol	Purpose	Function
1		Dummy	Keep open
2,3	VSL	Output	Negative source voltage, connect to capacitor
4,5	VSH	Output	Positive source voltage, connect to capacitor
6,7	VGL	Input	Negative gate voltage, input from booster
8,9	VGH	Input	Positive gate voltage, input from booster
10	GDR_P	Output	P-MOS booster gate control
11	GDR_N	Output	N-MOS booster gate control
12,13	GND	Power Supply	Ground
14,15	VDD	Power Supply	Core Logic Power VDD can be regulated internally from VDDA. A capacitor should be connected between VDD and VSS.
16,17	VDDIO	Power Supply	Interface power connect to VDDA for 3.3V I/O, connect to VDD for 1.8V I/O
18,19	VDDA	Power Supply	Analog power
20,21	VPP	Power Supply	MTP programming voltage, keep open if not used
22	SPI_MISO	Output	SPI data output
23	SPI_MOSI	Input	SPI data input
24	SPI_CLK	Input	SPI clock
25	SPI_CS	Input	SPI chip select
26	RST_N	Input	Global reset, low active When RST_N become low, driver will reset. All register will be reset to default value, and all driver functions will be disabled. SD output and VCOM will base on previous condition; and they may have two conditions: 0V or floating.
27	BUSY_N	Output	BUSY pin - indicates the driver status. L: Driver is busy, data/VCOM is transforming. H: non-busy. Host side can send command/data to driver.
28	IRQ	Output	Host interrupt pin
29	GPIO_3	I/O	Programmable general purpose I/O pin can be used to connect an external I²C temperature sensor
30	GPIO_2	I/O	Programmable general purpose I/O pin can be used to connect an external I²C temperature sensor
31	GPIO_1	I/O	Programmable general purpose I/O pin
32,33,34	VDD	Power Supply	Core Logic Power VDD can be regulated internally from VDDA. A capacitor should be connected between VDD and GND.
35,36,37	VDDA	Power Supply	Analog power
38	EXTVDD	Input	Controls internal regulator for VDD EXTVDD connected GND: internal regulator is on. EXTVDD connected VDDA: internal regulator is off, need an external 1.8V supply to VDD.
39,40,41	GND	Power Supply	Ground
42,43,44	TPCOM	Output	Test pin, connect to capacitor
45		Dummy	Keep open

Table 3 – Pin list

Note1: Refer to the display drawing for Pin/Pad 1 orientation.

Reference connector type:

Omron XF2B4545-31A, rotary back lock connector, 0.3mm pitch, dual contact

4.2 *Controller*

The display is driven and controlled by the UC8156 which is an all-in-one EPD driver and timing controller from Ultrachip. This chip is bonded to the Plastic Logic display substrate via a new bonding technology called “Chip on Plastic” (COP).

The UC8156 supports up to 4 grey level per pixel. The timing controller provides control signals for the source and gate drivers.
The DC-DC controller allows it to generate the source output voltage VSH/VSL (+/-8~+/-15V). The chip also includes an output buffer for the supply of the COM electrode (AC-VCOM or DC-VCOM). The system is configurable through a 3-wire/4-wire SPI serial interface.

Feature highlights:

- System-on-chip (SOC) for EPD displays
- Support up to 240(sources)x160(gates) @ 300Hz
- Up to 2-bit greyscale waveforms (4 level grey-shades)
- Source driver: VSL -8 to -15V, VSH +8 to +15V
- Gate driver: VGL -20 to -27V, VGH +15 to +22V
- DC VCOM: -4V to +10V with a 30mV resolution
- AC VCOM: VCOML=VSL + VCOM_DC or VCOMH=VSH + VCOM_DC
- Individual switches for power supplies.
- Transparency write support
- Built-in temperature sensor
- Supports external LM75 Digital Temperature sensor and compatible devices
- MTP Memory for Waveform storage
- Power Management Integrated Circuit (PMIC)
- Serial peripheral interface (3-wire/4-wire SPI)
- Built-in Frame memory (Max.): 240x160x2bitx2
- Support UT1 waveform format
- IO interface supply voltage:1.7~ 3.6V
- Operation frequency: 60Mhz (max)
- Operating temperature range -30°C to 85°C
- Package: COG, COP (COF compatible)

Please refer to Ultrachip UC8156 datasheet for the full controller specification.

4.3 *Application reference circuit*

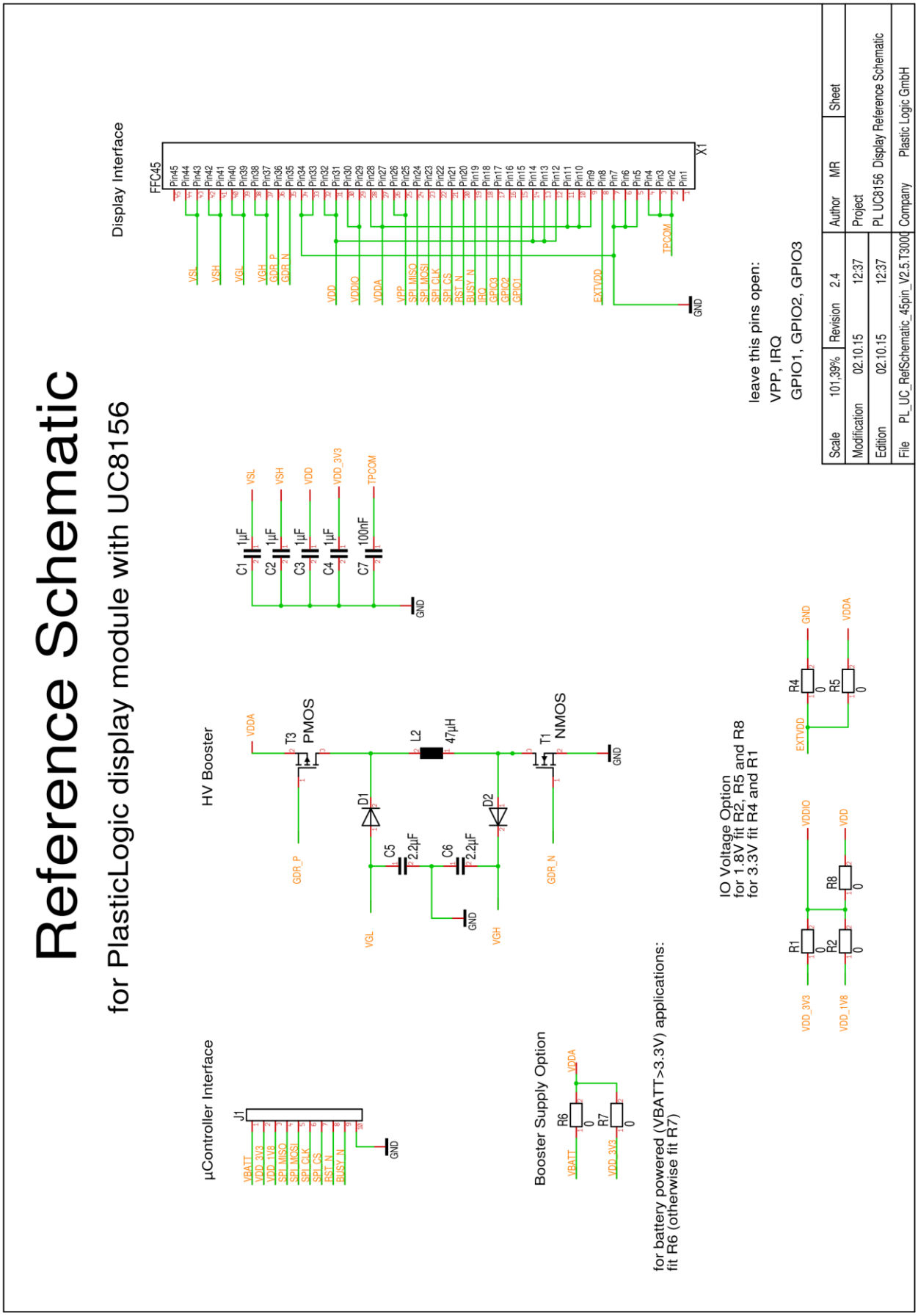


Figure 1 - Application reference circuit

5. Optical and electrical specification

5.1 *Waveform and update time*

The update time is very much dependent on the waveform design. It might vary based on:

- Number of grey level
- Expected optical performance (contrast, ghosting, etc.)

Temp [°C]	>15	10-15	5-10	0-5
typical update time [sec]	<0.9	<2.0	<2.5	<3.5

Table 4: Typical update time

Note: "Update time" is complete BUSY high time

5.2 *Optical parameter*

Parameter	**Symbol**	**Minimum**	**Typical**	**Maximum**	**Unit**
Reflectance White	R_w	30	38 … 41		%
Contrast Ratio	CR	5:1	8:1 … 10:1		
Ghosting			<1	2	L*

Table 5: Optical parameter

Note: The reflectance and contrast ratio is measured between 0ºC and 40°C at 50%rH. Reflectance measurements are done using a spectrophotometer. Plastic Logic is using the "spectro guide" from BYK-Gardner GmbH.

5.2.1 Ghosting measurement method

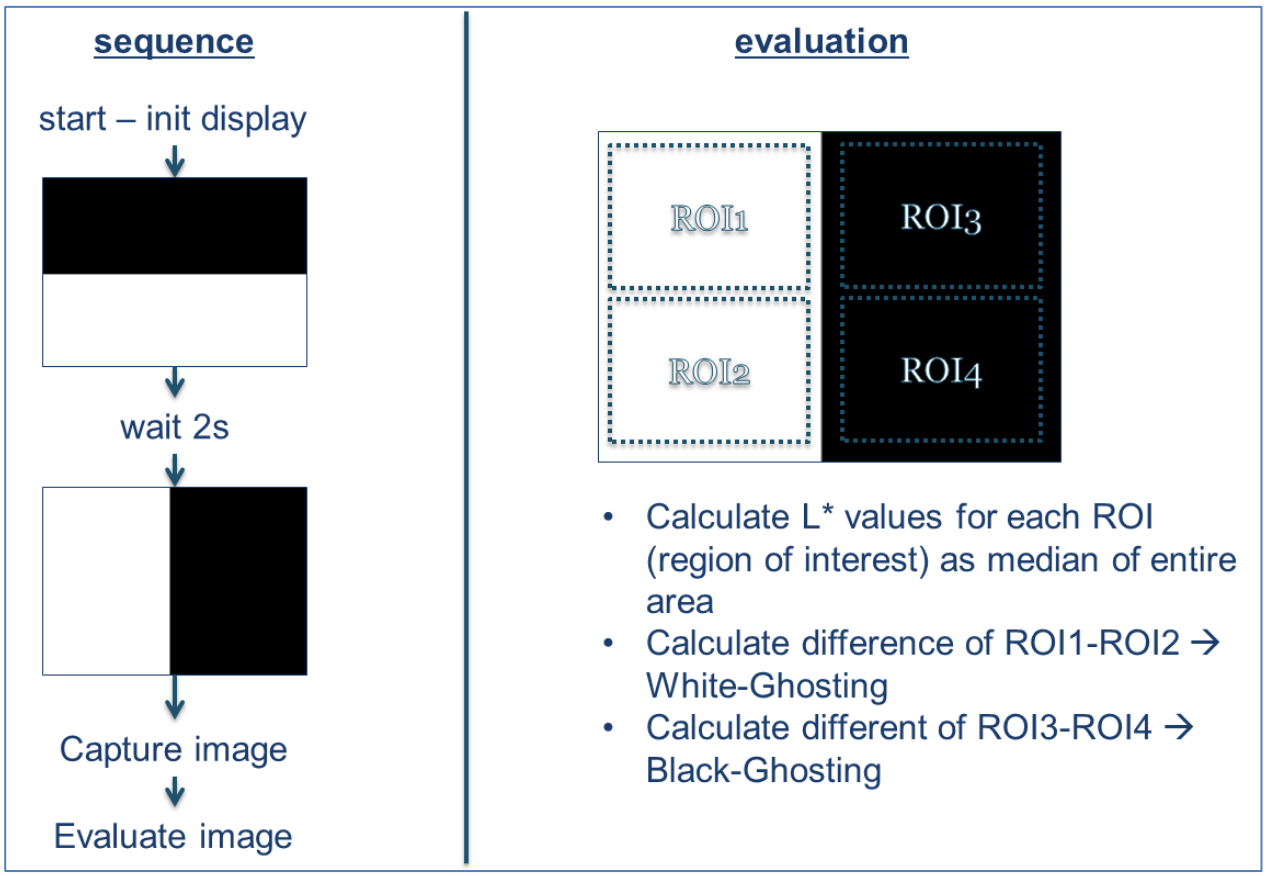


Figure 2 - ghosting measurement method

5.3 *Display power consumption*

Mode	Parameter	Minimum	Typical	Maximum	Unit
Operation (during update)	Mean current for “typical” image update		3..5		mA
Operation (during update)	Mean current for a “worst case” image update		6..7	8	mA
Operation (during update)	Peak current		35..40	50	mA
Stand-by with HV’s on	Stand-by current 1		600..700		µA
Stand-by with HV’s off	Stand-by current 2		38..40		µA
Sleep	Sleep current		7..8		µA

Table 6 – Display power consumption

Note (1): see detailed conditions, measurement setup and value calculation below
Note (2): peak duration <1ms

Power consumption is very much depending on the finally implemented waveform.

5.3.1 Conditions

1) "Worst case" image = Stripe Pattern

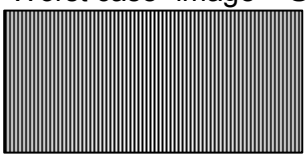


Figure 3 – "Worst case" image used for power consumption measurement

2) "Typical" image = Stripe Pattern

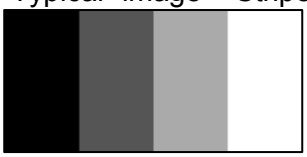


Figure 4 – "Typical" image used for power consumption measurement

3) Room temperature conditions (ca. 23°C + 50%rH)
4) Latest register settings and operation sequence used. Waveform and VCOM value is already programmed into controller internal memory.

5.3.2 Measurement setup

For the current measurement a 0.5Ohm shunt resistance were soldered into the 3.3V power supply line. The voltage drop over the shunt resistance is measured using Keithley DMM K3706 within production test or an Oscilloscope for analysis.

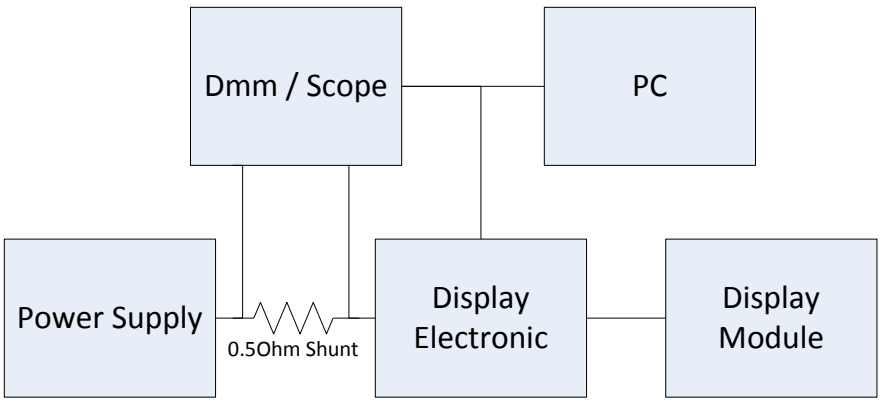


Figure 5 - Measurement Setup

5.3.3 Value calculation for mean power

- The "input current" value is calculated as average value over the whole update (approx. BUSY high time). Sample rate is 1kHz, so ~1000 measurement values are averaged.
- The given value includes the consumption of the display and the complete external display related electronic (HV generation).

6. Visual parameter

6.1 *Defects*

- No line-outs
- 99.99% functional pixel

7. Handling requirements

- Please assemble or install the displays in a clean working area.
- Take appropriate care to protect the rear side of the display module from indents and punctures as this may damage the display.
- The display module is an electrostatic discharge (ESD) sensitive device. Ensure proper ESD precautions are in place to avoid damage to the display module. Take care on grounding (e.g. wrist straps) maybe use Ion fans.
- Please handle the display with care during assembly. Do not over-bend and twist the display. Protect especially the COP (chip on plastic) region and the FPC bonding connection.
- Do not connect or disconnect the display from the interface connector while power is on (no “hot-plugging”).
- Do not stack the displays.

8. Safety and Flammability requirements

The integrator of this display module into a final product is responsible for ensuring that the relevant safety and flammability requirements are me