

| Operation   | Operator<br>VHDL                                   | Verilog                                  |
|---|--|--|
| <b>Arithmetic Operators</b><br>exponential<br>multiplication<br>division<br>addition<br>subtraction<br>modulus<br>remainder<br>absolute value                         | <br>**<br>*<br>/<br>+<br>-<br>mod<br>rem<br>abs    | <br><br>*<br>/<br>+<br>-<br>%            |
| <b>Unary Arithmetic (Sign) Operators</b><br>identity<br>negation  | <br>+<br>-   | <br>+<br>-                               |
| <b>Relational Operators</b><br>less than<br>less than or equal to<br>greater than<br>greater than or equal to   | <br><<br><=<br>><br>>=                             | <br><<br><=<br>><br>>=                   |
| <b>Equality Operators</b><br>equality<br>inequality   | <br>=<br>/=  | <br>==<br>!=                             |
| <b>Logical Comparison Operators</b><br>NOT<br>AND<br>OR   | <br>not<br>and<br>or                               | <br>!<br>&&<br>                          |
| <b>Logical Bit-wise Operators</b><br>unary negation NOT<br>binary AND<br>binary OR<br>binary nAND<br>binary NOR<br>binary XOR<br>binary XNOR                          | <br>not<br>and<br>or<br>nand<br>nor<br>xor<br>xnor | <br>~<br>&<br> <br><br><br>^<br>^~ or ~^ |
| <b>Shift Operators</b><br>logical shift left<br>logical shift right<br>arithmetic shift left<br>arithmetic shift right<br>logical rotate left<br>logical rotate right | <br>sll<br>srl<br>sla<br>sra<br>rol<br>ror         | <br><<<br>>><br><<<<br>>>>               |
| <b>Concatenation &amp; Replication Operators</b><br>concatenation<br>replication  | <br>&  | <br>{ }<br>{ { } }                       |
| <b>Reduction Operators</b><br>AND<br>OR<br>NAND<br>NOR<br>XOR<br>XNOR   |  | <br>&<br> <br>~&<br>~ <br>^<br>^~ or ~^  |
| <b>Conditional Operator</b><br>conditional  |  | ? :                                      |